A new approach to maximum drain current rating for QFN packages

Cu clip packages (3.3x3.3, 5x6, 8x8, sTOLL)

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About this document

Scope and purpose

This application note explains the new methodology used for continuous current (I_D) and pulsed drain current ($I_{D,pulse}$) rating on the datasheet (DS) of Power QFN (3.3 x 3.3, 5 x 6, 8 x 8 and sTOLL) products that use a copper (Cu) clip to connect the Silicon die to the package leadframe. The conditions for the drain current calculations are specified. This application note explains the need for this new approach and highlights the assumptions used. Impact of the new I_D rating on the DS parameters and graphs is included. The test set-up and experimental results are shown. The new limit provides significantly improved I_D rating. Guidance on MOSFET selection is provided, focusing on the junction to ambient/PCB thermal resistance and the de-rating due to temperature.

Intended audience

Power electronics engineers, component engineers; applicable to all applications that use PQFN parts where high current inrush events influence MOSFET selection.

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1 Introduction

The datasheet current limit is one of the most important parameters for applications like motor drives, especially in the present context with low-voltage drives, where motor stall and braking scenarios result in very high currents through the MOSFETs. It is also critical for Battery Management Systems (BMSs), where it is used as a battery protection switch during inrush and/or short-circuit protection. A fair comparison and capability assessment of the product is necessary for successful part selection.

The 5 x 6 PQFN or Super S08 is one of the most popular surface mount packages. It is compact in size with no leads and the Cu clipped version has additional benefits compared to wirebond (aluminum (Al) or copper) counterparts such as low profile, low package parasitics (inductance and resistance) and improved thermals. This enables products with ultra low on-state resistance $R_{DS(on)}$ especially for low-voltage MOSFETs (less than 200 V). This combination of Cu Clip and lower $R_{DS(on)}$ improves the continuous current carrying capability (I_D rating). That is the focus of this application note.

In this application note we will discuss the changes in the methodology to calculate the I_D rating. The impact on the DS parameters is shown, in both tables and graphs. Changes in I_D rating also influence the pulse current rating. To verify the performance an experimental set-up was created. The test set-up and the results are discussed in the later sections. Pre- and post-test parametrics (both static and dynamic) are compared to quantify the shifts before and after the tests. The actual test conditions are mapped onto the SOA diagram to show the screening effectiveness.

This method is applicable to all Cu clip products (3.3 x 3.3, 5 x 6 PQFN) and can be expanded to other packages like 8 x 8 PQFN as long as they use a Cu clip to connect the silicon (Si) chip to the lead-frame as illustrated in Figure 1 for a 5 x 6 PQFN. This I_D rating change is then discussed in the real application context where $R_{thJ\text{-}C\text{-}PCB}$ and $R_{thJ\text{-}ambient}$ must be considered. This will help users with the appropriate part selection.

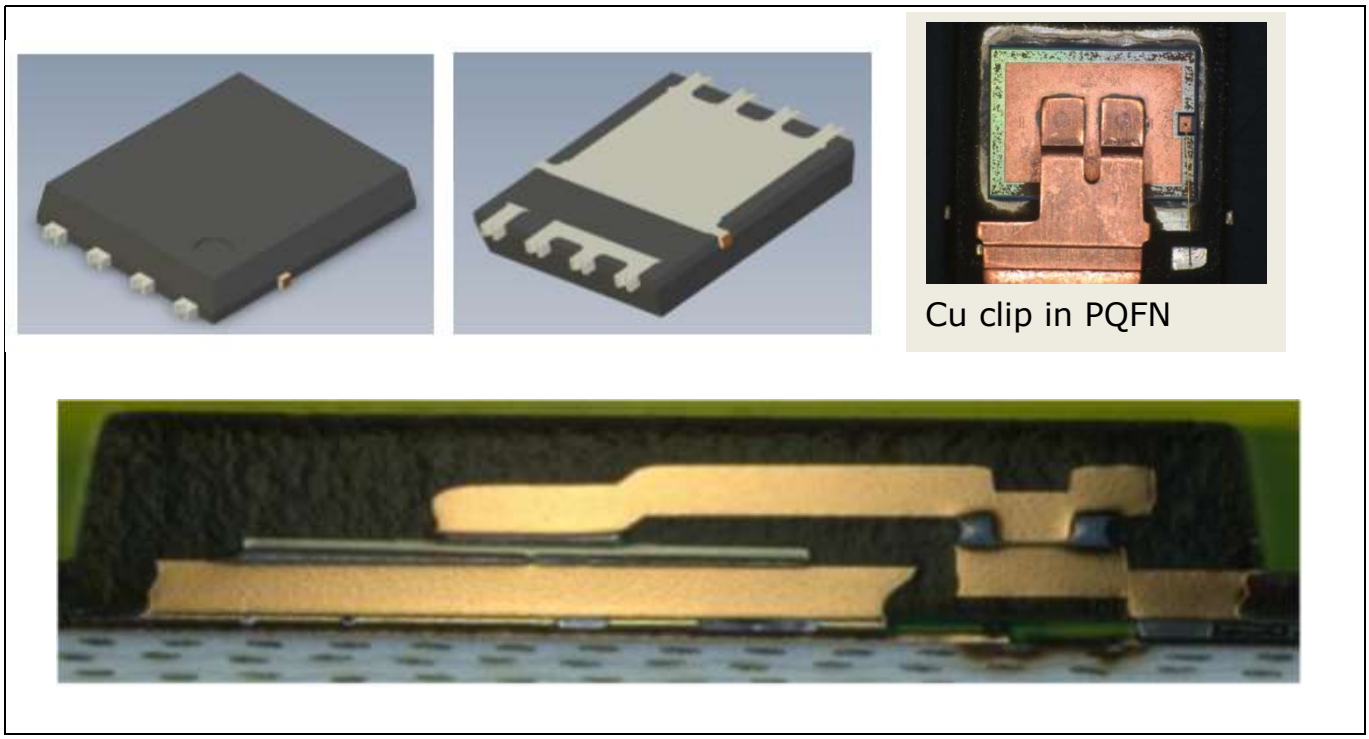


Figure 1 5 x 6 PQFN package and internal construction

2 Change in the I_D rating methodology

2.1 Rationale behind the change

Historically, the 3.3 x 3.3 and 5 x 6 PQFN package I_D rating was limited to 40 A and 100 A respectively. There were multiple aspects to this lower I_D rating. This rating was based on certain assumptions such as a board temperature of 85°C, and the chip temperature that was set to T_{Jmax}, typically 150°C. The maximum temperature along the Cu clip/mold was not to exceed 220°C as limited by the glass transition temperature of the mold compound. The same methodology was used for both plastic packages such as D^2PAK, DPAK, etc. and PQFNs [1, 2]. The case for PQFNs is interesting as it uses a Cu clip instead of the wire bonds and hence the package can in theory carry much higher current than the wire bonds. In addition, there were also tester current capability limitations at final test screening. For these reasons a very conservative rating was derived. This rating was sufficient when the product $R_{DS(on)}$ was high enough such that the product was limited by the Si chip current rating. With the latest sub mΩ on-state resistance products, a fresh look at the assumptions is warranted.

2.2 Understanding the new method and assumptions (footnote)

Internal components of the PQFN product to understand the components responsible for heat transfer and current capability calculations:

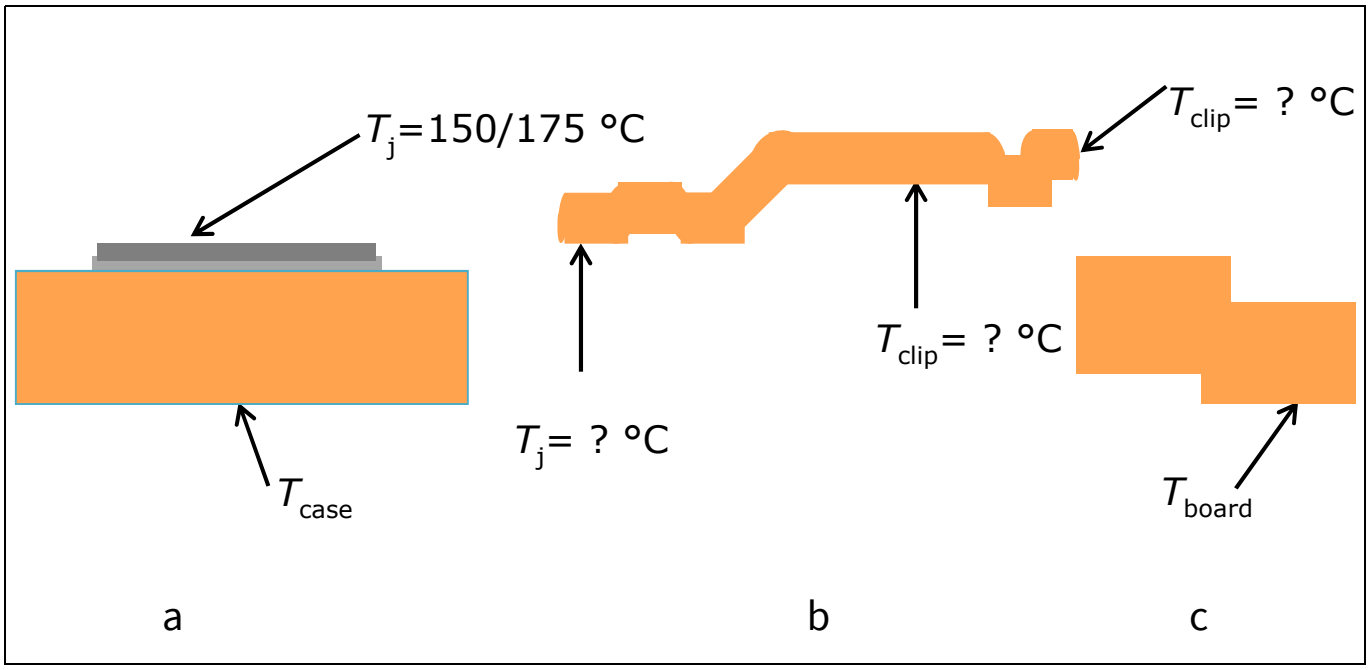


Figure 2 Explaining the new approach

There are actually three components that can limit the current rating of this product. Thermal calculations can be divided into three sections.

a. Silicon limit: Uses max. on-state resistance, max. thermal resistance R_{thJC}, and I_D is calculated until $T_j = T_{jmax}$.

$$I_D(T_C) = \sqrt{\frac{\frac{T_j - T_C}{R_{thJC}}}{R_{DS(on),Tj(\max)}}}$$

b. Cu clip limit: Based on a given junction temperature T_j calculate the clip temperature using heat transfer along the clip until the clip reaches 220°C.

c. Post/leads limit: Calculate current until the post reaches a maximum temperature of 220°C.

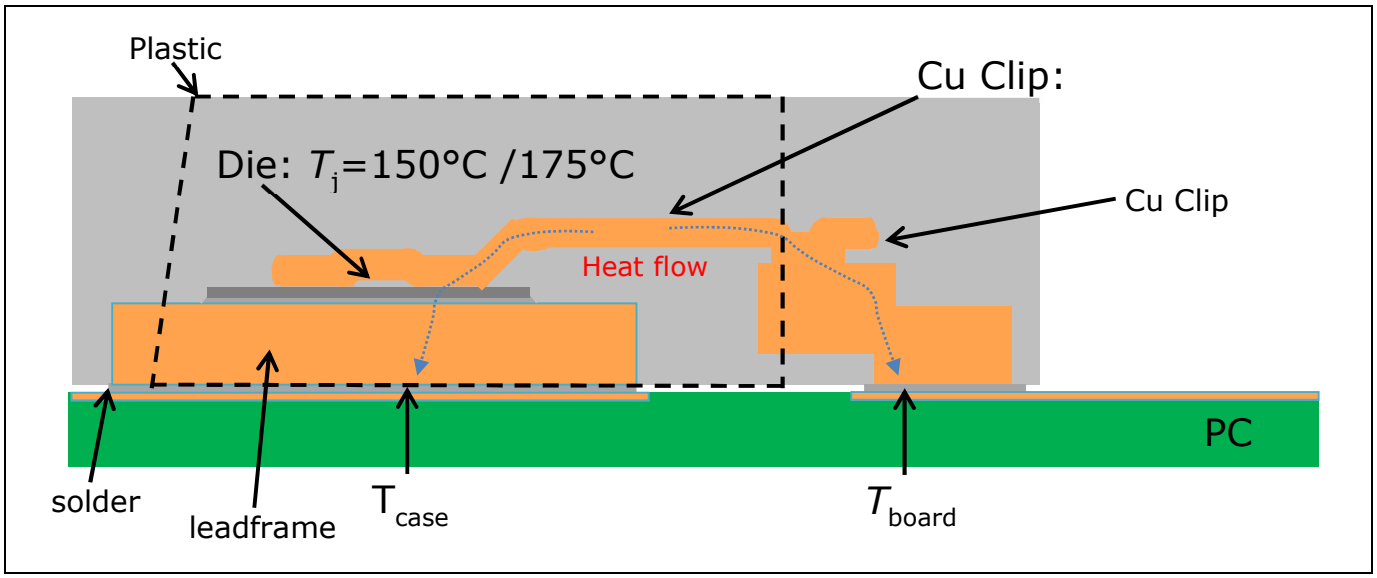


Figure 3 Package internal heat flow path

In the nominal case, board temperature and case temperature are both set to 25°C. For the package limit the maximum temperature should not exceed a maximum value, where we keep a limit of 220°C. As shown in Figure 3, heat flows either from the chip or the clip to the case or to the board. First we calculate the magnitude of current needed to reach a given junction temperature in the chip. This is represented by dashed lines in Figure 4. In the second phase the amount of current needed to reach 220°C along the clip or lead is calculated as represented by solid lines in Figure 4 for various board/junction temperatures. The calculations here are done for the OptiMOS™ product BSC010N04LS with $R_{DS(on)MAX}$ of 1 mΩ. The clip/lead can handle significantly higher current compared to the Si chip, as shown in Figure 4. For example, a case temperature of 25°C and a current of 282 A increase the junction temperature to 150°C (marked by a blue dot in Figure 4). On the other hand, even with a board temperature (temperature at the source lead) of 150°C and a junction temperature of 150°C, the clip reaches its maximum temperature of 220°C only at 386 A (marked by a red dot in Figure 4).

The I_D rating is defined by the lower one of the two values. Unless the clip is significantly smaller than the die, the main limitation for the I_D rating is given by the Si chip. Further details of this approach when applied to other SMD plastic packages (e.g. D^2PAK, DPAK, etc.) can be found in Ref [3]. I_{Dpulse} is calculated by the same formula as before and is typically four times the continuous I_D rating [2].

This new rating is mainly limited to the product while maintaining the case and board temperature at a given condition with a nominal value of 25°C. It does not require taking into account the $R_{thJ\text{-}PCB}$ and is therefore independent of the environmental conditions. For higher temperatures de-rating is required. This is also highlighted in the footnote in the datasheet. In many cases, there might also be restrictions from other components which limit the current carrying capability.

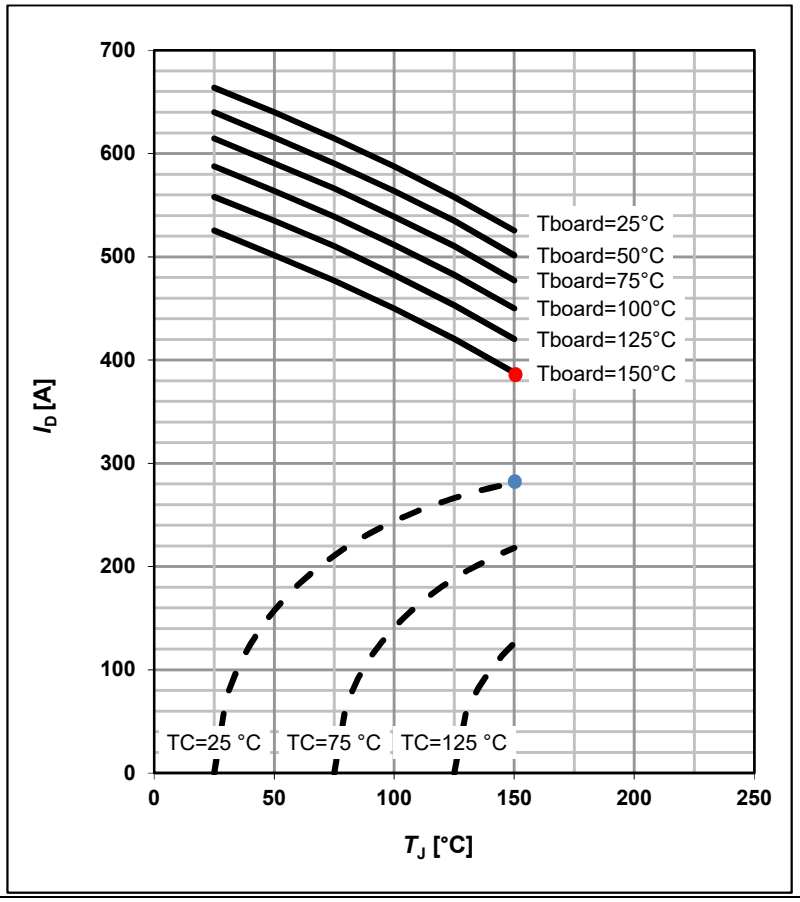


Figure 4 Graphical representation of the new methodology for PQFN

3 Impact on the datasheet parameters

3.1 Changes in the tables

One of the major changes in the datasheet is the continuous and pulsed drain current rating as shown in Table 1, below. To compare the old vs new methodlogy, best in class Infineon product BSC010N04LS, a 40 V 1 mΩ max. OptiMOS™ 5 device in a 5 x 6 PQFN package, was selected. This part has a max. R_{thJC} of 0.9°C/W. The new I_D value is based on the methodology described in the previous section, where T_{CASE} and T_{BOARD} are both maintained at 25°C. With ideal cooling the product is capable of much higher currents: 282 A (NEW) vs. 100 A (OLD). When derated at higher case temperatures, as shown in the table below e.g. at 100°C, the new I_D rating is 178 A vs. 100 A for the old. In addition, the pulsed current rating is also improved to 1128 A (NEW) vs. 400 A (OLD). Note that the change is mainly in the methodology of assessing the product current capability and no internal physical changes have been made to the Si chip, package construction and/or the interfaces.

Table 1 Comparison of drain current with old method vs. new method (BSC010N04LS)

Parameter	Symbol	Max. value (OLD)	Max. value (NEW)	Test condition
Continuous drain current	I_D	100 A	282 A	V_{GS} = 10 V, T_C = 25°C
		100 A	178 A	V_{GS} = 10 V, T_C = 100°C
		38 A	38 A	V_{GS} = 10 V, T_A =25°C, R_{thJA} = 50°C/W
Pulsed drain current	$I_{D,pulse}$	400 A	1128 A	T_C = 25°C

A similar methodology is applied to diode performance, as shown in Table 2, below. The diode current is lower than the MOSFET (channel) current as the power dissipation is higher due to higher forward voltage drop. The pulse rating is still maintained similar to the MOSFET as this is a short-duration (few µs) pulse.

Table 2 Comparison of diode performance with old method vs. new method (BSC010N04LS)

Parameter	Symbol	Max. value (OLD)	Max. value (NEW)	Test condition
Diode continuous forward current	I_S	100 A	139 A	T_C = 25°C
Diode pulse current	$I_{S,pulse}$	400 A	1128 A	T_C = 25°C
Diode forward voltage	V_{SD}	1 V	1 V	V_{GS} = 10 V, I_F = 50 A, T_j = 25°C

3.2 Changes in the graphs

The new methodlogy calls for datasheet changes for three curves: Drain current vs. case temperature, the Safe Operating Area (SOA), and in some cases, the diode current chart. Figure 5 shows the old vs. new drain current vs. temperature plot. In the old method the current was limited to 100 A with a steep decline at high temperature. With the new method, the product capability at room temperature is high and shows a gradual decline as the case temperature is increased. This also suggests the need for better cooling as lower case temperature enables higher currents.

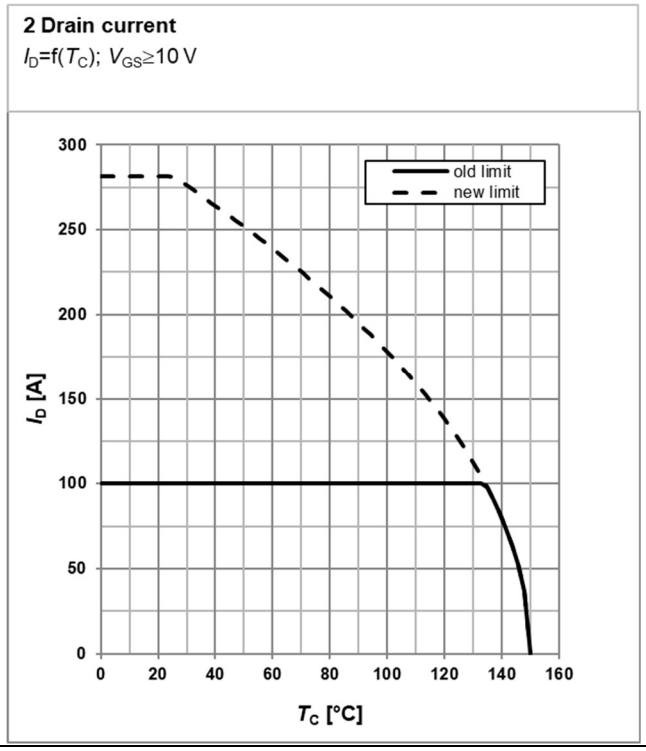


Figure 5 Old vs. new continuous current rating (BSC010N04LS)

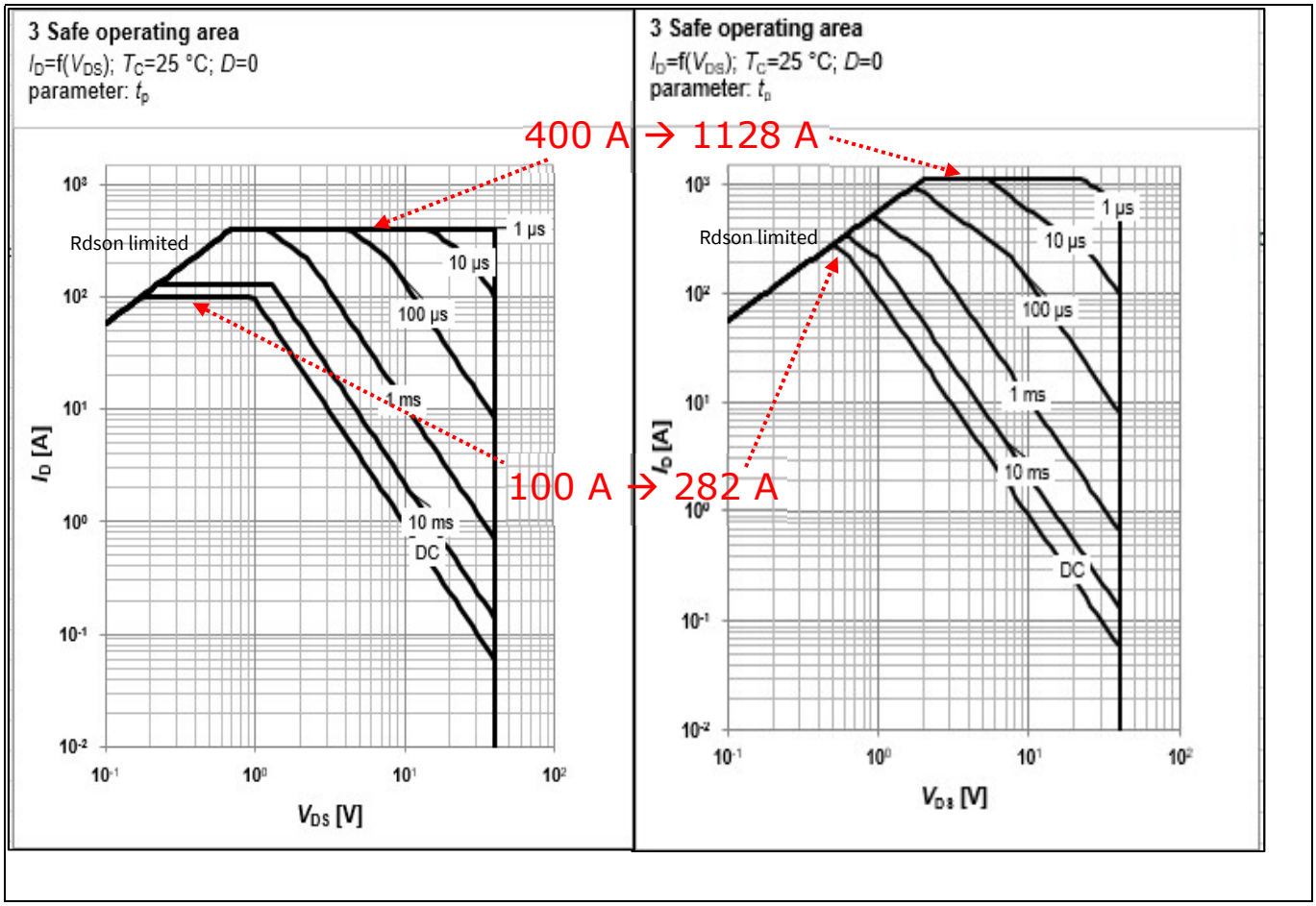


Figure 6 Old (left) vs. new (right) SOA diagram (BSC010N04LS)

Impact on the datasheet parameters

The SOA diagrams for the old vs. new methods are shown in Figure 6. An explanation of how to read the SOA diagram and various regions on the SOA diagram can be found in [4]. The $R_{DS(on)}$ limit line remains the same between the two methods. Due to the increase in continuous and pulsed I_D rating, the intersection of the power line limit to the $R_{DS(on)}$ limit line improves significantly. The flat portion of the DC and the 10 ms curves for this particular device altered. For the DC-line, due to high I_D, the thermal stability line directly approached the $R_{DS(on)}$ limit line. As the pulsed current is high, even the 1 µs line at high V_{DS} is limited by power. De-rating is necessary if the starting temperature is higher than room temperature, as explained in [4].

Where applicable, in updated datasheets the diagram showing the forward voltage drop of the intrinsic reverse diode is extended to higher pulse currents.

4 Experimental verification

4.1 Test set-up

The schematic of the test set-up is illustrated in Figure 7. The high-side MOSFETs (driver MOSFETs, four in parallel Q1 to Q4) are low on state resistance devices with sufficient breakdown voltage, higher than the supply voltage. Multiple MOSFETs are used in parallel to reduce the ohmic losses and the power dissipation. These MOSFETs are pulsed with a predetermined frequency (5 to 10 Hz). The low-side MOSFET is the Device Under Test (DUT). The DUT is always kept in an on-state to avoid switching losses. Since the high-side MOSFETs are switched they incur switching losses and in some cases they also experience an avalanche event. Care must be taken to size the top-side MOSFETs properly to avoid avalanche failures. This is also one of the main reasons to use multiple MOSFETs in parallel. Power supply selection is critical as it must be capable of providing up to 2000 A current for 10 s of µs. The main motivation of this test set-up was to evaluate and verify the new I_{Dpulse} values.

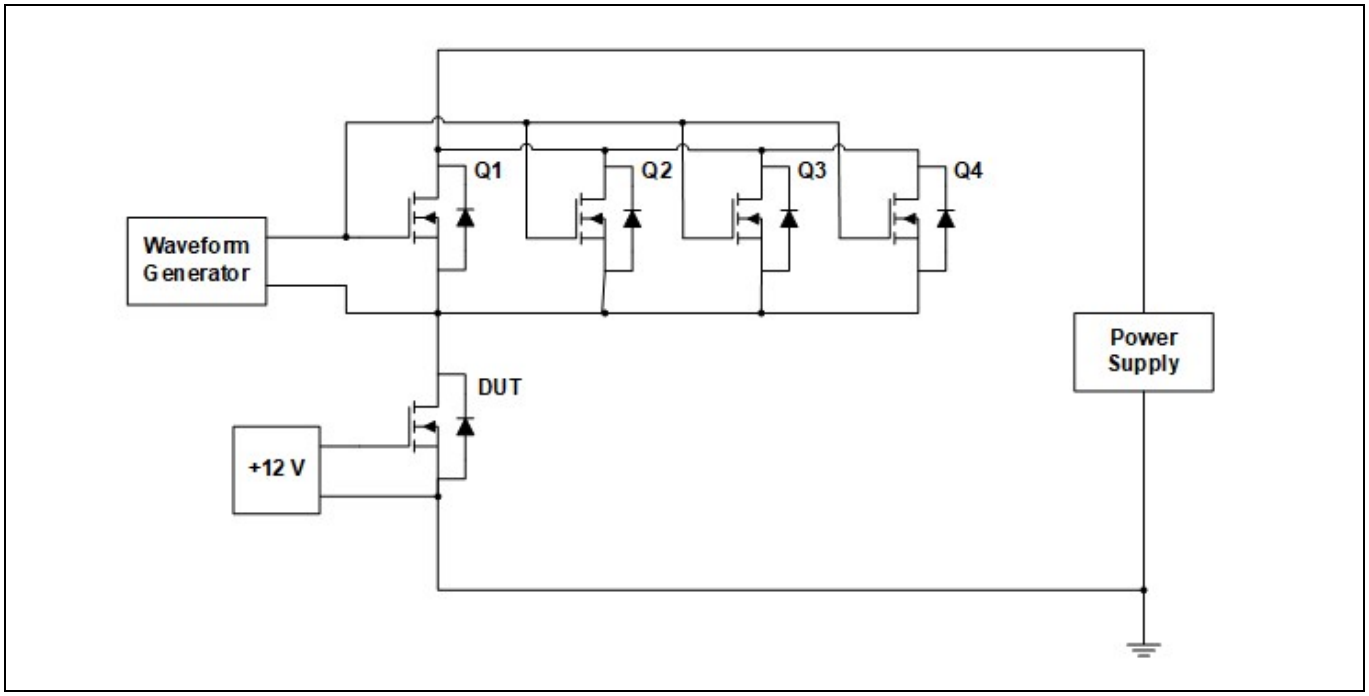
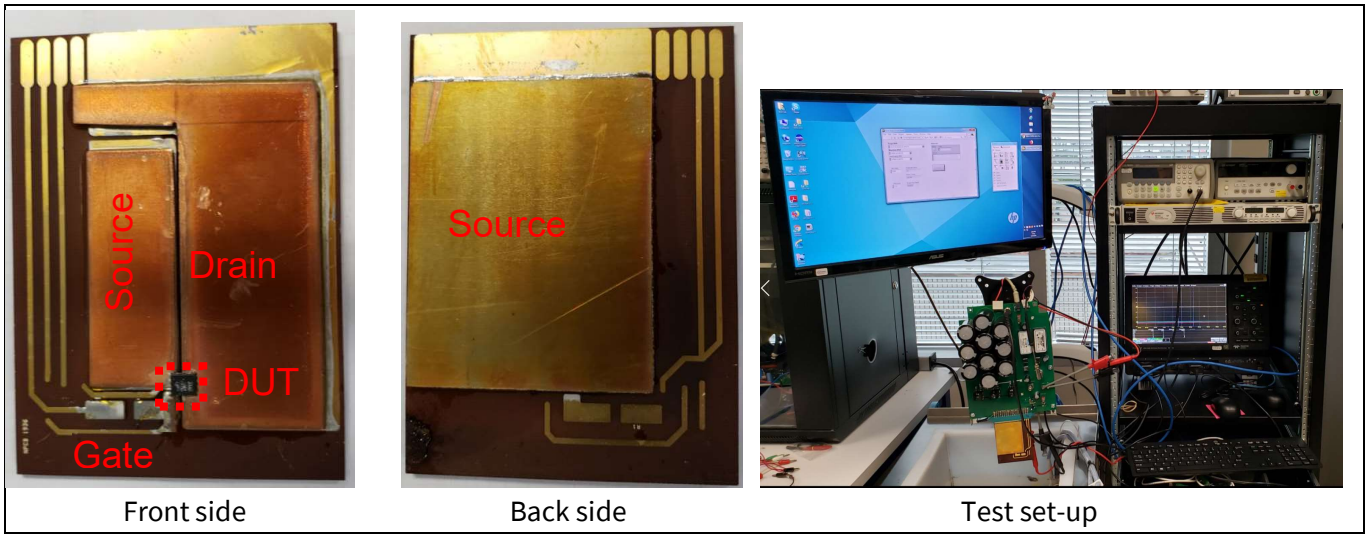


Figure 7 Test schematic



Front side Back side Test set-up

Figure 8 Test board and set-up

The DUT is mounted on a test board, as shown in Figure 8. The drain and source regions are on either side of the board. Since the drain pad is the most efficient heat flow path, a large 50 oz copper plate was used to dissipate the heat effectively. The size of the board is 2.2 x 2.7 sq inches (38 cm^2). The material is pure copper (99.9 percent Cu). The temperature profile for reflow was developed to get a reliable solder contact on both source and drain pads. X-ray images were captured after the reflow to monitor the solder interface to the board, with the intent of minimizing the number and size of solder voids at the interface between the pads and the test board. In addition, the test board is immersed in a circulating liquid bath with temperature set and held constant at 25°C.

4.2 Test results

The sample test waveform is shown in Figure 9. Multiple devices were tested with 2000 A pulsed drain current, for 20 to 30 µs pulse widths for one million pulses with a frequency of 5 Hz. It took approximately 56 hours to complete testing of one part. Since the new current calculation methodology affects especially low ohmic products from the 25 to 100 voltage nodes, the testing included some of the 0.5 to 3 mΩ; 25 V, 40 V, 60 V and 100 V devices. Both source pad outlines, non-fused source leads and fused source leads, were evaluated [5].

Pre- and post-test DC and AC parameters were measured. Specifically DC parameters like breakdown voltage, threshold voltage, gate and source leakages (I_{DSS} and I_{GSS}), diode forward voltage drop and AC parameters like gate charge values (Q_{gs}, Q_{gd}, Q_g) and capacitance values (C_{iss}, C_{rss} and C_{oss}) were compared pre- and post-test. Between pre- and post-tests, 1.2 percent reduction in $R_{DS(on)}$ was observed, and no failures were encountered. The DC parameters pre- and post-test were measured as per the datasheet conditions as tabulated in Table 3. I_{DSS} and I_{GSS} show larger change; however, it is in the nanoampere range and is limited by tester resolution. No change in AC parameters like capacitance and gate charge was observed. Fused and non-fused source lead products also showed similar performance.

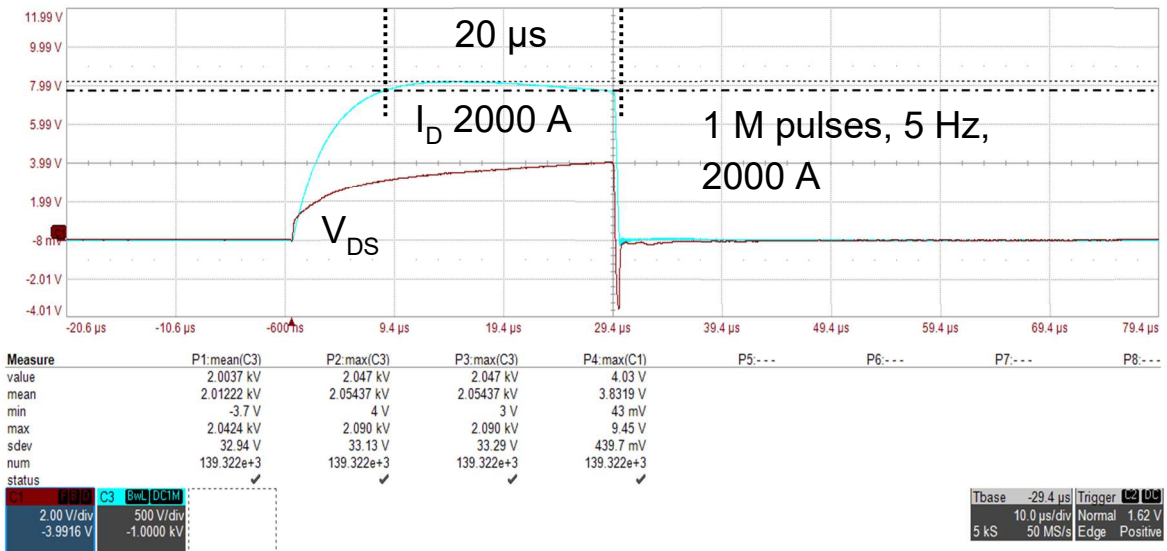


Figure 9 Test waveform (BSC010N04LS)

Table 3 Average electrical parameters pre- and post-1 million pulses (BSC010N04LS)

Average values	$V_{GS(th)}$ [V]	I_{GSS} [nA]	I_{DSS} [nA]	$V_{(BR)DSS}$ [V]	$R_{DS(on)}$ at V_{GS} = 10 V [mΩ]	V_{SD} [V]
Pre-test	1.48	21.4	21.3	43.5	0.85	0.807
Post-test	1.47	22.4	15.9	43.3	0.84	0.813
Percentage change	0.5 %	-4.7 %	25.3 %	0.3 %	1.2 %	-0.8 %

4.3 Mapping the test conditions onto the SOA diagram

Figure 10 highlights the improvement in the SOA due to the I_D and I_{Dpulse} rating increase. The triangles represent the enlarged area at DC, 10 and 1 ms pulse widths. The dashed polygons represent increase in SOA at 10 and 1 µs pulse widths. The largest improvement is happening due to improved I_{Dpulse} at 1 and 10 µs pulse widths. Hence, tests were also carried out to verify this region. The test points are plotted on the SOA diagram as indicated by the green star (2000 A). The 2000 A condition was chosen to make sure that the new I_{Dpulse} rating can be confidently applied to sub-mΩ products. All tested parts survived the 1 M pulse target. Please note that we tested above the DS limits to make sure the new I_D rating provides sufficient margin against the existing process distribution. As such the use of any part above the DS limits is not recommended.

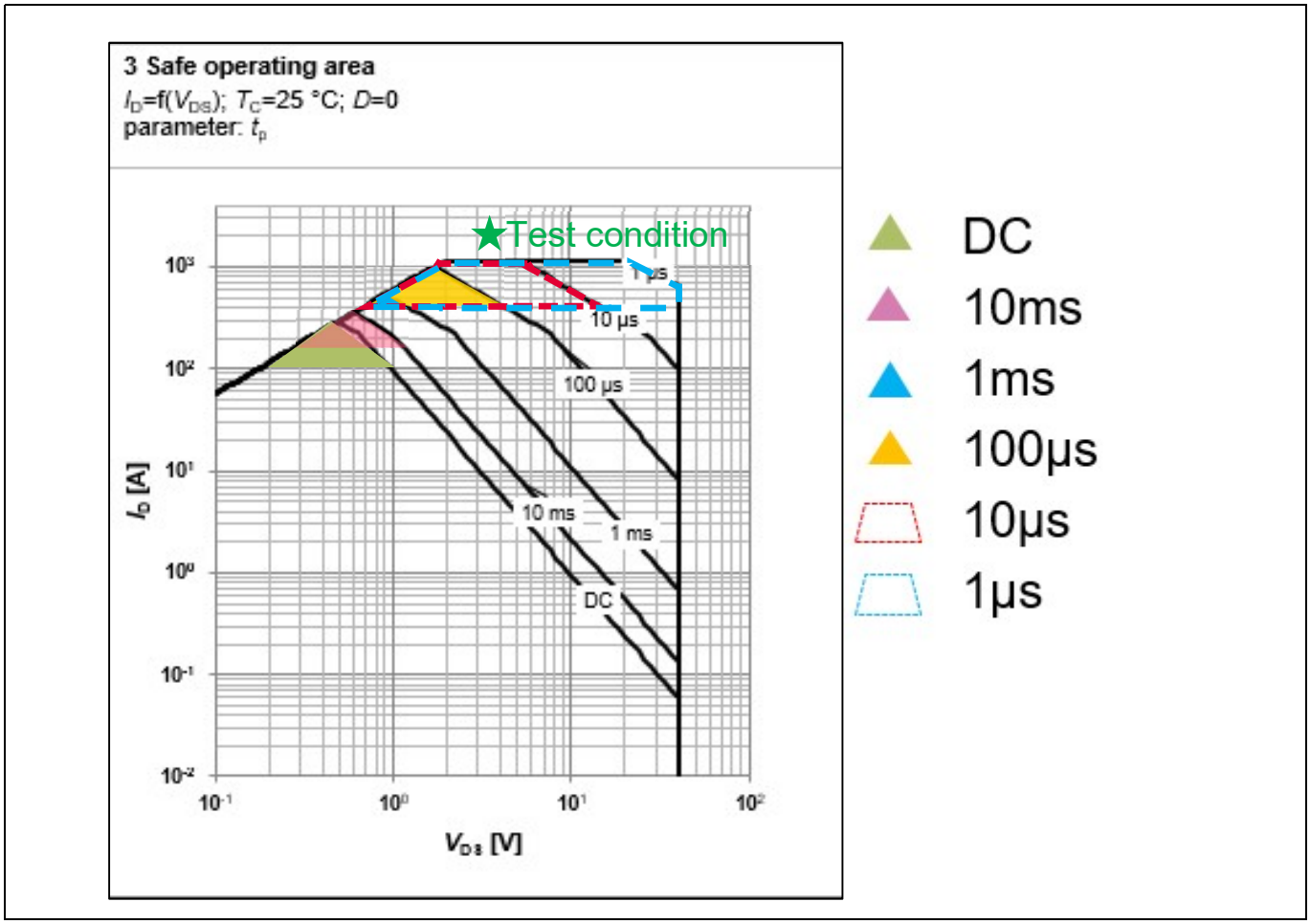


Figure 10 Test condition mapping onto SOA diagram (BSC010N04LS)

5 Influences on MOSFET selection

5.1 What limits the current in real application?

The method described in this application note, as mentioned earlier, is based on the ideal conditions with board and case temperatures held constant with no influence of environmental conditions. In reality the board/PCB temperature may be higher than the room temperature, hence de-rating will be required as indicated by the I_D vs. T_C graph (Figure 5 shown earlier). This method assumes negligible thermal resistance from the package case/leads to the PCB. As such the solder and PCB thermal resistances are neglected. These could be significant especially for an FR4-type board. Uneven solder joints and voids will also adversely affect the current rating. Two simple examples are illustrated below for better understanding of this topic.

Part under consideration: BSC010N04LS

$R_{thJ\text{-}C\ MAX}$ = 0.9°C/W

ΔT = 150 °C – 25 °C = 125°C

$R_{DS(on)MAX}$ at T_{jMAX} = 1.75 mΩ

$$I_{DMAX} = \sqrt{\frac{\Delta T}{RthJCMAX \times Rdon\ MAX\ @\ TjMAX}} = \sqrt{\frac{125}{0.00175 \times 0.9}} = 281.8\ A$$

Assuming 3 in x 3 in, four-layer (2 oz. per layer) Cu FR4 board and 20 vias under the drain pad (refer to Fig. 11), R_{th} from solder and PCB is about 9°C/W. This is a typical scenario in a battery-powered application. The vias are 13 mil (330 µm) diameter and minimum via (wall to wall) spacing is 5 mil (125 µm). Further details of how to calculate R_{th} can be found in [6].

System R_{th} (PCB + solder + product $R_{thJCMAX}$) = 9.9°C/W

$$I_{DMAX} = \sqrt{\frac{125}{0.00175 \times 9.9}} = 85\ A$$

With increase in case/PCB temperature further de-rating will be required.

Another approach is to use $R_{thJAMAX}$ for the system. For this product BSC010N04LS, $R_{thJAMAX}$ = 50°C/W (as per data sheet test conditions, 40mm x 40mm x 1.5mm epoxy FR4 PCB with 6 cm^2, one layer 70µm thick Copper area for drain connection in still air) .

$$I_{DMAX} = \sqrt{\frac{125}{0.00175 \times 50}} = 37.8\ A$$

It can be concluded from these calculations that for more realistic usage conditions, significant de-rating in I_D is required. Even though the I_D is lowered, I_{Dpulse} for a few µs pulse widths can still be high (as indicated by the datasheet) as this is mainly limited by the thermal capacity of the product with lesser influence of the external factors.

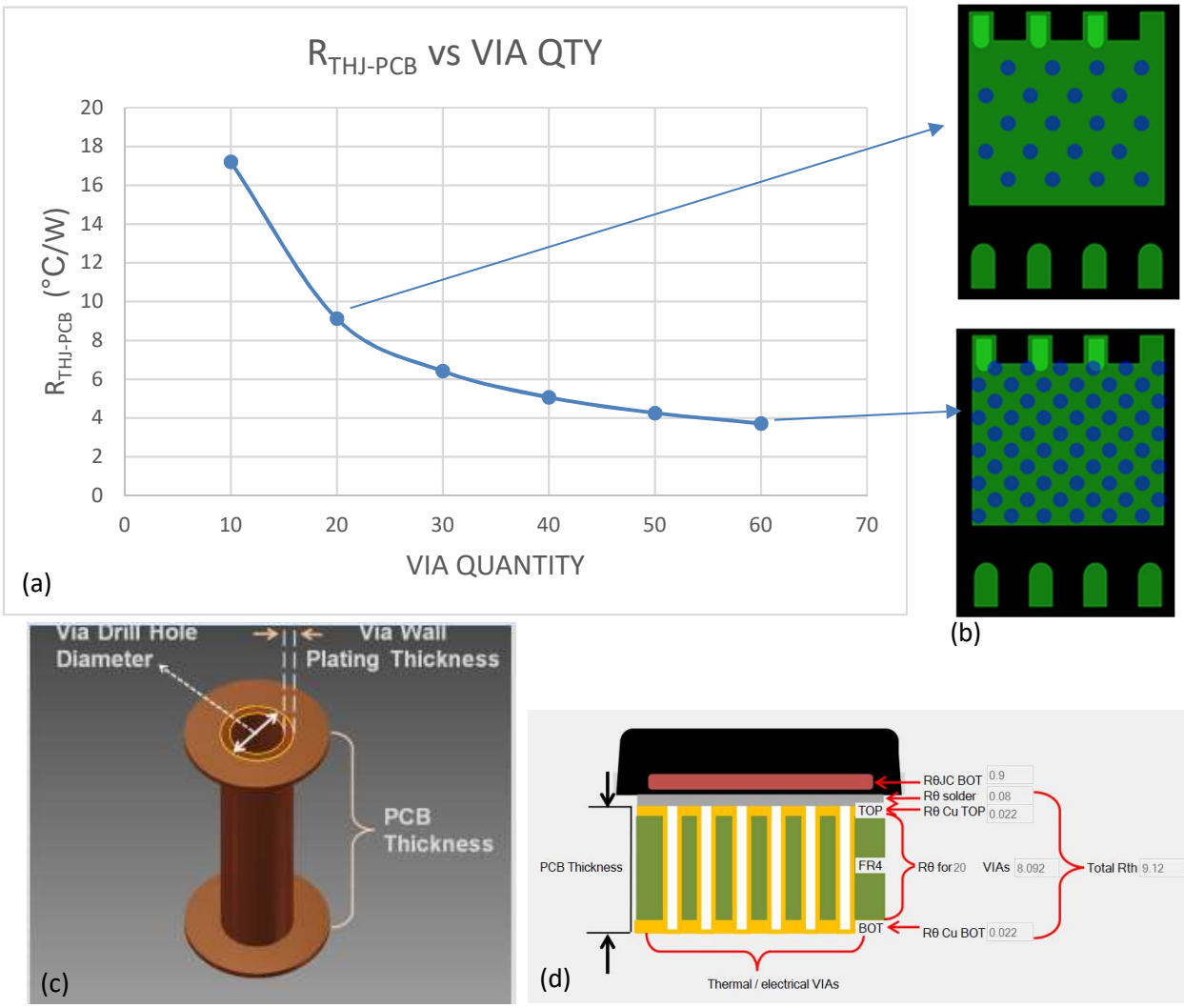


Figure 11 **$R_{thJ-PCB}$ for FR4 (a) calculated R_{th} for various number of vias, (b) illustration of outline showing number of vias, (c) illustration of via geometry, (d) simplified drawing of the PCB showing vias**

6 Summary

A new approach to calculating the maximum continuous and pulsed drain current ratings of Cu clip PQFN packages has been presented in this paper. Under specified boundary conditions the new approach yields significantly better current ratings over the previous method and also makes Infineon products more competitive. The impact of this change on the tables and diagrams has been shown. The improvements in the safe operating area have been verified with experimental results as described in this application note. The tests show low to no degradation in electrical performance under very stringent operating conditions over million pulses. Experimental data suggests that applied assumptions provide sufficient guardbanding against the process margin. The improved current ratings are based on certain assumptions of boundary conditions and no physical changes in the device/package construction have been made. The real limitation comes from the environmental conditions that must be considered for appropriate product selection. The new current ratings should help design engineers make a fair comparison among different devices. It should also be noted that for best performance/results adequate heat sinking must be applied.

All released data sheets for QFN products using Cu clip will be revised retroactively to reflect the new current rating method.

7 References

[1] Continuous DC Current Ratings of International Rectifier's Large Semiconductor Packages. Application Note AN-1140. May 2009.

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[3] A new approach to datasheet maximum drain current I_D rating of low voltage MOSFETs. AN_201709_PL11_006 October 2017.

[4] Linear Mode Operation and Safe Operating Diagrams of Power-MOSFETs. Application Note V1.1 May 2017.

[5] Discrete Power Qual Flat No-Lead (PQFN) Board Mounting Application Note. Application Note AN-1136, Version 22, Feb 2017.

[6] Thermal performance of surface mount semiconductor packages. AN_201708_PL52_023 March 2017.

Revision history

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V2.0	April 2020	Corrected minor typos

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