

CoolMOS™ gate drive and switching dynamics

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About this document

Scope and purpose

This document gives a systematic and comprehensive overview of the possibilities for influencing the switching dynamics of CoolMOS™ power transistors by varying the gate loop impedance. It turns out that potential effects essentially depend on system topology. Based on a thorough investigation of the driver/switch interaction mechanisms, several guidelines for optimizing gate resistors are derived and verified by simulation results.

Intended audience

Engineers with basic background in power switches, gate drive and the associated interactions.

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Introduction

1 Introduction

It is common knowledge among power system designers that the dynamics of switching transients can be influenced by the gate resistor. It is also clear to most of them that an increased gate resistor causes slower transients, and thus higher switching losses and less voltage overshoot. In contrast to these basic physical trade-offs, it turns out that the quantitative impact and thus the relevance of gate resistor tuning depends not only on the switch parameters; system and topological aspects are usually of even higher importance.

As most papers and practical investigations deal with specific and dedicated conditions only, it is the intention of this Application Note to provide a systematic and general overview of the possibilities for influencing the switching behavior of CoolMOS™ switches in whatever constellation by varying external impedances in the gate loop. Finally this should enable power system designers to come up with a reasonable “first guess” when dimensioning the gate drive in a given application.

The equivalent circuit

2 The equivalent circuit

The subject of this Application Note is depicted in Figure 1. This equivalent circuit of the switch/driver interface contains all the components that are relevant for the final switching waveforms. However, in addition to the parameters in Figure 1, it is absolutely crucial to differentiate with respect to general system aspects like hard-/soft-switching, single-switch/half-bridge topology, 3-/4-pin switches and current level. There is no general answer to the question of optimum gate impedance; it strongly depends on the actual application.

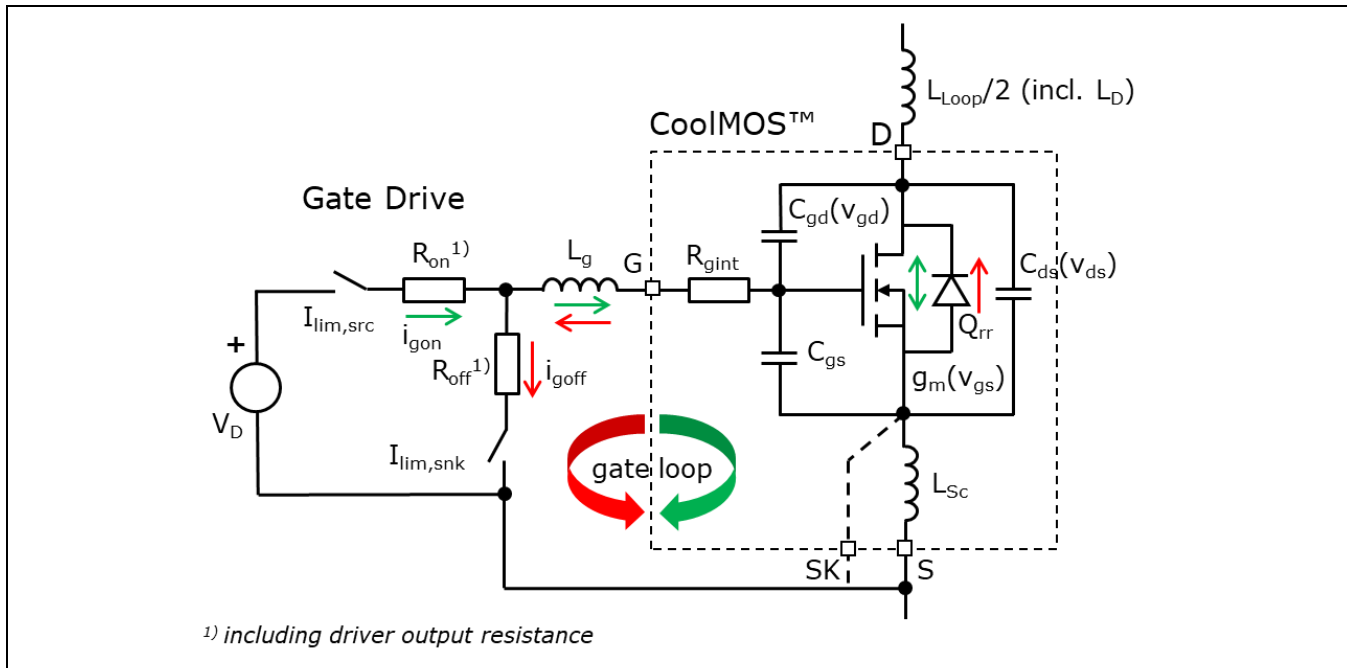


Figure 1 Equivalent circuit of CoolMOS™ switch and gate drive

2.1 Switch-related parameters

As for any other MOSFET, the CoolMOS™ equivalent circuit essentially consists of the inner transistor characterized by its static transfer function (drain current vs. terminal voltages), the body diode with the associated reverse recovery charge Q_{rr} , the three terminal capacitances (C_{gs} , C_{gd} and C_{ds}), and the inductance common to both gate and power loop (common source inductance L_{sc}). This inductance has a particularly significant influence on switching dynamics – so we have to clearly distinguish between switches with a separate Kelvin source connection SK as the gate driver reference (4-pin switches with negligible L_{sc}) and the more common 3-pin switches with an L_{sc} of several nH for large TO-packages.

Besides, the switch contributes to the total resistance in the gate loop with its intrinsic gate resistor R_{gint} . The gate and source inductances within the switch package are assumed to be included in L_g and $L_{loop}/2$, representing the total gate and half the power loop inductance (as usually two devices form the power loop).

The equivalent circuit

2.2 Gate driver parameters

The gate driver output stage can be regarded as two current-limited switches ($I_{lim,src}$ and $I_{lim,snk}$, respectively) with small on-resistance, connecting the output to either the positive or the negative node of the driver supply voltage V_D . In the case of Infineon's EiceDRIVER™ family, the on-resistance of the sourcing pMOS is a low 0.85Ω , whereas the sinking nMOS transistor shows even lower 0.35Ω . In most applications this is negligible compared to the total gate loop resistance. The source and sink current limit values are 4 A and 8 A, respectively. Again this is high enough to not become a limiting factor in most applications. And as an EiceDRIVER™ uses pMOS common-source transistors in the sourcing path instead of the source-followers in many competitor products, the current limits are accurate, well-defined and independent of output voltage.

2.3 PCB-related parameters

Obviously the parameters that are essentially determined by the PCB-structure and layout are the total inductances in gate and power loop, L_g and L_{Loop} , respectively. It is definitely and in any application advantageous to minimize the power loop inductance – so this should have highest priority in PCB design. The situation is not so evident for the gate loop inductance; it will be further discussed in chapter 9.

Beside power loop inductance, special attention must be paid to minimizing any capacitance connected from the high-side gate to ground or any other fixed potential, as such a capacitance would directly add to the gate-drain capacitance. Only a few pF could significantly increase the effective gate-to-drain charge and thus influence switching dynamics.

2.4 External components

There are only few parameters in Figure 1 that can be varied. First of all these are the external gate resistors R_{on} and R_{off} . Throughout this paper separate on/off resistors are assumed; however, there are many applications compatible with one common gate resistor.

Under certain conditions, particularly for 3-pin switches operated at high current, a variation of L_g also makes sense.

Driving voltage V_D is not considered separately, as a change of V_D is more or less equivalent to a change of gate resistor R_{on} , at least for the most interesting switching transients. Thus in the following a fixed driver supply voltage $V_D = 12 \text{ V}$ is assumed.

So the central question remains: How should the external gate impedance be chosen to optimize the switching behavior of a CoolMOS™ transistor?

Although a simple question, there is no simple answer – and this is for a simple reason: the mechanisms and effects involved strongly depend on switching topology and conditions, and thus different applications must be treated differently.

Switching topology and conditions

3 Switching topology and conditions

As already mentioned, the common source inductance L_{sc} dramatically influences switching dynamics. And because this parameter is either negligible or dominant, the first classification refers to the availability of a Kelvin source, i.e. we must distinguish 4-pin from 3-pin switches. Regarding topologies, it is also useful to differentiate between single-switch and half-bridge applications. Typical examples are the classic boost PFC with low-side switch and high-side diode on the one hand, and the LLC converter on the other.

Out of these criteria, the four main topologies of Figure 2 are as follows:

- 4sw: single switch with Kelvin source
- 4hb: half-bridge with Kelvin source
- 3hb: half-bridge in 3-pin package
- 3sw: single switch in 3-pin package

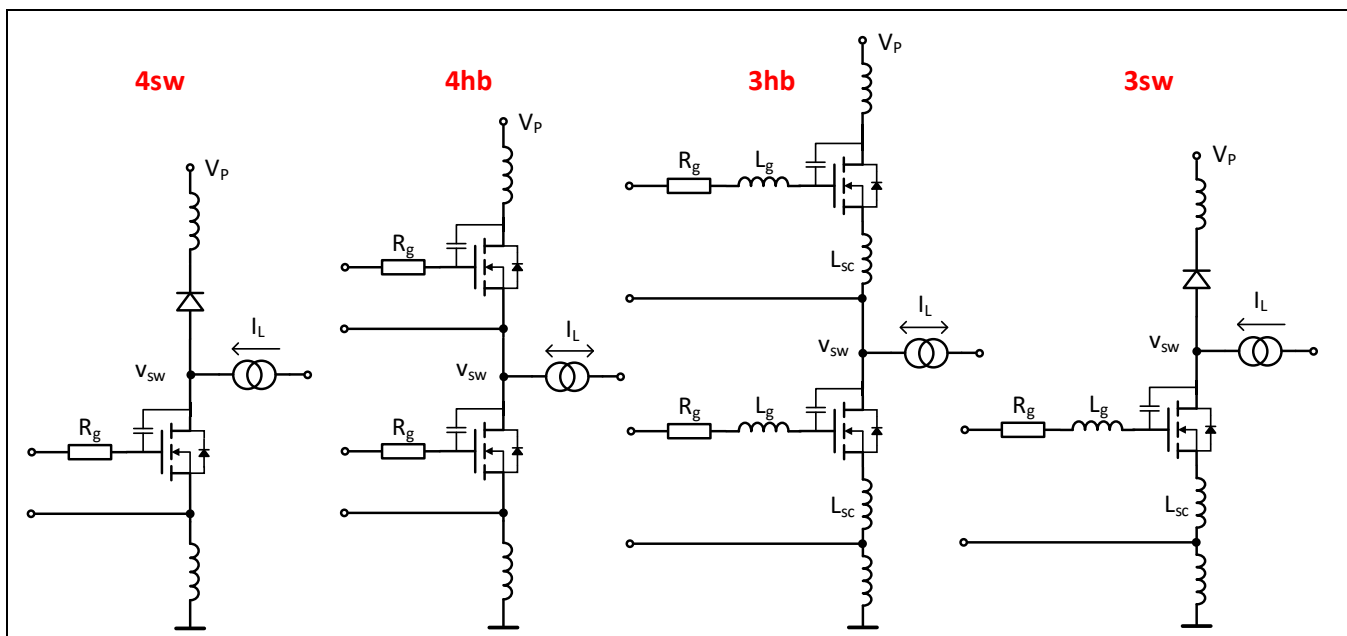


Figure 2 Main switching topologies under investigation

A further essential differentiation is related to hard- and soft-switching, respectively. Hard-switching takes place when a transistor is switched “on” at a high drain-source voltage. The transient of the switch node voltage v_{sw} is thus caused by the switch-“on” event, while in soft-switching cases the v_{sw} transient is initiated by switching “off” a transistor. In most applications the switching node is connected to an inductive filter with very long time constant compared to the switching period; this is why the constant current source I_L at v_{sw} in Figure 2 is a valid assumption for the investigation of single switching events.

In certain cases it is also necessary to distinguish between low-to-moderate and high current levels. High current refers to operation at load current levels close to the switches’ maximum ratings. A typical example is the “AC-line cycle drop-out” situation in PFCs as defined in IEC 61000-4-11, when the current level increases to two to three times the nominal current for a limited time (e.g. 20 ms).

4 Terminal capacitances, transfer characteristics and gate charge curve

By far the most important characteristics regarding switching behavior are the well-known terminal capacitances over drain voltage curves. A typical set is depicted in Figure 3a) for a 95 mΩ CoolMOS™ switch of the C7 family. While the input capacitance $C_{iss} = C_{gs} + C_{gd}$ is nearly constant over the entire voltage range except for very low drain voltage, the other capacitances $C_{oss} = C_{gd} + C_{ds}$ and $C_{rss} = C_{gd}$ exhibit an extremely high dependence on drain voltage with the capacitance values varying by three orders of magnitude. This behavior is characteristic for Superjunction (SJ) MOSFETs and, as we will see, essentially influences the shape of the switching waveforms.

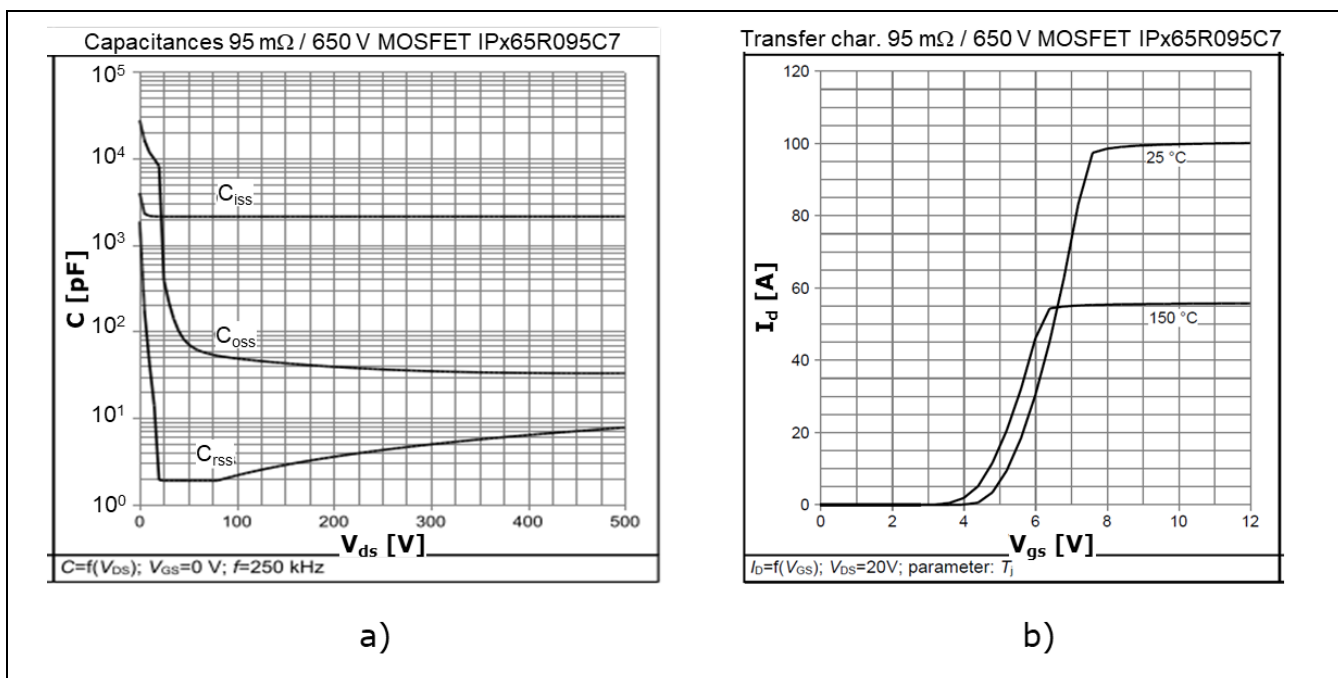


Figure 3 Terminal capacitances over V_{ds} (a) and transfer characteristic (b) of 95 mΩ/650 V C7 CoolMOS™ switch IPx65R095C7

Beside the terminal capacitances the static transfer characteristic $I_d = f(V_{gs})$ as given in Figure 3b) is of importance. It is worth noticing that the transconductance $g_m = dI_d/dV_{gs}$, i.e. the derivative of the transfer characteristic, is non-zero only for a range of a few volts above the threshold voltage V_{th} . Particularly in the steady "off" and "on" states, when the gate-to-source voltage is 0 and 12 V, respectively, the transconductance of the switch is zero.

A further well-known switch characteristic is the so-called gate charge curve as shown in Figure 4, again for IPx65R095C7. It can be derived from the above capacitance curves and describes the load a MOSFET presents to the gate driver in a certain switching situation. As the gate charge curve depicts the gate-to-source voltage V_{gs} as a function of gate charge Q_g , any linear part of this curve corresponds to a constant capacitance. So in the usual representation the slope of the branch from $V_{gs} = 0$ up to the Miller level (i.e. the gate voltage associated with a given drain current as derived from the transfer characteristic) is nothing else than the gate-to-source capacitance C_{gs} at high V_{ds} ("off" state), while the right branch from Miller level up to the steady "on" state is the characteristic of the (higher) C_{gs} at low V_{ds} . The length of the Miller plateau represents the change in Q_{gd} associated with any voltage transient and thus slightly depends on the switched voltage itself. However, due to the extremely non-linear C_{gd} the contribution of the high drain voltage region to the total charge Q_{gd} is rather small.

Terminal capacitances, transfer characteristics and gate charge curve

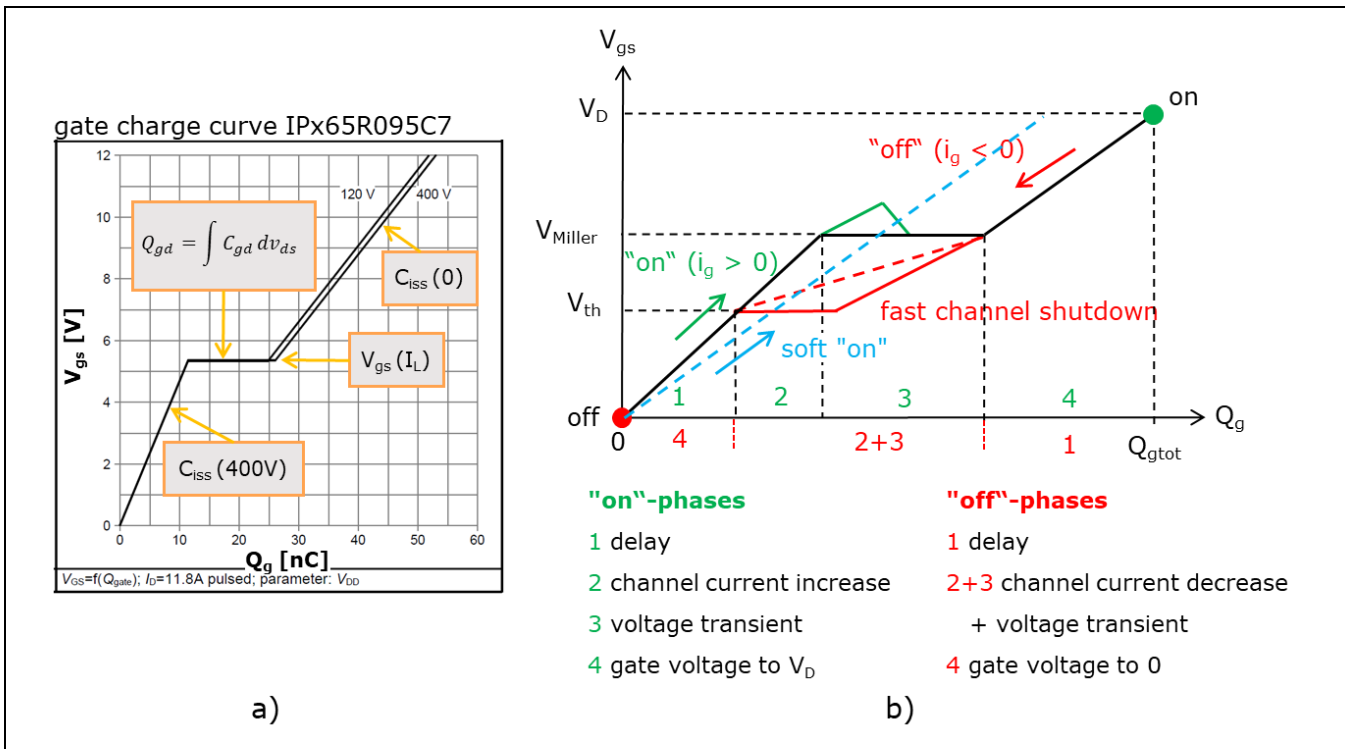


Figure 4 Quasi-static gate charge curve IPx65R095C7 (a) and deviations for fast switching (b)

An obvious assumption with this gate charge curve is that the drain voltage transient is caused by the gate voltage transient. In “on” direction this means that it is only valid under hard-switching conditions. For soft-switching events the drain voltage transient has happened before the transistor is switched “on”. Then the gate simply behaves like the constant capacitance $C_{iss}(0)$. Q_{gd} is part of the total output charge Q_{oss} and has been provided by the output current I_L prior to the gate voltage transient.

As gate charge is the integrated gate current, the question arises, if and when the gate charge curve equals the real gate voltage switching waveform. Although for a constant gate current the charge axis becomes equivalent to a time axis, the gate voltage would only follow the curve in Figure 4a) with the flat Miller plateau, if during this phase (voltage transient) there is no change in v_{gs} and all the gate current i_g is flowing into C_{gd} . Then the channel current i_{ch} stays constant at a value slightly above the external current I_L . The difference $i_{ch} - I_L$, however, is responsible for charging the capacitances connected to the switching node, and small total charging current means also small current into C_{gd} and thus small i_g . As switching time is inversely proportional to i_g , we can say that the common gate charge curve reflects the v_{gs} waveform only for slow, quasi-static switching.

In realistic fast-switching cases the resulting waveforms are similar to the green and red curves in Figure 4b). The non-constant Miller “plateau” can be interpreted as a significant peak in channel current during a hard-switching-on event that allows a high charging current and fast voltage transient. In “off”-direction a high gate current causes a fast channel current decrease, when the Miller level is reached. So, in contrast to the quasi-static case, voltage and current transient happen simultaneously (during switching phase 2 in Figure 4). As it is again the difference between external current I_L and channel current i_{ch} that charges the output capacitances, a fast shutdown of the channel current means high available charging current and consequently a fast-switching voltage transient.

Simulation and measurement

5 Simulation and measurement

In the following most conclusions are derived from analog network simulation results. The simulator used, SIMETRIX, is compatible with PSpice transistor models as provided on the Infineon website. Usually transient simulations of single switching events are performed, and the key strategy is to include all relevant components and parameters, but to keep complexity as low as possible. This is very important in understanding the main mechanisms determining switching waveforms, a precondition for any target-oriented optimization measures.

In Figure 5 an example simulation circuit is depicted with a single low-side switch in boost configuration and a CoolSiC™ diode (IDx06G65C6) at the high-side; this is the classic topology for PFC stages.

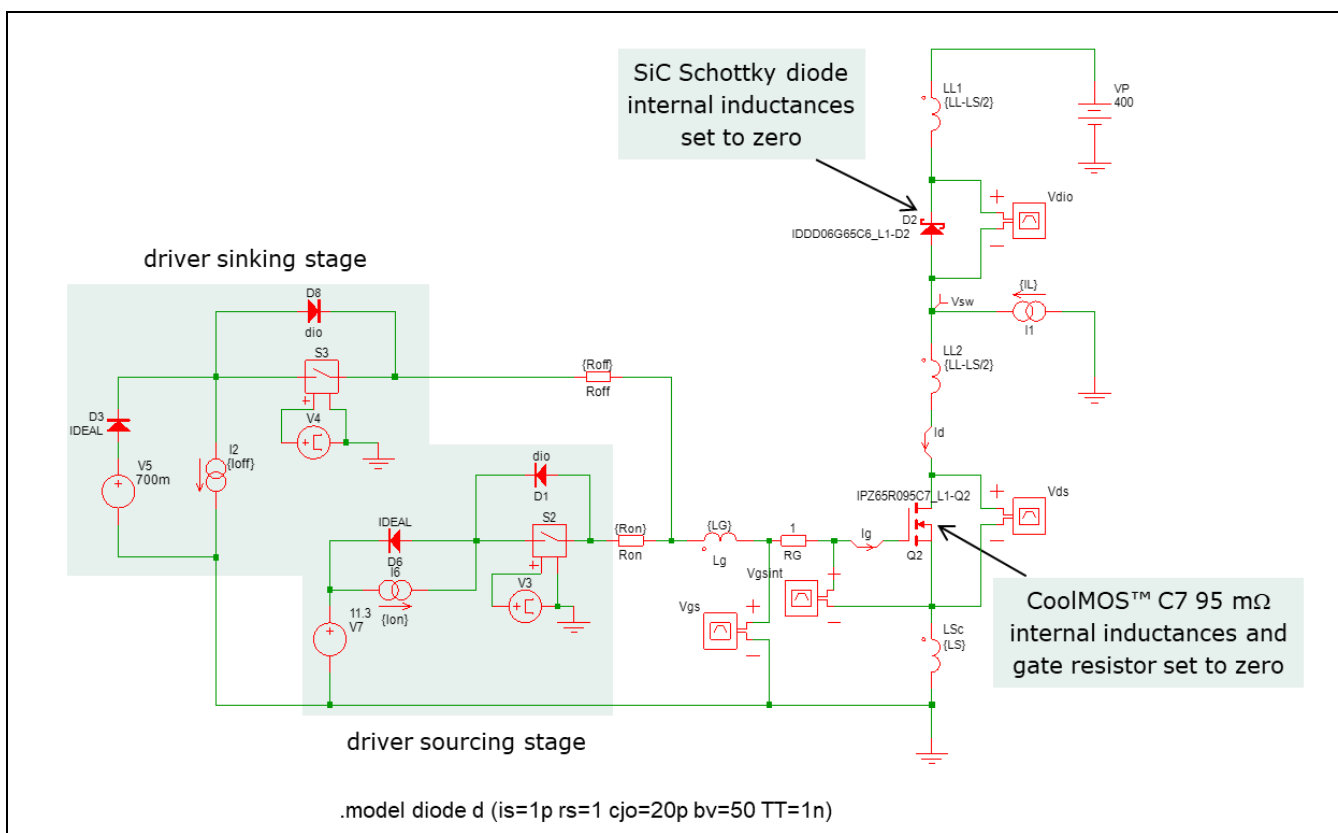


Figure 5 Simulation circuit for boost stage with 95 mΩ C7 CoolMOS™ switch

The switch model, as available on the internet or in the SIMETRIX device library, contains the inner transistor, characterized by its transfer characteristics, the terminal capacitances, the internal gate resistor and package inductances. To allow access to the inner transistor terminals, gate resistor and terminal inductances have been set to zero within the model and have separately been put into the simulation circuit (R_1 , L_g , L_{Sc} and L_L). The total power loop inductance L_{Loop} has been split into two equal parts, L_{L1} and L_{L2} , associated with the switch and diode, respectively. L_{Loop} is assumed to be 12 nH (a rather good value in standard PCB designs), whereas the default gate inductance L_g is 16 nH.

The common source inductance L_{Sc} is chosen in a range from 4 nH (for 3-pin switches in TO-220 package) to zero (for 4-pin switches). With a value below 1 Ω, the internal gate resistor for IPx65R095C7 is very low and has only a small impact on switching dynamics.

Simulation and measurement

The driver output stage is modeled as two switchable voltage sources for the “off” and “on” state with the respective current limitations I_{off} and I_{on} , e.g. 8 and 4 A for a typical EiceDRIVER™ output stage. The driver output resistance is rather small (0.35 and 0.85 Ω , respectively); it is assumed to be merged with the external gate resistors R_{off} and R_{on} . The two diodes “dio” are added in parallel with the ideal switches to model the body diodes of the driver output transistors. The voltage sources in the driver equivalent circuit correspond to the gate drive levels 0 and 12 V, corrected by the voltage drop of diodes D3 and D6.

Interestingly, many system designers share reservations about simulation results. They regard measurements as far more trustworthy. In fact the opposite is true. Reliable measurement results in fast-switching circuits need a lot of experience and expensive high-end equipment due to the required extreme common-mode suppression, if for example V_{gs} of a high-side switch has to be measured. Besides, current measurements are not possible without impacting the switching behavior due to the insertion of additional parasitic components. Finally, many points of interest, for example the intrinsic transistor terminals, are simply not accessible.

On the other hand, if the relevant transistor parameters are correctly modeled and if the simulation circuit is complete and reasonable estimations for PCB parasitics are available, the simulated behavior very well describes reality in most practical cases. Of course some knowledge of model validity and restrictions is also important; effects resulting from the distributed nature of some components (like the gate resistor for very large switches) or from a hysteresis of the terminal capacitance characteristics, leading to the so-called E-passive losses, are not included in the models.

It is very important to understand that the actual voltages at the inner transistor terminals cannot be measured directly, but have to be derived from measurable voltages. Looking at the power loop, the only node voltage accessible for a measurement is the switching node voltage v_{sw} . This voltage differs, however, from the voltages seen at the switch and diode terminals, v_{ds} and v_{dio} , respectively. Obviously, in Figure 5

$$v_{\text{ds}} + v_{\text{dio}} + 2v_{\text{LL}} = 400 \text{ V}$$

with v_{LL} denoting the inductive voltage drop over L_{L} (L_{Sc} is assumed to be zero). In the simulation circuit the total loop inductance is split into two equally valued parts L_{L} , and as di/dt is the same for both inductances (the difference of the inductor currents is the constant I_{L}), also the inductive voltage drops are equal. Whenever the drain current falls, a negative voltage v_{LL} is induced on L_{L} , and the voltage over the diode can reach $v_{\text{dio}} = 400 - 2v_{\text{LL}}$; i.e. it exhibits a voltage overshoot of $2v_{\text{LL}}$. The measurable v_{sw} , however, only includes one of these inductive drops; the actual diode over-voltage is thus twice the negative voltage seen at v_{sw} . Vice versa, for switching “off” the voltage overshoot at the inner drain/source terminals is double the overshoot seen at node v_{sw} . In Figure 6 this is visualized by depicting the three voltage waveforms v_{ds} , v_{dio} and v_{sw} .

Simulation and measurement

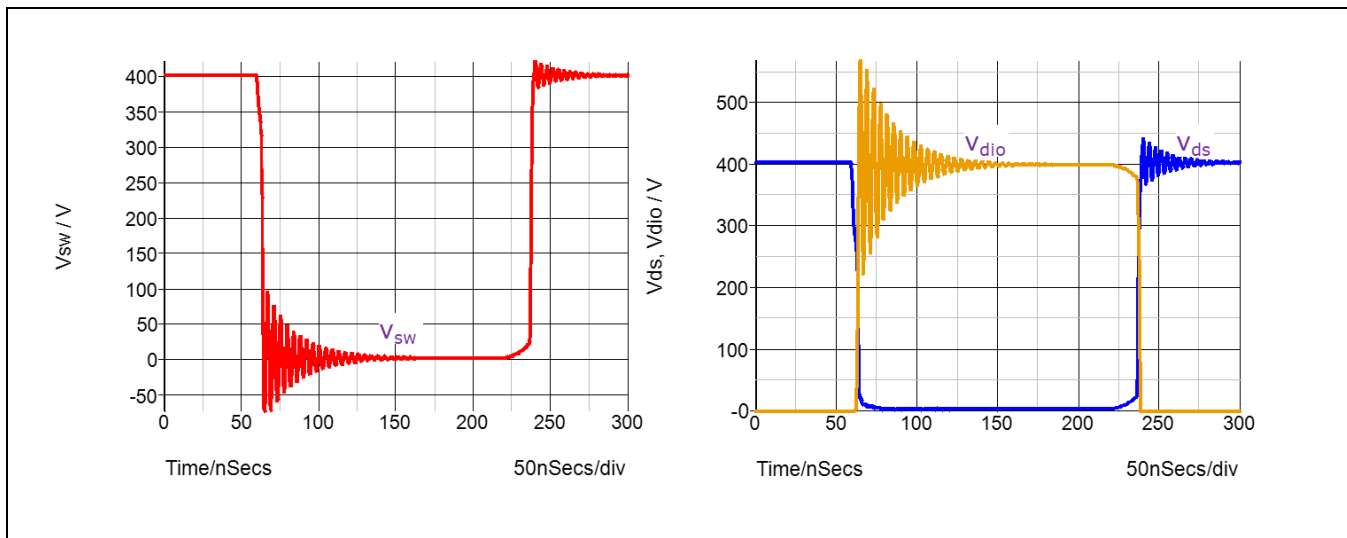


Figure 6 Voltage waveforms at switching node v_{sw} and device terminals (v_{dio} , v_{ds})

The situation is similar when measuring v_{gs} . Again, the inner transistor nodes cannot be accessed, and the measured voltage includes the voltage drops over the internal gate resistor and the package-associated gate inductance. The deviation can be positive or negative, depending on gate current direction, and a judgment of measurement results requires careful consideration of these effects.

For 3-pin switches the situation is even worse. Now the voltage induced in the common source inductance by the commutation of the power loop current is unavoidably included in the measurements. And as this is by far higher than the intrinsic v_{gs} level, the gate-to-source voltage of 3-pin switches simply cannot be measured (see also 9.5). Simulations, then, are very helpful to allow realistic estimations of the actual terminal voltages.

The steady state - Dimensioning Guideline 1 (DG 1)

6 The steady state - Dimensioning Guideline 1 (DG 1)

Although the equivalent circuit as given in Figure 1 does not look very complicated, really it is. This is due to the fact that gate and power loop are not independent, but interact via the switch transconductance (change in gate voltage influences drain current), the gate-to-drain capacitance (change in switch node voltage causes gate current) and the common source inductance (change in drain current influences gate voltage). Besides, the time constants associated with gate driver output, switching node and gate terminal cover a broad range from some tenths to several tens of nanoseconds.

However, all these interactions take place only during the switching transients, and these are typically very short compared to the switching period. So most of the time a switch spends in the steady “on” and “off” states with V_{gs} equal to V_d or zero. Then the transconductance is zero, too, and there is no interaction between gate and power loop. The switch behaves like an open circuit in “off” state or a small resistance R_{dson} when “on”. The equivalent circuit thus simplifies to the two cases depicted in Figure 7.

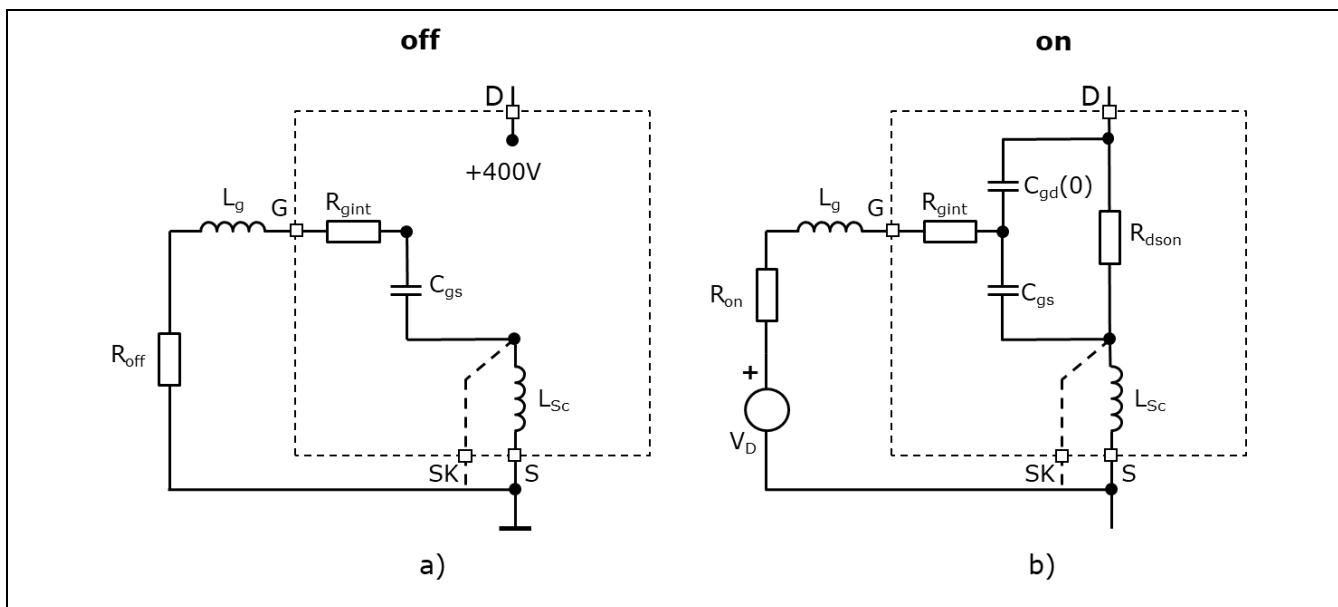
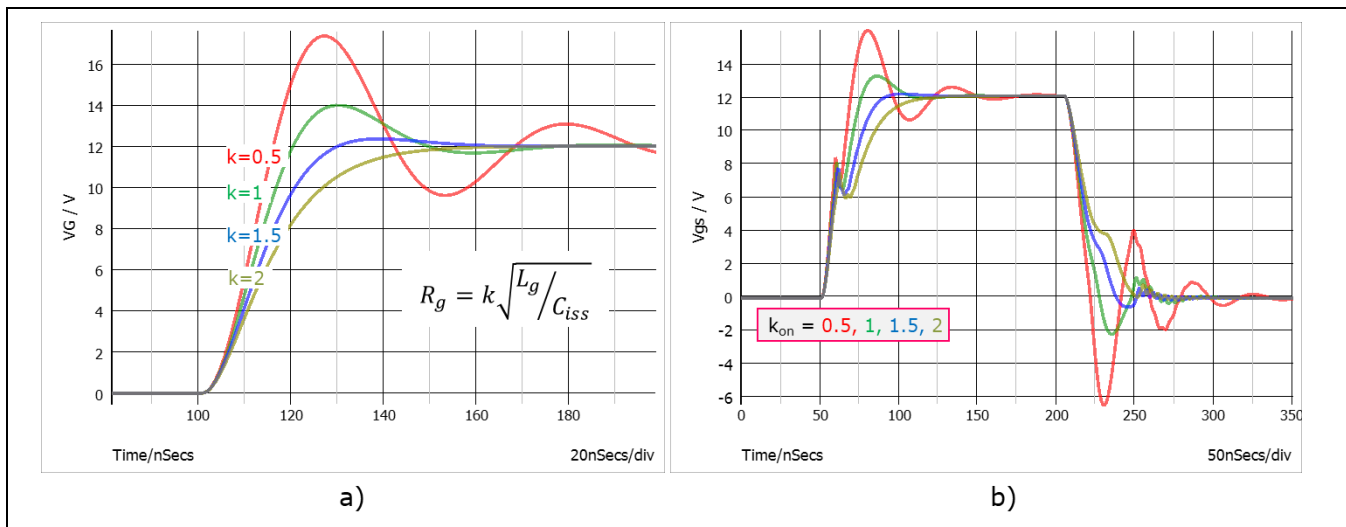


Figure 7 Equivalent circuit for steady “off” (a) and “on” states (b)

Obviously the gate loop forms a simple RLC circuit containing the total loop resistance R_g and inductance L_g and the input capacitance C_{iss} , equaling C_{gs} in the “off” state (as then C_{gd} is negligible) and $C_{gs} + C_{gd}(0) \sim 2 \cdot C_{gs}$ in the “on” state (see also Figure 3a).

The settling behavior of such a circuit is well known and depicted in Figure 8a). Ideally, the step response is defined by the parameter $k = R_g \sqrt{C_{iss}/L_g}$ only. For $k > 2$ the response to a voltage step exhibits zero overshoot. In practical switching applications the main criterion is that during settling after a change of states the gate voltage stays safely away from the threshold voltage. For usual MOSFET gates driven at 0 and 12 V, this is easily fulfilled even for the waveforms corresponding to $k = 1.5$ or 1. So in the following $k = 1.5$ is assumed to be sufficient to dampen any gate voltage ringing to uncritical values.

The steady state - Dimensioning Guideline 1 (DG 1)

Figure 8 Settling behavior of RLC circuit (a) and boost stage (b)

The real application differs from the ideal one particularly by the fact that due to the Miller plateau the gate voltage deviates from a step voltage. Anyway, the gate voltage waveforms of the simulated boost stage with our 95 mΩ CoolMOS™ switch (Figure 8b) show a similar settling behavior as the ideal oscillator of Figure 8a). The external gate resistors in 8b) (0, 1, 2 and 3 Ω) are chosen to result in the same damping parameter in “on” direction. However, it can be clearly seen that the overshoot after the “off” transient is higher; this is due to lower C_{iss} and thus less damping for the “off” transient. With $k_{on} = 0.5$ (no external gate resistor) the gate voltage ringing after the “off” transient nearly reaches the threshold voltage. The proposed $k_{on} = 1.5$ ($R_g = 2 \Omega$), however, results in very smooth gate voltage waveforms without significant impact on losses. Thus, as a first guideline for dimensioning the gate resistor, we can state:

Dimensioning Guideline 1

The minimum values for the external gate resistors must fulfill $R_{min} = 1.5 \sqrt{L_g / C_{iss}} - R_{int}$

We have seen that C_{iss} is different for “on” and “off” transient. To fulfill DG1, R_{off} has to be larger than R_{on} because of the lower C_{iss} in the “off” state. However, other criteria often call for a higher value of R_{on} . It is also worth mentioning that in certain CoolMOS™ families (e.g. CFD7) the internal gate resistor is high enough to always fulfill DG1, even with zero external resistance.

To give a practical example:

IPx65R095C7 has an internal gate resistance of $\sim 1 \Omega$; C_{iss} is ~ 2 nF in “off” and ~ 4 nF in “on” state. Assuming a total gate inductance of 16 nH, DG1 then yields a minimum external R_{on} of 2 Ω and a minimum external R_{off} of 3 Ω (including driver output resistance).

IPx60R090CFD7, a similar switch of the CFD7 family, has an internal gate resistor of $\sim 6 \Omega$ and thus would not require any external resistance with respect to gate voltage ringing.

7 Transient behavior for single-switch 4-pin topologies (DG2, 3)

7.1 Basic equations

Although a typical power switch spends nearly all the time in two stable steady states, it is nevertheless the transients between these states that determine a switching system's overall performance. In the following we will discuss the basic trade-offs and the possibilities of influencing switching behavior via gate drive. Due to various interaction mechanisms a differentiation with respect to topologies makes sense, and thus we start with the "simplest" topology, 4sw – single switch with Kelvin source connection (negligible common source inductance).

Without any loss of generality, we assume a low-side switch combined with a high-side "freewheeling" diode and a constant load current I_L flowing into the switching node, as depicted in Figure 9. With the switch in "off" state, the current flows through the diode and the switching node voltage v_{sw} is high. So the switch is turned "on" at high v_{ds} , and by definition this means hard-switching. After turning "off" the switch, I_L drives v_{sw} again up to and even slightly above the supply voltage V_P .

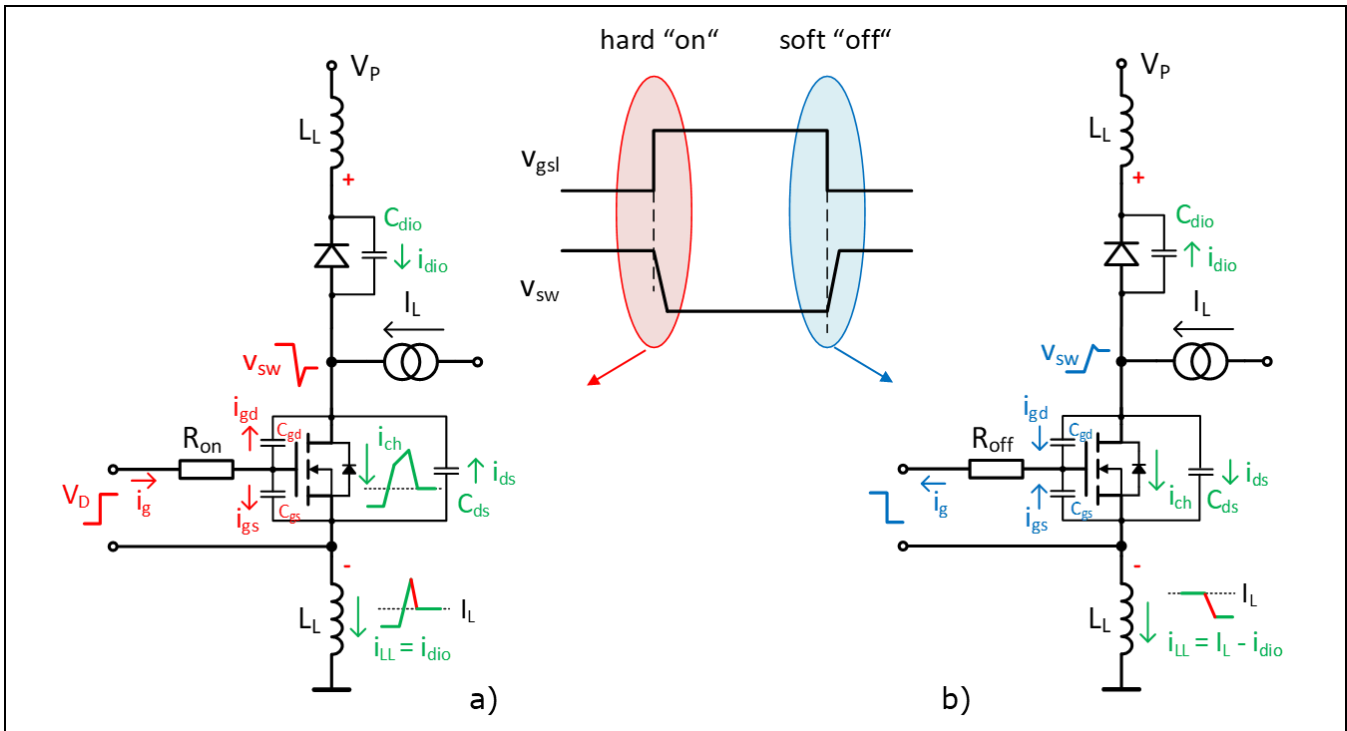


Figure 9 4sw topology with hard switch-on (a) and soft switch-off (b) transients

In Figure 9 the basic shapes of the switching waveforms are also given. When switching "on" (Figure 9a), the voltage transient starts as soon as the transistor channel current i_{ch} exceeds I_L , with the difference $i_{ch} - I_L$ discharging the capacitances connected to the switching node, i.e. C_{ds} , C_{gd} and the diode capacitance C_{dio} (eventually including diffusion capacitance to deal with reverse recovery charge).

The channel current i_{ch} now essentially depends on the gate current $i_g = i_{gs} + i_{gd}$ via the basic transistor equation

$$\frac{di_{ch}}{dt} = \frac{di_{ch}}{dv_{gs}} \cdot \frac{dv_{gs}}{dt} = g_m \frac{dv_{gs}}{dt} = g_m \frac{i_{gs}}{C_{gs}} = g_m \frac{i_g - i_{gd}}{C_{gs}} \quad (1)$$

Transient behavior for single-switch 4-pin topologies (DG2, 3)

Equation (1) completely describes the interaction between gate and power loop. It looks simple, but only in special cases it is. With respect to the switching phases indicated in Figure 4, both phases 1 and 4 are characterized by negligible transconductance. Then equation (1) simply means that there is no change in channel current during these phases (and of course in the steady states). During phase 2 i_{gd} is zero, and (1) describes the increase in channel current at a more or less constant rate, as both g_m and i_g vary only slightly.

However, during phase 3 the moving switching node causes a current i_{gd} into C_{gd} that is given by

$$i_{gd} = -C_{gd} \frac{dv_{sw}}{dt} = \frac{C_{gd}}{C_{sw}} (i_{ch} - i_L) \quad (2)$$

with C_{sw} denoting the total capacitance connected to the switching node; i.e. $C_{sw} = C_{gd} + C_{ds} + C_{dio}$. It is the difference between channel current and constant load current ($i_{ch} - i_L$) that is available to discharge C_{sw} . Equation (2) then states that i_{gd} is proportional to the capacitance ratio C_{gd}/C_{sw} . (1) and (2) completely describe the interaction between power and gate loop, but they form a coupled system of equations with a strongly non-linear coefficient (C_{gd}/C_{sw}). In some papers complicated closed-form approximations can be found for such equations, although they usually don't provide so much insight. The better way is to let a network simulator calculate solutions within a few seconds and then try to understand the dominant effects that determine switching waveforms.

The gate current i_g , in the “on”-case given by

$$i_g = \frac{V_D - v_{gs}}{R_{on}} \sim \frac{V_D - V_{Miller}}{R_{on}} \quad (3)$$

is the only parameter in the above equations we can influence, namely by varying R_{on} (the driving voltage is assumed to be fixed). As is evident from (1), i_g directly influences the channel current shape and thereby controls switching time and losses.

Also indicated in Figure 9a) is the effect of the unavoidable inductances in the power loop. We assume a split of the total inductance into two equal parts L_L associated with switch and diode, respectively. And as already explained in chapter 5, the falling edge of the current through L_L (red line in current shape i_{LL}), causes an over-voltage of $2 v_{LL}$ at the diode terminals. It is worth mentioning that i_{LL} is not equivalent to the channel current i_{ch} . As can be seen in Figure 9a), the discharging currents i_{ds} and i_{gd} contribute to the channel current, but do not flow through L_L . Thus i_{LL} is equal to i_{dio} . Qualitatively the transient starts with i_{dio} dominating compared to i_{oss} , the sum of i_{ds} and i_{gd} , as for high v_{sw} the diode capacitance C_{dio} is at least 10 times larger than C_{oss} . During the voltage transient this ratio decreases and finally i_{oss} contributes 99% to the discharging current $i_{ch} - i_L$. The shape of i_{LL} is thus completely determined by the voltage dependence of C_{oss} and C_{dio} .

The maximum negative i_{LL} slope is achieved for v_{sw} in the 20 to 50 V range, and according to Eq. (1) the absolute value depends on the peak channel current and thus on i_g . At the diode terminals the associated inductive voltages indicated in Figure 9a) ($2 v_{LL}$) add to V_P . And as already discussed, only the voltage across the switch inductance is seen as an undershoot voltage below zero, if the voltage is measured at the switching node.

In “off” direction (Figure 9b) the situation is similar. Now the difference $i_L - i_{ch}$ is charging the switch node capacitances. The gate current is given by

$$i_g = -\frac{v_{gs}}{R_{off}} \sim -\frac{V_{Miller}}{R_{off}} \quad (4)$$

and again equation (1) governs the decline of the channel current when the Miller plateau is reached. The higher the gate current value, the higher the discharging current i_{gs} of C_{gs} and the faster this decline.

Transient behavior for single-switch 4-pin topologies (DG2, 3)

Equation (2) is still valid to describe the gate/power loop coupling. A fast channel shutdown is particularly important in soft-switching applications to realize the virtually zero soft-switching losses, whereas in hard-switched topologies usually switch-on losses dominate.

The effect of power loop inductance can be described similarly (Figure 9b). Obviously i_{LL} is given now by $I_L - i_{dio}$, with i_{dio} changing from a negligible value in the first turn-off phase to the dominating part of total charging current for high v_{sw} . The maximum i_{LL} slope again happens between 20 and 50 V. In contrast to the switching-on event, however, the maximum charging current is now limited to I_L (when the channel is completely switched off). Although the resulting voltage overshoot at the switch is usually less critical than the diode voltage overshoot during switching on, inductive voltage drops may become a problem in case of switches with common source inductance, as the induced voltage tends to turn on the switch again, particularly when a high current has to be switched off fast; this problem is covered in detail in chapter 9.

7.2 Ideal switching waveforms (without inductances)

To visualize the basic switching behavior and facilitate the interpretation of switching waveforms, simulations with certain idealizations can be very helpful. This is why as a first step the circuit of Figure 5 has been simulated without inductances. It is quite instructive to look at the switching waveforms as a function of gate current. So in Figure 10a) the main waveforms describing the switching-on transient for different gate currents and an I_L of 10 A are compared: gate voltage v_{gs} (at the inner terminals), gate current i_g , drain current i_d and switch node voltage v_{sw} . For simplicity, the gate current is defined by directly varying the current sources in the driver equivalent circuit and the gate resistors are kept small.

It is obvious from Figure 10 that higher gate current means faster switching. And as expected, a pronounced Miller plateau exists only for small gate current. The impact of Eq. (1) can be seen in the drain current shapes, with both slope and peak value strongly increasing with i_g . The reduced switching time for higher i_g is then also reflected in the switching energies of Figure 10b), showing the integrated and summed current/voltage product for switch transistor and diode. The step corresponds to the “on” switching losses E_{on} , whereas the slope in steady-state is due to conduction losses E_{cond} .

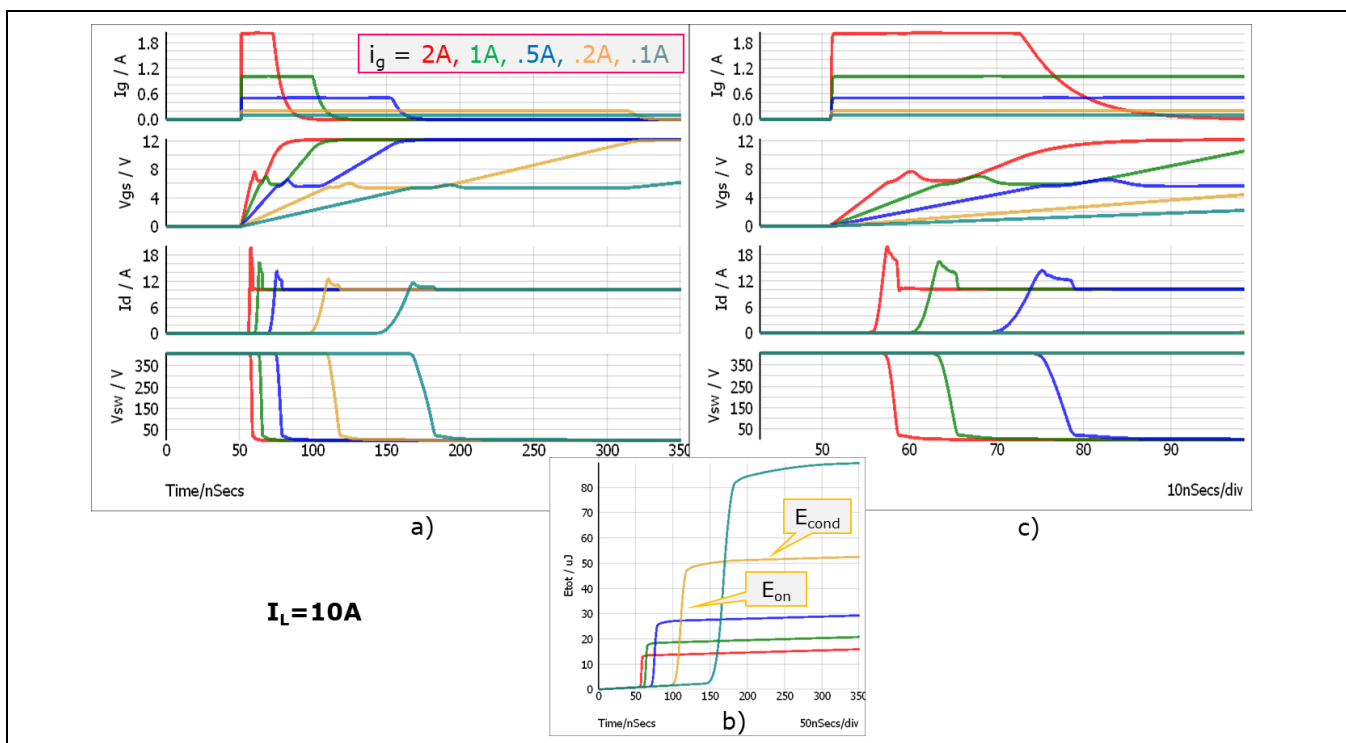


Figure 10 Switch-on waveforms over gate current (a), total losses (b) and waveform details (c)

Transient behavior for single-switch 4-pin topologies (DG2, 3)

Figure 10c) zooms into the transient. We see that the voltage transient starts soon after the current has exceeded I_L (as there is no significant reverse recovery charge of the SiC diode). However, when reaching some tens of volts, C_{oss} increases dramatically and most of the total gate charge / time is needed to reach the final “on” state.

In Figure 10c) it also can be clearly seen that the positive slope of the drain current is relatively constant and proportional to i_g , whereas the negative slope gets very steep when C_{oss} exhibits its strong increase. Finally, it is interesting to compare the shapes of i_d and v_{gs} . The peak in v_{gs} does not coincide with the peak in i_d , and this is due to the difference between the drain current and the (unmeasurable) channel current, as explained before (Figure 9a). Only the latter is controlled by v_{gs} . The charge defined by the area under the i_d waveform above I_L equals the charge in C_{dio} only, while a corresponding charge calculated from channel current also contains Q_{oss} .

Figure 11 shows the same curves for the “off” transient.

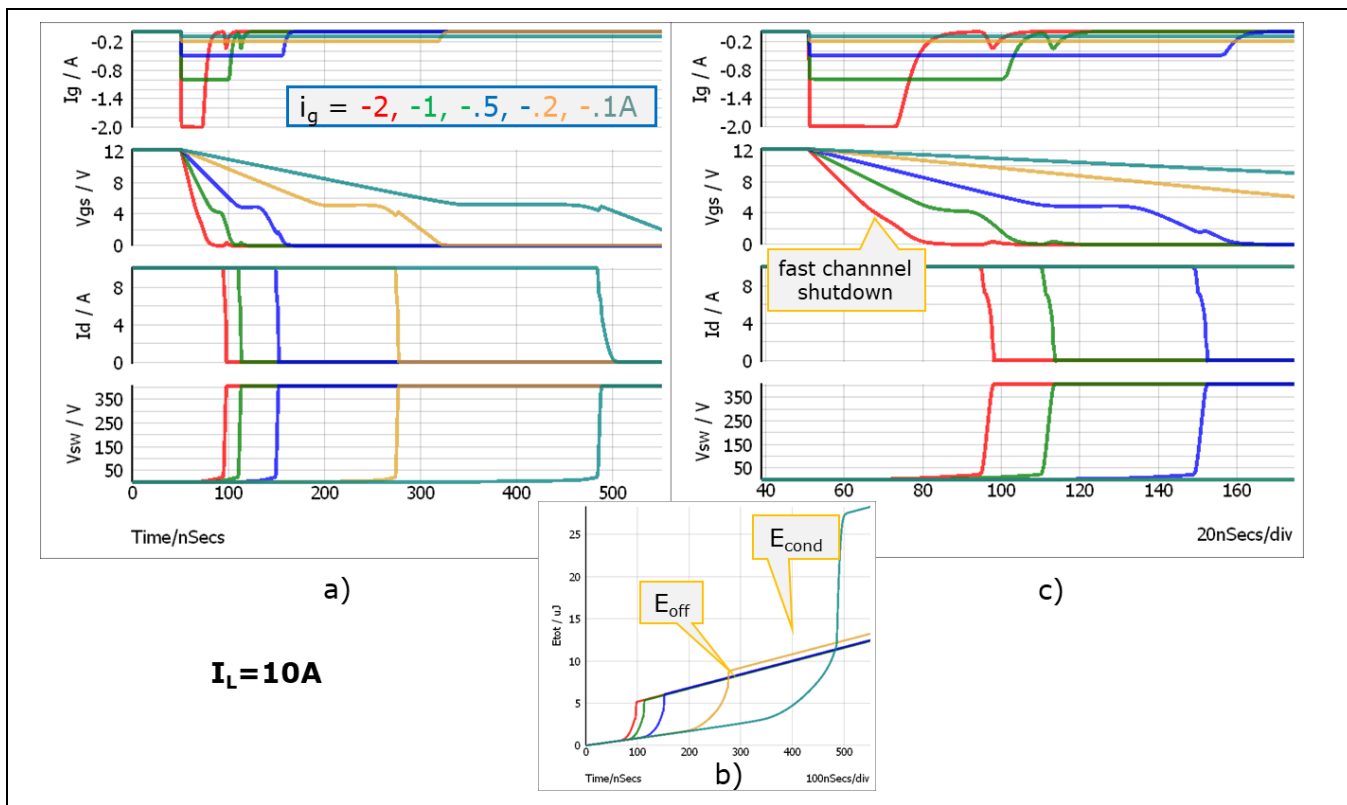


Figure 11 Switch-off waveforms over gate current (a), total losses (b) and waveform details (c)

At first sight the total transient time seems to be longer. But this is not true. The transient now starts when C_{oss} is huge, and the long delay in the v_{sw} curves is the equivalent to the long discharging time for the final 20 V of the “on”-transient. Anyway, in applications the “off”-delay is usually more relevant. It can also be seen that for high gate current the channel current (represented by v_{gs}) in fact reaches zero before the voltage rises significantly (fast channel shutdown). Even for moderate gate currents the switching loss stays nearly unchanged, but it increases dramatically for the lowest gate current (100 mA). Although E_{on} is by far larger than E_{off} , it makes sense to choose a high “off” gate current, too, due to the benefit of short delays for minimizing system dead-time.

Transient behavior for single-switch 4-pin topologies (DG2, 3)
7.3 Realistic waveforms, loss/overshoot trade-off (DG2, 3)

The above simulations help to understand basic relations and dependencies; however, the waveforms are not realistic due to the lack of inductances. Figure 12 illustrates what happens when they are included. It differs from Figure 10 only by introducing a total power loop inductance of 12 nH (a relatively low value requiring small packages and optimized PCB layout) and a gate loop inductance of 16 nH. Besides, the gate current limitation is not achieved by directly varying the current source in the gate driver equivalent circuit, but more realistically by utilizing a high internal current limitation (4 A) and defining the actual gate current by an external resistor R_{on} . The gate resistors have been chosen to allow maximum gate current values similar to those in Figure 10.

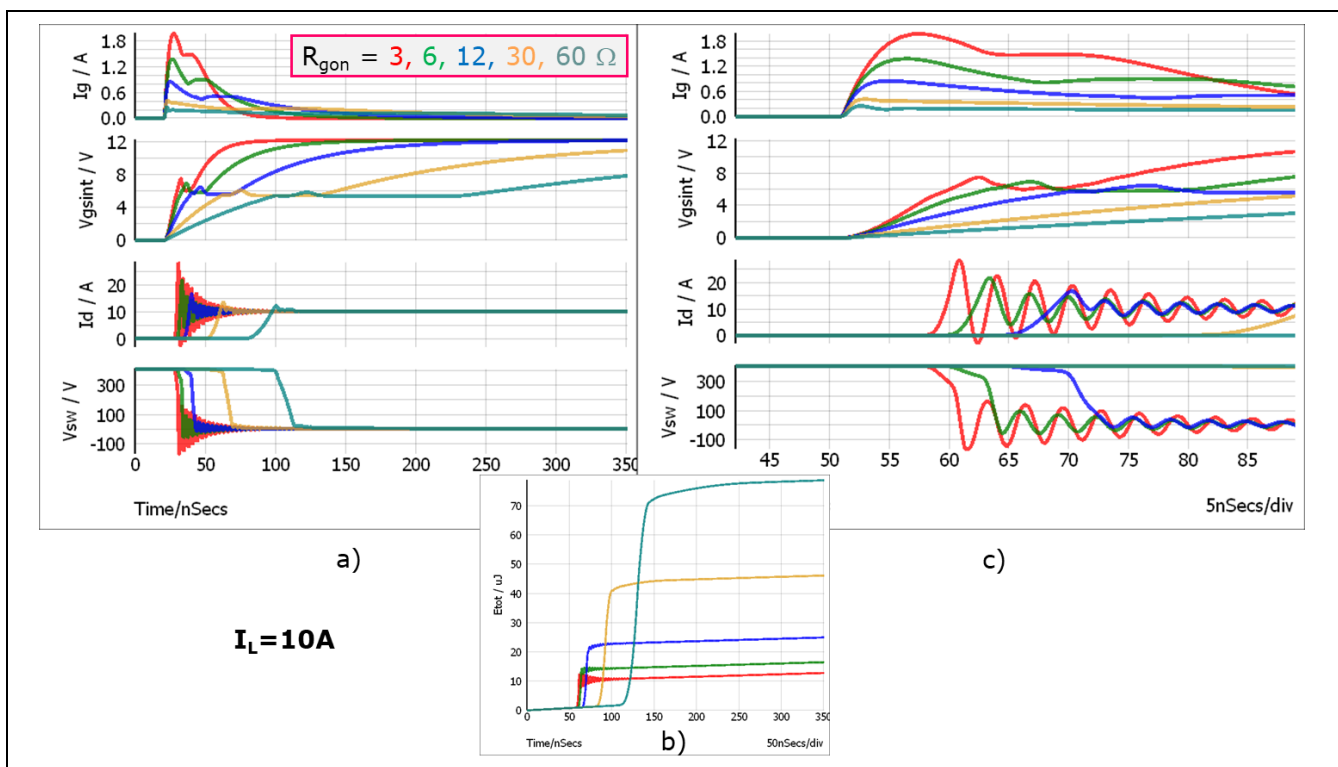


Figure 12 Waveforms of Figure 10 with gate and power loop inductance

Figure 12a) can now be directly compared with Figure 10a). Of course the gate current shape has slightly changed by the substitution of the ideal current with a resistive voltage source, but this has only a small impact on the gate voltage. The main difference can be seen in the switching node behavior. Due to the power loop inductance now a 300 MHz oscillation is superimposed on the ideal waveforms with its amplitude strongly depending on gate current and of course inductance value.

If we want to limit the switch node voltage to e.g. -100 V (corresponding to a maximum overshoot voltage at the diode terminals of 200 V!), it is obvious that a 3 Ω gate resistor is definitely too low, although it provides sufficient damping in the gate loop. 6 Ω , corresponding to an average gate current of 1 A, would limit v_{sw} to a reasonable value while hardly sacrificing efficiency. However, it is clear that there exists a basic trade-off between voltage overshoot and switching losses. This trade-off is fundamental and cannot be overcome. And as the resulting overshoot only slightly depends on the switched current, we can now formulate dimensioning guideline 2 (DG2).

Dimensioning Guideline 2

Choose R_{on} sufficiently high to limit i_g to a value that guarantees a safe peak voltage for the passive (high-side) device (SiC diode).

Typical minimum R_{on} values for different I_L are given in Table 1. For realistic power loop inductance they are higher than the minimum R_{on} defined in DG1.

Figure 13 now in the same way compares realistic switch-“off” waveforms with those of Figure 11.

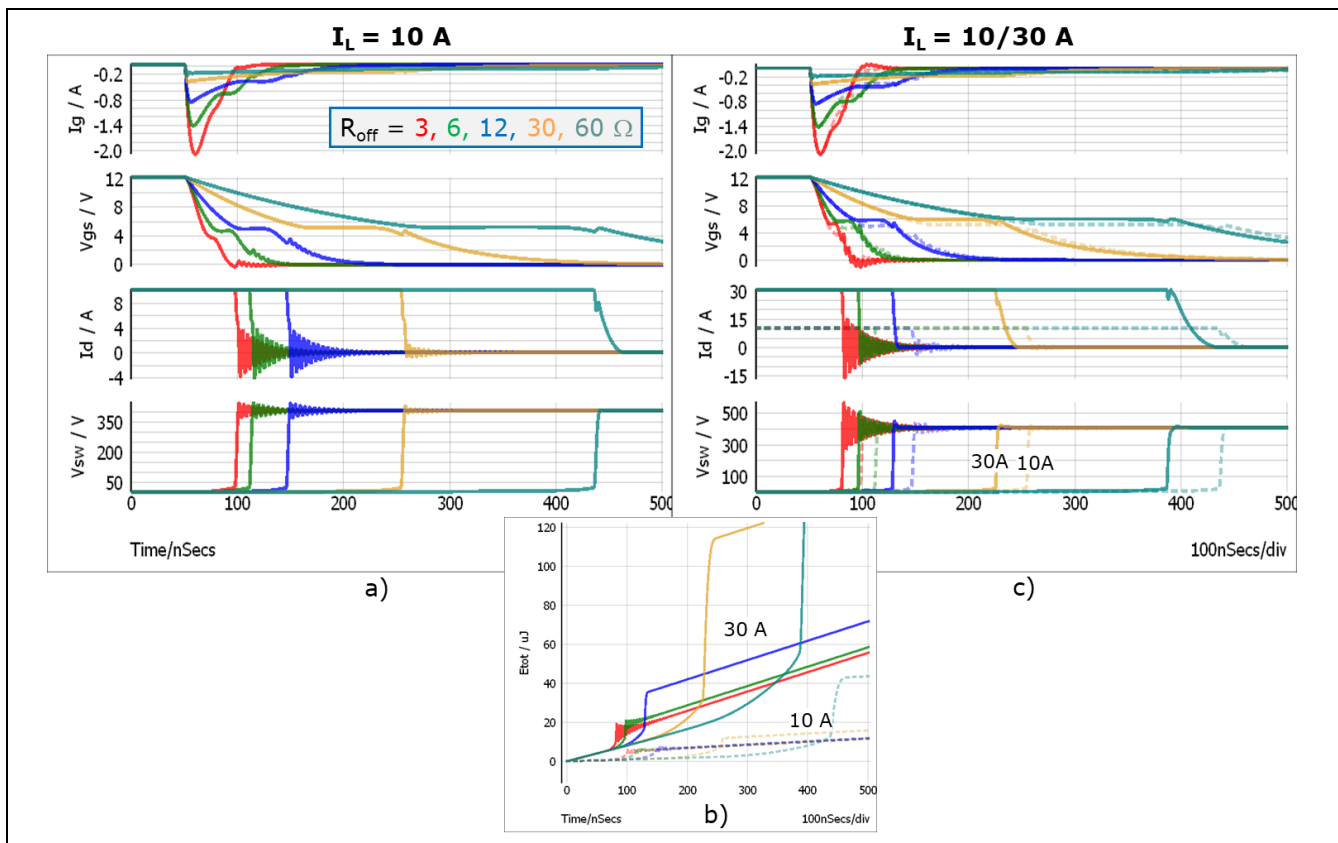


Figure 13 Switch-off waveforms over gate resistor at $I_L = 10\text{ A}$ (a), total losses (b) and waveform details at $I_L = 10\text{ A}$ (dashed lines) and 30 A (solid lines) (c)

Figure 13a) shows that the voltage overshoot at v_{sw} stays at reasonably low values, even for the lowest R_{off} of $3\ \Omega$. The delays have become somewhat shorter compared to Figure 11a); this is due to the resistive gate impedance that allows a larger gate current at the beginning of the transient (high v_{gs}). In contrast to switching “on”, the total transient time now strongly depends on the load current, as Figure 13c) clearly depicts. While 10 A is a typical average current, e.g. in a boost PFC, the maximum current under non-regular conditions like “AC-line cycle drop-out” can be up to three times higher. From Figure 13c), however, an I_L of 30 A (solid lines) would for the lowest R_{off} cause an overshoot voltage at the transistor terminals in excess of 200 V (more than 100 V at V_{sw}).

Transient behavior for single-switch 4-pin topologies (DG2, 3)

This leads directly to:

Dimensioning Guideline 3

Choose R_{off} sufficiently high to limit the voltage overshoot at the switch terminals to a safe value for the highest load current I_L under consideration

Some values of the minimum required R_{off} for different power loop inductance L_{loop} and load current I_L are again given in Table 1.

As the power loop inductance is usually unknown, it is recommended to measure the switching node voltage at a point with equal inductances to ground and bulk voltage, respectively. Then the actual voltage stress for both switches at their terminals can be derived from the measured waveforms by simply doubling the observed over-/undershoot voltages; no further knowledge of power loop inductances is needed. By contrast, the usual technique of measuring voltages as close as possible to the transistor or diode pins would require explicit numbers for the ratio of inner (package) to outer (PCB) inductance contributions.

Table 1 contains some practical gate resistor examples for different power loop inductance values.

Table 1 Minimum gate resistors vs. total power loop inductance for IPx65R095C7

L_{Loop} [nH]	R_{on} [Ω]	R_{off} [Ω]		
		$I_L = 10$ A	20 A	30 A
12	6	3	3	7
20	9	3	9	8
30	12	3	10	10

When using a CFD-type switch (e.g. IPx60R090CFD7), the values in Table 1 can be reduced by the difference of the internal gate resistors (5 Ω).

Transient behavior for half-bridge topologies (DG4 to 6)

8 Transient behavior for half-bridge topologies (DG4 to 6)

8.1 Topology 4hb in hard-switching operation

What happens if the high-side diode in the boost PFC topology of Figure 9 is substituted by a further CoolMOS™ switch? How does the resulting hard-switched half-bridge (Figure 14a and b) behave?

Part of the answer is shown in Figure 14c). The total capacitance seen at v_{sw} is the sum of $C_{oss,ls}$ and $C_{oss,hs}$. $C_{oss,hs}$ is the output capacitance of the high-side (hs) CoolMOS™ “diode”, i.e. the mirrored C_{oss} curve; it is added to the capacitance diagram of the low-side (ls) switch and compared with the capacitance C_{dio} of a 6 A SiC diode. It turns out that the capacitance of the transistor is significantly larger than that of the diode, particularly for high switch node voltage, i.e. at the beginning of the hard “on”-transient. As the output charge associated with $C_{oss,hs}$ is reflected in the area under the excess drain current, this means a dramatic increase in peak current and transient time, resulting in typically 10 times higher E_{on} losses. In addition, the high peak current causes a steep current decay (according to equations (1) and (2)) and thus high overshoot voltages. Even at moderate gate current the “diode” is driven into avalanche. Besides, the fast voltage transient induces a positive voltage peak at the v_{gs} of the high-side switch that may lead to cross-conduction (“spurious turn-on”) and even instability.

To make things worse, a significant amount of charge has to further be added to the pure C_{oss} -related part. It is the reverse recovery charge of the body diode, as the hs switch has to be in “off”-state, before the hard transient is initiated by switching “on” the ls switch (Figure 14a). I_L thus flows through the hs body diode and Q_{rr} is the associated charge required to switch off this current and reverse the voltage. To provide a feeling for the relations of the involved charges: the capacitive charge of a SiC diode is in the 10 nC range, whereas Q_{oss} of a 95 mΩ C7 switch equals 300 nC. Q_{rr} is in the same range for the CFD family, while it is again 10 times larger for C7, i.e. a few μ C. Finally this simply means that current SJ MOSFETs are not suited to continuously operate under hard commutation conditions in half-bridge topologies.

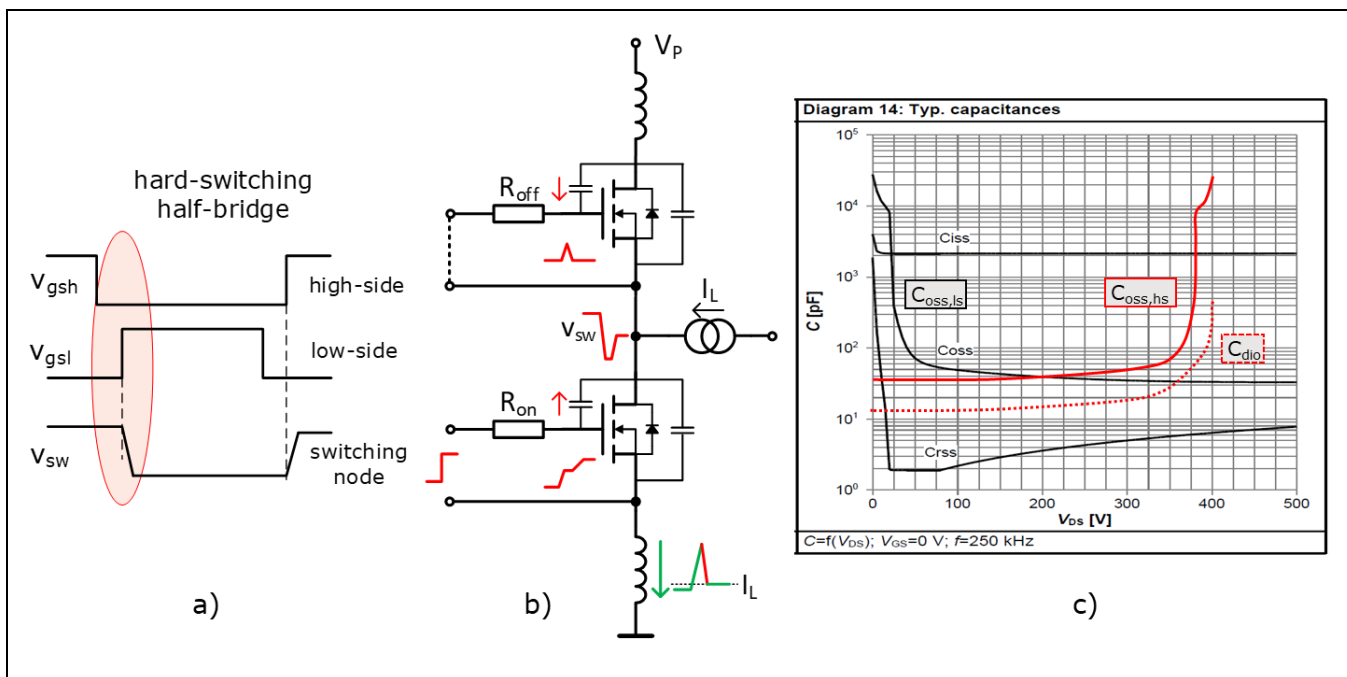


Figure 14 Hard-switched half-bridge: signals (a), basic schematic (b) and capacitance curves (c)

Transient behavior for half-bridge topologies (DG4 to 6)

8.2 Soft-switching half-bridge topologies (DG4)

By definition soft-switching means near-zero V_{ds} when turning “on” a switch. To achieve this, the transient of the switch node voltage has to happen before this turn-on, i.e. during the dead-time, when both switches in a half-bridge are “off”. The transient then is caused by the external current I_L and initiated by switching “off” the conducting switch. Obviously, to ensure both transitions are soft, I_L has to change polarity between the switching events. This situation is depicted in Figure 15a). A typical example can be found in LLC applications with the triangularly shaped “magnetizing current” that drives the switching transients.

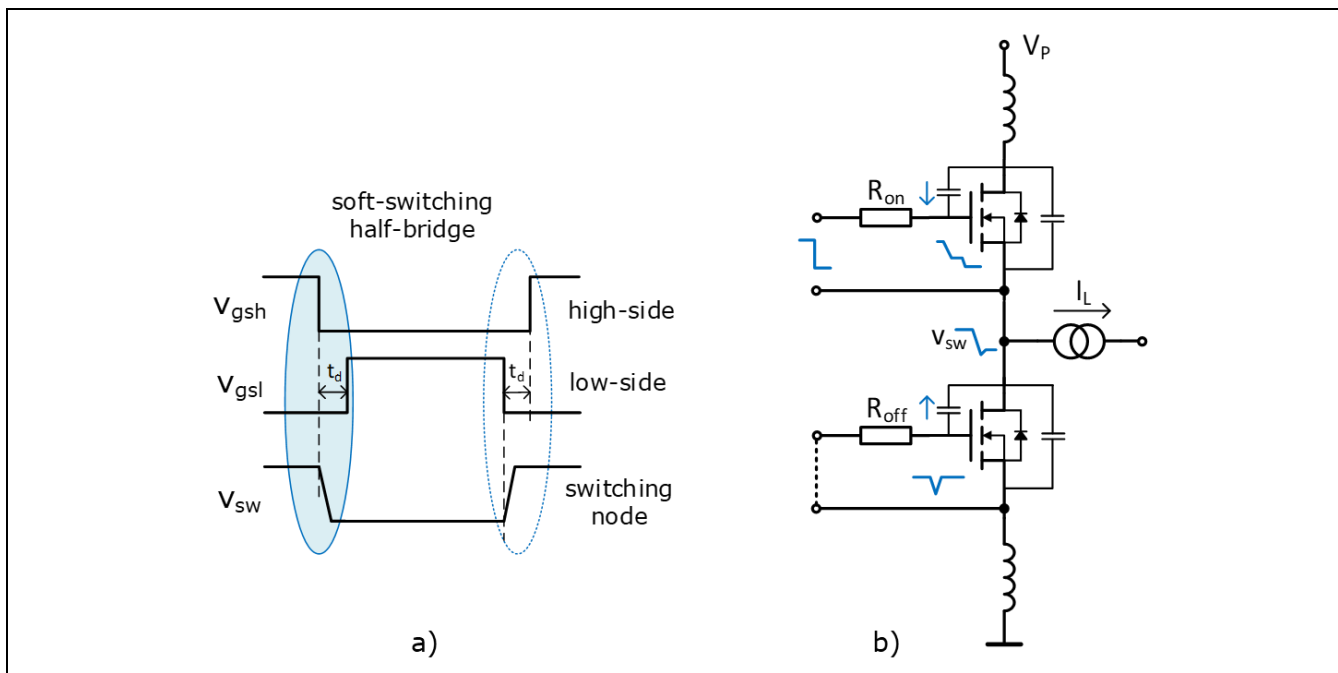


Figure 15 Soft-switched half-bridge: control and output signals (a) and basic schematic (b)

In Figure 15b) the falling v_{sw} transient is depicted. The transient is initiated by switching “off” the high-side switch, and an I_L of a few amps, but of opposite polarity compared to Figure 14, drives v_{sw} down. The transition must be finished (with I_L flowing in the body diode of the low-side switch) before the dead-time t_d ends and the low-side is switched “on”, commutating I_L from body diode to transistor channel. This, however, is rather uncritical, as no current and voltage changes happen in the power loop. The impact of the voltage transient on the passive (low-side) v_{gs} is also indicated. It causes a small negative spike; there is no possibility for any kind of cross-conduction. The second transient looks completely equal, but with high- and low-side interchanged.

Simulation confirms the above. In Figure 16a) the simulation circuit is shown: now switches of the CFD family are used (IPL60R075CFD7), again with internal inductances and gate resistors set to zero. I_L is chosen to have a constant value and changing polarity as indicated. Obviously, if “dead-time charge” Q_{dt} , the product of I_L and t_d , equals the total output charge $2 \cdot Q_{oss}$, (~ 800 nC), soft-switching can be ensured. Simulations indicate that with an I_L of 5 A a dead-time of 150 ns is sufficient. The waveforms given in Figure 16b) look very smooth, and switching losses are in fact negligible.

Transient behavior for half-bridge topologies (DG4 to 6)

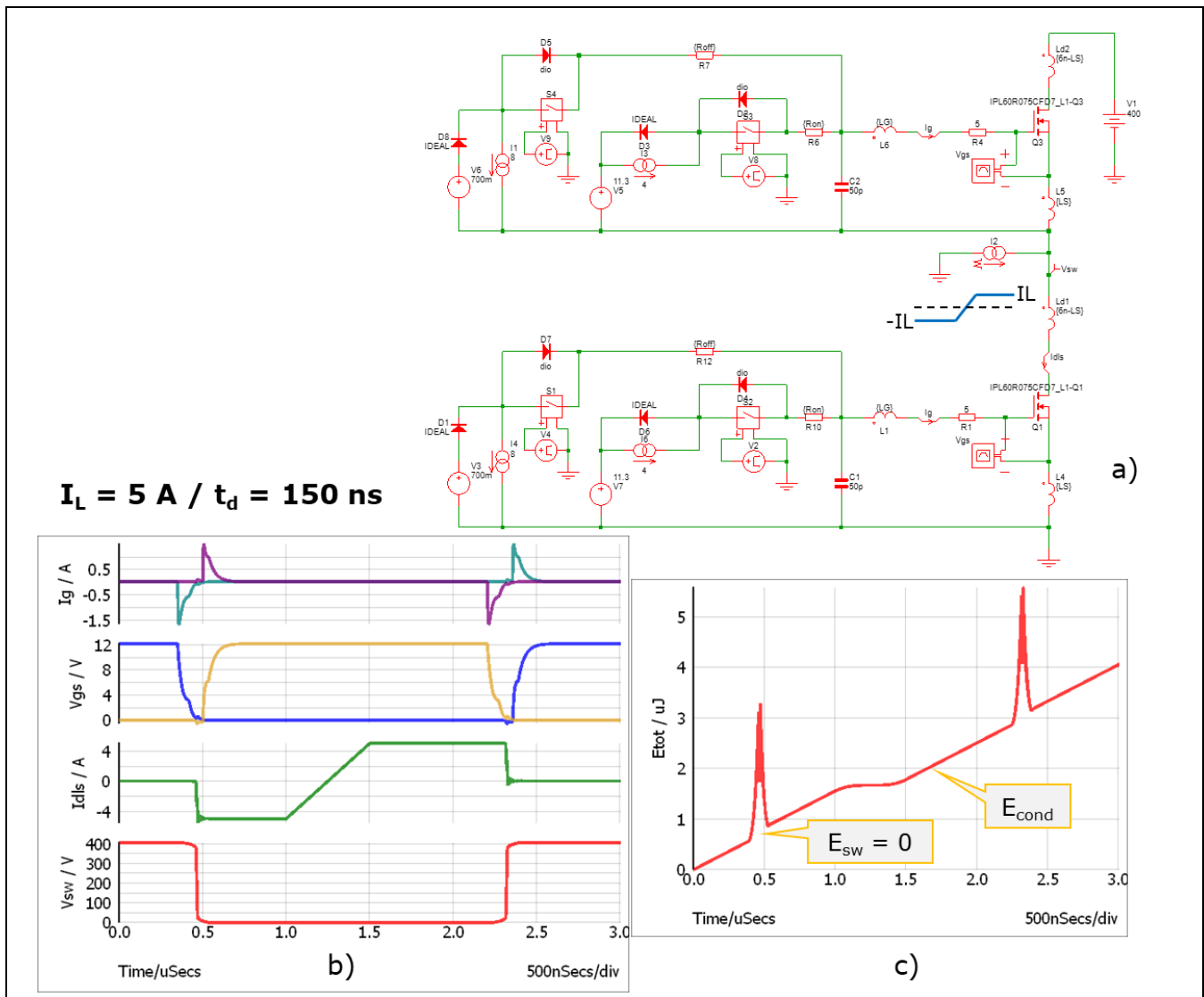


Figure 16 Simulation circuit (a), waveforms (b) and total losses (c) for soft-switching half-bridge

For maximum efficiency it is usually beneficial to keep the dead-time short. This is why any switching-off delay should be avoided and R_{off} chosen to be as small as possible. R_{on} is more or less uncritical.

Dimensioning Guideline 4
In purely soft-switching half-bridge applications choose R_{off} equal to R_{min} as calculated from DG1) to minimize delay and dead-time; as R_{on} is uncritical, it can be chosen to be equal to R_{off} to enable a single gate resistor.

Again, due to the intentionally increased internal gate resistor, CFD switches usually need no external resistor. The waveforms of Figure 16b) have been simulated without inductances, but their introduction keeps the results nearly unchanged.

Transient behavior for half-bridge topologies (DG4 to 6)

8.3 Partial hard-switching (DG5, 6)

So far CoolMOS™ half-bridges are easy to handle: hard-switching is not possible and soft-switching is uncritical. The most interesting case, however, is none of these. It is the practically relevant situation, when in soft-switching systems under certain conditions dead-time t_d and/or current I_L are too low to guarantee that the transient of the switching node has been completed prior to switching “on”. In other words, during the dead-time only part of the total output charge ($2 Q_{oss}$) of the “off”-switching transistor is delivered by the magnetizing current I_L . Due to the concentration of the output charge components at very high and very low v_{ds} (Figure 14c), a “dead-time charge” somewhat larger than half the total output charge ($Q_{dt} > Q_{oss}$) results in small v_{ds} at turn-on and low switching losses, whereas $Q_{dt} < Q_{oss}$ gives large v_{ds} and high losses. The difference $Q_{oss} - Q_{dt}$ appears as a drain current peak when switching “on” the opposite device. Thus both switches are involved in the transient. This “partial hard-switching” situation is depicted in Figure 17 for the falling edge of v_{sw} (for the rising it is completely symmetrical with switch functions and I_L polarity changed); it may happen in LLCs during start-up or load changes.

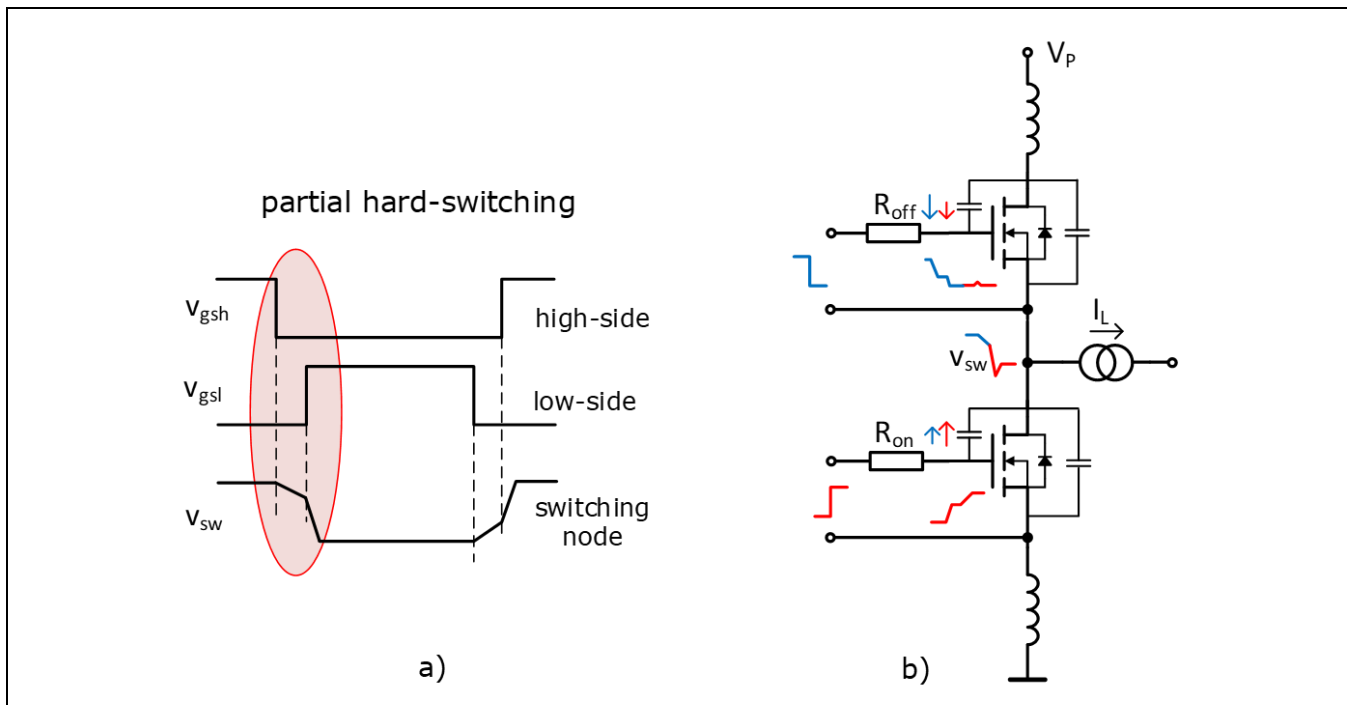


Figure 17 Partial hard-switching: control and output signals (a) and basic schematic (b)

The simplest way to simulate the effects described is to reduce I_L in the circuit of Figure 16a). Taking into account that the critical charge Q_{oss} is about 400 nC, and that the actual dead-time is lower than the 150 ns seen at the driver output due to the relatively slow turn-off, we would expect the critical I_L between 3 and 4 A. This is exactly what we can observe in Figure 18, showing waveforms and losses when varying I_L .

Transient behavior for half-bridge topologies (DG4 to 6)

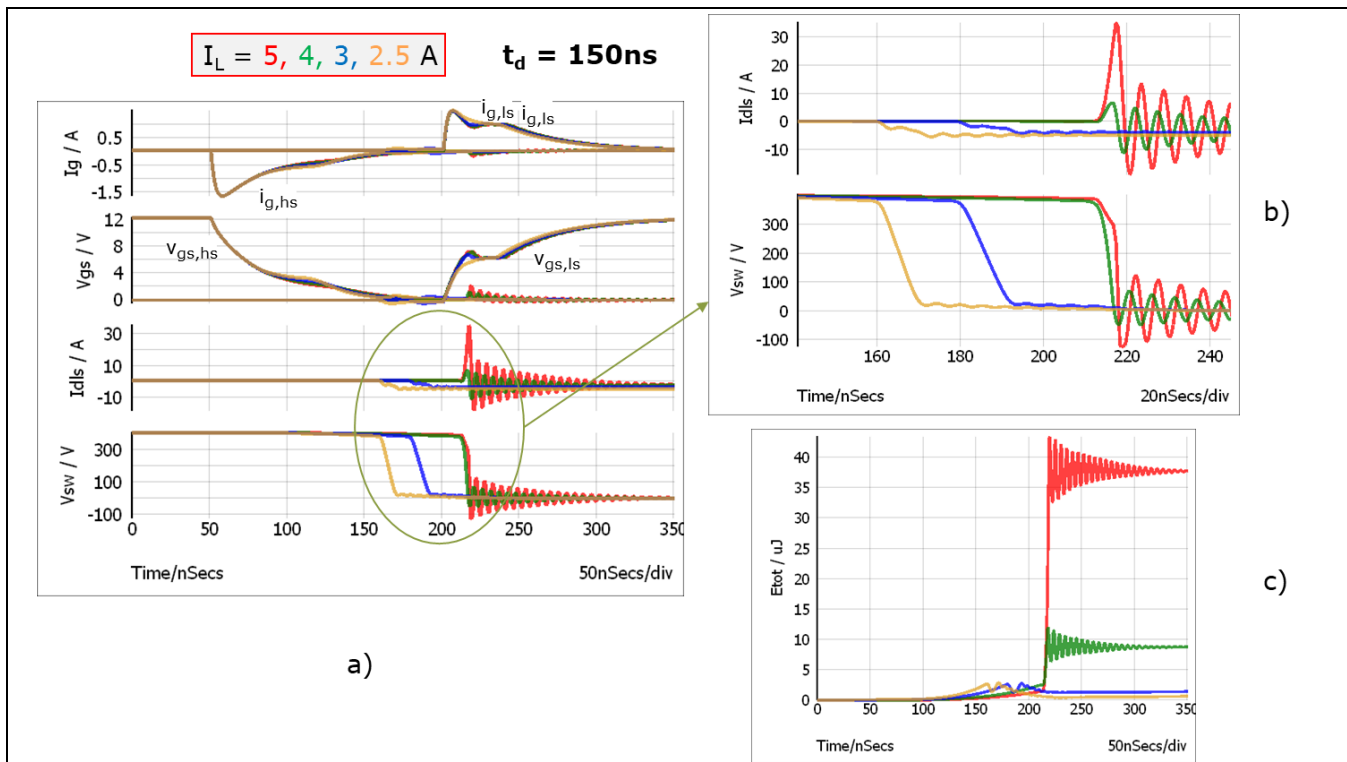


Figure 18 Partial hard-switching depending on I_L : waveforms (a), details (b) and losses (c)

While for 4 A and 5 A the transition is nearly finished when the low-side is switched “on” (at $t = 200$ ns), for 3 A it is not. Here Q_{dt} is lower than Q_{oss} , and the hard-switched “rest charge” Q_{hs} corresponds to the area under the ~ 8 A current peak of i_{dls} (green curve in upper graph of Figure 18b). It is in the 10 to 20 nC range, similar to the output charge of a SiC diode, and low compared to a typical Q_{oss} . Losses and voltage stress correspond to the results obtained in chapter 7, taking into account the large internal R_g of CFD-type switches.

With decrease of I_L , peak current, rest charge and losses strongly increase; for $I_L = 2.5$ A the respective values are 35 A, 100 nC and 40 μJ. The switch node voltage, however, reaches -125 V, which means that v_{ds} of the high-side switch exceeds $400 + 2 \cdot 125 = 650$ V (at this value the voltage is clamped in the transistor model).

Further lowering of I_L dramatically increases stress. So the question arises, if there are any measures to improve this behavior and allow a higher Q_{hs} in the partial hard-switching situation without jeopardizing reliability and lifetime. As the voltage stress depends on the peak drain current, it can be influenced by the gate current according to Eq. (1). The standard method to reduce the gate current is of course to increase the gate resistor. Figure 19 shows the effect for a magnetizing current of 2 A, corresponding to a rest charge Q_{hs} of about 200 nC.

Transient behavior for half-bridge topologies (DG4 to 6)

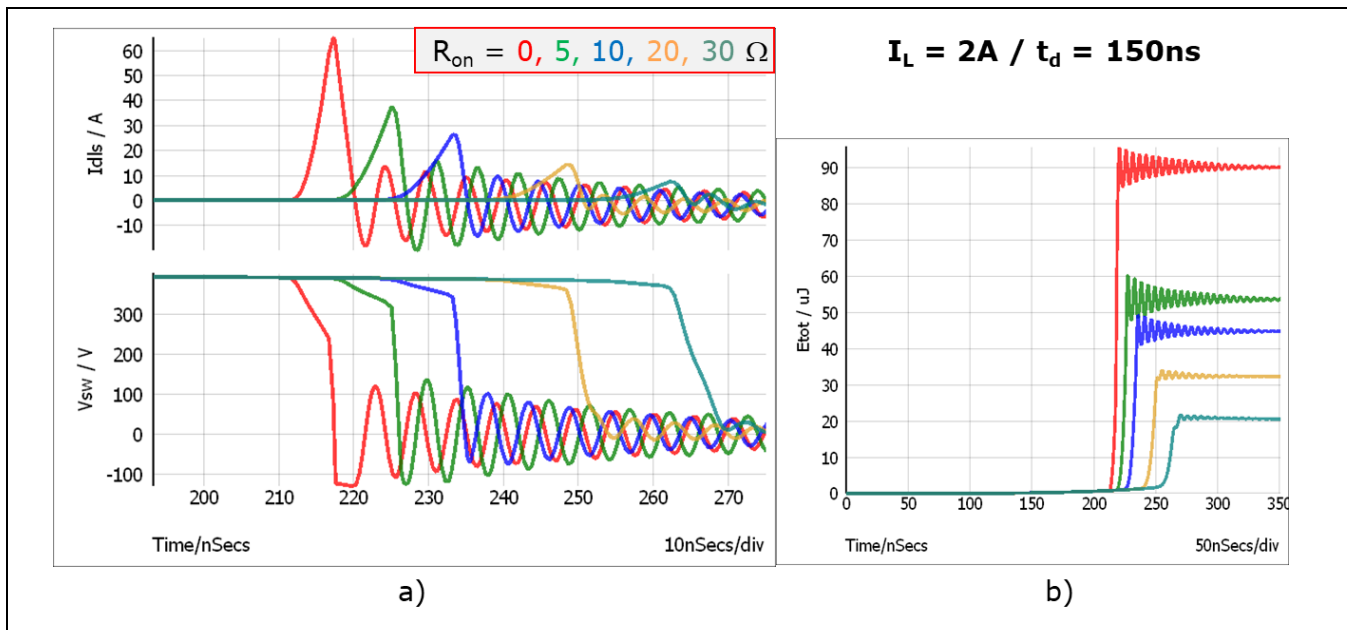


Figure 19 Effect of R_{on} on switching waveforms (a) and losses (b) for partial hard-switching

At first sight it seems not evident that slower switching decreases losses (Figure 19b). The reason is that by decreasing the gate current also the “on”-transient is delayed, and this lengthens the effective dead-time and thus reduces the hard-switched charge Q_{hs} . Besides, the voltage clamp causes avalanche, thereby further increasing Q_{hs} for $R_{on} = 0$. In the simulated case a resistor of 10Ω would be sufficient for acceptable voltage stress. And a gate resistor of 30Ω would do the job even for zero magnetizing current; however, it would lead to a slight increase in losses also in the regular soft-switching case due to the delayed switch-on and longer body-diode conduction time.

But there is an alternative way to reduce the gate current. In a standard 3-pin package the source inductance is included in both gate and power loop (Figure 1). The voltage induced in this common source inductance L_{sc} by any changing switch current subtracts from the driver supply and thereby influences i_g . A rising current in the power loop reduces i_g as indicated in Figure 20a). Figure 20b) depicts the simulated i_d and v_{sw} waveforms for different L_{sc} values from 0 to 4 nH, which is in accordance with the package spectrum available for CoolMOS™ switches.

Transient behavior for half-bridge topologies (DG4 to 6)

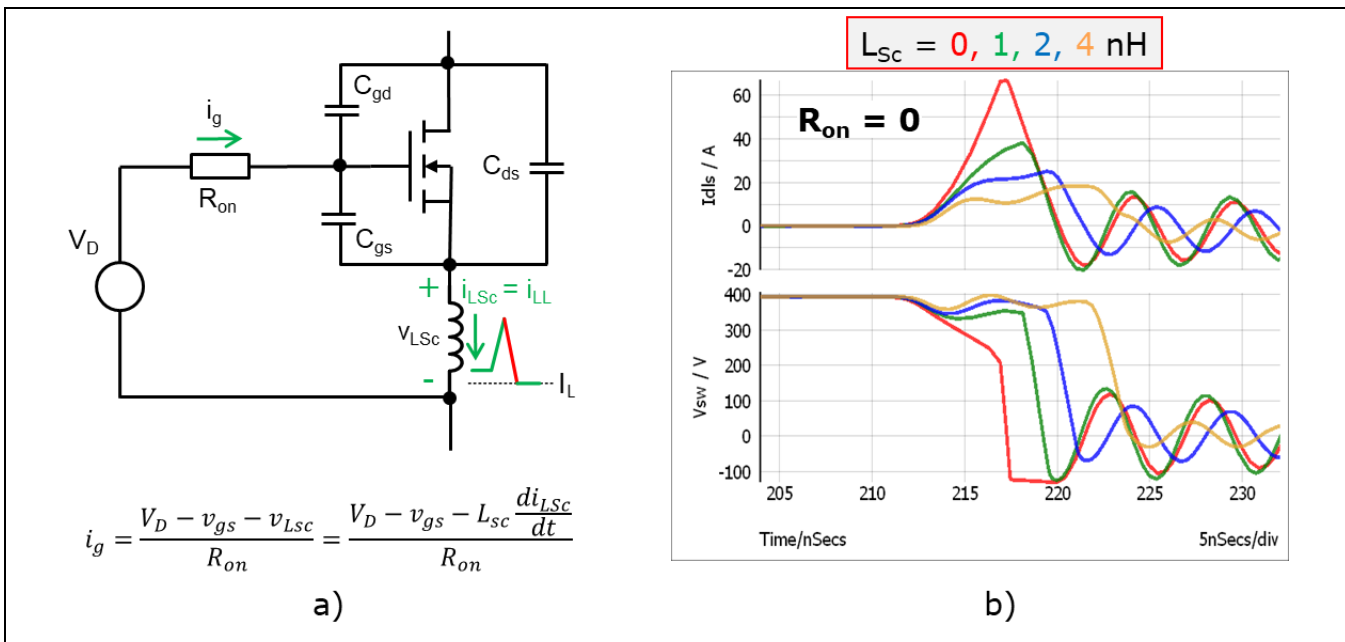


Figure 20 Effect of common source inductance: equivalent circuit (a) and waveforms (b)

It demonstrates a significant reduction of peak current and voltage stress with increasing L_{sc} ; the additional delay is rather short. Losses are similar to those in Figure 19, but they are of less importance, as partial hard-switching is not the regular case in the intended applications. And in regular soft-switching operation the introduction of a common source inductance has virtually no effect. We thus can formulate:

Dimensioning Guideline 5

When partial hard-switching can happen in half-bridge applications, 3-pin switches should be used; 4-pin devices cannot be recommended.

Depending on the highest possible hard-switched “rest charge” Q_{hs} , in addition an increase of R_{on} could be helpful.

Dimensioning Guideline 6

If in partial hard-switching applications even with 3-pin switches the voltage/current stress is still too high due to low L_{sc} and high Q_{hs} , in addition an increase of R_{on} is recommended.

To give an example: up to a Q_{hs} of 200 nC the CFD7 switch can be operated with zero external gate resistor R_{on} (R_{off} can anyway be zero due to the internal gate resistor). If the magnetizing current can also become zero in worst case, i.e. $Q_{hs} = Q_{oss} = 400$ nC, an additional gate resistor of 10 to 20 Ω helps to limit over-voltage in case of low L_{sc} packages.

Single switch with common source inductance (DG7 to 9)

9 Single switch with common source inductance (DG7 to 9)

9.1 The effects of L_{sc}

We have seen that in the usually soft-switching CoolMOS™ half-bridge 3-pin switches with common source inductance are beneficial to limit stress on the switches in abnormal conditions (partial hard-switching). The influence of L_{sc} in normal operation is negligible.

This is definitely not true for the single-switch topology of Figure 21.

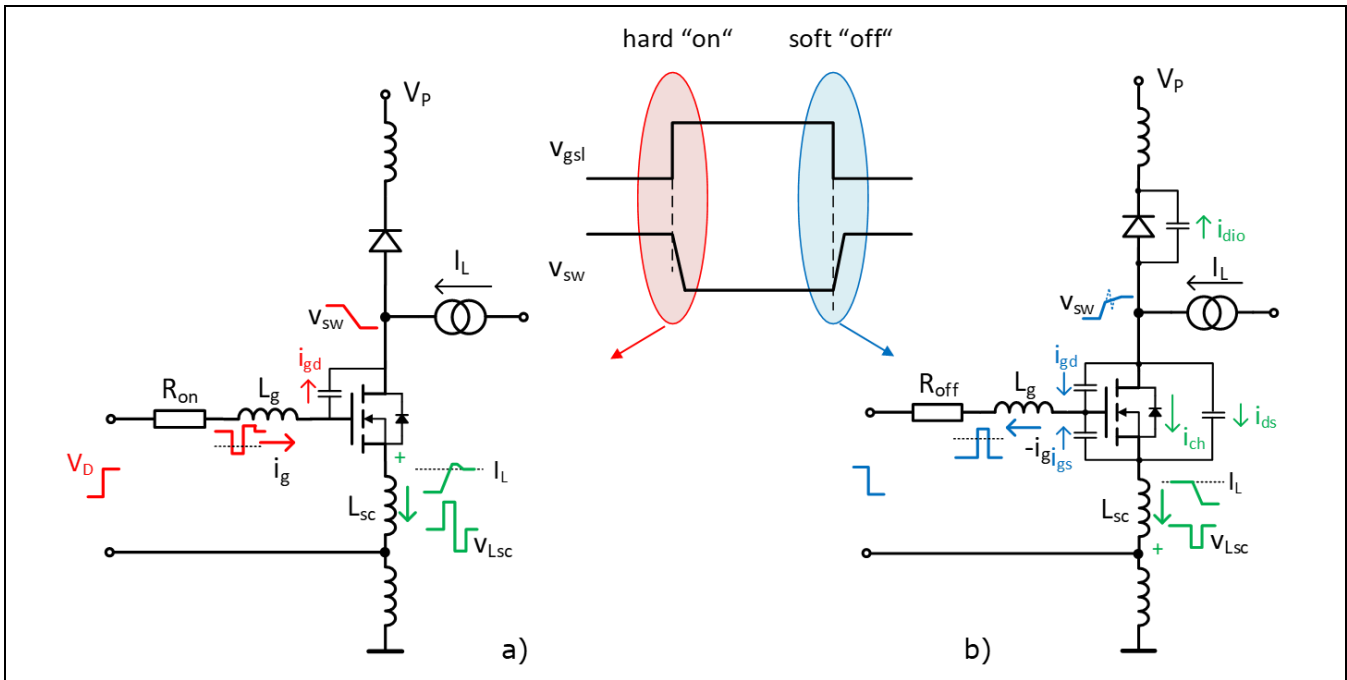


Figure 21 3sw topology with hard switch-on (a) and soft switch-off (b) transients

Compared to the 4-pin situation of Figure 9 there is now an additional interaction between gate and power loop. Any current change in L_{sc} causes an inductive voltage drop that simply adds to the driving voltage. If we ignore for the moment the effect of gate inductance L_g (will be covered in chapter 9.4), Eq. (3) in 7.1 has to be modified to:

$$i_g = \frac{V_D - v_{gs} - v_{Lsc}}{R_{on}} = \frac{V_D - v_{gs} - L_{sc} \frac{di_{Lsc}}{dt}}{R_{on}} \quad (3a)$$

For the switching-on event in Figure 21a) the rising current causes a positive v_{Lsc} that reduces the gate current. In switching phase 2 (prior to the voltage transient), di_{Lsc}/dt is rather constant and proportional to dv_{gs}/dt , which in turn is proportional to i_g (eq. 1). But a linear relation between v_{Lsc} and i_g means that in this switching phase L_{sc} acts like an increased gate resistor of value $R_{eq} = g_m L_{sc} / C_{gs}$. This is in the several tens of ohms range and thus is typically higher than the physical R_{on} , causing lower gate current, slower switching and increased losses.

This effect of L_{sc} is well known and described in literature. Not so well known is that the mechanism for switching off is somewhat different and again strongly related to the non-linear capacitances. When the transient starts, C_{ds} is huge compared to C_{dio} . Even if the channel current i_{ch} is switched off very fast, it is just shifted to i_{ds} to charge capacitance C_{ds} (Figure 21b). However, it is the sum of i_{ch} and i_{ds} that flows through L_{sc} ,

Single switch with common source inductance (DG7 to 9)

and this current stays constant as long as V_{ds} is low; no voltage is induced in L_{sc} . But as soon as C_{ds} exhibits its sharp decline (at $V_{ds} \sim 20$ V), the charging current distribution between C_{ds} and C_{dio} changes and causes a negative di/dt in L_{sc} . The resulting v_{Lsc} can be rather high (up to several tens of volts for large I_L), and according to Eq. (3a) it acts as a positive gate drive voltage that easily can turn on the channel again and as a consequence cause oscillations and instabilities. A more detailed analysis can be found in [1]. As shown there, the resulting v_{Lsc} depends on the square of the charging current. This effect thus becomes dominant and has to be considered carefully, when high current has to be switched off fast.

9.2 Switch-on waveforms (DG7)

The curves of Figure 22a) are similar to those of Figure 12c). They demonstrate the effect of L_{sc} for the “on” transient as discussed above. L_{sc} is increased from 0 to 4 nH with the total loop inductance kept constant. R_{on} is fixed at 6 Ω as the minimum required for zero L_{sc} . So the red curves correspond to the green ones of Figure 12.

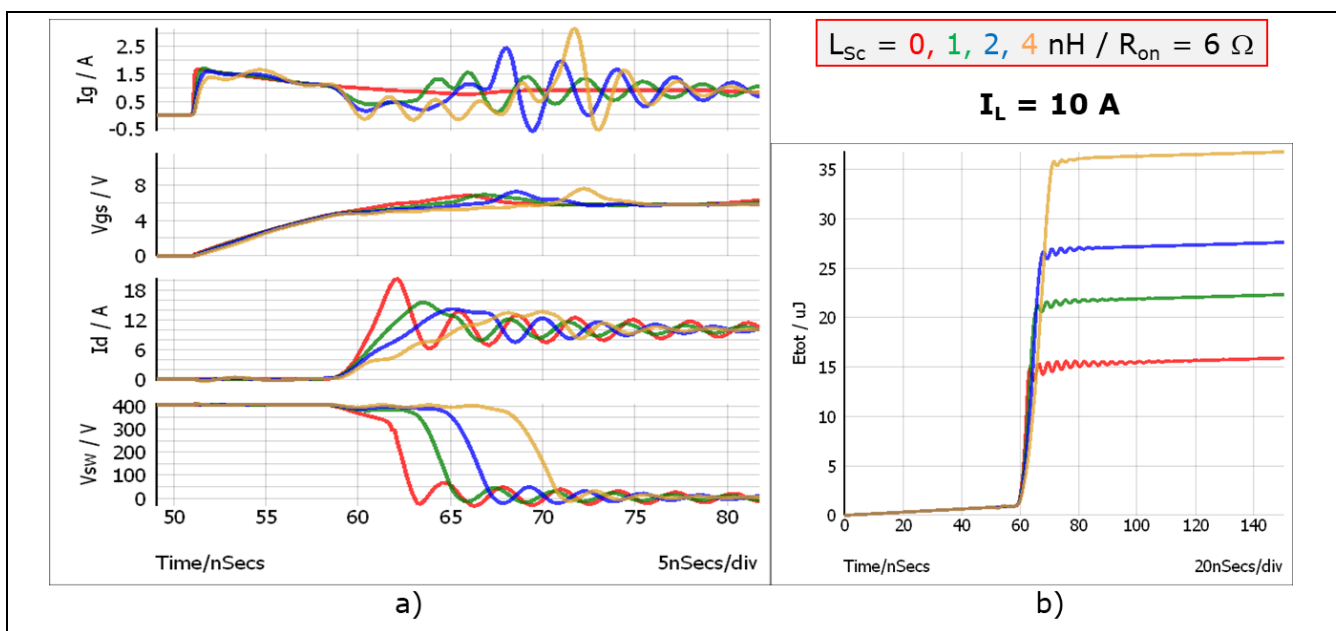


Figure 22 L_{sc} effect for switching “on”: waveform details (a) and losses (b) for fixed R_{on}

We clearly see the expected behavior. As soon as i_d starts to rise (at $t = 60$ ns) the inductive voltage drop over L_{sc} subtracts from gate drive voltage and thus reduces the gate current. So the voltage transient takes longer and the losses increase. An L_{sc} of 4 nH results in similar losses as a gate resistor of 30 Ω ; however, the delay is shorter, as the charging of C_{gs} up to the Miller level happens at high gate current.

Nevertheless, this comparison is not completely fair. The chosen R_{on} of 6 Ω is only required for zero L_{sc} and could be reduced for the other cases, depending on the L_{sc} value. In Figure 23 the minimum R_{on} required to keep v_{sw} safely above -100 V has been independently chosen for each L_{sc} value. In Figure 23b this yields the interesting result that with optimized R_{on} losses with an L_{sc} of 1 or 2 nH are similar or even lower than for zero L_{sc} . This is valid for moderate current levels, e.g. 10 A (Figure 23b). For significantly higher current (30 A in Figure 23c), the 4 nH case, corresponding to a 3-pin TO package, exhibits a dramatic increase in losses. However, such a current level is usually not reached in normal operation, and the relevance of these losses has to be treated separately for any specific application.

Single switch with common source inductance (DG7 to 9)

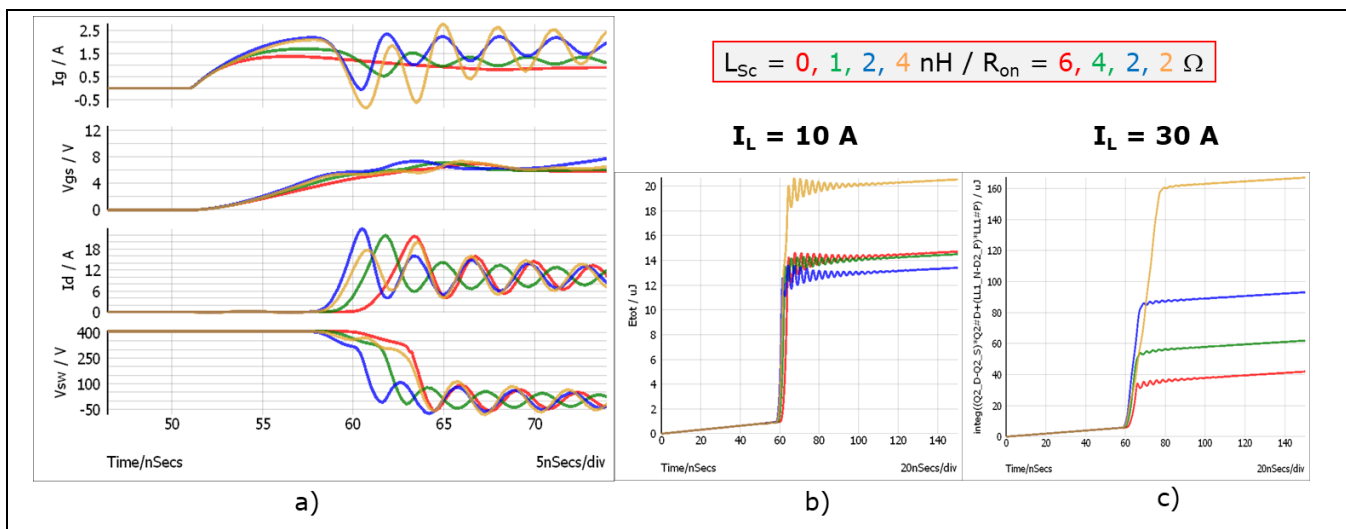


Figure 23 L_{Sc} effect for switching “on”: waveform details (a) and losses (b) for optimized R_{on}

Dimensioning Guideline 7

Compared to their 4-pin counterparts, 3-pin devices in single-switch applications can be operated at lower R_{on} . It is recommended to use the minimum value required to guarantee a safe peak voltage for the passive device.

Example values can be found in Figure 23.

3-pin TO packages can often be operated without an external gate resistor; approximately 1Ω is the contribution of the gate driver.

9.3 Switch-off waveforms (DG8)

In Figure 24 the simulation is repeated for the “off” transient, i.e. L_{Sc} is increased, while R_{off} is held at the minimum value of 3Ω (resulting from DG1). And it is obvious that there are really significant differences regarding the effect of L_{Sc} . While for the switching “on” transient the common source inductance acts like an additional gate resistor 10 ns after the transient has been initiated ($t = 50 \text{ ns}$), the situation is completely different for switching “off”.

There is no additional delay of the transient, as it would result from increasing R_{off} (Figure 13). And L_{Sc} has no effect, until v_{sw} reaches about 20 V (C_{ds} decline). This, however, happens rather late, almost 50 ns after the transient has started. A potential fast channel turn-off is thus not affected by L_{Sc} , but with the shift of charging current from C_{ds} to C_{dio} the resulting v_{LSc} acts as a positive voltage within the gate loop, causing the observed positive gate current and the associated gate voltage increase indicated in Figure 24a). If v_{gs} exceeds the threshold voltage V_{th} sufficiently to again turn on the transistor channel, not only do the losses increase, but even oscillations and instabilities may result.

Single switch with common source inductance (DG7 to 9)

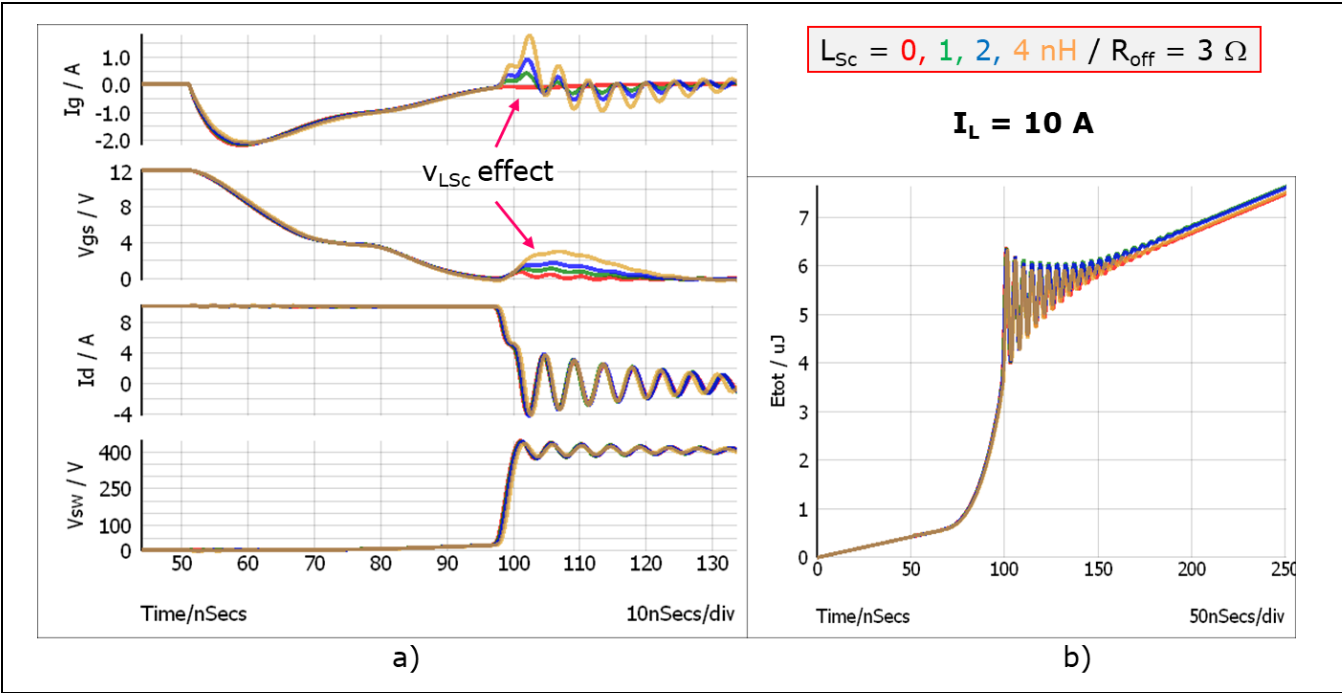


Figure 24 L_{Sc} effect for switching “off” at moderate current: waveform details (a) and losses (b) for fixed R_{off}

This obviously does not happen at the moderate 10 A current level in Figure 24 and there is no impact of $v_{L_{Sc}}$ regarding losses. But as deduced in [1], $v_{L_{Sc}}$ is proportional to the square of the charging current, and this in turn depends on I_L . For fast channel turn-off the charging current is equal to I_L at the time when $-di_{L_{Sc}}/dt$ reaches its maximum due to the capacitance changes. So Figure 25 shows the critical case of fast switching “off” a high current of 30 A, a situation that can temporarily happen in PFC applications (“AC-line cycle drop-out”).

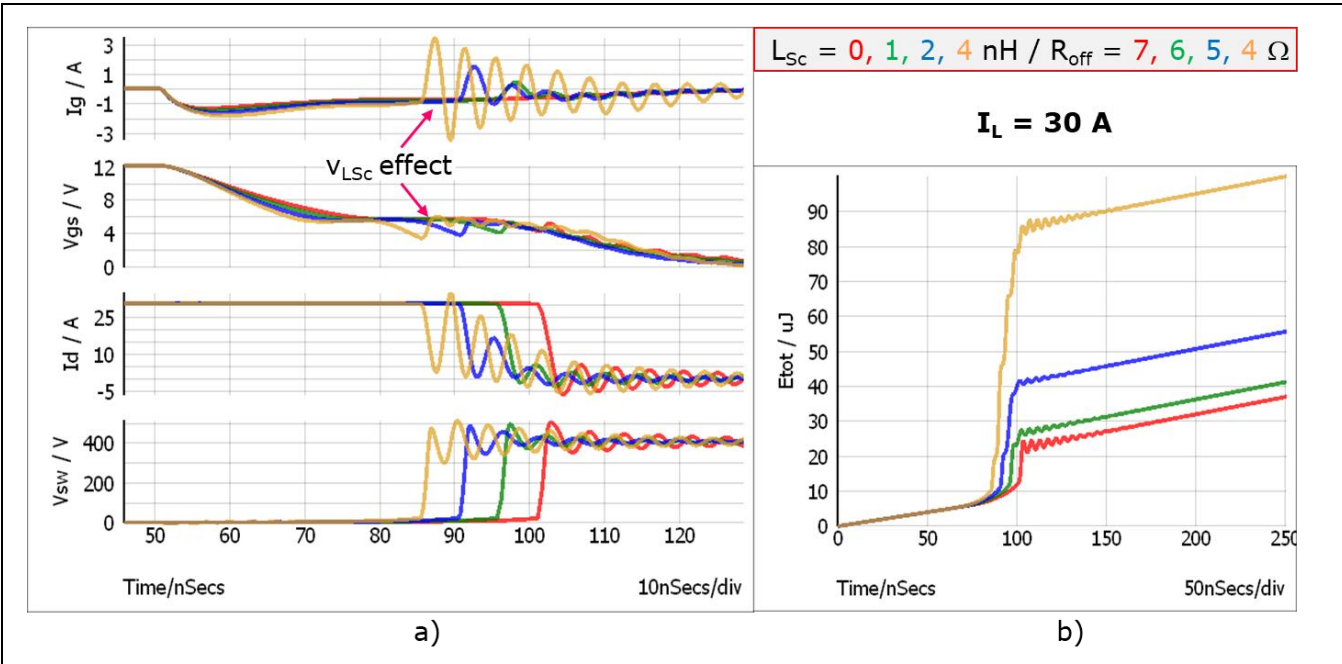


Figure 25 L_{Sc} effect for switching “off” at high current: waveform details (a) and losses (b) for optimized R_{off}

Single switch with common source inductance (DG7 to 9)

Now, due to the higher charging current, the v_{LSc} peak (not shown in Figure 25) is large (80 V for $L_{Sc} = 4$ nH) and appears earlier (at $t = 85$ ns). The associated positive gate current causes an increase in v_{gs} that for 4 nH is large enough to fully turn the switch “on” again, as can be seen in the i_d waveform. Clearly this leads to significant losses increasing from 10 to about 80 μ J, although in Figure 25 the gate resistor has been adapted to the minimum value necessary to fulfill overshoot limits. For 4-pin packages this minimum is 7 Ω (see also Table 1); it can be reduced to 4 Ω with the 4 nH source inductance. However, as the total gate impedance determines the gate current peak for a given v_{LSc} , decreasing R_{off} might become critical with respect to oscillation sensitivity, particularly if the gate inductance is small. DG8 summarizes the findings.

Dimensioning Guideline 8

For moderate current levels, 3-pin switches can be operated at the minimum R_{off} (DG1).

For very high current, R_{off} must eventually be increased both to limit over-voltage and avoid turn-on-induced oscillations.

Nevertheless, usually the required R_{off} is lower than for 4-pin switches; example values are given in Figure 25.

Single switch with common source inductance (DG7 to 9)

9.4 The role of gate inductance L_g (DG9)

Regarding gate loop impedance, the common assumption is that it is always beneficial to minimize the gate inductance L_g and define the gate current by the gate resistor only. Although this is often a good strategy, it is not in every case. For 3-pin switches with high common source inductance (4 nH), the gate inductance L_g plays an important role in shaping the gate current. This is demonstrated in Figure 26 for a complete switching cycle.

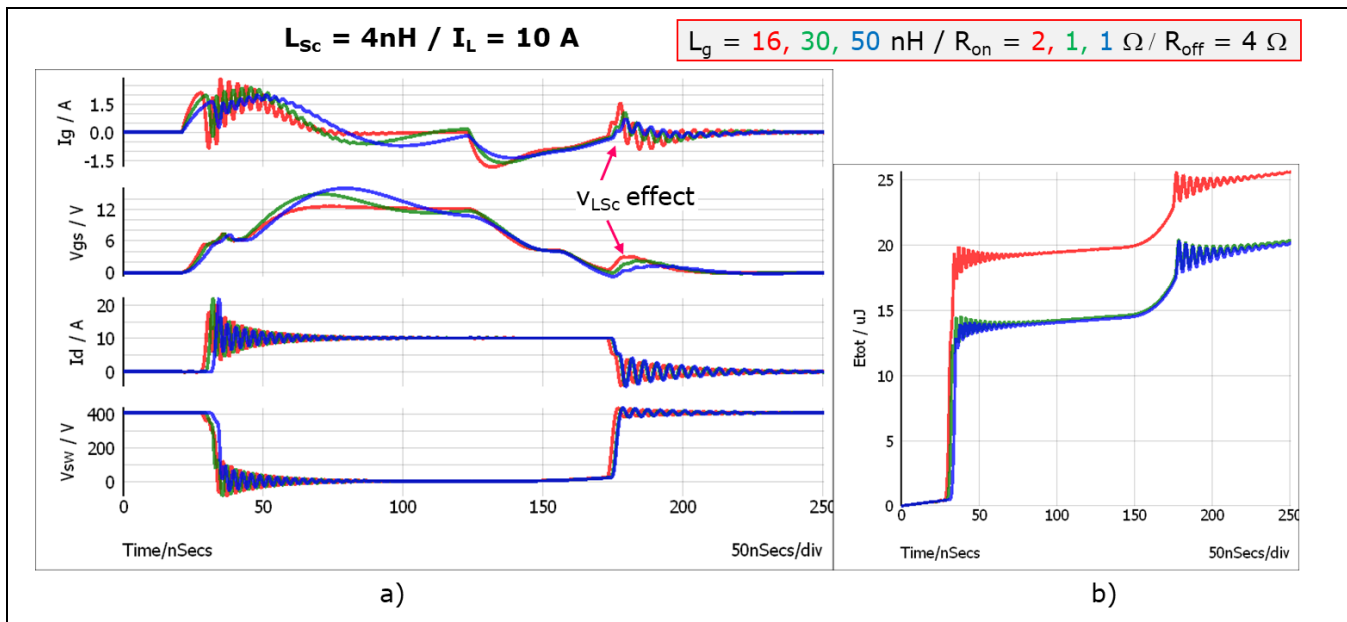


Figure 26 Effect of gate inductance: switching waveforms (a) and losses (b) for $L_{Sc} = 4$ nH at $I_L = 10$ A

Obviously an increase in gate inductance has a smoothing effect on the gate current (blue curves). Increasing L_g causes a slight delay, but finally a higher average gate current during the transient. For moderate current a gate inductance of 30 nH is able to completely compensate for the effects of L_{Sc} , because it acts as a kind of current storage loaded during the first switching phase (“delay”) and then providing sufficient gate current for a fast transient. The gate resistors in Figure 26 have again been minimized based on over-voltages. But the gate current is determined by the total gate impedance, so higher L_g allows lower R_g . However, as can be clearly seen, the damping criterion in the gate loop is not fulfilled any more, resulting in some overshoot of the gate voltage at a relatively low resonant frequency determined by L_g and C_{iss} . A few volts of overshoot in V_{gs} can usually be accepted, and so it is a reasonable strategy to shift gate impedance from resistance to inductance.

How does this look in the critical high-current case?

Single switch with common source inductance (DG7 to 9)

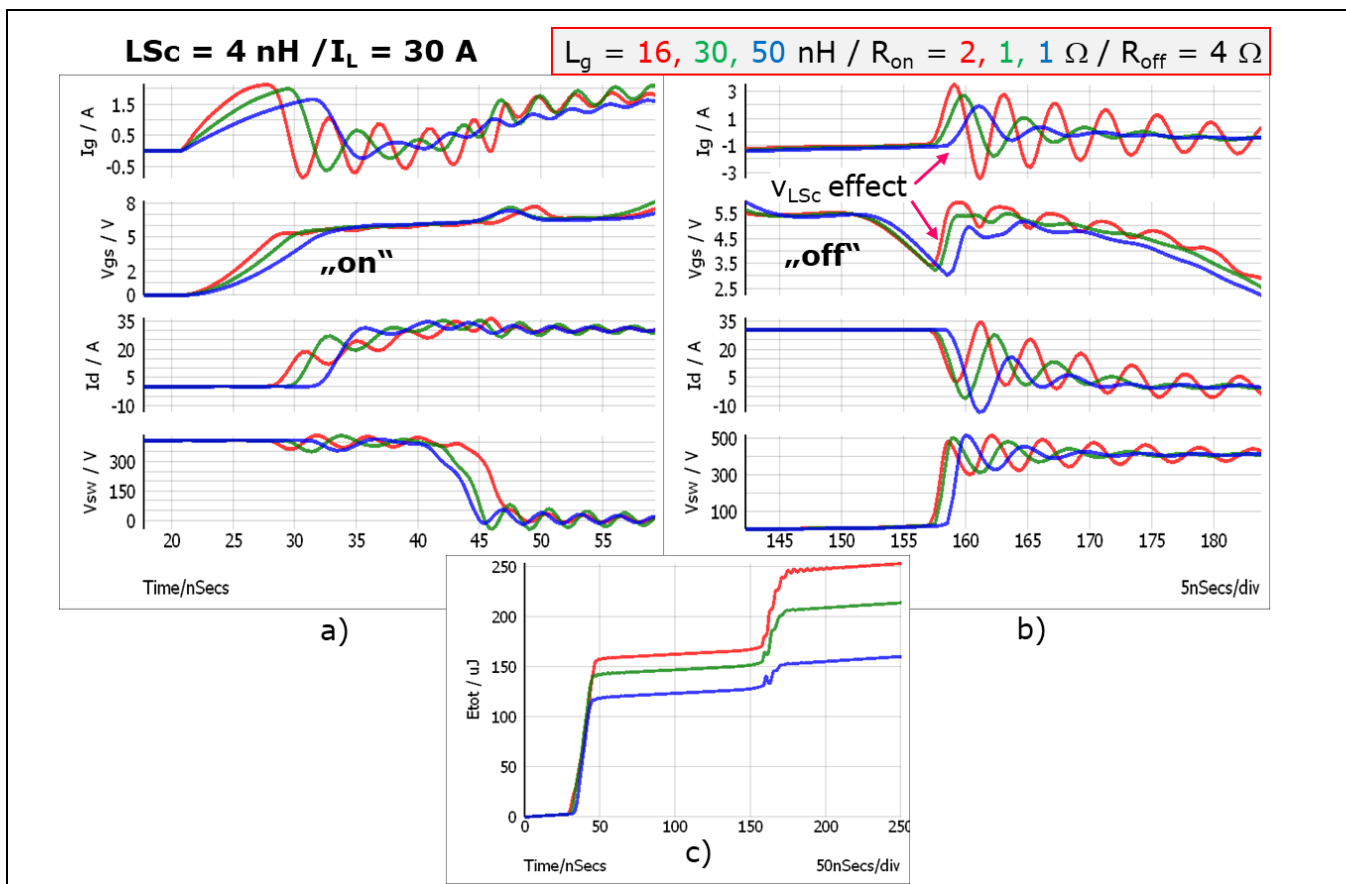


Figure 27 Effect of gate inductance: switching waveform details "on" (a) and "off" (b) and losses (c) for $L_{Sc} = 4 \text{ nH}$ at $I_L = 30 \text{ A}$

From the detailed gate current waveforms in Figure 27a) the smoothing effect of L_g is again evident. Particularly noticeable are the critical positive gate current peaks in the switching "off" waveforms of Figure 27b). The blue gate current peak resulting from $v_{L_{Sc}}$ is not only smaller, but also happens later and at a lower v_{gs} , finally resulting in a less severe re-turn-on and much lower "off" losses (20 versus 80 μJ).

The chosen gate inductance values are 16, 30 and 50 nH, respectively. At least the first two are within the range of realistic parasitic gate loop inductances. This leads to our final dimensioning guideline.

Dimensioning Guideline 9

An increase of gate inductance L_g can significantly improve switching performance of 3-pin switches. PCB layout measures to minimize L_g cannot be recommended. As a rule of thumb, L_g should be in the $10 \times L_{Sc}$ range.

Single switch with common source inductance (DG7 to 9)

9.5 Gate voltage measurement for 3-pin switches

It was mentioned in chapter 5 that the measurement of the gate-to-source voltage is difficult for high-side switches due to the fast and high common-mode content. With 3-pin switches, it is not only difficult, but basically impossible to get relevant information about v_{gs} by measurement.

Figure 28 compares the internal gate-source voltage (v_{gsint}) with the measurable voltage at the switch pins (v_{gsmeas}). The huge difference is due to the fact that v_{Lsc} is necessarily included in the measurement. There is no realistic way to derive the real transistor terminal voltage from the measured voltage; even with appropriate low-pass filtering the deviations remain significant. This important restriction must be clear when interpreting gate voltage measurements. So it is strongly recommended to perform switch/driver simulations similar to those presented in this paper, if in critical cases (3-pin, high current) an optimization of gate drive is required.

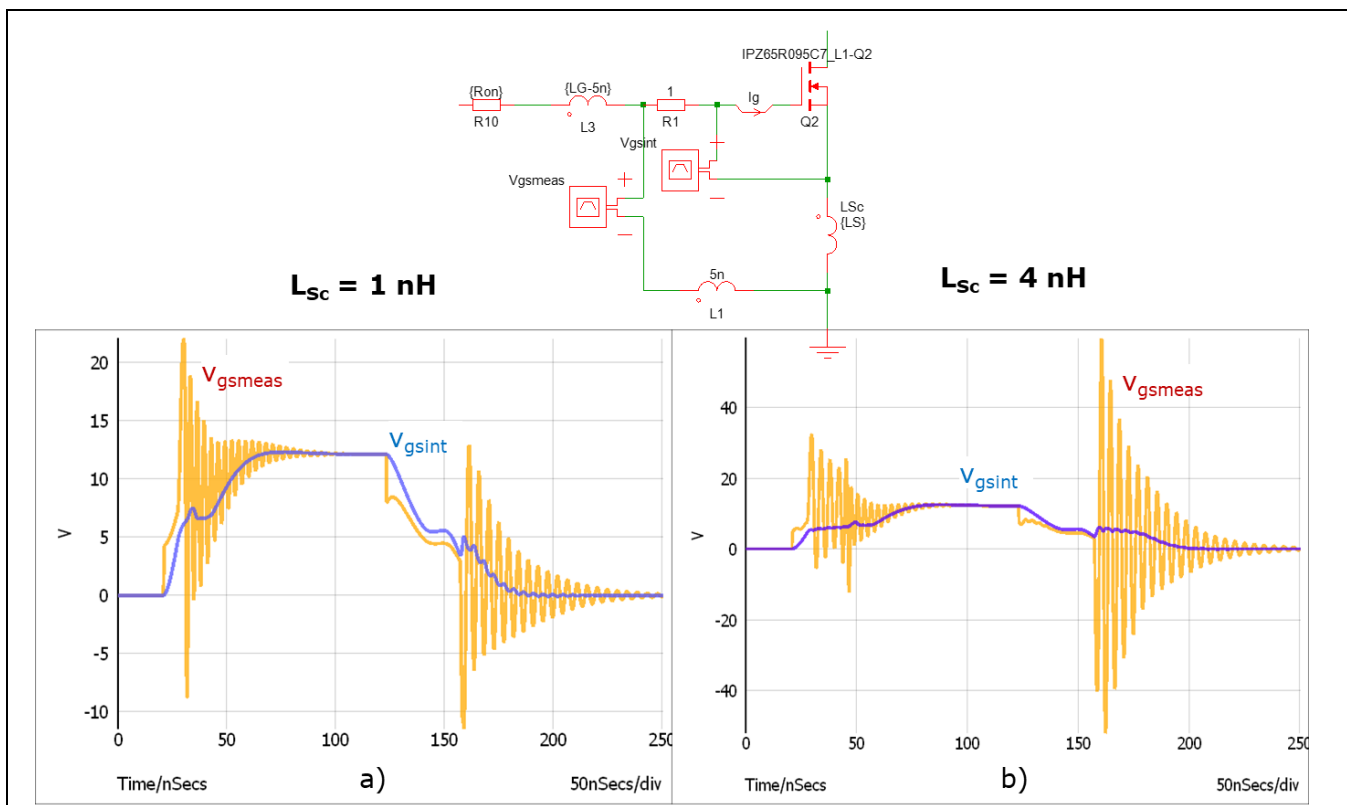


Figure 28 Comparison between internal and measurable V_{gs} voltage waveforms for 3-pin switches with $L_{sc} = 1 \text{ nH}$ (a) and 4 nH (b)

Summary and conclusions

10 Summary and conclusions

The following table gives a summary of the dimensioning guidelines derived in this paper. Generally, in half-bridge applications only 3-pin switches should be used, while in hard-switching systems operated at high current, 4-pin switches are preferable. Although the driver reference then is different from power ground even for low-side switches, this does not necessarily mean that an isolated driver like for example EiceDRIVER™ 2EDi is required; the differential non-isolated EiceDRIVER™ 1EDN7550/8550 family [4] is best suited to such an application. If for any reason nevertheless a 3-pin switch is used, it makes no sense to minimize gate loop inductance. On the contrary, an intentional increase can be beneficial.

Table 2 Overview and summary of gate loop dimensioning criteria

Topology			R_{on}	R_{off}	L_g	Comment
4-pin	single	hard	$\geq R_{min,on}^{(1)}$ (DG2)	$\geq R_{min,off}^{(2)}$ (DG3)	$L_{min}^{(3)}$	
4	hb ⁴⁾	soft	R_{min}	R_{min}	L_{min}	DG5
4	hb ⁴⁾	(partially) hard			L_{min}	DG5
3-pin	hb	soft	$= R_{off}$	$R_{min,off}$	$> L_{min}$	DG4
3	hb	partially hard	DG6	$R_{min,off}$	$> L_{min}$	DG6
3	single	hard	DG7	$R_{min,off}$	$> L_{min}$	moderate current
3	single	hard	DG7	DG8	$\sim 10 \cdot L_{sc}$ (DG9)	high current

¹⁾ Minimum R_{on} fulfilling DG1

²⁾ Minimum R_{off} fulfilling DG1

³⁾ PCB optimized with respect to gate loop inductance

⁴⁾ 4-pin switches in hb application: **not recommended**

The guidelines summarized in Table 2 should be helpful to find a reasonable first guess for dimensioning the gate drive components in a given power system operating with CoolMOS™ switches. Nevertheless, a final optimization requires detailed knowledge of the intended application. In addition to measurements simulations can be extremely valuable.

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11 References

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