High voltage CoolMOS™ P7 and PFD7 superjunction MOSFET in ThinPAK 5x6 package

About this document

Scope and purpose

In chargers and adapters there is a constant push towards higher power densities and reduced form factors to reduce charge times and increase portability. To address this market, Infineon has introduced the new 600 V CoolMOS™ PFD7 and 700 V and 800 V CoolMOS™ P7 superjunction (SJ) MOSFETs in the ThinPAK 5x6 package, with devices from 360 mΩ to 2 Ω. These products offer the benefits of the latest CoolMOS™ 7 technologies in a cost effective, high performance package with an improved mechanical form factor, improved electrical parasitics and a reduced external enclosure hotspot temperature. The challenge when switching to this new package is the different thermal behavior of the device. This application note will show the behavior of the CoolMOS™ 7 in the ThinPAK 5x6 package when used as a DPAK replacement, and shows the behavior of this device in a 45 W adapter application.

Intended audience

This application note is intended to give SMPS design engineers guidance on using the new ThinPAK 5x6 package.

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1 Mechanical dimensions

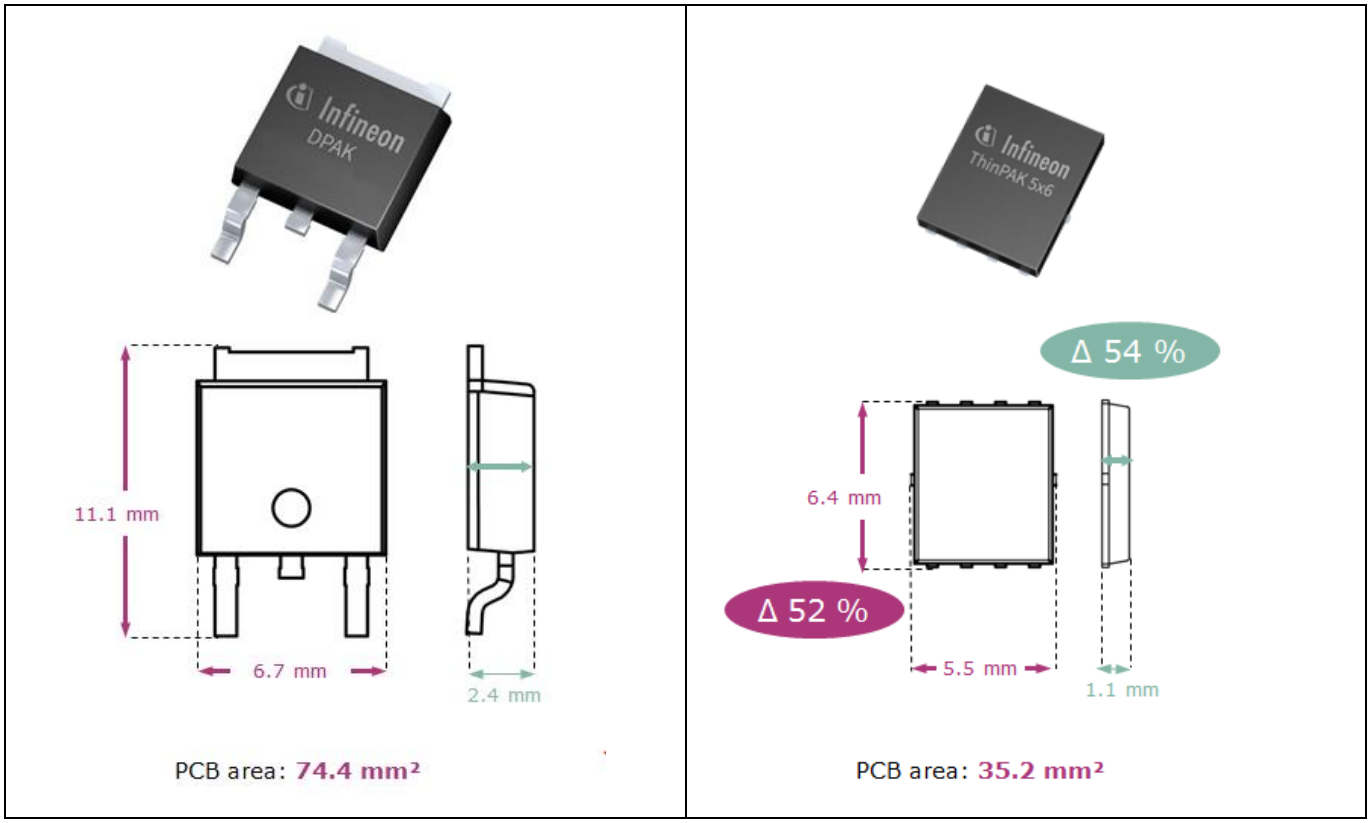


Figure 1 Package comparison of DPAK (74.4 mm² PCB area) and ThinPAK 5x6 (35.2 mm²)

In **Figure 1** it can be seen that the overall mechanical dimensions of the ThinPAK 5x6 package offer an improvement when compared to the DPAK package. The PCB area usage is reduced by 52 percent and the overall height of the package is reduced by 54 percent, to only 1.1 mm. Typically, the lead trimming height required on the bottom side of a PCB when using a standard low-cost configuration with through-hole components on the top and SMD components on the bottom means that 1 mm to 1.5 mm is the minimum lead trimming height. By changing to a ThinPAK 5x6, the component height can be kept below the height of standard lead trimming lengths on the bottom side of the PCB. This can help to reduce the overall form factor of the charger. As we will see in the later chapters, the reduced lead sizes and mechanical dimensions also give electrical and system-level thermal advantages.

2 Electrical parameters

2.1 CoolMOS™ PFD7/P7 technology key improvements

The technology improvements of the 600 V CoolMOS™ PFD7 and 700 V and 800 V P7 technologies are covered in detail in the **700 V CoolMOS™ P7** and **600 V CoolMOS™ PFD7** application notes. The key parameters that have been improved in the new PFD7/P7 technology are a reduction in switching losses and conduction losses as well as inclusion of an integrated gate source Zener diode for improved ESD protection and system reliability during operation.

The switching losses of the MOSFETs are improved by having a lower total gate charge (Q_g) as well as lower energy storage in the MOSFET output capacitance, which needs to be burned off every cycle during hard switching (E_{oss}). By reducing these total charges, which are dissipated every switching cycle, the efficiency of the system at light loads can be improved.

The device conduction losses are reduced by an improvement in the technology, which gives an improved device temperature coefficient. The $R_{DS(on)}$ of a MOSFET is typically rated at 25°C, but during operation the junction temperature will be hotter. The PFD7/P7 technology offers a 10 percent reduction in the $R_{DS(on)}$ at 100°C for lower conduction losses when compared to the older C6 technology. The rule of thumb before was that the $R_{DS(on)}$ is 2x the datasheet value at 125°C, but now with this technology it is only 1.9x the datasheet value at 125°C. More information on this improvement can be found in the **700 V CoolMOS™ P7** application note in section 2.2.

With these improvements in conduction losses and switching losses, the new technology opens the possibility for moving to higher $R_{DS(on)}$ MOSFETs, to reduce the overall system costs or to increase the overall system switching frequency, to reduce the form factor and to reduce passive component costs.

2.2 Package parasitics

In SMPS, the total loop inductance of the MOSFET gate source inductance and drain source inductances are important to avoid re-turn-on of the MOSFET and to reduce EMI. As shown in **Table 1** below, the ThinPAK 5x6 offers a reduction in gate, drain and source inductances (shown in **Figure 2**) when compared to the DPAK package, and an even greater improvement when compared to the FullPAK through-hole package. The ThinPAK 5x6 internal source inductance is reduced by 63 percent compared to the DPAK package.

The total gate source inductance ($L_{gate\_loop} = L_{source} + L_{gate}$) is important in order to reduce the ringing on the gate of the MOSFET. When the LC resonant tank, which is formed by the gate capacitance (C_{iss}) and the total gate loop inductance ($L_{source\ ext.} + L_{gate\_loop}$), is excited by a square wave driving waveform, this can cause ringing on the gate of the MOSFET. By reducing the total L_{gate_loop}, the amount of ringing seen on the gate of the MOSFET can be reduced. Comparing the IPLK70R600P7 to the IPD70R600P7S, there is a reduction in the power loop inductance of 62.8 percent or 2.15 nH.

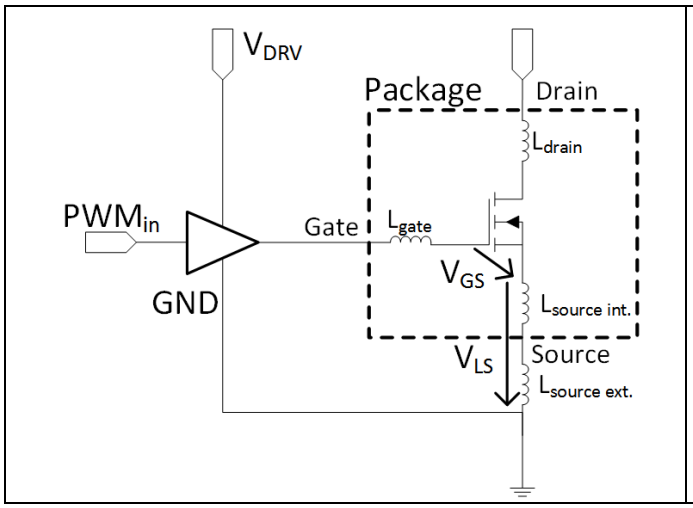
The total drain source inductance ($L_{power\_loop} = L_{drain} + L_{source}$) of the MOSFET is important, since this is the primary power path of the MOSFET and this loop can ring with the total parasitic capacitance, causing additional EMI in the system. Comparing the IPLK70R600P7 to the IPD70R600P7S, there is a reduction in the power loop inductance of 33 percent or 2.4 nH.

Table 1 Nominal package parasitic inductances

	FullPAK IPA70R600P7S	DPAK IPD70R600P7S	ThinPAK 5x6 IPLK70R600P7	Reduction DPAK to ThinPAK 5x6
L_{source} (nH)	3.68	3.34	1.23	63 percent
L_{drain} (nH)	2.13	0.08	0.04	50 percent
L_{gate} (nH)	6.18	4.06	3.74	8 percent
L_{power_loop} (nH)	5.81	3.42	1.27	63 percent
L_{gate_loop} (nH)	9.86	7.40	4.97	33 percent

2.3 Kelvin connection

In order to achieve faster switching at higher currents and to increase gate source driving signal integrity, the total gate source inductance of the MOSFET needs to be reduced as mentioned in the previous section. Another way to increase the switching speed and signal integrity of the gate source waveforms of the MOSFET is to use a separate Kelvin-source connection just for the gate driving of the MOSFET. This Kelvin connection can be used by a ground reference to the gate driver and bypasses the voltage induced in the source connection, which is caused by the di/dt from switching the device, as shown in **Figure 2**.



$$L_{source\_tot} = L_{source\ int.} + L_{source\ ext.}$$

$$V_{GS} = V_{GS-} V_{LS} = V_{DRV} - L_{source\_tot} \frac{di}{dt}$$

Figure 2 Standard gate drive schematic with parasitic source inductance in the gate drive loop

The ThinPAK 5x6 package has three source pins, with one of these source pins (pin 3) configured as a Kelvin-source connection. This pin offers a potential advantage in the MOSFET switching speed and signal integrity due to reducing the gate source ringing. If it is desired to use a standard gate driver, this pin can be shorted to the other source pins (pin 1 and pin 2) and then the MOSFET will behave like a standard 3-pin MOSFET. In many low-power applications this is not necessary due to the lower currents seen in the system, but this leaves the flexibility up to the design engineer if the 4-pin configuration is necessary.

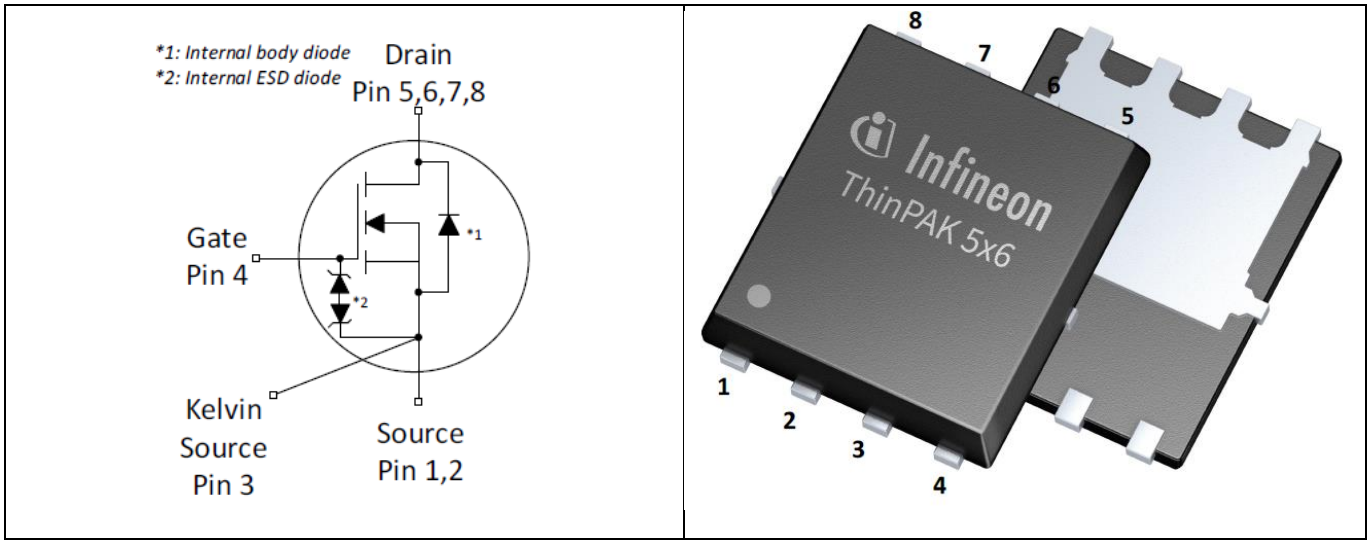


Figure 3 ThinPAK 5x6 pin-out showing the Kelvin source on pin 3

3 Thermal behavior compared to other packages

The challenge when working with new smaller packages is always the thermal behavior due to the lower amount of mold compound and the smaller lead-frame. This section will address some of the key concerns when designing in the ThinPAK 5x6.

3.1 R_{thMA} – measured temperature

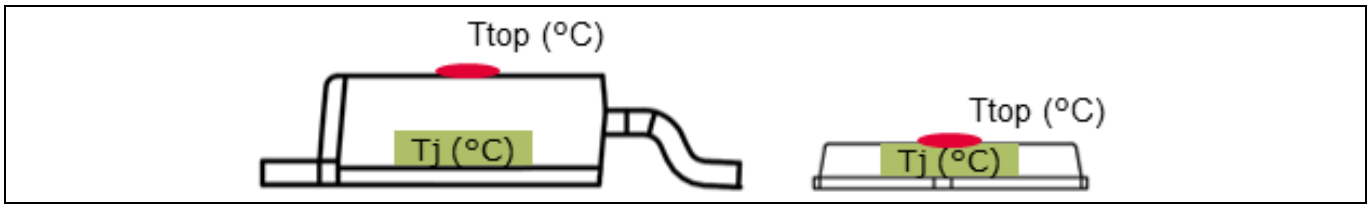


Figure 4 DPAK (left) and ThinPAK 5x6 (right) showing the difference in mold compound thickness between the chip and the top surface

When measuring the MOSFET temperature in an application it is common to use a thermal camera or thermocouple to measure the top surface temperature (T_{top}) of the MOSFET. When comparing the top surface temperature of the DPAK vs. the ThinPAK 5x6 package, the ThinPAK 5x6 will always measure with a higher top surface temperature, even with exactly the same junction temperature. This is because to reduce the package height of the ThinPAK 5x6 there is less mold compound in the package, making it so the top surface temperature of the MOSFET junction is closer to the top of the package, as shown in **Figure 4**.

The top surface temperature of the device can be calculated using the following equation:

$$T_{top} = T_j - Psi_{JunctionTop} P_{dissipated}$$

The thermal resistance from the junction to the top surface of the device is the $Psi_{junctiontop}$ value shown in the equation below and in **Table 2**. As seen below, if we assume a 90°C junction temperature and 1 W of power dissipation, the difference in package top surface temperatures can be seen. The ThinPAK 5x6 shows a hotter top surface temperature than the SOT-223 and DPAK packages, even though the CoolMOS™ junction temperature is the same.

Table 2 Calculating top case temperature with the same junction temperature

Package	Part number	T_j (°C)	P_{total} (W)	$Psi_{JunctionTop}$ (°C/W)	T_{top} (°C)
ThinPAK 5x6	IPLK70R600P7	90.0	1.0	1.83	88.2
SOT-223	IPN70R600P7S	90.0	1.0	3.26	86.7
DPAK	IPD70R600P7S	90.0	1.0	5.19	84.8

As we will see in the next sections, even though the top surface temperature is higher than the DPAK package, the temperature seen on the enclosure hotspot is reduced. The overall thermal performance of the ThinPAK 5x6 package is also reduced when compared to the SOT-223.

3.2 R_{thJA}– steady-state thermal behavior

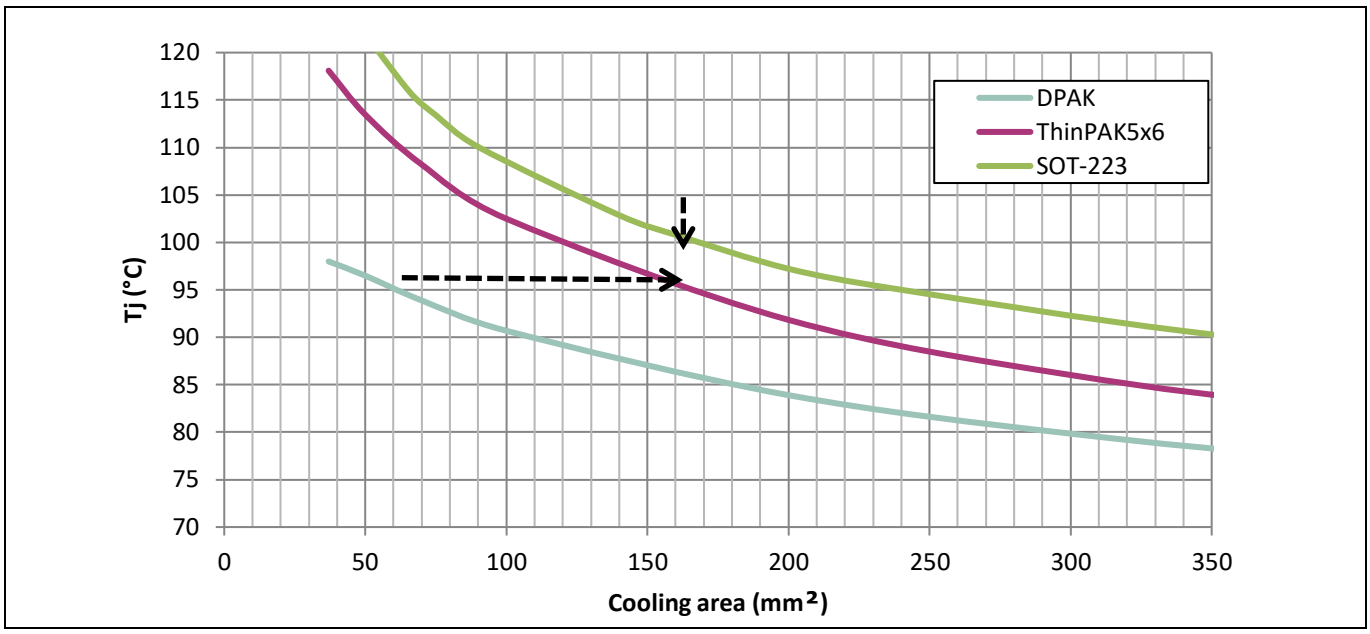


Figure 5 Simulated junction temperature vs. PCB area with 0.5 W dissipation in 50°C ambient

The plot in **Figure 5** shows the behavior of the R_{thJA} of the ThinPAK 5x6 package vs. copper area. This plot is based on a simulation of a standard 1.5 mm FR4 PCB while varying the copper area and with a constant 0.5 W of power dissipation and 50°C ambient. As shown, the junction temperature of the ThinPAK 5x6 is lower than the junction temperature of the SOT-223 package but still higher than the DPAK package. This is due to the fact that the ThinPAK 5x6 package simply has less material than the DPAK package to act as a heatsink. So, in order to keep the same junction temperature, additional copper area or equivalent heatsinking needs to be added to the package.

As shown in **Figure 5** with the dotted arrows, when compared to the SOT-223 with the same copper area and power dissipation, the ThinPAK 5x6 will have a lower junction temperature by around 5°C. When replacing the DPAK with the ThinPAK 5x6 the junction temperature will increase, but this can be compensated for by 100 mm² of additional copper or equivalent heatsinking such as glue, gap pads or thermal vias.

Even though the junction temperature and top surface of the package measure hotter than a DPAK package, as we will see in the next section, the overall hotspot on the product enclosure can be reduced.

3.3 Enclosure hotspot reduction

One of the key requirements for chargers and adapters is the overall system enclosure temperature. This is because if the surface of the charger is too hot while the device is charging or operating, it can be a concern for the user, and at high enough temperatures can violate safety requirements.

The ThinPAK 5x6 has less mold compound, which results in a slightly higher junction temperature than the DPAK package and a higher measured top surface temperature, but the reduced height leads to a large improvement in the enclosure hotspot temperature, as shown below in **Figure 6**.

These measurements were done in an 18 W cell phone charger with 770 mW of power dissipation and a 25°C ambient temperature. The same power was dissipated in the ThinPAK 5x6 and the DPAK package, and it can be seen in **Figure 6** that the top surface of the ThinPAK 5x6 is hotter, but the overall case temperature of the charger is 12.2°C lower than with the DPAK package. This is because there is a 3.5 mm total space between the PCB and the enclosure. The gap between the top of the DPAK device is only 1.1 mm while the ThinPAK 5x6 has 2.4 mm before the device and the enclosure. This additional air

gap acts as an insulator and helps to spread the hotspot that can be seen on the outside of the enclosure.

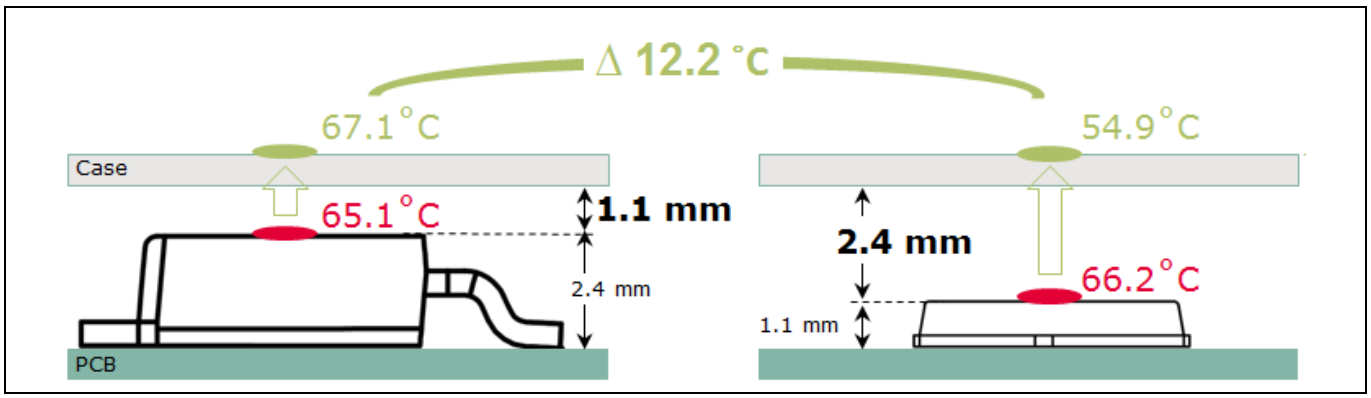


Figure 6 PCB side view of DPAK (left) and ThinPAK 5x6 (right) showing additional air gap, which provides additional heat spreading

Figure 7 shows thermal camera images with the enclosure temperature difference when measured with the DPAK vs. the ThinPAK 5x6 in 25°C ambient. This reduction of the enclosure hotspot can make it so that a higher $R_{DS(on)}$ MOSFET can be used to reduce costs with the same enclosure hotspot temperature. It is also possible to reduce the overall height of the enclosure to take advantage of the ThinPAK 5x6 reduced height while not increasing the system hotspot temperature.

These measurements are comparing the surface temperature of the two open-frame MOSFETs vs. the two enclosed MOSFETs, which is why once the DPAK is in the enclosure, the surface temperature is 2°C hotter than the open-frame measurement.

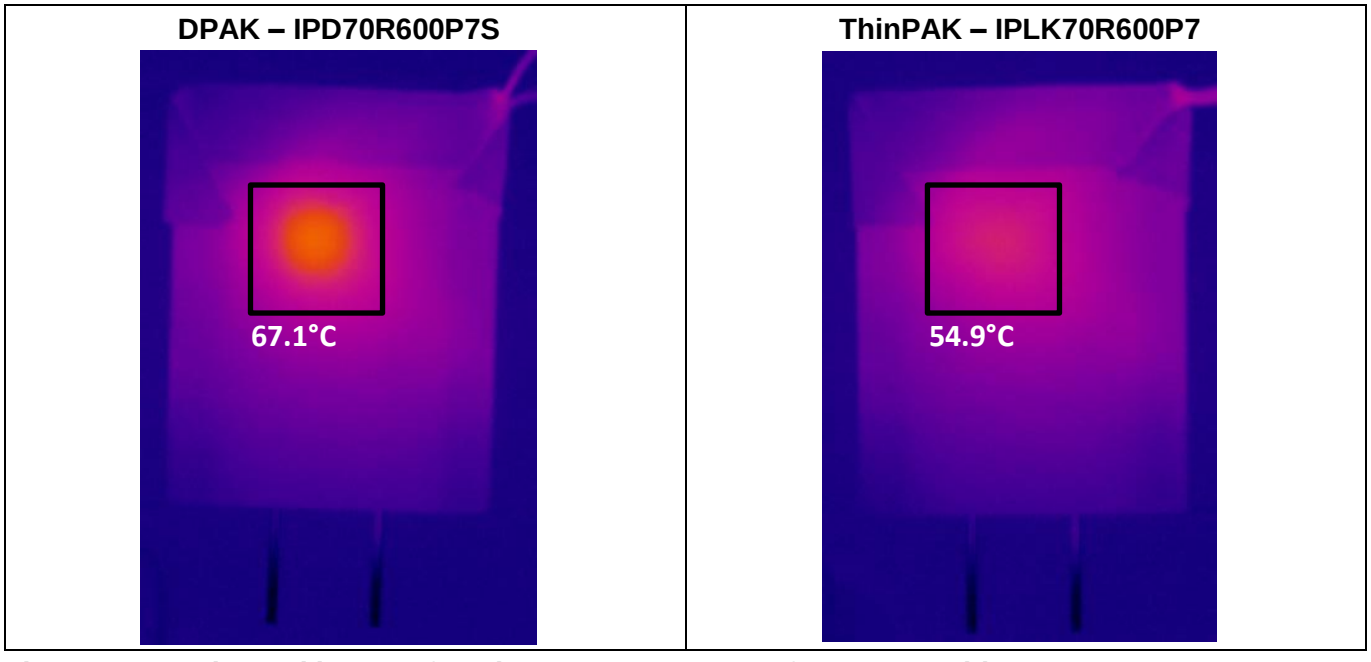


Figure 7 Thermal image of enclosure temperature of DPAK vs. ThinPAK 5x6

4 Manufacturability

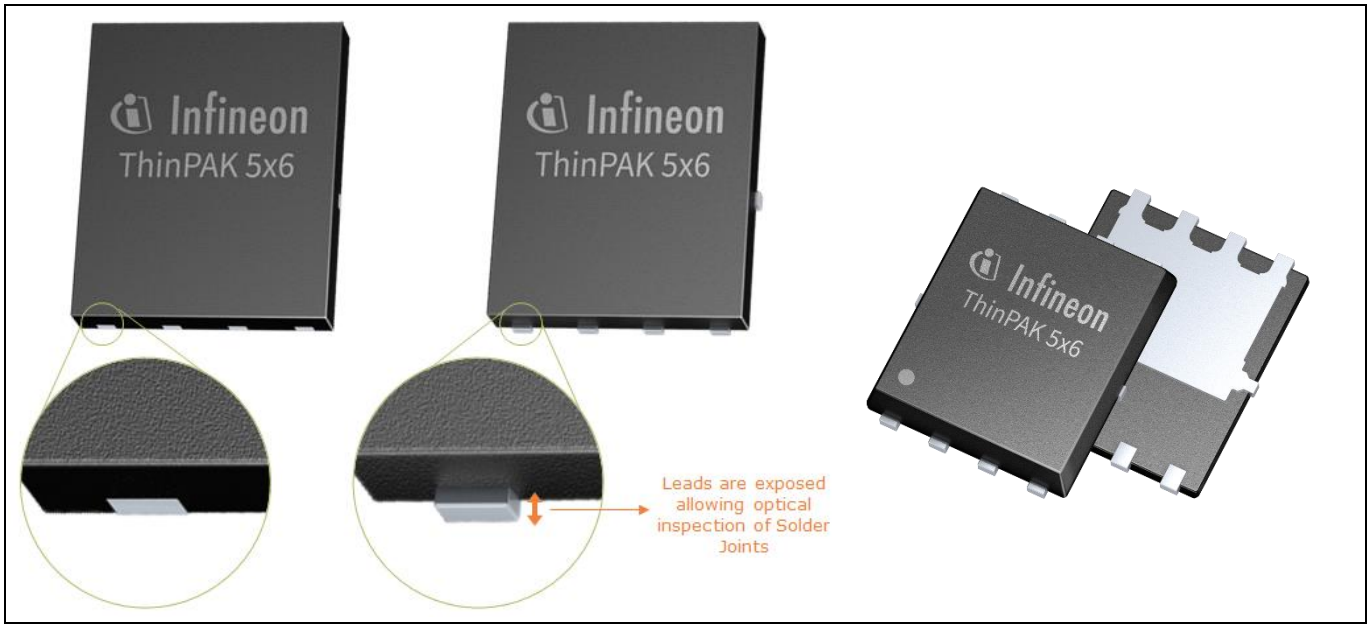


Figure 8 Top view of a ThinPAK 5x6 package showing the old lead-frame on the left and the new lead-frame on the right, allowing for simple automated optical inspection of solder joints

The new version of the ThinPAK 5x6 package offers several benefits when compared to the old ThinPAK 5x6 package when it comes to manufacturability.

The ThinPAK 5x6 now has exposed leads, as shown in **Figure 8**. These exposed leads allow for automated optical inspection (AOI) to ensure that the pads of the device have been soldered correctly. This was not possible with the old Infineon ThinPAK 5x6 package before, since these leads were hidden under the mold compound of the package. This can help to reduce fallout in mass production.

The ThinPAK 5x6 used for the PFD7 600 V, P7 700 V and 800 V devices is also compatible with wave soldering exposure. This was not possible with the old version of the ThinPAK 5x6 package, and to use the package on a PCB with mixed devices it was necessary to mask the device so as not to expose it to the solder wave. This can help to reduce production costs by removing an additional manufacturing process.

With the combination of these two benefits, the PFD7/P7 in ThinPAK 5x6 can help to reduce manufacturing costs of the final charger assembly.

5 45 W application measurements

To show the behavior of the P7 700 V in ThinPAK 5x6, the Infineon 45 W SOT-223 demo board (**DEMO_45W_19V_FLYB_P7 45W**) was modified and used for benchmarking. This 45 W demo board has a 19 V output at 45 W and meets the EU CoC version 6 efficiency requirements as well as radiated and conducted emissions.

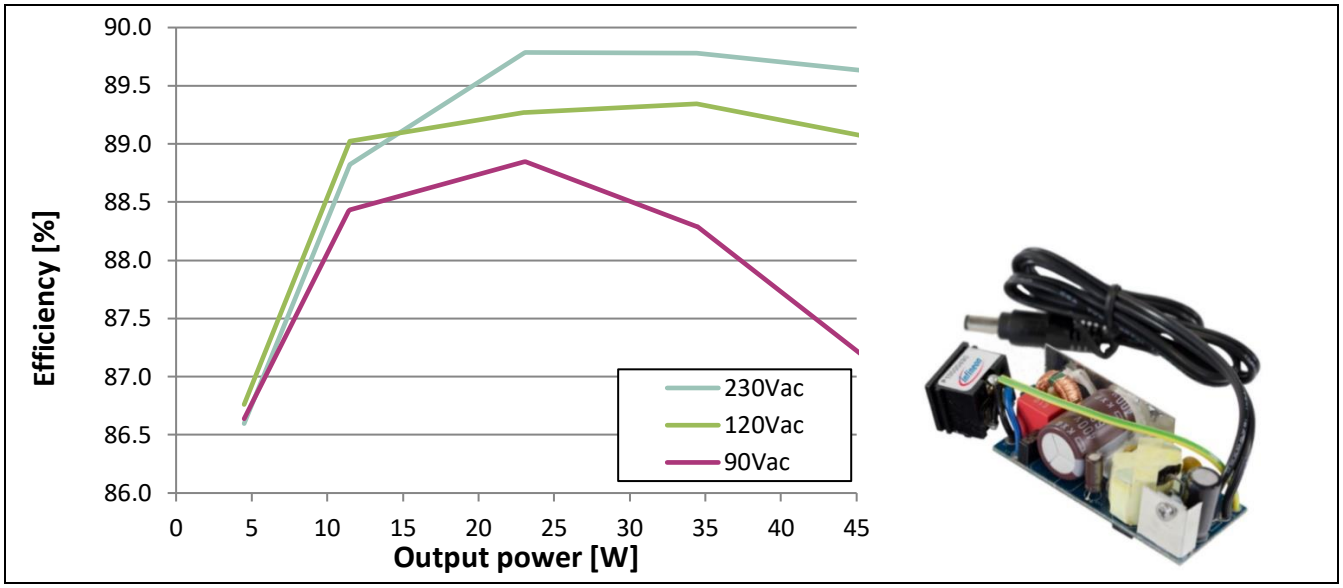


Figure 9 Infineon 45 W SOT-223 adapter demo board (DEMO_45W_19V_FLYB_P7 45W) efficiency vs. load at key common operating voltages (left); image of the demo board (right)

To benchmark the performance of the ThinPAK 5x6, the board was modified with the 600 mΩ 700 V in ThinPAK 5x6, SOT-223 and DPAK as well as devices available on the market with a similar footprint package. The critical point for meeting a design's thermal requirements is the 90 V AC input where conduction losses are the highest. This is the constraint on how great an $R_{DS(on)}$ can be used in the design to minimize the system's costs. It can be seen in **Figure 10** that the performance difference between the IPx70R600P7 in different packages is not significant. The improvement in performance between the P7 700 V 600 mΩ devices in various packages and the closest available devices with a similar footprint to the ThinPAK 5x6 is clear. At full load the 700 V 600 mΩ is even capable of competing with the 650 V 475 mΩ and 600 V 495 mΩ devices from the competition due to the improved temperature coefficient and reduced device parasitics.

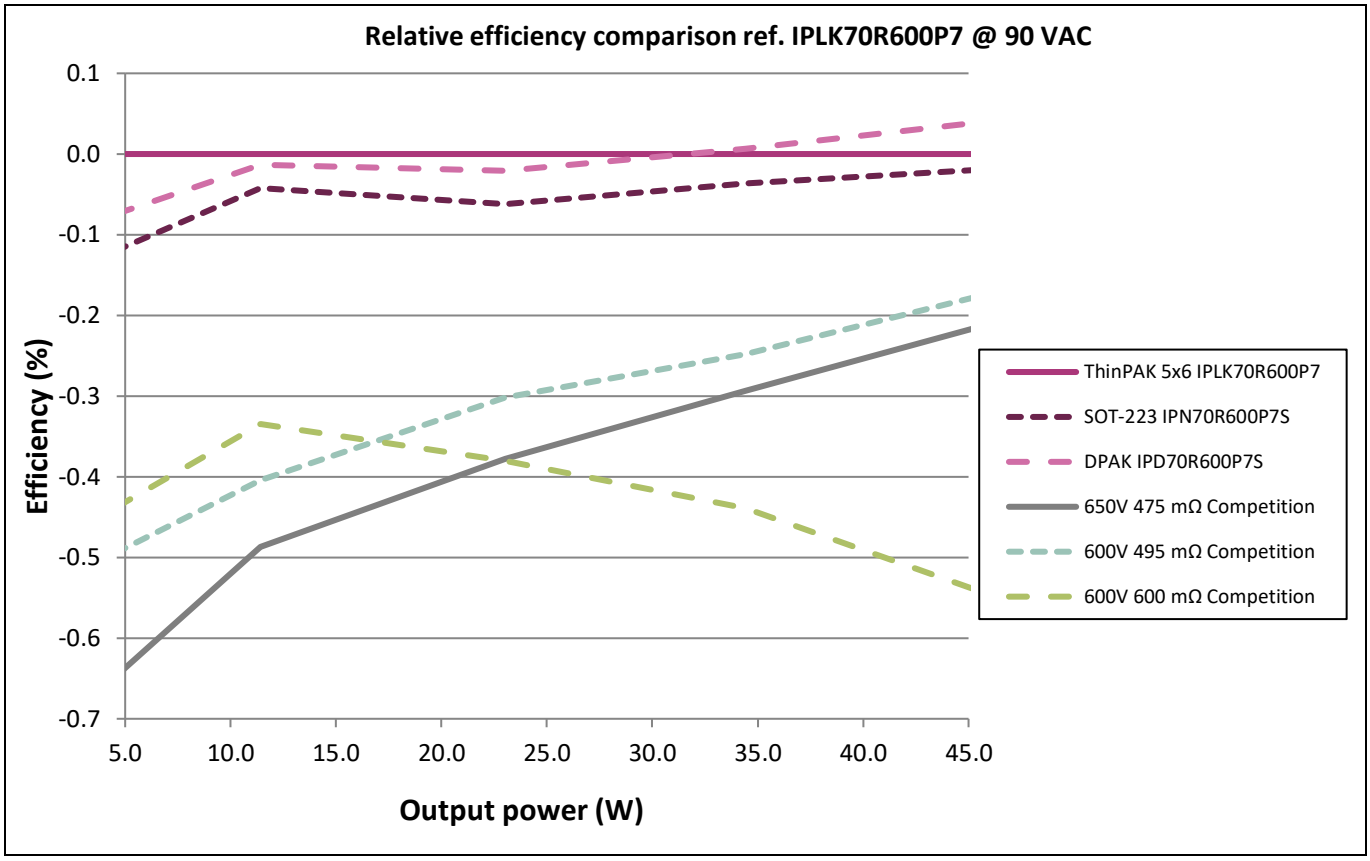


Figure 10 Relative efficiency comparing IPx70R600P7 to competition in different packages

In **Figure 11**, the different thermal behavior of the ThinPAK 5x6 package becomes apparent. Thermally, the P7 can outperform the closest available ThinPAK devices on the market, even devices with a lower $R_{DS(on)}$. The ThinPAK 5x6 and SOT-223 are showing similar thermal results, but the ThinPAK 5x6 is measuring 10°C hotter than the DPAK package. As shown in **Figure 11**, comparing relative efficiency of IPx70R600P7 in different packages (**Table 2**) to competition, the top surface of the ThinPAK 5x6 will show a hotter temperature due to the additional exposure of the junction temperature of the device. Based on the efficiency measurements and the R_{thJA} measurements shown earlier, the junction temperature is operating between the junction temperature of the DPAK and SOT-223 devices.

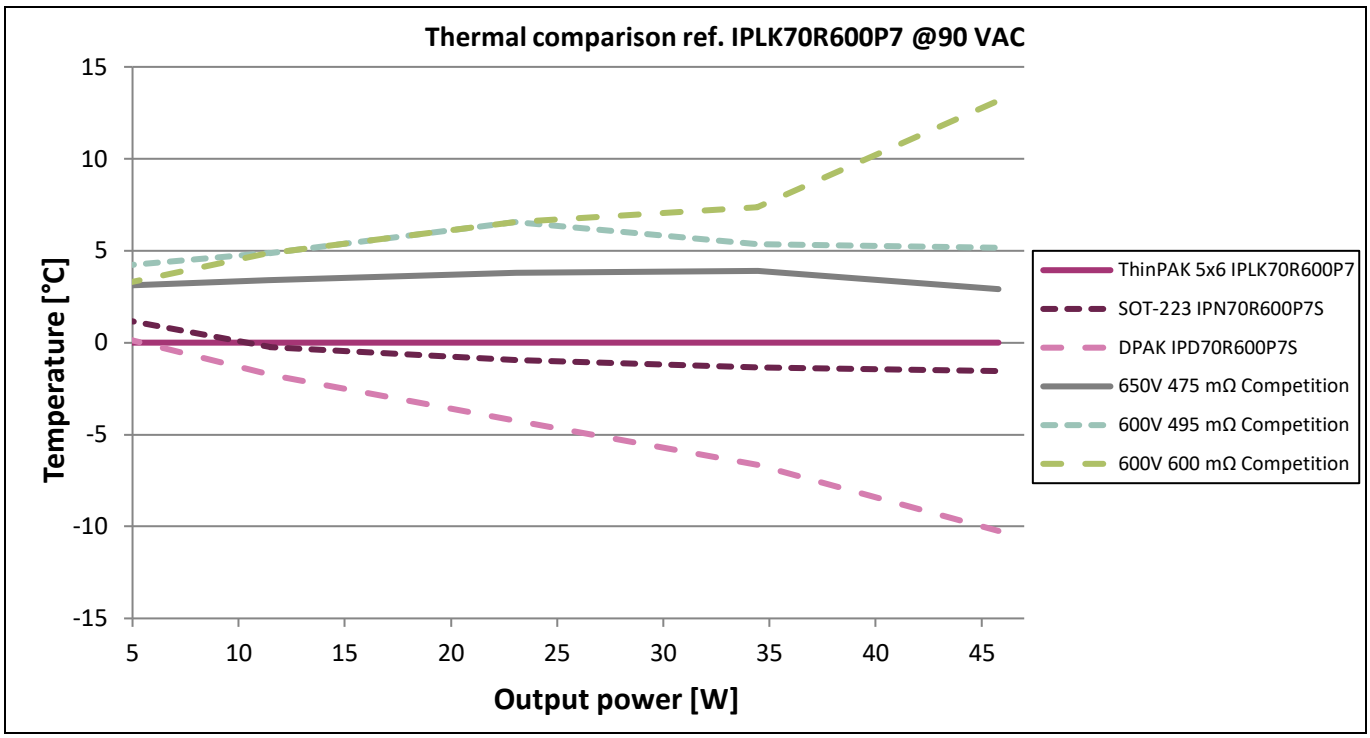


Figure 11 Relative thermals comparing IPx70R600P7 to competition in different packages

6 Conclusion and portfolio

The 600 V PFD7 and 700 V and 800 V P7 in ThinPAK 5x6 offer 16 different devices as shown in **Table 3**, while benefiting charger and adapter designs in several ways. This package helps to provide a smaller mechanical footprint, which enables smaller form factors and increased power densities. The improved electrical characteristics of the package help to reduce system parasitics and improve signal integrity as well as providing the benefits of Infineon's CoolMOS™ technology in a small form factor. Thermally, the ThinPAK 5x6 can compete with the DPAK package while giving a great improvement in the system enclosure temperature and reducing the hotspot seen on the enclosure from the MOSFET. The wave soldering capability of the device and exposed leads allow for easy manufacturing when using the ThinPAK 5x6. As shown in the 45 W adapter measurements, the ThinPAK 5x6 is the best performing and best form factor device on the market, and is capable of competing with even lower $R_{DS(on)}$ devices available from competitors. All of these benefits make the CoolMOS™ device in ThinPAK 5x6 a good fit for the adapter market.

Table 3 CoolMOS™ PFD7/P7 ThinPAK 5x6 portfolio

$R_{DS(on)}$ [mΩ]	800 V P7	700 V P7	600 V PFD7
2000	IPLK80R2K0P7	IPLK70R2K0P7	
1400 / 1500	IPLK80R1K4P7	IPLK70R1K4P7	IPLK60R1K5PFD7
1200	IPLK80R1K2P7	IPLK70R1K2P7	
900 / 1000	IPLK80R900P7	IPLK70R900P7	IPLK60R1K0PFD7
750	IPLK80R750P7	IPLK70R750P7	
600	IPLK80R600P7	IPLK70R600P7	IPLK60R600PFD7
360			IPLK60R360PFD7

[1] See the code examples at **www.infineon.com**

Revision history

Document version	Date of release	Description of changes
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