Thermal performance of CoolMOS™ CFD7A in D2PAK 7-pin on insulated metal substrates

About this document

Scope and purpose

This document shows the results from a thermal investigation with different 650 V CoolMOS™ CFD7A chips in the D2PAK-7 package placed on a high-voltage Insulated Metal Substrate (IMS).

The 650 V CoolMOS™ CFD7A is a silicon Superjunction (SJ) MOSFET technology for automotive applications in electric vehicles, such as on-board chargers for BEVs and PHEVs and on-board HV-LV DC-DC converters.

The final data indicates that the IMS is an excellent choice for high-power applications since the thermal resistance from the heat source (the MOSFET junction) toward the heat sink (the liquid cooling system) is very low in comparison to other substrates (such as FR4).

Intended audience

Design engineers who are responsible for selecting the best solution for automotive on-board power electronic applications, such as on-board chargers, on-board HV-LV DC-DC converters and/or active discharge applications.

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1 Introduction

Power conversion systems in modern electric cars need to be able to handle high voltages and high currents. In order to ensure long-term operation in the field, the generated heat (which naturally occurs during the power conversion due to power losses) must be dissipated with a cooling system.

Most on-board chargers and on-board DC-DC converters utilize discrete power components with either FR4 or IMS. While FR4 offers the possibility of full flexibility and multilayer routing, the advantage of IMS is that it offers high isolation strength combined with very low thermal resistance. The disadvantage of using IMS is that the substrate offers only one copper layer for routing and suffers from a higher parasitic capacitance.

This document shows the thermal performance of different 650 V CoolMOS™ CFD7A SJ MOSFETs on an IMS "HT-07006" from Henkel/Bergquist. This material was chosen as a representative for IMS materials for high-voltage environments offering a breakdown voltage of 11 kV AC (according to [1]).

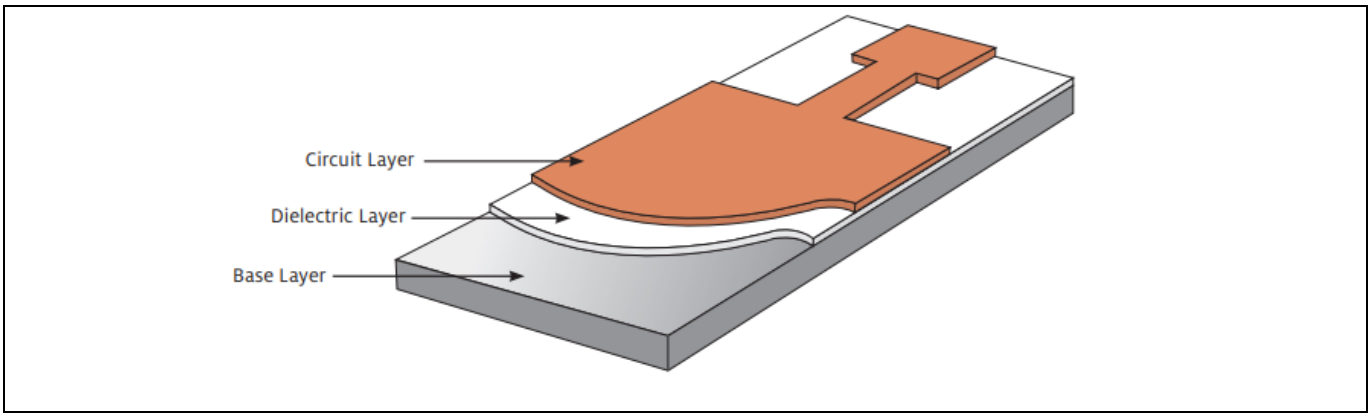

Figure 1 Layers of an IMS board – source [1]

Table 1 Properties of the selected IMS [1]

Layer	Material	Thickness	Thermal conductivity in W/(m*K)
Circuit layer	Copper, single layer	70 µm	388
Dielectric layer	HT-07006, single layer	152 µm	4.1
Base layer	Aluminum	1278 µm	220

2 Thermal models and simulation results

A full thermal FEM simulation was performed in order to assess the thermal resistance of several different CoolMOS™ SJ MOSFETs. This chapter describes the setup, the methodology and the results of this thermal simulation.

2.1 3D geometrical model

Several 650 V CoolMOS™ CFD7A power MOSFETs were placed on this insulated metal substrate and a 3D FEM simulation was performed to determine the junction temperature of the individual power chips.

These CoolMOS™ CFD7A power chips are available in SMD and through-hole packages. For IMSs we recommend using the D2PAK-7 package due to its superiority in terms of electrical performance and creepage distance.

A graphical representation of the model is depicted in **Figure 2**.

Figure 3 shows a cross-cut of the 3D model, indicating the internals of the package and the heat flow.

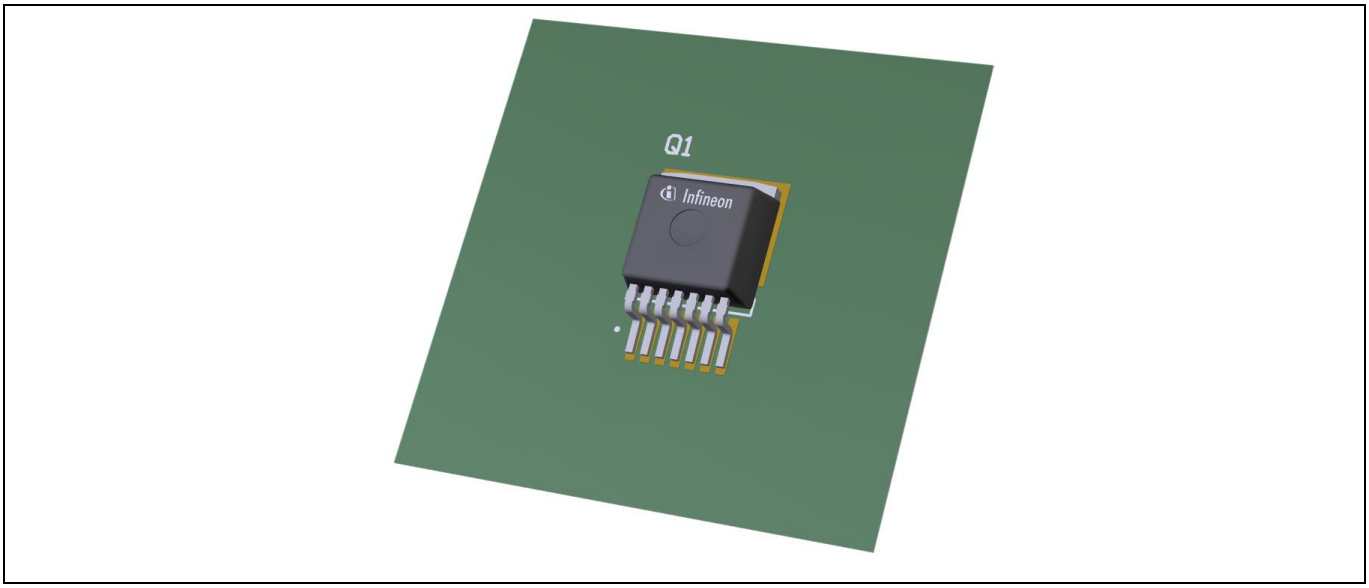

Figure 2 3D model for thermal FEM simulation: CoolMOS™ CFD7A chips in D2PAK 7-pin on IMS

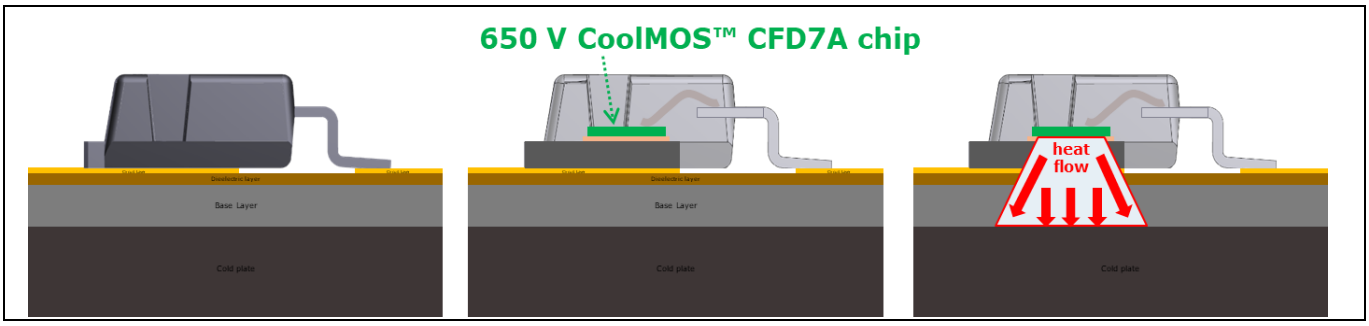

Figure 3 Cross-cut of the thermal path showing the internals and the heat flow

2.2 Initial conditions

Beside the geometrical inputs, the simulation needs initial conditions of the thermal parameters. We assume a constant power dissipation of 20 W homogeneously distributed in the active area of the power chip.

This 20 W power dissipation is derived from an automotive DC-DC converter operating at 3600 W. It assumes a soft-switching CLLC topology using a 650 V CoolMOS™ CFD7A with an on-channel resistance of 50 mΩ (IPBE65R050CFD7A). The assumed power dissipation of 20 W also contains a safety margin to anticipate variations during the operation. The heat generated is being transferred through the chip, through the package and further through the IMS substrate toward the aluminum base layer of the IMS, and eventually supplied to the liquid cooling system.

The model assumes that the cooling system (and the connected base layer of the IMS) is able to keep a constant temperature (acting like an ideal heatsink). In reality, the liquid cooling system will control this temperature by controlling the amount and the pressure of the coolant flowing through the cold plate. Therefore some temperature swing of the cold plate is expected (since the power of the cooling system is limited in reality). To anticipate this effect in the simulation, we assume a worst-case cold-plate temperature of 85°C (T_{CP}). This value also serves as the mathematical boundary condition for the FEM simulation.

In real-world systems, the maximum temperature of the coolant might be significantly lower depending on the efficiency of the cooling system and the environmental conditions of the individual electric vehicle. This will allow a bigger thermal budget and, consequently, an even higher power dissipation (than the assumed 20 W per package in this simulation).

2.3 Assumptions for the thermal propagation

For the sake of simplicity, we assume that the heat is being transferred only by thermal conduction toward the heatsink – there is no convection or thermal radiation included in this model. This simplification can be motivated by looking at the thermal resistances of the individual thermal paths. In well-designed power supplies the conduction toward the heatsink exhibits by far the highest thermal conductivity and therefore the lowest thermal resistance (R_{th}) in comparison to the convection or radiation on the mold compound on the top-side of the PCB.

In other words, the total amount of heat generated within the power chips will be dissipated by the cooling system. The temperature representing the cooling system temperature is T_{CP}.

2.4 Definition of results

The 3D FEM thermal simulation delivers the junction temperature of the chip (T_j) and the temperature of the cold plate (the aluminum layer of the substrate, which is connected to the liquid cooling system) (T_{CP}) versus the simulated time (t).

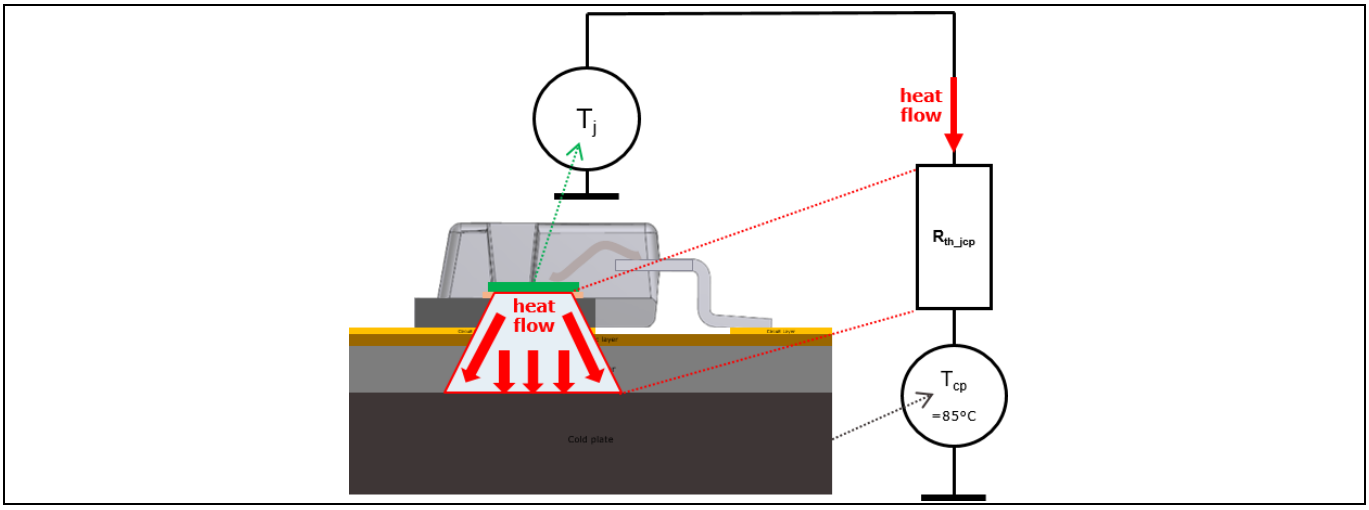

Figure 4 Heat flow through the system and principle of thermal model

Putting these quantities in context, the thermal impedance $Z_{th_{jh}}$ can be calculated based on the formula shown here:

$$Z_{th_{jcp}}(\mathrm{t}) = \frac{\Delta \mathrm{T(t)}}{\Delta \mathrm{P}} = \frac{T_j(t) - T_{CP}(t)}{\Delta \mathrm{P}} = \frac{T_j(t) - T_{CP}}{\Delta \mathrm{P}}$$

As mentioned above, the ambient temperature T_a is constantly set to 85°C and is therefore independent of the time. This will simplify the formula to:

$$Z_{th_{jcp}}(\mathrm{t}) = \frac{T_j(t) - T_{CP}}{\Delta \mathrm{P}}$$

Since the focus of this investigation is on the static thermal resistance, we can simplify the formula even further. Assuming that t_{max} is much greater than the dominant thermal time constant of our system will lead to:

$$R_{th\_jcp} = \frac{T_{j(tmax)} - T_{CP}}{\Delta \mathrm{P}} = \frac{T_{j(tmax)} - 85°C}{20\mathrm{W}}$$

An analysis of the dynamics of the thermal system suggested that t_{max} can be set to 1000 s. Therefore the definition of the R_{th_jcp} finally yields:

$$R_{th\_jcp} = \frac{T_{j(1000s)} - 85°C}{20\mathrm{W}}$$

2.5 Results of thermal simulation

The results of the thermal simulation for different chips of the 650 V CoolMOS™ CFD7A series are summarized in Table 2.

This table shows the following results:

1. The assumed temperature of the cold plate attached to the liquid cooling system: T_{cp} in °C
2. The steady-state junction temperature T_j in °C (in steady-state, which means at t = 1000 s)
3. The thermal resistance R_{th_jcp} in K/W. This thermal resistance represents the complete thermal resistance from the junction of the power MOSFET to the aluminum base plate of the IMS ("cold plate").

These values are given for two different solder qualities: the "good" process assumes a void rate of 10 percent along the main thermal path, whereas the "bad" solder process assumes 50 percent voids. This is being modeled by a homogeneously distributed loss of contact area causing a decreased thermal conductivity among the solder layers. A direct comparison of the R_{th_jcp} shows that the influence of the solder quality impacts the result with maximal 10 percent.

Note: A direct comparison of R_{th_jcp} to the datasheet value $R_{th,jc}$ is not possible since its definition is different to the definition of $R_{th,jc}$ in the individual power semiconductor datasheets.

Table 2 Results of 3D thermal FEM simulation

CoolMOS™ CFD7A power chip	**Assumed temperature of the cooling system (T_{cp})**	**Junction temperature T_j** (assuming ΔP = 20 W)	**Thermal resistance junction-to-cold plate R_{th_jcp}**	**Junction temperature T_j** (assuming ΔP=20W)	**Thermal resistance junction-to-cold plate R_{th_jcp}**
		"Good" solder process: 10 percent voids		*"Bad" solder process: 50 percent voids*	
IPBE65R050CFD7A	85°C	112.42°C	1.371 K/W	113.40°C	1.420 K/W
IPBE65R075CFD7A	85°C	115.96°C	1.515 K/W	116.41°C	1.570 K/W
IPBE65R099CFD7A	85°C	117.32°C	1.616 K/W	118.76°C	1.688 K/W
IPBE65R115CFD7A	85°C	119.27°C	1.713 K/W	121.24°C	1.812 K/W
IPBE65R230CFD7A	85°C	126.61°C	2.081 K/W	129.58°C	2.229 K/W

3 Conclusion

The thermal investigation shows that the 650 V CoolMOS™ CFD7A chips in the new D2PAK-7 show outstanding thermal behavior when used on IMSs. Even if a worst-case coolant temperature is assumed with 85°C, the MOSFET's junction temperature will stay within datasheet limits.

The maximum thermal resistance from the junction to the base layer of the IMS was calculated to ~2.2 K/W.

The data indicates that the values of the thermal resistance between the junction of the power MOSFETs toward the cooling system (R_{th_jcp}) depend mostly on the selected CoolMOS™ MOSFET.

The quality of soldering attached plays a minor role: an improvement of merely 10 percent approximately can be achieved by minimizing the number of solder voids (optimizing the solder process). More detailed information about the influence of solder voids on the thermal resistance is available in the Chapter 3.4.1 "Voids in solder joints" of application note [3].

We can perform a customized 3D FEM simulation for your specific system! Please contact us via the Infineon Sales Office [4] to get design-in support for our automotive CoolMOS™ SJ MOSFETs.

4 References

[1] "Comprehensive Selection Guide THERMAL CLAD": https://dm.henkel-dam.com/is/content/henkel/Bergquist%20Comprensive%20Selection%20Guide%20-%20Thermal%20Cladpdf

[2] Infineon's 650 V automotive CoolMOS™ CFD7A family with product datasheets: https://www.infineon.com/CFD7A

[3] Infineon application note "Thermal performance of surface mount semiconductor packages": https://www.infineon.com/dgdl/Infineon-Package_MOSFET_Thermal_performance_of_surface_mount_semiconductor_packages-AN-v01_01-EN.pdf?fileId=5546d462636cc8fb0163bbc605c2585f

[4] Your contact at Infineon for 3D thermal simulations of your system: https://www.infineon.com/cms/en/about-infineon/company/find-a-location/

Revision history

Document version	Date of release	Description of changes
V 1.0	20-04-2020	First release

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