

600 V CoolMOS™ S7 with temperature sense

About this document

Scope and purpose

Infineon Technologies has been investing in solid-state applications for many years. Now it is making further improvements to its S7 family with additional functionality, namely temperature sense integration. This application note describes the functionality, target applications and benefits of using this new feature.

Intended audience

The intended audience for this document includes design engineers, technicians and developers of electronic systems.

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Introduction

1 Introduction

Infineon released its first CoolMOS™ S7 products in 2021. They were intended for applications which do not show a high switching frequency, such as active bridge rectifiers and S4 applications. To provide an additional safety feature, temperature sense has been included in the newest CoolMOS™ S7T family.

The embedded temperature sensor significantly enhances junction temperature sensing accuracy and robustness. The S7T is a testament to the continuous innovation in the industry, designed to ensure easy and seamless implementation while allowing optimal utilization of both the power transistor and the system as a whole.

The CoolMOS™ S7T family will be released for industrial applications, and there will be a portfolio extension in 2024 for additional package variants and qualification grades focusing on automotive applications.

As CoolMOS™ S7 is already known, this document will focus on the additional temperature sense feature. First, the following section will give an overview of the portfolio and the target applications.

1.1 Portfolio

As shown below, CoolMOS™ S7T will focus on industrial applications for the moment.

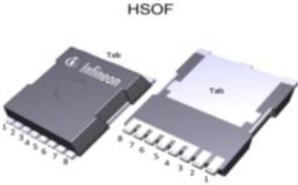
600 V CoolMOS™ S7T	
$R_{DS(on),max}$ [mΩ]	TOLL
	
	IPT60T065S7
	IPT60T040S7
22	IPT60T022S7

Figure 1 Portfolio

Infineon previously released three products in the CoolMOS™ S7T family in TO-leadless (TOLL) package, with an $R_{DS(on),max}$ of 22, 40 and 60 mΩ at $T_J = 25^\circ\text{C}$ and a rated blocking voltage of 600 V. As mentioned, the portfolio will be extended in 2024.

For further information please see the [Infineon website](#).

Before continuing to the technical section of this application note, the next chapter will briefly describe the target applications.

1.2 Target applications

This new product family can be used in various applications in which the switching frequency is limited, or where solid-state operation (continuous conducting) with fast turn-off may be needed during fault events. The applications discussed below will give some idea of possible uses.

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1.2.1 Totem-pole PFC (slow switching leg)

In totem-pole power factor correction (PFC), CoolMOS™ can be used in the slow switching leg, which is operated as a rectifier and therefore is only switching with line frequency. There the devices switch with a frequency of 50/60 Hz. This can be seen in the following figure, which also shows the operating principle.

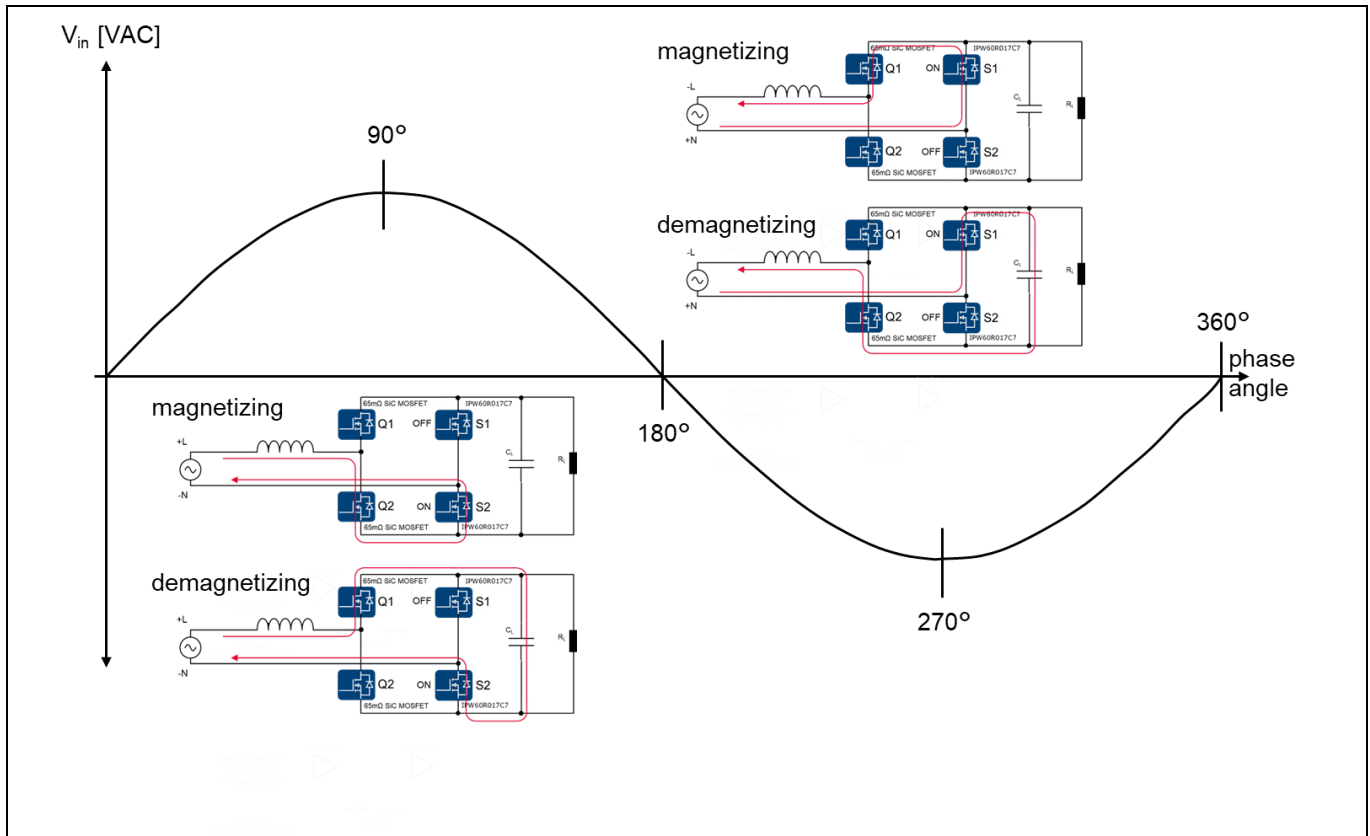


Figure 2 Block diagram and operating principle of the totem-pole PFC

As can be seen, S1 and S2, which are currently C7- and or S7-based, can be replaced by the new CoolMOS™ S7 family with temperature sense. Additionally, it can be seen that S1 is only active during the positive half of the AC sinewave and S2 is on the negative half. This means that only one switch is turned on while the other is completely turned off. In this application or topology only the $R_{DS(on)}$ is relevant; not the switching behavior. Implementation of the temperature sense can increase the reliability of the overall system.

1.2.2 Solid-state relay

The most commonly used relays, from 110 V AC to 400 V AC and 300 V DC to 700 V DC, and the current range from 0 A to 16 A, are electromechanical relays (EMRs). An EMR is an actuator device with electrically controlled physical moving parts. This is achieved by having an electromagnetic coil inside the relay, which produces a magnetic field that closes or opens the physical contacts of the relay. EMRs intrinsically enable galvanic isolation of the control and high-voltage circuits.

The main advantage of EMRs is their affordable price and very high-power density. Power density is defined as a key performance indicator (KPI) of $\frac{V_{sw} \cdot I_{nominal}}{Volume}$. The downsides of EMRs include slow response time, high control power consumption, arcing between contacts, sensitivity to vibration and orientation, and acoustic switching noise. Mechanical contacts deteriorate over time, especially in applications requiring frequent switching events under biased (loaded) conditions. All these problems result in reliability and durability issues.

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Compared to EMRs, SSRs have no moving parts. Infineon is following the evolution from EMRs to SSRs shown in the following figure by introducing the new CoolMOS™ S7 family, and increasing safety through the new temperature sense feature.

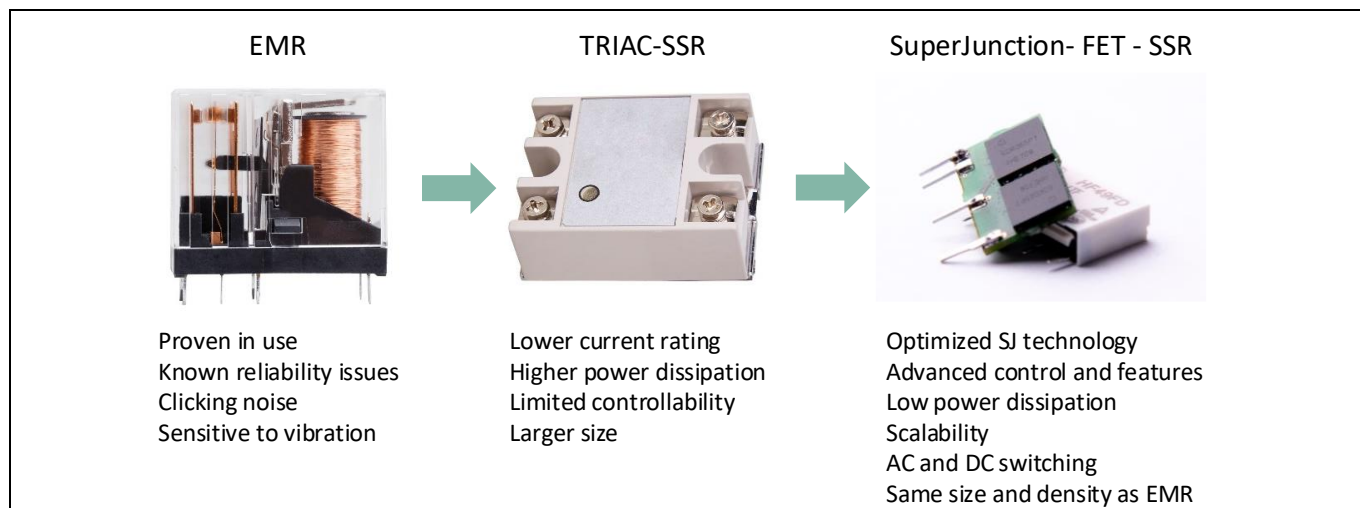


Figure 3 Looking to the future with superjunction FET SSRs

1.2.3 Solid-state circuit-breaker

Another important target application in which CoolMOS™ S7T can provide an additional safety feature especially during overload operations is the solid-state circuit-breaker (SSCB). SSCBs combine all required functions of a power distribution topology into one single device.

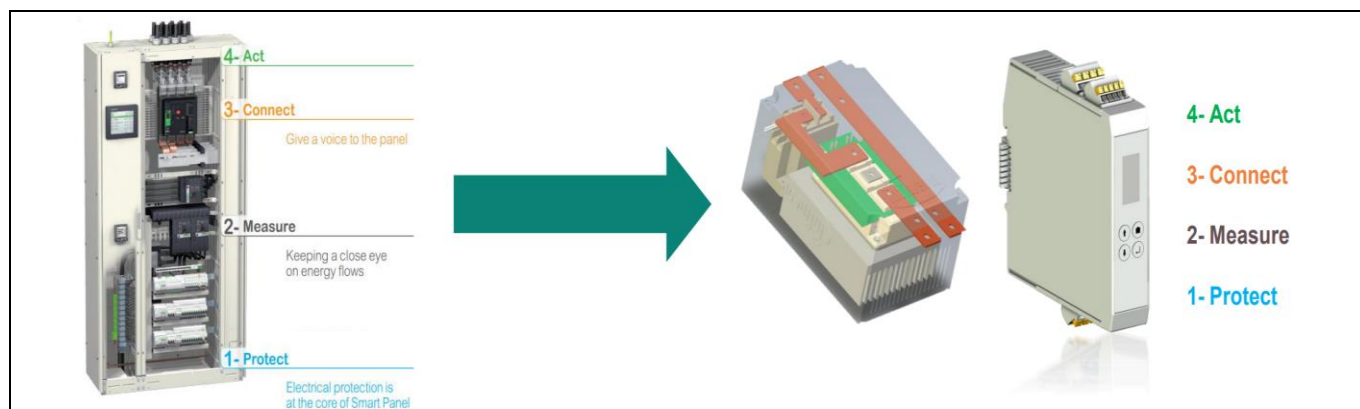


Figure 4 SSCBs combine all required functions in a single device

The combination of fast switching devices in failure and SSCBs benefits the user through the reduction of protection time from the milliseconds range to sub-microseconds. Additionally, the system allows wear- and arc-free operation to avoid maintenance, avoid manual diagnostics and reduce the constructed space due to avoidance of the arcing chamber. This chapter has shown the main target applications, but there are nearly no limits for our CoolMOS™ S7T family. As the CoolMOS™ S7T will have the same chip design as S7, the next chapter will describe the technical differences.

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Technical differences between CoolMOS™ S7 and S7T

2 Technical differences between CoolMOS™ S7 and S7T

2.1 Package and pin-out

In general, the package has the same outer dimensions and also the lead frame thickness stays completely the same as in CoolMOS™ S7. Nevertheless, there is a crucial difference with respect to the pin-out which is visualized in the following picture.

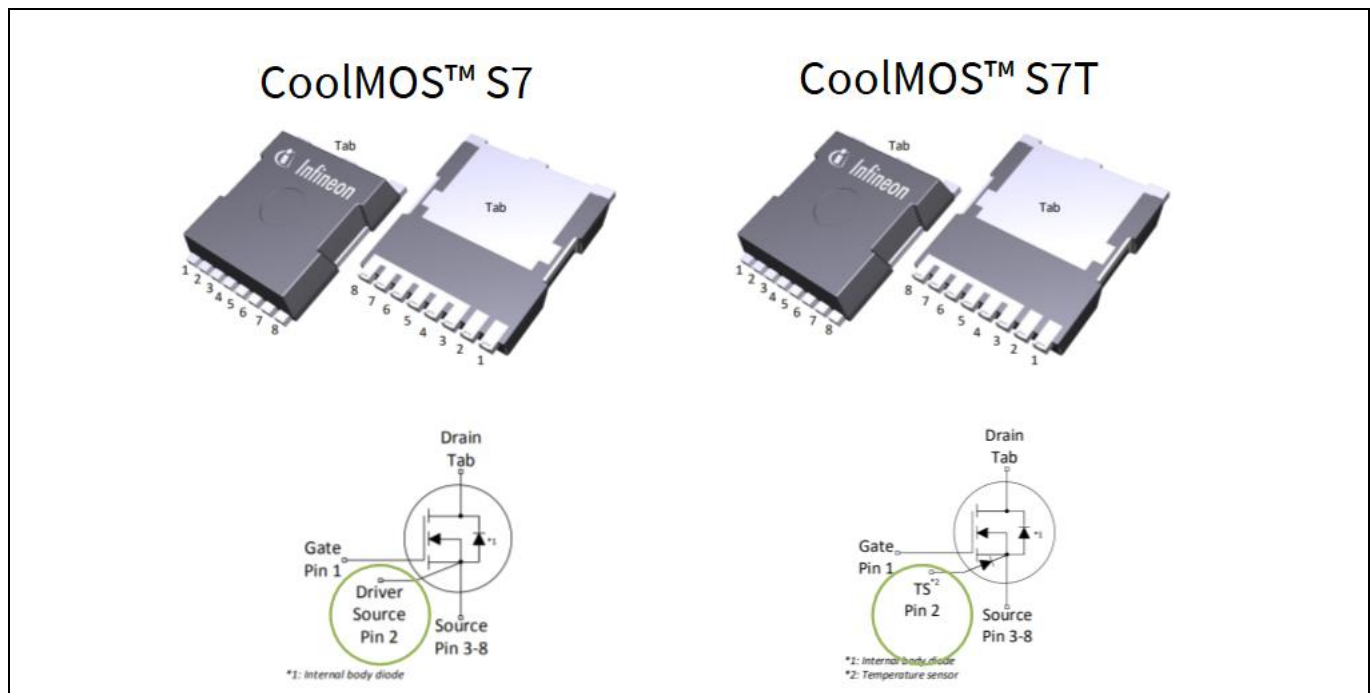


Figure 5 Package pin-out

Pin 2 for CoolMOS™ S7T is changed and will be used for temperature sensing. There is no longer any driver/Kelvin source available for this product.

2.2 Temperature sensor

Typically in applications, overtemperature protection is included. Nevertheless, the temperature sensor for this is often located on the heatsink on which the power semiconductors are mounted or connected. This represents good thermal protection but typically the R_{TH} chain from the junction to the sensor is very high, resulting in significant latency between thermal increase of the power semiconductor due to fault events. This thermal sensor is placed as close as possible to the active cells in the power semiconductor, leading to reduced delay times, which will be described in [Section 3.2](#) of this application note. The location of the temperature sensor brings an additional safety feature to the overall system alongside the implementation of well-known thermal protection concepts.

The temperature sensor is simply a series connection of three diodes. Due to the linear temperature behavior of these diodes, their forward voltage (V_F) directly relates to a certain temperature these diodes have, provided they are biased with a current source.

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Technical differences between CoolMOS™ S7 and S7T

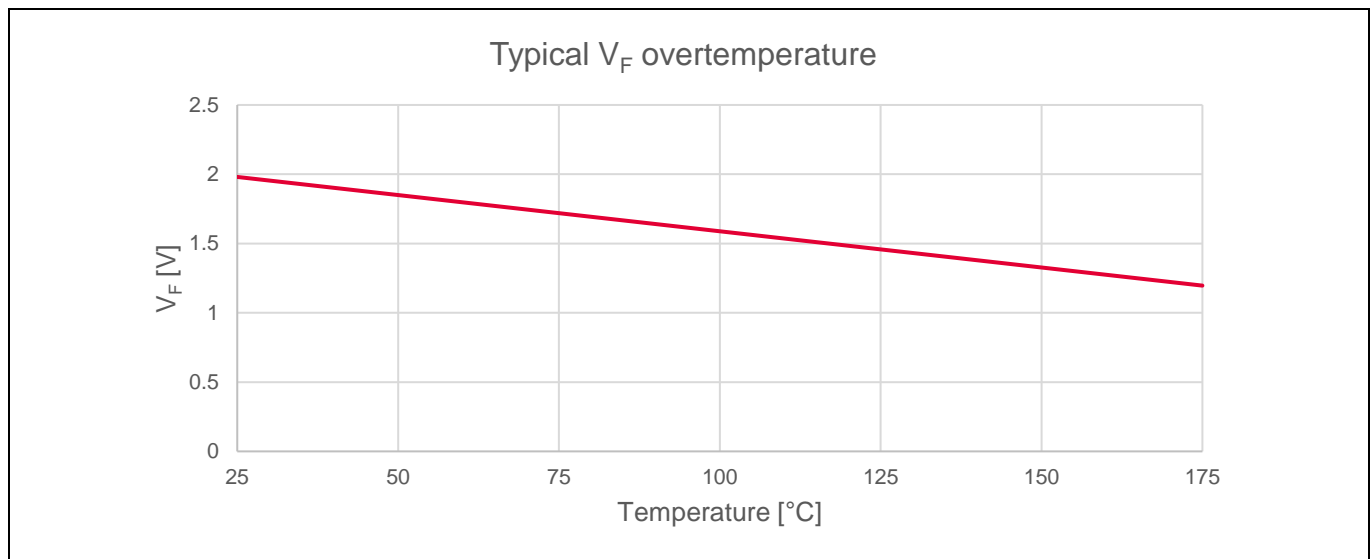


Figure 6 V_F over temperature of the sensor diodes for a forward current of 200 μA included in the corresponding datasheets as table.

The sense current I_F for the diagram in [Figure 6](#) is 200 μA , which results in a V_F of the diodes of 1.9806 V for $T_J = 25^\circ\text{C}$ and 1.1963 V for $T_J = 175^\circ\text{C}$. This results in a sensor forward voltage temperature coefficient (TC) of 5.2287 mV/K at $I_F = 200 \mu\text{A}$.

The design of the chip itself is completely carried over from the already well-known CoolMOS™ S7, and the temperature sensor is also implemented near the gate pad.

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Temperature read-out

3 Temperature read-out

In order to understand how the temperature sensor works, a procedure for reading out information from the sensor is needed.

3.1 Procedure

The procedure to read out the V_F of the diodes is straightforward, as shown in the following simplified schematic.

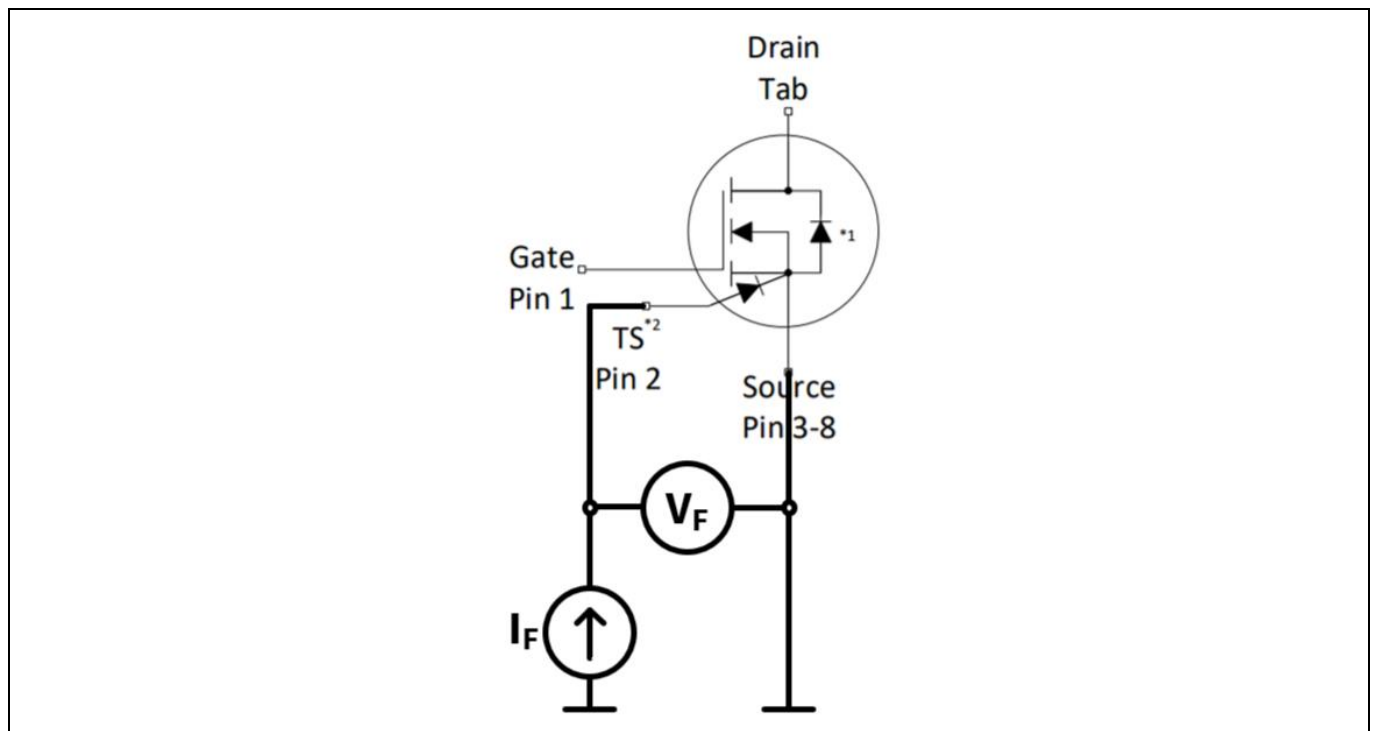


Figure 7 Simplified schematic for temperature read-out

As can be seen in [Figure 7](#), it is necessary to force a current (I_F) through the temperature sensor. This current is stated in the corresponding datasheets and can be typically set to 200 μA . At the same time, it is possible to sense the voltage from the temperature pin to source (V_F).

Due to the fact that there is no longer any driver source, the sensing of the V_F is also influenced by parasitic resistances such as the design, the package, the PCB and the drain current flowing. It is generally recommended to locate the V_F as close as possible to the pins or directly on them. The related datasheets of the S7T products represent the ideal connection without parasitics. This means the designer needs to know which I_D is flowing and what the parasitics are in the sensing loop. In order to provide an easier adaption, the available simulation models of the S7T family have the parasitics from design and package resistances included. Therefore, it is recommended to verify the resulting V_F and T_J correlation of the customer system via a Spice simulation.

3.2 Hot-spot to thermal sensor ΔT

[Figure 8](#) shows that the temperature sense diodes are not directly in the center of the active area of the chip. There is still a distance between the real hot-spot coming from the center of the active area to the temperature sense diodes.

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This results in a delta of temperature between hot spot and temperature sensor, which needs to be considered by the designer. The following figure shows this behavior.

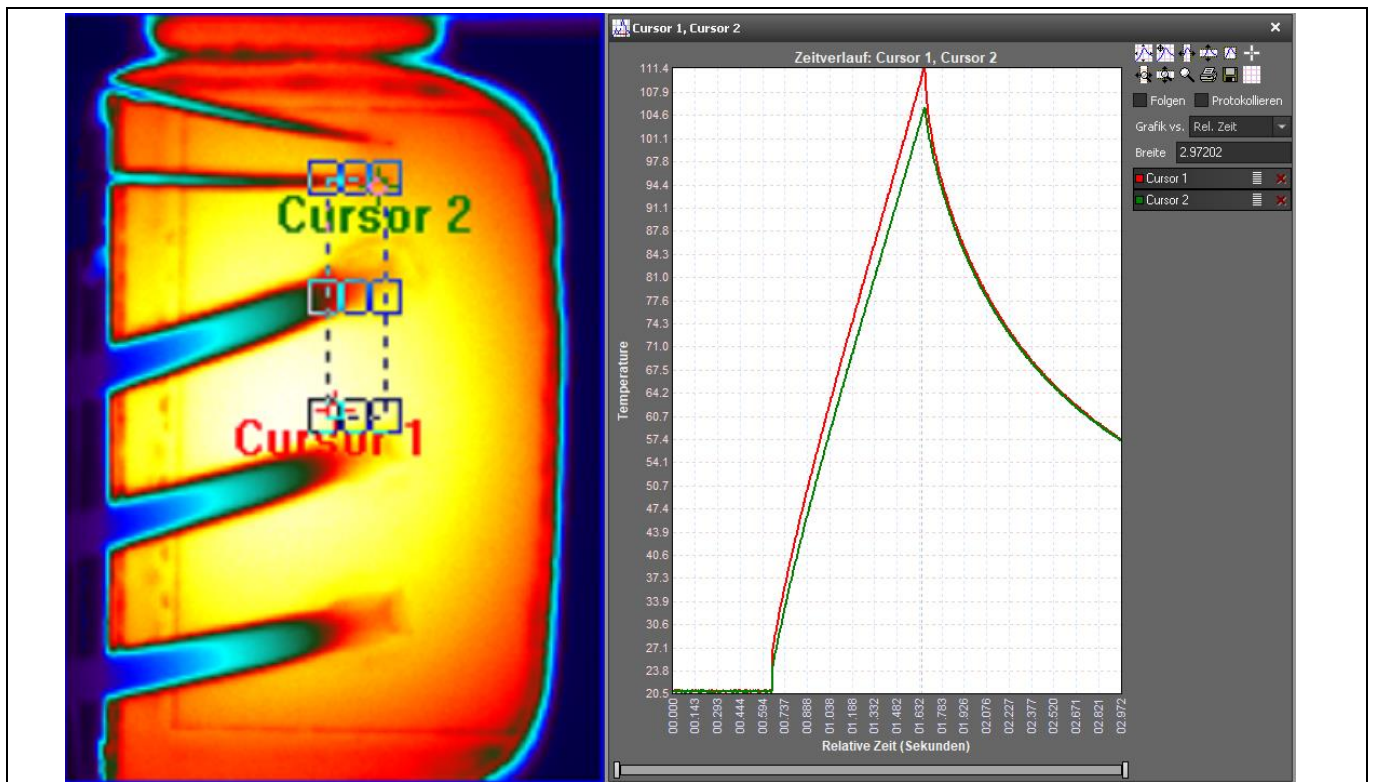


Figure 8 Delta hot-spot to temperature sensor

In this figure it can be seen that the hottest point is located at “Cursor 1”, which is the center of the active area. “Cursor 2” is at the location of the temperature sense diodes. In the diagram on the right the red line corresponds to the temperature of the hot-spot and the green line represents the temperature of the diode sensor. Due to this distance and the thermal impedance between these two locations a delta temperature (ΔT) of ~5 K is present. As there is a thermal impedance this ΔT depends on the settling time, meaning for shorter heat pulses the delta is higher than with long heat pulses. The diagram below will show the behavior of the ΔT for each product.

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Temperature read-out

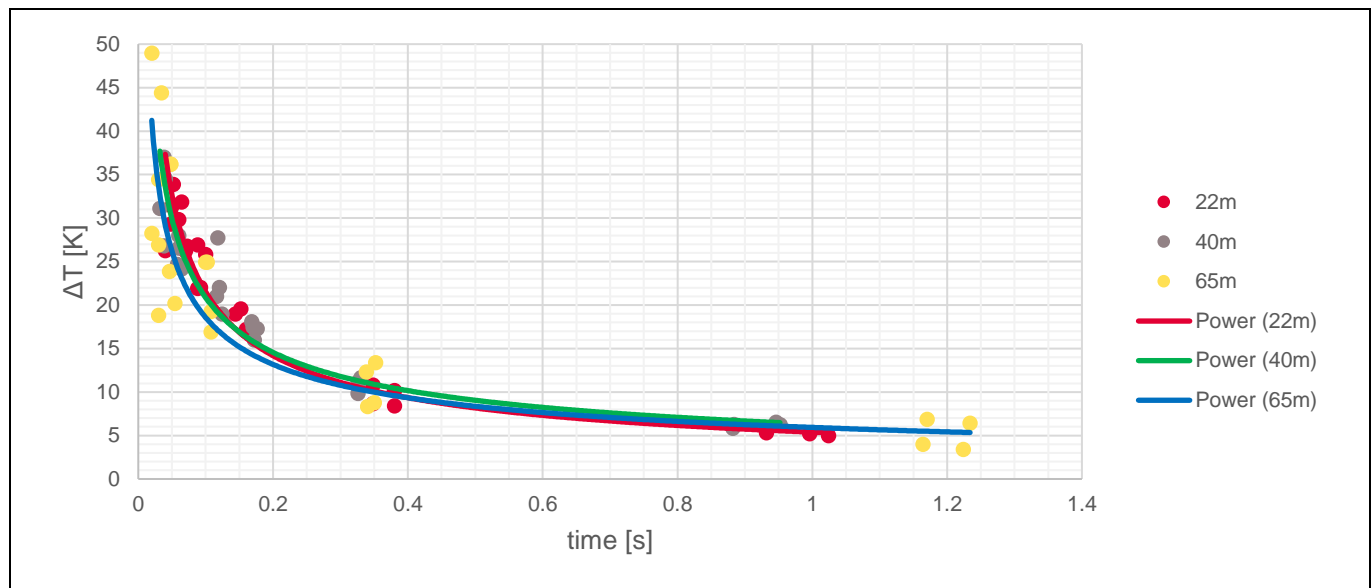


Figure 9 Delta between hot-spot and temperature sensor depending on heat pulse

Based on this diagram the following delta temperatures can be extracted.

Table 1 Delta temperature depending on heat pulse

Time	ΔT
Less than 50 ms	More than 30 K
Less than 100 ms	More than 20 K
Less than 400 ms	More than 10 K
Less than 1 s	More than 5 K
More than 1 s	~5 K

Notice that these time constants do not evolve with component aging and thus can be hardwired into the measurement setup to compensate for these differences.

Furthermore, the delta temperature can be explained over the power per mm^2 on the different dies. [Figure 10](#) to [Figure 12](#) are describing this for each available $R_{DS(on)}$.

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Temperature read-out

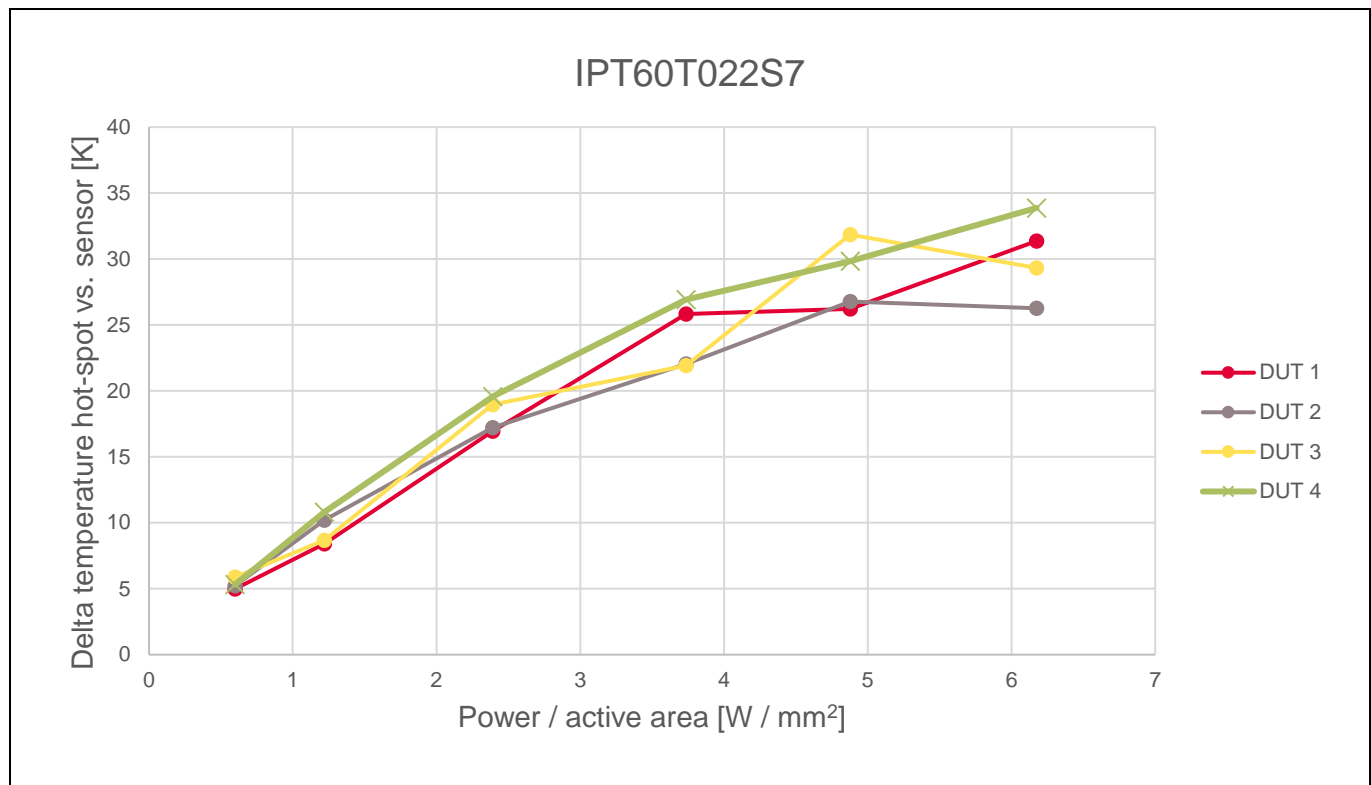


Figure 10 ΔT of hot-spot vs. sensor over power per active area IPT60T022S7

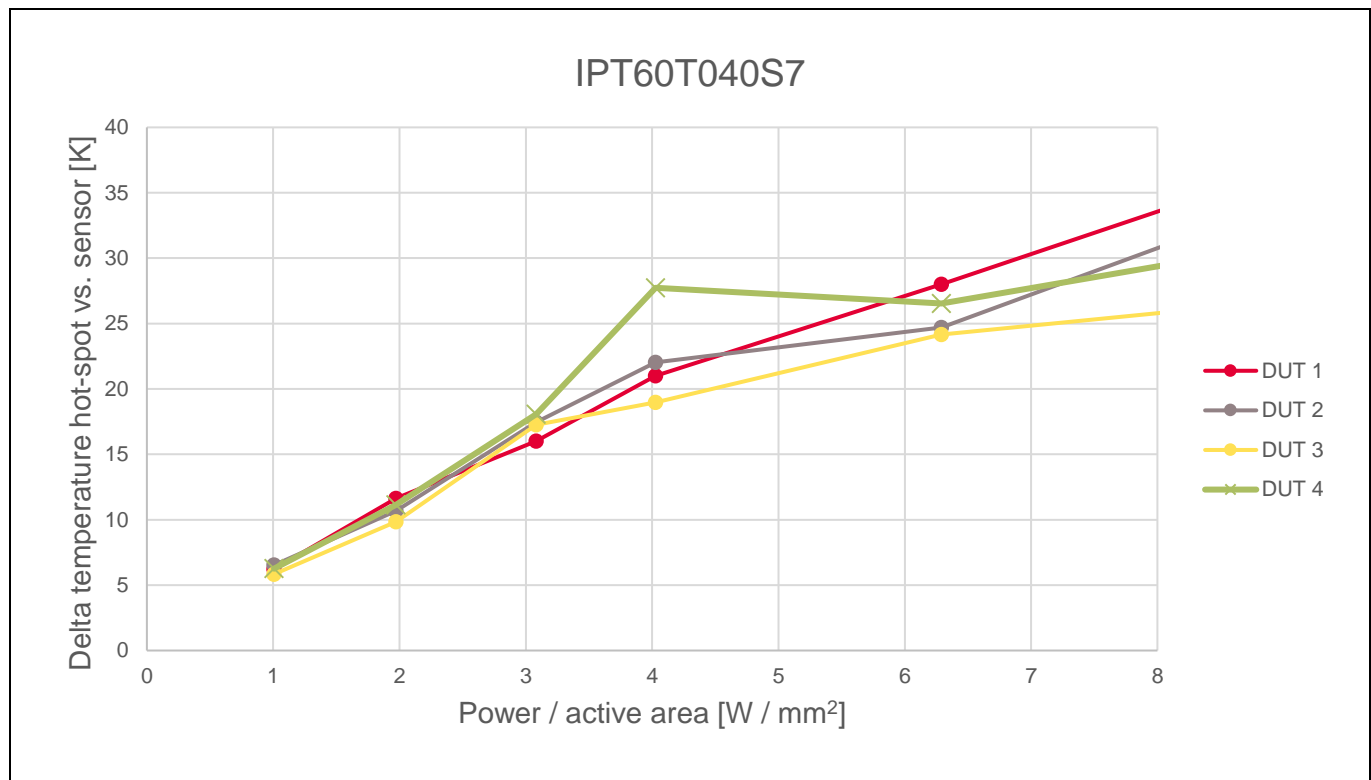


Figure 11 ΔT of hot-spot vs. sensor over power per active area IPT60T040S7

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Temperature read-out

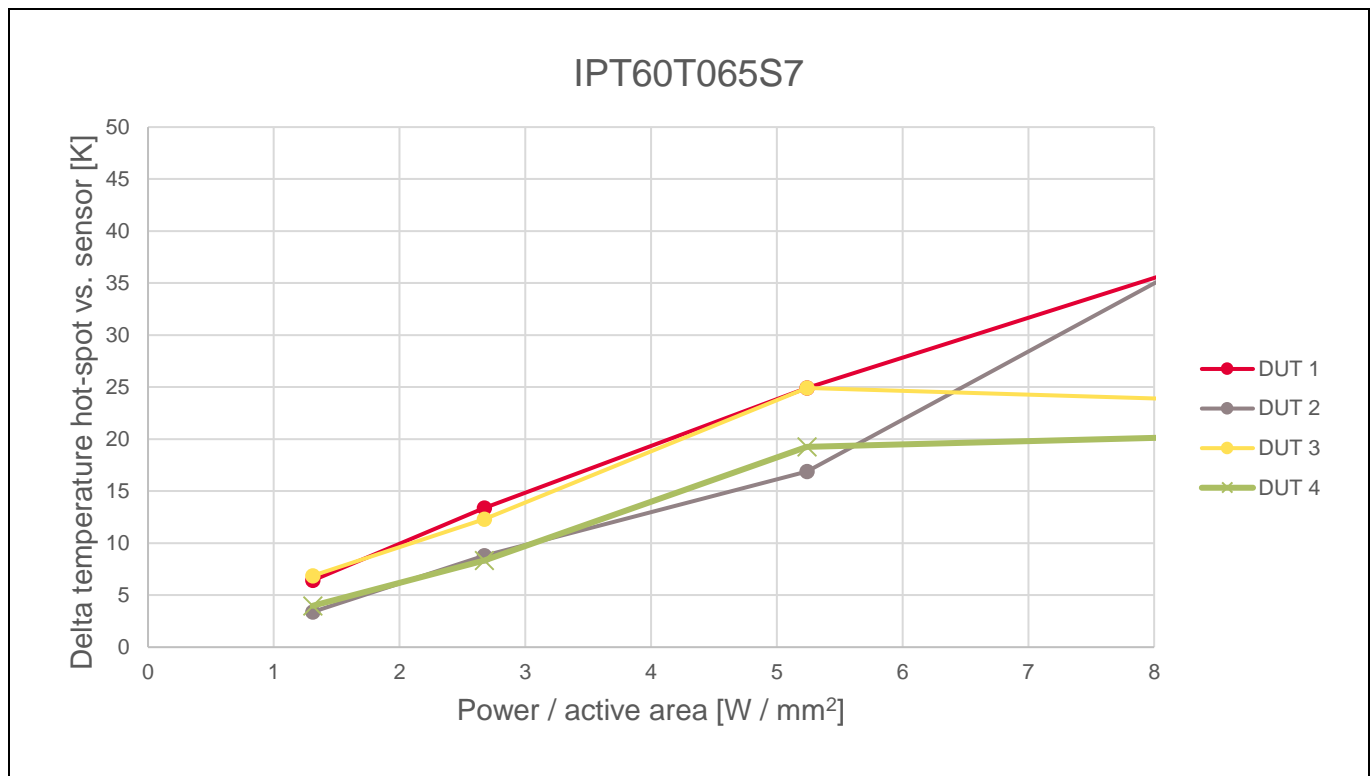


Figure 12 ΔT of hot-spot vs. sensor over power per active area IPT60T065S7

As can be seen from [Figure 10](#) to [Figure 12](#), the higher the power per active area, the higher the difference between different DUTs. Nevertheless, the samples show excellent consistency and reproducibility in the typical operation range from 2 - 3 W/mm². Only IPT60T065S7 shows a delta also in this range. This results from solder differences from the package to the PCB (test board).

To show the operation of the new product, the next chapter will show application tests tailored to verify the functionality of the temperature sense and product ruggedness.

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Application measurements

4 Application measurements

4.1 Overtemperature test

The goal of this test is to verify the functionality of the temperature sense and the interaction with the gate driver to control safe turn-off of the devices. For this a new Infineon gate driver is used. For more information please see the Infineon website (search for “iSSI30R12H”).

The following figure shows the evaluation board and the corresponding block diagram.

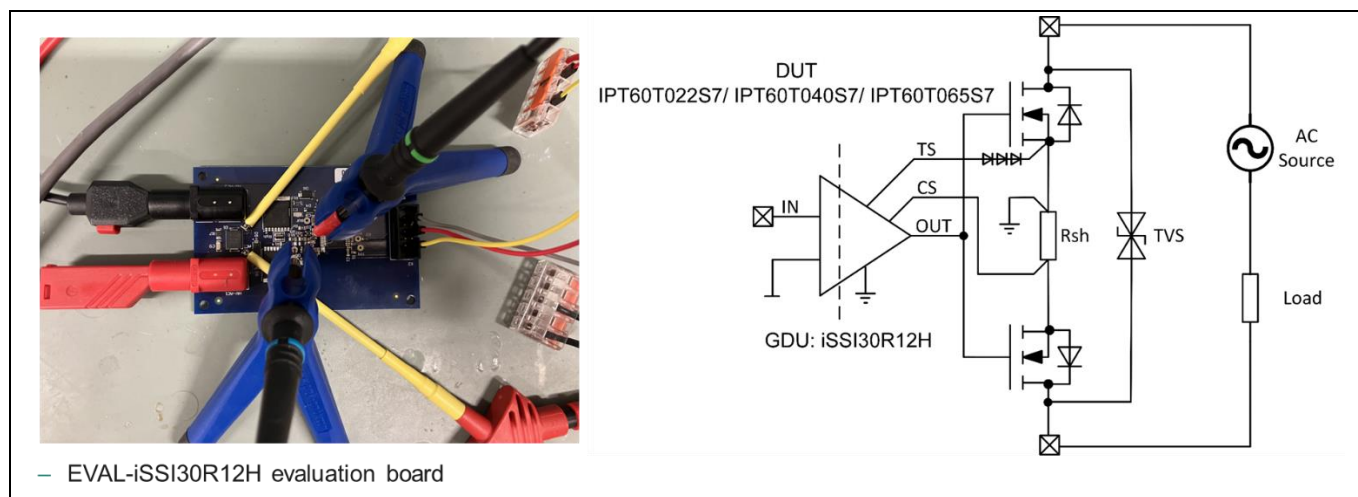


Figure 13 Overtemperature test setup

For this test an AC signal is applied and the devices under test (DUTs) are turned on. The load forces a certain sinusoidal current to flow through the DUTs until the defined threshold voltage on the TS pin is reached and the gate signal is removed (see [Figure 14](#)).

The load is chosen so that a slight overload condition is present, which heats the device constantly. This should lead to a constant drop in the measured forward voltage between the TS and ground pins over time.

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Application measurements

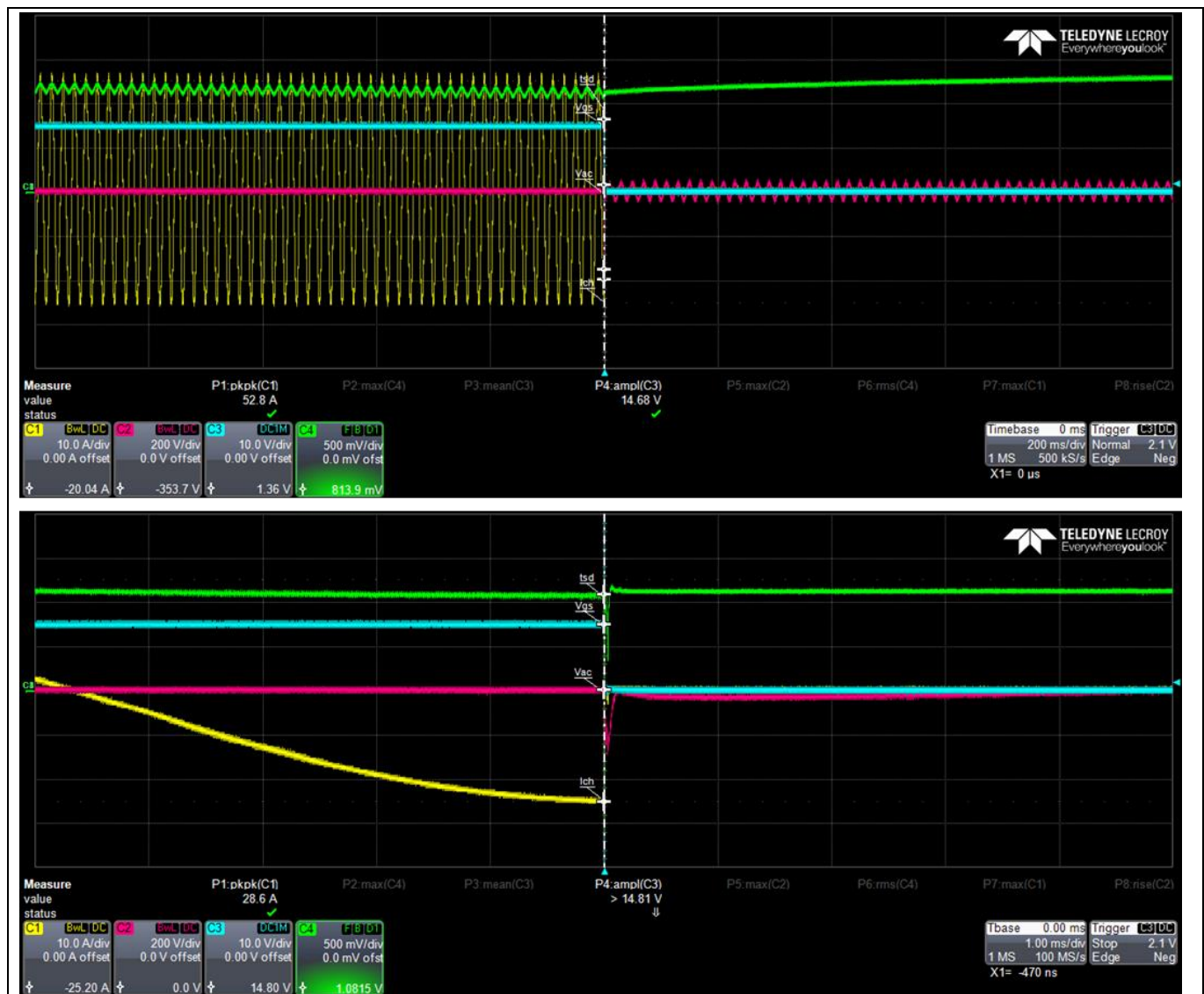


Figure 14 Waveforms overtemperature shutdown test (“green” TS pin voltage; “yellow” drain current; “magenta” V_{DS} ; “cyan” V_{GS})

In the figure above the shutdown of the current transfer is clearly visible and the TS pin voltage is increasing as the devices are cooling down again. This test was performed on several devices for all products and demonstrates that the temperature sense can work as an additional safety feature in all relevant applications.

4.2 Overcurrent test

This test is introduced to verify the current-switching capability of the new products. Particularly in solid-state applications, the drain current can achieve values close to the pulse current rating in the products’ datasheets. Therefore, it is very important to verify if the devices are suitable for turning off these high currents safely. For this test the same setup as before is used, but without the temperature sense functionality. The following figure shows this test, which is also performed on a number of samples for each product to ensure datasheet limits.

As this is intended to test ruggedness, all samples have been tested up to the application requirement for solid-state solutions. For the use case described in this application note a 5 mΩ shunt was used and the current sense (CS) threshold limit between 185 and 215 mV was implemented. This leads to an overcurrent shutdown at ~40 A.

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Application measurements

Even the lowest $R_{DS(on)}$ devices in the portfolio passed this test, which can be seen in the following figure.

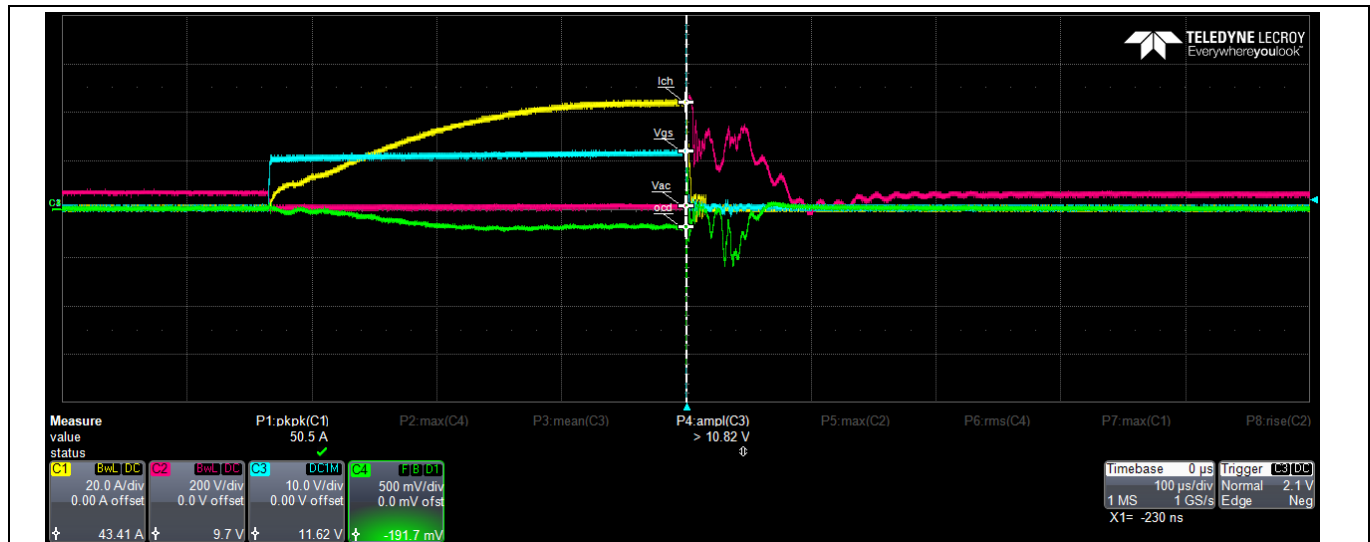


Figure 15 Overcurrent shutdown test waveforms (“green” CS voltage; “yellow” drain current; “magenta” V_{DS} ; “cyan” V_{GS})

During the high current turn-off, it can be seen that the devices are driven into avalanche operation due to the inductance in the current path. During the design-in phase it is necessary to stay below the rated avalanche characteristics, which are limited and indicated in the corresponding datasheets.

4.3 AC-15 test

The AC-15 utilization category is described in IEC 60947-5-1 and considers a system with a nominal current of 2 A. The test uses a highly inductive load with a power factor of less than 0.3. A high inrush current, at least 10 times the nominal current, is conducting, as can be seen in the following figure.

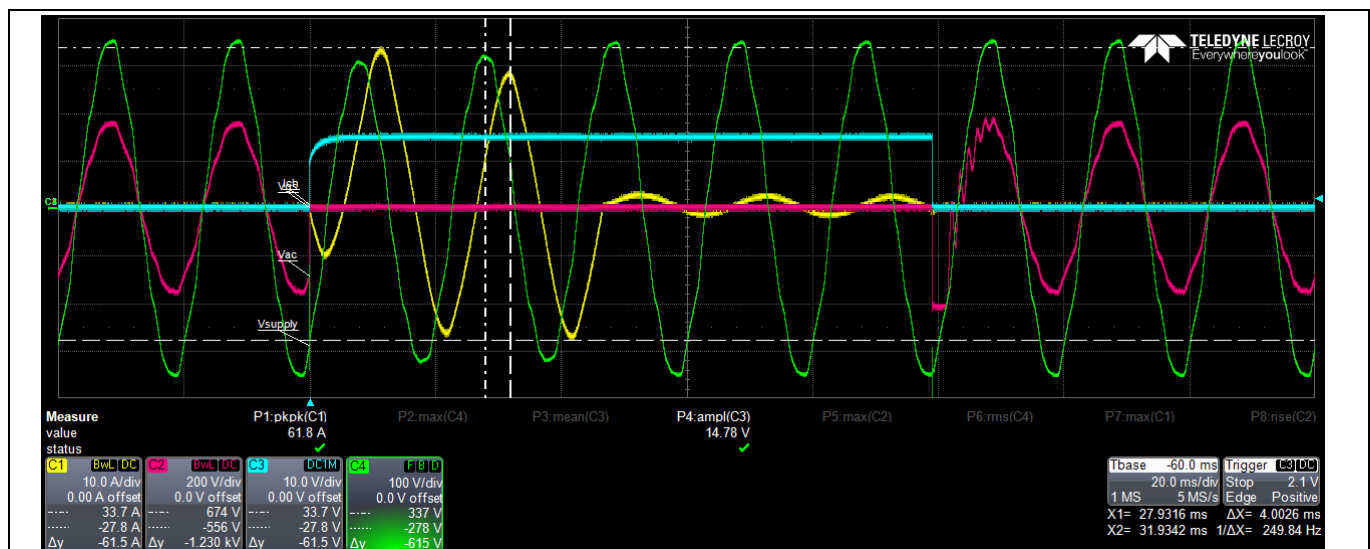


Figure 16 AC-15 test waveforms (“green” supply voltage; “yellow” drain current; “magenta” V_{DS} ; “cyan” V_{GS})

In [Figure 16](#) a peak inrush current of 33.7 A and a working peak current of 3.3 A can be seen. This test was performed to show the functionality in a real application environment. All devices of all $R_{DS(on)}$ classes survived

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the AC-15 test. The important safety element in this test is the TVS diode, which needs to be properly dimensioned, as a turn-off in the inrush current period can be critical and is generally recommended to be used. The simplified block schematic can be seen in the following figure.

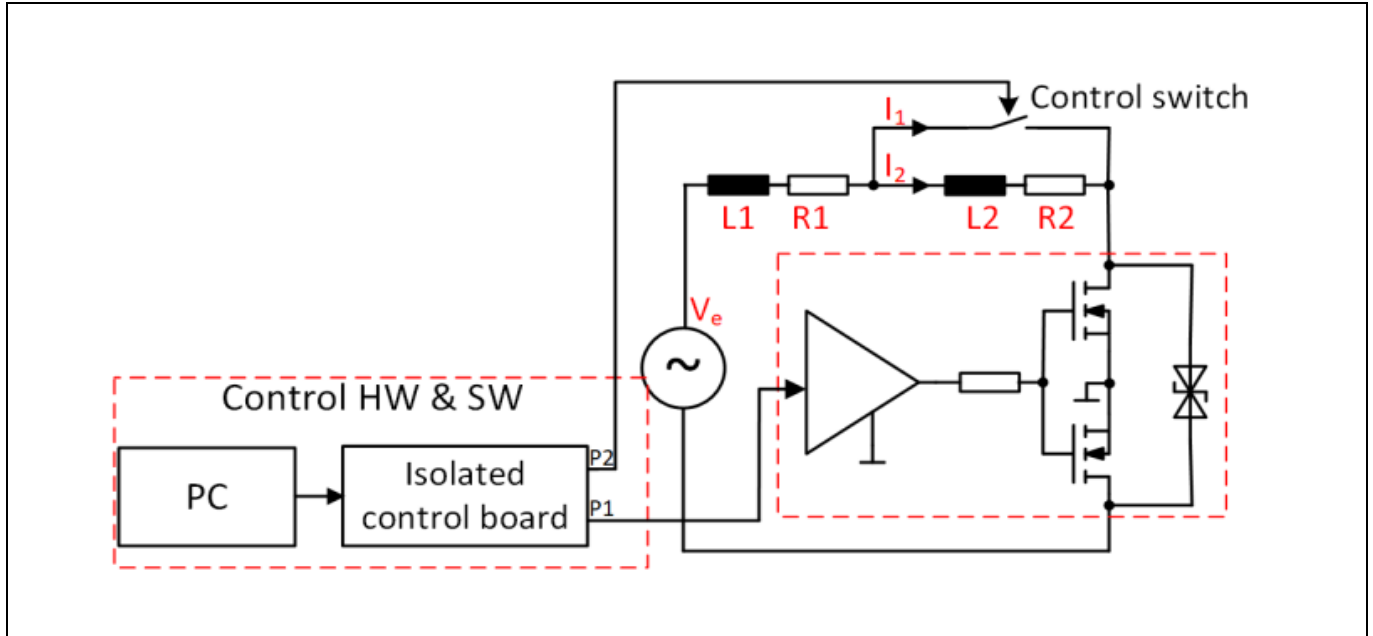


Figure 17 Block schematic of AC-15 test

The final chapter in this application note will focus on the power cycling capability of the new CoolMOS™ S7T family.

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Power cycling test

5 Power cycling test

During a power cycle measurement, the DUT is heated up to a preset junction temperature T_J of 150°C, by running a constant load current through the device for a fixed time. The load pulse results in a T_J which is typically around the $T_{J,max}$ of the DUT. After heating up, the device is cooled down for a fixed time to the inlet temperature of the cooling block. This process is repeated until the device breaks, due to thermo-mechanical stress on the different materials used inside. Faults are developed at different interfaces from the device die attachment and wire bonds all the way to PCB and heatsink.

As the power cycling standards are application specific, we recommend that the designer qualifies the devices based on their mission profiles and application behavior.

5.1 Test setup

To perform the measurements, the test setup shown in the following figure is used.

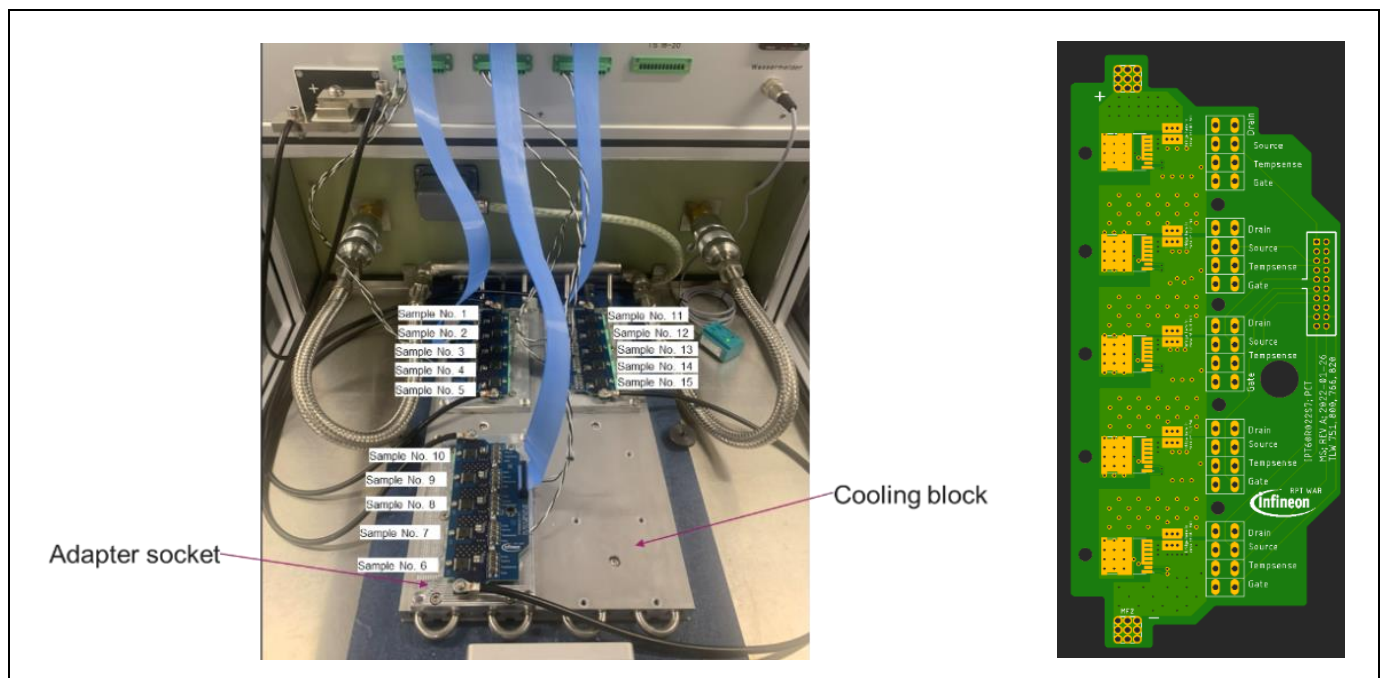


Figure 18 Test setup for power cycling test

The adapter PCBs contain the soldered DUTs and are supplied with the test current for heating up the samples. The samples are in series connection. These PCBs are mounted on a cooling block, which has suitable adapter sockets to ensure a good cooling performance. Each PCB has a total of five MOSFETs in the TOLL package, soldered in series. The junction temperature is determined by measuring the calibrated temperature sense voltage of the DUT shortly after the load current is turned off. In the test setup shown in [Figure 18](#), a total of 15 samples can be measured at the same time.

Due to the thermal stress inside the MOSFET die, the junction temperature T_J and the voltage drop from drain to source change with the number of switching cycles. A change in the junction temperature also results in a change of the thermal resistance chain from junction to ambient ($R_{th,JA}$). To make sure the device is still working without any damage caused by thermal stress, the following criteria are set.

The power cycling test promotes deterioration of the interfaces that carry the heating current and conduct the heat away from the die. The former is detected by monitoring the on-state voltage and the latter is monitored through the temperature difference between the junction and the heatsink.

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Power cycling test

The industry-standard end-of-life criteria for modules were adopted: thermal resistance increases above 20 percent or a drain source voltage drop exceeding 5 percent of the initial value.

5.2 Test results

The results of this test for each product are visible in the following table. The cooling block has a constant temperature of 25°C.

Table 2 First failure after power cycling

Product	Stress current [A]	Average $T_{J,max}$ [°C]	First failure after [cycles]
IPT60T022S7	52	159	20,500
IPT60T040S7	36	156	32,900
IPT60T065S7	26	180	33,000

All experiments were stopped due to increased thermal resistance. The number of cycles to failure is unusually low for discrete devices. This prompted us to investigate further and identify the weak spot in the thermo-mechanical assembly of the devices.

5.3 Power cycling test strongly depending on solder interface from package to PCB

After the power cycling test, the PCBs and the DUTs were checked by X-ray. The X-ray pictures indicate severe deterioration of the solder between package and PCB, with extended voids from the PCB through-vias, mostly concentrated below the center of the device package.

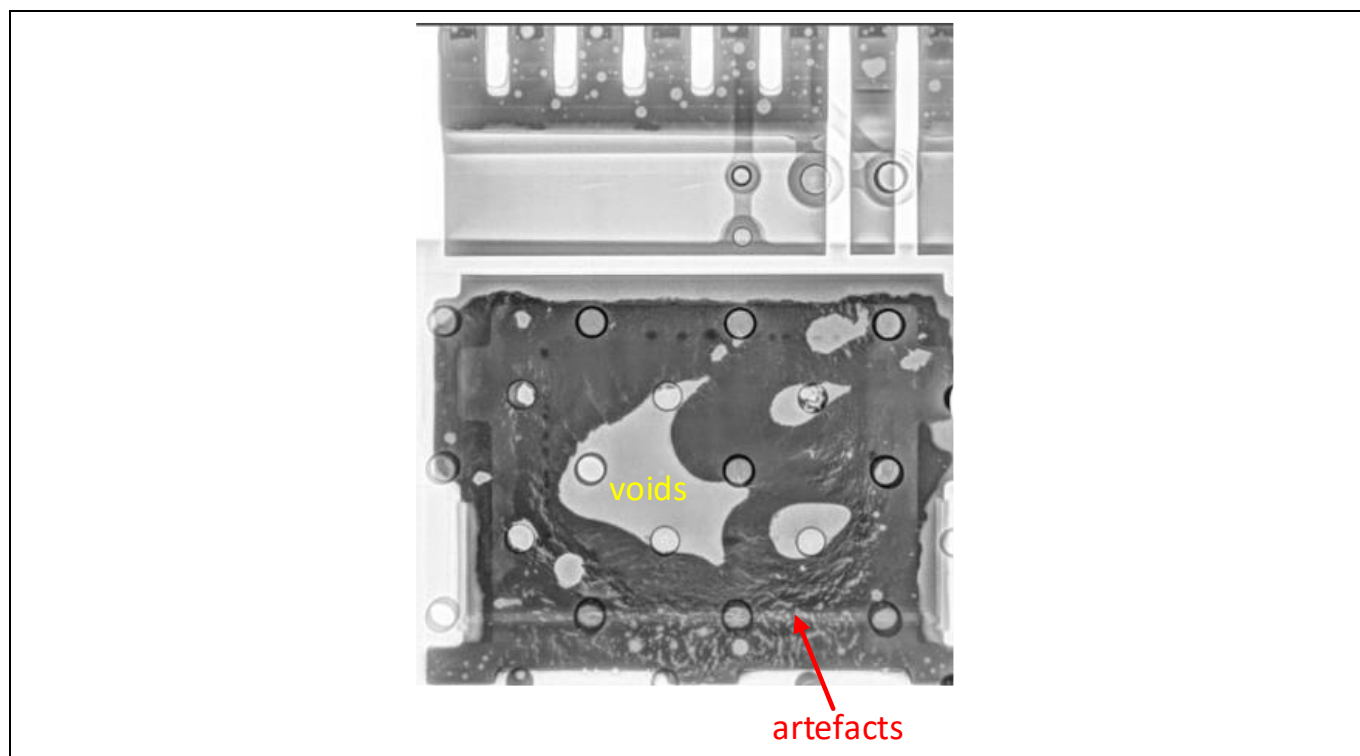


Figure 19 Artefacts in the solder between package and PCB

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Power cycling test

This was confirmed by a cross-section of the PCBs and the DUTs, where extended (virtually complete) delamination of the solder PCB/package layer is clearly visible. The state of the PCB solder is similar for all samples investigated.

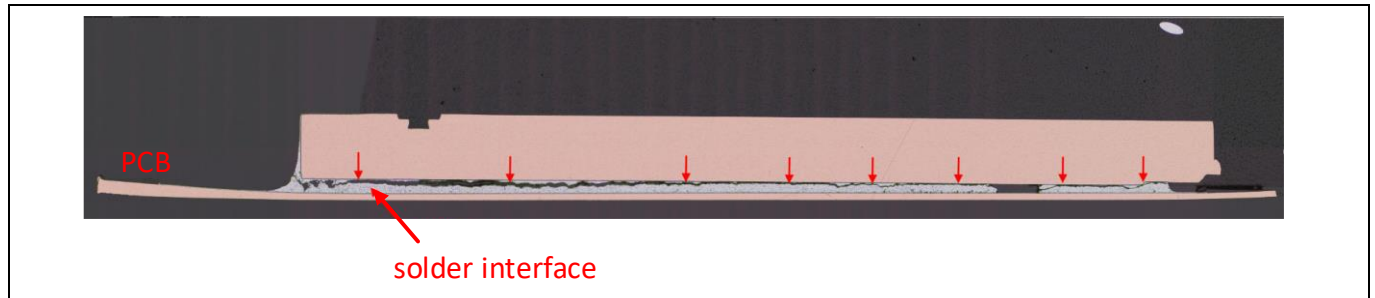


Figure 20 Cracks in solder interface between package and PCB

This degradation of the solder joint between the DUT and the PCB is caused by different materials and their expansion coefficients. This adds stress, causing the final cracking of the interface material.

Based on the investigation above and the fact that all failed DUTs in the power cycling test have shown these artefacts, it is clear that the interface and the solder quality are key to achieving high power cycle ruggedness.

Should greater power cycling ruggedness be necessary, we recommend the following:

- Use blind vias below the solder pad of the package to avoid concentration of stress.
- Use solders known to have increased resistance to metal fatigue.
- Use soldering profiles that guarantee the absence of initial voids (known to promote crack inception and propagation).

6 Summary

This application note has described the newest CoolMOS™ S7T family, which brings an additional protection feature that can increase safety in all target applications. Furthermore, the differences in the CoolMOS™ S7 were given, describing the exchange of the driver source pin with the temperature sense pin. Thirdly, the delta temperature between temperature sense and hot-spot was discussed. Last but not least, application and ruggedness measurements were shown, including the finding that the solder joint degradation between package and PCB is the main criteria for power cycling operation. All of the above point to the fact that CoolMOS™ S7T is the ideal technology for various applications such as SSCBs, motor starters, μ Grids, power distribution units and, in future, also automotive applications such as eFuse and battery main switch.

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Revision history

Revision history

Document revision	Date	Description of changes
V 1.0	2023-12-04	Initial release

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