A new approach to datasheet maximum drain current I_D rating of low voltage MOSFETs

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About this document

Scope and purpose

In recent years the continuous reduction of on-resistance of MOSFETs has been the most important factor in improving system performance of high-power applications. Low $R_{DS(on)}$ devices reduce losses in the silicon, which in turn allows higher chip currents. As a consequence, packaging becomes more critical for higher-performance devices. In many cases, the package properties define an upper limit for the current-handling capability. This is especially the case for low-$R_{DS(on)}$-resistance products.

Datasheet current limits are common parameters for component selection in the field of power applications such as forklifts, low-speed cars and power tools. Products are compared against each other, where a fair comparison requires a definition of current limits based on standardized boundary conditions.

A new method to define nominal product currents based on a consistent set of boundary conditions is shown here. This new approach does not consider the silicon chip and package independently, but uses a product approach, taking into account resistive losses and temperatures in the entire component.

The goal of this application note (AN) is to provide detailed information on how Infineon is defining the datasheet continuous maximum drain current I_D of low voltage (LV) MOSFETs. In order to identify whether a datasheet is made according to the new method of I_D current rating, please refer to Appendix 1.

Intended audience (background)

In high-power designs in which MOSFETs have to conduct high currents, a hardware designer will often select a component based on the I_D rating, a datasheet parameter which can be different from manufacturer to manufacturer for the same package. In reality, these numbers should be the same for the same chip dimensions, bond wires and package characteristics, but due to different definitions of test conditions, such as different boundary conditions or derating assumptions, one manufacturer may claim higher current than another.

However, the numbers could be different due to package variants, such as pin dimensions, leadframe thickness or different silicon technologies. Ideally, the product current rating in a datasheet should be standardized, to enable a designer to select the appropriate product.

This calls for an improved method using standardized conditions, which is able to show the benefit of individual chip and package modifications. This method provides the necessary deratings for actual conditions in the application.

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1 Product current limit specifications

Commonly, the maximum drain current I_D in a MOSFET is limited by temperature in either:

- the silicon die, or
- the package.

In order to determine the maximum drain current, several conditions and limits need to be defined, including the following:

- Printed Circuit Board (PCB) temperature
- Maximum die temperature, commonly referred to as the MOSFET's maximum junction temperature $T_{j,max}$
- Maximum bond wire temperature

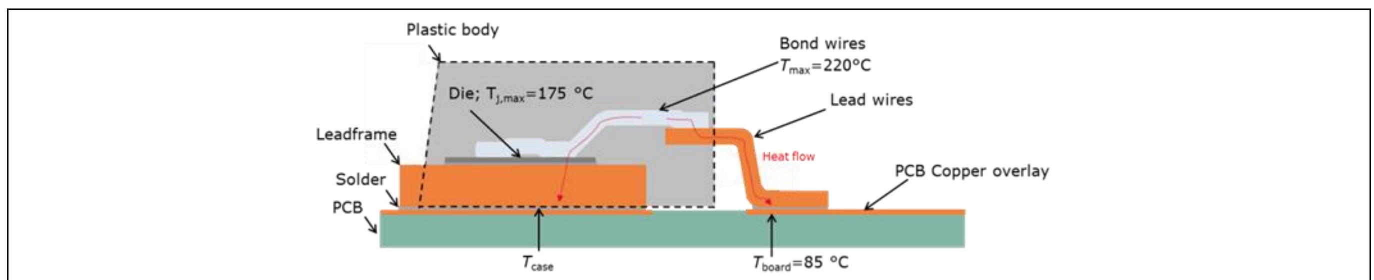


Figure 1 D²PAK cross-section and individual components of the package

In Figure 1 we can identify multiple components of a D²PAK package. In the previous calculation method, Infineon was considering the following boundary conditions for the calculation of the chip-independent package current limit. These conditions are as follows:

- Board temperature is set to 85°C, as this was roughly the limit for most standard FR4 PCBs (now an outdated specification, as the PCB technology has evolved and improved)
- Chip temperature is set to $T_{j,max}$ (typically 175°C)
- The maximum temperature along the wire should not exceed T_{max} = 220°C, which is based on the glass transition temperature of the package mold compound
- Radial heat flow from the bond wire to the mold compound is not taken into account for bond wires larger than 250 µm (10 mils); the mold compound is in physical contact with the bond wires, effectively cooling the bond wires

Based on these assumptions, the maximum package current was calculated and, if smaller than the nominal chip current, it was used as product continuous drain current I_D. This is a fairly straightforward method and has been in use for many years.

However, this approach has some drawbacks. In reality, the chip cannot be considered separately from the bond wires or the leadframe when the product continuous drain current I_D is calculated. In particular, low-ohmic devices will have a far lower junction temperature than $T_{j,max}$ when operated at I_D and ideal cooling at the component surface (T_{case}) is applied. In addition, better PCBs and cooling techniques result in temperatures at the lead wires that are lower than the assumed 85°C. In general, a calculation method should be flexible so that for any board temperature the appropriate derating can be applied.

The new method improves on the previous approach. In detail, the assumptions are the following:

- The product nominal current is based on a case temperature of 25°C; the same temperature is assumed for the lead wire temperature on the board (T_{board}), and the necessary derating at higher temperatures is shown in a diagram, where, for simplicity, $T_{case} = T_{board}$
- The junction temperature T_j is calculated at the temperature-dependent maximum on-state resistance $R_{DS(on)}$ and the maximum thermal resistance R_{THJC}; the maximum temperature is the value stated in the datasheet, $T_{j,max}$
- The maximum bond wire temperature is set to 220°C – no change
- The radial heat flow from wire to mold compound is considered only for thin bond wires (less than or equal to 125 µm)

The new approach yields higher nominal product currents for devices with lower on-state resistance, which is in line with expectations. The assumption of a standardized PCB temperature of 25°C allows for a better comparison with competitor parts.

The calculation requires an iterative approach, as the temperature profile along the package internal current path needs to be computed. This approach utilizes the board and case temperature, the current and the respective chip, bond wires and package lead dimensions. In addition the temperature-dependent material properties of the MOSFET, wires and leadframe are used.

1.1 Impact of the board and the chip temperature on I_D rating

To visualize the effect of the old and the new current calculation method, the D²PAK product IPB017N08N5, with three 500 µm (20 mils) bond wires, is used as an example. The product has a maximum on-state resistance of 1.7 mΩ at 25°C. The solid lines in Figure 2 show the maximum allowable drain current dependent on board temperature, and a junction temperature based on the assumptions made above. In particular, the lines in the chart show the necessary drain current derating if the board temperature at the source leads cannot be kept at 25°C.

The old current calculation method assumed a junction temperature of T_j = 175°C, thereby not taking into account the low on-resistance of the product, which normally would not reach this temperature, and the board temperature was assumed to be 85°C. With these boundary conditions, the maximum current was determined to be I_D = 120 A (orange data point).

The new method requires a parallel calculation of the junction temperature and the package limit until convergence is reached. The junction temperature can be calculated dependent on drain current, temperature-dependent on-state resistance, and thermal resistance R_{THJC}. The dashed line in Figure 2 shows the necessary current to reach a certain junction temperature T_J at the case temperature T_C = 25°C.

For this particular product an equilibrium is established at a junction temperature of 49°C and a current of I_D = 177 A assuming standardized boundary conditions of $T_{case} = T_{board}$ = 25°C and the technology-specific temperature coefficient of the on-state resistance.

$$T_j = T_{case} + P_{tot}R_{THJC} = T_{case} + I_D^2 R_{DS(on)} R_{THJC} = 25°C + 177\ A^2 * 1.88\ m\Omega * 0.4 \frac{K}{W} = 49°C$$

This result can be obtained graphically by looking at the intersection of the T_{board} = 25°C package line and the dashed chip line in Figure 2 (green data point). Deratings for other board temperatures can be concluded from the graphics.

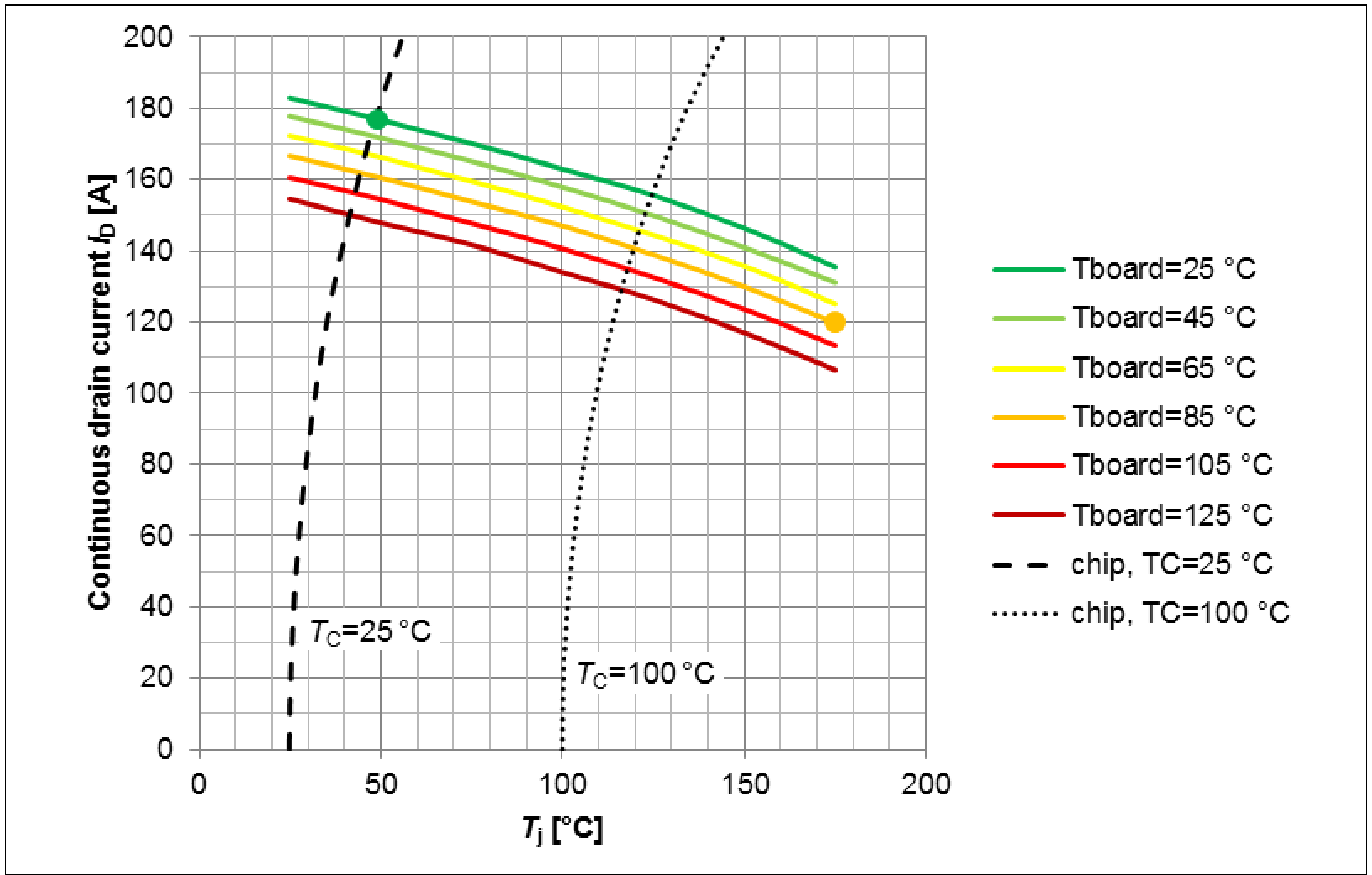


Figure 2 **Graphical representation of the old and the new method of drain current determination**

With a worst-case assumption of T_j = 175°C and a board temperature at the source lead of 85°C (orange marker), the nominal drain current is 120 A, which confirms the result from the old method used. The new method takes into account the low resistance of the MOSFET and better cooling on the board with a standardized temperature of 25°C both at the package case and the leads. This new method results in a nominal drain current of 177 A.

2 Affected datasheet diagrams and how to read them

The following datasheet parameters may change depending on the MOSFET's package and its $R_{DS(on)}$:

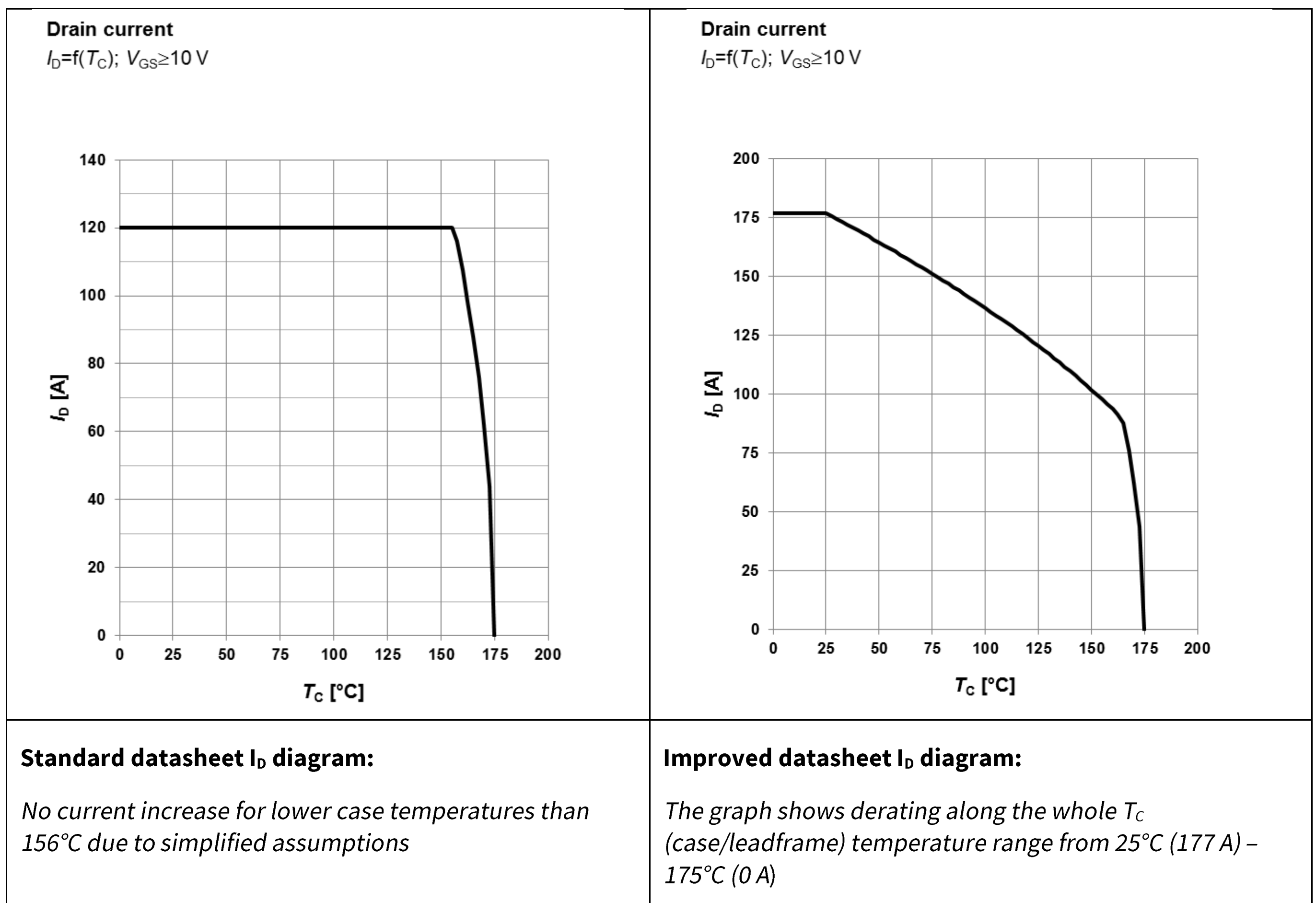
- I_D at T_C = 25°C
- I_D at T_C = 100°C
- $I_{D,pulse}$ at T_C = 25°C
- Diode continuous forward current I_S
- Diode pulse current $I_{S,pulse}$

The following datasheet graphs may change depending on the MOSFET's package and its $R_{DS(on)}$:

- Drain current I_D
- Safe Operating Area (SOA) diagram

2.1 Drain current I_D

An obvious change in the datasheet will be the derating graph of the drain current I_D versus case temperature T_C. In datasheets, the diagram is calculated assuming the same temperature at case T_C and at the source lead(s) (T_{board}). The resultant diagram for the device IPB017N08N5 is shown in Figure 3. As mentioned above, the maximum on-state resistance of this D²PAK product is 1.7 mΩ, and the worst-case thermal resistance is 0.4 K/W. Whereas the old datasheet shows no increase of allowable drain current if the case temperature T_C is reduced, the new approach allows higher currents in case of good cooling of the package leadframe.



Standard datasheet I_D diagram:

No current increase for lower case temperatures than 156°C due to simplified assumptions

Improved datasheet I_D diagram:

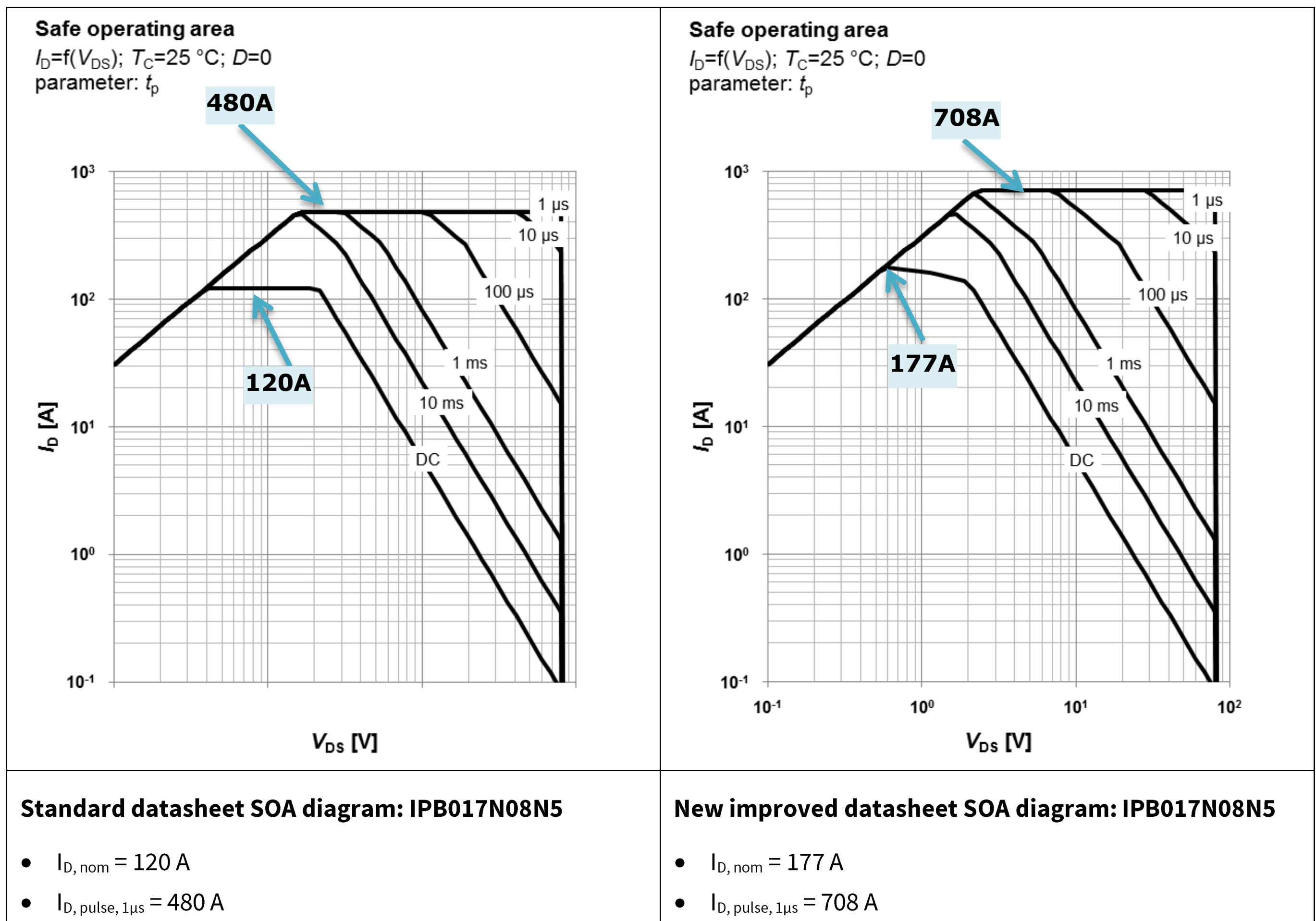
The graph shows derating along the whole T_C (case/leadframe) temperature range from 25°C (177 A) – 175°C (0 A)

Figure 3 Comparison of old and new I_D derating diagram

2.2 Safe Operating Area (SOA) diagram

The new method is based on a calculation of the junction temperature where the benefits of low on-state resistance allow higher continuous drain currents. If, however, the device is not fully turned on, it operates in linear mode, characterized by higher V_{DS}. Due to the higher power dissipation in the chip, some derating has to be taken into account. As a consequence, the part of the DC-line that has so far been flat in the SOA diagram changes. At low V_{DS} the DC-line reaches the continuous drain current I_D, whereas at higher V_{DS} the line approaches the power limit line [1].

Generally, the new calculation method is also applied to transients. New datasheets also show an increase in the pulse current $I_{D,pulse}$.



Standard datasheet SOA diagram: IPB017N08N5	**New improved datasheet SOA diagram: IPB017N08N5**
• $I_{D,\,nom}$ = 120 A • $I_{D,\,pulse,\,1\mu s}$ = 480 A	• $I_{D,\,nom}$ = 177 A • $I_{D,\,pulse,\,1\mu s}$ = 708 A

Figure 4 Comparison of the old and the new SOA diagram of IPB017N08N5

2.3 Diode currents

A similar approach is used for the definition of maximum diode currents. In many cases, diode forward currents (I_F or I_S) are lower than MOSFET currents I_D as the power loss in diode operation is higher than at MOSFET on-state conditions. For the example IPB017N08N5, the diode continuous forward current is 152 A.

3 Bench test

The circuit depicted in Figure 5 has been implemented to confirm the continuous current capabilities of a MOSFET. In the test, the Device Under Test (DUT) is not switching in order to avoid very high switching losses and test the package limit with the die.

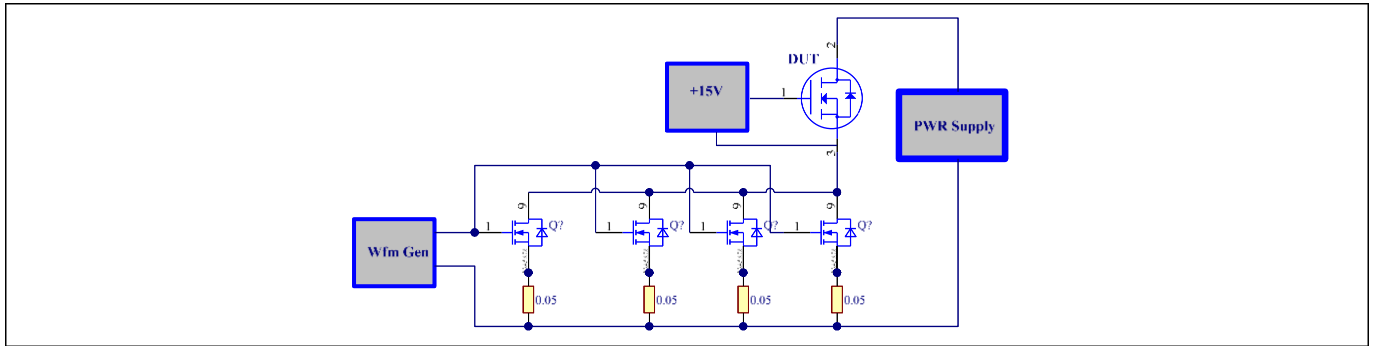


Figure 5 Test circuit

Figure 6 shows details of the mechanical set-up. Such a concept with a direct copper attachment to the MOSFET's leadframe can be achieved with a copper inlay PCB.

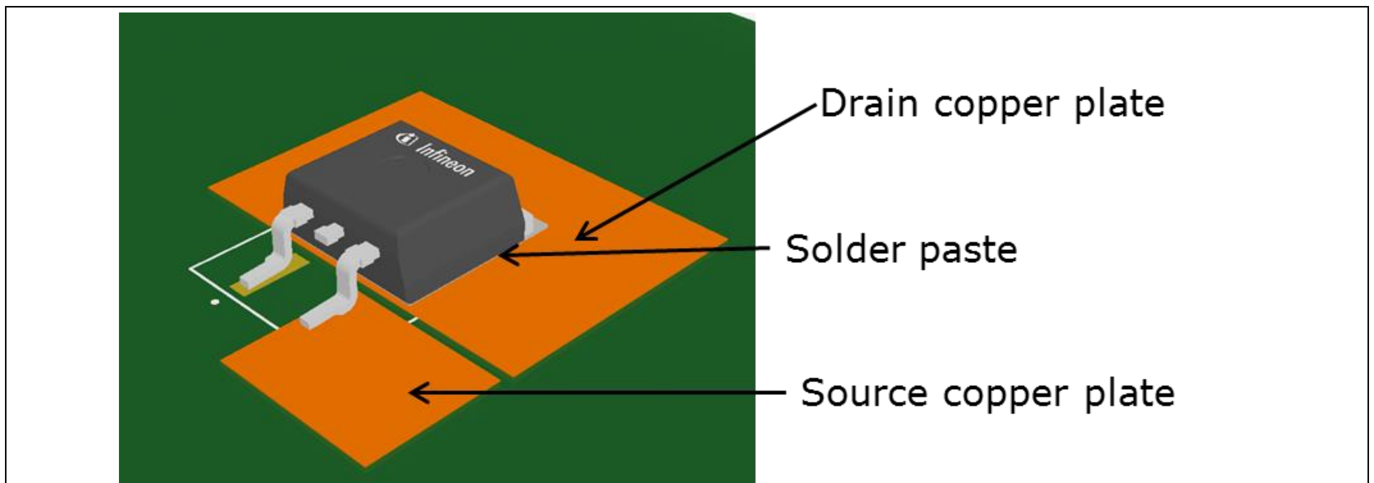


Figure 6 D²PAK mounted on test PCB with copper inlay

The MOSFET is directly soldered to the copper plate in order to achieve best possible thermal resistance between the leadframe and heatsink.

- The solder thickness is ~100 µm
- The drain copper plate is 10 cm × 5 cm and 2 mm thick
- The source copper plate is 5 cm × 2.5 cm and 2 mm thick

In order to establish nominal conditions of 25°C at the source lead and the heatsink, the pulse duration was reduced to 200 ms, which is applied every 5 s (Figure 7). Such pulse lengths can be considered as steady-state for the device, but still transient for the PCB due to its large thermal mass. As a consequence, the temperature of the copper plate will remain close to the ambient temperature.

In the example above using IPB017N08N5, which is rated at 177 A, the MOSFET was tested up to the current source output limit of 315 A (a margin of 138 A) without a failure. This shows that the D^2PAK package can withstand a safely rated maximum continuous current of 177 A.

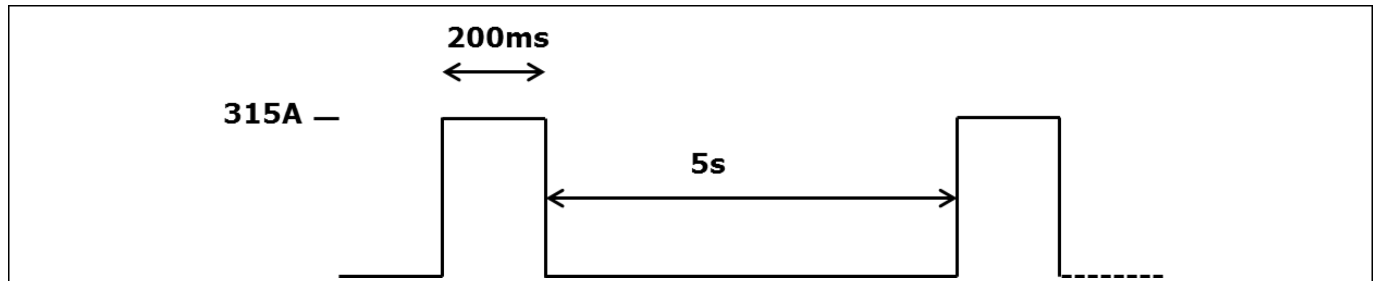


Figure 7 Current profile during bench testing – due to the small duty cycle, the board temperature can be kept at the standardized temperature

4 Case study

In previous chapters we considered the case in which the heatsink (a copper plate in our test) of a MOSFET is kept at a constant temperature of 25°C. This is required to have a standardized comparison to other MOSFETs but does not necessarily apply to a real application.

In a real application (see Figure 8) MOSFETs are placed on a PCB, which cannot be kept at a constant temperature due to practical cooling limitations. Even if the heatsink is kept at constant temperature, there is still a dielectric layer, which presents a thermally resistive interface between the MOSFET's leadframe and the heatsink. This dielectric layer constitutes ~90% of the thermal resistance between the MOSFET junction and the heatsink. Consequently, the current that can be applied without exceeding $T_{j,max}$ is lower and depends greatly on the thermal resistance of the dielectric layer.

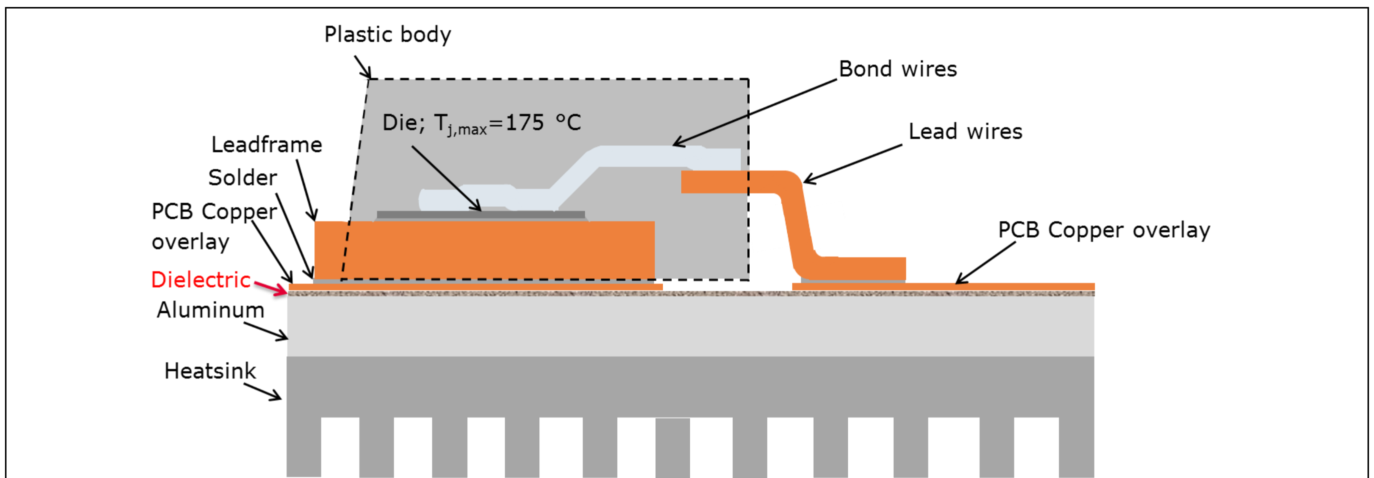


Figure 8 Stacked elements of a MOSFET mounted on an Insulated Metal Substrate (IMS) PCB

Table 1 Typical thickness and thermal conductivity of a thermal network on the IMS PCB

Layer	Thickness	Thermal conductivity
Copper leadframe thickness	~1.3 mm	~400 W/mK
Solder	~50 µm	~60 W/mK
PCB copper overlay	35–105 µm (1–3 Oz)	~400 W/mK
Dielectric	**75–120 µm**	**~2 W/mK**
Aluminum PCB substrate	1–2 mm	~200 W/mK
Aluminum heatsink	1–3 cm	~200 W/mK

From the information in Table 1 we can clearly see the impact of dielectric layer on the overall thermal network. Due to its very low thermal conductivity, compared to aluminum and copper, the thermal conductivity and the thickness of the dielectric layer is a determining factor in how much power can be dissipated in the MOSFET, i.e. what is the maximum current that can be applied in the system. This means that the MOSFET is likely not limited by the $I_{D,max}$ specified in the datasheet, but rather is thermally limited by the PCB.

Let us take a look at a simplified calculation example of the thermal system in a case study, without having to employ an extensive thermal simulation:

Example 1: Calculate the maximum applicable sinusoidal drain current of IPB017N08N5 (D^2PAK), thereby keeping the junction temperature at $T_{j,max}$ = 175°C.

Solution:

Package: D^2PAK – drain tab dimensions 7.5 mm × 8 mm → $A = 60\text{mm}^2$ (presents the heat dissipation area to the PCB)

IMS PCB dielectric layer – λ = 2 W/m-K; d = 120 µm

λ – thermal conductivity of the material in [W/m-K]

d – thickness of the dielectric layer in [m]

$$Rth_{dielectric} = \frac{d}{\lambda * A} = \frac{120\mu m}{2\frac{W}{mK} * 60mm^2} = 1\frac{K}{W}$$

Thermal junction-to-case resistance for IPB017N08N5 is:

$$Rth_{jc,max} = 0.4\frac{K}{W}$$

So, the thermal resistance from the junction to heatsink is:

$$Rth_{JS} = Rth_{dielectric} + Rth_{jc,max} = 1\frac{K}{W} + 0.4\frac{K}{W} = 1.4\frac{K}{W}$$

This results means that for each Watt dissipated in the MOSFET, the die junction temperature will increase by 1.4°C.

Since the conduction power loss in the MOSFET is defined as $P_d = I_D^2 * R_{DS(ON)}$, we could calculate the value of the maximum allowable I_D current; however, first there are several factors we need to consider in the real application:

- The PCB temperature presents a starting temperature for the MOSFET.
- The current in case of motor drive application is sinusoidal in shape, and in case of very low frequencies (less than 1 Hz at the motor start) the peak current is more relevant than the RMS current because its duration can be longer than 100 ms. Why 100 ms?

  By looking at the maximum transient thermal impedance from the datasheet ~100 ms is the timescale at which the MOSFET is thermally saturated. This means that the RMS current should be multiplied by $\sqrt{2}$ to get the peak current.
- Switching losses should also be considered in power loss calculations. Here in this example we will assume 30 percent switching loss.
- $R_{DS(on)}$ increases with temperature. Here in this example we will assume a value $R_{DS(on),max@175°C}$ = 3.2 mΩ for IPB017N08N5.

From the statements above we can now perform a more realistic calculation:

T_{PCB} = 100°C
$T_{j,max}$ = 175°C } $\Delta T = 75°C$
$Rth_{j\text{-}S}$ = 1.4 K/W

$R_{DS(on),max@175°C}$ = 3.2 mΩ

The maximum allowable power dissipation P_d of the MOSFET:

$$P_d = \frac{\Delta T}{Rth_{JS}} = \frac{75°C}{1.4K/W} = 53.5W$$

Now we have to calculate a drain current, which will result in this power dissipation:

$P_d = P_{cond} + P_{sw} \rightarrow P_d = P_{cond} + 0.3 * P_d \rightarrow P_d = I_D^2 * R_{DS(ON)} + 0.3 * P_d \rightarrow$
$53.5W = I_D^2 * 3.2m\Omega + 0.3 * 53.5W \rightarrow \boldsymbol{I_D = 108A_{Peak}\ or\ I_D = \frac{108A}{\sqrt{2}} = 76A_{RMS}}$ **for a sinusoidal current**

From this simplified example with rough calculations we can see that even if the MOSFET is able to conduct 177 A on a datasheet level, in the application the maximum RMS current that can be safely applied is 76 A.

This calculation can provide a good estimation of the thermal capability of the system. More precise results can be obtained by running a thermal simulation, taking into account more details of the thermal management.

5 Conclusion

In the previous datasheet specification of maximum drain current, Infineon was using a conservative approach with a large margin.

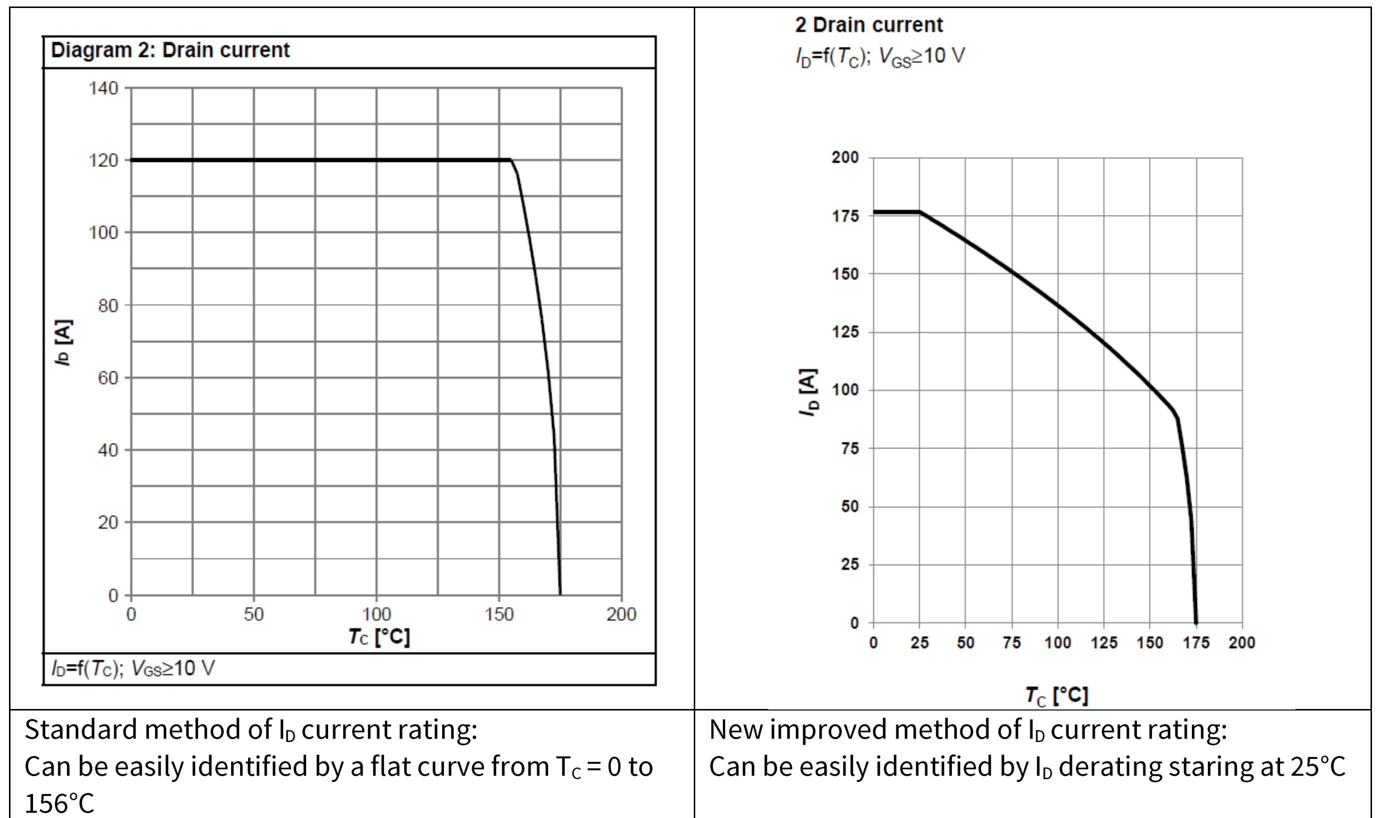
Due to improvements in cooling techniques (IMS PCB) and the development of very low on-state resistance products, Infineon proposes a more sophisticated approach to determine product current ratings, taking into account both the chip and the package properties. The new approach uses standardized boundary conditions for the calculation of nominal product current, and also provides the necessary deratings. Derating diagrams are given in the product datasheet.

Bench tests have shown that devices can even withstand significantly higher currents, demonstrating that the applied assumptions provide sufficient margins.

The new approach is applied to a selection of existing and new datasheets.

Appendix 1 – How to identify whether a datasheet was created according to the new method

In order to avoid confusion on whether a datasheet was created under the new method of current rating, Figure 9 (Diagram 2 of the datasheet) can be used.



Standard method of I_D current rating: Can be easily identified by a flat curve from T_C = 0 to 156°C	New improved method of I_D current rating: Can be easily identified by I_D derating staring at 25°C

Figure 9 Drain current derating – the new method will always have derating starting at 25°C

6 References

[1] Linear Mode Operation and Safe Operating Diagram of Power MOSFETs – J. Schoiswohl

Revision history

Document version	Date of release	Description of changes

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