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MB91F527R/MB91F527U/MB91F527M/MB91F527Y MB91F528R/MB91F528U/MB91F528M/MB91F528Y

32-bit FR81S Microcontroller

The MB91520 series is a Cypress 32-bit microcontroller designed for automotive devices. This series contains the FR81S CPU which is compatible with the FR family.

Note: This series is a composition of the end of the above-mentioned each name of articles of presence, According to Presence of sub-clock, CSV initial value and LVD initial value. Please see "ORDERING INFORMATION" for details.

Features

FR81S CPU Core

- 32-bit RISC, load/store architecture, 5-stage pipeline
- Maximum operating frequency:
 - MB91F52xR/MB91F52xU(LQS144/LQN144/LQP176): 80 MHz (Source oscillation = 4.0 MHz and 20 multiplied (PLL clock multiplication system))
 - MB91F52xR/MB91F52xU(LES144/LEP176): 128 MHz (Source oscillation = 4.0 MHz and 32 multiplied (PLL clock multiplication system))
 - MB91F52xM/ MB91F52xY: 128 MHz (Source oscillation = 4.0 MHz and 32 multiplied (PLL clock multiplication system))
- General-purpose register : 32-bit × 16 sets
- 16-bit fixed length instructions (basic instruction), 1 instruction per cycle
- Instructions appropriate to embedded applications
 - Memory-to-memory transfer instruction
 - Bit processing instruction
 - Barrel shift instruction etc.
- High-level language support instructions
 - Function entry/exit instructions
 - Register content multi-load and store instructions
- Bit search instructions
 - Logical 1 detection, 0 detection, and change-point detection
- Branch instructions with delay slot
 - Decrease overhead during branch process
- Register interlock function
 - Easy assembler writing
- Built-in multiplier and instruction level support
 - Signed 32-bit multiplication : 5 cycles
 - Signed 16-bit multiplication : 3 cycles
- Interrupt (PC/PS saving)
 - 6 cycles (16 priority levels)
- The Harvard architecture allows simultaneous execution of program and data access.
- Instruction compatibility with the FR family
- Built-in memory protection function (MPU)
 - Eight protection areas can be specified commonly for instructions and the data.
 - Control access privilege in both privilege mode and user mode.
- Built-in FPU (floating point arithmetic)

- IEEE754 compliant
- Floating-point register 32-bit × 16 sets

Peripheral Functions

- Clock generation (equipped with SSCG function)
- Main oscillation (4MHz to 16MHz)
 - Sub oscillation (32kHz) or no sub oscillation
 - PLL multiplication rate
 - : 1 to 20 times for MB91F52xR/MB91F52xU (LQS144/LQN144/LQP176)
 - : 1 to 32 times for MB91F52xR/MB91F52xU (LES144/LEP176)
 - : 1 to 32 times for MB91F52xM/MB91F52xY
- 100 kHz CR oscillator mounted
- Maximum operating frequency:
- Peripheral bus clock: 40MHz
- External bus clock: 40MHz
- Built-in Program flash capacity
- MB91F527 : 1536KB + 64KB
- MB91F528 : 2048KB + 64KB
- Built-in Data flash (WorkFlash) 64KB
- Built-in RAM capacity
 - Main RAM
 - MB91F527 : 192KB
 - MB91F528 : 192KB + 128KB (128KB located in the AHB area, a penalty given at access)
 - Backup RAM 16KB
- General-purpose ports :
 - MB91F527R/MB91F528R : 115 (none sub oscillation), 113 (with sub oscillation)
 - MB91F527U/MB91F528U : 147 (none sub oscillation), 145 (with sub oscillation)
 - MB91F527M/MB91F528M : 177 (none sub oscillation), 175 (with sub oscillation)
 - MB91F527Y/MB91F528Y 219 (none sub oscillation), 217 (with sub oscillation)
 - Included I²C pseudo open drain ports : Max. 30
- External bus interface
 - 22-bit address, 8/16-bit data
- DMA Controller
 - Up to 16 channels can be started simultaneously.

- 2 transfer factors (Internal peripheral request and software)
- A/D converter (successive approximation type)
 - 12-bit resolution : Max. 64 channels (32 channels +32 channels)
 - Conversion time : 1.4μs
- D/A converter (R-2R type)
 - 8-bit resolution : 2 channels
- External interrupt input: Max. 24 channels
 - Level ("H" / "L"), or edge detection (rising or falling) supported
- Multi-function serial communication (built-in transmission/reception FIFO memory) : Max. 20 channels 5V tolerant input 8 channels (ch.6, ch.8, ch.9, ch.11, ch.16 to ch.19) CMOS hysteresis input
 - < UART (Asynchronous serial interface) >
 - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
 - Parity or no parity is selectable.
 - Built-in dedicated baud rate generator
 - The external clock can be used as the transfer clock
 - Parity, frame, and overrun error detect functions provided
 - DMA transfer support
 - < CSIO (Synchronous serial interface) >
 - Full-duplex double buffering system, 64-byte transmission FIFO, memory, 64-byte reception FIFO memory
 - SPI supported; master and slave systems supported; 5-bit to 16-bit, 20-bit, 24-bit, 32-bit data length can be set.
 - Built-in dedicated baud rate generator (Master operation)
 - The external clock can be entered. (Slave operation)
 - Overrun error detection function is provided
 - DMA transfer support
 - Serial chip select SPI function
 - < LIN (Asynchronous Serial Interface for LIN) >
 - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
 - LIN protocol revision 2.1 supported
 - Master and slave systems supported
 - Framing error and overrun error detection
 - LIN synch break generation and detection; LIN synch delimiter generation
 - Built-in dedicated baud rate generator
 - The external clock can be adjusted by the reload counter
 - DMA transfer support
 - Hardware assist function
 - < I2C >
 - 10 channels (ch.3, ch.4, ch.12 to ch.19) Standard mode / Fast mode supported
 - 5 channels (ch.5 to ch.8, ch.11) Standard mode supported
 - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
 - Standard mode (Max. 100kbps) / Fast mode (Max. 400kbps) supported
 - DMA transfer supported (for transmission only)
- CAN : 6 channels
 - Transfer speed : Up to 1Mbps
 - 128-transmission/reception message buffering : 6 channels
- FlexRay controller: 1 unit (ch.A/ch.B)
- FlexRay specification version 2.1 supported
 - Max. 128-message buffer configuration
 - 8KB message RAM
 - Variable-length message buffer configuration
 - Each message buffer can be configured as a part of a reception buffer, transmission buffer, or reception FIFO.
 - Host access to message buffers through input and output buffers
 - Filtering the slot counter, cycle counter, and channels
 - Maskable interrupts
- PPG : 16-bit × Max. 88 channels
 - LED drive output 4 channels (ch.11 to ch.14)
- Reload timer : 16-bit × 8 channels
- Free-run timer :
 - 16-bit × 3 channels
 - 32-bit × Max. 8 channels
- Input capture :
 - 16-bit × 4 channels (linked to the free-run timer)
 - 32-bit × Max. 8 channels (linked to the free-run timer)
- Output compare :
 - 16-bit × 6 channels (linked to the free-run timer)
 - 32-bit × Max. 8 channels (linked to the free-run timer)
- Wave generator : 6 channels
- U/D counter:
 - 8/16-bit up/down counter × Max. 4 channels
- Real-time clock (RTC) (for day, hours, minutes, seconds)
 - Main oscillation / sub oscillation frequency can be selected for the operation clock.
- Calibration: A real-time clock (RTC) of the sub clock drive.
 - The main clock to sub clock ratio can be corrected by setting the real-time clock prescaler
- Clock Supervisor
 - Monitoring abnormality (damage of crystal etc.) of sub oscillation (32kHz) (dual clock products) and main oscillation (4 MHz).
 - When abnormality is detected, it switches to the CR clock.
- For some devices, ON/OFF can be selected as the initial value.
- Base timer : 2 channels
 - 16-bit timer
 - The timer mode is selected from PWM/PPG/PWC/reload.
 - In the cascaded mode, a pair of 16-bit timers can be used as one 32-bit timer.
- CRC generation
- Watchdog timer
 - Hardware watchdog
 - Software watchdog (An effective range of a clear counter can be set.)
- NMI

- Interrupt controller
- Interrupt request batch read
 - Multiple interrupts from peripherals can be read by a series of registers.
- I/O relocation
- Peripheral function pins can be reassigned.
- Low-power consumption mode
 - Sleep / Stop / Watch / Sub RUN mode
 - Stop (power shutdown) / Watch (power shutdown) mode
- Power on reset
- Low-voltage detection reset (External power supply and Internal power supply are independently observed.)
- For some devices, ON/OFF can be selected as the initial value for external power supply.
- Tuning RAM
- Capacity: 128 KB
- Can be used as RAM for data tuning.
- JTAG pins (TRST, TCK, TMS, TDI, TDO)
- Device Package : 144/176/208/416
- CMOS 90nm Technology
- Power supplies
 - 5V or 3V Power supply
 - The internal 1.2V is generated from 5V with the voltage step-down regulator.
 - Restriction on the power-on sequence (from VCC to VCCE)
 - Applying a voltage higher than the power supply voltage to an analog signal input is prohibited.
- Operation guaranteed voltage range (recommended): 3.0V to 5.5V (within the range guaranteed by AC and DC spec)
- Operation guaranteed voltage range: 2.7V to 5.5V

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1. Product Lineup

Product lineup comparison 144 pins

	MB91F527R	MB91F528R
System Clock	On-chip PLL Clock multiple method	
Minimum instruction execution time	12.5ns(80MHz) (LQS144/LQN144) 8.0ns(128MHz) (LES144)	
FLASH Capacity (Program)	1536KB + 64KB	2048KB + 64KB
FLASH Capacity (Data)	64KB	
RAM Capacity	192KB + 16KB	(192KB + 128KB) + 16KB
External Bus I/F (22 address/16 data/4cs)	Yes	
DMA Transfer	16 channels	
16-bit Base Timer	2 channels	
Free-run Timer	16-bit × 3 channels, 32-bit × 3 channels	
Input capture	16-bit × 4 channels, 32-bit × 6 channels	
Output Compare	16-bit × 6 channels, 32-bit × 6 channels	
16-bit Reload Timer	8 channels	
PPG	16-bit × 44 channels ^{*2}	
Up/down Counter	2 channels	
Clock Supervisor	Yes	
External interrupt	8 channels × 2 units	
A/D	12-bit × 32 channels (1 unit), 12-bit × 16 channels (1 unit)	
D/A (8-bit)	2 channels	
Multi-Function Serial	12 channels ^{*3}	
CAN	128msg × 6 channels	
FlexRay	1 channel	
Hardware watchdog	Yes	
CRC generation	Yes	
Low-voltage detection reset	Yes	

	MB91F527R	MB91F528R
Flash Security	Yes	
ECC Flash/WorkFlash	Yes	
ECC RAM	Yes	
Memory Protection Function (MPU)	Yes	
Floating-point arithmetic (FPU)	Yes	
Real Time Clock (RTC)	Yes	
General-purpose port (#GPIOs)	115 ports (no sub clock) / 113 ports (with sub clock)	
SSCG	Yes	
Sub clock	Yes	
CR oscillator	Yes	
NMI request function	Yes	
OCD (On Chip Debug)	Yes	
TPU (Timing Protection Unit)	Yes	
Key Code Register	Yes	
Wave Generator	6 channels	
Tuning RAM	None	Yes
JTAG	Yes	
Operation guaranteed temperature (Ta)	-40°C to +125°C *1	
Power supply	2.7 V to 5.5 V *4 VCCE = 5.0 V±10% or VCCE = 3.0 V to 3.6 V (VCCE: 1-pin to 39-pin and 128-pin to 144-pin power supply) (External bus I/F: 3.0 V to 3.6 V)	
Package	LQS144 / LQN144 / LES144	

*1: The limitation with the package has been described by the item of the power consumption of "Absolute maximum ratings".

*2: PPG output pins on ch.38 and ch.39 do not exist. See "Pins of PPG (ch.0 to ch.87)."

*3: Only channel 3 and channel 4 support the I²C (fast mode/standard mode).

Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I²C (standard mode).

*4: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V).

This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.

Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Product lineup comparison 176 pins

	MB91F527U	MB91F528U
System Clock	On-chip PLL Clock multiple method	
Minimum instruction execution time	12.5ns(80MHz) (LQP176) 8.0ns(128MHz) (LEP176)	
FLASH Capacity (Program)	1536KB + 64KB	2048KB + 64KB
FLASH Capacity (Data)	64KB	
RAM Capacity	192KB + 16KB	(192KB + 128KB) + 16KB
External Bus I/F (22 address/16 data/4cs)	Yes	
DMA Transfer	16 channels	
16-bit Base Timer	2 channels	
Free-run Timer	16-bit × 3 channels, 32-bit × 3 channels	
Input capture	16-bit × 4 channels, 32-bit × 6 channels	
Output Compare	16-bit × 6 channels, 32-bit × 6 channels	
16-bit Reload Timer	8 channels	
PPG	16-bit × 48 channels	
Up/down Counter	2 channels	
Clock Supervisor	Yes	
External interrupt	8 channels × 2 units	
A/D	12-bit × 32 channels (1 unit), 12-bit × 16 channels (1 unit)	
D/A (8-bit)	2 channels	
Multi-Function Serial	12 channels *2	
CAN	128msg × 6 channels	
FlexRay	1 channel	
Hardware watchdog	Yes	
CRC generation	Yes	
Low-voltage detection reset	Yes	

	MB91F527U	MB91F528U
Flash Security	Yes	
ECC Flash/WorkFlash	Yes	
ECC RAM	Yes	
Memory Protection Function (MPU)	Yes	
Floating-point arithmetic (FPU)	Yes	
Real Time Clock (RTC)	Yes	
General-purpose port (#GPIOs)	147 ports (no sub clock) / 145 ports (with sub clock)	
SSCG	Yes	
Sub clock	Yes	
CR oscillator	Yes	
NMI request function	Yes	
OCD (On Chip Debug)	Yes	
TPU (Timing Protection Unit)	Yes	
Key Code Register	Yes	
Wave Generator	6 channels	
Tuning RAM	None	Yes
JTAG	Yes	
Operation guaranteed temperature (Ta)	-40°C to +125°C *1	
Power supply	2.7 V to 5.5 V *3 VCCE = 5.0 V±10% or VCCE = 3.0 V to 3.6 V (VCCE: 1-pin to 49-pin and 156-pin to 176-pin power supply) (External bus I/F: 3.0 V to 3.6 V)	
Package	LQP176 / LEP176	

*1: The limitation with the package has been described by the item of the power consumption of "Absolute maximum ratings".

*2: Only channel 3 and channel 4 support the I²C (high-speed mode/standard mode).

Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I²C (standard mode).

*3: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.

Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Product lineup comparison 208 pins

	MB91F527M	MB91F528M
System Clock	On-chip PLL Clock multiple method	
Minimum instruction execution time	8.0ns (128MHz)	
FLASH Capacity (Program)	1536KB + 64KB	2048KB + 64KB
FLASH Capacity (Data)	64KB	
RAM Capacity	192KB + 16KB	(192KB + 128KB) + 16KB
External Bus I/F (22 address/16 data/4cs)	Yes	
DMA Transfer	16 channels	
16-bit Base Timer	2 channels	
Free-run Timer	16-bit × 3 channels, 32-bit × 8 channels	
Input capture	16-bit × 4 channels, 32-bit × 8 channels	
Output Compare	16-bit × 6 channels, 32-bit × 8 channels	
16-bit Reload Timer	8 channels	
PPG	16-bit × 64 channels	
Up/down Counter	4 channels	
Clock Supervisor	Yes	
External interrupt	8 channels × 3 units	
A/D	12-bit × 32 channels (2 units)	
D/A (8-bit)	2 channels	
Multi-Function Serial	20 channels *2	
CAN	128msg × 6 channels	
FlexRay	1 channel	
Hardware watchdog	Yes	
CRC generation	Yes	
Low-voltage detection reset	Yes	

	MB91F527M	MB91F528M
Flash Security	Yes	
ECC Flash/WorkFlash	Yes	
ECC RAM	Yes	
Memory Protection Function (MPU)	Yes	
Floating-point arithmetic (FPU)	Yes	
Real Time Clock (RTC)	Yes	
General-purpose port (#GPIOs)	177 ports (no sub clock) / 175 ports (with sub clock)	
SSCG	Yes	
Sub clock	Yes	
CR oscillator	Yes	
NMI request function	Yes	
OCD(On Chip Debug)	Yes	
TPU (Timing Protection Unit)	Yes	
Key Code Register	Yes	
Wave Generator	6 channels	
Tuning RAM	None	Yes
JTAG	Yes	
Operation guaranteed temperature (Ta)	-40°C to +125°C *1	
Power supply	2.7 V to 5.5 V *3 VCCE = 5.0 V±10% or VCCE = 3.0 V to 3.6 V (VCCE: 1-pin to 57-pin and 188-pin to 208-pin power supply) (External bus I/F: 3.0 V to 3.6 V)	
Package	LQR208 / LER208	

*1: The limitation with the package has been described by the item of the power consumption of "Absolute maximum ratings".

*2: Only channel 3, channel 4 and channel 12 to channel 19 support the I²C (high-speed mode/standard mode).

Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I²C (standard mode)

*3: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V).

This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.

Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Product lineup comparison 416 pins

	MB91F527Y	MB91F528Y
System Clock	On-chip PLL Clock multiple method	
Minimum instruction execution time	8.0ns (128MHz)	
FLASH Capacity (Program)	1536KB + 64KB	2048KB + 64KB
FLASH Capacity (Data)	64KB	
RAM Capacity	192KB + 16KB	(192KB + 128KB) + 16KB
External Bus I/F (22 address/16 data/4cs)	Yes	
DMA Transfer	16 channels	
16-bit Base Timer	2 channels	
Free-run Timer	16-bit × 3 channels, 32-bit × 8 channels	
Input capture	16-bit × 4 channels, 32-bit × 8 channels	
Output Compare	16-bit × 6 channels, 32-bit × 8 channels	
16-bit Reload Timer	8 channels	
PPG	16-bit × 88 channels	
Up/down Counter	4 channels	
Clock Supervisor	Yes	
External interrupt	8 channels × 3 units	
A/D	12-bit × 32 channels (2 units)	
D/A (8-bit)	2 channels	
Multi-Function Serial	20 channels *1	
CAN	128msg × 6 channels	
FlexRay	1 channel	
Hardware watchdog	Yes	
CRC generation	Yes	
Low-voltage detection reset	Yes	
Flash Security	Yes	
ECC Flash/WorkFlash	Yes	

	MB91F527Y	MB91F528Y
ECC RAM	Yes	
Memory Protection Function (MPU)	Yes	
Floating-point arithmetic (FPU)	Yes	
Real Time Clock (RTC)	Yes	
General-purpose port (#GPIOs)	219 ports (no sub clock) / 217 ports (with sub clock)	
SSCG	Yes	
Sub clock	Yes	
CR oscillator	Yes	
NMI request function	Yes	
OCD(On Chip Debug)	Yes	
TPU (Timing Protection Unit)	Yes	
Key Code Register	Yes	
Wave Generator	6 channels	
Tuning RAM	None	Yes
JTAG	Yes	
Operation guaranteed temperature (Ta)	-40°C to +125°C	
Power supply	2.7 V to 5.5 V ^{*2} VCCE = 5.0 V±10% or VCCE = 3.0 V to 3.6 V (VCCE: See pin assignment) (External bus I/F: 3.0 V to 3.6 V)	
Package	PAB416	

*1: Only channel 3, channel 4 and channel 12 to channel 19 support the I²C (high-speed mode/standard mode).
Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I²C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V).

This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.

Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

Table for Clock Supervisor and External Low Voltage Detection Reset Initial Value ON/OFF

Clock	Initial value of clock supervisor	Initial value of external low-voltage detection reset	Function
Single	ON	ON	S
		OFF	U
	OFF	ON	H
		OFF	K
Dual	ON	ON	W
		OFF	Y
	OFF	ON	J
		OFF	L

MB91F52Xxyz

- Revision: C, D, E
- Function: See Table 3-5
- PKG Type: R 144 pin
U 176 pin
M 208 pin
Y PAB 416 pin
- Memory Size: 7 1.5MB
8 2MB

2. Pin Assignment

MB91F52xR

MB91F527R, MB91F528R

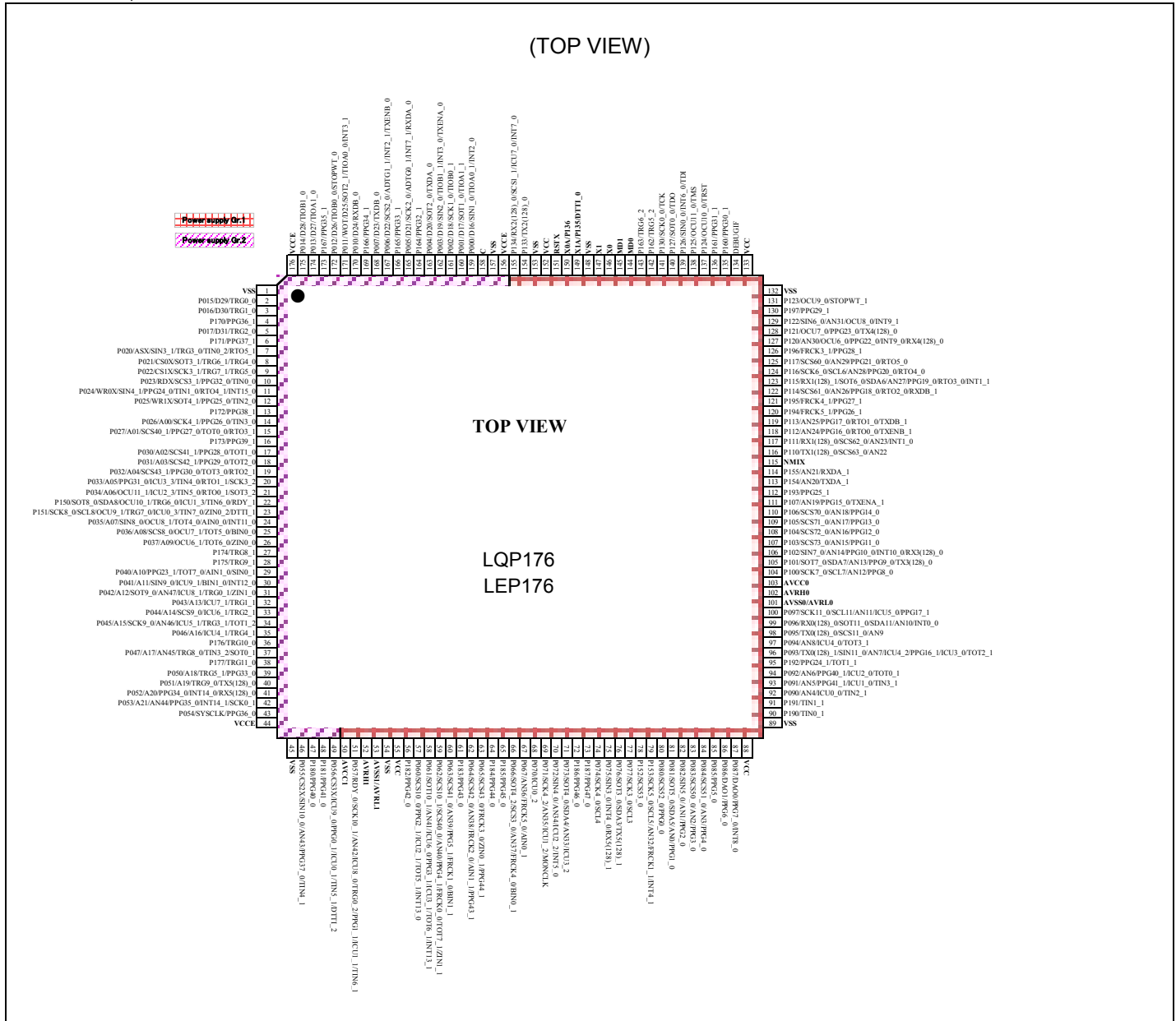
(TOP VIEW)

TOP VIEW

LQS144/LQN144
LES144

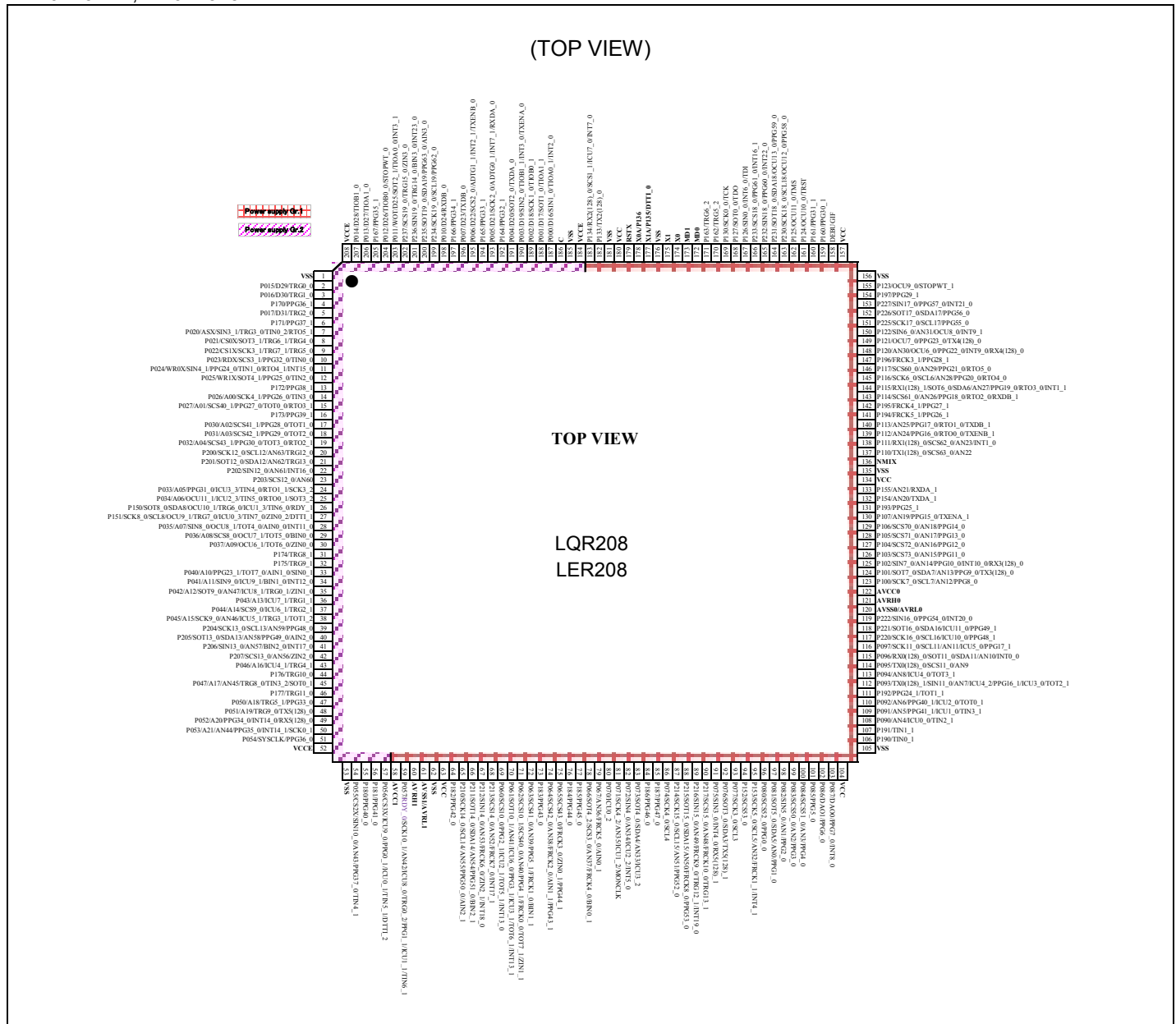
MB91F52xU

MB91F527U, MB91F528U



MB91F52xM

MB91F527M, MB91F528M



MB91F52xY

MB91F527Y, MB91F528Y

Top view

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26						
A	VSS B 1	VSS B 100	VCCE B 99	P014 B 98	P012 B 97	P010 B 96	P006 B 95	P004 B 94	P002 B 93	P000 B 92	VCCE B 91	VSS B 90	C B 89	VCC B 88	VSS B 87	P136 B 86	P135 B 85	VSS B 84	X1 B 83	X0 B 82	VSS B 81	P125 B 80	MD1 B 79	VCC B 78	VSS B 77	VSS B 76	A					
B	VSS B 2	VSS B 101	VCCE B 102	VSS B 191	P013 B 190	P011 B 189	P007 B 188	P005 B 187	P003 B 186	P001 B 185	VCCE B 184	VSS B 183	VSS B 182	VCC B 181	RSTX B 180	VSS B 179	VSS B 178	P291 B 177	VSS B 176	VSS B 175	P230 B 174	P286 B 173	MD0 B 172	VCC B 171	VSS B 170	VSS B 75	B					
C	P015 B 3	VSS B 102	VSS B 193	P296 B 276	P295 B 275	P294 B 274	VSS B 273	VSS B 272	P234 B 271	P293 B 270	P165 B 269	VSS B 268	VSS B 267	VSS B 266	VSS B 265	P162 B 264	P127 B 263	P126 B 262	P233 B 261	P231 B 260	P287 B 259	P160 B 258	VSS B 257	VSS B 256	P284 B 169	DEBUGF B 74	C					
D	P016 B 4	P017 B 103	P240 B 194	VSS B 277	P297 B 352	P167 B 351	P237 B 350	P236 B 349	P235 B 348	P166 B 347	P292 B 346	P164 B 345	VSS B 344	P134 B 343	P133 B 342	P163 B 341	P130 B 340	P290 B 339	P232 B 338	P124 B 337	P161 B 336	P285 B 335	VSS B 334	VSS B 255	P226 B 168	P121 B 73	D					
E	P020 B 5	P021 B 104	P170 B 195	P241 B 278	Index																		P123 B 333	P227 B 254	P122 B 167	P282 B 72	E					
F	P022 B 6	P023 B 105	VSS B 196	P171 B 279			Power supply Gr.2											Power supply Gr.1										P197 B 332	VSS B 253	P283 B 166	P115 B 71	F
G	P024 B 7	P025 B 106	VSS B 197	P242 B 280																			P225 B 331	VSS B 252	P116 B 165	P280 B 70	G					
H	P026 B 8	VSS B 107	VSS B 198	P243 B 281																			P120 B 330	P117 B 251	P281 B 164	P194 B 69	H					
J	P027 B 9	P030 B 108	P244 B 199	P245 B 282																			P196 B 329	VSS B 250	P195 B 163	P111 B 68	J					
K	P031 B 10	P032 B 109	P172 B 200	P173 B 283								VSS B 353	VSS B 380	VSS B 379	VSS B 378	VSS B 377	VSS B 376	VSS B 375	VSS B 374					P114 B 328	VSS B 249	P113 B 162	P112 B 67	K				
L	P033 B 11	P034 B 110	P200 B 201	P201 B 284								VSS B 354	VSS B 381	VSS B 400	VSS B 399	VSS B 398	VSS B 397	VSS B 396	VSS B 395					P110 B 327	P277 B 248	NMX B 161	P155 B 66	L				
M	VCCE B 12	VCCE B 111	P202 B 202	P203 B 285								VSS B 355	VSS B 382	VSS B 401	VSS B 412	VSS B 411	VSS B 410	VSS B 395	VSS B 372					VSS B 326	VSS B 247	VSS B 160	VSS B 65	M				
N	VSS B 13	VSS B 112	VSS B 203	VSS B 286								VSS B 356	VSS B 383	VSS B 402	VSS B 413	VSS B 416	VSS B 409	VSS B 394	VSS B 371					P154 B 325	VSS B 246	VCC B 159	VCC B 64	N				
P	VSS B 14	VSS B 113	VSS B 204	VSS B 287								VSS B 357	VSS B 384	VSS B 403	VSS B 414	VSS B 415	VSS B 408	VSS B 393	VSS B 370					P107 B 324	P106 B 245	P105 B 158	P193 B 63	P				
R	P035 B 15	P036 B 114	P150 B 205	P151 B 288								VSS B 358	VSS B 385	VSS B 404	VSS B 405	VSS B 406	VSS B 407	VSS B 392	VSS B 369					P104 B 323	VSS B 244	P103 B 157	P102 B 62	R				
T	P037 B 16	P040 B 115	VSS B 206	P174 B 289								VSS B 359	VSS B 386	VSS B 387	VSS B 388	VSS B 389	VSS B 390	VSS B 391	VSS B 368					P101 B 322	VSS B 243	P100 B 156	AVCC0 B 61	T				
U	P041 B 17	P042 B 116	VSS B 207	P175 B 290								VSS B 360	VSS B 361	VSS B 362	VSS B 363	VSS B 364	VSS B 365	VSS B 366	VSS B 367					P221 B 321	P275 B 242	P276 B 155	AVRH0 B 60	U				
V	P043 B 18	P044 B 117	P204 B 208	P205 B 291																				P096 B 320	VSS B 241	P222 B 154	AVRL0 B 59	V				
W	P045 B 19	P046 B 118	VSS B 209	P206 B 292																				P093 B 319	VSS B 240	P220 B 153	AVSS0 B 58	W				
Y	P047 B 20	P050 B 119	VSS B 210	P207 B 293																				P092 B 318	P273 B 239	P095 B 152	P097 B 57	Y				
AA	P051 B 21	P052 B 120	P176 B 211	P177 B 294																				P270 B 317	VSS B 238	P272 B 151	P094 B 56	AA				
AB	P053 B 22	P054 B 121	P250 B 212	P251 B 295																				P267 B 316	P090 B 237	P091 B 150	P192 B 55	AB				
AC	P252 B 23	P253 B 122	VSS B 213	VSS B 296	P180 B 297	P181 B 298	P182 B 299	P211 B 300	VSS B 301	P061 B 302	P063 B 303	P065 B 304	P066 B 305	P072 B 306	P263 B 307	P074 B 308	P265 B 309	P080 B 310	P082 B 311	TCK B 312	P083 B 313	P086 B 314	VSS B 315	P266 B 236	P191 B 149	P271 B 54	AC					
AD	VCCE B 24	VCCE B 123	VSS B 214	VSS B 215	P255 B 216	P256 B 217	VSS B 218	P213 B 219	VSS B 220	VSS B 221	P062 B 222	VSS B 223	VSS B 224	P071 B 225	VSS B 226	VSS B 227	VSS B 228	VSS B 229	VSS B 230	TDI B 231	VSS B 232	VSS B 233	P085 B 234	VSS B 235	P087 B 148	P190 B 53	AD					
AE	VSS B 25	VSS B 124	P056 B 125	P254 B 126	P057 B 127	P210 B 128	P212 B 129	P060 B 130	VSS B 131	VSS B 132	VCC B 133	P064 B 134	P185 B 135	P070 B 136	P262 B 137	P187 B 138	P216 B 139	P075 B 140	P264 B 141	P153 B 142	TDO B 143	TRST B 144	TMS B 145	VCC B 146	VSS B 147	VSS B 52	AE					
AF	VSS B 26	VSS B 27	P055 B 28	AVCC1 B 29	AVRH1 B 30	AVRL1 B 31	AVSS1 B 32	VSS B 33	VSS B 34	VCC B 35	VCC B 36	P183 B 37	P184 B 38	P067 B 39	P073 B 40	P186 B 41	P215 B 42	P214 B 43	P217 B 44	P077 B 45	P152 B 46	P081 B 47	P084 B 48	VCC B 49	VSS B 50	VSS B 51	AF					
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26						

PAB416

3. Pin Description

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
-	-	-	D3	P240	-	A	General-purpose I/O port
-	-	-	E4	P241	-	A	General-purpose I/O port
2	2	2	C1	P015	-	R	General-purpose I/O port
				D29	-		External Bus data bit29 I/O pin
				TRG0_0	-		PPG trigger 0 input pin(0)
3	3	3	D1	P016	-	R	General-purpose I/O port
				D30	-		External Bus data bit30 I/O pin
				TRG1_0	-		PPG trigger 1 input pin(0)
-	4	4	E3	P170	-	A	General-purpose I/O port
				PPG36_1	-		PPG ch.36 output pin(1)
4	5	5	D2	P017	-	R	General-purpose I/O port
				D31	-		External Bus data bit31 I/O pin
				TRG2_0	-		PPG trigger 2 input pin(0)
-	6	6	F4	P171	-	A	General-purpose I/O port
				PPG37_1	-		PPG ch.37 output pin(1)
-	-	-	G4	P242	-	A	General-purpose I/O port
				TRG16_0	-		PPG trigger 16 input pin(0)
-	-	-	H4	P243	-	A	General-purpose I/O port
				TRG17_0	-		PPG trigger 17 input pin(0)
5	7	7	E1	P020	-	F	General-purpose I/O port
				ASX	-		External Bus address strobe output pin
				SIN3_1	-		Multi-function serial ch.3 serial data input pin(1)
				TRG3_0	-		PPG trigger 3 input pin(0)
				TIN0_2	-		Reload timer ch.0 event input pin(2)
				RTO5_1	-		Waveform generator ch.5 output pin(1)
6	8	8	E2	P021	-	A	General-purpose I/O port
				CS0X	-		External Bus chip select 0 output pin
				SOT3_1	-		Multi-function serial ch.3 serial data output pin(1)
				TRG6_1	-		PPG trigger 6 input pin(1)
				TRG4_0	-		PPG trigger 4 input pin(0)
7	9	9	F1	P022	-	F	General-purpose I/O port
				CS1X	-		External Bus chip select 1 output pin
				SCK3_1	-		Multi-function serial ch.3 clock I/O pin(1)
				TRG7_1	-		PPG trigger 7 input pin(1)
				TRG5_0	-		PPG trigger 5 input pin(0)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
8	10	10	F2	P023	-	A	General-purpose I/O port
				RDX	-		External Bus read strobe output pin
				SCS3_1	-		Serial chip select 3 I/O pin(1)
				PPG32_0	-		PPG ch.32 output pin(0)
				TIN0_0	-		Reload timer ch.0 event input pin(0)
-	-	-	J3	P244	-	A	General-purpose I/O port
				PPG64_0	-		PPG ch.64 output pin(0)
-	-	-	J4	P245	-	A	General-purpose I/O port
				PPG65_0	-		PPG ch.65 output pin(0)
9	11	11	G1	P024	-	F	General-purpose I/O port
				WR0X	-		External Bus write strobe 0 output pin
				SIN4_1	-		Multi-function serial ch.4 serial data input pin(1)
				PPG24_0	-		PPG ch.24 output pin(0)
				TIN1_0	-		Reload timer ch.1 event input pin(0)
				RTO4_1	-		Waveform generator ch.4 output pin(1)
				INT15_0	-		INT15 external interrupt input pin(0)
10	12	12	G2	P025	-	A	General-purpose I/O port
				WR1X	-		External Bus write strobe 1 output pin
				SOT4_1	-		Multi-function serial ch.4 serial data output pin(1)
				PPG25_0	-		PPG ch.25 output pin(0)
				TIN2_0	-		Reload timer ch.2 event input pin(0)
-	13	13	K3	P172	-	A	General-purpose I/O port
				PPG38_1	-		PPG ch.38 output pin(1)
11	14	14	H1	P026	-	F	General-purpose I/O port
				A00	-		External Bus address bit0 output pin
				SCK4_1	-		Multi-function serial ch.4 clock I/O pin(1)
				PPG26_0	-		PPG ch.26 output pin(0)
				TIN3_0	-		Reload timer ch.3 event input pin(0)
12	15	15	J1	P027	-	A	General-purpose I/O port
				A01	-		External Bus address bit1 output pin
				SCS40_1	-		Serial chip select 40 I/O pin(1)
				PPG27_0	-		PPG ch.27 output pin(0)
				TOT0_0	-		Reload timer ch.0 output pin(0)
				RTO3_1	-		Waveform generator ch.3 output pin(1)
-	16	16	K4	P173	-	A	General-purpose I/O port
				PPG39_1	-		PPG ch.39 output pin(1)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
13	17	17	J2	P030	-	A	General-purpose I/O port
				A02	-		External Bus address bit2 output pin
				SCS41_1	-		Serial chip select 41 output pin(1)
				PPG28_0	-		PPG ch.28 output pin(0)
				TOT1_0	-		Reload timer ch.1 output pin(0)
14	18	18	K1	P031	-	A	General-purpose I/O port
				A03	-		External Bus address bit3 output pin
				SCS42_1	-		Serial chip select 42 output pin(1)
				PPG29_0	-		PPG ch.29 output pin(0)
				TOT2_0	-		Reload timer ch.2 output pin(0)
15	19	19	K2	P032	-	A	General-purpose I/O port
				A04	-		External Bus address bit4 output pin
				SCS43_1	-		Serial chip select 43 output pin(1)
				PPG30_0	-		PPG ch.30 output pin(0)
				TOT3_0	-		Reload timer ch.3 output pin(0)
				RTO2_1	-		Waveform generator ch.2 output pin(1)
-	-	20	L3	P200	-	Q	General-purpose I/O port
				SCK12_0/SCL12	-		Multi-function serial ch.12 clock I/O pin(0)/ I ² C bus serial clock I/O pin
				AN63	-		ADC analog 63 input pin
				TRG12_0	-		PPG trigger 12 input pin(0)
-	-	21	L4	P201	-	Q	General-purpose I/O port
				SOT12_0/SDA12	-		Multi-function serial ch.12 serial data output pin(0)/I ² C bus serial data I/O pin
				AN62	-		ADC analog 62 input pin
				TRG13_0	-		PPG trigger 13 input pin(0)
-	-	22	M3	P202	-	G	General-purpose I/O port
				SIN12_0	-		Multi-function serial ch.12 serial data input pin(0)
				AN61	-		ADC analog 61 input pin
				INT16_0	-		INT16 external interrupt input pin(0)
-	-	23	M4	P203	-	B	General-purpose I/O port
				SCS12_0	-		Serial chip select 12 I/O pin(0)
				AN60	-		ADC analog 60 input pin

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
16	20	24	L1	P033	-	A	General-purpose I/O port
				A05	-		External Bus address bit5 output pin
				PPG31_0	-		PPG ch.31 output pin(0)
				ICU3_3	-		Input capture ch.3 input pin(3)
				TIN4_0	-		Reload timer ch.4 event input pin(0)
				RTO1_1	-		Waveform generator ch.1 output pin(1)
				SCK3_2	-		Multi-function serial ch.3 clock I/O pin(2)
17	21	25	L2	P034	-	A	General-purpose I/O port
				A06	-		External Bus address bit6 output pin
				OCU11_1	-		Output compare ch.11 output pin(1)
				ICU2_3	-		Input capture ch.2 input pin(3)
				TIN5_0	-		Reload timer ch.5 event input pin(0)
				RTO0_1	-		Waveform generator ch.0 output pin(1)
				SOT3_2	-		Multi-function serial ch.3 serial data output pin(2)
18	22	26	R3	P150	-	F	General-purpose I/O port
				RDY_1	-		External Bus RDY input pin (1)
				SOT8_0/SDA8	-		Multi-function serial ch.8 serial data output pin(0)/I ² C bus serial data I/O pin
				OCU10_1	-		Output compare ch.10 output pin(1)
				TRG6_0	-		PPG trigger 6 input pin(0)
				ICU1_3	-		Input capture ch.1 input pin(3)
				TIN6_0	-		Reload timer ch.6 event input pin(0)
19	23	27	R4	P151	-	F	General-purpose I/O port
				SCK8_0/SCL8	-		Multi-function serial ch.8 clock I/O pin(0)/I ² C bus serial clock I/O pin
				OCU9_1	-		Output compare ch.9 output pin(1)
				TRG7_0	-		PPG trigger 7 input pin(0)
				ICU0_3	-		Input capture ch.0 input pin(3)
				TIN7_0	-		Reload timer ch.7 event input pin(0)
				ZIN0_2	-		U/D counter ch.0 ZIN input pin(2)
				DTTI_1	-		Waveform generator ch.0-ch.5 input pin(1)
20	24	28	R1	P035	-	I	General-purpose I/O port
				A07	-		External Bus address bit7 output pin
				SIN8_0	-		Multi-function serial ch.8 serial data input pin(0)
				OCU8_1	-		Output compare ch.8 output pin(1)
				TOT4_0	-		Reload timer ch.4 output pin(0)
				AIN0_0	-		U/D counter ch.0 AIN input pin(0)
				INT11_0	-		INT11 external interrupt input pin(0)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
21	25	29	R2	P036	-	A	General-purpose I/O port
				A08	-		External Bus address bit8 output pin
				SCS8_0	-		Serial chip select 8 I/O pin(0)
				OCU7_1	-		Output compare ch.7 output pin(1)
				TOT5_0	-		Reload timer ch.5 output pin(0)
				BIN0_0	-		U/D counter ch.0 BIN input pin(0)
22	26	30	T1	P037	-	A	General-purpose I/O port
				A09	-		External Bus address bit9 output pin
				OCU6_1	-		Output compare ch.6 output pin(1)
				TOT6_0	-		Reload timer ch.6 output pin(0)
				ZIN0_0	-		U/D counter ch.0 ZIN input pin(0)
-	27	31	T4	P174	-	A	General-purpose I/O port
				TRG8_1	-		PPG trigger 8 input pin(1)
-	28	32	U4	P175	-	A	General-purpose I/O port
				TRG9_1	-		PPG trigger 9 input pin(1)
23	29	33	T2	P040	-	A	General-purpose I/O port
				A10	-		External Bus address bit10 output pin
				PPG23_1	-		PPG ch.23 output pin(1)
				TOT7_0	-		Reload timer ch.7 output pin(0)
				AIN1_0	-		U/D counter ch.1 AIN input pin(0)
				SIN0_1	-		Multi-function serial ch.0 serial data input pin(1)
24	30	34	U1	P041	-	I	General-purpose I/O port
				A11	-		External Bus address bit11 output pin
				SIN9_0	-		Multi-function serial ch.9 serial data input pin(0)
				ICU9_1	-		Input capture ch.9 input pin(1)
				BIN1_0	-		U/D counter ch.1 BIN input pin(0)
				INT12_0	-		INT12 external interrupt input pin(0)
25	31	35	U2	P042	-	B	General-purpose I/O port
				A12	-		External Bus address bit12 output pin
				SOT9_0	-		Multi-function serial ch.9 serial data output pin(0)
				AN47	-		ADC analog 47 input pin
				ICU8_1	-		Input capture ch.8 input pin(1)
				TRG0_1	-		PPG trigger 0 input pin(1)
				ZIN1_0	-		U/D counter ch.1 ZIN input pin(0)
26	32	36	V1	P043	-	A	General-purpose I/O port
				A13	-		External Bus address bit13 output pin
				ICU7_1	-		Input capture ch.7 input pin(1)
				TRG1_1	-		PPG trigger 1 input pin(1)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
27	33	37	V2	P044	-	A	General-purpose I/O port
				A14	-		External Bus address bit14 output pin
				SCS9_0	-		Serial chip select 9 I/O pin(0)
				ICU6_1	-		Input capture ch.6 input pin(1)
				TRG2_1	-		PPG trigger 2 input pin(1)
28	34	38	W1	P045	-	G	General-purpose I/O port
				A15	-		External Bus address bit15 output pin
				SCK9_0	-		Multi-function serial ch.9 clock I/O pin(0)
				AN46	-		ADC analog 46 input pin
				ICU5_1	-		Input capture ch.5 input pin(1)
				TRG3_1	-		PPG trigger 3 input pin(1)
				TOT1_2	-		Reload timer ch.1 output pin(2)
-	-	39	V3	P204	-	Q	General-purpose I/O port
				SCK13_0/SCL13	-		Multi-function serial ch.13 clock I/O pin(0)/ I ² C bus serial clock I/O pin
				AN59	-		ADC analog 59 input pin
				PPG48_0	-		PPG ch.48 output pin(0)
-	-	40	V4	P205	-	Q	General-purpose I/O port
				SOT13_0/SDA13	-		Multi-function serial ch.13 serial data output pin(0)/I ² C bus serial data I/O pin
				AN58	-		ADC analog 58 input pin
				PPG49_0	-		PPG ch.49 output pin(0)
				AIN2_0	-		U/D counter ch.2 AIN input pin(0)
-	-	41	W4	P206	-	G	General-purpose I/O port
				SIN13_0	-		Multi-function serial ch.13 serial data input pin(0)
				AN57	-		ADC analog 57 input pin
				BIN2_0	-		U/D counter ch.2 BIN input pin(0)
				INT17_0	-		INT17 external interrupt input pin(0)
-	-	42	Y4	P207	-	B	General-purpose I/O port
				SCS13_0	-		Serial chip select 13 I/O pin(0)
				AN56	-		ADC analog 56 input pin
				ZIN2_0	-		U/D counter ch.2 ZIN input pin(0)
29	35	43	W2	P046	-	A	General-purpose I/O port
				A16	-		External Bus address bit16 output pin
				ICU4_1	-		Input capture ch.4 input pin(1)
				TRG4_1	-		PPG trigger 4 input pin(1)
-	36	44	AA3	P176	-	A	General-purpose I/O port
				TRG10_0	-		PPG trigger 10 input pin(0)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
30	37	45	Y1	P047	-	B	General-purpose I/O port
				A17	-		External Bus address bit17 output pin
				AN45	-		ADC analog 45 input pin
				TRG8_0	-		PPG trigger 8 input pin(0)
				TIN3_2	-		Reload timer ch.3 event input pin(2)
				SOT0_1	-		Multi-function serial ch.0 serial data output pin(1)
-	38	46	AA4	P177	-	A	General-purpose I/O port
				TRG11_0	-		PPG trigger 11 input pin(0)
31	39	47	Y2	P050	-	A	General-purpose I/O port
				A18	-		External Bus address bit18 output pin
				TRG5_1	-		PPG trigger 5 input pin(1)
				PPG33_0	-		PPG ch.33 output pin(0)
32	40	48	AA1	P051	-	A	General-purpose I/O port
				A19	-		External Bus address bit19 output pin
				TRG9_0	-		PPG trigger 9 input pin(0)
				TX5(128)_0	-		CAN transmission data 5 output pin(0)
-	-	-	AB3	P250	-	A	General-purpose I/O port
				PPG66_0	-		PPG ch.66 output pin(0)
-	-	-	AB4	P251	-	A	General-purpose I/O port
				PPG67_0	-		PPG ch.67 output pin(0)
33	41	49	AA2	P052	-	R	General-purpose I/O port
				A20	-		External Bus address bit20 output pin
				PPG34_0	-		PPG ch.34 output pin(0)
				INT14_0	-		INT14 external interrupt input pin(0)
				RX5(128)_0	-		CAN reception data 5 input pin(0)
34	42	50	AB1	P053	-	B	General-purpose I/O port
				A21	-		External Bus address bit21 output pin
				AN44	-		ADC analog 44 input pin
				PPG35_0	-		PPG ch.35 output pin(0)
				INT14_1	-		INT14 external interrupt input pin(1)
				SCK0_1	-		Multi-function serial ch.0 clock I/O pin(1)
35	43	51	AB2	P054	-	A	General-purpose I/O port
				SYSCCLK	-		External Bus system clock output pin
				PPG36_0	-		PPG ch.36 output pin(0)
-	-	-	AC1	P252	-	A	General-purpose I/O port
-	-	-	AC2	P253	-	A	General-purpose I/O port
-	-	-	AE4	P254	-	A	General-purpose I/O port
				PPG68_0	-		PPG ch.68 output pin(0)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
-	-	-	AD5	P255	-	A	General-purpose I/O port
-	-	-	AD5	PPG69_0	-		PPG ch.69 output pin(0)
38	46	54	AF3	P055	-	G	General-purpose I/O port
				CS2X	-		External Bus chip select 2 output pin
				SIN10_0	-		Multi-function serial ch.10 serial data input pin(0)
				AN43	-		ADC analog 43 input pin
				PPG37_0	-		PPG ch.37 output pin(0)
				TIN4_1	-		Reload timer ch.4 event input pin(1)
-	47	55	AC5	P180	-	A	General-purpose I/O port
-	47	55	AC5	PPG40_0	-		PPG ch.40 output pin(0)
-	48	56	AC6	P181	-	A	General-purpose I/O port
-	48	56	AC6	PPG41_0	-		PPG ch.41 output pin(0)
39	49	57	AE3	P056	-	A	General-purpose I/O port
				CS3X	-		External Bus chip select 3 output pin
				ICU9_0	-		Input capture ch.9 input pin(0)
				PPG0_1	-		PPG ch.0 output pin(1)
				ICU0_1	-		Input capture ch.0 input pin(1)
				TIN5_1	-		Reload timer ch.5 event input pin(1)
				DTTI_2	-		Waveform generator ch.0 to ch.5 input pin(2)
-	-	-	AD6	P256	-	A	General-purpose I/O port
-	-	-	AD6	PPG66_1	-		PPG ch.66 output pin(1)
41	51	59	AE5	P057	-	G	General-purpose I/O port
				RDY_0	-		External Bus RDY input pin (0)
				SCK10_1	-		Multi-function serial ch.10 clock I/O pin(1)
				AN42	-		ADC analog 42 input pin
				ICU8_0	-		Input capture ch.8 input pin(0)
				TRG0_2	-		PPG trigger 0 input pin(2)
				PPG1_1	-		PPG ch.1 output pin(1)
				ICU1_1	-		Input capture ch.1 input pin(1)
				TIN6_1	-		Reload timer ch.6 event input pin(1)
-	56	64	AC7	P182	-	A	General-purpose I/O port
-	56	64	AC7	PPG42_0	-		PPG ch.42 output pin(0)
-	-	65	AE6	P210	-	Q	General-purpose I/O port
				SCK14_0/SCL14	-		Multi-function serial ch.14 clock I/O pin(0)/ I ² C bus serial clock I/O pin
				AN55	-		ADC analog 55 input pin
				PPG50_0	-		PPG ch.50 output pin(0)
				AIN2_1	-		U/D counter ch.2 AIN input pin(1)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
-	-	66	AC8	P211	-	Q	General-purpose I/O port
				SOT14_0/SDA14	-		Multi-function serial ch.14 serial data output pin(0)/I ² C bus serial data I/O pin
				AN54	-		ADC analog 54 input pin
				PPG51_0	-		PPG ch.51 output pin(0)
				BIN2_1	-		U/D counter ch.2 BIN input pin(1)
-	-	67	AE7	P212	-	G	General-purpose I/O port
				SIN14_0	-		Multi-function serial ch.14 serial data input pin(0)
				AN53	-		ADC analog 53 input pin
				FRCK6_0	-		Free-run timer 6 clock input pin(0)
				ZIN2_1	-		U/D counter ch.2 ZIN input pin(1)
				INT18_0	-		INT18 external interrupt input pin(0)
-	-	68	AD8	P213	-	B	General-purpose I/O port
				SCS14_0	-		Serial chip select 14 I/O pin(0)
				AN52	-		ADC analog 52 input pin
				FRCK7_0	-		Free-run timer 7 clock input pin(0)
				INT17_1	-		INT17 external interrupt input pin(1)
46	57	69	AE8	P060	-	A	General-purpose I/O port
				SCS10_0	-		Serial chip select 10 I/O pin(0)
				PPG2_1	-		PPG ch.2 output pin(1)
				ICU2_1	-		Input capture ch.2 input pin(1)
				TOT5_1	-		Reload timer ch.5 output pin(1)
				INT13_0	-		INT13 external interrupt input pin(0)
47	58	70	AC10	P061	-	B	General-purpose I/O port
				SOT10_1	-		Multi-function serial ch.10 serial data output pin(1)
				AN41	-		ADC analog 41 input pin
				ICU6_0	-		Input capture ch.6 input pin(0)
				PPG3_1	-		PPG ch.3 output pin(1)
				ICU3_1	-		Input capture ch.3 input pin(1)
				TOT6_1	-		Reload timer ch.6 output pin(1)
				INT13_1	-		INT13 external interrupt input pin(1)
48	59	71	AD11	P062	-	B	General-purpose I/O port
				SCS10_1	-		Serial chip select 10 I/O pin(1)
				SCS40_0	-		Serial chip select 40 I/O pin(0)
				AN40	-		ADC analog 40 input pin
				PPG4_1	-		PPG ch.4 output pin(1)
				FRCK0_0	-		Free-run timer 0 clock input pin(0)
				TOT7_1	-		Reload timer ch.7 output pin(1)
				ZIN1_1	-		U/D counter ch.1 ZIN input pin(1)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
49	60	72	AC11	P063	-	B	General-purpose I/O port
				SCS41_0	-		Serial chip select 41 output pin(0)
				AN39	-		ADC analog 39 input pin
				PPG5_1	-		PPG ch.5 output pin(1)
				FRCK1_0	-		Free-run timer 1 clock input pin(0)
				BIN1_1	-		U/D counter ch.1 BIN input pin(1)
-	61	73	AF12	P183	-	A	General-purpose I/O port
				PPG43_0	-		PPG ch.43 output pin(0)
50	62	74	AE12	P064	-	B	General-purpose I/O port
				SCS42_0	-		Serial chip select 42 output pin(0)
				AN38	-		ADC analog 38 input pin
				FRCK2_0	-		Free-run timer 2 clock input pin(0)
				AIN1_1	-		U/D counter ch.1 AIN input pin(1)
				PPG43_1	-		PPG ch.43 output pin(1)
51	63	75	AC12	P065	-	A	General-purpose I/O port
				SCS43_0	-		Serial chip select 43 output pin(0)
				FRCK3_0	-		Free-run timer 3 clock input pin(0)
				ZIN0_1	-		U/D counter ch.0 ZIN input pin(1)
				PPG44_1	-		PPG ch.44 output pin(1)
-	64	76	AF13	P184	-	A	General-purpose I/O port
				PPG44_0	-		PPG ch.44 output pin(0)
-	65	77	AE13	P185	-	A	General-purpose I/O port
				PPG45_0	-		PPG ch.45 output pin(0)
52	66	78	AC13	P066	-	B	General-purpose I/O port
				SOT4_2	-		Multi-function serial ch.4 serial data output pin(2)
				SCS3_0	-		Serial chip select 3 I/O pin(0)
				AN37	-		ADC analog 37 input pin
				FRCK4_0	-		Free-run timer 4 clock input pin(0)
				BIN0_1	-		U/D counter ch.0 BIN input pin(1)
53	67	79	AF14	P067	-	B	General-purpose I/O port
				AN36	-		ADC analog 36 input pin
				FRCK5_0	-		Free-run timer 5 clock input pin(0)
				AIN0_1	-		U/D counter ch.0 AIN input pin(1)
54	68	80	AE14	P070	-	A	General-purpose I/O port
				ICU0_2	-		Input capture ch.0 input pin(2)
55	69	81	AD14	P071	-	G	General-purpose I/O port
				SCK4_2	-		Multi-function serial ch.4 clock I/O pin(2)
				AN35	-		ADC analog 35 input pin
				ICU1_2	-		Input capture ch.1 input pin(2)
				MONCLK	-		Clock monitor output pin

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
56	70	82	AC14	P072	-	G	General-purpose I/O port
				SIN4_0	-		Multi-function serial ch.4 serial data input pin(0)
				AN34	-		ADC analog 34 input pin
				ICU2_2	-		Input capture ch.2 input pin(2)
				INT5_0	-		INT5 external interrupt input pin(0)
57	71	83	AF15	P073	-	D	General-purpose I/O port
				SOT4_0/SDA4	-		Multi-function serial ch.4 serial data output pin(0)/I ² C bus serial data I/O pin
				AN33	-		ADC analog 33 input pin
				ICU3_2	-		Input capture ch.3 input pin(2)
-	-	-	AE15	P262	-	A	General-purpose I/O port
				PPG70_0	-		PPG ch.70 output pin(0)
-	-	-	AC15	P263	-	A	General-purpose I/O port
				PPG71_0	-		PPG ch.71 output pin(0)
-	72	84	AF16	P186	-	A	General-purpose I/O port
				PPG46_0	-		PPG ch.46 output pin(0)
-	73	85	AE16	P187	-	A	General-purpose I/O port
				PPG47_0	-		PPG ch.47 output pin(0)
58	74	86	AC16	P074	-	E	General-purpose I/O port
				SCK4_0/SCL4	-		Multi-function serial ch.4 clock I/O pin(0) / I ² C bus serial clock I/O pin
-	-	87	AF18	P214	-	Q	General-purpose I/O port
				SCK15_0/SCL15	-		Multi-function serial ch.15 clock I/O pin(0)/ I ² C bus serial clock I/O pin
				AN51	-		ADC analog 51 input pin
				PPG52_0	-		PPG ch.52 output pin(0)
-	-	88	AF17	P215	-	Q	General-purpose I/O port
				SOT15_0/SDA15	-		Multi-function serial ch.15 serial data output pin(0)/I ² C bus serial data I/O pin
				AN50	-		ADC analog 50 input pin
				FRCK8_0	-		Free-run timer 8 clock input pin(0)
				PPG53_0	-		PPG ch.53 output pin(0)
-	-	89	AE17	P216	-	G	General-purpose I/O port
				SIN15_0	-		Multi-function serial ch.15 serial data input pin(0)
				AN49	-		ADC analog 49 input pin
				FRCK9_0	-		Free-run timer 9 clock input pin(0)
				TRG12_1	-		PPG trigger 12 input pin(1)
				INT19_0	-		INT19 external interrupt input pin(0)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
-	-	90	AF19	P217	-	B	General-purpose I/O port
				SCS15_0	-		Serial chip select 15 I/O pin(0)
				AN48	-		ADC analog 48 input pin
				FRCK10_0	-		Free-run timer 10 clock input pin(0)
				TRG13_1	-		PPG trigger 13 input pin(1)
59	75	91	AE18	P075	-	F	General-purpose I/O port
				SIN3_0	-		Multi-function serial ch.3 serial data input pin(0)
				INT4_0	-		INT4 external interrupt input pin(0)
				RX5(128)_1	-		CAN reception data 5 input pin(1)
60	76	92	AD17	P076	-	P	General-purpose I/O port
				SOT3_0/SDA3	-		Multi-function serial ch.3 serial data output pin(0)/I ² C bus serial data I/O pin
				TX5(128)_1	-		CAN transmission data 5 output pin(1)
61	77	93	AF20	P077	-	E	General-purpose I/O port
				SCK3_0/SCL3	-		Multi-function serial ch.3 clock I/O pin(0)/I ² C bus serial clock I/O pin
-	-	-	AE19	P264	-	A	General-purpose I/O port
				PPG72_0	-		PPG ch.72 output pin(0)
-	-	-	AC17	P265	-	A	General-purpose I/O port
				PPG73_0	-		PPG ch.73 output pin(0)
62	78	94	AF21	P152	-	A	General-purpose I/O port
				SCS53_0	-		Serial chip select 53 output pin(0)
63	79	95	AE20	P153	-	G	General-purpose I/O port
				SCK5_0/SCL5	-		Multi-function serial ch.5 clock I/O pin(0)/I ² C bus serial clock I/O pin
				AN32	-		ADC analog 32 input pin
				FRCK1_1	-		Free-run timer 1 clock input pin(1)
				INT4_1	-		INT4 external interrupt input pin(1)
64	80	96	AC18	P080	-	A	General-purpose I/O port
				SCS52_0	-		Serial chip select 52 output pin(0)
				PPG0_0	-		PPG ch.0 output pin(0)
65	81	97	AF22	P081	-	G	General-purpose I/O port
				SOT5_0/SDA5	-		Multi-function serial ch.5 serial data output pin(0)/I ² C bus serial data I/O pin
				AN0	-		ADC analog 0 input pin
				PPG1_0	-		PPG ch.1 output pin(0)
-	-	-	AE21	TDO	-	W	JTAG test data output
-	-	-	AD20	TDI	-	V	JTAG test data input

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
66	82	98	AC19	P082	-	G	General-purpose I/O port
				SIN5_0	-		Multi-function serial ch.5 serial data input pin(0)
				AN1	-		ADC analog 1 input pin
				PPG2_0	-		PPG ch.2 output pin(0)
-	-	-	AE22	TRST	-	V	JTAG test reset input
-	-	-	AC20	TCK	-	V	JTAG test clock input
-	-	-	AE23	TMS	-	V	JTAG test mode state input
67	83	99	AC21	P083	-	B	General-purpose I/O port
				SCS50_0	-		Serial chip select 50 I/O pin(0)
				AN2	-		ADC analog 2 input pin
				PPG3_0	-		PPG ch.3 output pin(0)
68	84	100	AF23	P084	-	B	General-purpose I/O port
				SCS51_0	-		Serial chip select 51 output pin(0)
				AN3	-		ADC analog 3 input pin
				PPG4_0	-		PPG ch.4 output pin(0)
69	85	101	AD23	P085	-	A	General-purpose I/O port
				PPG5_0	-		PPG ch.5 output pin(0)
70	86	102	AC22	P086	-	C	General-purpose I/O port
				DAO1	-		DAC analog 1 output pin
				PPG6_0	-		PPG ch.6 output pin(0)
71	87	103	AD25	P087	-	C	General-purpose I/O port
				DAO0	-		DAC analog 0 output pin
				PPG7_0	-		PPG ch.7 output pin(0)
				INT8_0	-		INT8 external interrupt input pin(0)
-	-	-	AC24	P266	-	A	General-purpose I/O port
				PPG74_0	-		PPG ch.74 output pin(0)
-	-	-	AB23	P267	-	A	General-purpose I/O port
				PPG75_0	-		PPG ch.75 output pin(0)
-	90	106	AD26	P190	-	A	General-purpose I/O port
				TIN0_1	-		Reload timer ch.0 event input pin(1)
-	91	107	AC25	P191	-	A	General-purpose I/O port
				TIN1_1	-		Reload timer ch.1 event input pin(1)
74	92	108	AB24	P090	-	B	General-purpose I/O port
				AN4	-		ADC analog 4 input pin
				ICU0_0	-		Input capture ch.0 input pin(0)
				TIN2_1	-		Reload timer ch.2 event input pin(1)
-	-	-	AA23	P270	-	A	General-purpose I/O port
				PPG76_0	-		PPG ch.76 output pin(0)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
-	-	-	AC26	P271	-	A	General-purpose I/O port
-	-	-	AC26	PPG77_0	-		PPG ch.77 output pin(0)
75	93	109	AB25	P091	-	B	General-purpose I/O port
				AN5	-		ADC analog 5 input pin
				PPG41_1	-		PPG ch.41 output pin(1)
				ICU1_0	-		Input capture ch.1 input pin(0)
				TIN3_1	-		Reload timer ch.3 event input pin(1)
76	94	110	Y23	P092	-	B	General-purpose I/O port
				AN6	-		ADC analog 6 input pin
				PPG40_1	-		PPG ch.40 output pin(1)
				ICU2_0	-		Input capture ch.2 input pin(0)
				TOT0_1	-		Reload timer ch.0 output pin(1)
-	95	111	AB26	P192	-	A	General-purpose I/O port
				PPG24_1	-		PPG ch.24 output pin(1)
				TOT1_1	-		Reload timer ch.1 output pin(1)
-	-	-	AA25	P272	-	A	General-purpose I/O port
				PPG78_0	-		PPG ch.78 output pin(0)
-	-	-	Y24	P273	-	A	General-purpose I/O port
				PPG79_0	-		PPG ch.79 output pin(0)
77	96	112	W23	P093	-	J	General-purpose I/O port
				TX0(128)_1	-		CAN transmission data 0 output pin(1)
				SIN11_0	-		Multi-function serial ch.11 serial data input pin(0)
				AN7	-		ADC analog 7 input pin
				ICU4_2	-		Input capture ch.4 input pin(2)
				PPG16_1	-		PPG ch.16 output pin(1)
				ICU3_0	-		Input capture ch.3 input pin(0)
				TOT2_1	-		Reload timer ch.2 output pin(1)
78	97	113	AA26	P094	-	B	General-purpose I/O port
				AN8	-		ADC analog 8 input pin
				ICU4_0	-		Input capture ch.4 input pin(0)
				TOT3_1	-		Reload timer ch.3 output pin(1)
79	98	114	Y25	P095	-	B	General-purpose I/O port
				TX0(128)_0	-		CAN transmission data 0 output pin(0)
				SCS11_0	-		Serial chip select 11 I/O pin(0)
				AN9	-		ADC analog 9 input pin

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
80	99	115	V23	P096	-	G	General-purpose I/O port
				RX0(128)_0	-		CAN reception data 0 input pin(0)
				SOT11_0/SDA11	-		Multi-function serial ch.11 serial data output pin(0)/I ² C bus serial data I/O pin
				AN10	-		ADC analog 10 input pin
				INT0_0	-		INT0 external interrupt input pin(0)
81	100	116	Y26	P097	-	G	General-purpose I/O port
				SCK11_0/SCL11	-		Multi-function serial ch.11 clock I/O pin(0)/I ² C bus serial clock I/O pin
				AN11	-		ADC analog 11 input pin
				ICU5_0	-		Input capture ch.5 input pin(0)
				PPG17_1	-		PPG ch.17 output pin(1)
-	-	117	W25	P220	-	P	General-purpose I/O port
				SCK16_0/SCL16	-		Multi-function serial ch.16 clock I/O pin(0)/I ² C bus serial clock I/O pin
				ICU10_0	-		Input capture ch.10 input pin(0)
				PPG48_1	-		PPG ch.48 output pin(1)
-	-	118	U23	P221	-	P	General-purpose I/O port
				SOT16_0/SDA16	-		Multi-function serial ch.16 serial data output pin(0)/I ² C bus serial data I/O pin
				ICU11_0	-		Input capture ch.11 input pin(0)
				PPG49_1	-		PPG ch.49 output pin(1)
-	-	119	V25	P222	-	I	General-purpose I/O port
				SIN16_0	-		Multi-function serial ch.16 serial data input pin(0)
				PPG54_0	-		PPG ch.54 output pin(0)
				INT20_0	-		INT20 external interrupt input pin(0)
-	-	-	U24	P275	-	A	General-purpose I/O port
				PPG67_1	-		PPG ch.67 output pin(1)
-	-	-	U25	P276	-	A	General-purpose I/O port
				TRG16_1	-		PPG trigger 16 input pin(1)
				PPG86_1	-		PPG ch.86 output pin(1)
85	104	123	T25	P100	-	G	General-purpose I/O port
				SCK7_0/SCL7	-		Multi-function serial ch.7 clock I/O pin(0)/I ² C bus serial clock I/O pin
				AN12	-		ADC analog 12 input pin
				PPG8_0	-		PPG ch.8 output pin(0)
86	105	124	T23	P101	-	G	General-purpose I/O port
				SOT7_0/SDA7	-		Multi-function serial ch.7 serial data output pin(0)/I ² C bus serial data I/O pin
				AN13	-		ADC analog 13 input pin
				PPG9_0	-		PPG ch.9 output pin(0)
				TX3(128)_0	-		CAN transmission data 3 output pin(0)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
87	106	125	R26	P102	-	G	General-purpose I/O port
				SIN7_0	-		Multi-function serial ch.7 serial data input pin(0)
				AN14	-		ADC analog 14 input pin
				PPG10_0	-		PPG ch.10 output pin(0)
				INT10_0	-		INT10 external interrupt input pin(0)
				RX3(128)_0	-		CAN reception data 3 input pin(0)
88	107	126	R25	P103	-	H	General-purpose I/O port
				SCS73_0	-		Serial chip select 73 output pin(0)
				AN15	-		ADC analog 15 input pin
				PPG11_0	-		PPG ch.11 output pin(0)
89	108	127	R23	P104	-	H	General-purpose I/O port
				SCS72_0	-		Serial chip select 72 output pin(0)
				AN16	-		ADC analog 16 input pin
				PPG12_0	-		PPG ch.12 output pin(0)
90	109	128	P25	P105	-	H	General-purpose I/O port
				SCS71_0	-		Serial chip select 71 output pin(0)
				AN17	-		ADC analog 17 input pin
				PPG13_0	-		PPG ch.13 output pin(0)
91	110	129	P24	P106	-	H	General-purpose I/O port
				SCS70_0	-		Serial chip select 70 I/O pin(0)
				AN18	-		ADC analog 18 input pin
				PPG14_0	-		PPG ch.14 output pin(0)
92	111	130	P23	P107	-	U	General-purpose I/O port
				AN19	-		ADC analog 19 input pin
				PPG15_0	-		PPG ch.15 output pin(0)
				TXENA_1	-		FlexRay ch.A operation enable output(1)
-	112	131	P26	P193	-	A	General-purpose I/O port
				PPG25_1	-		PPG ch.25 output pin(1)
93	113	132	N23	P154	-	U	General-purpose I/O port
				AN20	-		ADC analog 20 input pin
				TXDA_1	-		FlexRay ch.A data output(1)
94	114	133	L26	P155	-	S	General-purpose I/O port
				AN21	-		ADC analog 21 input pin
				RXDA_1	-		FlexRay ch.A data input(1)
95	115	136	L25	NMIX	N	M	Non-maskable interrupt input pin
-	-	-	L24	P277	-	A	General-purpose I/O port
				TRG17_1	-		PPG trigger 17 input pin(1)
				PPG87_1	-		PPG ch.87 output pin(1)
96	116	137	L23	P110	-	B	General-purpose I/O port
				TX1(128)_0	-		CAN transmission data 1 output pin(0)
				SCS63_0	-		Serial chip select 63 output pin(0)
				AN22	-		ADC analog 22 input pin

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
97	117	138	J26	P111	-	G	General-purpose I/O port
				RX1(128)_0	-		CAN reception data 1 input pin(0)
				SCS62_0	-		Serial chip select 62 output pin(0)
				AN23	-		ADC analog 23 input pin
				INT1_0	-		INT1 external interrupt input pin(0)
98	118	139	K26	P112	-	U	General-purpose I/O port
				AN24	-		ADC analog 24 input pin
				PPG16_0	-		PPG ch.16 output pin(0)
				RTO0_0	-		Waveform generator ch.0 output pin(0)
				TXENB_1	-		FlexRay ch.B operation enable output(1)
99	119	140	K25	P113	-	U	General-purpose I/O port
				AN25	-		ADC analog 25 input pin
				PPG17_0	-		PPG ch.17 output pin(0)
				RTO1_0	-		Waveform generator ch.1 output pin(0)
				TXDB_1	-		FlexRay ch.B data output(1)
-	120	141	H26	P194	-	A	General-purpose I/O port
				FRCK5_1	-		Free-run timer 5 clock input pin(1)
				PPG26_1	-		PPG ch.26 output pin(1)
-	121	142	J25	P195	-	A	General-purpose I/O port
				FRCK4_1	-		Free-run timer 4 clock input pin(1)
				PPG27_1	-		PPG ch.27 output pin(1)
-	-	-	G26	P280	-	A	General-purpose I/O port
				PPG80_0	-		PPG ch.80 output pin(0)
-	-	-	H25	P281	-	A	General-purpose I/O port
				PPG81_0	-		PPG ch.81 output pin(0)
100	122	143	K23	P114	-	S	General-purpose I/O port
				SCS61_0	-		Serial chip select 61 output pin(0)
				AN26	-		ADC analog 26 input pin
				PPG18_0	-		PPG ch.18 output pin(0)
				RTO2_0	-		Waveform generator ch.2 output pin(0)
				RXDB_1	-		FlexRay ch.B data input(1)
101	123	144	F26	P115	-	G	General-purpose I/O port
				RX1(128)_1	-		CAN reception data 1 input pin(1)
				SOT6_0/SDA6	-		Multi-function serial ch.6 serial data output pin(0)/I ² C bus serial data I/O pin
				AN27	-		ADC analog 27 input pin
				PPG19_0	-		PPG ch.19 output pin(0)
				RTO3_0	-		Waveform generator ch.3 output pin(0)
				INT1_1	-		INT1 external interrupt input pin(1)
102	124	145	G25	P116	-	G	General-purpose I/O port
				SCK6_0/SCL6	-		Multi-function serial ch.6 clock I/O pin(0)/I ² C bus serial clock I/O pin
				AN28	-		ADC analog 28 input pin
				PPG20_0	-		PPG ch.20 output pin(0)
				RTO4_0	-		Waveform generator ch.4 output pin(0)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
103	125	146	H24	P117	-	B	General-purpose I/O port
				SCS60_0	-		Serial chip select 60 I/O pin(0)
				AN29	-		ADC analog 29 input pin
				PPG21_0	-		PPG ch.21 output pin(0)
				RTO5_0	-		Waveform generator ch.5 output pin(0)
-	126	147	J23	P196	-	A	General-purpose I/O port
				FRCK3_1	-		Free-run timer 3 clock input pin(1)
				PPG28_1	-		PPG ch.28 output pin(1)
-	-	-	E26	P282	-	A	General-purpose I/O port
				PPG82_0	-		PPG ch.82 output pin(0)
-	-	-	F25	P283	-	A	General-purpose I/O port
				PPG83_0	-		PPG ch.83 output pin(0)
104	127	148	H23	P120	-	S	General-purpose I/O port
				AN30	-		ADC analog 30 input pin
				OCU6_0	-		Output compare ch.6 output pin(0)
				PPG22_0	-		PPG ch.22 output pin(0)
				INT9_0	-		INT9 external interrupt input pin(0)
				RX4(128)_0	-		CAN reception data 4 input pin(0)
105	128	149	D26	P121	-	A	General-purpose I/O port
				OCU7_0	-		Output compare ch.7 output pin(0)
				PPG23_0	-		PPG ch.23 output pin(0)
				TX4(128)_0	-		CAN transmission data 4 output pin(0)
106	129	150	E25	P122	-	J	General-purpose I/O port
				SIN6_0	-		Multi-function serial ch.6 serial data input pin(0)
				AN31	-		ADC analog 31 input pin
				OCU8_0	-		Output compare ch.8 output pin(0)
				INT9_1	-		INT9 external interrupt input pin(1)
-	-	151	G23	P225	-	P	General-purpose I/O port
				SCK17_0/SCL17	-		Multi-function serial ch.17 clock I/O pin(0)/ I ² C bus serial clock I/O pin
				PPG55_0	-		PPG ch.55 output pin(0)
-	-	152	D25	P226	-	P	General-purpose I/O port
				SOT17_0/SDA17	-		Multi-function serial ch.17 serial data output pin(0)/I ² C bus serial data I/O pin
				PPG56_0	-		PPG ch.56 output pin(0)
-	-	153	E24	P227	-	I	General-purpose I/O port
				SIN17_0	-		Multi-function serial ch.17 serial data input pin(0)
				PPG57_0	-		PPG ch.57 output pin(0)
				INT21_0	-		INT21 external interrupt input pin(0)
-	130	154	F23	P197	-	A	General-purpose I/O port
				PPG29_1	-		PPG ch.29 output pin(1)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
107	131	155	E23	P123	-	R	General-purpose I/O port
				OCU9_0	-		Output compare ch.9 output pin(0)
				STOPWT_1	-		FlexRay stopwatch input(1)
110	134	158	C26	DEBUGIF	-	L	DEBUGIF I/O pin for debug (OCD)
-	-	-	C25	P284	-	A	General-purpose I/O port
				PPG84_0	-		PPG ch.84 output pin(0)
-	-	-	D22	P285	-	A	General-purpose I/O port
				PPG85_0	-		PPG ch.85 output pin(0)
-	135	159	C22	P160	-	A	General-purpose I/O port
				PPG30_1	-		PPG ch.30 output pin(1)
-	136	160	D21	P161	-	A	General-purpose I/O port
				PPG31_1	-		PPG ch.31 output pin(1)
-	-	-	B22	P286	-	A	General-purpose I/O port
				TRG18_0	-		PPG trigger 18 input pin(0)
-	-	-	C21	P287	-	A	General-purpose I/O port
				TRG19_0	-		PPG trigger 19 input pin(0)
111	137	161	-	P124	-	A	General-purpose I/O port
				OCU10_0	-		Output compare ch.10 output pin(0)
				TRST	-		JTAG test reset input
-	-	-	D20	P124	-	A	General-purpose I/O port
				OCU10_0	-		Output compare ch.10 output pin(0)
112	138	162	-	P125	-	A	General-purpose I/O port
				OCU11_0	-		Output compare ch.11 output pin(0)
				TMS	-		JTAG test mode state input
-	-	-	A22	P125	-	A	General-purpose I/O port
				OCU11_0	-		Output compare ch.11 output pin(0)
-	-	163	B21	P230	-	P	General-purpose I/O port
				SCK18_0/SCL18	-		Multi-function serial ch.18 clock I/O pin(0)/ I ² C bus serial clock I/O pin
				OCU12_0	-		Output compare ch.12 output pin(0)
				PPG58_0	-		PPG ch.58 output pin(0)
-	-	164	C20	P231	-	P	General-purpose I/O port
				SOT18_0/SDA18	-		Multi-function serial ch.18 serial data output pin(0)/I ² C bus serial data I/O pin
				OCU13_0	-		Output compare ch.13 output pin(0)
				PPG59_0	-		PPG ch.59 output pin(0)
-	-	165	D19	P232	-	I	General-purpose I/O port
				SIN18_0	-		Multi-function serial ch.18 serial data input pin(0)
				PPG60_0	-		PPG ch.60 output pin(0)
				INT22_0	-		INT22 external interrupt input pin(0)
-	-	166	C19	P233	-	A	General-purpose I/O port
				SCS18_0	-		Serial chip select 18 I/O pin(0)
				PPG61_0	-		PPG ch.61 output pin(0)
				INT16_1	-		INT16 external interrupt input pin(1)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
-	-	-	D18	P290	-	A	General-purpose I/O port
				TRG20_0	-		PPG trigger 20 input pin(0)
				PPG64_1	-		PPG ch.64 output pin(1)
-	-	-	B18	P291	-	A	General-purpose I/O port
				TRG21_0	-		PPG trigger 21 input pin(0)
				PPG65_1	-		PPG ch.65 output pin(1)
113	139	167	-	P126	-	F	General-purpose I/O port
				SIN0_0	-		Multi-function serial ch.0 serial data input pin(0)
				INT6_0	-		INT6 external interrupt input pin(0)
				TDI	-		JTAG test data input
-	-	-	C18	P126	-	F	General-purpose I/O port
				SIN0_0	-		Multi-function serial ch.0 serial data input pin(0)
				INT6_0	-		INT6 external interrupt input pin(0)
114	140	168	-	P127	-	A	General-purpose I/O port
				SOT0_0	-		Multi-function serial ch.0 serial data output pin(0)
				TDO	-		JTAG test data output
-	-	-	C17	P127	-	A	General-purpose I/O port
				SOT0_0	-		Multi-function serial ch.0 serial data output pin(0)
115	141	169	-	P130	-	F	General-purpose I/O port
				SCK0_0	-		Multi-function serial ch.0 clock I/O pin(0)
				TCK	-		JTAG test clock input
-	-	-	D17	P130	-	F	General-purpose I/O port
				SCK0_0	-		Multi-function serial ch.0 clock I/O pin(0)
-	142	170	C16	P162	-	A	General-purpose I/O port
				TRG5_2	-		PPG trigger 5 input pin(2)
-	143	171	D16	P163	-	A	General-purpose I/O port
				TRG6_2	-		PPG trigger 6 input pin(2)
116	144	172	B23	MD0	-	K	Mode pin 0
117	145	173	A23	MD1	-	K	Mode pin 1
118	146	174	A20	X0	-	N	Main clock oscillation input pin
119	147	175	A19	X1	-	N	Main clock oscillation output pin
121	149	177	A17	P135	-	A	General-purpose I/O port
				DTTI_0	-		Waveform generator ch.0 to ch.5 input pin(0)
				X1A	-	O	Sub clock oscillation output pin
122	150	178	A16	P136	-	A	General-purpose I/O port
				X0A	-	O	Sub clock oscillation input pin
123	151	179	B15	RSTX	N	M	External reset input pin
126	154	182	D15	P133	-	A	General-purpose I/O port
				TX2(128)_0	-		CAN transmission data 2 output pin(0)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
127	155	183	D14	P134	-	F	General-purpose I/O port
				RX2(128)_0	-		CAN reception data 2 input pin(0)
				SCS1_1	-		Serial chip select 1 I/O pin(1)
				ICU7_0	-		Input capture ch.7 input pin(0)
				INT7_0	-		INT7 external interrupt input pin(0)
131	159	187	A10	P000	-	F	General-purpose I/O port
				D16	-		External Bus data bit16 I/O pin
				SIN1_0	-		Multi-function serial ch.1 serial data input pin(0)
				TIOA0_1	-		Base timer ch.0 TIOA output pin(1)
				INT2_0	-		INT2 external interrupt input pin(0)
132	160	188	B10	P001	-	R	General-purpose I/O port
				D17	-		External Bus data bit17 I/O pin
				SOT1_0	-		Multi-function serial ch.1 serial data output pin(0)
				TIOA1_1	-		Base timer ch.1 TIOA I/O pin(1)
133	161	189	A9	P002	-	F	General-purpose I/O port
				D18	-		External Bus data bit18 I/O pin
				SCK1_0	-		Multi-function serial ch.1 clock I/O pin(0)
				TIOB0_1	-		Base timer ch.0 TIOB input pin(1)
134	162	190	B9	P003	-	T	General-purpose I/O port
				D19	-		External Bus data bit19 I/O pin
				SIN2_0	-		Multi-function serial ch.2 serial data input pin(0)
				TIOB1_1	-		Base timer ch.1 TIOB input pin(1)
				INT3_0	-		INT3 external interrupt input pin(0)
				TXENA_0	-		FlexRay ch.A operation enable output(0)
135	163	191	A8	P004	-	R	General-purpose I/O port
				D20	-		External Bus data bit20 I/O pin
				SOT2_0	-		Multi-function serial ch.2 serial data output pin(0)
				TXDA_0	-		FlexRay ch.A data output(0)
-	164	192	D12	P164	-	A	General-purpose I/O port
				PPG32_1	-		PPG ch.32 output pin(1)
136	165	193	B8	P005	-	F	General-purpose I/O port
				D21	-		External Bus data bit21 I/O pin
				SCK2_0	-		Multi-function serial ch.2 clock I/O pin(0)
				ADTG0_1	-		A/D converter external trigger input pin 0(1)
				INT7_1	-		INT7 external interrupt input pin(1)
				RXDA_0	-		FlexRay ch.A data input(0)
-	166	194	C11	P165	-	A	General-purpose I/O port
				PPG33_1	-		PPG ch.33 output pin(1)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
137	167	195	A7	P006	-	R	General-purpose I/O port
				D22	-		External Bus data bit22 I/O pin
				SCS2_0	-		Serial chip select 2 I/O pin(0)
				ADTG1_1	-		A/D converter external trigger input pin 1(1)
				INT2_1	-		INT2 external interrupt input pin(1)
				TXENB_0	-		FlexRay ch.B operation enable output(0)
138	168	196	B7	P007	-	R	General-purpose I/O port
				D23	-		External Bus data bit23 I/O pin
				TXDB_0	-		FlexRay ch.B data output(0)
-	-	-	D11	P292	-	A	General-purpose I/O port
-	-	-	C10	P293	-	A	General-purpose I/O port
-	169	197	D10	P166	-	A	General-purpose I/O port
				PPG34_1	-		PPG ch.34 output pin(1)
139	170	198	A6	P010	-	R	General-purpose I/O port
				D24	-		External Bus data bit24 I/O pin
				RXDB_0	-		FlexRay ch.B data input(0)
-	-	199	C9	P234	-	P	General-purpose I/O port
				SCK19_0/SCL19	-		Multi-function serial ch.19 clock I/O pin(0)/ I ² C bus serial clock I/O pin
				PPG62_0	-		PPG ch.62 output pin(0)
-	-	200	D9	P235	-	P	General-purpose I/O port
				SOT19_0/SDA19	-		Multi-function serial ch.19 serial data output pin(0)/I ² C bus serial data I/O pin
				PPG63_0	-		PPG ch.63 output pin(0)
				AIN3_0	-		U/D counter ch.3 AIN input pin(0)
-	-	201	D8	P236	-	I	General-purpose I/O port
				SIN19_0	-		Multi-function serial ch.19 serial data input pin(0)
				TRG14_0	-		PPG trigger 14 input pin(0)
				BIN3_0	-		U/D counter ch.3 BIN input pin(0)
				INT23_0	-		INT23 external interrupt input pin(0)
-	-	202	D7	P237	-	A	General-purpose I/O port
				SCS19_0	-		Serial chip select 19 I/O pin(0)
				TRG15_0	-		PPG trigger 15 input pin(0)
				ZIN3_0	-		U/D counter ch.3 ZIN input pin(0)
140	171	203	B6	P011	-	R	General-purpose I/O port
				WOT	-		RTC output pin
				D25	-		External Bus data bit25 I/O pin
				SOT2_1	-		Multi-function serial ch.2 serial data output pin(1)
				TIOA0_0	-		Base timer ch.0 TIOA output pin(0)
				INT3_1	-		INT3 external interrupt input pin(1)
141	172	204	A5	P012	-	R	General-purpose I/O port
				D26	-		External Bus data bit26 I/O pin
				TIOB0_0	-		Base timer ch.0 TIOB input pin(0)
				STOPWT_0	-		FlexRay stopwatch input(0)

Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
-	-	-	C6	P294	-	A	General-purpose I/O port
-	-	-	C6	PPG86_0	-		PPG ch.86 output pin(0)
-	-	-	C5	P295	-	A	General-purpose I/O port
-	-	-	C5	PPG87_0	-		PPG ch.87 output pin(0)
-	173	205	D6	P167	-	A	General-purpose I/O port
-	173	205	D6	PPG35_1	-		PPG ch.35 output pin(1)
-	-	-	C4	P296	-	A	General-purpose I/O port
-	-	-	D5	P297	-	A	General-purpose I/O port
142	174	206	B5	P013	-	R	General-purpose I/O port
				D27	-		External Bus data bit27 I/O pin
				TIOA1_0	-		Base timer ch.1 TIOA I/O pin(0)
143	175	207	A4	P014	-	R	General-purpose I/O port
				D28	-		External Bus data bit28 I/O pin
				TIOB1_0	-		Base timer ch.1 TIOB input pin(0)
40	50	58	AF4	AVCC1	-	-	A/D, D/A converter unit1 analog power supply pin
84	103	122	T26	AVCC0	-	-	A/D, D/A converter unit0 analog power supply pin
42	52	60	AF5	AVRH1	-	-	A/D converter unit1 upper limit reference voltage pin
83	102	121	U26	AVRH0	-	-	A/D converter unit0 upper limit reference voltage pin
43	53	61	-	AVSS1/AVRL1	-	-	A/D, D/A converter unit1 GND / A/D converter unit1 lower limit reference voltage pin
-	-	-	AF7	AVSS1	-	-	A/D, D/A converter unit1 GND
-	-	-	AF6	AVRL1	-	-	A/D converter unit1 lower limit reference voltage pin
82	101	120	-	AVSS0/AVRL0	-	-	A/D, D/A converter unit0 GND / A/D converter unit0 lower limit reference voltage pin
-	-	-	W26	AVSS0	-	-	A/D, D/A converter unit0 GND
-	-	-	V26	AVRL0	-	-	A/D converter unit0 lower limit reference voltage pin
130	158	186	A13	C	-	-	External capacity connection output pin
-	-	63	AF10	VCC	-	-	Power supply (1)
45	55	104	AF11				
72	88	134	AE10				
109	133	157	AE11				
124	152	180	AE24				
-	-	-	AF24				
-	-	-	N25				
-	-	-	N26				
-	-	-	A24				
-	-	-	B24				
-	-	-	A14				
-	-	-	B14				

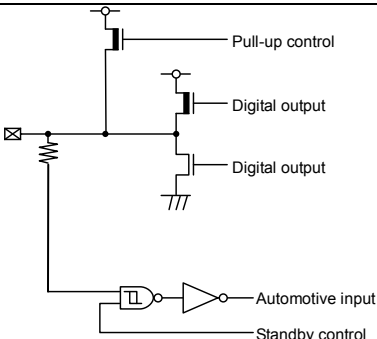
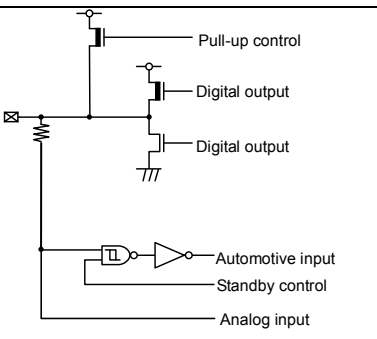
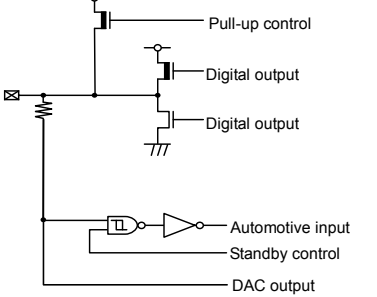
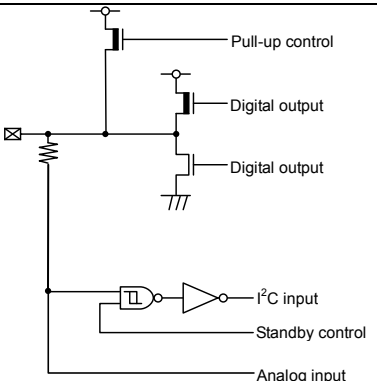
Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
36	44	52	M1	VCCE	-	-	Power supply (2)
128	156	184	M2				
144	176	208	AD2				
-	-	-	AD1				
-	-	-	A11				
-	-	-	B11				
-	-	-	B3				
-	-	-	A3				
1	1	1	A1	VSS	-	-	GND
37	45	53	B2				
44	54	62	P1				
73	89	105	P2				
108	132	135	AF1				
120	148	156	AE2				
125	153	176	AF8				
129	157	181	AF9				
-	-	185	AE9				
-	-	-	AD10				
-	-	-	AF26				
-	-	-	AE25				
-	-	-	M26				
-	-	-	M25				
-	-	-	A26				
-	-	-	B25				
-	-	-	A21				
-	-	-	A18				
-	-	-	B16				
-	-	-	A15				
-	-	-	A12				
-	-	-	B12				
-	-	-	A2,A25				
-	-	-	B1,B4				
-	-	-	B13,B17				
-	-	-	B19,B20				
-	-	-	B26				
-	-	-	C2,C3				
-	-	-	C7,C8				
-	-	-	C12,C13				
-	-	-	C14,C15				
-	-	-	C23,C24				
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-	-	-	D23,D24				
-	-	-	F3,F24				
-	-	-	G3,G24				

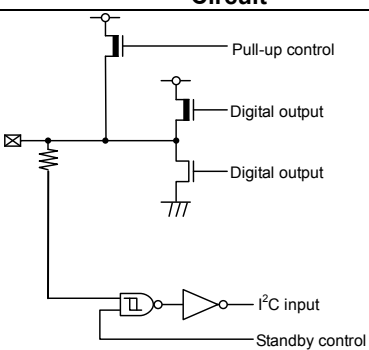
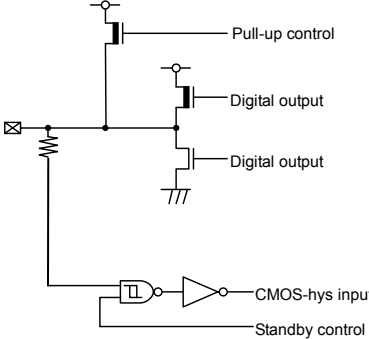
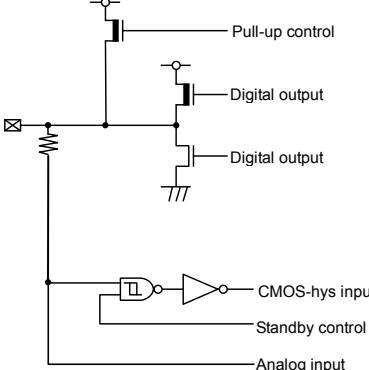
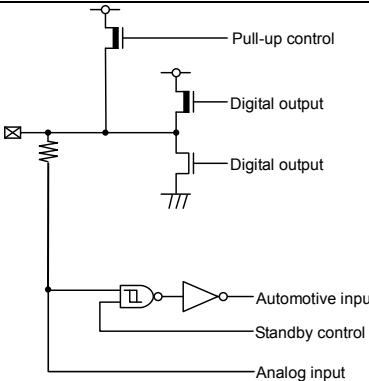
Pin Number				Pin Name	Polarity	I/O circuit type*1	Function*2
144	176	208	PAB 416				
-	-	-	H2,H3	VSS	-	-	GND
-	-	-	J24				
-	-	-	K10-K17				
-	-	-	K24				
-	-	-	L10-L17				
-	-	-	M10-M17				
-	-	-	M23,M24				
-	-	-	N1-N4				
-	-	-	N10-N17				
-	-	-	N24				
-	-	-	P3,P4				
-	-	-	P10-P17				
-	-	-	R10-R17				
-	-	-	R24				
-	-	-	T3				
-	-	-	T10-T17				
-	-	-	T24				
-	-	-	U3				
-	-	-	U10-U17				
-	-	-	V24				
-	-	-	W3,W24				
-	-	-	Y3				
-	-	-	AA24				
-	-	-	AC3,AC4				
-	-	-	AC9,AC23				
-	-	-	AD3,AD4				
-	-	-	AD7,AD9				
-	-	-	AD12,AD13				
-	-	-	AD15,AD16				
-	-	-	AD18,AD19				
-	-	-	AD21,AD22				
-	-	-	AD24				
-	-	-	AE1,AE26				
-	-	-	AF2,AF25				

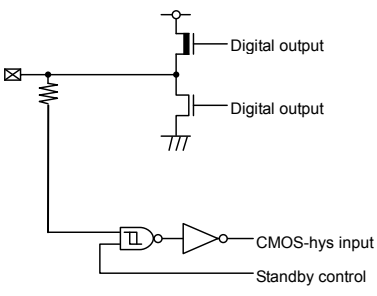
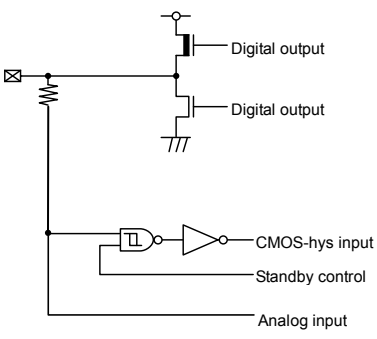
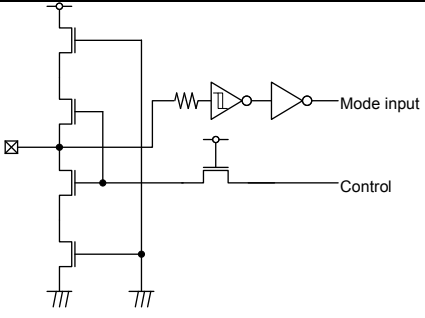
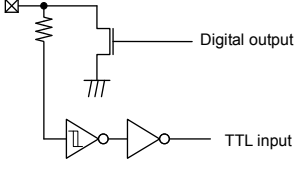
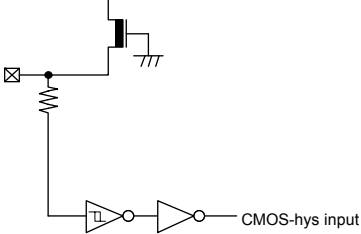
*1: For the I/O circuit types, see "4. I/O CIRCUIT TYPE".

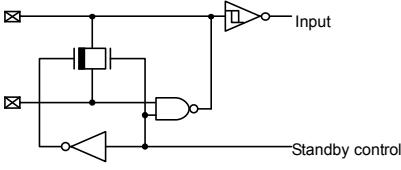
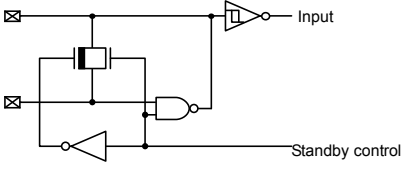
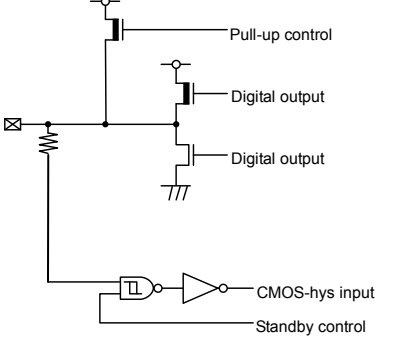
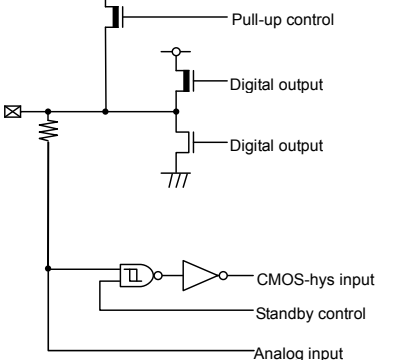
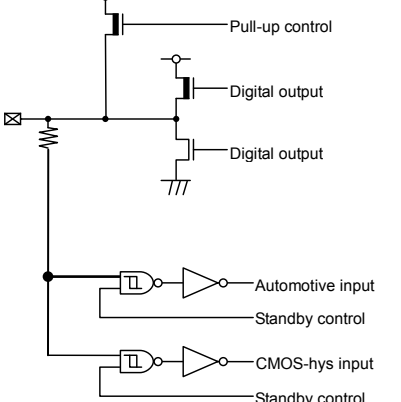
*2: For switching, see "I/O Port" in HARDWARE MANUAL.

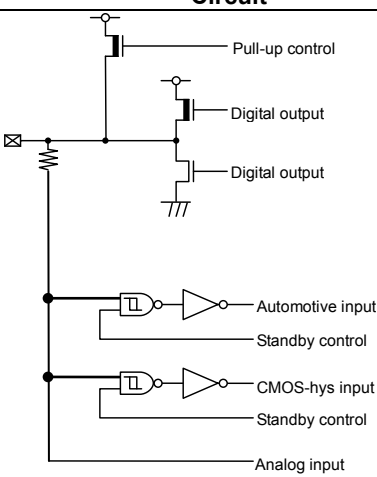
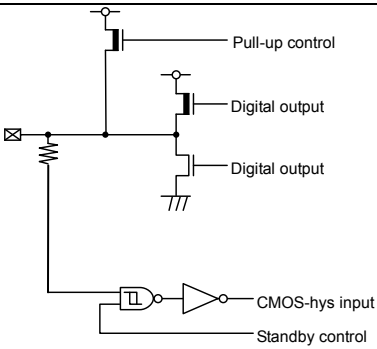
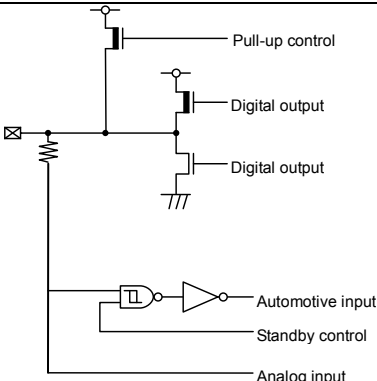
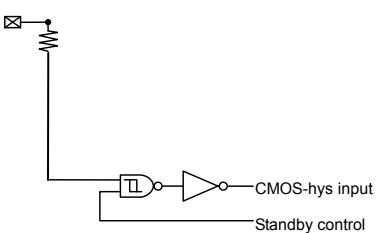
4. I/O Circuit Type

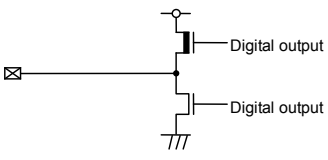
Type	Circuit	Remarks
A	 <p>Pull-up control</p> <p>Digital output</p> <p>Digital output</p> <p>Automotive input</p> <p>Standby control</p>	<ul style="list-style-type: none"> - General-purpose I/O port - Output 4mA - Pull-up resistor control 50kΩ - Automotive input
B	 <p>Pull-up control</p> <p>Digital output</p> <p>Digital output</p> <p>Automotive input</p> <p>Standby control</p> <p>Analog input</p>	<ul style="list-style-type: none"> - Analog input, General-purpose I/O port - Output 4mA - Pull-up resistor control 50kΩ - Automotive input
C	 <p>Pull-up control</p> <p>Digital output</p> <p>Digital output</p> <p>Automotive input</p> <p>Standby control</p> <p>DAC output</p>	<ul style="list-style-type: none"> - DAC output, General-purpose I/O port - Output 4mA - Pull-up resistor control 50kΩ - Automotive input
D	 <p>Pull-up control</p> <p>Digital output</p> <p>Digital output</p> <p>I²C input</p> <p>Standby control</p> <p>Analog input</p>	<ul style="list-style-type: none"> - I²C Analog input, General-purpose I/O port - Output 3mA - Pull-up resistor control 50kΩ - I²C hysteresis input

Type	Circuit	Remarks
E		<ul style="list-style-type: none"> - I²C, General-purpose I/O port - Output 3mA - Pull-up resistor control 50kΩ - I²C hysteresis input
F		<ul style="list-style-type: none"> - General-purpose I/O port - Output 4mA - Pull-up resistor control 50kΩ - CMOS hysteresis input
G		<ul style="list-style-type: none"> - Analog input, General-purpose I/O port - Output 4mA - Pull-up resistor control 50kΩ - CMOS hysteresis input
H		<ul style="list-style-type: none"> - Analog input, General-purpose I/O port - Output 12mA - Pull-up resistor control 50kΩ - Automotive input

Type	Circuit	Remarks
I		<ul style="list-style-type: none"> - General-purpose I/O port (5V tolerant) - Output 4mA - CMOS hysteresis input
J		<ul style="list-style-type: none"> - Analog input, General-purpose I/O port (5V tolerant) - Output 4mA - CMOS hysteresis input
K		<ul style="list-style-type: none"> - Mode I/O - CMOS hysteresis input
L		<ul style="list-style-type: none"> - Open-drain I/O - Output 25mA (Nch open drain) - TTL input
M		<ul style="list-style-type: none"> - Hysteresis input - Pull-up resistor 50k

Type	Circuit	Remarks
N		- Main oscillation I/O
O		- Sub oscillation I/O
P		<ul style="list-style-type: none"> - General-purpose I/O port - Output 4mA - Output 3mA (Nch open drain) - Pull-up resistor control 50kΩ - CMOS hysteresis input
Q		<ul style="list-style-type: none"> - Analog input, General-purpose I/O port - Output 4mA - Output 3mA (Nch open drain) - Pull-up resistor control 50kΩ - CMOS hysteresis input
R		<ul style="list-style-type: none"> - General-purpose I/O port - Output 4mA - Output 4mA (FlexRay output) - Pull-up resistor control 50kΩ - Automotive input - CMOS hysteresis input

Type	Circuit	Remarks
S		<ul style="list-style-type: none"> - Analog input, General-purpose I/O port - Output 4mA - Output 4mA (FlexRay output) - Pull-up resistor control 50kΩ - Automotive input - CMOS hysteresis input
T		<ul style="list-style-type: none"> - General-purpose I/O port - Output 4mA - Output 4mA (FlexRay output) - Pull-up resistor control 50kΩ - CMOS hysteresis input
U		<ul style="list-style-type: none"> - Analog input, General-purpose I/O port - Output 4mA - Output 4mA (FlexRay output) - Pull-up resistor control 50kΩ - Automotive input
V		<ul style="list-style-type: none"> - CMOS hysteresis input

Type	Circuit	Remarks
W	 <p>Digital output</p> <p>Digital output</p> <p>GND</p>	- Output 4mA

5. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device. Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNP junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

- (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
- (2) Be sure that abnormal current flows do not occur during the power-on sequence.

Code: DS00-00004-2Ea

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (PAB) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

- (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
- (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.

When you open Dry Package that recommends humidity 40% to 70% relative humidity.

- (3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
- (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

- (1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
- (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- (4) Ground all fixtures and instruments, or protect with anti-static measures.
- (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

- (1) Humidity
Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
- (2) Discharge of Static Electricity
When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
- (3) Corrosive Gases, Dust, or Oil
Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
- (4) Radiation, Including Cosmic Radiation
Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
- (5) Smoke, Flame
CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

6. Handling Devices

This section explains the latch-up prevention and pin processing.

■ For latch-up prevention

If a voltage higher than V_{CC} (V_{CCE} in case of terminal corresponding to V_{CCE} power supply.) or a voltage lower than V_{SS} is applied to an I/O pin, or if a voltage exceeding the ratings is applied between V_{CC} and V_{SS} pins or V_{CCE} and V_{SS} pins, a latch-up may occur in CMOS IC. If the latch-up occurs, the power supply current increases excessively and device elements may be damaged by heat. Take care to prevent any voltage from exceeding the maximum ratings in device application.

Also, the analog power supply (AV_{CC} , $AVRH$), analog input and digital power supply (V_{CCE}) must not be exceed the digital power supply (V_{CC}) when the power supply to the analog system and digital power supply (V_{CCE}) are turned on or off.

In the correct power-on sequence of the microcontroller, turn on the digital power supply (V_{CC}), analog power supplies (AV_{CC} , $AVRH$) and digital power supply (V_{CCE}) simultaneously. Or, turn on the digital power supply (V_{CC}), and then turn on analog power supplies (AV_{CC} , $AVRH$) and digital power supply (V_{CCE}).

■ Treatment of unused pins

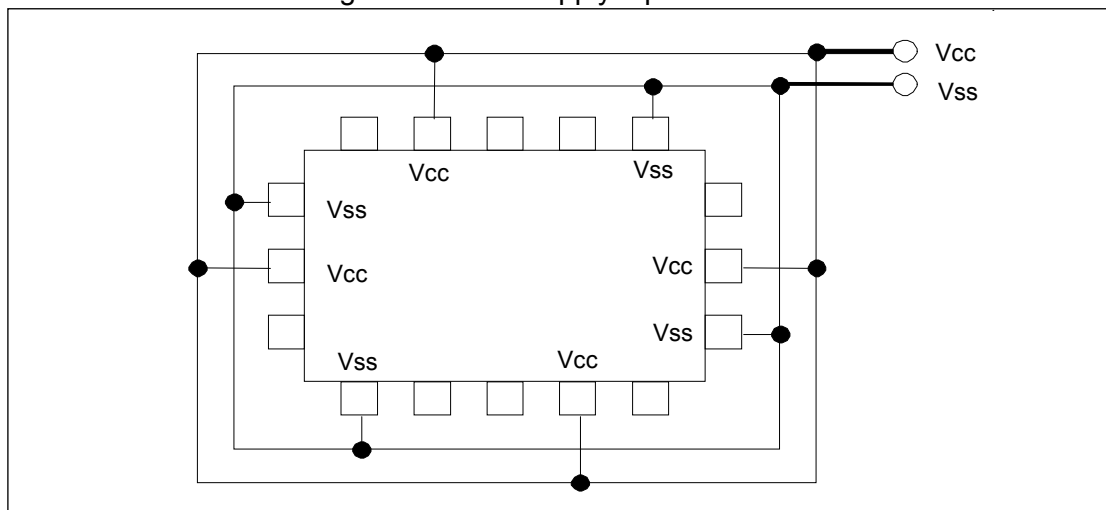
If unused input pins are left open, they may cause a permanent damage to the device due to malfunction or latch-up. Connect at least a 2k Ω resistor to each of the unused pins for pull-up or pull-down processing.

Also, if I/O pins are not used, they must be set to the output state for releasing or they must be set to the input state and treated in the same way as for the input pins.

■ Power supply pins

The device is designed to ensure that if the device contains multiple V_{CC} or V_{SS} pins, the pins that should be at the same potential are interconnected to prevent latch-up or other malfunctions. Further, connect these pins to an external power supply or ground to reduce unwanted radiation, prevent strobe signals from malfunctioning due to a raised ground level, and fulfill the total output current standard, etc. As shown in figure 1, all V_{SS} power supply pins must be treated in the similar way. If multiple V_{CC} or V_{SS} systems are connected, the device cannot operate correctly even within the guaranteed operating range.

Figure 1 Power Supply Input Pins



The power supply pins should be connected to V_{CC} and V_{SS} pins of this device at the low impedance from the power supply source.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between V_{CC} and V_{SS} pins.

■ **Crystal oscillation circuit**

An external noise to the X0 or X1 pin may cause a device malfunction. The printed circuit board must be designed to lay out X0 and X1 pins, crystal oscillator (or ceramic resonator), and the bypass capacitor to be grounded to the close position to the device.

The printed circuit board artwork is recommended to surround the X0 and X1 pins by ground circuits.

■ **Mode pins (MD1, MD0)**

Connect the MD1 and MD0 mode pins to the V_{CC} or V_{SS} pin directly. To prevent an erroneous selection of test mode caused by the noise, reduce the pattern length between each mode pin and V_{CC} or V_{SS} pin on the printed circuit board. Also, use the low-impedance pin connection.

■ **During power-on**

To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic during power-on.

■ **Notes during PLL clock operation**

When the PLL clock is selected and if the oscillator is disconnected or if the input is stopped, this clock may continue to operate at the free running frequency of the self-oscillator circuit built in the PLL clock. This operation is not guaranteed.

■ **Treatment of A/D converter power supply pins**

Connect the pins to have $AV_{CC}=AVRH=V_{CC}$ and $AV_{SS}/AVRL=V_{SS}$ even if the A/D converter is not used.

■ **Notes on using external clock**

An external clock is not supported. None of the external direct clock input can be used for both main clock and sub clock.

■ **Power-on sequence of A/D converter analog inputs**

Be sure to turn on the digital power supply (V_{CC} , V_{CCE}) first, and then turn on the A/D converter power supplies (AV_{CC} , $AVRH$, $AVRL$) and analog inputs ($AN0$ to $AN63$). Also, turn off the A/D converter power supplies and analog inputs first, and then turn off the digital power supply (V_{CC} , V_{CCE}). When the $AVRH$ pin voltage is turned on or off, it must not exceed AV_{CC} . Even if a common analog input pin is used as an input port, its input voltage must not exceed AV_{CC} . (However, the analog power supply and digital power supply can be turned on or off simultaneously.)

■ **Treatment of C pin**

This device contains a voltage step-down circuit. A capacitor must always be connected to the C pin to assure the internal stabilization of the device. For the standard values, see the "Recommended Operating Conditions" of the latest data sheet.

Note: Please see the latest data sheet for a detailed specification of the operation voltage.

■ **Function switching of a multiplexed port**

To switch between the port function and the multiplexed pin function, use the PFR (port function register). However, if a pin is also used for an external bus, its function is switched by the external bus setting. For details, see "I/O PORTS" in the hardware manual.

■ **Low-power consumption mode**

To transit to the sleep mode, watch mode, stop mode, watch mode(power-off) or stop mode(power-off), follow the procedure explained in "Activating the sleep mode, watch mode, or stop mode" or "Activating the watch mode (power-off) or stop mode(power-off)" of "POWER CONSUMPTION CONTROL" in the hardware manual.

Take the following notes when using a monitor debugger.

Do not set a break point for the low-power consumption transition program.

Do not execute an operation step for the low-power consumption transition program.

■ **Notes When Writing Data in a Register Having the Status Flag**

When writing data in the register that has a status flag (especially, an interrupt request flag) to control function, taking care not to clear its status flag erroneously must be followed.

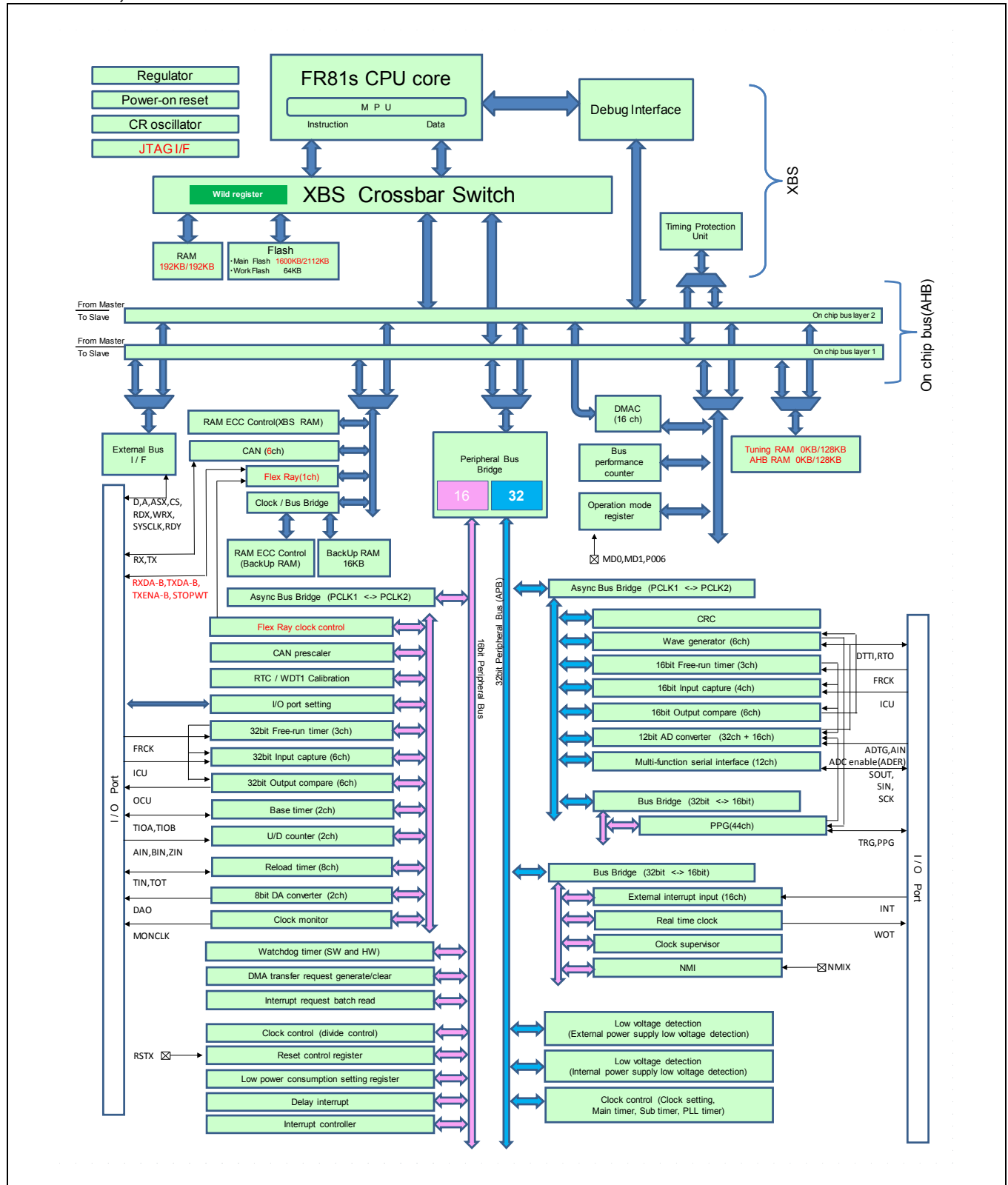
The program must be written not to clear the flag to the status bit, and then to set the control bits to have the desired value.

Especially, if multiple control bits are used, the bit instruction cannot be used. (The bit instruction can access to a single bit only.) By the Byte, Half-word, or Word access, data is written to the control bits and status flag simultaneously. During this time, take care not to clear other bits (in this case, the bits of status flag) erroneously.

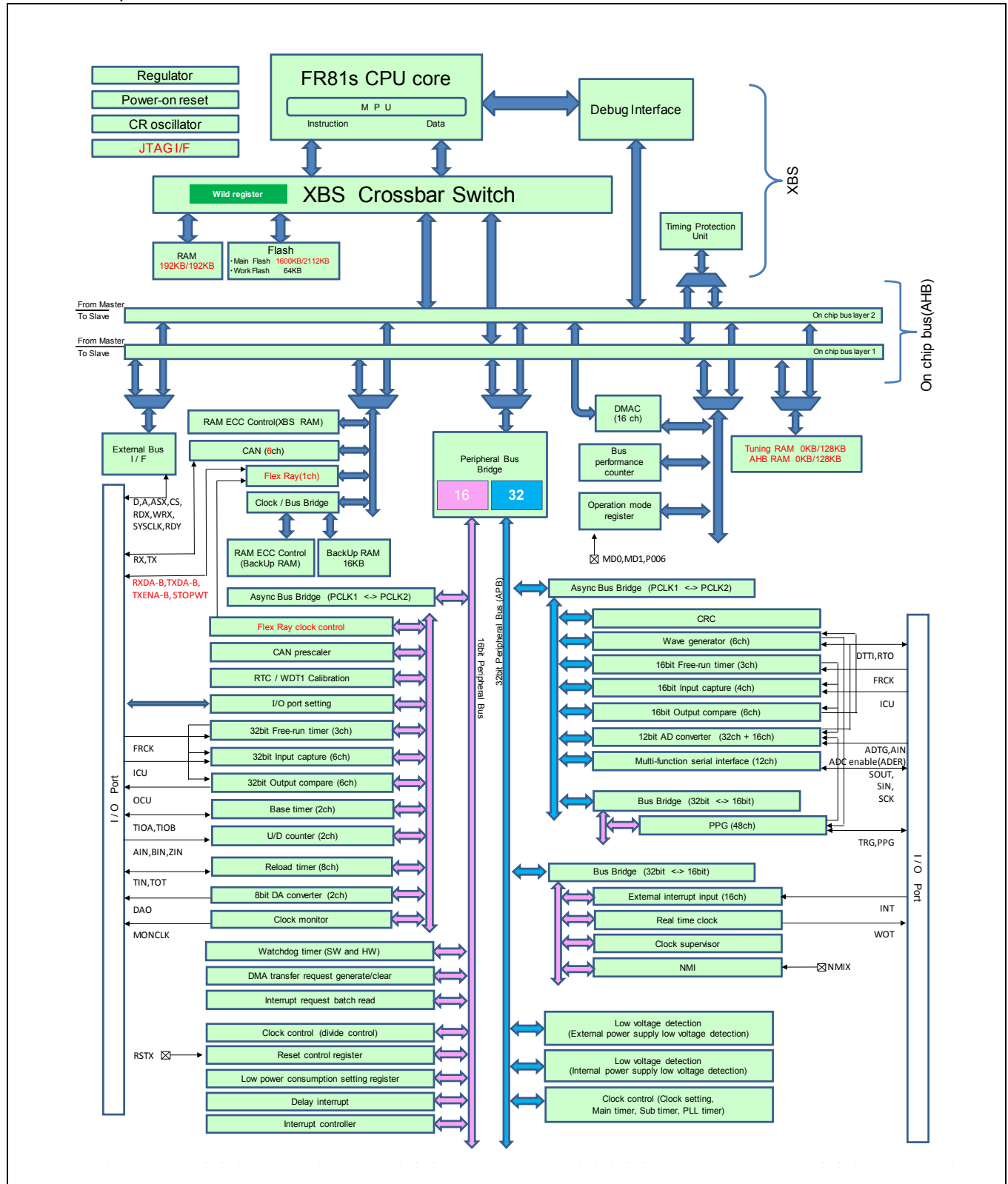
Note: These points can be ignored because the bit instructions are already taken the points into consideration.

7. Block Diagram

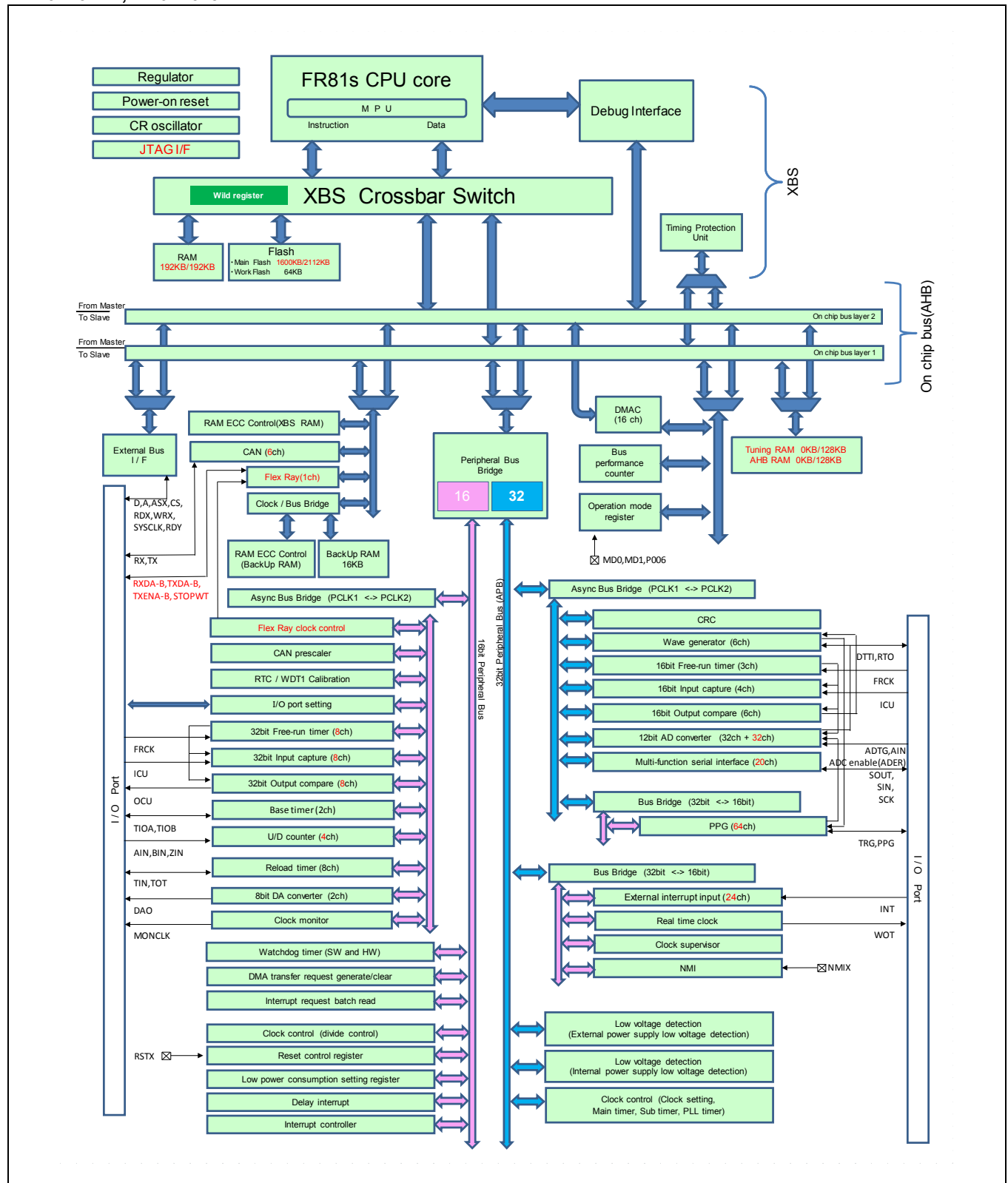
MB91F527R, MB91F528R



MB91F527U, MB91F528U



MB91F527M, MB91F528M





The diagram illustrates the system architecture of the FR81s CPU core. At the top, the **FR81s CPU core** (containing **M P U**) is connected to a **Regulator**, **Power-on reset**, **CR oscillator**, and **JTAG I/F**. It also interfaces with a **Debug Interface** and a **Timing Protection Unit**. The core is connected to an **XBS Crossbar Switch**, which manages data flow between the CPU, **RAM** (192KB/192KB), **Flash** (Main Flash 1600KB/2112KB, Work Flash 64KB), and various peripheral controllers. The system is organized into two main bus layers: **On chip bus layer 1** and **On chip bus layer 2**, collectively forming the **On chip bus(AHB)**. Key components include:

- External Bus I/F**: Handles signals like D, A, ASX, CS, RDX, WRX, SYSCLK, RDY, RX, TX, RXDA-B, TXDA-B, TXENA-B, STOPWT.
- Peripheral Bus Bridge**: A 16/32-bit bridge connecting the internal bus to a 16-bit Peripheral Bus.
- Async Bus Bridge**: Connects the Peripheral Bus to various peripheral modules.
- Peripheral Modules**:
 - Left Column**: CAN (6ch), Flex Ray (1ch), Clock / Bus Bridge, RAM ECC Control (BackUp RAM), BackUp RAM (16KB), Async Bus Bridge (PCLK1 <-> PCLK2), Flex Ray clock control, CAN prescaler, RTC / WDT1 Calibration, I/O port setting, 32bit Free-run timer (8ch), 32bit Input capture (8ch), 32bit Output compare (8ch), Base timer (2ch), U/D counter (4ch), Reload timer (8ch), 8bit DA converter (2ch), Clock monitor, Watchdog timer (SW and HW), DMA transfer request generate/clear, Interrupt request batch read, Clock control (divide control), Reset control register, Low power consumption setting register, Delay interrupt, and Interrupt controller.
 - Right Column**: DMAC (16 ch), Bus performance counter, Operation mode register (MD0, MD1, P006), Async Bus Bridge (PCLK1 <-> PCLK2), CRC, Wave generator (6ch), 16bit Free-run timer (3ch), 16bit Input capture (4ch), 16bit Output compare (6ch), 12bit AD converter (32ch + 32ch), Multi-function serial interface (20ch), Bus Bridge (32bit <-> 16bit), PPG (88ch), Bus Bridge (32bit <-> 16bit), External interrupt input (24ch), Real time clock, Clock supervisor, NMI, Low voltage detection (External power supply low voltage detection), Low voltage detection (Internal power supply low voltage detection), and Clock control (Clock setting, Main timer, Sub timer, PLL timer).
- Other Components**: Tuning RAM (0KB/128KB), AHB RAM (0KB/128KB), and various I/O ports (DTTI, RTO, FRCK, ICU, ADTG, AIN, ADC enable (ADER), SOUT, SIN, SCK, TRG, PPG, INT, WOT, NMIX).

8. Memory Map

MB91F527, MB91F528

MB91F527			[Tuning RAM function not used] MB91F528			[Tuning RAM function used] MB91F528							
0000	0000	H	I/O	0000	0000	H	I/O	0000	0000	H	I/O		
0000	4000	H	BackUp RAM(16KB)	0000	4000	H	BackUp RAM(16KB)	0000	4000	H	BackUp RAM(16KB)		
0000	8000	H	I/O	0000	8000	H	I/O	0000	8000	H	I/O		
0001	0000	H	RAM(192KB)	0001	0000	H	RAM(192KB)	0001	0000	H	RAM(192KB)		
0004	0000	H	Reserved	0004	0000	H	Reserved	0004	0000	H	Reserved		
0007	0000	H	Flash Memory (1536+64)KB	0007	0000	H	Flash Memory (2048+64)KB	0007	0000	H	Flash Memory (2048+64)KB		
									0008	0000	H	Tuning Area (128KB)	
									000A	0000	H	Tuning Area (128KB)	
									000C	0000	H		
000F	FC00	H	Interrupt Vector Reset Vector	000F	FC00	H	Interrupt Vector Reset Vector	000F	FC00	H	Interrupt Vector Reset Vector		
0010	0000	H		0010	0000	H		0010	0000	H			
0020	0000	H	Reserved	0028	0000	H	Reserved	0028	0000	H	Reserved		
0033	0000	H	Work Flash (64KB)	0033	0000	H	Work Flash (64KB)	0033	0000	H	Work Flash (64KB)		
0034	0000	H	Reserved	0034	0000	H	Reserved	0034	0000	H	Reserved		
						7FFE	0000	H	RAM (128KB)	7FFE	0000	H	Tuning RAM (128KB) Mirror region of Tuning Area
8000	0000	H	External Area	8000	0000	H	External Area	8000	0000	H	External Area		
FFFF	FFFF	H		FFFF	FFFF	H		FFFF	FFFF	H			

Register switching

Register switching

9. I/O Map

The following I/O map shows the relationship between memory space and registers for peripheral resources.

Legend of I/O Map

Address	Address offset value/ register name				Block
	+0	+1	+2	+3	
000090 _H	BT1TMR[R] H 0000000000000000		BT1TMCR[R/W]B,H,W 00000000 00000000		Base timer 1
000094 _H	-	BT1STC[R/W] B 00000000	-	-	
000098 _H	BT1PCSR/BT1PRLL[R /W] H 0000000000000000		BT1PDU T/BT1PRLH/BT1DTBF[R/W] H 0000000000000000		
00009C _H	BTSEL[R/W] B ----000 0	-	BTSSSR[W] B,H -----11		
0000A0 _H	ADERH [R/W]B, H, W 00000000 00000000		ADERL [R/W]B, H, W 00000000 00000000		A/D converter
0000A4 _H	ADCS1 [R/W] B, H,W 00000000	ADCS0 [R/W] B, H,W 00000000	ADCR1 [R] B, H,W -----XX	ADCR0 [R] B, H,W XXXXX XXX	
0000A8 _H	ADCT1 [R/W] B, H,W 00010000	ADCT0 [R/W] B, H,W 00101100	ADSCH [R/W] B, H,W ---00000	ADECH [R/W] B, H,W ---00000	

Read/Write attribute (R: Read W: Write)

Initial register value after reset

Data access attribute
B: Byte
H: Half-word
W: Word
(Note)The access by the data
access attribute not described
is disabled.

The initial register value after reset indicates as follows:

- "1": Initial value "1"
- "0": Initial value "0"
- "X": Initial value undefined
- "-": Reserved bit/Undefined bit
- "**": Initial value "0" or "1" according to the setting

Note: The access to addresses not described is disabled.

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000000 _H	PDR00 [R/W] B,H,W XXXXXXXXXX	PDR01 [R/W] B,H,W XXXXXXXXXX	PDR02 [R/W] B,H,W XXXXXXXXXX	PDR03 [R/W] B,H,W XXXXXXXXXX	Port Data Register
000004 _H	PDR04 [R/W] B,H,W XXXXXXXXXX	PDR05 [R/W] B,H,W XXXXXXXXXX	PDR06 [R/W] B,H,W XXXXXXXXXX	PDR07 [R/W] B,H,W XXXXXXXXXX	
000008 _H	PDR08 [R/W] B,H,W XXXXXXXXXX	PDR09 [R/W] B,H,W XXXXXXXXXX	PDR10 [R/W] B,H,W XXXXXXXXXX	PDR11 [R/W] B,H,W XXXXXXXXXX	
00000C _H	PDR12 [R/W] B,H,W XXXXXXXXXX	PDR13 [R/W] B,H,W -XXX--XX	PDR14 [R/W] B,H,W -----	PDR15 [R/W] B,H,W --XXXXXX	
000010 _H	PDR20 [R/W] B,H,W XXXXXXXXXX	PDR21 [R/W] B,H,W XXXXXXXXXX	PDR22 [R/W] B,H,W XXX--XXX	PDR23 [R/W] B,H,W XXXXXXXXXX	
000014 _H	PDR24 [R/W] B,H,W --XXXXXX	PDR25 [R/W] B,H,W -XXXXXXX	PDR26 [R/W] B,H,W XXXXXX--	PDR27 [R/W] B,H,W XXX-XXXX	
000018 _H	PDR16 [R/W] B,H,W XXXXXXXXXX	PDR17 [R/W] B,H,W XXXXXXXXXX	PDR18 [R/W] B,H,W XXXXXXXXXX	PDR19 [R/W] B,H,W XXXXXXXXXX	
00001C _H	PDR28 [R/W] B,H,W XXXXXXXXXX	PDR29 [R/W] B,H,W XXXXXXXXXX	—	—	
000020 _H	MSCY10 [R] H,W XXXXXXXXXX XXXXXXXXXX XXXXXXXXXX XXXXXXXXXX				Input Capture 10,11 32-bit ICU
000024 _H	MSCY11 [R] H,W XXXXXXXXXX XXXXXXXXXX XXXXXXXXXX XXXXXXXXXX				
000028 _H	—	—	MSCH1011 [R] B,H,W 00000000	MSCL1011 [R/W] B,H,W -----00	
00002C _H	IPCP10 [R] W XXXXXXXXXX XXXXXXXXXX XXXXXXXXXX XXXXXXXXXX				
000030 _H	IPCP11 [R] W XXXXXXXXXX XXXXXXXXXX XXXXXXXXXX XXXXXXXXXX				
000034 _H	—	—	—	ICS1011 [R/W] B,H,W 00000000	
000038 _H	WDTECR0 [R/W] B,H,W ---00000	—	—	—	Watchdog Timer [S]
00003C _H	WDTCR0 [R/W] B,H,W -0--0000	WDTCPR0 [W] B,H,W 00000000	WDTCR1 [R] B,H,W ----0110	WDTCPR1 [W] B,H,W 00000000	
000040 _H	—	—	—	—	Reserved
000044 _H	DICR [R/W] B -----0	—	—	—	Delayed Interrupt
000048 _H to 00005C _H	—	—	—	—	Reserved
000060 _H	TMRLRA0 [R/W] H XXXXXXXXXX XXXXXXXXXX		TMR0 [R] H XXXXXXXXXX XXXXXXXXXX		Reload Timer 0
000064 _H	TMRLRB0 [R/W] H XXXXXXXXXX XXXXXXXXXX		TMCSR0 [R/W] B,H,W 00000000 0-000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000068 _H	TMRLRA7 [R/W] H XXXXXXXX XXXXXXXX		TMR7 [R] H XXXXXXXX XXXXXXXX		Reload Timer 7
00006C _H	TMRLRB7 [R/W] H XXXXXXXX XXXXXXXX		TMCSR7 [R/W] B,H,W 00000000 0-000000		
000070 _H	FRS8 [R/W] B,H,W -000-000 -000-000 -000-000 -000-000				Free-run timer selection register 8
000074 _H	FRS9 [R/W] B,H,W -000-000 -000-000 -000-000 -000-000				Free-run timer selection register 9
000078 _H	—	—	—	OCLS67 [R/W] B,H,W ----0000	OCU67 Output level control register
00007C _H	—	—	—	OCLS89 [R/W] B,H,W ----0000	OCU89 Output level control register
000080 _H	BT0TMR [R] H 00000000 00000000		BT0TMCR [R/W] H -000--00 -000-000		Base Timer 0
000084 _H	BT0TMCR2 [R/W] B -----0	BT0STC [R/W] B -0-0-0-0	—	—	
000088 _H	BT0PCSR/BT0PRL [R/W] H 00000000 00000000		BT0PDUT/BT0PRLH/BT0DTBF [R/W] H 00000000 00000000		
00008C _H	—	—	—	—	Reserved
000090 _H	BT1TMR [R] H 00000000 00000000		BT1TMCR [R/W] H -000--00 -000-000		Base Timer 1
000094 _H	BT1TMCR2 [R/W] B -----0	BT1STC [R/W] B -0-0-0-0	—	—	
000098 _H	BT1PCSR/BT1PRL [R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H 00000000 00000000		
00009C _H	BTSEL01 [R/W] B ----0000	—	BTSSSR [W] B,H -----11		Base Timer 0,1
0000A0 _H to 0000FC _H	—	—	—	—	Reserved
000100 _H	TMRLRA1 [R/W] H XXXXXXXX XXXXXXXX		TMR1 [R] H XXXXXXXX XXXXXXXX		Reload Timer 1
000104 _H	TMRLRB1 [R/W] H XXXXXXXX XXXXXXXX		TMCSR1 [R/W] B, H,W 00000000 0-000000		
000108 _H	TMRLRA2 [R/W] H XXXXXXXX XXXXXXXX		TMR2 [R] H XXXXXXXX XXXXXXXX		Reload Timer 2
00010C _H	TMRLRB2 [R/W] H XXXXXXXX XXXXXXXX		TMCSR2 [R/W] B,H,W 00000000 0-000000		
000110 _H	TMRLRA3 [R/W] H XXXXXXXX XXXXXXXX		TMR3 [R] H XXXXXXXX XXXXXXXX		Reload Timer 3
000114 _H	TMRLRB3 [R/W] H XXXXXXXX XXXXXXXX		TMCSR3 [R/W] B,H,W 00000000 0-000000		
000118 _H	MSCY4 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 4,5 Cycle measurement data register 45
00011C _H	MSCY5 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000120 _H	OCCP6 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 6,7 32-bit OCU
000124 _H	OCCP7 [R/W] W 00000000 00000000 00000000 00000000				
000128 _H	—	—	OCSH67 [R/W] B,H,W ---0--00	OCSL67 [R/W] B,H,W 0000--00	
00012C _H	OCCP8 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 8,9 32-bit OCU
000130 _H	OCCP9 [R/W] W 00000000 00000000 00000000 00000000				
000134 _H	—	—	OCSH89 [R/W] B,H,W ---0--00	OCSL89 [R/W] B,H,W 0000--00	
000138 _H	OCCP12 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 12,13 32-bit OCU
00013C _H	OCCP13 [R/W] W 00000000 00000000 00000000 00000000				
000140 _H	—	—	OCSH1213 [R/W] B,H,W ---0--00	OCSL1213 [R/W] B,H,W 0000--00	
000144 _H to 0001B4 _H	—	—	—	—	Reserved
0001B8 _H	EPFR64 [R/W] B,H,W ----00-	EPFR65 [R/W] B,H,W 0000-00-	EPFR66 [R/W] B,H,W --000000	EPFR67 [R/W] B,H,W ----0000	Extended port function register
0001BC _H	EPFR68 [R/W] B,H,W ----0000	EPFR69 [R/W] B,H,W ----0000	EPFR70 [R/W] B,H,W ---00000	EPFR71 [R/W] B,H,W -0-0-0-0	
0001C0 _H	EPFR72 [R/W] B,H,W 000000-0	EPFR73 [R/W] B,H,W 00000000	EPFR74 [R/W] B,H,W 00000000	EPFR75 [R/W] B,H,W 00000000	
0001C4 _H	EPFR76 [R/W] B,H,W 00000-0-	EPFR77 [R/W] B,H,W --000000	EPFR78 [R/W] B,H,W -----00	EPFR79 [R/W] B,H,W 00000000	
0001C8 _H	EPFR80 [R/W] B,H,W ---00000	EPFR81 [R/W] B,H,W 00000000	EPFR82 [R/W] B,H,W 00000000	EPFR83 [R/W] B,H,W -0000000	
0001CC _H	EPFR84 [R/W] B,H,W 00000000	EPFR85 [R/W] B,H,W --000000	EPFR86 [R/W] B,H,W ---00000	EPFR87 [R/W] B,H,W -----	
0001D0 _H	EPFR88 [R/W] B,H,W -----0	EPFR89 [R/W] B,H,W -0-00000	EPFR90 [R/W] B,H,W -0-0-0-0	EPFR91 [R/W] B,H,W -0-0-0-0	
0001D4 _H	EPFR92 [R/W] B,H,W -0-0-0-0	EPFR93 [R/W] B,H,W 00000000	EPFR94 [R/W] B,H,W -0-0-0-0	EPFR95 [R/W] B,H,W -0-0-0-0	
0001D8 _H	TMRLRA4 [R/W] H XXXXXXXXXX XXXXXXXXX		TMR4 [R] H XXXXXXXXXX XXXXXXXXX		Reload Timer 4

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0001DC _H	TMRLRB4 [R/W] H XXXXXXXX XXXXXXXX		TMCSR4 [R/W] B, H,W 00000000 0-000000		Reload Timer 4
0001E0 _H	EPFR96 [R/W] B,H,W -0-0-0-0	EPFR97 [R/W] B,H,W -0-0-0-0	EPFR98 [R/W] B,H,W 0000-0-0	EPFR99 [R/W] B,H,W ----0000	Extended port function register
0001E4 _H	EPFR100 [R/W] B,H,W ----00-	EPFR101 [R/W] B,H,W ----00-	EPFR102 [R/W] B,H,W ----00-	EPFR103 [R/W] B,H,W ----00-	
0001E8 _H	EPFR104 [R/W] B,H,W ----00-	EPFR105 [R/W] B,H,W ----00-	EPFR106 [R/W] B,H,W ----00-	EPFR107 [R/W] B,H,W ----00-	
0001EC _H	EPFR108 [R/W] B,H,W ---00000	EPFR109 [R/W] B,H,W --000000	EPFR110 [R/W] B,H,W --000000	EPFR111 [R/W] B,H,W -----0	
0001F0 _H	TMRLRA5 [R/W] H XXXXXXXX XXXXXXXX		TMR5 [R] H XXXXXXXX XXXXXXXX		
0001F4 _H	TMRLRB5 [R/W] H XXXXXXXX XXXXXXXX		TMCSR5 [R/W] B, H,W 00000000 0-000000		
0001F8 _H	TMRLRA6 [R/W] H XXXXXXXX XXXXXXXX		TMR6 [R] H XXXXXXXX XXXXXXXX		Reload Timer 6
0001FC _H	TMRLRB6 [R/W] H XXXXXXXX XXXXXXXX		TMCSR6 [R/W] B, H,W 00000000 0-000000		
000200 _H to 000238 _H	—	—	—	—	Reserved
00023C _H	DACR0 [R/W] B,H,W -----0	DADR0 [R/W] B,H,W XXXXXXXX	DACR1 [R/W] B,H,W -----0	DADR1 [R/W] B,H,W XXXXXXXX	DA Converter
000240 _H	CPCLR3 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 3 32-bit FRT
000244 _H	TCDT3 [R/W] W 00000000 00000000 00000000 00000000				
000248 _H	TCCSH3 [R/W] B,H,W 0-----00	TCCSL3 [R/W] B,H,W -1-00000	—	—	
00024C _H	CPCLR4 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 4 32-bit FRT
000250 _H	TCDT4 [R/W] W 00000000 00000000 00000000 00000000				
000254 _H	TCCSH4 [R/W] B,H,W 0-----00	TCCSL4 [R/W] B,H,W -1-00000	—	—	
000258 _H to 0002C0 _H	—	—	—	—	Reserved
0002C4 _H to 0002FC _H	—	—	—	—	Reserved
000300 _H to 00030C _H	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000310 _H	—	—	MPUCR [R/W] H 000000-0 ----0100		MPU [S] (Only CPU core can access this area)
000314 _H	—	—	—	—	
000318 _H	—				
00031C _H	—	—	—		
000320 _H	DPVAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000324 _H	—	—	DPVSR [R/W] H ----- 00000--0		
000328 _H	DEAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00032C _H	—	—	DESR [R/W] H ----- 00000--0		
000330 _H	PABR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000334 _H	—	—	PACR0 [R/W] H 000000-0 00000--0		
000338 _H	PABR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00033C _H	—	—	PACR1 [R/W] H 000000-0 00000--0		
000340 _H	PABR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000344 _H	—	—	PACR2 [R/W] H 000000-0 00000--0		
000348 _H	PABR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				MPU [S] (Only CPU core can access this area)
00034C _H	—	—	PACR3 [R/W] H 000000-0 00000--0		
000350 _H	PABR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000354 _H	—	—	PACR4 [R/W] H 000000-0 00000--0		
000358 _H	PABR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00035C _H	—	—	PACR5 [R/W] H 000000-0 00000--0		
000360 _H	PABR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000364 _H	—	—	PACR6 [R/W] H 000000-0 00000--0		
000368 _H	PABR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00036C _H	—	—	PACR7 [R/W] H 000000-0 00000--0		
000370 _H to 0003AC _H	—				Reserved [S]

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0003B0 _H to 0003FC _H	—	—	—	—	Reserved [S]
000400 _H	ICSEL0 [R/W] B,H,W -----000	ICSEL1 [R/W] B,H,W ----0000	ICSEL2 [R/W] B,H,W -----0	ICSEL3 [R/W] B,H,W -----0	DMA request generation and clear
000404 _H	ICSEL4 [R/W] B,H,W -----0	ICSEL5 [R/W] B,H,W ----000	ICSEL6 [R/W] B,H,W ----0000	ICSEL7 [R/W] B,H,W ----0000	
000408 _H	ICSEL8 [R/W] B,H,W -----00	ICSEL9 [R/W] B,H,W -----00	ICSEL10 [R/W] B,H,W -----00	ICSEL11 [R/W] B,H,W -----00	
00040C _H	ICSEL12 [R/W] B,H,W -----0	ICSEL13 [R/W] B,H,W -----00	ICSEL14 [R/W] B,H,W -----00	ICSEL15 [R/W] B,H,W -----00	
000410 _H	ICSEL16 [R/W] B,H,W ---0000	ICSEL17 [R/W] B,H,W -----00	ICSEL18 [R/W] B,H,W --000000	ICSEL19 [R/W] B,H,W ----000	
000414 _H	ICSEL20 [R/W] B,H,W ----000	ICSEL21 [R/W] B,H,W -----00	ICSEL22 [R/W] B,H,W -----00	ICSEL23 [R/W] B,H,W -----00	
000418 _H	IRPR0H [R] B,H,W 00-----	IRPR0L [R] B,H,W 00-----	IRPR1H [R] B,H,W 00-----	IRPR1L [R] B,H,W 00-----	Interrupt Request Batch Reading Register
00041C _H	—	—	IRPR3H [R] B,H,W 000000--	IRPR3L [R] B,H,W 000000--	
000420 _H	IRPR4H [R] B,H,W 0000----	IRPR4L [R] B,H,W 0000----	IRPR5H [R] B,H,W 0000----	IRPR5L [R] B,H,W 0000000-	
000424 _H	IRPR6H [R] B,H,W --00----	IRPR6L [R] B,H,W 0000----	IRPR7H [R] B,H,W -0-00---	IRPR7L [R] B,H,W -----00	
000428 _H	IRPR8H [R] B,H,W --0-----	IRPR8L [R] B,H,W -0-----	IRPR9H [R] B,H,W -0-----	IRPR9L [R] B,H,W -0-----	
00042C _H	IRPR10H [R] B,H,W -0-----	IRPR10L [R] B,H,W -0-----	IRPR11H [R] B,H,W 0-----	IRPR11L [R] B,H,W 0-----	
000430 _H	IRPR12H [R] B,H,W --0000--	IRPR12L [R] B,H,W ---00--	IRPR13H [R] B,H,W 00-----	IRPR13L [R] B,H,W 00-----	Interrupt Request Batch Reading Register
000434 _H	IRPR14H [R] B,H,W 00000000	IRPR14L [R] B,H,W 00000000	IRPR15H [R] B,H,W 000----	IRPR15L [R] B,H,W 00000000	
000438 _H	ICSEL24 [R/W] B,H,W -----00	ICSEL25 [R/W] B,H,W ---00000	ICSEL26 [R/W] B,H,W -----0	ICSEL27 [R/W] B,H,W -----0	DMA request generation and clear
00043C _H	IRPR16H [R] B,H,W 000-----	IRPR16L [R] B,H,W 00000---	IRPR17H [R] B,H,W 000-----	IRPR17L [R] B,H,W 000-----	Interrupt Request Batch Reading Register

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000440 _H	ICR00 [R/W] B,H,W ---11111	ICR01 [R/W] B,H,W ---11111	ICR02 [R/W] B,H,W ---11111	ICR03 [R/W] B,H,W ---11111	Interrupt Controller [S]
000444 _H	ICR04 [R/W] B,H,W ---11111	ICR05 [R/W] B,H,W ---11111	ICR06 [R/W] B,H,W ---11111	ICR07 [R/W] B,H,W ---11111	
000448 _H	ICR08 [R/W] B,H,W ---11111	ICR09 [R/W] B,H,W ---11111	ICR10 [R/W] B,H,W ---11111	ICR11 [R/W] B,H,W ---11111	
00044C _H	ICR12 [R/W] B,H,W ---11111	ICR13 [R/W] B,H,W ---11111	ICR14 [R/W] B,H,W ---11111	ICR15 [R/W] B,H,W ---11111	
000450 _H	ICR16 [R/W] B,H,W ---11111	ICR17 [R/W] B,H,W ---11111	ICR18 [R/W] B,H,W ---11111	ICR19 [R/W] B,H,W ---11111	
000454 _H	ICR20 [R/W] B,H,W ---11111	ICR21 [R/W] B,H,W ---11111	ICR22 [R/W] B,H,W ---11111	ICR23 [R/W] B,H,W ---11111	
000458 _H	ICR24 [R/W] B,H,W ---11111	ICR25 [R/W] B,H,W ---11111	ICR26 [R/W] B,H,W ---11111	ICR27 [R/W] B,H,W ---11111	
00045C _H	ICR28 [R/W] B,H,W ---11111	ICR29 [R/W] B,H,W ---11111	ICR30 [R/W] B,H,W ---11111	ICR31 [R/W] B,H,W ---11111	
000460 _H	ICR32 [R/W] B,H,W ---11111	ICR33 [R/W] B,H,W ---11111	ICR34 [R/W] B,H,W ---11111	ICR35 [R/W] B,H,W ---11111	
000464 _H	ICR36 [R/W] B,H,W ---11111	ICR37 [R/W] B,H,W ---11111	ICR38 [R/W] B,H,W ---11111	ICR39 [R/W] B,H,W ---11111	
000468 _H	ICR40 [R/W] B,H,W ---11111	ICR41 [R/W] B,H,W ---11111	ICR42 [R/W] B,H,W ---11111	ICR43 [R/W] B,H,W ---11111	
00046C _H	ICR44 [R/W] B,H,W ---11111	ICR45 [R/W] B,H,W ---11111	ICR46 [R/W] B,H,W ---11111	ICR47 [R/W] B,H,W ---11111	
000470 _H to 00047C _H	—	—	—	—	Reserved [S]
000480 _H	RSTRR [R] B,H,W XXXX--XX	RSTCR [R/W] B,H,W 111----0	STBCR [R/W] B,H,W * 000---11	—	Reset Control [S] Power Control [S] *: Writing STBCR by DMA is forbidden
000484 _H	—	—	—	—	Reserved [S]
000488 _H	DIVR0 [R/W] B,H,W 000-----	DIVR1 [R/W] B,H,W 0001----	DIVR2 [R/W] B,H,W 0011----	—	Clock Control [S]
00048C _H	—	—	—	—	Reserved [S]
000490 _H	IORR0 [R/W] B,H,W -0000000	IORR1 [R/W] B,H,W -0000000	IORR2 [R/W] B,H,W -0000000	IORR3 [R/W] B,H,W -0000000	DMA request by peripheral [S]
000494 _H	IORR4 [R/W] B,H,W -0000000	IORR5 [R/W] B,H,W -0000000	IORR6 [R/W] B,H,W -0000000	IORR7 [R/W] B,H,W -0000000	
000498 _H	IORR8 [R/W] B,H,W -0000000	IORR9 [R/W] B,H,W -0000000	IORR10 [R/W] B,H,W -0000000	IORR11 [R/W] B,H,W -0000000	
00049C _H	IORR12 [R/W] B,H,W -0000000	IORR13 [R/W] B,H,W -0000000	IORR14 [R/W] B,H,W -0000000	IORR15 [R/W] B,H,W -0000000	
0004A0 _H	—	—	—	—	Reserved
0004A4 _H	CANPRE [R/W] B,H,W ---00000	—	—	—	CAN prescaler
0004A8 _H	—	—	CSCFG [R/W] B,H,W ---0----	CMCFG [R/W] B,H,W 00000000	Clock monitor control register

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0004AC _H	ADERH0[R/W] B,H 11111111 11111111		ADERL0[R/W] B,H 11111111 11111111		Analog input control register 0
0004B0 _H	ADERH1[R/W] B,H 11111111 11111111		ADERL1[R/W] B,H 11111111 11111111		Analog input control register 1
0004B4 _H	—	—	—	—	Reserved
0004B8 _H	CUCR0 [R/W] B,H,W -----0--00		CUTD0 [R/W] B,H,W 10000000 00000000		RTC/WDT1 calibration
0004BC _H	CUTR0 [R] B,H,W -----00000000 00000000 00000000				
0004C0 _H	—	—	—	—	
0004C4 _H	CUCR1 [R/W] B,H,W -----0--00		CUTD1 [R/W] B,H,W 11000011 01010000		
0004C8 _H	CUTR1 [R] B,H,W -----00000000 00000000 00000000				
0004CC _H	—	—	—	—	Reserved
0004D0 _H	PLL2DIVM[R/W] B,H,W ----0000	PLL2DIVN[R/W] B,H,W -0000000	PLL2DIVG[R/W] B,H,W ----0000	PLL2MULG[R/W] B,H,W 00000000	Clock control for FlexRay
0004D4 _H	PLL2CTRL[R/W] B,H,W ----0000	PLL2DIVK[R/W] B,H,W -----0	CLKR2[R/W] B,H,W 000--000	—	
0004D8 _H	ICSEL28 [R/W] B,H,W -----0	ICSEL29 [R/W] B,H,W -----0	ICSEL30 [R/W] B,H,W -----0	ICSEL31 [R/W] B,H,W -----0	DMA request generation and clear
0004DC _H	ICSEL32 [R/W] B,H,W -----0	ICSEL33 [R/W] B,H,W -----0	—	—	
0004E0 _H to 00050C _H	—	—	—	—	Reserved
000510 _H	CSELR [R/W] B,H,W 001---00	CMONR [R] B,H,W 001---00	MTMCR [R/W] B,H,W 00001111	STMCR [R/W] B,H,W 0000-111	Clock Control [S]
000514 _H	PLLCR [R/W] B,H,W -----11110000		CSTBR [R/W] B,H,W -0000000	PTMCR [R/W] B,H,W 00-----	
000518 _H	—	—	CPUAR [R/W] B,H,W 0----XXX	—	Reset Control [S]
00051C _H	—	—	—	—	Reserved [S]
000520 _H	CCPSSELR [R/W] B,H,W -----0	—	—	CCPSDIVR [R/W] B,H,W -000-000	Clock Control 2 [S]
000524 _H	—	CCPLLFBR [R/W] B,H,W -0000000	CCSSFBR0 [R/W] B,H,W --000000	CCSSFBR1 [R/W] B,H,W ---00000	
000528 _H	—	CCSSCCR0 [R/W] B,H,W ----0000	CCSSCCR1 [R/W] H,W 000-----		
00052C _H	—	CCCGRCR0 [R/W] B,H,W 00----00	CCCGRCR1 [R/W] B,H,W 00000000	CCCGRCR2 [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000530 _H	CCRTSEL [R/W] B,H,W 0-----0	—	CCPMUCR0 [R/W] B,H,W 0-----00	CCPMUCR1 [R/W] B,H,W 0--00000	Clock Control 2 [S]
000534 _H to 00053C _H	—	—	—	—	Reserved
000540 _H	EIRR2 [R/W] B,H,W XXXXXXXX	ENIR2 [R/W] B,H,W 00000000	ELVR2 [R/W] B,H,W 00000000 00000000	External Interrupt (INT16 to 23)	
000544 _H to 00054C _H	—	—	—	—	Reserved
000550 _H	EIRR0 [R/W] B,H,W XXXXXXXX	ENIR0 [R/W] B,H,W 00000000	ELVR0 [R/W] B,H,W 00000000 00000000		External Interrupt (INT0 to 7)
000554 _H	EIRR1 [R/W] B,H,W XXXXXXXX	ENIR1 [R/W] B,H,W 00000000	ELVR1 [R/W] B,H,W 00000000 00000000		External Interrupt (INT8 to 15)
000558 _H	—	—	—	—	Reserved
00055C _H	—	—	WTDR [R/W] H 00000000 00000000		Real Time Clock (RTC)
000560 _H	—	WTCRH [R/W] B -----00	WTCRM [R/W] B,H 00000000	WTCRL [R/W] B,H ----00-0	
000564 _H	—	WTCRH [R/W] B --XXXXXX	WTCRM [R/W] B XXXXXXXXXX	WTCRL [R/W] B XXXXXXXXXX	
000568 _H	WTHR [R/W] B,H ---00000	WTMR [R/W] B,H --000000	WTSR [R/W] B --000000	—	
00056C _H	—	CSVCR [R/W] B 000111--	—	—	Clock Supervisor
000570 _H to 00057C _H	—	—	—	—	Reserved
000580 _H	REGSEL [R/W] B,H,W 0110011-	—	—	—	Regulator Control / Low Voltage Detection
000584 _H	LVD5R [R/W] B,H,W -----1	LVD5F [R/W] B,H,W 00000001	LVD [R/W] B,H,W 01000--0	—	
000588 _H , 00058C _H	—	—	—	—	Reserved
000590 _H	PMUSTR [R/W] B,H,W 0----1X	PMUCTLR [R/W] B,H,W 0-00---	PWRTMCTL [R/W] B,H,W ----011	—	PMU
000594 _H	PMUINTF0 [R/W] B,H,W 00000000	PMUINTF1 [R/W] B,H,W 00000000	PMUINTF2 [R/W] B,H,W 0000----	PMUINTF3 [R/W] B,H,W 00000000	PMU
000598 _H	—	—	—	—	
00059C _H to 0005FC _H	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000600 _H	ASR0 [R/W] W 00000000 00000000 ----- 1111-001				External Bus Interface [S]
000604 _H	ASR1 [R/W] W XXXXXXXX XXXXXXXX ----- XXXX-XX0				
000608 _H	ASR2 [R/W] W XXXXXXXX XXXXXXXX ----- XXXX-XX0				
00060C _H	ASR3 [R/W] W XXXXXXXX XXXXXXXX ----- XXXX-XX0				External Bus Interface [S]
000610 _H to 00063C _H	—	—	—	—	Reserved [S]
000640 _H	ACR0 [R/W] W ----- 01--00--				External Bus Interface [S]
000644 _H	ACR1 [R/W] W ----- XX--XX--				
000648 _H	ACR2 [R/W] W ----- XX--XX--				
00064C _H	ACR3 [R/W] W ----- XX--XX--				
000650 _H to 00067C _H	—	—	—	—	Reserved [S]
000680 _H	AWR0 [R/W] W ----1111 00000000 11110000 00000-0-				External Bus Interface [S]
000684 _H	AWR1 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
000688 _H	AWR2 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
00068C _H	AWR3 [R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
000690 _H to 0006FC _H	—	—	—	—	Reserved [S]
000700 _H to 00070C _H	—	—	—	—	Reserved
000710 _H	BPCCRA [R/W] B 00000000	BPCCRB [R/W] B 00000000	BPCCRC [R/W] B 00000000	—	Bus Performance Counter
000714 _H	BPCTRA [R/W] W 00000000 00000000 00000000 00000000				
000718 _H	BPCTRB [R/W] W 00000000 00000000 00000000 00000000				
00071C _H	BPCTRC [R/W] W 00000000 00000000 00000000 00000000				
000720 _H to 0007F8 _H	—	—	—	—	Reserved
0007FC _H	BMODR [R] B, H, W XXXXXXXX	—	—	—	Mode Register

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000800 _H to 00083C _H	—	—	—	—	Reserved [S]
000840 _H	FCTLR [R/W] H -0--1000 0--0----		—	FSTR [R/W] B -----001	Flash Memory Register [S]
000844 _H to 000854 _H	—	—	—	—	Reserved [S]
000858 _H	—	—	WREN [R/W] H 00000000 00000000		Wild Register [S]
00085C _H to 00087C _H	—	—	—	—	Reserved [S]
000880 _H	WRAR00 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXXX--				Wild Register [S]
000884 _H	WRDR00 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000888 _H	WRAR01 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXXX--				
00088C _H	WRDR01 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000890 _H	WRAR02 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXXX--				
000894 _H	WRDR02 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000898 _H	WRAR03 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXXX--				
00089C _H	WRDR03 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008A0 _H	WRAR04 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXXX--				
0008A4 _H	WRDR04 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008A8 _H	WRAR05 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXXX--				
0008AC _H	WRDR05 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008B0 _H	WRAR06 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXXX--				
0008B4 _H	WRDR06 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008B8 _H	WRAR07 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXXX--				
0008BC _H	WRDR07 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008C0 _H	WRAR08 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXXX--				
0008C4 _H	WRDR08 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0008C8 _H	WRAR09 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				Wild Register [S]
0008CC _H	WRDR09 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008D0 _H	WRAR10 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008D4 _H	WRDR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008D8 _H	WRAR11 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008DC _H	WRDR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008E0 _H	WRAR12 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008E4 _H	WRDR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008E8 _H	WRAR13 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008EC _H	WRDR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008F0 _H	WRAR14 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008F4 _H	WRDR14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008F8 _H	WRAR15 [R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008FC _H	WRDR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000900 _H	TPUUNLOCK [R/W] W 00000000 00000000 00000000 00000000				Time Protection Unit [S]
000904 _H	TPULST [R] B,H,W -----0	—	TPUVST [R/W] B,H,W -----000	—	
000908 _H	TPUCFG [R/W] B,H,W -----0 0-000000 -----0				
00090C _H	TPUTIR [R] B,H,W 00000000	—	—	—	
000910 _H	TPUTST [R] B,H,W 00000000	—	—	—	
000914 _H	TPUTIE [R/W] B,H,W 00000000	—	—	—	
000918 _H	TPUTMID [R] B,H,W 00000000 00000000 00000000 00000000				
00091C _H to 00092C _H	—	—	—	—	
000930 _H	TPUTCN00 [R/W] B,H,W 000000-- 00000000 00000000 00000000				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000934 _H	TPUTCN01 [R/W] B,H,W 000000-- 00000000 00000000 00000000				Time Protection Unit [S]
000938 _H	TPUTCN02 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
00093C _H	TPUTCN03 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000940 _H	TPUTCN04 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000944 _H	TPUTCN05 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000948 _H	TPUTCN06 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
00094C _H	TPUTCN07 [R/W] B,H,W 000000-- 00000000 00000000 00000000				
000950 _H	TPUTCN10 [R/W] B,H,W ---00000	—	—	—	
000954 _H	TPUTCN11 [R/W] B,H,W ---00000	—	—	—	
000958 _H	TPUTCN12 [R/W] B,H,W ---00000	—	—	—	
00095C _H	TPUTCN13 [R/W] B,H,W ---00000	—	—	—	
000960 _H	TPUTCN14 [R/W] B,H,W ---00000	—	—	—	
000964 _H	TPUTCN15 [R/W] B,H,W ---00000	—	—	—	
000968 _H	TPUTCN16 [R/W] B,H,W ---00000	—	—	—	
00096C _H	TPUTCN17 [R/W] B,H,W ---00000	—	—	—	
000970 _H	TPUTCC0 [R] B,H,W ----- 00000000 00000000 00000000				
000974 _H	TPUTCC1 [R] B,H,W ----- 00000000 00000000 00000000				
000978 _H	TPUTCC2 [R] B,H,W ----- 00000000 00000000 00000000				
00097C _H	TPUTCC3 [R] B,H,W ----- 00000000 00000000 00000000				
000980 _H	TPUTCC4 [R] B,H,W ----- 00000000 00000000 00000000				
000984 _H	TPUTCC5 [R] B,H,W ----- 00000000 00000000 00000000				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000988 _H	TPUTC6 [R] B,H,W ----- 00000000 00000000 00000000				Time Protection Unit [S]
00098C _H	TPUTC7 [R] B,H,W ----- 00000000 00000000 00000000				
000990 _H to 0009FC _H	—	—	—	—	
000A00 _H to 000BEC _H	—	—	—	—	
000BF0 _H	HSCFR [R/W] B,H,W ----- 00 00000000 00000000				OCDU
000BF4 _H	—	—	—	—	
000BF8 _H	—	—	MBR [R/W] B,H,W 00----- XXXXXXXX		
000BFC _H	—	—	UER [W] B,H,W -----X		
000C00 _H	DCCR0 [R/W] W 0---000 --00--00 00000000 0-000000				DMA Controller [S]
000C04 _H	DCSR0 [R/W] H 0----- 000		DTCR0 [R/W] H 00000000 00000000		
000C08 _H	DSAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C0C _H	DDAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C14 _H	DCSR1 [R/W] H 0----- 000		DTCR1 [R/W] H 00000000 00000000		
000C18 _H	DSAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C1C _H	DDAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C20 _H	DCCR2 [R/W] W 0---000 --00--00 00000000 0-000000				
000C24 _H	DCSR2 [R/W] H 0----- 000		DTCR2 [R/W] H 00000000 00000000		
000C28 _H	DSAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C2C _H	DDAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C30 _H	DCCR3 [R/W] W 0---000 --00--00 00000000 0-000000				
000C34 _H	DCSR3 [R/W] H 0----- 000		DTCR3 [R/W] H 00000000 00000000		
000C38 _H	DSAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C3C _H	DDAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C40 _H	DCCR4 [R/W] W 0---000 --00--00 00000000 0-000000				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000C44 _H	DCSR4 [R/W] H 0-----000		DTCR4 [R/W] H 00000000 00000000		DMA Controller [S]
000C48 _H	DSAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C4C _H	DDAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C50 _H	DCCR5 [R/W] W 0---000 --00--00 00000000 0-000000				
000C54 _H	DCSR5 [R/W] H 0-----000		DTCR5 [R/W] H 00000000 00000000		
000C58 _H	DSAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C5C _H	DDAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C60 _H	DCCR6 [R/W] W 0---000 --00--00 00000000 0-000000				
000C64 _H	DCSR6 [R/W] H 0-----000		DTCR6 [R/W] H 00000000 00000000		
000C68 _H	DSAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C6C _H	DDAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C70 _H	DCCR7 [R/W] W 0---000 --00--00 00000000 0-000000				
000C74 _H	DCSR7 [R/W] H 0-----000		DTCR7 [R/W] H 00000000 00000000		
000C78 _H	DSAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C7C _H	DDAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C80 _H	DCCR8 [R/W] W 0---000 --00--00 00000000 0-000000				
000C84 _H	DCSR8 [R/W] H 0-----000		DTCR8 [R/W] H 00000000 00000000		
000C88 _H	DSAR8 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C8C _H	DDAR8 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C90 _H	DCCR9 [R/W] W 0---000 --00--00 00000000 0-000000				
000C94 _H	DCSR9 [R/W] H 0-----000		DTCR9 [R/W] H 00000000 00000000		
000C98 _H	DSAR9 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C9C _H	DDAR9 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CA0 _H	DCCR10 [R/W] W 0---000 --00--00 00000000 0-000000				
000CA4 _H	DCSR10 [R/W] H 0-----000		DTCR10 [R/W] H 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000CA8 _H	DSAR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMA Controller [S]
000CAC _H	DDAR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CB0 _H	DCCR11 [R/W] W 0----000 --00--00 00000000 0-000000				
000CB4 _H	DCSR11 [R/W] H 0----- ----000		DTCR11 [R/W] H 00000000 00000000		
000CB8 _H	DSAR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CBC _H	DDAR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CC0 _H	DCCR12 [R/W] W 0----000 --00--00 00000000 0-000000				
000CC4 _H	DCSR12 [R/W] H 0----- ----000		DTCR12 [R/W] H 00000000 00000000		
000CC8 _H	DSAR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CCC _H	DDAR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CD0 _H	DCCR13 [R/W] W 0----000 --00--00 00000000 0-000000				
000CD4 _H	DCSR13 [R/W] H 0----- ----000		DTCR13 [R/W] H 00000000 00000000		
000CD8 _H	DSAR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CDC _H	DDAR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CE0 _H	DCCR14 [R/W] W 0----000 --00--00 00000000 0-000000				
000CE4 _H	DCSR14 [R/W] H 0----- ----000		DTCR14 [R/W] H 00000000 00000000		
000CE8 _H	DSAR14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CEC _H	DDAR14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CF0 _H	DCCR15 [R/W] W 0----000 --00--00 00000000 0-000000				
000CF4 _H	DCSR15 [R/W] H 0----- ----000		DTCR15 [R/W] H 00000000 00000000		
000CF8 _H	DSAR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CFC _H	DDAR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000D00 _H to 000DF0 _H	—	—	—	—	Reserved [S]

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000DF4 _H	—	—	DNMIR [R/W] B 0-----0	DILVR [R/W] B ---11111	DMA Controller [S]
000DF8 _H	DMACR[R/W] W 0----- 0-----				
000DFC _H	—	—	—	—	Reserved [S]
000E00 _H	DDR00 [R/W] B,H,W 00000000	DDR01 [R/W] B,H,W 00000000	DDR02 [R/W] B,H,W 00000000	DDR03 [R/W] B,H,W 00000000	Data Direction Register
000E04 _H	DDR04 [R/W] B,H,W 00000000	DDR05 [R/W] B,H,W 00000000	DDR06 [R/W] B,H,W 00000000	DDR07 [R/W] B,H,W 00000000	
000E08 _H	DDR08 [R/W] B,H,W 00000000	DDR09 [R/W] B,H,W 00000000	DDR10 [R/W] B,H,W 00000000	DDR11 [R/W] B,H,W 00000000	
000E0C _H	DDR12 [R/W] B,H,W 00000000	DDR13 [R/W] B,H,W -000-00	DDR14 [R/W] B,H,W -----	DDR15 [R/W] B,H,W --000000	
000E10 _H	DDR20 [R/W] B,H,W 00000000	DDR21 [R/W] B,H,W 00000000	DDR22 [R/W] B,H,W 000--000	DDR23 [R/W] B,H,W 00000000	
000E14 _H	DDR24 [R/W] B,H,W --000000	DDR25 [R/W] B,H,W -0000000	DDR26 [R/W] B,H,W 000000--	DDR27 [R/W] B,H,W 000-0000	
000E18 _H	DDR16 [R/W] B,H,W 00000000	DDR17 [R/W] B,H,W 00000000	DDR18 [R/W] B,H,W 00000000	DDR19 [R/W] B,H,W 00000000	
000E1C _H	DDR28 [R/W] B,H,W 00000000	DDR29 [R/W] B,H,W 00000000	—	—	
000E20 _H	PFR00 [R/W] B,H,W 00000000	PFR01 [R/W] B,H,W 00000000	PFR02 [R/W] B,H,W 00000000	PFR03 [R/W] B,H,W 00000000	Port Function Register
000E24 _H	PFR04 [R/W] B,H,W 00000000	PFR05 [R/W] B,H,W 00000000	PFR06 [R/W] B,H,W 00000000	PFR07 [R/W] B,H,W 00000000	
000E28 _H	PFR08 [R/W] B,H,W 00000000	PFR09 [R/W] B,H,W 00000000	PFR10 [R/W] B,H,W 00000000	PFR11 [R/W] B,H,W 00000000	
000E2C _H	PFR12 [R/W] B,H,W 00000000	PFR13 [R/W] B,H,W -000-00	PFR14 [R/W] B,H,W -----	PFR15 [R/W] B,H,W --000000	
000E30 _H	PFR20 [R/W] B,H,W 00000000	PFR21 [R/W] B,H,W 00000000	PFR22 [R/W] B,H,W 000--000	PFR23 [R/W] B,H,W 00000000	
000E34 _H	PFR24 [R/W] B,H,W --000000	PFR25 [R/W] B,H,W -0000000	PFR26 [R/W] B,H,W 000000--	PFR27 [R/W] B,H,W 000-0000	
000E38 _H	PFR16 [R/W] B,H,W 00000000	PFR17 [R/W] B,H,W 00000000	PFR18 [R/W] B,H,W 00000000	PFR19 [R/W] B,H,W 00000000	
000E3C _H	PFR28 [R/W] B,H,W 00000000	PFR29 [R/W] B,H,W 00000000	—	—	
000E40 _H	PDDR00 [R] B,H,W XXXXXXXXXX	PDDR01 [R] B,H,W XXXXXXXXXX	PDDR02 [R] B,H,W XXXXXXXXXX	PDDR03 [R] B,H,W XXXXXXXXXX	Port Direct Read Register
000E44 _H	PDDR04 [R] B,H,W XXXXXXXXXX	PDDR05 [R] B,H,W XXXXXXXXXX	PDDR06 [R] B,H,W XXXXXXXXXX	PDDR07 [R] B,H,W XXXXXXXXXX	
000E48 _H	PDDR08 [R] B,H,W XXXXXXXXXX	PDDR09 [R] B,H,W XXXXXXXXXX	PDDR10 [R] B,H,W XXXXXXXXXX	PDDR11 [R] B,H,W XXXXXXXXXX	
000E4C _H	PDDR12 [R] B,H,W XXXXXXXXXX	PDDR13 [R] B,H,W -XXX-XX	PDDR14 [R] B,H,W -----	PDDR15 [R] B,H,W --XXXXXX	
000E50 _H	PDDR20 [R] B,H,W XXXXXXXXXX	PDDR21 [R] B,H,W XXXXXXXXXX	PDDR22 [R] B,H,W XXX-XXX	PDDR23 [R] B,H,W XXXXXXXXXX	
000E54 _H	PDDR24 [R] B,H,W --XXXXXX	PDDR25 [R] B,H,W -XXXXXX	PDDR26 [R] B,H,W XXXXXX--	PDDR27 [R] B,H,W XXX-XXXX	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000E58 _H	PDDR16 [R] B,H,W XXXXXXXXXX	PDDR17 [R] B,H,W XXXXXXXXXX	PDDR18 [R] B,H,W XXXXXXXXXX	PDDR19 [R] B,H,W XXXXXXXXXX	Port Direct Read Register
000E5C _H	PDDR28 [R] B,H,W XXXXXXXXXX	PDDR29 [R] B,H,W XXXXXXXXXX	—	—	
000E60 _H	EPFR00 [R/W] B,H,W 00000000	EPFR01 [R/W] B,H,W -0-0-000	EPFR02 [R/W] B,H,W ----0000	EPFR03 [R/W] B,H,W ---000-0	Extended Port Function Register
000E64 _H	EPFR04 [R/W] B,H,W ----00-0	EPFR05 [R/W] B,H,W ----0000	EPFR06 [R/W] B,H,W ----000-	EPFR07 [R/W] B,H,W ---00000	
000E68 _H	EPFR08 [R/W] B,H,W ---00000	EPFR09 [R/W] B,H,W -----00-	EPFR10 [R/W] B,H,W ----0000	EPFR11 [R/W] B,H,W ----0000	
000E6C _H	EPFR12 [R/W] B,H,W ----0000	EPFR13 [R/W] B,H,W -----00	EPFR14 [R/W] B,H,W -----00	EPFR15 [R/W] B,H,W -----000	
000E70 _H	—	—	—	—	
000E74 _H	—	—	—	—	
000E78 _H	—	—	EPFR26 [R/W] B,H,W 00000000	EPFR27 [R/W] B,H,W --0----	
000E7C _H	EPFR28 [R/W] B,H,W --000-0-	EPFR29 [R/W] B,H,W 00000000	—	—	
000E80 _H	—	EPFR33 [R/W] B,H,W -----00-	EPFR34 [R/W] B,H,W -----00-	EPFR35 [R/W] B,H,W ---00000	
000E84 _H	EPFR36 [R/W] B,H,W ----0-0-	—	—	—	
000E88 _H	—	—	EPFR42 [R/W] B,H,W -----00	EPFR43 [R/W] B,H,W 0--0000-	
000E8C _H	EPFR44 [R/W] B,H,W -00---0-	EPFR45 [R/W] B,H,W -0000000	—	—	
000E90 _H	EPFR48 [R/W] B,H,W ----0-0	EPFR49 [R/W] B,H,W -----000	EPFR50 [R/W] B,H,W -----00	EPFR51 [R/W] B,H,W ---00000	
000E94 _H	—	—	—	—	
000E98 _H	EPFR56 [R/W] B,H,W ----0-0	EPFR57 [R/W] B,H,W -----0-0	EPFR58 [R/W] B,H,W ----00-0	EPFR59 [R/W] B,H,W ---00-0	
000E9C _H	EPFR60 [R/W] B,H,W ----00--	EPFR61 [R/W] B,H,W -----00-	EPFR62 [R/W] B,H,W -----00-	EPFR63 [R/W] B,H,W ---0-0--	
000EA0 _H to 000EB0 _H	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000EB4 _H	CPCLR9 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 9 32-bit FRT
000EB8 _H	TCDT9 [R/W] W 00000000 00000000 00000000 00000000				
000EBC _H	TCCSH9 [R/W] B,H,W 0-----00	TCCSL9 [R/W] B,H,W -1-00000	—	—	Free-run Timer 9 32-bit FRT
000EC0 _H	PPER00 [R/W] B,H,W 00000000	PPER01 [R/W] B,H,W 00000000	PPER02 [R/W] B,H,W 00000000	PPER03 [R/W] B,H,W 00000000	Port Pull-up/down Enable Register
000EC4 _H	PPER04 [R/W] B,H,W 00000000	PPER05 [R/W] B,H,W 00000000	PPER06 [R/W] B,H,W 00000000	PPER07 [R/W] B,H,W 00000000	
000EC8 _H	PPER08 [R/W] B,H,W 00000000	PPER09 [R/W] B,H,W 00000000	PPER10 [R/W] B,H,W 00000000	PPER11 [R/W] B,H,W 00000000	
000ECC _H	PPER12 [R/W] B,H,W 00000000	PPER13 [R/W] B,H,W -000--00	PPER14 [R/W] B,H,W -----	PPER15 [R/W] B,H,W --000000	
000ED0 _H	PPER20 [R/W] B,H,W 00000000	PPER21 [R/W] B,H,W 00000000	PPER22 [R/W] B,H,W 000--000	PPER23 [R/W] B,H,W 00000000	Port Pull-up/down Enable Register
000ED4 _H	PPER24 [R/W] B,H,W --000000	PPER25 [R/W] B,H,W -0000000	PPER26 [R/W] B,H,W 000000--	PPER27 [R/W] B,H,W 000-0000	
000ED8 _H	PPER16 [R/W] B,H,W 00000000	PPER17 [R/W] B,H,W 00000000	PPER18 [R/W] B,H,W 00000000	PPER19 [R/W] B,H,W 00000000	
000EDC _H	PPER28 [R/W] B,H,W 00000000	PPER29 [R/W] B,H,W 00000000	—	—	
000EE0 _H	PILR00[R/W] B,H,W 11-1--1-	PILR01[R/W] B,H,W 11111111	—	—	Port Input Level Register
000EE4 _H	—	PILR05[R/W] B,H,W -----1--	—	—	
000EE8 _H	—	—	—	PILR11[R/W] B,H,W ---1----	
000EEC _H	PILR12[R/W] B,H,W ----1--1	—	—	PILR15[R/W] B,H,W --1-----	
000EF0 _H	CPCLR10 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 10 32-bit FRT
000EF4 _H	TCDT10 [R/W] W 00000000 00000000 00000000 00000000				
000EF8 _H	TCCSH10 [R/W] B,H,W 0-----00	TCCSL10 [R/W] B,H,W -1-00000	—	—	
000EFC _H to 000F0C _H	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000F10 _H	RCRH2 [R/W] H,W XXXXXXXXXX	RCRL2 [R/W] B,H,W XXXXXXXXXX	UDCRH2 [R/W] H,W 00000000	UDCRL2 [R/W] B,H,W 00000000	UpDown Counter 2
000F14 _H	CCR2 [R/W] B,H 00000000 -0001000		—	CSR2 [R/W] B 00000000	
000F18 _H	RCRH3 [R/W] H,W XXXXXXXXXX	RCRL3 [R/W] B,H,W XXXXXXXXXX	UDCRH3 [R/W] H,W 00000000	UDCRL3 [R/W] B,H,W 00000000	UpDown Counter 3
000F1C _H	CCR3 [R/W] B,H 00000000 -0001000		—	CSR3 [R/W] B 00000000	
000F20 _H to 000F30 _H	—	—	—	—	Reserved
000F34 _H , 000F38 _H	—	—	—	—	Reserved
000F3C _H	—	—	—	OCLS1213 [R/W] B,H,W ----0000	OCU12,13 Output level control register
000F40 _H	PORTEN [R/W] B,H,W -----0	—	—	—	Port Enable Register
000F44 _H	KEYCDR [R/W] H 00000000 00000000		—	—	KeyCodeRegister
000F48 _H to 000F64 _H	—	—	—	—	Reserved
000F68 _H	MSCY6 [R] H,W XXXXXXXXXX XXXXXXXXXXXX XXXXXXXXXXXX XXXXXXXXXXXX				Input Capture 6,7 Cycle measurement data register 67
000F6C _H	MSCY7 [R] H,W XXXXXXXXXX XXXXXXXXXXXX XXXXXXXXXXXX XXXXXXXXXXXX				
000F70 _H	RCRH0 [W] H,W XXXXXXXXXX	RCRL0 [W] B,H,W XXXXXXXXXX	UDCRH0 [R] H,W 00000000	UDCRL0 [R] B,H,W 00000000	UpDown Counter 0
000F74 _H	CCR0 [R/W] B,H 00000000 -0001000		—	CSR0 [R/W] B 00000000	
000F78 _H , 000F7C _H	—	—	—	—	Reserved
000F80 _H	RCRH1 [W] H,W XXXXXXXXXX	RCRL1 [W] B,H,W XXXXXXXXXX	UDCRH1 [R] H,W 00000000	UDCRL1 [R] B,H,W 00000000	UpDown Counter 1
000F84 _H	CCR1 [R/W] B,H 00000000 -0001000		—	CSR1 [R/W] B 00000000	
000F88 _H	—	—	MSCH45 [R] B,H,W 00000000	MSCL45 [R/W] B,H,W -----00	Input Capture 4,5 32-bit ICU Cycle and pulse width measurement control 45
000F8C _H	—	—	MSCH67 [R] B,H,W 00000000	MSCL67 [R/W] B,H,W -----00	Input Capture 6,7 32-bit ICU Cycle and pulse width measurement control 67
000F90 _H	OCCP10 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 10,11 32-bit OCU

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000F94 _H	OCCP11 [R/W] W 00000000 00000000 00000000 00000000				Output Compare 10,11 32-bit OCU
000F98 _H	—	—	OCSH1011 [R/W] B,H,W ---0--00	OCSL1011 [R/W] B,H,W 0000--00	
000F9C _H	—	—	—	OCLS1011 [R/W] B,H,W ----0000	OCU10,11 Output level control register
000FA0 _H	CPCLR5 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 5 32-bit FRT
000FA4 _H	TCDT5 [R/W] W 00000000 00000000 00000000 00000000				
000FA8 _H	TCCSH5 [R/W]B,H,W 0-----00	TCCSL5 [R/W]B,H,W -1-00000	—	—	
000FAC _H	CPCLR6 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 6 32-bit FRT
000FB0 _H	TCDT6 [R/W] W 00000000 00000000 00000000 00000000				
000FB4 _H	TCCSH6 [R/W]B,H,W 0-----00	TCCSL6 [R/W]B,H,W -1-00000	—	—	
000FB8 _H	CPCLR7 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 7 32-bit FRT
000FBC _H	TCDT7 [R/W] W 00000000 00000000 00000000 00000000				
000FC0 _H	TCCSH7 [R/W]B,H,W 0-----00	TCCSL7 [R/W]B,H,W -1-00000	—	—	
000FC4 _H	CPCLR8 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 8 32-bit FRT
000FC8 _H	TCDT8 [R/W] W 00000000 00000000 00000000 00000000				
000FCC _H	TCCSH8 [R/W]B,H,W 0-----00	TCCSL8 [R/W]B,H,W -1-00000	—	—	
000FD0 _H	IPCP4 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 4,5 32-bit ICU
000FD4 _H	IPCP5 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FD8 _H	—	LSYNS2 [R/W] B,H,W --000000	LSYNS1 [R/W] B,H,W 00000000	ICS45 [R/W] B,H,W 00000000	
000FDC _H	IPCP6 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 6,7 32-bit ICU
000FE0 _H	IPCP7 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FE4 _H	—	—	—	ICS67 [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000FE8 _H	IPCP8 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 8,9 32-bit ICU
000FEC _H	IPCP9 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FF0 _H	—	—	—	ICS89 [R/W] B,H,W 00000000	
000FF4 _H	MSCY8 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 8,9 32-bit ICU
000FF8 _H	MSCY9 [R] H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FFC _H	—	—	MSCH89 [R] B,H,W 00000000	MSCL89 [R/W] B,H,W -----00	
001000 _H	SACR [R/W] B,H,W -----0	PICD [R/W] B,H,W ----0011	—	—	Clock Control
001004 _H to 00112C _H	—	—	—	—	Reserved
001130 _H	—	—	—	CRCCR [R/W] B,H,W -0000000	CRC calculation unit
001134 _H	CRCINIT [R/W] B,H,W 11111111 11111111 11111111 11111111				
001138 _H	CRCIN [R/W] B,H,W 00000000 00000000 00000000 00000000				
00113C _H	CRCR [R] B,H,W 11111111 11111111 11111111 11111111				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001140 _H	SCR16/(IBCR16) [R/W] B,H,W 0--00000	SMR16 [R/W] B,H,W 000-00-0	SSR16 [R/W] B,H,W 0-000011	ESCR16/(IBSR16) [R/W] B,H,W 00000000	Multi-UART16 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001144 _H	—/(RDR116/(TDR116))[R/W] B,H,W -----*3		RDR016/(TDR016)[R/W] B,H,W -----0 00000000* ¹		
001148 _H	SACSR16[R/W] B,H,W 0---000 00000000		STMR16[R] B,H,W 00000000 00000000		
00114C _H	STMCR16[R/W] B,H,W 00000000 00000000		—/(SCSCR16/SFUR16)[R/W] B,H,W -----*3 * ⁴		
001150 _H	—/(SCSTR316)/ (LAMSR16) [R/W] B,H,W -----*3	—/(SCSTR216)/ (LAMCR16) [R/W] B,H,W -----*3	— /(SCSTR116)/(SFLR16) [R/W] B,H,W -----*3	— /(SCSTR016)/(SFLR016) [R/W] B,H,W -----*3	
001154 _H	—	—/(SCSFR216) [R/W] B,H,W -----*3	—/(SCSFR116) [R/W] B,H,W -----*3	—/(SCSFR016) [R/W] B,H,W -----*3	
001158 _H	—/(TBYTE316)/ (LAMESR16) [R/W] B,H,W -----*3	—/(TBYTE216)/ (LAMERT16) [R/W] B,H,W -----*3	—/(TBYTE116)/ (LAMIER16) [R/W] B,H,W -----*3	TBYTE016/(LAMRID16)/(LAMTID16) [R/W] B,H,W 00000000	
00115C _H	BGR16[R/W] H,W 00000000 00000000		—/(ISMK16) [R/W] B,H,W -----* ²	—/(ISBA16) [R/W] B,H,W -----* ²	
001160 _H	FCR116 [R/W] B,H,W ---00100	FCR016 [R/W] B,H,W -0000000	FBYTE16[R/W] B,H,W 00000000 00000000		
001164 _H	FTICR16[R/W] B,H,W 00000000 00000000		—	—	

MB91F527R/MB91F527U/MB91F527M/MB91F527Y MB91F528R/MB91F528U/MB91F528M/MB91F528Y

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001168 _H	SCR17/(IBCR17) [R/W] B,H,W 0--00000	SMR17 [R/W] B,H,W 000-00-0	SSR17 [R/W] B,H,W 0-000011	ESCR17/(IBSR17) [R/W] B,H,W 00000000	Multi-UART17 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
00116C _H	—/(RDR117/(TDR117))[R/W] B,H,W -----*3		RDR017/(TDR017)[R/W] B,H,W -----0 00000000*1		
001170 _H	SACSR17[R/W] B,H,W 0----000 00000000		STMR17[R] B,H,W 00000000 00000000		
001174 _H	STMCR17[R/W] B,H,W 00000000 00000000		—/(SCSCR17/SFUR17)[R/W] B,H,W -----*3 *4		
001178 _H	—/(SCSTR317)/ (LAMSR17) [R/W] B,H,W -----*3	—/(SCSTR217)/ (LAMCR17) [R/W] B,H,W -----*3	—/(SCSTR117)/(SFLR17) [R/W] B,H,W -----*3	—/(SCSTR017)/(SFLR017) [R/W] B,H,W -----*3	
00117C _H	—	—/(SCSFR217) [R/W] B,H,W -----*3	—/(SCSFR117) [R/W] B,H,W -----*3	—/(SCSFR017) [R/W] B,H,W -----*3	
001180 _H	—/(TBYTE317)/ (LAMESR17) [R/W] B,H,W -----*3	—/(TBYTE217)/ (LAMERT17) [R/W] B,H,W -----*3	—/(TBYTE117)/ (LAMIER17) [R/W] B,H,W -----*3	TBYTE017/(LAMRID17)/(LAMTID17) [R/W] B,H,W 00000000	
001184 _H	BGR17[R/W] H,W 00000000 00000000		—/(ISMK17) [R/W] B,H,W -----*2	—/(ISBA17) [R/W] B,H,W -----*2	
001188 _H	FCR117 [R/W] B,H,W ---00100	FCR017 [R/W] B,H,W -0000000	FBYTE17[R/W] B,H,W 00000000 00000000		
00118C _H	FTICR17[R/W] B,H,W 00000000 00000000		—	—	
001190 _H	SCR18/(IBCR18) [R/W] B,H,W 0--00000	SMR18 [R/W] B,H,W 000-00-0	SSR18 [R/W] B,H,W 0-000011	ESCR18/(IBSR18) [R/W] B,H,W 00000000	Multi-UART18 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001194 _H	—/(RDR118/(TDR118))[R/W] B,H,W -----*3		RDR018/(TDR018)[R/W] B,H,W -----0 00000000*1		
001198 _H	SACSR18[R/W] B,H,W 0----000 00000000		STMR18[R] B,H,W 00000000 00000000		
00119C _H	STMCR18[R/W] B,H,W 00000000 00000000		—/(SCSCR18/SFUR18)[R/W] B,H,W -----*3 *4		
0011A0 _H	—/(SCSTR318)/ (LAMSR18) [R/W] B,H,W -----*3	—/(SCSTR218)/ (LAMCR18) [R/W] B,H,W -----*3	—/(SCSTR118)/(SFLR18) [R/W] B,H,W -----*3	—/(SCSTR018)/(SFLR018) [R/W] B,H,W -----*3	
0011A4 _H	—	—/(SCSFR218) [R/W] B,H,W -----*3	—/(SCSFR118) [R/W] B,H,W -----*3	—/(SCSFR018) [R/W] B,H,W -----*3	
0011A8 _H	—/(TBYTE318)/ (LAMESR18) [R/W] B,H,W -----*3	—/(TBYTE218)/ (LAMERT18) [R/W] B,H,W -----*3	—/(TBYTE118)/ (LAMIER18) [R/W] B,H,W -----*3	TBYTE018/(LAMRID18)/(LAMTID18) [R/W] B,H,W 00000000	

MB91F527R/MB91F527U/MB91F527M/MB91F527Y MB91F528R/MB91F528U/MB91F528M/MB91F528Y

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0011AC _H	BGR18[R/W] H,W 00000000 00000000		— /(ISMK18) [R/W] B,H,W -----*2	— /(ISBA18) [R/W] B,H,W -----*2	Multi-UART18
0011B0 _H	FCR118 [R/W] B,H,W ---00100	FCR018 [R/W] B,H,W -0000000	FBYTE18[R/W] B,H,W 00000000 00000000		
0011B4 _H	FTICR18[R/W] B,H,W 00000000 00000000		—	—	
0011B8 _H	SCR19/(IBCR19) [R/W] B,H,W 0--00000	SMR19 [R/W] B,H,W 000-00-0	SSR19 [R/W] B,H,W 0-000011	ESCR19/(IBSR19) [R/W] B,H,W 00000000	Multi-UART19 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
0011BC _H	— /(RDR119/(TDR119))[R/W] B,H,W -----*3		RDR019/(TDR019)[R/W] B,H,W -----0 00000000*1		
0011C0 _H	SACSR19[R/W] B,H,W 0----000 00000000		STMR19[R] B,H,W 00000000 00000000		
0011C4 _H	STMCR19[R/W] B,H,W 00000000 00000000		— /(SCSCR19/SFUR19)[R/W] B,H,W -----*3 *4		
0011C8 _H	— /(SCSTR319)/ (LAMSR19) [R/W] B,H,W -----*3	— /(SCSTR219)/ (LAMCR19) [R/W] B,H,W -----*3	— /(SCSTR119)/(SFLR19) [R/W] B,H,W -----*3	— /(SCSTR019)/(SFLR019) [R/W] B,H,W -----*3	
0011CC _H	—	— /(SCSFR219) [R/W] B,H,W -----*3	— /(SCSFR119) [R/W] B,H,W -----*3	— /(SCSFR019) [R/W] B,H,W -----*3	
0011D0 _H	—/(TBYTE319)/ (LAMESR19) [R/W] B,H,W -----*3	—/(TBYTE219)/ (LAMERT19) [R/W] B,H,W -----*3	—/(TBYTE119)/ (LAMIER19) [R/W] B,H,W -----*3	TBYTE019/(LAMRID19)/(LAMTID19) [R/W] B,H,W 00000000	
0011D4 _H	BGR19[R/W] H,W 00000000 00000000		— /(ISMK19) [R/W] B,H,W -----*2	— /(ISBA19) [R/W] B,H,W -----*2	
0011D8 _H	FCR119 [R/W] B,H,W ---00100	FCR019 [R/W] B,H,W -0000000	FBYTE19[R/W] B,H,W 00000000 00000000		
0011DC _H	FTICR19[R/W] B,H,W 00000000 00000000		—	—	
0011E0 _H to 0011FC _H	—	—	—	—	Reserved
001200 _H	TCGS [R/W] B,H,W -----00	—	—	TCGSE [R/W] B,H,W -----000	16-bit Free-run timer synchronous activation
001204 _H	CPCLRB0/CPCLR0 [W] H,W 11111111 11111111		TCDT0 [R/W] H,W 00000000 00000000		16-bit Free-run timer 0
001208 _H	TCCS0 [R/W] B,H,W 00000000 01000000 ----0000 -----				
00120C _H	CPCLRB1/CPCLR1 [W] H,W 11111111 11111111		TCDT1 [R/W] H,W 00000000 00000000		16-bit Free-run timer 1
001210 _H	TCCS1 [R/W] B,H,W 00000000 01000000 ----0000 -----				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001214 _H	CPCLRB2/CPCLR2 [W] H,W 11111111 11111111		TCDT2 [R/W] H,W 00000000 00000000		16-bit Free-run timer 2
001218 _H	TCCS2 [R/W] B,H,W 00000000 01000000 ----0000 -----				
00121C _H to 001230 _H	—	—	—	—	Reserved
001234 _H	FRS0 [R/W] B,H,W ----- --00--00 --00--00 --00--00				16-bit Free-run timer selection
001238 _H	—		FRS1 [R/W] B,H,W --00--00 --00--00		
00123C _H	FRS2 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
001240 _H	FRS3 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
001244 _H	FRS4 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
001248 _H	—	—	—	—	Reserved
00124C _H	OCCPB0/OCCP0 [R/W] H,W 00000000 00000000		OCCPB1/OCCP1 [R/W] H,W 00000000 00000000		16-bit Output compare 0/1
001250 _H	OCS01 [R/W] B,H,W -110--00 00001100		—	OCMOD01 [R/W] B,H,W -----00	
001254 _H	OCCPB2/OCCP2 [R/W] H,W 00000000 00000000		OCCPB3/OCCP3 [R/W] H,W 00000000 00000000		16-bit Output compare 2/3
001258 _H	OCS23 [R/W] B,H,W -110--00 00001100		—	OCMOD23 [R/W] B,H,W -----00	
00125C _H	OCCPB4/OCCP4 [R/W] H,W 00000000 00000000		OCCPB5/OCCP5 [R/W] H,W 00000000 00000000		16-bit Output compare 4/5
001260 _H	OCS45 [R/W] B,H,W -110--00 00001100		—	OCMOD45 [R/W] B,H,W -----00	
001264 _H to 001278 _H	—	—	—	—	Reserved
00127C _H	IPCP0 [R] H,W 00000000 00000000		IPCP1 [R] H,W 00000000 00000000		16-bit Input capture 0/1
001280 _H	ICS01 [R/W] B,H,W -----00 00000000		—	LSYNS [R/W] B,H,W ---0000	
001284 _H	IPCP2 [R] H,W 00000000 00000000		IPCP3 [R] H,W 00000000 00000000		16-bit Input capture 2/3
001288 _H	ICS23 [R/W] B,H,W -----00 00000000		—	—	
00128C _H to 001298 _H	—	—	—	—	Reserved
00129C _H	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0012A0 _H	TMRR0 [R/W] H,W 00000000 00000001		TMRR1 [R/W] H,W 00000000 00000001		Waveform generator 0/1/2
0012A4 _H	TMRR2 [R/W] H,W 00000000 00000001		—	—	
0012A8 _H	DTSCR0 [R/W] B,H,W 00000000	DTSCR1 [R/W] B,H,W 00000000	DTSCR2 [R/W] B,H,W 00000000	—	
0012AC _H	—	DTIR0 [R/W] B,H,W 000000--	—	DTMNS0 [R/W] B,H,W 00---000	
0012B0 _H	—	SIGCR10 [R/W] B,H,W 00000000	—	SIGCR20 [R/W] B,H,W 000000-1	
0012B4 _H	PICS0 [R/W] B,H,W 000000-- -----				
0012B8 _H to 0012CC _H	—	—	—	—	Reserved
0012D0 _H	FRS5 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				16-bit Free-run timer selection A/D activation compare
0012D4 _H	FRS6 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
0012D8 _H	FRS7 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
0012DC _H	FRS10 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
0012E0 _H	FRS11 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				
0012E4 _H to 0012FC _H	—	—	—	—	Reserved
001300 _H	—				Reserved
001304 _H	ADTSS0[R/W] B,H,W -----0	—	—	—	12-bit A/D converter 1/2 unit
001308 _H	ADTSE0[R/W] B,H,W 00000000 00000000 00000000 00000000				
00130C _H	ADCOMP0/ADCOMPB0[R/W] H,W 00000000 00000000		ADCOMP1/ADCOMPB1[R/W] H,W 00000000 00000000		
001310 _H	ADCOMP2/ADCOMPB2[R/W] H,W 00000000 00000000		ADCOMP3/ADCOMPB3[R/W] H,W 00000000 00000000		
001314 _H	ADCOMP4/ADCOMPB4[R/W] H,W 00000000 00000000		ADCOMP5/ADCOMPB5[R/W] H,W 00000000 00000000		
001318 _H	ADCOMP6/ADCOMPB6[R/W] H,W 00000000 00000000		ADCOMP7/ADCOMPB7[R/W] H,W 00000000 00000000		
00131C _H	ADCOMP8/ADCOMPB8[R/W] H,W 00000000 00000000		ADCOMP9/ADCOMPB9[R/W] H,W 00000000 00000000		
001320 _H	ADCOMP10/ADCOMPB10[R/W] H,W 00000000 00000000		ADCOMP11/ADCOMPB11[R/W] H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001324 _H	ADCOMP12/ADCOMPB12[R/W] H,W 00000000 00000000		ADCOMP13/ADCOMPB13[R/W] H,W 00000000 00000000		12-bit A/D converter 1/2 unit
001328 _H	ADCOMP14/ADCOMPB14[R/W] H,W 00000000 00000000		ADCOMP15/ADCOMPB15[R/W] H,W 00000000 00000000		
00132C _H	ADCOMP16/ADCOMPB16[R/W] H,W 00000000 00000000		ADCOMP17/ADCOMPB17[R/W] H,W 00000000 00000000		
001330 _H	ADCOMP18/ADCOMPB18[R/W] H,W 00000000 00000000		ADCOMP19/ADCOMPB19[R/W] H,W 00000000 00000000		
001334 _H	ADCOMP20/ADCOMPB20[R/W] H,W 00000000 00000000		ADCOMP21/ADCOMPB21[R/W] H,W 00000000 00000000		
001338 _H	ADCOMP22/ADCOMPB22[R/W] H,W 00000000 00000000		ADCOMP23/ADCOMPB23[R/W] H,W 00000000 00000000		
00133C _H	ADCOMP24/ADCOMPB24[R/W] H,W 00000000 00000000		ADCOMP25/ADCOMPB25[R/W] H,W 00000000 00000000		
001340 _H	ADCOMP26/ADCOMPB26[R/W] H,W 00000000 00000000		ADCOMP27/ADCOMPB27[R/W] H,W 00000000 00000000		
001344 _H	ADCOMP28/ADCOMPB28[R/W] H,W 00000000 00000000		ADCOMP29/ADCOMPB29[R/W] H,W 00000000 00000000		
001348 _H	ADCOMP30/ADCOMPB30[R/W] H,W 00000000 00000000		ADCOMP31/ADCOMPB31[R/W] H,W 00000000 00000000		
00134C _H	ADTCS0[R/W] B,H,W 00000000 0010----		ADTCS1[R/W] B,H,W 00000000 0010----		
001350 _H	ADTCS2[R/W] B,H,W 00000000 0010----		ADTCS3[R/W] B,H,W 00000000 0010----		
001354 _H	ADTCS4[R/W] B,H,W 00000000 0010----		ADTCS5[R/W] B,H,W 00000000 0010----		
001358 _H	ADTCS6[R/W] B,H,W 00000000 0010----		ADTCS7[R/W] B,H,W 00000000 0010----		
00135C _H	ADTCS8[R/W] B,H,W 00000000 0010----		ADTCS9[R/W] B,H,W 00000000 0010----		
001360 _H	ADTCS10[R/W] B,H,W 00000000 0010----		ADTCS11[R/W] B,H,W 00000000 0010----		
001364 _H	ADTCS12[R/W] B,H,W 00000000 0010----		ADTCS13[R/W] B,H,W 00000000 0010----		
001368 _H	ADTCS14[R/W] B,H,W 00000000 0010----		ADTCS15[R/W] B,H,W 00000000 0010----		
00136C _H	ADTCS16[R/W] B,H,W 00000000 0010----		ADTCS17[R/W] B,H,W 00000000 0010----		
001370 _H	ADTCS18[R/W] B,H,W 00000000 0010----		ADTCS19[R/W] B,H,W 00000000 0010----		
001374 _H	ADTCS20[R/W] B,H,W 00000000 0010----		ADTCS21[R/W] B,H,W 00000000 0010----		
001378 _H	ADTCS22[R/W] B,H,W 00000000 0010----		ADTCS23[R/W] B,H,W 00000000 0010----		
00137C _H	ADTCS24[R/W] B,H,W 00000000 0010----		ADTCS25[R/W] B,H,W 00000000 0010----		
001380 _H	ADTCS26[R/W] B,H,W 00000000 0010----		ADTCS27[R/W] B,H,W 00000000 0010----		
001384 _H	ADTCS28[R/W] B,H,W 00000000 0010----		ADTCS29[R/W] B,H,W 00000000 0010----		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001388 _H	ADTCS30[R/W] B,H,W 00000000 0010----		ADTCS31[R/W] B,H,W 00000000 0010----		12-bit A/D converter 1/2 unit
00138C _H	ADTCD0[R] B,H,W 10--0000 00000000		ADTCD1[R] B,H,W 10--0000 00000000		
001390 _H	ADTCD2[R] B,H,W 10--0000 00000000		ADTCD3[R] B,H,W 10--0000 00000000		
001394 _H	ADTCD4[R] B,H,W 10--0000 00000000		ADTCD5[R] B,H,W 10--0000 00000000		
001398 _H	ADTCD6[R] B,H,W 10--0000 00000000		ADTCD7[R] B,H,W 10--0000 00000000		
00139C _H	ADTCD8[R] B,H,W 10--0000 00000000		ADTCD9[R] B,H,W 10--0000 00000000		
0013A0 _H	ADTCD10[R] B,H,W 10--0000 00000000		ADTCD11[R] B,H,W 10--0000 00000000		
0013A4 _H	ADTCD12[R] B,H,W 10--0000 00000000		ADTCD13[R] B,H,W 10--0000 00000000		
0013A8 _H	ADTCD14[R] B,H,W 10--0000 00000000		ADTCD15[R] B,H,W 10--0000 00000000		
0013AC _H	ADTCD16[R] B,H,W 10--0000 00000000		ADTCD17[R] B,H,W 10--0000 00000000		
0013B0 _H	ADTCD18[R] B,H,W 10--0000 00000000		ADTCD19[R] B,H,W 10--0000 00000000		
0013B4 _H	ADTCD20[R] B,H,W 10--0000 00000000		ADTCD21[R] B,H,W 10--0000 00000000		
0013B8 _H	ADTCD22[R] B,H,W 10--0000 00000000		ADTCD23[R] B,H,W 10--0000 00000000		
0013BC _H	ADTCD24[R] B,H,W 10--0000 00000000		ADTCD25[R] B,H,W 10--0000 00000000		
0013C0 _H	ADTCD26[R] B,H,W 10--0000 00000000		ADTCD27[R] B,H,W 10--0000 00000000		
0013C4 _H	ADTCD28[R] B,H,W 10--0000 00000000		ADTCD29[R] B,H,W 10--0000 00000000		
0013C8 _H	ADTCD30[R] B,H,W 10--0000 00000000		ADTCD31[R] B,H,W 10--0000 00000000		
0013CC _H	ADTECS0[R/W] B,H,W -----0 ---00000		ADTECS1[R/W] B,H,W -----0 ---00000		
0013D0 _H	ADTECS2[R/W] B,H,W -----0 ---00000		ADTECS3[R/W] B,H,W -----0 ---00000		
0013D4 _H	ADTECS4[R/W] B,H,W -----0 ---00000		ADTECS5[R/W] B,H,W -----0 ---00000		
0013D8 _H	ADTECS6[R/W] B,H,W -----0 ---00000		ADTECS7[R/W] B,H,W -----0 ---00000		
0013DC _H	ADTECS8[R/W] B,H,W -----0 ---00000		ADTECS9[R/W] B,H,W -----0 ---00000		
0013E0 _H	ADTECS10[R/W] B,H,W -----0 ---00000		ADTECS11[R/W] B,H,W -----0 ---00000		
0013E4 _H	ADTECS12[R/W] B,H,W -----0 ---00000		ADTECS13[R/W] B,H,W -----0 ---00000		
0013E8 _H	ADTECS14[R/W] B,H,W -----0 ---00000		ADTECS15[R/W] B,H,W -----0 ---00000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0013EC _H	ADTECS16[R/W] B,H,W -----0 ---00000		ADTECS17[R/W] B,H,W -----0 ---00000		12-bit A/D converter 1/2 unit
0013F0 _H	ADTECS18[R/W] B,H,W -----0 ---00000		ADTECS19[R/W] B,H,W -----0 ---00000		
0013F4 _H	ADTECS20[R/W] B,H,W -----0 ---00000		ADTECS21[R/W] B,H,W -----0 ---00000		
0013F8 _H	ADTECS22[R/W] B,H,W -----0 ---00000		ADTECS23[R/W] B,H,W -----0 ---00000		
0013FC _H	ADTECS24[R/W] B,H,W -----0 ---00000		ADTECS25[R/W] B,H,W -----0 ---00000		
001400 _H	ADTECS26[R/W] B,H,W -----0 ---00000		ADTECS27[R/W] B,H,W -----0 ---00000		
001404 _H	ADTECS28[R/W] B,H,W -----0 ---00000		ADTECS29[R/W] B,H,W -----0 ---00000		
001408 _H	ADTECS30[R/W] B,H,W -----0 ---00000		ADTECS31[R/W] B,H,W -----0 ---00000		
00140C _H	ADRCUT0[R/W] B,H,W ---0000 00000000		ADRCLT0[R/W] B,H,W ---0000 00000000		
001410 _H	ADRCUT1[R/W] B,H,W ---0000 00000000		ADRCLT1[R/W] B,H,W ---0000 00000000		
001414 _H	ADRCUT2[R/W] B,H,W ---0000 00000000		ADRCLT2[R/W] B,H,W ---0000 00000000		
001418 _H	ADRCUT3[R/W] B,H,W ---0000 00000000		ADRCLT3[R/W] B,H,W ---0000 00000000		
00141C _H	ADRCCS0[R/W] B,H,W 00000000	ADRCCS1[R/W] B,H,W 00000000	ADRCCS2[R/W] B,H,W 00000000	ADRCCS3[R/W] B,H,W 00000000	
001420 _H	ADRCCS4[R/W] B,H,W 00000000	ADRCCS5[R/W] B,H,W 00000000	ADRCCS6[R/W] B,H,W 00000000	ADRCCS7[R/W] B,H,W 00000000	
001424 _H	ADRCCS8[R/W] B,H,W 00000000	ADRCCS9[R/W] B,H,W 00000000	ADRCCS10[R/W] B,H,W 00000000	ADRCCS11[R/W] B,H,W 00000000	
001428 _H	ADRCCS12[R/W] B,H,W 00000000	ADRCCS13[R/W] B,H,W 00000000	ADRCCS14[R/W] B,H,W 00000000	ADRCCS15[R/W] B,H,W 00000000	
00142C _H	ADRCCS16[R/W] B,H,W 00000000	ADRCCS17[R/W] B,H,W 00000000	ADRCCS18[R/W] B,H,W 00000000	ADRCCS19[R/W] B,H,W 00000000	
001430 _H	ADRCCS20[R/W] B,H,W 00000000	ADRCCS21[R/W] B,H,W 00000000	ADRCCS22[R/W] B,H,W 00000000	ADRCCS23[R/W] B,H,W 00000000	
001434 _H	ADRCCS24[R/W] B,H,W 00000000	ADRCCS25[R/W] B,H,W 00000000	ADRCCS26[R/W] B,H,W 00000000	ADRCCS27[R/W] B,H,W 00000000	
001438 _H	ADRCCS28[R/W] B,H,W 00000000	ADRCCS29[R/W] B,H,W 00000000	ADRCCS30[R/W] B,H,W 00000000	ADRCCS31[R/W] B,H,W 00000000	
00143C _H	ADRCOT0[R] B,H,W 00000000 00000000 00000000 00000000				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001440 _H	ADRCIF0[R,W] B,H,W 00000000 00000000 00000000 00000000				12-bit A/D converter 1/2 unit
001444 _H	ADSCANS0[R/W] B,H,W 000-----	—	—	—	
001448 _H	ADNCS0[R/W] B,H,W 0-000-00	ADNCS1[R/W] B,H,W 0-000-00	ADNCS2[R/W] B,H,W 0-000-00	ADNCS3[R/W] B,H,W 0-000-00	
00144C _H	ADNCS4[R/W] B,H,W 0-000-00	ADNCS5[R/W] B,H,W 0-000-00	ADNCS6[R/W] B,H,W 0-000-00	ADNCS7[R/W] B,H,W 0-000-00	
001450 _H	ADNCS8[R/W] B,H,W 0-000-00	ADNCS9[R/W] B,H,W 0-000-00	ADNCS10[R/W] B,H,W 0-000-00	ADNCS11[R/W] B,H,W 0-000-00	
001454 _H	ADNCS12[R/W] B,H,W 0-000-00	ADNCS13[R/W] B,H,W 0-000-00	ADNCS14[R/W] B,H,W 0-000-00	ADNCS15[R/W] B,H,W 0-000-00	
001458 _H	ADPRTF0[R] B,H,W 00000000 00000000 00000000 00000000				
00145C _H	ADEOCF0[R] B,H,W 11111111 11111111 11111111 11111111				
001460 _H	ADCS0[R] B,H,W 0-----		ADCH0[R] B,H,W ---00000	ADMD0[R/W] B,H,W 0--0000	
001464 _H	ADSTPCS0[R/W] B,H,W 00000000	ADSTPCS1[R/W] B,H,W 00000000	ADSTPCS2[R/W] B,H,W 00000000	ADSTPCS3[R/W] B,H,W 00000000	
001468 _H	ADSTPCS4[R/W] B,H,W 00000000	ADSTPCS5[R/W] B,H,W 00000000	ADSTPCS6[R/W] B,H,W 00000000	ADSTPCS7[R/W] B,H,W 00000000	
00146C _H	—				
001470 _H	ADTSS1[R/W] B,H,W -----0	—	—	—	12-bit A/D converter 2/2 unit
001474 _H	ADTSE1[R/W] B,H,W 00000000 00000000 00000000 00000000				
001478 _H	ADCOMP32/ADCOMPB32[R/W] H,W 00000000 00000000		ADCOMP33/ADCOMPB33[R/W] H,W 00000000 00000000		
00147C _H	ADCOMP34/ADCOMPB34[R/W] H,W 00000000 00000000		ADCOMP35/ADCOMPB35[R/W] H,W 00000000 00000000		
001480 _H	ADCOMP36/ADCOMPB36[R/W] H,W 00000000 00000000		ADCOMP37/ADCOMPB37[R/W] H,W 00000000 00000000		
001484 _H	ADCOMP38/ADCOMPB38[R/W] H,W 00000000 00000000		ADCOMP39/ADCOMPB39[R/W] H,W 00000000 00000000		
001488 _H	ADCOMP40/ADCOMPB40[R/W] H,W 00000000 00000000		ADCOMP41/ADCOMPB41[R/W] H,W 00000000 00000000		
00148C _H	ADCOMP42/ADCOMPB42[R/W] H,W 00000000 00000000		ADCOMP43/ADCOMPB43[R/W] H,W 00000000 00000000		
001490 _H	ADCOMP44/ADCOMPB44[R/W] H,W 00000000 00000000		ADCOMP45/ADCOMPB45[R/W] H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001494 _H	ADCOMP46/ADCOMPB46[R/W] H,W 00000000 00000000		ADCOMP47/ADCOMPB47[R/W] H,W 00000000 00000000		12-bit A/D converter 2/2 unit
001498 _H	ADCOMP48/ADCOMPB48[R/W] H,W 00000000 00000000		ADCOMP49/ADCOMPB49[R/W] H,W 00000000 00000000		
00149C _H	ADCOMP50/ADCOMPB50[R/W] H,W 00000000 00000000		ADCOMP51/ADCOMPB51[R/W] H,W 00000000 00000000		
0014A0 _H	ADCOMP52/ADCOMPB52[R/W] H,W 00000000 00000000		ADCOMP53/ADCOMPB53[R/W] H,W 00000000 00000000		
0014A4 _H	ADCOMP54/ADCOMPB54[R/W] H,W 00000000 00000000		ADCOMP55/ADCOMPB55[R/W] H,W 00000000 00000000		
0014A8 _H	ADCOMP56/ADCOMPB56[R/W] H,W 00000000 00000000		ADCOMP57/ADCOMPB57[R/W] H,W 00000000 00000000		
0014AC _H	ADCOMP58/ADCOMPB58[R/W] H,W 00000000 00000000		ADCOMP59/ADCOMPB59[R/W] H,W 00000000 00000000		
0014B0 _H	ADCOMP60/ADCOMPB60[R/W] H,W 00000000 00000000		ADCOMP61/ADCOMPB61[R/W] H,W 00000000 00000000		
0014B4 _H	ADCOMP62/ADCOMPB62[R/W] H,W 00000000 00000000		ADCOMP63/ADCOMPB63[R/W] H,W 00000000 00000000		
0014B8 _H	ADTCS32[R/W] B,H,W 00000000 0010----		ADTCS33[R/W] B,H,W 00000000 0010----		
0014BC _H	ADTCS34[R/W] B,H,W 00000000 0010----		ADTCS35[R/W] B,H,W 00000000 0010----		
0014C0 _H	ADTCS36[R/W] B,H,W 00000000 0010----		ADTCS37[R/W] B,H,W 00000000 0010----		
0014C4 _H	ADTCS38[R/W] B,H,W 00000000 0010----		ADTCS39[R/W] B,H,W 00000000 0010----		
0014C8 _H	ADTCS40[R/W] B,H,W 00000000 0010----		ADTCS41[R/W] B,H,W 00000000 0010----		
0014CC _H	ADTCS42[R/W] B,H,W 00000000 0010----		ADTCS43[R/W] B,H,W 00000000 0010----		
0014D0 _H	ADTCS44[R/W] B,H,W 00000000 0010----		ADTCS45[R/W] B,H,W 00000000 0010----		
0014D4 _H	ADTCS46[R/W] B,H,W 00000000 0010----		ADTCS47[R/W] B,H,W 00000000 0010----		
0014D8 _H	ADTCS48[R/W] B,H,W 00000000 0010----		ADTCS49[R/W] B,H,W 00000000 0010----		
0014DC _H	ADTCS50[R/W] B,H,W 00000000 0010----		ADTCS51[R/W] B,H,W 00000000 0010----		
0014E0 _H	ADTCS52[R/W] B,H,W 00000000 0010----		ADTCS53[R/W] B,H,W 00000000 0010----		
0014E4 _H	ADTCS54[R/W] B,H,W 00000000 0010----		ADTCS55[R/W] B,H,W 00000000 0010----		
0014E8 _H	ADTCS56[R/W] B,H,W 00000000 0010----		ADTCS57[R/W] B,H,W 00000000 0010----		
0014EC _H	ADTCS58[R/W] B,H,W 00000000 0010----		ADTCS59[R/W] B,H,W 00000000 0010----		
0014F0 _H	ADTCS60[R/W] B,H,W 00000000 0010----		ADTCS61[R/W] B,H,W 00000000 0010----		
0014F4 _H	ADTCS62[R/W] B,H,W 00000000 0010----		ADTCS63[R/W] B,H,W 00000000 0010----		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0014F8 _H	ADTCD32[R] B,H,W 10--0000 00000000		ADTCD33[R] B,H,W 10--0000 00000000		12-bit A/D converter 2/2 unit
0014FC _H	ADTCD34[R] B,H,W 10--0000 00000000		ADTCD35[R] B,H,W 10--0000 00000000		
001500 _H	ADTCD36[R] B,H,W 10--0000 00000000		ADTCD37[R] B,H,W 10--0000 00000000		
001504 _H	ADTCD38[R] B,H,W 10--0000 00000000		ADTCD39[R] B,H,W 10--0000 00000000		
001508 _H	ADTCD40[R] B,H,W 10--0000 00000000		ADTCD41[R] B,H,W 10--0000 00000000		
00150C _H	ADTCD42[R] B,H,W 10--0000 00000000		ADTCD43[R] B,H,W 10--0000 00000000		
001510 _H	ADTCD44[R] B,H,W 10--0000 00000000		ADTCD45[R] B,H,W 10--0000 00000000		
001514 _H	ADTCD46[R] B,H,W 10--0000 00000000		ADTCD47[R] B,H,W 10--0000 00000000		
001518 _H	ADTCD48[R] B,H,W 10--0000 00000000		ADTCD49[R] B,H,W 10--0000 00000000		
00151C _H	ADTCD50[R] B,H,W 10--0000 00000000		ADTCD51[R] B,H,W 10--0000 00000000		
001520 _H	ADTCD52[R] B,H,W 10--0000 00000000		ADTCD53[R] B,H,W 10--0000 00000000		
001524 _H	ADTCD54[R] B,H,W 10--0000 00000000		ADTCD55[R] B,H,W 10--0000 00000000		
001528 _H	ADTCD56[R] B,H,W 10--0000 00000000		ADTCD57[R] B,H,W 10--0000 00000000		
00152C _H	ADTCD58[R] B,H,W 10--0000 00000000		ADTCD59[R] B,H,W 10--0000 00000000		
001530 _H	ADTCD60[R] B,H,W 10--0000 00000000		ADTCD61[R] B,H,W 10--0000 00000000		
001534 _H	ADTCD62[R] B,H,W 10--0000 00000000		ADTCD63[R] B,H,W 10--0000 00000000		
001538 _H	ADTECS32[R/W] B,H,W -----0 ---00000		ADTECS33[R/W] B,H,W -----0 ---00000		
00153C _H	ADTECS34[R/W] B,H,W -----0 ---00000		ADTECS35[R/W] B,H,W -----0 ---00000		
001540 _H	ADTECS36[R/W] B,H,W -----0 ---00000		ADTECS37[R/W] B,H,W -----0 ---00000		
001544 _H	ADTECS38[R/W] B,H,W -----0 ---00000		ADTECS39[R/W] B,H,W -----0 ---00000		
001548 _H	ADTECS40[R/W] B,H,W -----0 ---00000		ADTECS41[R/W] B,H,W -----0 ---00000		
00154C _H	ADTECS42[R/W] B,H,W -----0 ---00000		ADTECS43[R/W] B,H,W -----0 ---00000		
001550 _H	ADTECS44[R/W] B,H,W -----0 ---00000		ADTECS45[R/W] B,H,W -----0 ---00000		
001554 _H	ADTECS46[R/W] B,H,W -----0 ---00000		ADTECS47[R/W] B,H,W -----0 ---00000		
001558 _H	ADTECS48[R/W] B,H,W -----0 ---00000		ADTECS49[R/W] B,H,W -----0 ---00000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00155C _H	ADTECS50[R/W] B,H,W -----0 ---00000		ADTECS51[R/W] B,H,W -----0 ---00000		12-bit A/D converter 2/2 unit
001560 _H	ADTECS52[R/W] B,H,W -----0 ---00000		ADTECS53[R/W] B,H,W -----0 ---00000		
001564 _H	ADTECS54[R/W] B,H,W -----0 ---00000		ADTECS55[R/W] B,H,W -----0 ---00000		
001568 _H	ADTECS56[R/W] B,H,W -----0 ---00000		ADTECS57[R/W] B,H,W -----0 ---00000		
00156C _H	ADTECS58[R/W] B,H,W -----0 ---00000		ADTECS59[R/W] B,H,W -----0 ---00000		
001570 _H	ADTECS60[R/W] B,H,W -----0 ---00000		ADTECS61[R/W] B,H,W -----0 ---00000		
001574 _H	ADTECS62[R/W] B,H,W -----0 ---00000		ADTECS63[R/W] B,H,W -----0 ---00000		
001578 _H	ADRCUT4[R/W] B,H,W ---0000 00000000		ADRCLT4[R/W] B,H,W ---0000 00000000		
00157C _H	ADRCUT5[R/W] B,H,W ---0000 00000000		ADRCLT5[R/W] B,H,W ---0000 00000000		
001580 _H	ADRCUT6[R/W] B,H,W ---0000 00000000		ADRCLT6[R/W] B,H,W ---0000 00000000		
001584 _H	ADRCUT7[R/W] B,H,W ---0000 00000000		ADRCLT7[R/W] B,H,W ---0000 00000000		
001588 _H	ADRCCS32[R/W] B,H,W 00000000	ADRCCS33[R/W] B,H,W 00000000	ADRCCS34[R/W] B,H,W 00000000	ADRCCS35[R/W] B,H,W 00000000	
00158C _H	ADRCCS36[R/W] B,H,W 00000000	ADRCCS37[R/W] B,H,W 00000000	ADRCCS38[R/W] B,H,W 00000000	ADRCCS39[R/W] B,H,W 00000000	
001590 _H	ADRCCS40[R/W] B,H,W 00000000	ADRCCS41[R/W] B,H,W 00000000	ADRCCS42[R/W] B,H,W 00000000	ADRCCS43[R/W] B,H,W 00000000	
001594 _H	ADRCCS44[R/W] B,H,W 00000000	ADRCCS45[R/W] B,H,W 00000000	ADRCCS46[R/W] B,H,W 00000000	ADRCCS47[R/W] B,H,W 00000000	
001598 _H	ADRCCS48[R/W] B,H,W 00000000	ADRCCS49[R/W] B,H,W 00000000	ADRCCS50[R/W] B,H,W 00000000	ADRCCS51[R/W] B,H,W 00000000	
00159C _H	ADRCCS52[R/W] B,H,W 00000000	ADRCCS53[R/W] B,H,W 00000000	ADRCCS54[R/W] B,H,W 00000000	ADRCCS55[R/W] B,H,W 00000000	
0015A0 _H	ADRCCS56[R/W] B,H,W 00000000	ADRCCS57[R/W] B,H,W 00000000	ADRCCS58[R/W] B,H,W 00000000	ADRCCS59[R/W] B,H,W 00000000	
0015A4 _H	ADRCCS60[R/W] B,H,W 00000000	ADRCCS61[R/W] B,H,W 00000000	ADRCCS62[R/W] B,H,W 00000000	ADRCCS63[R/W] B,H,W 00000000	
0015A8 _H	ADRCOT1 [R] B,H,W 00000000 00000000 00000000 00000000				
0015AC _H	ADRCIF1 [R,W] B,H,W 00000000 00000000 00000000 00000000				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0015B0 _H	ADSCANS1 [R/W] B,H,W 000-----	—	—	—	12-bit A/D converter 2/2 unit
0015B4 _H	ADNCS16 [R/W] B,H,W 0-000-00	ADNCS17 [R/W] B,H,W 0-000-00	ADNCS18 [R/W] B,H,W 0-000-00	ADNCS19 [R/W] B,H,W 0-000-00	
0015B8 _H	ADNCS20 [R/W] B,H,W 0-000-00	ADNCS21 [R/W] B,H,W 0-000-00	ADNCS22 [R/W] B,H,W 0-000-00	ADNCS23 [R/W] B,H,W 0-000-00	
0015BC _H	ADNCS24 [R/W] B,H,W 0-000-00	ADNCS25 [R/W] B,H,W 0-000-00	ADNCS26 [R/W] B,H,W 0-000-00	ADNCS27 [R/W] B,H,W 0-000-00	
0015C0 _H	ADNCS28 [R/W] B,H,W 0-000-00	ADNCS29 [R/W] B,H,W 0-000-00	ADNCS30 [R/W] B,H,W 0-000-00	ADNCS31 [R/W] B,H,W 0-000-00	
0015C4 _H	ADPRTF1 [R] B,H,W 00000000 00000000 00000000 00000000				
0015C8 _H	ADEOCF1 [R] B,H,W 11111111 11111111 11111111 11111111				
0015CC _H	ADCS1 [R] B,H,W 0-----		ADCH1 [R] B,H,W ---00000	ADMD1 [R/W] B,H,W 0---0000	
0015D0 _H	ADSTPCS8 [R/W] B,H,W 00000000	ADSTPCS9 [R/W] B,H,W 00000000	ADSTPCS10 [R/W] B,H,W 00000000	ADSTPCS11 [R/W] B,H,W 00000000	
0015D4 _H	ADSTPCS12[R/W] B,H,W 00000000	ADSTPCS13[R/W] B,H,W 00000000	ADSTPCS14[R/W] B,H,W 00000000	ADSTPCS15[R/W] B,H,W 00000000	
0015D8 _H to 00174C _H	—	—	—	—	Reserved
001750 _H	SCR0/(IBCR0)[R/W] B,H,W 0--00000	SMR0[R/W] B,H,W 000-00-0	SSR0[R/W] B,H,W 0-000011	ESCR0/(IBSR0)[R/W]] B,H,W 00000000	Multi-UART0 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001754 _H	—/(RDR10/(TDR10))[R/W] B,H,W -----*3		RDR00/(TDR00)[R/W] B,H,W -----0 00000000*1		
001758 _H	SACSR0[R/W] B,H,W 0----000 00000000		STMR0[R] B,H,W 00000000 00000000		
00175C _H	STMCR0[R/W] B,H,W 00000000 00000000		—/(SCSCR0/SFUR0)[R/W] B,H,W -----*3 *4		
001760 _H	—/(SCSTR30)/ (LAMSR0) [R/W] B,H,W -----*3	—/(SCSTR20)/ (LAMCR0) [R/W] B,H,W -----*3	—/(SCSTR10) /(SFLR10) [R/W] B,H,W -----*3	—/(SCSTR00)/ (SFLR00) [R/W] B,H,W -----*3	
001764 _H	—	—/(SCSFR20) [R/W] B,H,W -----*3	—/(SCSFR10) [R/W] B,H,W -----*3	—/(SCSFR00) [R/W] B,H,W -----*3	
001768 _H	—/(TBYTE30)/ (LAMESR0) [R/W] B,H,W -----*3	—/(TBYTE20) /(LAMERT0) [R/W] B,H,W -----*3	—/(TBYTE10)/ (LAMIER0) [R/W] B,H,W -----*3	TBYTE00/(LAMRID0) /(LAMTID0) [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00176C _H	BGR0[R/W] H, W 00000000 00000000		— /(ISMK0) [R/W] B,H,W -----*2	— /(ISBA0) [R/W] B,H,W -----*2	Multi-UART0 *2: Reserved because I ² C mode is not set immediately after reset.
001770 _H	FCR10[R/W] B,H,W ---00100	FCR00[R/W] B,H,W -0000000	FBYTE0[R/W] B,H,W 00000000 00000000		
001774 _H	FTICR0[R/W] B,H,W 00000000 00000000		—	—	
001778 _H	SCR1/(IBCR1) [R/W] B,H,W 0--00000	SMR1[R/W] B,H,W 000-00-0	SSR1[R/W] B,H,W 0-000011	ESCR1/(IBSR1)[R/W]] B,H,W 00000000	Multi-UART1 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
00177C _H	— /(RDR11/(TDR11))[R/W] B,H,W -----*3		RDR01/(TDR01)[R/W] B,H,W -----0 00000000*1		
001780 _H	SACSR1[R/W] B,H,W 0---000 00000000		STMR1[R] B,H,W 00000000 00000000		
001784 _H	STMCR1[R/W] B,H,W 00000000 00000000		— /(SCSCR1/SFUR1)[R/W] B,H,W -----*3 *4		
001788 _H	— /(SCSTR31)/ (LAMSR1) [R/W] B,H,W -----*3	— /(SCSTR21)/ (LAMCR1) [R/W] B,H,W -----*3	— /(SCSTR11)/ (SFLR11) [R/W] B,H,W -----*3	— /(SCSTR01)/ (SFLR01) [R/W] B,H,W -----*3	
00178C _H	—	— /(SCSFR21)[R/W] B,H,W -----*3	— /(SCSFR11) [R/W] B,H,W -----*3	— /(SCSFR01) [R/W] B,H,W -----*3	
001790 _H	—/(TBYTE31)/ (LAMESR1) [R/W] B,H,W -----*3	—/(TBYTE21)/ (LAMERT1) [R/W] B,H,W -----*3	—/(TBYTE11)/ (LAMIER1) [R/W] B,H,W -----*3	TBYTE01/(LAMRID1) /(LAMTID1) [R/W] B,H,W 00000000	
001794 _H	BGR1[R/W] H,W 00000000 00000000		— /(ISMK1)[R/W] B,H,W -----*2	— /(ISBA1)[R/W] B,H,W -----*2	
001798 _H	FCR11[R/W] B,H,W ---00100	FCR01[R/W] B,H,W -0000000	FBYTE1[R/W] B,H,W 00000000 00000000		
00179C _H	FTICR1[R/W] B,H,W 00000000 00000000		—	—	
0017A0 _H	SCR2/(IBCR2)[R/W] B,H,W 0--00000	SMR2[R/W] B,H,W 000-00-0	SSR2[R/W] B,H,W 0-000011	ESCR2/(IBSR2)[R/W]] B,H,W 00000000	Multi-UART2 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset.
0017A4 _H	— /(RDR12/(TDR12))[R/W] B,H,W -----*3		RDR02/(TDR02)[R/W] B,H,W -----0 00000000*1		
0017A8 _H	SACSR2[R/W] B,H,W 0---000 00000000		STMR2[R] B,H,W 00000000 00000000		
0017AC _H	STMCR2[R/W] B,H,W 00000000 00000000		— /(SCSCR2/SFUR2)[R/W] B,H,W -----*3 *4		
0017B0 _H	— /(SCSTR32)/ (LAMSR2) [R/W] B,H,W -----*3	— /(SCSTR22)/ (LAMCR2) [R/W] B,H,W -----*3	— /(SCSTR12)/ (SFLR12) [R/W] B,H,W -----*3	— /(SCSTR02)/ (SFLR02) [R/W] B,H,W -----*3	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0017B4 _H	—	—/(SCSFR22) [R/W] B,H,W -----*3	—/(SCSFR12) [R/W] B,H,W -----*3	—/(SCSFR02) [R/W] B,H,W -----*3	Multi-UART2 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
0017B8 _H	—/(TBYTE32)/ (LAMESR2) [R/W] B,H,W -----*3	—/(TBYTE22)/ (LAMERT2) [R/W] B,H,W -----*3	—/(TBYTE12)/ (LAMIER2) [R/W] B,H,W -----*3	TBYTE02/(LAMRID2) /(LAMTID2) [R/W] B,H,W 00000000	
0017BC _H	BGR2[R/W] H, W 00000000 00000000		—/(ISMK2)[R/W] B,H,W -----*2	—/(ISBA2)[R/W] B,H,W -----*2	
0017C0 _H	FCR12[R/W] B,H,W ---00100	FCR02[R/W] B,H,W -0000000	FBYTE2[R/W] B,H,W 00000000 00000000		
0017C4 _H	FTICR2[R/W] B,H,W 00000000 00000000		—	—	
0017C8 _H	SCR3/(IBCR3) [R/W] B,H,W 0--00000	SMR3[R/W] B,H,W 000-00-0	SSR3[R/W] B,H,W 0-000011	ESCR3/(IBSR3)[R/W]] B,H,W 00000000	Multi-UART3 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
0017CC _H	—/(RDR13/(TDR13))[R/W] B,H,W -----*3		RDR03/(TDR03)[R/W] B,H,W -----0 00000000*1		
0017D0 _H	SACSR3[R/W] B,H,W 0---000 00000000		STMR3[R] B,H,W 00000000 00000000		
0017D4 _H	STMCR3[R/W] B,H,W 00000000 00000000		—/(SCSCR3/SFUR3)[R/W] B,H,W -----*3 *4		
0017D8 _H	—/(SCSTR33)/ (LAMSR3) [R/W] B,H,W -----*3	—/(SCSTR23)/ (LAMCR3) [R/W] B,H,W -----*3	—/(SCSTR13)/ (SFLR13) [R/W] B,H,W -----*3	—/(SCSTR03)/ (SFLR03) [R/W] B,H,W -----*3	
0017DC _H	—	—/(SCSFR23) [R/W] B,H,W -----*3	—/(SCSFR13) [R/W] B,H,W -----*3	—/(SCSFR03) [R/W] B,H,W -----*3	
0017E0 _H	—/(TBYTE33)/ (LAMESR3) [R/W] B,H,W -----*3	—/(TBYTE23)/ (LAMERT3) [R/W] B,H,W -----*3	—/(TBYTE13)/ (LAMIER3) [R/W] B,H,W -----*3	TBYTE03/(LAMRID3) /(LAMTID3) [R/W] B,H,W 00000000	
0017E4 _H	BGR3[R/W] H, W 00000000 00000000		—/(ISMK3)[R/W] B,H,W -----*2	—/(ISBA3)[R/W] B,H,W -----*2	
0017E8 _H	FCR13[R/W] B,H,W ---00100	FCR03[R/W] B,H,W -0000000	FBYTE3[R/W] B,H,W 00000000 00000000		
0017EC _H	FTICR3[R/W] B,H,W 00000000 00000000		—	—	
0017F0 _H	SCR4/(IBCR4) [R/W] B,H,W 0--00000	SMR4[R/W] B,H,W 000-00-0	SSR4[R/W] B,H,W 0-000011	ESCR4/(IBSR4)[R/W]] B,H,W 00000000	Multi-UART4 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset.
0017F4 _H	—/(RDR14/(TDR14))[R/W] B,H,W -----*3		RDR04/(TDR04)[R/W] B,H,W -----0 00000000*1		
0017F8 _H	SACSR4[R/W] B,H,W 0---000 00000000		STMR4[R] B,H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0017FC _H	STMCR4[R/W] B,H,W 00000000 00000000		— /(SCSCR4/SFUR4)[R/W] B,H,W -----*3 *4		Multi-UART4 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001800 _H	— /(SCSTR34)/ (LAMSR4) [R/W] B,H,W -----*3	— /(SCSTR24)/ (LAMCR4) [R/W] B,H,W -----*3	— /(SCSTR14)/ (SFLR14) [R/W] B,H,W -----*3	— /(SCSTR04)/ (SFLR04) [R/W] B,H,W -----*3	
001804 _H	—	— /(SCSFR24) [R/W] B,H,W -----*3	— /(SCSFR14) [R/W] B,H,W -----*3	— /(SCSFR04) [R/W] B,H,W -----*3	
001808 _H	—/(TBYTE34)/ (LAMESR4) [R/W] B,H,W -----*3	—/(TBYTE24)/ (LAMERT4) [R/W] B,H,W -----*3	—/(TBYTE14)/ (LAMIER4) [R/W] B,H,W -----*3	TBYTE04/(LAMRID4) /(LAMTID4) [R/W] B,H,W 00000000	
00180C _H	BGR4[R/W] H, W 00000000 00000000		— /(ISMK4)[R/W] B,H,W -----*2	— /(ISBA4)[R/W] B,H,W -----*2	
001810 _H	FCR14[R/W] B,H,W ---00100	FCR04[R/W] B,H,W -0000000	FBYTE4[R/W] B,H,W 00000000 00000000		
001814 _H	FTICR4[R/W] B,H,W 00000000 00000000		—	—	
001818 _H	SCR5/(IBCR5) [R/W] B,H,W 0-00000	SMR5[R/W] B,H,W 000-00-0	SSR5[R/W] B,H,W 0-000011	ESCR5/(IBSR5)[R/W]] B,H,W 00000000	Multi-UART5 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
00181C _H	— /(RDR15/(TDR15))[R/W] B,H,W -----*3		RDR05/(TDR05)[R/W] B,H,W -----0 00000000*1		
001820 _H	SACSR5[R/W] B,H,W 0----000 00000000		STMR5[R] B,H,W 00000000 00000000		
001824 _H	STMCR5[R/W] B,H,W 00000000 00000000		— /(SCSCR5/SFUR5)[R/W] B,H,W -----*3 *4		
001828 _H	— /(SCSTR35)/ (LAMSR5) [R/W] B,H,W -----*3	— /(SCSTR25)/ (LAMCR5) [R/W] B,H,W -----*3	— /(SCSTR15)/ (SFLR15) [R/W] B,H,W -----*3	— /(SCSTR05)/ (SFLR05) [R/W] B,H,W -----*3	
00182C _H	—	— /(SCSFR25) [R/W] B,H,W -----*3	— /(SCSFR15) [R/W] B,H,W -----*3	— /(SCSFR05) [R/W] B,H,W -----*3	
001830 _H	—/(TBYTE35)/ (LAMESR5) [R/W] B,H,W -----*3	—/(TBYTE25)/ (LAMERT5) [R/W] B,H,W -----*3	—/(TBYTE15)/ (LAMIER5) [R/W] B,H,W -----*3	TBYTE05/(LAMRID5) /(LAMTID5) [R/W] B,H,W 00000000	
001834 _H	BGR5[R/W] H, W 00000000 00000000		— /(ISMK5)[R/W] B,H,W -----*2	— /(ISBA5)[R/W] B,H,W -----*2	
001838 _H	FCR15[R/W] B,H,W ---00100	FCR05[R/W] B,H,W -0000000	FBYTE5[R/W] B,H,W 00000000 00000000		
00183C _H	FTICR5[R/W] B,H,W 00000000 00000000		—	—	

MB91F527R/MB91F527U/MB91F527M/MB91F527Y MB91F528R/MB91F528U/MB91F528M/MB91F528Y

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001840 _H	SCR6/(IBCR6) [R/W] B,H,W 0--00000	SMR6[R/W] B,H,W 000-00-0	SSR6[R/W] B,H,W 0-000011	ESCR6/(IBSR6)[R/W]] B,H,W 00000000	Multi-UART6 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001844 _H	—/(RDR16/(TDR16))[R/W] B,H,W -----*3		RDR06/(TDR06)[R/W] B,H,W -----0 00000000*1		
001848 _H	SACSR6[R/W] B,H,W 0---000 00000000		STMR6[R] B,H,W 00000000 00000000		
00184C _H	STMCR6[R/W] B,H,W 00000000 00000000		—/(SCSCR6/SFUR6)[R/W] B,H,W -----*3 *4		
001850 _H	—/(SCSTR36)/ (LAMSR6) [R/W] B,H,W -----*3	—/(SCSTR26)/ (LAMCR6) [R/W] B,H,W -----*3	—/(SCSTR16)/ (SFLR16) [R/W] B,H,W -----*3	—/(SCSTR06)/ (SFLR06) [R/W] B,H,W -----*3	
001854 _H	—	—/(SCSFR26) [R/W] B,H,W -----*3	—/(SCSFR16) [R/W] B,H,W -----*3	—/(SCSFR06) [R/W] B,H,W -----*3	
001858 _H	—/(TBYTE36)/ (LAMESR6) [R/W] B,H,W -----*3	—/(TBYTE26)/ (LAMERT6) [R/W] B,H,W -----*3	—/(TBYTE16)/ (LAMIER6) [R/W] B,H,W -----*3	TBYTE06/(LAMRID6) /(LAMTID6) [R/W] B,H,W 00000000	
00185C _H	BGR6[R/W] H, W 00000000 00000000		—/(ISMK6)[R/W] B,H,W -----*2	—/(ISBA6)[R/W] B,H,W -----*2	
001860 _H	FCR16[R/W] B,H,W ---00100	FCR06[R/W] B,H,W -0000000	FBYTE6[R/W] B,H,W 00000000 00000000		
001864 _H	FTICR6[R/W] B,H,W 00000000 00000000		—	—	
001868 _H	SCR7/(IBCR7) [R/W] B,H,W 0--00000	SMR7[R/W] B,H,W 000-00-0	SSR7[R/W] B,H,W 0-000011	ESCR7/(IBSR7)[R/W]] B,H,W 00000000	Multi-UART7 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
00186C _H	—/(RDR17/(TDR17))[R/W] B,H,W -----*3		RDR07/(TDR07)[R/W] B,H,W -----0 00000000*1		
001870 _H	SACSR7[R/W] B,H,W 0---000 00000000		STMR7[R] B,H,W 00000000 00000000		
001874 _H	STMCR7[R/W] B,H,W 00000000 00000000		—/(SCSCR7/SFUR7)[R/W] B,H,W -----*3 *4		
001878 _H	—/(SCSTR37)/ (LAMSR7) [R/W] B,H,W -----*3	—/(SCSTR27)/ (LAMCR7) [R/W] B,H,W -----*3	—/(SCSTR17)/ (SFLR17) [R/W] B,H,W -----*3	—/(SCSTR07)/ (SFLR07) [R/W] B,H,W -----*3	
00187C _H	—	—/(SCSFR27) [R/W] B,H,W -----*3	—/(SCSFR17) [R/W] B,H,W -----*3	—/(SCSFR07) [R/W] B,H,W -----*3	
001880 _H	—/(TBYTE37)/ (LAMESR7) [R/W] B,H,W -----*3	—/(TBYTE27)/ (LAMERT7) [R/W] B,H,W -----*3	—/(TBYTE17)/ (LAMIER7) [R/W] B,H,W -----*3	TBYTE07/(LAMRID7) /(LAMTID7) [R/W] B,H,W 00000000	

MB91F527R/MB91F527U/MB91F527M/MB91F527Y MB91F528R/MB91F528U/MB91F528M/MB91F528Y

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001884 _H	BGR7[R/W] H, W 00000000 00000000		— /(ISMK7)[R/W] B,H,W -----*2	— /(ISBA7)[R/W] B,H,W -----*2	Multi-UART7
001888 _H	FCR17[R/W] B,H,W ---00100	FCR07[R/W] B,H,W -0000000	FBYTE7[R/W] B,H,W 00000000 00000000		
00188C _H	FTICR7[R/W] B,H,W 00000000 00000000		—	—	
001890 _H	SCR8/(IBCR8) [R/W] B,H,W 0--00000	SMR8[R/W] B,H,W 000-00-0	SSR8[R/W] B,H,W 0-000011	ESCR8/(IBSR8)[R/W]] B,H,W 00000000	Multi-UART8 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001894 _H	— /(RDR18/(TDR18))[R/W] B,H,W -----*3		RDR08/(TDR08)[R/W] B,H,W -----0 00000000* ¹		
001898 _H	SACSR8[R/W] B,H,W 0---000 00000000		STMR8[R] B,H,W 00000000 00000000		
00189C _H	STMCR8[R/W] B,H,W 00000000 00000000		— /(SCSCR8/SFUR8)[R/W] B,H,W -----*3 * ⁴		
0018A0 _H	— /(SCSTR38)/ (LAMSR8) [R/W] B,H,W -----*3	— /(SCSTR28)/ (LAMCR8) [R/W] B,H,W -----*3	— /(SCSTR18)/ (SFLR18) [R/W] B,H,W -----*3	— /(SCSTR08)/ (SFLR08) [R/W] B,H,W -----*3	
0018A4 _H	—	— /(SCSFR28) [R/W] B,H,W -----*3	— /(SCSFR18) [R/W] B,H,W -----*3	— /(SCSFR08) [R/W] B,H,W -----*3	
0018A8 _H	—/(TBYTE38)/ (LAMESR8) [R/W] B,H,W -----*3	—/(TBYTE28)/ (LAMERT8) [R/W] B,H,W -----*3	—/(TBYTE18)/ (LAMIER8) [R/W] B,H,W -----*3	TBYTE08/(LAMRID8) /(LAMTID8) [R/W] B,H,W 00000000	
0018AC _H	BGR8[R/W] H,W 00000000 00000000		— /(ISMK8)[R/W] B,H,W -----*2	— /(ISBA8)[R/W] B,H,W -----*2	
0018B0 _H	FCR18[R/W] B,H,W ---00100	FCR08[R/W] B,H,W -0000000	FBYTE8[R/W] B,H,W 00000000 00000000		
0018B4 _H	FTICR8[R/W] B,H,W 00000000 00000000		—	—	
0018B8 _H	SCR9/(IBCR9) [R/W] B,H,W 0--00000	SMR9[R/W] B,H,W 000-00-0	SSR9[R/W] B,H,W 0-000011	ESCR9/(IBSR9)[R/W]] B,H,W 00000000	Multi-UART9 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset.
0018BC _H	— /(RDR19/(TDR19))[R/W] B,H,W -----*3		RDR09/(TDR09)[R/W] B,H,W -----0 00000000* ¹		
0018C0 _H	SACSR9[R/W] B,H,W 0---000 00000000		STMR9[R] B,H,W 00000000 00000000		
0018C4 _H	STMCR9[R/W] B,H,W 00000000 00000000		— /(SCSCR9/SFUR9)[R/W] B,H,W -----*3 * ⁴		
0018C8 _H	— /(SCSTR39)/ (LAMSR9) [R/W] B,H,W -----*3	— /(SCSTR29)/ (LAMCR9) [R/W] B,H,W -----*3	— /(SCSTR19)/ (SFLR19) [R/W] B,H,W -----*3	— /(SCSTR09)/ (SFLR09) [R/W] B,H,W -----*3	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0018CC _H	—	—/(SCSFR29) [R/W] B,H,W -----*3	—/(SCSFR19) [R/W] B,H,W -----*3	—/(SCSFR09) [R/W] B,H,W -----*3	Multi-UART9 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
0018D0 _H	—/(TBYTE39)/ (LAMESR9) [R/W] B,H,W -----*3	—/(TBYTE29)/ (LAMERT9) [R/W] B,H,W -----*3	—/(TBYTE19)/ (LAMIER9) [R/W] B,H,W -----*3	TBYTE09/(LAMRID9) /(LAMTID9) [R/W] B,H,W 00000000	
0018D4 _H	BGR9[R/W] H, W 00000000 00000000		—/(ISMK9)[R/W] B,H,W -----*2	—/(ISBA9)[R/W] B,H,W -----*2	
0018D8 _H	FCR19[R/W] B,H,W ---00100	FCR09[R/W] B,H,W -0000000	FBYTE9[R/W] B,H,W 00000000 00000000		
0018DC _H	FTICR9[R/W] B,H,W 00000000 00000000		—	—	Multi-UART10 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
0018E0 _H	SCR10/(IBCR10) [R/W] B,H,W 0--00000	SMR10[R/W] B,H,W 000-00-0	SSR10[R/W] B,H,W 0-000011	ESCR10/(IBSR10) [R/W] B,H,W 00000000	
0018E4 _H	—/(RDR110/(TDR110))[R/W] B,H,W -----*3		RDR010/(TDR010)[R/W] B,H,W -----0 00000000*1		
0018E8 _H	SACSR10[R/W] B,H,W 0---000 00000000		STMR10[R] B,H,W 00000000 00000000		
0018EC _H	STMCR10[R/W] B,H,W 00000000 00000000		—/(SCSCR10/SFUR10)[R/W] B,H,W -----*3 *4		
0018F0 _H	—/(SCSTR310)/ (LAMSR10) [R/W] B,H,W -----*3	—/(SCSTR210)/ (LAMCR10) [R/W] B,H,W -----*3	—/(SCSTR110)/ (SFLR110)[R/W] B,H,W -----*3	—/(SCSTR010)/ (SFLR010)[R/W] B,H,W -----*3	
0018F4 _H	—	—/(SCSFR210) [R/W] B,H,W -----*3	—/(SCSFR110) [R/W] B,H,W -----*3	—/(SCSFR010) [R/W] B,H,W -----*3	
0018F8 _H	—/(TBYTE310)/ (LAMESR10) [R/W] B,H,W -----*3	—/(TBYTE210)/ (LAMERT10) [R/W] B,H,W -----*3	—/(TBYTE110)/ (LAMIER10) [R/W] B,H,W -----*3	TBYTE010/(LAMRID10)/(LAMTID10) [R/W] B,H,W 00000000	
0018FC _H	BGR10[R/W] H, W 00000000 00000000		—/(ISMK10)[R/W] B,H,W -----*2	—/(ISBA10)[R/W] B,H,W -----*2	
001900 _H	FCR110[R/W] B,H,W ---00100	FCR010[R/W] B,H,W -0000000	FBYTE10[R/W] B,H,W 00000000 00000000		
001904 _H	FTICR10[R/W] B,H,W 00000000 00000000		—	—	
001908 _H	SCR11/(IBCR11) [R/W] B,H,W 0--00000	SMR11[R/W] B,H,W 000-00-0	SSR11[R/W] B,H,W 0-000011	ESCR11/(IBSR11) [R/W] B,H,W 00000000	Multi-UART11 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset.
00190C _H	—/(RDR111/(TDR111))[R/W] B,H,W -----*3		RDR011/(TDR011)[R/W] B,H,W -----0 00000000*1		
001910 _H	SACSR11[R/W] B,H,W 0---000 00000000		STMR11[R] B,H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001914 _H	STMCR11[R/W] B,H,W 00000000 00000000		— /(SCSCR11/SFUR11)[R/W] B,H,W -----*3 *4		Multi-UART11
001918 _H	— /(SCSTR311)/ (LAMSR11) [R/W] B,H,W -----*3	— /(SCSTR211)/ (LAMCR11) [R/W] B,H,W -----*3	— /(SCSTR111)/ (SFLR111)[R/W] B,H,W -----*3	— /(SCSTR011)/ (SFLR011)[R/W] B,H,W -----*3	
00191C _H	—	— /(SCSFR211) [R/W] B,H,W -----*3	— /(SCSFR111) [R/W] B,H,W -----*3	— /(SCSFR011) [R/W] B,H,W -----*3	
001920 _H	—/(TBYTE311)/ (LAMESR11) [R/W] B,H,W -----*3	—/(TBYTE211)/ (LAMERT11) [R/W] B,H,W -----*3	—/(TBYTE111)/ (LAMIER11) [R/W] B,H,W -----*3	TBYTE011/(LAMRID 11)/(LAMTID11) [R/W] B,H,W 00000000	
001924 _H	BGR11[R/W] H, W 00000000 00000000		— /(ISMK11)[R/W] B,H,W -----*2	— /(ISBA11)[R/W] B,H,W -----*2	
001928 _H	FCR111[R/W] B,H,W ---00100	FCR011[R/W] B,H,W -0000000	FBYTE11[R/W] B,H,W 00000000 00000000		
00192C _H	FTICR11[R/W] B,H,W 00000000 00000000		—	—	
001930 _H	SCR12/(IBCR12) [R/W] B,H,W 0--00000	SMR12 [R/W] B,H,W 000-00-0	SSR12 [R/W] B,H,W 0-000011	ESCR12/(IBSR12) [R/W] B,H,W 00000000	Multi-UART12
001934 _H	— /(RDR112/(TDR112))[R/W] B,H,W -----*3		RDR012/(TDR012)[R/W] B,H,W -----0 00000000*1		
001938 _H	SACSR12[R/W] B,H,W 0----000 00000000		STMR12[R] B,H,W 00000000 00000000		
00193C _H	STMCR12[R/W] B,H,W 00000000 00000000		— /(SCSCR12/SFUR12)[R/W] B,H,W -----*3 *4		
001940 _H	— /(SCSTR312)/ (LAMSR12) [R/W] B,H,W -----*3	— /(SCSTR212)/ (LAMCR12) [R/W] B,H,W -----*3	— /(SCSTR112)/(SFLR1 12) [R/W] B,H,W -----*3	— /(SCSTR012)/(SFLR 012) [R/W] B,H,W -----*3	
001944 _H	—	— /(SCSFR212) [R/W] B,H,W -----*3	— /(SCSFR112) [R/W] B,H,W -----*3	— /(SCSFR012) [R/W] B,H,W -----*3	
001948 _H	—/(TBYTE312)/ (LAMESR12) [R/W] B,H,W -----*3	—/(TBYTE212)/ (LAMERT12) [R/W] B,H,W -----*3	—/(TBYTE112)/ (LAMIER12) [R/W] B,H,W -----*3	TBYTE012/(LAMRID 12)/(LAMTID12) [R/W] B,H,W 00000000	
00194C _H	BGR12[R/W] H,W 00000000 00000000		— /(ISMK12) [R/W] B,H,W -----*2	— /(ISBA12) [R/W] B,H,W -----*2	
001950 _H	FCR112 [R/W] B,H,W ---00100	FCR012 [R/W] B,H,W -0000000	FBYTE12[R/W] B,H,W 00000000 00000000		
001954 _H	FTICR12[R/W] B,H,W 00000000 00000000		—	—	

*3: Reserved because CSIO mode is not set immediately after reset.

*4: Reserved because LIN2.1 mode is not set immediately after reset.

*1: Byte access is possible only for access to lower 8 bits.

*2: Reserved because I²C mode is not set immediately after reset.

*3: Reserved because CSIO mode is not set immediately after reset.

*4: Reserved because LIN2.1 mode is not set immediately after reset.

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001958 _H	SCR13/(IBCR13) [R/W] B,H,W 0--00000	SMR13 [R/W] B,H,W 000-00-0	SSR13 [R/W] B,H,W 0-000011	ESCR13/(IBSR13) [R/W] B,H,W 00000000	Multi-UART13 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
00195C _H	—/(RDR113/(TDR113))[R/W] B,H,W -----*3		RDR013/(TDR013)[R/W] B,H,W -----0 00000000*1		
001960 _H	SACSR13[R/W] B,H,W 0----000 00000000		STMR13[R] B,H,W 00000000 00000000		
001964 _H	STMCR13[R/W] B,H,W 00000000 00000000		—/(SCSCR13/SFUR13)[R/W] B,H,W -----*3 *4		
001968 _H	—/(SCSTR313)/ (LAMSR13) [R/W] B,H,W -----*3	—/(SCSTR213)/ (LAMCR13) [R/W] B,H,W -----*3	—/(SCSTR113)/(SFLR1 13) [R/W] B,H,W -----*3	—/(SCSTR013)/(SFLR 013) [R/W] B,H,W -----*3	
00196C _H	—	—/(SCSFR213) [R/W] B,H,W -----*3	—/(SCSFR113) [R/W] B,H,W -----*3	—/(SCSFR013) [R/W] B,H,W -----*3	
001970 _H	—/(TBYTE313)/ (LAMESR13) [R/W] B,H,W -----*3	—/(TBYTE213)/ (LAMERT13) [R/W] B,H,W -----*3	—/(TBYTE113)/ (LAMIER13) [R/W] B,H,W -----*3	TBYTE013/(LAMRID 13)/(LAMTID13) [R/W] B,H,W 00000000	
001974 _H	BGR13[R/W] H,W 00000000 00000000		—/(ISMK13) [R/W] B,H,W -----*2	—/(ISBA13) [R/W] B,H,W -----*2	
001978 _H	FCR113 [R/W] B,H,W ---00100	FCR013 [R/W] B,H,W -0000000	FBYTE13[R/W] B,H,W 00000000 00000000		
00197C _H	FTICR13[R/W] B,H,W 00000000 00000000		—	—	
001980 _H	SCR14/(IBCR14) [R/W] B,H,W 0--00000	SMR14 [R/W] B,H,W 000-00-0	SSR14 [R/W] B,H,W 0-000011	ESCR14/(IBSR14) [R/W] B,H,W 00000000	Multi-UART14 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001984 _H	—/(RDR114/(TDR114))[R/W] B,H,W -----*3		RDR014/(TDR014)[R/W] B,H,W -----0 00000000*1		
001988 _H	SACSR14[R/W] B,H,W 0----000 00000000		STMR14[R] B,H,W 00000000 00000000		
00198C _H	STMCR14[R/W] B,H,W 00000000 00000000		—/(SCSCR14/SFUR14)[R/W] B,H,W -----*3 *4		
001990 _H	—/(SCSTR314)/ (LAMSR14) [R/W] B,H,W -----*3	—/(SCSTR214)/ (LAMCR14) [R/W] B,H,W -----*3	—/(SCSTR114)/(SFLR1 14) [R/W] B,H,W -----*3	—/(SCSTR014)/(SFLR 014) [R/W] B,H,W -----*3	
001994 _H	—	—/(SCSFR214) [R/W] B,H,W -----*3	—/(SCSFR114) [R/W] B,H,W -----*3	—/(SCSFR014) [R/W] B,H,W -----*3	
001998 _H	—/(TBYTE314)/ (LAMESR14) [R/W] B,H,W -----*3	—/(TBYTE214)/ (LAMERT14) [R/W] B,H,W -----*3	—/(TBYTE114)/ (LAMIER14) [R/W] B,H,W -----*3	TBYTE014/(LAMRID 14)/(LAMTID14) [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00199C _H	BGR14[R/W] H,W 00000000 00000000		— /(ISMK14) [R/W] B,H,W -----*2	— /(ISBA14) [R/W] B,H,W -----*2	Multi-UART14
0019A0 _H	FCR114 [R/W] B,H,W ---00100	FCR014 [R/W] B,H,W -0000000	FBYTE14[R/W] B,H,W 00000000 00000000		
0019A4 _H	FTICR14[R/W] B,H,W 00000000 00000000		—	—	
0019A8 _H	SCR15/(IBCR15) [R/W] B,H,W 0--00000	SMR15 [R/W] B,H,W 000-00-0	SSR15 [R/W] B,H,W 0-000011	ESCR15/(IBSR15) [R/W] B,H,W 00000000	Multi-UART15 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
0019AC _H	— /(RDR115/(TDR115))[R/W] B,H,W -----*3		RDR015/(TDR015)[R/W] B,H,W -----0 00000000*1		
0019B0 _H	SACSR15[R/W] B,H,W 0---000 00000000		STMR15[R] B,H,W 00000000 00000000		
0019B4 _H	STMCR15[R/W] B,H,W 00000000 00000000		— /(SCSCR15/SFUR15)[R/W] B,H,W -----*3 *4		
0019B8 _H	— /(SCSTR315)/ (LAMSR15) [R/W] B,H,W -----*3	— /(SCSTR215)/ (LAMCR15) [R/W] B,H,W -----*3	— /(SCSTR115)/(SFLR15) [R/W] B,H,W -----*3	— /(SCSTR015)/(SFLR015) [R/W] B,H,W -----*3	
0019BC _H	—	— /(SCSFR215) [R/W] B,H,W -----*3	— /(SCSFR115) [R/W] B,H,W -----*3	— /(SCSFR015) [R/W] B,H,W -----*3	
0019C0 _H	— /(TBYTE315)/ (LAMESR15) [R/W] B,H,W -----*3	— /(TBYTE215)/ (LAMERT15) [R/W] B,H,W -----*3	— /(TBYTE115)/ (LAMIER15) [R/W] B,H,W -----*3	TBYTE015/(LAMRID15)/(LAMTID15) [R/W] B,H,W 00000000	
0019C4 _H	BGR15[R/W] H,W 00000000 00000000		— /(ISMK15) [R/W] B,H,W -----*2	— /(ISBA15) [R/W] B,H,W -----*2	
0019C8 _H	FCR115 [R/W] B,H,W ---00100	FCR015 [R/W] B,H,W -0000000	FBYTE15[R/W] B,H,W 00000000 00000000		
0019CC _H	FTICR15[R/W] B,H,W 00000000 00000000		—	—	
0019D0 _H	GTRS40 [R/W] B,H,W -0000000 -0000000		GTRS41 [R/W] B,H,W -0000000 -0000000		PPG controller
0019D4 _H	GTRS42 [R/W] B,H,W -0000000 -0000000		GTRS43 [R/W] B,H,W -0000000 -0000000		
0019D8 _H	GTREN4 [R/W] H,W 00000000 00000000		GTREN5 [R/W] H,W ----- 00000000		
0019DC _H	—	GATEC0 [R/W] B,H,W -----00	—	GATEC2 [R/W] B,H,W -----00	PPG GATE control
0019E0 _H	—	GATEC4 [R/W] B,H,W -----00	—	—	
0019E4 _H	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0019E8 _H	GTRS0 [R/W] B,H,W -0000000 -0000000		GTRS1 [R/W] B,H,W -0000000 -0000000		PPG controller
0019EC _H	GTRS2 [R/W] B,H,W -0000000 -0000000		GTRS3 [R/W] B,H,W -0000000 -0000000		
0019F0 _H	GTRS4 [R/W] B,H,W -0000000 -0000000		GTRS5 [R/W] B,H,W -0000000 -0000000		
0019F4 _H	GTRS6 [R/W] B,H,W -0000000 -0000000		GTRS7 [R/W] B,H,W -0000000 -0000000		
0019F8 _H	GTRS8 [R/W] B,H,W -0000000 -0000000		GTRS9 [R/W] B,H,W -0000000 -0000000		
0019FC _H	GTRS10 [R/W] B,H,W -0000000 -0000000		GTRS11 [R/W] B,H,W -0000000 -0000000		
001A00 _H	GTRS12 [R/W] B,H,W -0000000 -0000000		GTRS13 [R/W] B,H,W -0000000 -0000000		
001A04 _H	GTRS14 [R/W] B,H,W -0000000 -0000000		GTRS15 [R/W] B,H,W -0000000 -0000000		
001A08 _H	GTRS16 [R/W] B,H,W -0000000 -0000000		GTRS17 [R/W] B,H,W -0000000 -0000000		
001A0C _H	GTRS18 [R/W] B,H,W -0000000 -0000000		GTRS19 [R/W] B,H,W -0000000 -0000000		
001A10 _H	GTRS20 [R/W] B,H,W -0000000 -0000000		GTRS21 [R/W] B,H,W -0000000 -0000000		
001A14 _H	GTRS22 [R/W] B,H,W -0000000 -0000000		GTRS23 [R/W] B,H,W -0000000 -0000000		
001A18 _H	GTRS24 [R/W] B,H,W -0000000 -0000000		GTRS25 [R/W] B,H,W -0000000 -0000000		
001A1C _H	GTRS26 [R/W] B,H,W -0000000 -0000000		GTRS27 [R/W] B,H,W -0000000 -0000000		
001A20 _H	GTRS28 [R/W] B,H,W -0000000 -0000000		GTRS29 [R/W] B,H,W -0000000 -0000000		
001A24 _H	GTRS30 [R/W] B,H,W -0000000 -0000000		GTRS31 [R/W] B,H,W -0000000 -0000000		
001A28 _H	GTRS32 [R/W] B,H,W -0000000 -0000000		GTRS33 [R/W] B,H,W -0000000 -0000000		
001A2C _H	GTRS34 [R/W] B,H,W -0000000 -0000000		GTRS35 [R/W] B,H,W -0000000 -0000000		
001A30 _H	GTRS36 [R/W] B,H,W -0000000 -0000000		GTRS37 [R/W] B,H,W -0000000 -0000000		
001A34 _H	GTRS38 [R/W] B,H,W -0000000 -0000000		GTRS39 [R/W] B,H,W -0000000 -0000000		
001A38 _H	GTREN0 [R/W] H,W 00000000 00000000		GTREN1 [R/W] H,W 00000000 00000000		PPG controller
001A3C _H	GTREN2 [R/W] H,W 00000000 00000000		GTREN3 [R/W] H,W 00000000 00000000		
001A40 _H	PCN0 [R/W] B,H,W 00000000 000000-0		PCSR0 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG0 (Note) for communication
001A44 _H	PDUT0 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR0 [R] H,W 11111111 11111111		
001A48 _H	PCN200 [R/W] B,H,W --000000 -----110		PSDR0 [R/W] H,W 00000000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001A4C _H	PTPC0 [R/W] H,W 00000000 00000000		PCMDWD0 [R/W] B,H,W ----- ----0000		PPG0 (Note) for communication
001A50 _H	PHCSR0 [W] H,W XXXXXXXX XXXXXXXX		PLCSR0 [W] H,W XXXXXXXX XXXXXXXX		
001A54 _H	PHDUT0 [W] H,W XXXXXXXX XXXXXXXX		PLDUT0 [W] H,W XXXXXXXX XXXXXXXX		
001A58 _H	PCMDDT0 [R/W] H,W 00000000 00000000		—	—	
001A5C _H	PCN1 [R/W] B,H,W 00000000 000000-0		PCSR1 [W] H,W XXXXXXXX XXXXXXXX		PPG1 (Note) for communication
001A60 _H	PDUT1 [W] H,W XXXXXXXX XXXXXXXX		PTMR1 [R] H,W 11111111 11111111		
001A64 _H	PCN201 [R/W] B,H,W --000000 ----110		PSDR1 [R/W] H,W 00000000 00000000		
001A68 _H	PTPC1 [R/W] H,W 00000000 00000000		PCMDWD1 [R/W] B,H,W ----- ----0000		
001A6C _H	PHCSR1 [W] H,W XXXXXXXX XXXXXXXX		PLCSR1 [W] H,W XXXXXXXX XXXXXXXX		
001A70 _H	PHDUT1 [W] H,W XXXXXXXX XXXXXXXX		PLDUT1 [W] H,W XXXXXXXX XXXXXXXX		
001A74 _H	PCMDDT1 [R/W] H,W 00000000 00000000		—	—	
001A78 _H	PCN2 [R/W] B,H,W 00000000 000000-0		PCSR2 [W] H,W XXXXXXXX XXXXXXXX		PPG2 (Note) for communication
001A7C _H	PDUT2 [W] H,W XXXXXXXX XXXXXXXX		PTMR2 [R] H,W 11111111 11111111		
001A80 _H	PCN202 [R/W] B,H,W --000000 ----110		PSDR2 [R/W] H,W 00000000 00000000		
001A84 _H	PTPC2 [R/W] H,W 00000000 00000000		PCMDWD2 [R/W] B,H,W ----- ----0000		
001A88 _H	PHCSR2 [W] H,W XXXXXXXX XXXXXXXX		PLCSR2 [W] H,W XXXXXXXX XXXXXXXX		
001A8C _H	PHDUT2 [W] H,W XXXXXXXX XXXXXXXX		PLDUT2 [W] H,W XXXXXXXX XXXXXXXX		
001A90 _H	PCMDDT2 [R/W] H,W 00000000 00000000		—	—	
001A94 _H	PCN3 [R/W] B,H,W 00000000 000000-0		PCSR3 [W] H,W XXXXXXXX XXXXXXXX		PPG3 (Note) for communication
001A98 _H	PDUT3 [W] H,W XXXXXXXX XXXXXXXX		PTMR3 [R] H,W 11111111 11111111		
001A9C _H	PCN203 [R/W] B,H,W --000000 ----110		PSDR3 [R/W] H,W 00000000 00000000		
001AA0 _H	PTPC3 [R/W] H,W 00000000 00000000		PCMDWD3 [R/W] B,H,W ----- ----0000		
001AA4 _H	PHCSR3 [W] H,W XXXXXXXX XXXXXXXX		PLCSR3 [W] H,W XXXXXXXX XXXXXXXX		
001AA8 _H	PHDUT3 [W] H,W XXXXXXXX XXXXXXXX		PLDUT3 [W] H,W XXXXXXXX XXXXXXXX		
001AAC _H	PCMDDT3 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001AB0 _H	PCN4 [R/W] B,H,W 00000000 000000-0		PCSR4 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG4
001AB4 _H	PDUT4 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR4 [R] H,W 11111111 11111111		
001AB8 _H	PCN204 [R/W] B,H,W --000000 -----110		PSDR4 [R/W] H,W 00000000 00000000		
001ABC _H	PTPC4 [R/W] H,W 00000000 00000000		—	—	
001AC0 _H	PCN5 [R/W] B,H,W 00000000 000000-0		PCSR5 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG5
001AC4 _H	PDUT5 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR5 [R] H,W 11111111 11111111		
001AC8 _H	PCN205 [R/W] B,H,W --000000 -----110		PSDR5 [R/W] H,W 00000000 00000000		
001ACC _H	PTPC5 [R/W] H,W 00000000 00000000		—	—	
001AD0 _H	PCN6 [R/W] B,H,W 00000000 000000-0		PCSR6 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG6
001AD4 _H	PDUT6 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR6 [R] H,W 11111111 11111111		
001AD8 _H	PCN206 [R/W] B,H,W --000000 -----110		PSDR6 [R/W] H,W 00000000 00000000		
001ADC _H	PTPC6 [R/W] H,W 00000000 00000000		—	—	
001AE0 _H	PCN7 [R/W] B,H,W 00000000 000000-0		PCSR7 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG7
001AE4 _H	PDUT7 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR7 [R] H,W 11111111 11111111		
001AE8 _H	PCN207 [R/W] B,H,W --000000 -----110		PSDR7 [R/W] H,W 00000000 00000000		
001AEC _H	PTPC7 [R/W] H,W 00000000 00000000		—	—	
001AF0 _H	PCN8 [R/W] B,H,W 00000000 000000-0		PCSR8 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG8
001AF4 _H	PDUT8 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR8 [R] H,W 11111111 11111111		
001AF8 _H	PCN208 [R/W] B,H,W --000000 -----110		PSDR8 [R/W] H,W 00000000 00000000		
001AFC _H	PTPC8 [R/W] H,W 00000000 00000000		—	—	
001B00 _H	PCN9 [R/W] B,H,W 00000000 000000-0		PCSR9 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG9
001B04 _H	PDUT9 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR9 [R] H,W 11111111 11111111		
001B08 _H	PCN209 [R/W] B,H,W --000000 -----110		PSDR9 [R/W] H,W 00000000 00000000		
001B0C _H	PTPC9 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001B10 _H	PCN10 [R/W] B,H,W 00000000 000000-0		PCSR10 [W] H,W XXXXXXXX XXXXXXXX		PPG10
001B14 _H	PDUT10 [W] H,W XXXXXXXX XXXXXXXX		PTMR10 [R] H,W 11111111 11111111		
001B18 _H	PCN210 [R/W] B,H,W --000000 -----110		PSDR10 [R/W] H,W 00000000 00000000		
001B1C _H	PTPC10 [R/W] H,W 00000000 00000000		—	—	
001B20 _H	PCN11 [R/W] B,H,W 00000000 000000-0		PCSR11 [W] H,W XXXXXXXX XXXXXXXX		PPG11
001B24 _H	PDUT11 [W] H,W XXXXXXXX XXXXXXXX		PTMR11 [R] H,W 11111111 11111111		
001B28 _H	PCN211 [R/W] B,H,W --000000 -----110		PSDR11 [R/W] H,W 00000000 00000000		
001B2C _H	PTPC11 [R/W] H,W 00000000 00000000		—	—	
001B30 _H	PCN12 [R/W] B,H,W 00000000 000000-0		PCSR12 [W] H,W XXXXXXXX XXXXXXXX		PPG12
001B34 _H	PDUT12 [W] H,W XXXXXXXX XXXXXXXX		PTMR12 [R] H,W 11111111 11111111		
001B38 _H	PCN212 [R/W] B,H,W --000000 -----110		PSDR12 [R/W] H,W 00000000 00000000		
001B3C _H	PTPC12 [R/W] H,W 00000000 00000000		—	—	
001B40 _H	PCN13 [R/W] B,H,W 00000000 000000-0		PCSR13 [W] H,W XXXXXXXX XXXXXXXX		PPG13
001B44 _H	PDUT13 [W] H,W XXXXXXXX XXXXXXXX		PTMR13 [R] H,W 11111111 11111111		
001B48 _H	PCN213 [R/W] B,H,W --000000 -----110		PSDR13 [R/W] H,W 00000000 00000000		
001B4C _H	PTPC13 [R/W] H,W 00000000 00000000		—	—	
001B50 _H	PCN14 [R/W] B,H,W 00000000 000000-0		PCSR14 [W] H,W XXXXXXXX XXXXXXXX		PPG14
001B54 _H	PDUT14 [W] H,W XXXXXXXX XXXXXXXX		PTMR14 [R] H,W 11111111 11111111		
001B58 _H	PCN214 [R/W] B,H,W --000000 -----110		PSDR14 [R/W] H,W 00000000 00000000		
001B5C _H	PTPC14 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001B60 _H	PCN15 [R/W] B,H,W 00000000 000000-0		PCSR15 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG15
001B64 _H	PDUT15 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR15 [R] H,W 11111111 11111111		
001B68 _H	PCN215 [R/W] B,H,W --000000 -----110		PSDR15 [R/W] H,W 00000000 00000000		
001B6C _H	PTPC15 [R/W] H,W 00000000 00000000		—	—	
001B70 _H	PCN16 [R/W] B,H,W 00000000 000000-0		PCSR16 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG16
001B74 _H	PDUT16 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR16 [R] H,W 11111111 11111111		
001B78 _H	PCN216 [R/W] B,H,W --000000 -----110		PSDR16 [R/W] H,W 00000000 00000000		
001B7C _H	PTPC16 [R/W] H,W 00000000 00000000		—	—	
001B80 _H	PCN17 [R/W] B,H,W 00000000 000000-0		PCSR17 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG17
001B84 _H	PDUT17 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR17 [R] H,W 11111111 11111111		
001B88 _H	PCN217 [R/W] B,H,W --000000 -----110		PSDR17 [R/W] H,W 00000000 00000000		
001B8C _H	PTPC17 [R/W] H,W 00000000 00000000		—	—	
001B90 _H	PCN18 [R/W] B,H,W 00000000 000000-0		PCSR18 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG18
001B94 _H	PDUT18 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR18 [R] H,W 11111111 11111111		
001B98 _H	PCN218 [R/W] B,H,W --000000 -----110		PSDR18 [R/W] H,W 00000000 00000000		
001B9C _H	PTPC18 [R/W] H,W 00000000 00000000		—	—	
001BA0 _H	PCN19 [R/W] B,H,W 00000000 000000-0		PCSR19 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG19
001BA4 _H	PDUT19 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR19 [R] H,W 11111111 11111111		
001BA8 _H	PCN219 [R/W] B,H,W --000000 -----110		PSDR19 [R/W] H,W 00000000 00000000		
001BAC _H	PTPC19 [R/W] H,W 00000000 00000000		—	—	
001BB0 _H	PCN20 [R/W] B,H,W 00000000 000000-0		PCSR20 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG20
001BB4 _H	PDUT20 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR20 [R] H,W 11111111 11111111		
001BB8 _H	PCN220 [R/W] B,H,W --000000 -----110		PSDR20 [R/W] H,W 00000000 00000000		
001BBC _H	PTPC20 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001BC0 _H	PCN21 [R/W] B,H,W 00000000 000000-0		PCSR21 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG21
001BC4 _H	PDUT21 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR21 [R] H,W 11111111 11111111		
001BC8 _H	PCN221 [R/W] B,H,W --000000 -----110		PSDR21 [R/W] H,W 00000000 00000000		
001BCC _H	PTPC21 [R/W] H,W 00000000 00000000		—	—	
001BD0 _H	PCN22 [R/W] B,H,W 00000000 000000-0		PCSR22 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG22
001BD4 _H	PDUT22 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR22 [R] H,W 11111111 11111111		
001BD8 _H	PCN222 [R/W] B,H,W --000000 -----110		PSDR22 [R/W] H,W 00000000 00000000		
001BDC _H	PTPC22 [R/W] H,W 00000000 00000000		—	—	
001BE0 _H	PCN23 [R/W] B,H,W 00000000 000000-0		PCSR23 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG23
001BE4 _H	PDUT23 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR23 [R] H,W 11111111 11111111		
001BE8 _H	PCN223 [R/W] B,H,W --000000 -----110		PSDR23 [R/W] H,W 00000000 00000000		
001BEC _H	PTPC23 [R/W] H,W 00000000 00000000		—	—	
001BF0 _H	PCN24 [R/W] B,H,W 00000000 000000-0		PCSR24 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG24
001BF4 _H	PDUT24 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR24 [R] H,W 11111111 11111111		
001BF8 _H	PCN224 [R/W] B,H,W --000000 -----110		PSDR24 [R/W] H,W 00000000 00000000		
001BFC _H	PTPC24 [R/W] H,W 00000000 00000000		—	—	
001C00 _H	PCN25 [R/W] B,H,W 00000000 000000-0		PCSR25 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG25
001C04 _H	PDUT25 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR25 [R] H,W 11111111 11111111		
001C08 _H	PCN225 [R/W] B,H,W --000000 -----110		PSDR25 [R/W] H,W 00000000 00000000		
001C0C _H	PTPC25 [R/W] H,W 00000000 00000000		—	—	
001C10 _H	PCN26 [R/W] B,H,W 00000000 000000-0		PCSR26 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG26
001C14 _H	PDUT26 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR26 [R] H,W 11111111 11111111		
001C18 _H	PCN226 [R/W] B,H,W --000000 -----110		PSDR26 [R/W] H,W 00000000 00000000		
001C1C _H	PTPC26 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001C20 _H	PCN27 [R/W] B,H,W 00000000 000000-0		PCSR27 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG27
001C24 _H	PDUT27 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR27 [R] H,W 11111111 11111111		
001C28 _H	PCN227 [R/W] B,H,W --000000 -----110		PSDR27 [R/W] H,W 00000000 00000000		
001C2C _H	PTPC27 [R/W] H,W 00000000 00000000		—	—	
001C30 _H	PCN28 [R/W] B,H,W 00000000 000000-0		PCSR28 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG28
001C34 _H	PDUT28 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR28 [R] H,W 11111111 11111111		
001C38 _H	PCN228 [R/W] B,H,W --000000 -----110		PSDR28 [R/W] H,W 00000000 00000000		
001C3C _H	PTPC28 [R/W] H,W 00000000 00000000		—	—	
001C40 _H	PCN29 [R/W] B,H,W 00000000 000000-0		PCSR29 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG29
001C44 _H	PDUT29 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR29 [R] H,W 11111111 11111111		
001C48 _H	PCN229 [R/W] B,H,W --000000 -----110		PSDR29 [R/W] H,W 00000000 00000000		
001C4C _H	PTPC29 [R/W] H,W 00000000 00000000		—	—	
001C50 _H	PCN30 [R/W] B,H,W 00000000 000000-0		PCSR30 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG30
001C54 _H	PDUT30 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR30 [R] H,W 11111111 11111111		
001C58 _H	PCN230 [R/W] B,H,W --000000 -----110		PSDR30 [R/W] H,W 00000000 00000000		
001C5C _H	PTPC30 [R/W] H,W 00000000 00000000		—	—	
001C60 _H	PCN31 [R/W] B,H,W 00000000 000000-0		PCSR31 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG31
001C64 _H	PDUT31 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR31 [R] H,W 11111111 11111111		
001C68 _H	PCN231 [R/W] B,H,W --000000 -----110		PSDR31 [R/W] H,W 00000000 00000000		
001C6C _H	PTPC31 [R/W] H,W 00000000 00000000		—	—	
001C70 _H	PCN32 [R/W] B,H,W 00000000 000000-0		PCSR32 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG32
001C74 _H	PDUT32 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR32 [R] H,W 11111111 11111111		
001C78 _H	PCN232 [R/W] B,H,W --000000 -----110		PSDR32 [R/W] H,W 00000000 00000000		
001C7C _H	PTPC32 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001C80 _H	PCN33 [R/W] B,H,W 00000000 000000-0		PCSR33 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG33
001C84 _H	PDUT33 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR33 [R] H,W 11111111 11111111		
001C88 _H	PCN233 [R/W] B,H,W --000000 -----110		PSDR33 [R/W] H,W 00000000 00000000		
001C8C _H	PTPC33 [R/W] H,W 00000000 00000000		—	—	
001C90 _H	PCN34 [R/W] B,H,W 00000000 000000-0		PCSR34 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG34
001C94 _H	PDUT34 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR34 [R] H,W 11111111 11111111		
001C98 _H	PCN234 [R/W] B,H,W --000000 -----110		PSDR34 [R/W] H,W 00000000 00000000		
001C9C _H	PTPC34 [R/W] H,W 00000000 00000000		—	—	
001CA0 _H	PCN35 [R/W] B,H,W 00000000 000000-0		PCSR35 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG35
001CA4 _H	PDUT35 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR35 [R] H,W 11111111 11111111		
001CA8 _H	PCN235 [R/W] B,H,W --000000 -----110		PSDR35 [R/W] H,W 00000000 00000000		
001CAC _H	PTPC35 [R/W] H,W 00000000 00000000		—	—	
001CB0 _H	PCN36 [R/W] B,H,W 00000000 000000-0		PCSR36 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG36
001CB4 _H	PDUT36 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR36 [R] H,W 11111111 11111111		
001CB8 _H	PCN236 [R/W] B,H,W --000000 -----110		PSDR36 [R/W] H,W 00000000 00000000		
001CBC _H	PTPC36 [R/W] H,W 00000000 00000000		—	—	
001CC0 _H	PCN37 [R/W] B,H,W 00000000 000000-0		PCSR37 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG37
001CC4 _H	PDUT37 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR37 [R] H,W 11111111 11111111		
001CC8 _H	PCN237 [R/W] B,H,W --000000 -----110		PSDR37 [R/W] H,W 00000000 00000000		
001CCC _H	PTPC37 [R/W] H,W 00000000 00000000		—	—	
001CD0 _H	PCN38 [R/W] B,H,W 00000000 000000-0		PCSR38 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG38
001CD4 _H	PDUT38 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR38 [R] H,W 11111111 11111111		
001CD8 _H	PCN238 [R/W] B,H,W --000000 -----110		PSDR38 [R/W] H,W 00000000 00000000		
001CDC _H	PTPC38 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001CE0 _H	PCN39 [R/W] B,H,W 00000000 000000-0		PCSR39 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG39
001CE4 _H	PDUT39 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR39 [R] H,W 11111111 11111111		
001CE8 _H	PCN239 [R/W] B,H,W --000000 -----110		PSDR39 [R/W] H,W 00000000 00000000		
001CEC _H	PTPC39 [R/W] H,W 00000000 00000000		—	—	
001CF0 _H	PCN40 [R/W] B,H,W 00000000 000000-0		PCSR40 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG40
001CF4 _H	PDUT40 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR40 [R] H,W 11111111 11111111		
001CF8 _H	PCN240 [R/W] B,H,W --000000 -----110		PSDR40 [R/W] H,W 00000000 00000000		
001CFC _H	PTPC40 [R/W] H,W 00000000 00000000		—	—	
001D00 _H	PCN41 [R/W] B,H,W 00000000 000000-0		PCSR41 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG41
001D04 _H	PDUT41 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR41 [R] H,W 11111111 11111111		
001D08 _H	PCN241 [R/W] B,H,W --000000 -----110		PSDR41 [R/W] H,W 00000000 00000000		
001D0C _H	PTPC41 [R/W] H,W 00000000 00000000		—	—	
001D10 _H	PCN42 [R/W] B,H,W 00000000 000000-0		PCSR42 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG42
001D14 _H	PDUT42 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR42 [R] H,W 11111111 11111111		
001D18 _H	PCN242 [R/W] B,H,W --000000 -----110		PSDR42 [R/W] H,W 00000000 00000000		
001D1C _H	PTPC42 [R/W] H,W 00000000 00000000		—	—	
001D20 _H	PCN43 [R/W] B,H,W 00000000 000000-0		PCSR43 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG43
001D24 _H	PDUT43 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR43 [R] H,W 11111111 11111111		
001D28 _H	PCN243 [R/W] B,H,W --000000 -----110		PSDR43 [R/W] H,W 00000000 00000000		
001D2C _H	PTPC43 [R/W] H,W 00000000 00000000		—	—	
001D30 _H	PCN44 [R/W] B,H,W 00000000 000000-0		PCSR44 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG44
001D34 _H	PDUT44 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR44 [R] H,W 11111111 11111111		
001D38 _H	PCN244 [R/W] B,H,W --000000 -----110		PSDR44 [R/W] H,W 00000000 00000000		
001D3C _H	PTPC44 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001D40 _H	PCN45 [R/W] B,H,W 00000000 000000-0		PCSR45 [W] H,W XXXXXXXX XXXXXXXX		PPG45
001D44 _H	PDUT45 [W] H,W XXXXXXXX XXXXXXXX		PTMR45 [R] H,W 11111111 11111111		
001D48 _H	PCN245 [R/W] B,H,W --000000 -----110		PSDR45 [R/W] H,W 00000000 00000000		
001D4C _H	PTPC45 [R/W] H,W 00000000 00000000		—	—	
001D50 _H	PCN46 [R/W] B,H,W 00000000 000000-0		PCSR46 [W] H,W XXXXXXXX XXXXXXXX		PPG46
001D54 _H	PDUT46 [W] H,W XXXXXXXX XXXXXXXX		PTMR46 [R] H,W 11111111 11111111		
001D58 _H	PCN246 [R/W] B,H,W --000000 -----110		PSDR46 [R/W] H,W 00000000 00000000		
001D5C _H	PTPC46 [R/W] H,W 00000000 00000000		—	—	
001D60 _H	PCN47 [R/W] B,H,W 00000000 000000-0		PCSR47 [W] H,W XXXXXXXX XXXXXXXX		PPG47
001D64 _H	PDUT47 [W] H,W XXXXXXXX XXXXXXXX		PTMR47 [R] H,W 11111111 11111111		
001D68 _H	PCN247 [R/W] B,H,W --000000 -----110		PSDR47 [R/W] H,W 00000000 00000000		
001D6C _H	PTPC47 [R/W] H,W 00000000 00000000		—	—	
001D70 _H	PCN48 [R/W] B,H,W 00000000 000000-0		PCSR48 [W] H,W XXXXXXXX XXXXXXXX		PPG48
001D74 _H	PDUT48 [W] H,W XXXXXXXX XXXXXXXX		PTMR48 [R] H,W 11111111 11111111		
001D78 _H	PCN248 [R/W] B,H,W --000000 -----110		PSDR48 [R/W] H,W 00000000 00000000		
001D7C _H	PTPC48 [R/W] H,W 00000000 00000000		—	—	
001D80 _H	PCN49 [R/W] B,H,W 00000000 000000-0		PCSR49 [W] H,W XXXXXXXX XXXXXXXX		PPG49
001D84 _H	PDUT49 [W] H,W XXXXXXXX XXXXXXXX		PTMR49 [R] H,W 11111111 11111111		
001D88 _H	PCN249 [R/W] B,H,W --000000 -----110		PSDR49 [R/W] H,W 00000000 00000000		
001D8C _H	PTPC49 [R/W] H,W 00000000 00000000		—	—	
001D90 _H	PCN50 [R/W] B,H,W 00000000 000000-0		PCSR50 [W] H,W XXXXXXXX XXXXXXXX		PPG50
001D94 _H	PDUT50 [W] H,W XXXXXXXX XXXXXXXX		PTMR50 [R] H,W 11111111 11111111		
001D98 _H	PCN250 [R/W] B,H,W --000000 -----110		PSDR50 [R/W] H,W 00000000 00000000		
001D9C _H	PTPC50 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001DA0 _H	PCN51 [R/W] B,H,W 00000000 000000-0		PCSR51 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG51
001DA4 _H	PDUT51 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR51 [R] H,W 11111111 11111111		
001DA8 _H	PCN251 [R/W] B,H,W --000000 -----110		PSDR51 [R/W] H,W 00000000 00000000		
001DAC _H	PTPC51 [R/W] H,W 00000000 00000000		—	—	
001DB0 _H	PCN52 [R/W] B,H,W 00000000 000000-0		PCSR52 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG52
001DB4 _H	PDUT52 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR52 [R] H,W 11111111 11111111		
001DB8 _H	PCN252 [R/W] B,H,W --000000 -----110		PSDR52 [R/W] H,W 00000000 00000000		
001DBC _H	PTPC52 [R/W] H,W 00000000 00000000		—	—	
001DC0 _H	PCN53 [R/W] B,H,W 00000000 000000-0		PCSR53 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG53
001DC4 _H	PDUT53 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR53 [R] H,W 11111111 11111111		
001DC8 _H	PCN253 [R/W] B,H,W --000000 -----110		PSDR53 [R/W] H,W 00000000 00000000		
001DCC _H	PTPC53 [R/W] H,W 00000000 00000000		—	—	
001DD0 _H	PCN54 [R/W] B,H,W 00000000 000000-0		PCSR54 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG54
001DD4 _H	PDUT54 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR54 [R] H,W 11111111 11111111		
001DD8 _H	PCN254 [R/W] B,H,W --000000 -----110		PSDR54 [R/W] H,W 00000000 00000000		
001DDC _H	PTPC54 [R/W] H,W 00000000 00000000		—	—	
001DE0 _H	PCN55 [R/W] B,H,W 00000000 000000-0		PCSR55 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG55
001DE4 _H	PDUT55 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR55 [R] H,W 11111111 11111111		
001DE8 _H	PCN255 [R/W] B,H,W --000000 -----110		PSDR55 [R/W] H,W 00000000 00000000		
001DEC _H	PTPC55 [R/W] H,W 00000000 00000000		—	—	
001DF0 _H	PCN56 [R/W] B,H,W 00000000 000000-0		PCSR56 [W] H,W XXXXXXXXXX XXXXXXXXXX		PPG56
001DF4 _H	PDUT56 [W] H,W XXXXXXXXXX XXXXXXXXXX		PTMR56 [R] H,W 11111111 11111111		
001DF8 _H	PCN256 [R/W] B,H,W --000000 -----110		PSDR56 [R/W] H,W 00000000 00000000		
001DFC _H	PTPC56 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001E00 _H	PCN57 [R/W] B,H,W 00000000 000000-0		PCSR57 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG57
001E04 _H	PDUT57 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR57 [R] H,W 11111111 11111111		
001E08 _H	PCN257 [R/W] B,H,W --000000 -----110		PSDR57 [R/W] H,W 00000000 00000000		
001E0C _H	PTPC57 [R/W] H,W 00000000 00000000		—	—	
001E10 _H	PCN58 [R/W] B,H,W 00000000 000000-0		PCSR58 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG58
001E14 _H	PDUT58 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR58 [R] H,W 11111111 11111111		
001E18 _H	PCN258 [R/W] B,H,W --000000 -----110		PSDR58 [R/W] H,W 00000000 00000000		
001E1C _H	PTPC58 [R/W] H,W 00000000 00000000		—	—	
001E20 _H	PCN59 [R/W] B,H,W 00000000 000000-0		PCSR59 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG59
001E24 _H	PDUT59 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR59 [R] H,W 11111111 11111111		
001E28 _H	PCN259 [R/W] B,H,W --000000 -----110		PSDR59 [R/W] H,W 00000000 00000000		
001E2C _H	PTPC59 [R/W] H,W 00000000 00000000		—	—	
001E30 _H	PCN60 [R/W] B,H,W 00000000 000000-0		PCSR60 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG60
001E34 _H	PDUT60 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR60 [R] H,W 11111111 11111111		
001E38 _H	PCN260 [R/W] B,H,W --000000 -----110		PSDR60 [R/W] H,W 00000000 00000000		
001E3C _H	PTPC60 [R/W] H,W 00000000 00000000		—	—	
001E40 _H	PCN61 [R/W] B,H,W 00000000 000000-0		PCSR61 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG61
001E44 _H	PDUT61 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR61 [R] H,W 11111111 11111111		
001E48 _H	PCN261 [R/W] B,H,W --000000 -----110		PSDR61 [R/W] H,W 00000000 00000000		
001E4C _H	PTPC61 [R/W] H,W 00000000 00000000		—	—	
001E50 _H	PCN62 [R/W] B,H,W 00000000 000000-0		PCSR62 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG62
001E54 _H	PDUT62 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR62 [R] H,W 11111111 11111111		
001E58 _H	PCN262 [R/W] B,H,W --000000 -----110		PSDR62 [R/W] H,W 00000000 00000000		
001E5C _H	PTPC62 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001E60 _H	PCN63 [R/W] B,H,W 00000000 000000-0		PCSR63 [W] H,W XXXXXXXX XXXXXXXX		PPG63
001E64 _H	PDUT63 [W] H,W XXXXXXXX XXXXXXXX		PTMR63 [R] H,W 11111111 11111111		
001E68 _H	PCN263 [R/W] B,H,W --000000 ----110		PSDR63 [R/W] H,W 00000000 00000000		
001E6C _H	PTPC63 [R/W] H,W 00000000 00000000		—	—	
001E70 _H	PCN64 [R/W] B,H,W 00000000 000000-0		PCSR64 [W] H,W XXXXXXXX XXXXXXXX		PPG64
001E74 _H	PDUT64 [W] H,W XXXXXXXX XXXXXXXX		PTMR64 [R] H,W 11111111 11111111		
001E78 _H	PCN264 [R/W] B,H,W --000000 ----110		PSDR64 [R/W] H,W 00000000 00000000		
001E7C _H	PTPC64 [R/W] H,W 00000000 00000000		—	—	
001E80 _H	PCN65 [R/W] B,H,W 00000000 000000-0		PCSR65 [W] H,W XXXXXXXX XXXXXXXX		PPG65
001E84 _H	PDUT65 [W] H,W XXXXXXXX XXXXXXXX		PTMR65 [R] H,W 11111111 11111111		
001E88 _H	PCN265 [R/W] B,H,W --000000 ----110		PSDR65 [R/W] H,W 00000000 00000000		
001E8C _H	PTPC65 [R/W] H,W 00000000 00000000		—	—	
001E90 _H	PCN66 [R/W] B,H,W 00000000 000000-0		PCSR66 [W] H,W XXXXXXXX XXXXXXXX		PPG66
001E94 _H	PDUT66 [W] H,W XXXXXXXX XXXXXXXX		PTMR66 [R] H,W 11111111 11111111		
001E98 _H	PCN266 [R/W] B,H,W --000000 ----110		PSDR66 [R/W] H,W 00000000 00000000		
001E9C _H	PTPC66 [R/W] H,W 00000000 00000000		—	—	
001EA0 _H	PCN67 [R/W] B,H,W 00000000 000000-0		PCSR67 [W] H,W XXXXXXXX XXXXXXXX		PPG67
001EA4 _H	PDUT67 [W] H,W XXXXXXXX XXXXXXXX		PTMR67 [R] H,W 11111111 11111111		
001EA8 _H	PCN267 [R/W] B,H,W --000000 ----110		PSDR67 [R/W] H,W 00000000 00000000		
001EAC _H	PTPC67 [R/W] H,W 00000000 00000000		—	—	
001EB0 _H	PCN68 [R/W] B,H,W 00000000 000000-0		PCSR68 [W] H,W XXXXXXXX XXXXXXXX		PPG68
001EB4 _H	PDUT68 [W] H,W XXXXXXXX XXXXXXXX		PTMR68 [R] H,W 11111111 11111111		
001EB8 _H	PCN268 [R/W] B,H,W --000000 ----110		PSDR68 [R/W] H,W 00000000 00000000		
001EBC _H	PTPC68 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001EC0 _H	PCN69 [R/W] B,H,W 00000000 000000-0		PCSR69 [W] H,W XXXXXXXX XXXXXXXX		PPG69
001EC4 _H	PDUT69 [W] H,W XXXXXXXX XXXXXXXX		PTMR69 [R] H,W 11111111 11111111		
001EC8 _H	PCN269 [R/W] B,H,W --000000 ----110		PSDR69 [R/W] H,W 00000000 00000000		
001ECC _H	PTPC69 [R/W] H,W 00000000 00000000		—	—	
001ED0 _H	PCN70 [R/W] B,H,W 00000000 000000-0		PCSR70 [W] H,W XXXXXXXX XXXXXXXX		PPG70
001ED4 _H	PDUT70 [W] H,W XXXXXXXX XXXXXXXX		PTMR70 [R] H,W 11111111 11111111		
001ED8 _H	PCN270 [R/W] B,H,W --000000 ----110		PSDR70 [R/W] H,W 00000000 00000000		
001EDC _H	PTPC70 [R/W] H,W 00000000 00000000		—	—	
001EE0 _H	PCN71 [R/W] B,H,W 00000000 000000-0		PCSR71 [W] H,W XXXXXXXX XXXXXXXX		PPG71
001EE4 _H	PDUT71 [W] H,W XXXXXXXX XXXXXXXX		PTMR71 [R] H,W 11111111 11111111		
001EE8 _H	PCN271 [R/W] B,H,W --000000 ----110		PSDR71 [R/W] H,W 00000000 00000000		
001EEC _H	PTPC71 [R/W] H,W 00000000 00000000		—	—	
001EF0 _H	PCN72 [R/W] B,H,W 00000000 000000-0		PCSR72 [W] H,W XXXXXXXX XXXXXXXX		PPG72
001EF4 _H	PDUT72 [W] H,W XXXXXXXX XXXXXXXX		PTMR72 [R] H,W 11111111 11111111		
001EF8 _H	PCN272 [R/W] B,H,W --000000 ----110		PSDR72 [R/W] H,W 00000000 00000000		
001EFC _H	PTPC72 [R/W] H,W 00000000 00000000		—	—	
001F00 _H	PCN73 [R/W] B,H,W 00000000 000000-0		PCSR73 [W] H,W XXXXXXXX XXXXXXXX		PPG73
001F04 _H	PDUT73 [W] H,W XXXXXXXX XXXXXXXX		PTMR73 [R] H,W 11111111 11111111		
001F08 _H	PCN273 [R/W] B,H,W --000000 ----110		PSDR73 [R/W] H,W 00000000 00000000		
001F0C _H	PTPC73 [R/W] H,W 00000000 00000000		—	—	
001F10 _H	PCN74 [R/W] B,H,W 00000000 000000-0		PCSR74 [W] H,W XXXXXXXX XXXXXXXX		PPG74
001F14 _H	PDUT74 [W] H,W XXXXXXXX XXXXXXXX		PTMR74 [R] H,W 11111111 11111111		
001F18 _H	PCN274 [R/W] B,H,W --000000 ----110		PSDR74 [R/W] H,W 00000000 00000000		
001F1C _H	PTPC74 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001F20 _H	PCN75 [R/W] B,H,W 00000000 000000-0		PCSR75 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG75
001F24 _H	PDUT75 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR75 [R] H,W 11111111 11111111		
001F28 _H	PCN275 [R/W] B,H,W --000000 -----110		PSDR75 [R/W] H,W 00000000 00000000		
001F2C _H	PTPC75 [R/W] H,W 00000000 00000000		—	—	
001F30 _H	PCN76 [R/W] B,H,W 00000000 000000-0		PCSR76 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG76
001F34 _H	PDUT76 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR76 [R] H,W 11111111 11111111		
001F38 _H	PCN276 [R/W] B,H,W --000000 -----110		PSDR76 [R/W] H,W 00000000 00000000		
001F3C _H	PTPC76 [R/W] H,W 00000000 00000000		—	—	
001F40 _H	PCN77 [R/W] B,H,W 00000000 000000-0		PCSR77 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG77
001F44 _H	PDUT77 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR77 [R] H,W 11111111 11111111		
001F48 _H	PCN277 [R/W] B,H,W --000000 -----110		PSDR77 [R/W] H,W 00000000 00000000		
001F4C _H	PTPC77 [R/W] H,W 00000000 00000000		—	—	
001F50 _H	PCN78 [R/W] B,H,W 00000000 000000-0		PCSR78 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG78
001F54 _H	PDUT78 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR78 [R] H,W 11111111 11111111		
001F58 _H	PCN278 [R/W] B,H,W --000000 -----110		PSDR78 [R/W] H,W 00000000 00000000		
001F5C _H	PTPC78 [R/W] H,W 00000000 00000000		—	—	
001F60 _H	PCN79 [R/W] B,H,W 00000000 000000-0		PCSR79 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG79
001F64 _H	PDUT79 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR79 [R] H,W 11111111 11111111		
001F68 _H	PCN279 [R/W] B,H,W --000000 -----110		PSDR79 [R/W] H,W 00000000 00000000		
001F6C _H	PTPC79 [R/W] H,W 00000000 00000000		—	—	
001F70 _H	PCN80 [R/W] B,H,W 00000000 000000-0		PCSR80 [W] H,W XXXXXXXXXX XXXXXXXXX		PPG80
001F74 _H	PDUT80 [W] H,W XXXXXXXXXX XXXXXXXXX		PTMR80 [R] H,W 11111111 11111111		
001F78 _H	PCN280 [R/W] B,H,W --000000 -----110		PSDR80 [R/W] H,W 00000000 00000000		
001F7C _H	PTPC80 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001F80 _H	PCN81 [R/W] B,H,W 00000000 000000-0		PCSR81 [W] H,W XXXXXXXX XXXXXXXX		PPG81
001F84 _H	PDUT81 [W] H,W XXXXXXXX XXXXXXXX		PTMR81 [R] H,W 11111111 11111111		
001F88 _H	PCN281 [R/W] B,H,W --000000 ----110		PSDR81 [R/W] H,W 00000000 00000000		
001F8C _H	PTPC81 [R/W] H,W 00000000 00000000		—	—	
001F90 _H	PCN82 [R/W] B,H,W 00000000 000000-0		PCSR82 [W] H,W XXXXXXXX XXXXXXXX		PPG82
001F94 _H	PDUT82 [W] H,W XXXXXXXX XXXXXXXX		PTMR82 [R] H,W 11111111 11111111		
001F98 _H	PCN282 [R/W] B,H,W --000000 ----110		PSDR82 [R/W] H,W 00000000 00000000		
001F9C _H	PTPC82 [R/W] H,W 00000000 00000000		—	—	
001FA0 _H	PCN83 [R/W] B,H,W 00000000 000000-0		PCSR83 [W] H,W XXXXXXXX XXXXXXXX		PPG83
001FA4 _H	PDUT83 [W] H,W XXXXXXXX XXXXXXXX		PTMR83 [R] H,W 11111111 11111111		
001FA8 _H	PCN283 [R/W] B,H,W --000000 ----110		PSDR83 [R/W] H,W 00000000 00000000		
001FAC _H	PTPC83 [R/W] H,W 00000000 00000000		—	—	
001FB0 _H	PCN84 [R/W] B,H,W 00000000 000000-0		PCSR84 [W] H,W XXXXXXXX XXXXXXXX		PPG84
001FB4 _H	PDUT84 [W] H,W XXXXXXXX XXXXXXXX		PTMR84 [R] H,W 11111111 11111111		
001FB8 _H	PCN284 [R/W] B,H,W --000000 ----110		PSDR84 [R/W] H,W 00000000 00000000		
001FBC _H	PTPC84 [R/W] H,W 00000000 00000000		—	—	
001FC0 _H	PCN85 [R/W] B,H,W 00000000 000000-0		PCSR85 [W] H,W XXXXXXXX XXXXXXXX		PPG85
001FC4 _H	PDUT85 [W] H,W XXXXXXXX XXXXXXXX		PTMR85 [R] H,W 11111111 11111111		
001FC8 _H	PCN285 [R/W] B,H,W --000000 ----110		PSDR85 [R/W] H,W 00000000 00000000		
001FCC _H	PTPC85 [R/W] H,W 00000000 00000000		—	—	
001FD0 _H	PCN86 [R/W] B,H,W 00000000 000000-0		PCSR86 [W] H,W XXXXXXXX XXXXXXXX		PPG86
001FD4 _H	PDUT86 [W] H,W XXXXXXXX XXXXXXXX		PTMR86 [R] H,W 11111111 11111111		
001FD8 _H	PCN286 [R/W] B,H,W --000000 ----110		PSDR86 [R/W] H,W 00000000 00000000		
001FDC _H	PTPC86 [R/W] H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001FE0 _H	PCN87 [R/W] B,H,W 00000000 000000-0		PCSR87 [W] H,W XXXXXXXX XXXXXXXX		PPG87
001FE4 _H	PDUT87 [W] H,W XXXXXXXX XXXXXXXX		PTMR87 [R] H,W 11111111 11111111		
001FE8 _H	PCN287 [R/W] B,H,W --000000 -----110		PSDR87 [R/W] H,W 00000000 00000000		
001FEC _H	PTPC87 [R/W] H,W 00000000 00000000		—	—	
001FF0 _H to 001FFC _H	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002000 _H	CTRLR0 [R/W] B,H,W ----- 000-0001		STATR0 [R/W] B,H,W ----- 00000000		CAN0 (128msb)
002004 _H	ERRCNT0 [R] B,H,W 00000000 00000000		BTR0 [R/W] B,H,W -0100011 00000001		
002008 _H	INTR0 [R] B,H,W 00000000 00000000		TESTR0 [R/W] B,H,W ----- X00000--		
00200C _H	BRPER0 [R/W] B,H,W ----- ----0000		—	—	
002010 _H	IF1CREQ0 [R/W] B,H,W 0----- 00000001		IF1CMSK0 [R/W] B,H,W ----- 00000000		
002014 _H	IF1MSK20 [R/W] B,H,W 11-11111 11111111		IF1MSK10 [R/W] B,H,W 11111111 11111111		
002018 _H	IF1ARB20 [R/W] B,H,W 00000000 00000000		IF1ARB10 [R/W] B,H,W 00000000 00000000		
00201C _H	IF1MCTR0 [R/W] B,H,W 00000000 0---0000		—	—	
002020 _H	IF1DTA10 [R/W] B,H,W 00000000 00000000		IF1DTA20 [R/W] B,H,W 00000000 00000000		
002024 _H	IF1DTB10 [R/W] B,H,W 00000000 00000000		IF1DTB20 [R/W] B,H,W 00000000 00000000		
002028 _H	—	—	—	—	
00202C _H	—	—	—	—	
002030 _H , 002034 _H	Reserved (IF1 data mirror)				
002038 _H	—	—	—	—	
00203C _H	—	—	—	—	
002040 _H	IF2CREQ0 [R/W] B,H,W 0----- 00000001		IF2CMSK0 [R/W] B,H,W ----- 00000000		
002044 _H	IF2MSK20 [R/W] B,H,W 11-11111 11111111		IF2MSK10 [R/W] B,H,W 11111111 11111111		
002048 _H	IF2ARB20 [R/W] B,H,W 00000000 00000000		IF2ARB10 [R/W] B,H,W 00000000 00000000		
00204C _H	IF2MCTR0 [R/W] B,H,W 00000000 0---0000		—	—	
002050 _H	IF2DTA10 [R/W] B,H,W 00000000 00000000		IF2DTA20 [R/W] B,H,W 00000000 00000000		
002054 _H	IF2DTB10 [R/W] B,H,W 00000000 00000000		IF2DTB20 [R/W] B,H,W 00000000 00000000		
002058 _H	—	—	—	—	
00205C _H	—	—	—	—	
002060 _H , 002064 _H	Reserved (IF2 data mirror)				
002068 _H to 00207C _H	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002080 _H	TREQR20 [R] B,H,W 00000000 00000000		TREQR10 [R] B,H,W 00000000 00000000		CAN0 (128msb)
002084 _H	TREQR40 [R] B,H,W 00000000 00000000		TREQR30 [R] B,H,W 00000000 00000000		
002088 _H	TREQR60 [R] B,H,W 00000000 00000000		TREQR50 [R] B,H,W 00000000 00000000		
00208C _H	TREQR80 [R] B,H,W 00000000 00000000		TREQR70 [R] B,H,W 00000000 00000000		
002090 _H	NEWDT20 [R] B,H,W 00000000 00000000		NEWDT10 [R] B,H,W 00000000 00000000		
002094 _H	NEWDT40 [R] B,H,W 00000000 00000000		NEWDT30 [R] B,H,W 00000000 00000000		
002098 _H	NEWDT60 [R] B,H,W 00000000 00000000		NEWDT50 [R] B,H,W 00000000 00000000		
00209C _H	NEWDT80 [R] B,H,W 00000000 00000000		NEWDT70 [R] B,H,W 00000000 00000000		
0020A0 _H	INTPND20 [R] B,H,W 00000000 00000000		INTPND10 [R] B,H,W 00000000 00000000		
0020A4 _H	INTPND40 [R] B,H,W 00000000 00000000		INTPND30 [R] B,H,W 00000000 00000000		
0020A8 _H	INTPND60 [R] B,H,W 00000000 00000000		INTPND50 [R] B,H,W 00000000 00000000		
0020AC _H	INTPND80 [R] B,H,W 00000000 00000000		INTPND70 [R] B,H,W 00000000 00000000		
0020B0 _H	MSGVAL20 [R] B,H,W 00000000 00000000		MSGVAL10 [R] B,H,W 00000000 00000000		
0020B4 _H	MSGVAL40 [R] B,H,W 00000000 00000000		MSGVAL30 [R] B,H,W 00000000 00000000		
0020B8 _H	MSGVAL60 [R] B,H,W 00000000 00000000		MSGVAL50 [R] B,H,W 00000000 00000000		
0020BC _H	MSGVAL80 [R] B,H,W 00000000 00000000		MSGVAL70 [R] B,H,W 00000000 00000000		
0020C0 _H to 0020FC _H	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002100 _H	CTRLR1 [R/W] B,H,W ----- 000-0001		STATR1 [R/W] B,H,W ----- 00000000		CAN1 (128msb)
002104 _H	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1 [R/W] B,H,W -0100011 00000001		
002108 _H	INTR1 [R] B,H,W 00000000 00000000		TESTR1 [R/W] B,H,W ----- X00000--		
00210C _H	BRPER1 [R/W] B,H,W ----- ----0000		—	—	
002110 _H	IF1CREQ1 [R/W] B,H,W 0----- 00000001		IF1CMSK1 [R/W] B,H,W ----- 00000000		
002114 _H	IF1MSK21 [R/W] B,H,W 11-11111 11111111		IF1MSK11 [R/W] B,H,W 11111111 11111111		
002118 _H	IF1ARB21 [R/W] B,H,W 00000000 00000000		IF1ARB11 [R/W] B,H,W 00000000 00000000		
00211C _H	IF1MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	
002120 _H	IF1DTA11 [R/W] B,H,W 00000000 00000000		IF1DTA21 [R/W] B,H,W 00000000 00000000		
002124 _H	IF1DTB11 [R/W] B,H,W 00000000 00000000		IF1DTB21 [R/W] B,H,W 00000000 00000000		
002128 _H	—	—	—	—	
00212C _H	—	—	—	—	
002130 _H , 002134 _H	Reserved (IF1 data mirror)				
002138 _H	—	—	—	—	
00213C _H	—	—	—	—	
002140 _H	IF2CREQ1 [R/W] B,H,W 0----- 00000001		IF2CMSK1 [R/W] B,H,W ----- 00000000		
002144 _H	IF2MSK21 [R/W] B,H,W 11-11111 11111111		IF2MSK11 [R/W] B,H,W 11111111 11111111		
002148 _H	IF2ARB21 [R/W] B,H,W 00000000 00000000		IF2ARB11 [R/W] B,H,W 00000000 00000000		
00214C _H	IF2MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	
002150 _H	IF2DTA11 [R/W] B,H,W 00000000 00000000		IF2DTA21 [R/W] B,H,W 00000000 00000000		
002154 _H	IF2DTB11 [R/W] B,H,W 00000000 00000000		IF2DTB21 [R/W] B,H,W 00000000 00000000		
002158 _H	—	—	—	—	
00215C _H	—	—	—	—	
002160 _H , 002164 _H	Reserved (IF2 data mirror)				
002168 _H to 00217C _H	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002180 _H	TREQR21 [R] B,H,W 00000000 00000000		TREQR11 [R] B,H,W 00000000 00000000		CAN1 (128msb)
002184 _H	TREQR41 [R] B,H,W 00000000 00000000		TREQR31 [R] B,H,W 00000000 00000000		
002188 _H	TREQR61 [R] B,H,W 00000000 00000000		TREQR51 [R] B,H,W 00000000 00000000		
00218C _H	TREQR81 [R] B,H,W 00000000 00000000		TREQR71 [R] B,H,W 00000000 00000000		
002190 _H	NEWDT21 [R] B,H,W 00000000 00000000		NEWDT11 [R] B,H,W 00000000 00000000		
002194 _H	NEWDT41 [R] B,H,W 00000000 00000000		NEWDT31 [R] B,H,W 00000000 00000000		
002198 _H	NEWDT61 [R] B,H,W 00000000 00000000		NEWDT51 [R] B,H,W 00000000 00000000		
00219C _H	NEWDT81 [R] B,H,W 00000000 00000000		NEWDT71 [R] B,H,W 00000000 00000000		
0021A0 _H	INTPND21 [R] B,H,W 00000000 00000000		INTPND11 [R] B,H,W 00000000 00000000		
0021A4 _H	INTPND41 [R] B,H,W 00000000 00000000		INTPND31 [R] B,H,W 00000000 00000000		
0021A8 _H	INTPND61 [R] B,H,W 00000000 00000000		INTPND51 [R] B,H,W 00000000 00000000		
0021AC _H	INTPND81 [R] B,H,W 00000000 00000000		INTPND71 [R] B,H,W 00000000 00000000		
0021B0 _H	MSGVAL21 [R] B,H,W 00000000 00000000		MSGVAL11 [R] B,H,W 00000000 00000000		
0021B4 _H	MSGVAL41 [R] B,H,W 00000000 00000000		MSGVAL31 [R] B,H,W 00000000 00000000		
0021B8 _H	MSGVAL61 [R] B,H,W 00000000 00000000		MSGVAL51 [R] B,H,W 00000000 00000000		
0021BC _H	MSGVAL81 [R] B,H,W 00000000 00000000		MSGVAL71 [R] B,H,W 00000000 00000000		
0021C0 _H to 0021FC _H	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002200 _H	CTRLR2 [R/W] B,H,W ----- 000-0001		STATR2 [R/W] B,H,W ----- 00000000		CAN2 (128msb)
002204 _H	ERRCNT2 [R] B,H,W 00000000 00000000		BTR2 [R/W] B,H,W -0100011 00000001		
002208 _H	INTR2 [R] B,H,W 00000000 00000000		TESTR2 [R/W] B,H,W ----- X00000--		
00220C _H	BRPER2 [R/W] B,H,W ----- ----0000		—		
002210 _H	IF1CREQ2 [R/W] B,H,W 0----- 00000001		IF1CMSK2 [R/W] B,H,W ----- 00000000		
002214 _H	IF1MSK22 [R/W] B,H,W 11-11111 11111111		IF1MSK12 [R/W] B,H,W 11111111 11111111		
002218 _H	IF1ARB22 [R/W] B,H,W 00000000 00000000		IF1ARB12 [R/W] B,H,W 00000000 00000000		
00221C _H	IF1MCTR2 [R/W] B,H,W 00000000 0---0000		—		
002220 _H	IF1DTA12 [R/W] B,H,W 00000000 00000000		IF1DTA22 [R/W] B,H,W 00000000 00000000		
002224 _H	IF1DTB12 [R/W] B,H,W 00000000 00000000		IF1DTB22 [R/W] B,H,W 00000000 00000000		
002228 _H	—	—	—	—	
00222C _H	—	—	—	—	
002230 _H , 002234 _H	Reserved (IF1 data mirror)				
002238 _H	—	—	—	—	
00223C _H	—	—	—	—	
002240 _H	IF2CREQ2 [R/W] B,H,W 0----- 00000001		IF2CMSK2 [R/W] B,H,W ----- 00000000		
002244 _H	IF2MSK22 [R/W] B,H,W 11-11111 11111111		IF2MSK12 [R/W] B,H,W 11111111 11111111		
002248 _H	IF2ARB22 [R/W] B,H,W 00000000 00000000		IF2ARB12 [R/W] B,H,W 00000000 00000000		
00224C _H	IF2MCTR2 [R/W] B,H,W 00000000 0---0000		—		
002250 _H	IF2DTA12 [R/W] B,H,W 00000000 00000000		IF2DTA22 [R/W] B,H,W 00000000 00000000		
002254 _H	IF2DTB12 [R/W] B,H,W 00000000 00000000		IF2DTB22 [R/W] B,H,W 00000000 00000000		
002258 _H	—	—	—	—	
00225C _H	—	—	—	—	
002260 _H , 002264 _H	Reserved (IF2 data mirror)				
002268 _H to 00227C _H	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002280 _H	TREQR22 [R] B,H,W 00000000 00000000		TREQR12 [R] B,H,W 00000000 00000000		CAN2 (128msb)
002284 _H	TREQR42 [R] B,H,W 00000000 00000000		TREQR32 [R] B,H,W 00000000 00000000		
002288 _H	TREQR62 [R] B,H,W 00000000 00000000		TREQR52 [R] B,H,W 00000000 00000000		
00228C _H	TREQR82 [R] B,H,W 00000000 00000000		TREQR72 [R] B,H,W 00000000 00000000		
002290 _H	NEWDT22 [R] B,H,W 00000000 00000000		NEWDT12 [R] B,H,W 00000000 00000000		
002294 _H	NEWDT42 [R] B,H,W 00000000 00000000		NEWDT32 [R] B,H,W 00000000 00000000		
002298 _H	NEWDT62 [R] B,H,W 00000000 00000000		NEWDT52 [R] B,H,W 00000000 00000000		
00229C _H	NEWDT82 [R] B,H,W 00000000 00000000		NEWDT72 [R] B,H,W 00000000 00000000		
0022A0 _H	INTPND22 [R] B,H,W 00000000 00000000		INTPND12 [R] B,H,W 00000000 00000000		
0022A4 _H	INTPND42 [R] B,H,W 00000000 00000000		INTPND32 [R] B,H,W 00000000 00000000		
0022A8 _H	INTPND62 [R] B,H,W 00000000 00000000		INTPND52 [R] B,H,W 00000000 00000000		
0022AC _H	INTPND82 [R] B,H,W 00000000 00000000		INTPND72 [R] B,H,W 00000000 00000000		
0022B0 _H	MSGVAL22 [R] B,H,W 00000000 00000000		MSGVAL12 [R] B,H,W 00000000 00000000		
0022B4 _H	MSGVAL42 [R] B,H,W 00000000 00000000		MSGVAL32 [R] B,H,W 00000000 00000000		
0022B8 _H	MSGVAL62 [R] B,H,W 00000000 00000000		MSGVAL52 [R] B,H,W 00000000 00000000		
0022BC _H	MSGVAL82 [R] B,H,W 00000000 00000000		MSGVAL72 [R] B,H,W 00000000 00000000		
0022C0 _H to 0022FC _H	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002300 _H	DFCTLR [R/W] B,H,W -0-----		—	DFSTR [R/W] B,H,W ----001	WorkFlash
002304 _H	—	—	—	—	
002308 _H	FLIFCTLR [R/W] B,H,W --0--00	—	FLIFFER1 [R/W] B,H,W -----	FLIFFER2 [R/W] B,H,W -----	Flash / WorkFlash
00230C _H	—				Reserved
002310 _H	TRCR [R/W] B,H,W 00000000	TRAR [R/W] B,H,W 00000000	—		TuningRAM
002314 _H to 0023FC _H	—				Reserved
002400 _H	SEEARX [R] B,H,W 00000000 00000000		DEEARX [R] B,H,W 00000000 00000000		XBS RAM ECC control
002404 _H	EECSRX [R/W] B,H,W ----00--	—	EFEARX [R/W] B,H,W 00000000 00000000		
002408 _H	—	EFECRX [R/W] B,H,W -----0 00000000 00000000			
00240C _H to 0024FC _H	—				Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002500 _H	CTRLR3 [R/W] B,H,W ----- 000-0001		STATR3 [R/W] B,H,W ----- 00000000		CAN3 (128msb)
002504 _H	ERRCNT3 [R] B,H,W 00000000 00000000		BTR3 [R/W] B,H,W -0100011 00000001		
002508 _H	INTR3 [R] B,H,W 00000000 00000000		TESTR3 [R/W] B,H,W ----- X00000--		
00250C _H	BRPER3 [R/W] B,H,W ----- ----0000		—	—	
002510 _H	IF1CREQ3 [R/W] B,H,W 0----- 00000001		IF1CMSK3 [R/W] B,H,W ----- 00000000		
002514 _H	IF1MSK23 [R/W] B,H,W 11-11111 11111111		IF1MSK13 [R/W] B,H,W 11111111 11111111		
002518 _H	IF1ARB23 [R/W] B,H,W 00000000 00000000		IF1ARB13 [R/W] B,H,W 00000000 00000000		
00251C _H	IF1MCTR3 [R/W] B,H,W 00000000 0---0000		—	—	
002520 _H	IF1DTA13 [R/W] B,H,W 00000000 00000000		IF1DTA23 [R/W] B,H,W 00000000 00000000		
002524 _H	IF1DTB13 [R/W] B,H,W 00000000 00000000		IF1DTB23 [R/W] B,H,W 00000000 00000000		
002528 _H	—	—	—	—	
00252C _H	—	—	—	—	
002530 _H , 002534 _H	Reserved (IF1 data mirror)				
002538 _H	—	—	—	—	
00253C _H	—	—	—	—	
002540 _H	IF2CREQ3 [R/W] B,H,W 0----- 00000001		IF2CMSK3 [R/W] B,H,W ----- 00000000		
002544 _H	IF2MSK23 [R/W] B,H,W 11-11111 11111111		IF2MSK13 [R/W] B,H,W 11111111 11111111		
002548 _H	IF2ARB23 [R/W] B,H,W 00000000 00000000		IF2ARB13 [R/W] B,H,W 00000000 00000000		
00254C _H	IF2MCTR3 [R/W] B,H,W 00000000 0---0000		—	—	
002550 _H	IF2DTA13 [R/W] B,H,W 00000000 00000000		IF2DTA23 [R/W] B,H,W 00000000 00000000		
002554 _H	IF2DTB13 [R/W] B,H,W 00000000 00000000		IF2DTB23 [R/W] B,H,W 00000000 00000000		
002558 _H	—	—	—	—	
00255C _H	—	—	—	—	
002560 _H , 002564 _H	Reserved (IF2 data mirror)				
002568 _H	—	—	—	—	
00256C _H	—	—	—	—	
002570 _H to 00257C _H	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002580 _H	TREQR23 [R] B,H,W 00000000 00000000		TREQR13 [R] B,H,W 00000000 00000000		CAN3 (128msb)
002584 _H	TREQR43 [R] B,H,W 00000000 00000000		TREQR33 [R] B,H,W 00000000 00000000		
002588 _H	TREQR63 [R] B,H,W 00000000 00000000		TREQR53 [R] B,H,W 00000000 00000000		
00258C _H	TREQR83 [R] B,H,W 00000000 00000000		TREQR73 [R] B,H,W 00000000 00000000		
002590 _H	NEWDT23 [R] B,H,W 00000000 00000000		NEWDT13 [R] B,H,W 00000000 00000000		
002594 _H	NEWDT43 [R] B,H,W 00000000 00000000		NEWDT33 [R] B,H,W 00000000 00000000		
002598 _H	NEWDT63 [R] B,H,W 00000000 00000000		NEWDT53 [R] B,H,W 00000000 00000000		
00259C _H	NEWDT83 [R] B,H,W 00000000 00000000		NEWDT73 [R] B,H,W 00000000 00000000		
0025A0 _H	INTPND23 [R] B,H,W 00000000 00000000		INTPND13 [R] B,H,W 00000000 00000000		
0025A4 _H	INTPND43 [R] B,H,W 00000000 00000000		INTPND33 [R] B,H,W 00000000 00000000		
0025A8 _H	INTPND63 [R] B,H,W 00000000 00000000		INTPND53 [R] B,H,W 00000000 00000000		
0025AC _H	INTPND83 [R] B,H,W 00000000 00000000		INTPND73 [R] B,H,W 00000000 00000000		
0025B0 _H	MSGVAL23 [R] B,H,W 00000000 00000000		MSGVAL13 [R] B,H,W 00000000 00000000		
0025B4 _H	MSGVAL43 [R] B,H,W 00000000 00000000		MSGVAL33 [R] B,H,W 00000000 00000000		
0025B8 _H	MSGVAL63 [R] B,H,W 00000000 00000000		MSGVAL53 [R] B,H,W 00000000 00000000		
0025BC _H	MSGVAL83 [R] B,H,W 00000000 00000000		MSGVAL73 [R] B,H,W 00000000 00000000		
0025C0 _H to 0025FC _H	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002600 _H	CTRLR4 [R/W] B,H,W ----- 000-0001		STATR4 [R/W] B,H,W ----- 00000000		CAN4 (128msb)
002604 _H	ERRCNT4 [R] B,H,W 00000000 00000000		BTR4 [R/W] B,H,W -0100011 00000001		
002608 _H	INTR4 [R] B,H,W 00000000 00000000		TESTR4 [R/W] B,H,W ----- X00000--		
00260C _H	BRPER4 [R/W] B,H,W ----- ----0000		—	—	
002610 _H	IF1CREQ4 [R/W] B,H,W 0----- 00000001		IF1CMSK4 [R/W] B,H,W ----- 00000000		
002614 _H	IF1MSK24 [R/W] B,H,W 11-11111 11111111		IF1MSK14 [R/W] B,H,W 11111111 11111111		
002618 _H	IF1ARB24 [R/W] B,H,W 00000000 00000000		IF1ARB14 [R/W] B,H,W 00000000 00000000		
00261C _H	IF1MCTR4 [R/W] B,H,W 00000000 0---0000		—	—	
002620 _H	IF1DTA14 [R/W] B,H,W 00000000 00000000		IF1DTA24 [R/W] B,H,W 00000000 00000000		
002624 _H	IF1DTB14 [R/W] B,H,W 00000000 00000000		IF1DTB24 [R/W] B,H,W 00000000 00000000		
002628 _H	—	—	—	—	
00262C _H	—	—	—	—	
002630 _H , 002634 _H	Reserved (IF1 data mirror)				
002638 _H	—	—	—	—	
00263C _H	—	—	—	—	
002640 _H	IF2CREQ4 [R/W] B,H,W 0----- 00000001		IF2CMSK4 [R/W] B,H,W ----- 00000000		
002644 _H	IF2MSK24 [R/W] B,H,W 11-11111 11111111		IF2MSK14 [R/W] B,H,W 11111111 11111111		
002648 _H	IF2ARB24 [R/W] B,H,W 00000000 00000000		IF2ARB14 [R/W] B,H,W 00000000 00000000		
00264C _H	IF2MCTR4 [R/W] B,H,W 00000000 0---0000		—	—	
002650 _H	IF2DTA14 [R/W] B,H,W 00000000 00000000		IF2DTA24 [R/W] B,H,W 00000000 00000000		
002654 _H	IF2DTB14 [R/W] B,H,W 00000000 00000000		IF2DTB24 [R/W] B,H,W 00000000 00000000		
002658 _H	—	—	—	—	
00265C _H	—	—	—	—	
002660 _H , 002664 _H	Reserved (IF2 data mirror)				
002668 _H	—	—	—	—	
00266C _H	—	—	—	—	
002670 _H to 00267C _H	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002680 _H	TREQR24 [R] B,H,W 00000000 00000000		TREQR14 [R] B,H,W 00000000 00000000		CAN4 (128msb)
002684 _H	TREQR44 [R] B,H,W 00000000 00000000		TREQR34 [R] B,H,W 00000000 00000000		
002688 _H	TREQR64 [R] B,H,W 00000000 00000000		TREQR54 [R] B,H,W 00000000 00000000		
00268C _H	TREQR84 [R] B,H,W 00000000 00000000		TREQR74 [R] B,H,W 00000000 00000000		
002690 _H	NEWDT24 [R] B,H,W 00000000 00000000		NEWDT14 [R] B,H,W 00000000 00000000		
002694 _H	NEWDT44 [R] B,H,W 00000000 00000000		NEWDT34 [R] B,H,W 00000000 00000000		
002698 _H	NEWDT64 [R] B,H,W 00000000 00000000		NEWDT54 [R] B,H,W 00000000 00000000		
00269C _H	NEWDT84 [R] B,H,W 00000000 00000000		NEWDT74 [R] B,H,W 00000000 00000000		
0026A0 _H	INTPND24 [R] B,H,W 00000000 00000000		INTPND14 [R] B,H,W 00000000 00000000		
0026A4 _H	INTPND44 [R] B,H,W 00000000 00000000		INTPND34 [R] B,H,W 00000000 00000000		
0026A8 _H	INTPND64 [R] B,H,W 00000000 00000000		INTPND54 [R] B,H,W 00000000 00000000		
0026AC _H	INTPND84 [R] B,H,W 00000000 00000000		INTPND74 [R] B,H,W 00000000 00000000		
0026B0 _H	MSGVAL24 [R] B,H,W 00000000 00000000		MSGVAL14 [R] B,H,W 00000000 00000000		
0026B4 _H	MSGVAL44 [R] B,H,W 00000000 00000000		MSGVAL34 [R] B,H,W 00000000 00000000		
0026B8 _H	MSGVAL64 [R] B,H,W 00000000 00000000		MSGVAL54 [R] B,H,W 00000000 00000000		
0026BC _H	MSGVAL84 [R] B,H,W 00000000 00000000		MSGVAL74 [R] B,H,W 00000000 00000000		
0026C0 _H to 0026FC _H	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002700 _H	CTRLR5 [R/W] B,H,W ----- 000-0001		STATR5 [R/W] B,H,W ----- 00000000		CAN5 (128msb)
002704 _H	ERRCNT5 [R] B,H,W 00000000 00000000		BTR5 [R/W] B,H,W -0100011 00000001		
002708 _H	INTR5 [R] B,H,W 00000000 00000000		TESTR5 [R/W] B,H,W ----- X00000--		
00270C _H	BRPER5 [R/W] B,H,W ----- ----0000		—	—	
002710 _H	IF1CREQ5 [R/W] B,H,W 0----- 00000001		IF1CMSK5 [R/W] B,H,W ----- 00000000		
002714 _H	IF1MSK25 [R/W] B,H,W 11-11111 11111111		IF1MSK15 [R/W] B,H,W 11111111 11111111		
002718 _H	IF1ARB25 [R/W] B,H,W 00000000 00000000		IF1ARB15 [R/W] B,H,W 00000000 00000000		
00271C _H	IF1MCTR5 [R/W] B,H,W 00000000 0---0000		—	—	
002720 _H	IF1DTA15 [R/W] B,H,W 00000000 00000000		IF1DTA25 [R/W] B,H,W 00000000 00000000		
002724 _H	IF1DTB15 [R/W] B,H,W 00000000 00000000		IF1DTB25 [R/W] B,H,W 00000000 00000000		
002728 _H	—	—	—	—	
00272C _H	—	—	—	—	
002730 _H , 002734 _H	Reserved (IF1 data mirror)				
002738 _H	—	—	—	—	
00273C _H	—	—	—	—	
002740 _H	IF2CREQ5 [R/W] B,H,W 0----- 00000001		IF2CMSK5 [R/W] B,H,W ----- 00000000		
002744 _H	IF2MSK25 [R/W] B,H,W 11-11111 11111111		IF2MSK15 [R/W] B,H,W 11111111 11111111		
002748 _H	IF2ARB25 [R/W] B,H,W 00000000 00000000		IF2ARB15 [R/W] B,H,W 00000000 00000000		
00274C _H	IF2MCTR5 [R/W] B,H,W 00000000 0---0000		—	—	
002750 _H	IF2DTA15 [R/W] B,H,W 00000000 00000000		IF2DTA25 [R/W] B,H,W 00000000 00000000		
002754 _H	IF2DTB15 [R/W] B,H,W 00000000 00000000		IF2DTB25 [R/W] B,H,W 00000000 00000000		
002758 _H	—	—	—	—	
00275C _H	—	—	—	—	
002760 _H , 002764 _H	Reserved (IF2 data mirror)				
002768 _H	—	—	—	—	
00276C _H	—	—	—	—	
002770 _H to 00277C _H	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
002780 _H	TREQR25 [R] B,H,W 00000000 00000000		TREQR15 [R] B,H,W 00000000 00000000		CAN5 (128msb)
002784 _H	TREQR45 [R] B,H,W 00000000 00000000		TREQR35 [R] B,H,W 00000000 00000000		
002788 _H	TREQR65 [R] B,H,W 00000000 00000000		TREQR55 [R] B,H,W 00000000 00000000		
00278C _H	TREQR85 [R] B,H,W 00000000 00000000		TREQR75 [R] B,H,W 00000000 00000000		
002790 _H	NEWDT25 [R] B,H,W 00000000 00000000		NEWDT15 [R] B,H,W 00000000 00000000		
002794 _H	NEWDT45 [R] B,H,W 00000000 00000000		NEWDT35 [R] B,H,W 00000000 00000000		
002798 _H	NEWDT65 [R] B,H,W 00000000 00000000		NEWDT55 [R] B,H,W 00000000 00000000		
00279C _H	NEWDT85 [R] B,H,W 00000000 00000000		NEWDT75 [R] B,H,W 00000000 00000000		
0027A0 _H	INTPND25 [R] B,H,W 00000000 00000000		INTPND15 [R] B,H,W 00000000 00000000		
0027A4 _H	INTPND45 [R] B,H,W 00000000 00000000		INTPND35 [R] B,H,W 00000000 00000000		
0027A8 _H	INTPND65 [R] B,H,W 00000000 00000000		INTPND55 [R] B,H,W 00000000 00000000		
0027AC _H	INTPND85 [R] B,H,W 00000000 00000000		INTPND75 [R] B,H,W 00000000 00000000		
0027B0 _H	MSGVAL25 [R] B,H,W 00000000 00000000		MSGVAL15 [R] B,H,W 00000000 00000000		
0027B4 _H	MSGVAL45 [R] B,H,W 00000000 00000000		MSGVAL35 [R] B,H,W 00000000 00000000		
0027B8 _H	MSGVAL65 [R] B,H,W 00000000 00000000		MSGVAL55 [R] B,H,W 00000000 00000000		
0027BC _H	MSGVAL85 [R] B,H,W 00000000 00000000		MSGVAL75 [R] B,H,W 00000000 00000000		
0027C0 _H to 002FFC _H	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
003000 _H	SEEARA [R] B,H,W ----0000 00000000		DEEARA [R] B,H,W ----0000 00000000		Backup RAM ECC control
003004 _H	EECSRA [R/W] B,H,W ----00--	—	EFEARA [R/W] B,H,W ----0000 00000000		
003008 _H	—	EFECRA [R/W] B,H,W -----0 00000000 00000000			
00300C _H	TEAR0X[R] B,H,W 000----- 00000000 00000000				RAM/diagnosis XBS RAM
003010 _H	TEAR1X[R] B,H,W 000----- 00000000 00000000				
003014 _H	TEAR2X[R] B,H,W 000----- 00000000 00000000				
003018 _H	TAEARX [R/W] B,H,W 10111111 11111111		TASARX [R/W] B,H,W 00000000 00000000		
00301C _H	TFECRX [R/W] B,H,W ----0000	TICRX [R/W] B,H,W ----0000	TTCRX [R/W] B,H,W -----00 00001100		
003020 _H	TSRCRX [W] B,H,W 0-----	—	—	TKCCRX [R/W] B,H,W 00----00	
003024 _H to 00302C _H	—				Reserved
003030 _H	TEAR0A[R] B,H,W 000----- 0000 00000000				RAM/diagnosis Backup RAM
003034 _H	TEAR1A[R] B,H,W 000----- 0000 00000000				
003038 _H	TEAR2A[R] B,H,W 000----- 0000 00000000				
00303C _H	TAEARA[R/W] B,H,W ----1111 11111111		TASARA[R/W] B,H,W ----0000 00000000		
003040 _H	TFECRA [R/W] B,H,W ----0000	TICRA [R/W] B,H,W ----0000	TTCRA [R/W] B,H,W -----00 00001100		
003044 _H	TSRCRA [W] B,H,W 0-----	—	—	TKCCRA [R/W] B,H,W 00----00	
003048 _H , 00304C _H	—				Reserved
003050 _H	SEEARH [R] B,H,W --000000 00000000		DEEARH [R] B,H,W --000000 00000000		AHB RAM ECC control
003054 _H	EECSRH [R/W] B,H,W ----00--	—	EFEARH [R/W] B,H,W --000000 00000000		
003058 _H	—	EFECRH [R/W] B,H,W -----0 00000000 00000000			
00305C _H	—				Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
003060 _H	TEAR0H[R] B,H,W 000----- --000000 00000000				RAM/diagnosis AHB RAM
003064 _H	TEAR1H[R] B,H,W 000----- --000000 00000000				
003068 _H	TEAR2H[R] B,H,W 000----- --000000 00000000				
00306C _H	TAEARH[R/W] B,H,W --111111 11111111		TASARH[R/W] B,H,W --000000 00000000		
003070 _H	TFECRH [R/W] B,H,W ---0000	TICRH [R/W] B,H,W ---0000	TTCRH [R/W] B,H,W -----00 00001100		
003074 _H	TSRCRH [W] B,H,W 0-----	—	—	TKCCRH [R/W] B,H,W 00----00	
003078 _H to 0030FC _H	—				Reserved
003100 _H	BUSDIGSR0[R/W] H,W 00000000 0----00		BUSDIGSR1[R/W] H,W 00000000 0----00		BUS diagnosis
003104 _H	BUSDIGSR2[R/W] H,W 00000000 0----00		BUSTSTR0[R/W] H,W 00--0000 00000000		
003108 _H	BUSADR0 [R] W 00000000 00000000 00000000 00000000				
00310C _H	BUSADR1 [R] W 00000000 00000000 00000000 00000000				
003110 _H	BUSADR2 [R] W 00000000 00000000 00000000 00000000				
003114 _H	—	—	BUSDIGSR3[R/W] H,W 00000000 0----00		
003118 _H	BUSDIGSR4[R/W] H,W 00000000 0----00		BUSTSTR1[R/W] H,W 00--000- 00000000		
00311C _H	—	—	—	—	
003120 _H	BUSADR3 [R] W 00000000 00000000 00000000 00000000				
003124 _H	BUSADR4 [R] W 00000000 00000000 00000000 00000000				
003128 _H to 003FFC _H	—				Reserved
004000 _H to 007FFC _H	Backup-RAM				Backup RAM area
008000 _H to 00CFFC _H	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00D000 _H	CIF0[R] W 00000100 11111111 01011011 11111111				FlexRay CIF
00D004 _H	CIF1[R/W] W 00000000 -----0 -0000000 -----				
00D008 _H to 00D018 _H	—	—	—	—	Reserved
00D01C _H	LCK[R/W] W -----00000000				FlexRay GIF
00D020 _H	EIR[R/W] W ----000 ----000 ---0000 00000000				FlexRay INT
00D024 _H	SIR[R/W] W -----00 -----00 00000000 00000000				
00D028 _H	EILS[R/W] W ----000 ----000 ---0000 00000000				
00D02C _H	SILS[R/W] W -----11 -----11 11111111 11111111				
00D030 _H	EIES[R/W] W ----000 ----000 ---0000 00000000				
00D034 _H	EIER[R/W] W ----000 ----000 ---0000 00000000				
00D038 _H	SIES[R/W] W -----00 -----00 00000000 00000000				
00D03C _H	SIER[R/W] W -----00 -----00 00000000 00000000				
00D040 _H	ILE[R/W] W -----00				
00D044 _H	T0C[R/W] W --000000 00000000 -0000000 -----00				
00D048 _H	T1C[R/W] W --000000 00000010 -----00				
00D04C _H	STPW1[R/W] W --000000 00000000 --000000 -0000000				
00D050 _H	STPW2[R] W -----000 00000000 -----000 00000000				
00D054 _H to 00D07C _H	—	—	—	—	Reserved
00D080 _H	SUCC1[R/W] W ----1100 01000000 00010-00 1---0000				FlexRay SUC
00D084 _H	SUCC2[R/W] W ----0001 ---00000 00000101 00000100				
00D088 _H	SUCC3[R/W] W -----00010001				
00D08C _H	NEMC[R/W] W -----0000				FlexRay NEM
00D090 _H	PRTC1[R/W] W 000010-0 01001100 0000-110 00110011				FlexRay PRT
00D094 _H	PRTC2[R/W] W --001111 00101101 --001010 —001110				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00D098 _H	MHDC[R/W] W ---00000 00000000 ----- -0000000				FlexRay MHD
00D09C _H	—				Reserved
00D0A0 _H	GTUC1[R/W] W ----- ----0000 00000010 10000000				FlexRay GTU
00D0A4 _H	GTUC2[R/W] W ----- ----0010 --000000 00001010				
00D0A8 _H	GTUC3[R/W] W -0000010 -0000010 00000000 00000000				
00D0AC _H	GTUC4[R/W] W --000000 00001000 --000000 00000111				
00D0B0 _H	GTUC5[R/W] W 00001110 ---00000 00000000 00000000				
00D0B4 _H	GTUC6[R/W] W ----000 00000010 ----000 00000000				
00D0B8 _H	GTUC7[R/W] W -----00 00000010 -----00 00000100				
00D0BC _H	GTUC8[R/W] W --00000 00000000 ----- --000010				
00D0C0 _H	GTUC9[R/W] W ----- ----00 --00001 —000001				
00D0C4 _H	GTUC10[R/W] W ----000 00000010 --000000 00000101				
00D0C8 _H	GTUC11[R/W] W ----000 ----000 -----00 -----00				
00D0CC _H to 00D0FC _H	—	—	—	—	Reserved
00D100 _H	CCSV[R] W --000000 00010000 -100--00 00000000				FlexRay SUC
00D104 _H	CCEV[R] W ----- ----000000 00--0000				
00D108 _H	—				Reserved
00D10C _H	—				
00D110 _H	SCV[R] W ----000 00000000 ----000 00000000				FlexRay GTU
00D114 _H	MTCCV[R] W ----- --000000 --000000 00000000				
00D118 _H	RCV[R] W ----- ----0000 00000000				
00D11C _H	OCV[R] W ----- ----000 00000000 00000000				
00D120 _H	SFS[R] W ----- ----0000 00000000 00000000				
00D124 _H	SWNIT[R] W ----- ----0000 00000000				
00D128 _H	ACS[R/W] W ----- ----000000 ---000000				
00D12C _H	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00D130 _H	ESID1[R] W ----- 00---00 00000000				FlexRay GTU
00D134 _H	ESID2[R] W ----- 00---00 00000000				
00D138 _H	ESID3[R] W ----- 00---00 00000000				
00D13C _H	ESID4[R] W ----- 00---00 00000000				
00D140 _H	ESID5[R] W ----- 00---00 00000000				
00D144 _H	ESID6[R] W ----- 00---00 00000000				
00D148 _H	ESID7[R] W ----- 00---00 00000000				
00D14C _H	ESID8[R] W ----- 00---00 00000000				
00D150 _H	ESID9[R] W ----- 00---00 00000000				
00D154 _H	ESID10[R] W ----- 00---00 00000000				
00D158 _H	ESID11[R] W ----- 00---00 00000000				
00D15C _H	ESID12[R] W ----- 00---00 00000000				
00D160 _H	ESID13[R] W ----- 00---00 00000000				
00D164 _H	ESID14[R] W ----- 00---00 00000000				
00D168 _H	ESID15[R] W ----- 00---00 00000000				
00D16C _H	—				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00D170 _H	OSID1[R] W ----- 00----00 00000000				FlexRay GTU
00D174 _H	OSID2[R] W ----- 00----00 00000000				
00D178 _H	OSID3[R] W ----- 00----00 00000000				
00D17C _H	OSID4[R] W ----- 00----00 00000000				
00D180 _H	OSID5[R] W ----- 00----00 00000000				
00D184 _H	OSID6[R] W ----- 00----00 00000000				
00D188 _H	OSID7[R] W ----- 00----00 00000000				
00D18C _H	OSID8[R] W ----- 00----00 00000000				
00D190 _H	OSID9[R] W ----- 00----00 00000000				
00D194 _H	OSID10[R] W ----- 00----00 00000000				
00D198 _H	OSID11[R] W ----- 00----00 00000000				
00D19C _H	OSID12[R] W ----- 00----00 00000000				
00D1A0 _H	OSID13[R] W ----- 00----00 00000000				
00D1A4 _H	OSID14[R] W ----- 00----00 00000000				
00D1A8 _H	OSID15[R] W ----- 00----00 00000000				
00D1AC _H	—				Reserved
00D1B0 _H	NMV1[R] W 00000000 00000000 00000000 00000000				FlexRay NEM
00D1B4 _H	NMV2[R] W 00000000 00000000 00000000 00000000				
00D1B8 _H	NMV3[R] W 00000000 00000000 00000000 00000000				
00D1BC _H to 00D2FC _H	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00D300 _H	MRC[R/W] W -----001 10000000 00000000 00000000				FlexRay MHD
00D304 _H	FRF[R/W] W -----1 10000000 ---00000 00000000				
00D308 _H	FRFM[R/W] W -----00000 000000--				
00D30C _H	FCL[R/W] W -----10000000				
00D310 _H	MHDS[R/W] W -0000000 -0000000 -0000000 10000000				
00D314 _H	LDTS[R] W -----000 00000000 ----000 00000000				
00D318 _H	FSR[R] W -----00000000 ----000				
00D31C _H	MHDF[R/W] W -----0 00000000				
00D320 _H	TXRQ1[R] W 00000000 00000000 00000000 00000000				
00D324 _H	TXRQ2[R] W 00000000 00000000 00000000 00000000				
00D328 _H	TXRQ3[R] W 00000000 00000000 00000000 00000000				
00D32C _H	TXRQ4[R] W 00000000 00000000 00000000 00000000				
00D330 _H	NDAT1[R] W 00000000 00000000 00000000 00000000				
00D334 _H	NDAT2[R] W 00000000 00000000 00000000 00000000				
00D338 _H	NDAT3[R] W 00000000 00000000 00000000 00000000				
00D33C _H	NDAT4[R] W 00000000 00000000 00000000 00000000				
00D340 _H	MBSC1[R] W 00000000 00000000 00000000 00000000				
00D344 _H	MBSC2[R] W 00000000 00000000 00000000 00000000				
00D348 _H	MBSC3[R] W 00000000 00000000 00000000 00000000				
00D34C _H	MBSC4[R] W 00000000 00000000 00000000 00000000				
00D350 _H to 00D3EC _H	—	—	—	—	Reserved
00D3F0 _H	CREL[R] W 00010000 00111001 00000010 00000110				FlexRay GIF
00D3F4 _H	ENDN[R] W 10000111 01100101 01000011 00100001				
00D3F8 _H , 00D3FC _H	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00D400 _H to 00D4FC _H	WRDSn[1-64][R/W] W 00000000 00000000 00000000 00000000				FlexRay IBF
00D500 _H	WRHS1[R/W] W --000000 -00000000 -----000 00000000				
00D504 _H	WRHS2[R/W] W ----- -00000000 -----000 00000000				
00D508 _H	WRHS3[R/W] W ----- -----000 00000000				
00D50C _H	—				
00D510 _H	IBCM[R/W] W ----- -----000 -----000				
00D514 _H	IBCR[R/W] W 0----- -00000000 0----- -00000000				
00D518 _H to 00D5FC _H	—	—	—	—	Reserved
00D600 _H to 00D6FC _H	RDDSn[1-64][R] W 00000000 00000000 00000000 00000000				FlexRay OBF
00D700 _H	RDHS1[R] W --000000 -00000000 -----000 00000000				
00D704 _H	RDHS2[R] W -00000000 -00000000 -----000 00000000				
00D708 _H	RDHS3[R] W --000000 --000000 -----000 00000000				
00D70C _H	MBS[R] W --000000 --000000 00-000000 00000000				
00D710 _H	OBCM[R/W] W ----- -----00 -----00				
00D714 _H	OBCR[R/W] W ----- -00000000 0-----00 -00000000				
00D718 _H to 00D7FC _H	—	—	—	—	Reserved
00D800 _H to 00EFFC _H	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00F00 _H to 00FEFC _H	—	—	—	—	Reserved [S]
00FF00 _H	DSUCR [R/W] B,H,W -----0		—	—	OCDU [S]
00FF04 _H to 00FF0C _H	—				Reserved [S]
00FF10 _H	PCSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
00FF14 _H	PSSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
00FF18 _H to 00FFF4 _H	—				Reserved [S]
00FFF8 _H	EDIR1 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
00FFFC _H	EDIR0 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

[S]: It is a system register. The illegal instruction exception (data access error) is generated in these registers in the user mode when reading and writing to it.

10. Interrupt Vector Table

This list shows the assignments of interrupt factors and interrupt vectors/interrupt control registers.

Interrupt vector MB91F52xR (144pin)

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Reset	0	0	-	3FC _H	000FFFFC _H	-
System reserved	1	1	-	3F8 _H	000FFFF8 _H	-
System reserved	2	2	-	3F4 _H	000FFFF4 _H	-
System reserved	3	3	-	3F0 _H	000FFFF0 _H	-
System reserved	4	4	-	3EC _H	000FFFE _C	-
FPU exception	5	5	-	3E8 _H	000FFFE8 _H	-
Exception of instruction access protection violation	6	6	-	3E4 _H	000FFFE4 _H	-
Exception of data access protection violation	7	7	-	3E0 _H	000FFFE0 _H	-
Data access error interrupt	8	8	-	3DC _H	000FFFD _C	-
INTE instruction	9	9	-	3D8 _H	000FFFD8 _H	-
Instruction break	10	0A	-	3D4 _H	000FFFD4 _H	-
System reserved	11	0B	-	3D0 _H	000FFFD0 _H	-
System reserved	12	0C	-	3CC _H	000FFFC _C	-
System reserved	13	0D	-	3C8 _H	000FFFC8 _H	-
Exception of illegal instruction	14	0E	-	3C4 _H	000FFFC4 _H	-
NMI request	15	0F	15(F _H) Fixed	3C0 _H	000FFFC0 _H	-
Error generation at internal bus diagnosis						
XBS RAM double-bit error detection						
Backup RAM double-bit error detection						
AHB RAM double-bit error detection						
TPU violation						
External interrupt 0-7	16	10	ICR00	3BC _H	000FFFB _C	0
External interrupt 8-15	17	11	ICR01	3B8 _H	000FFFB8 _H	1* ⁶
External low-voltage detection interrupt						
-						
Reload timer 0/1/4/5	18	12	ICR02	3B4 _H	000FFFB4 _H	2* ²
Reload timer 2/3/6/7	19	13	ICR03	3B0 _H	000FFFB0 _H	3* ²
Multi-function serial interface ch.0 (reception completed)	20	14	ICR04	3AC _H	000FFFA _C	4* ¹
Multi-function serial interface ch.0 (status)						
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	3A8 _H	000FFFA8 _H	5* ¹
Multi-function serial interface ch.1 (reception completed)	22	16	ICR06	3A4 _H	000FFFA4 _H	6* ¹
Multi-function serial interface ch.1 (status)						
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	3A0 _H	000FFFA0 _H	7* ¹

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Multi-function serial interface ch.2 (reception completed)	24	18	ICR08	39C _H	000FFF9C _H	8* ¹
Multi-function serial interface ch.2 (status)						
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398 _H	000FFF98 _H	9* ¹
Multi-function serial interface ch.3 (reception completed)	26	1A	ICR10	394 _H	000FFF94 _H	10* ¹
Multi-function serial interface ch.3 (status)						
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390 _H	000FFF90 _H	11
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	38C _H	000FFF8C _H	12* ¹
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388 _H	000FFF88 _H	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384 _H	000FFF84 _H	14* ¹
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380 _H	000FFF80 _H	15* ⁷
FlexRay0						
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	37C _H	000FFF7C _H	16* ¹
Multi-function serial interface ch.6 (status)						
FlexRay1	33	21	ICR17	378 _H	000FFF78 _H	17* ⁸
Multi-function serial interface ch.6 (transmission completed)						
FlexRay timer 0	34	22	ICR18	374 _H	000FFF74 _H	-
CAN0						
CAN3	35	23	ICR19	370 _H	000FFF70 _H	-
FlexRay timer 1						
CAN1						
RAM diagnosis completed						
RAM initialization completed						
Error generation at RAM diagnosis						
Backup RAM diagnosis completed						
Backup RAM initialization completed						
Error generation at Backup RAM diagnosis						
AHB RAM diagnosis completed						
AHB RAM initialization completed						
Error generation at AHB RAM diagnosis						
CAN4						

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
CAN2	36	24	ICR20	36C _H	000FFF6C _H	-
Up/down counter 0						
Up/down counter 1						
CAN5						
FlexRay PLL gear/FlexRay PLL alarm	37	25	ICR21	368 _H	000FFF68 _H	-
Real time clock						
Multi-function serial interface ch.7 (reception completed)	38	26	ICR22	364 _H	000FFF64 _H	22* ¹
Multi-function serial interface ch.7 (status)						
16-bit free-run timer 0 ("0" detection) / (compare clear)	39	27	ICR23	360 _H	000FFF60 _H	23
Multi-function serial interface ch.7 (transmission completed)						
PPG0/1/10/11/20/21/30/31/40/41	40	28	ICR24	35C _H	000FFF5C _H	24* ³
16-bit free-run timer 1 ("0" detection) / (compare clear)						
PPG2/3/12/13/22/23/32/33/43	41	29	ICR25	358 _H	000FFF58 _H	25* ³
16-bit free-run timer 2 ("0" detection) / (compare clear)						
PPG4/5/14/15/24/25/34/35/44	42	2A	ICR26	354 _H	000FFF54 _H	26* ³
PPG6/7/16/17/26/27/36/37	43	2B	ICR27	350 _H	000FFF50 _H	27* ³
PPG8/9/18/19/28/29	44	2C	ICR28	34C _H	000FFF4C _H	28* ³
Multi-function serial interface ch.8 (reception completed)	45	2D	ICR29	348 _H	000FFF48 _H	29* ¹
Multi-function serial interface ch.8 (status)						
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)						
Main timer	46	2E	ICR30	344 _H	000FFF44 _H	30
Sub timer						
PLL timer						
Multi-function serial interface ch.8 (transmission completed)						
16-bit ICU 2 (fetching) / 16-bit ICU 3 (fetching)						
Clock calibration unit (Sub oscillation)	47	2F	ICR31	340 _H	000FFF40 _H	31* ¹ *4
Multi-function serial interface ch.9 (reception completed)						
Multi-function serial interface ch.9 (status)						
A/D converter	48	30	ICR32	33C _H	000FFF3C _H	32
0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16 17/18/19/20/21/22/23/24/25/26/27/28/29/30/31						
Clock calibration unit (CR oscillation)	49	31	ICR33	338 _H	000FFF38 _H	33
Multi-function serial interface ch.9 (transmission completed)						
16-bit OCU 0 (match) / 16-bit OCU 1 (match)						
32-bit free-run timer 4	50	32	ICR34	334 _H	000FFF34 _H	34* ⁵
16-bit OCU 2 (match) / 16-bit OCU 3 (match)						
32-bit free-run timer 3/5	51	33	ICR35	330 _H	000FFF30 _H	35* ⁵
16-bit OCU 4 (match) / 16-bit OCU 5 (match)						

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
32-bit ICU6 (fetching /measurement)	52	34	ICR36	32C _H	000FFF2C _H	36* ¹
Multi-function serial interface ch.10 (reception completed)						
Multi-function serial interface ch.10 (status)						
32-bit ICU7 (fetching /measurement)	53	35	ICR37	328 _H	000FFF28 _H	37
Multi-function serial interface ch.10 (transmission completed)						
32-bit ICU8 (fetching /measurement)						
Multi-function serial interface ch.11 (reception completed)	54	36	ICR38	324 _H	000FFF24 _H	38* ¹
Multi-function serial interface ch.11 (status)						
32-bit ICU9 (fetching /measurement)						
WG dead timer underflow 0 / 1/ 2	55	37	ICR39	320 _H	000FFF20 _H	39
WG dead timer reload 0 / 1/ 2						
WG DTTI 0						
32-bit ICU4 (fetching /measurement)	56	38	ICR40	31C _H	000FFF1C _H	40
Multi-function serial interface ch.11 (transmission completed)						
32-bit ICU5 (fetching /measurement)						
A/D converter	57	39	ICR41	318 _H	000FFF18 _H	41
32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47						
32-bit OCU6/7/10/11 (match)						
32-bit OCU8/9 (match)	58	3A	ICR42	314 _H	000FFF14 _H	42
Base timer 0 IRQ0	60	3C	ICR44	30C _H	000FFF0C _H	44
Base timer 0 IRQ1						
Base timer 1 IRQ0						
Base timer 1 IRQ1	61	3D	ICR45	308 _H	000FFF08 _H	45* ⁵
-						
-						
DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304 _H	000FFF04 _H	-
Delayed interrupt	63	3F	ICR47	300 _H	000FFF00 _H	-
System reserved (Used for REALOS™ ⁹)	64	40	-	2FC _H	000FFEFC _H	-
System reserved (Used for REALOS)	65	41	-	2F8 _H	000FFE8 _H	-
Used with the INT instruction.	66 255	42 FF	-	2F4 _H 000 _H	000FFE4 _H 000FFC00 _H	-

*: It does not support the DMA transfer request by the interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: The status of the multi-function serial interface does not support the DMA transfer by the I2C reception and FlexRay.

*2: The reload timer ch.4 to ch.7 does not support the DMA transfer by the interrupt.

*3: The PPG ch.24 to ch.87 does not support the DMA transfer by the interrupt.

- *4: The clock calibration unit does not support the DMA transfer by the interrupt.
- *5: The 32-bit free-run timer ch.3 to ch.10 does not support the DMA transfer by the interrupt.
- *6: It does not support the DMA transfer by the external low-voltage detection interrupt.
- *7: It does not support the DMA transfer by the FlexRay interrupt.
- *8: It does not support the DMA transfer by the FlexRay timer interrupt.
- *9: REALOS is a trademark of Cypress.

MB91F52xU (176pin)

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Reset	0	0	-	3FC _H	000FFFFC _H	-
System reserved	1	1	-	3F8 _H	000FFFF8 _H	-
System reserved	2	2	-	3F4 _H	000FFFF4 _H	-
System reserved	3	3	-	3F0 _H	000FFFF0 _H	-
System reserved	4	4	-	3EC _H	000FFFE _C	-
FPU exception	5	5	-	3E8 _H	000FFFE8 _H	-
Exception of instruction access protection violation	6	6	-	3E4 _H	000FFFE4 _H	-
Exception of data access protection violation	7	7	-	3E0 _H	000FFFE0 _H	-
Data access error interrupt	8	8	-	3DC _H	000FFFD _C	-
INTE instruction	9	9	-	3D8 _H	000FFFD8 _H	-
Instruction break	10	0A	-	3D4 _H	000FFFD4 _H	-
System reserved	11	0B	-	3D0 _H	000FFFD0 _H	-
System reserved	12	0C	-	3CC _H	000FFFCC _H	-
System reserved	13	0D	-	3C8 _H	000FFFC8 _H	-
Exception of illegal instruction	14	0E	-	3C4 _H	000FFFC4 _H	-
NMI request	15	0F	15(F _H) Fixed	3C0 _H	000FFFC0 _H	-
Error generation at internal bus diagnosis						
XBS RAM double-bit error detection						
Backup RAM double-bit error detection						
AHB RAM double-bit error detection						
TPU violation						
External interrupt 0-7	16	10	ICR00	3BC _H	000FFFBC _H	0
External interrupt 8-15	17	11	ICR01	3B8 _H	000FFFB8 _H	1* ⁶
External low-voltage detection interrupt						
-						
Reload timer 0/1/4/5	18	12	ICR02	3B4 _H	000FFFB4 _H	2* ²
Reload timer 2/3/6/7	19	13	ICR03	3B0 _H	000FFFB0 _H	3* ²
Multi-function serial interface ch.0 (reception completed)	20	14	ICR04	3AC _H	000FFFAC _H	4* ¹
Multi-function serial interface ch.0 (status)						
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	3A8 _H	000FFFA8 _H	5* ¹
Multi-function serial interface ch.1 (reception completed)	22	16	ICR06	3A4 _H	000FFFA4 _H	6* ¹
Multi-function serial interface ch.1 (status)						
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	3A0 _H	000FFFA0 _H	7* ¹
Multi-function serial interface ch.2 (reception completed)	24	18	ICR08	39C _H	000FFF9C _H	8* ¹
Multi-function serial interface ch.2 (status)						

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398 _H	000FFF98 _H	9* ¹
Multi-function serial interface ch.3 (reception completed)	26	1A	ICR10	394 _H	000FFF94 _H	10* ¹
Multi-function serial interface ch.3 (status)						
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390 _H	000FFF90 _H	11
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	38C _H	000FFF8C _H	12* ¹
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388 _H	000FFF88 _H	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384 _H	000FFF84 _H	14* ¹
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380 _H	000FFF80 _H	15* ⁷
FlexRay0						
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	37C _H	000FFF7C _H	16* ¹
Multi-function serial interface ch.6 (status)						
FlexRay1	33	21	ICR17	378 _H	000FFF78 _H	17* ⁸
Multi-function serial interface ch.6 (transmission completed)						
FlexRay timer 0	34	22	ICR18	374 _H	000FFF74 _H	-
CAN0						
CAN3	35	23	ICR19	370 _H	000FFF70 _H	-
FlexRay timer 1						
CAN1						
RAM diagnosis completed						
RAM initialization completed						
Error generation at RAM diagnosis						
Backup RAM diagnosis completed						
Backup RAM initialization completed						
Error generation at Backup RAM diagnosis						
AHB RAM diagnosis completed						
AHB RAM initialization completed						
Error generation at AHB RAM diagnosis						
CAN4						
CAN2	36	24	ICR20	36C _H	000FFF6C _H	-
Up/down counter 0						
Up/down counter 1						
CAN5						
FlexRay PLL gear/FlexRay PLL alarm	37	25	ICR21	368 _H	000FFF68 _H	-
Real time clock						

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Multi-function serial interface ch.7 (reception completed)	38	26	ICR22	364 _H	000FFF64 _H	22* ¹
Multi-function serial interface ch.7 (status)						
16-bit free-run timer 0 ("0" detection) / (compare clear)	39	27	ICR23	360 _H	000FFF60 _H	23
Multi-function serial interface ch.7 (transmission completed)						
PPG0/1/10/11/20/21/30/31/40/41	40	28	ICR24	35C _H	000FFF5C _H	24* ³
16-bit free-run timer 1 ("0" detection) / (compare clear)						
PPG2/3/12/13/22/23/32/33/42/43	41	29	ICR25	358 _H	000FFF58 _H	25* ³
16-bit free-run timer 2 ("0" detection) / (compare clear)						
PPG4/5/14/15/24/25/34/35/44/45	42	2A	ICR26	354 _H	000FFF54 _H	26* ³
PPG6/7/16/17/26/27/36/37/46/47	43	2B	ICR27	350 _H	000FFF50 _H	27* ³
PPG8/9/18/19/28/29/38/39	44	2C	ICR28	34C _H	000FFF4C _H	28* ³
Multi-function serial interface ch.8 (reception completed)	45	2D	ICR29	348 _H	000FFF48 _H	29* ¹
Multi-function serial interface ch.8 (status)						
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)						
Main timer	46	2E	ICR30	344 _H	000FFF44 _H	30
Sub timer						
PLL timer						
Multi-function serial interface ch.8 (transmission completed)						
16-bit ICU 2 (fetching) / 16-bit ICU 3 (fetching)						
Clock calibration unit (Sub oscillation)	47	2F	ICR31	340 _H	000FFF40 _H	31* ¹ * ⁴
Multi-function serial interface ch.9 (reception completed)						
Multi-function serial interface ch.9 (status)						
A/D converter 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16/17/18/19/20/21/22/23/24/25/26/27/28/29/30/31	48	30	ICR32	33C _H	000FFF3C _H	32
Clock calibration unit (CR oscillation)	49	31	ICR33	338 _H	000FFF38 _H	33
Multi-function serial interface ch.9 (transmission completed)						
16-bit OCU 0 (match) / 16-bit OCU 1 (match)						
32-bit free-run timer 4	50	32	ICR34	334 _H	000FFF34 _H	34* ⁵
16-bit OCU 2 (match) / 16-bit OCU 3 (match)						
32-bit free-run timer 3/5	51	33	ICR35	330 _H	000FFF30 _H	35* ⁵
16-bit OCU 4 (match) / 16-bit OCU 5 (match)						
32-bit ICU6 (fetching / measurement)	52	34	ICR36	32C _H	000FFF2C _H	36* ¹
Multi-function serial interface ch.10 (reception completed)						
Multi-function serial interface ch.10 (status)						
32-bit ICU7 (fetching / measurement)	53	35	ICR37	328 _H	000FFF28 _H	37
Multi-function serial interface ch.10 (transmission completed)						

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
32-bit ICU8 (fetching /measurement)	54	36	ICR38	324 _H	000FFF24 _H	38* ¹
Multi-function serial interface ch.11 (reception completed)						
Multi-function serial interface ch.11 (status)						
32-bit ICU9 (fetching /measurement)	55	37	ICR39	320 _H	000FFF20 _H	39
WG dead timer underflow 0 / 1 / 2						
WG dead timer reload 0 / 1 / 2						
WG DTTI 0						
32-bit ICU4 (fetching /measurement)	56	38	ICR40	31C _H	000FFF1C _H	40
Multi-function serial interface ch.11 (transmission completed)						
32-bit ICU5 (fetching /measurement)	57	39	ICR41	318 _H	000FFF18 _H	41
A/D converter						
32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47						
32-bit OCU6/7/10/11 (match)	58	3A	ICR42	314 _H	000FFF14 _H	42
32-bit OCU8/9 (match)	59	3B	ICR43	310 _H	000FFF10 _H	43
Base timer 0 IRQ0	60	3C	ICR44	30C _H	000FFF0C _H	44
Base timer 0 IRQ1						
Base timer 1 IRQ0	61	3D	ICR45	308 _H	000FFF08 _H	45* ⁵
Base timer 1 IRQ1						
-						
-						
DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304 _H	000FFF04 _H	-
Delayed interrupt	63	3F	ICR47	300 _H	000FFF00 _H	-
System reserved (Used for REALOS)	64	40	-	2FC _H	000FFEFC _H	-
System reserved (Used for REALOS)	65	41	-	2F8 _H	000FFE8 _H	-
Used with the INT instruction.	66	42	-	2F4 _H	000FEF4 _H	-
	255	FF		000 _H	000FFC00 _H	

*: It does not support the DMA transfer request by the interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: The status of the multi-function serial interface does not support the DMA transfer by the I²C reception and FlexRay.

*2: The reload timer ch.4 to ch.7 does not support the DMA transfer by the interrupt.

*3: The PPG ch.24 to ch.87 does not support the DMA transfer by the interrupt.

*4: The clock calibration unit does not support the DMA transfer by the interrupt.

*5: The 32-bit free-run timer ch.3 to ch.10 does not support the DMA transfer by the interrupt.

*6: It does not support the DMA transfer by the external low-voltage detection interrupt.

*7: It does not support the DMA transfer by the FlexRay interrupt.

*8: It does not support the DMA transfer by the FlexRay timer interrupt.

MB91F52xM (208pin)

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Reset	0	0	-	3FC _H	000FFFFC _H	-
System reserved	1	1	-	3F8 _H	000FFFF8 _H	-
System reserved	2	2	-	3F4 _H	000FFFF4 _H	-
System reserved	3	3	-	3F0 _H	000FFFF0 _H	-
System reserved	4	4	-	3EC _H	000FFFE _C	-
FPU exception	5	5	-	3E8 _H	000FFFE8 _H	-
Exception of instruction access protection violation	6	6	-	3E4 _H	000FFFE4 _H	-
Exception of data access protection violation	7	7	-	3E0 _H	000FFFE0 _H	-
Data access error interrupt	8	8	-	3DC _H	000FFFD _C	-
INTE instruction	9	9	-	3D8 _H	000FFFD8 _H	-
Instruction break	10	0A	-	3D4 _H	000FFFD4 _H	-
System reserved	11	0B	-	3D0 _H	000FFFD0 _H	-
System reserved	12	0C	-	3CC _H	000FFFCC _H	-
System reserved	13	0D	-	3C8 _H	000FFFC8 _H	-
Exception of illegal instruction	14	0E	-	3C4 _H	000FFFC4 _H	-
NMI request	15	0F	15(F _H) Fixed	3C0 _H	000FFFC0 _H	-
Error generation at internal bus diagnosis						
XBS RAM double-bit error detection						
Backup RAM double-bit error detection						
AHB RAM double-bit error detection						
TPU violation						
External interrupt 0-7	16	10	ICR00	3BC _H	000FFFBC _H	0
External interrupt 8-15	17	11	ICR01	3B8 _H	000FFFB8 _H	1* ⁶
External low-voltage detection interrupt						
External interrupt 16-23	18	12	ICR02	3B4 _H	000FFFB4 _H	2* ²
Reload timer 0/1/4/5						
Reload timer 2/3/6/7	19	13	ICR03	3B0 _H	000FFFB0 _H	3* ²
Multi-function serial interface ch.0 (reception completed)	20	14	ICR04	3AC _H	000FFFAC _H	4* ¹
Multi-function serial interface ch.0 (status)						
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	3A8 _H	000FFFA8 _H	5* ¹
Multi-function serial interface ch.1 (reception completed)	22	16	ICR06	3A4 _H	000FFFA4 _H	6* ¹
Multi-function serial interface ch.1 (status)						
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	3A0 _H	000FFFA0 _H	7* ¹
Multi-function serial interface ch.2 (reception completed)	24	18	ICR08	39C _H	000FFF9C _H	8* ¹
Multi-function serial interface ch.2 (status)						

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398 _H	000FFF98 _H	9* ¹
Multi-function serial interface ch.3 (reception completed)	26	1A	ICR10	394 _H	000FFF94 _H	10* ¹
Multi-function serial interface ch.3 (status)						
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390 _H	000FFF90 _H	11
Multi-function serial interface ch.4/ ch.12 (reception completed)	28	1C	ICR12	38C _H	000FFF8C _H	12* ¹
Multi-function serial interface ch.4/ ch.12 (status)						
Multi-function serial interface ch.4/ ch.12 (transmission completed)	29	1D	ICR13	388 _H	000FFF88 _H	13
Multi-function serial interface ch.5/ ch.13 (reception completed)	30	1E	ICR14	384 _H	000FFF84 _H	14* ¹
Multi-function serial interface ch.5/ ch.13 (status)						
Multi-function serial interface ch.5/ ch.13 (transmission completed)	31	1F	ICR15	380 _H	000FFF80 _H	15* ⁷
FlexRay0						
Multi-function serial interface ch.6/ ch.14 (reception completed)	32	20	ICR16	37C _H	000FFF7C _H	16* ¹
Multi-function serial interface ch.6/ ch.14 (status)						
FlexRay1	33	21	ICR17	378 _H	000FFF78 _H	17* ⁸
Multi-function serial interface ch.6/ ch.14 (transmission completed)						
FlexRay timer 0	34	22	ICR18	374 _H	000FFF74 _H	-
CAN0						
CAN3	35	23	ICR19	370 _H	000FFF70 _H	-
FlexRay timer 1						
CAN1						
RAM diagnosis completed						
RAM initialization completed						
Error generation at RAM diagnosis						
Backup RAM diagnosis completed						
Backup RAM initialization completed						
Error generation at Backup RAM diagnosis						
AHB RAM diagnosis completed						
AHB RAM initialization completed						
Error generation at AHB RAM diagnosis						
CAN4						
CAN2	36	24	ICR20	36C _H	000FFF6C _H	-
Up/down counter 0/2						
Up/down counter 1/3						
CAN5						
FlexRay PLL gear/FlexRay PLL alarm	37	25	ICR21	368 _H	000FFF68 _H	-
Real time clock						

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Multi-function serial interface ch.7/ ch.15 (reception completed)	38	26	ICR22	364 _H	000FFF64 _H	22* ¹
Multi-function serial interface ch.7/ ch.15 (status)						
16-bit free-run timer 0 ("0" detection) / (compare clear)	39	27	ICR23	360 _H	000FFF60 _H	23
Multi-function serial interface ch.7/ ch.15 (transmission completed)						
PPG0/1/10/11/20/21/30/31/40/41/50/51/60/61	40	28	ICR24	35C _H	000FFF5C _H	24* ³
16-bit free-run timer 1 ("0" detection) / (compare clear)						
PPG2/3/12/13/22/23/32/33/42/43/52/53/62/63	41	29	ICR25	358 _H	000FFF58 _H	25* ³
16-bit free-run timer 2 ("0" detection) / (compare clear)						
PPG4/5/14/15/24/25/34/35/44/45/54/55	42	2A	ICR26	354 _H	000FFF54 _H	26* ³
PPG6/7/16/17/26/27/36/37/46/47/56/57	43	2B	ICR27	350 _H	000FFF50 _H	27* ³
PPG8/9/18/19/28/29/38/39/48/49/58/59	44	2C	ICR28	34C _H	000FFF4C _H	28* ³
Multi-function serial interface ch.8/ ch.16 (reception completed)	45	2D	ICR29	348 _H	000FFF48 _H	29* ¹
Multi-function serial interface ch.8/ ch.16 (status)						
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)						
Main timer	46	2E	ICR30	344 _H	000FFF44 _H	30
Sub timer						
PLL timer						
Multi-function serial interface ch.8/ ch.16 (transmission completed)						
16-bit ICU 2 (fetching) / 16-bit ICU 3 (fetching)						
Clock calibration unit (Sub oscillation)	47	2F	ICR31	340 _H	000FFF40 _H	31* ¹ * ⁴
Multi-function serial interface ch.9/ ch.17 (reception completed)						
Multi-function serial interface ch.9/ ch.17 (status)						
A/D converter 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16/17/18/19/20/21/22/23/24/25/26/27/28/29/30/31	48	30	ICR32	33C _H	000FFF3C _H	32
Clock calibration unit (CR oscillation)	49	31	ICR33	338 _H	000FFF38 _H	33
Multi-function serial interface ch.9/ ch.17 (transmission completed)						
16-bit OCU 0 (match) / 16-bit OCU 1 (match)						
32-bit free-run timer 4/6/8/10	50	32	ICR34	334 _H	000FFF34 _H	34* ⁵
16-bit OCU 2 (match) / 16-bit OCU 3 (match)						
32-bit free-run timer 3/5/7/9	51	33	ICR35	330 _H	000FFF30 _H	35* ⁵
16-bit OCU 4 (match) / 16-bit OCU 5 (match)						
32-bit ICU6 (fetching / measurement)	52	34	ICR36	32C _H	000FFF2C _H	36* ¹
Multi-function serial interface ch.10/ ch.18 (reception completed)						
Multi-function serial interface ch.10/ ch.18 (status)						
32-bit ICU7 (fetching / measurement)	53	35	ICR37	328 _H	000FFF28 _H	37
Multi-function serial interface ch.10/ ch.18 (transmission completed)						

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
32-bit ICU8 (fetching /measurement)	54	36	ICR38	324 _H	000FFF24 _H	38* ¹
Multi-function serial interface ch.11/ ch.19 (reception completed)						
Multi-function serial interface ch.11/ ch.19 (status)						
32-bit ICU9 (fetching /measurement)	55	37	ICR39	320 _H	000FFF20 _H	39
WG dead timer underflow 0 / 1/ 2						
WG dead timer reload 0 / 1/ 2						
WG DTTI 0						
32-bit ICU4/10 (fetching /measurement)	56	38	ICR40	31C _H	000FFF1C _H	40
Multi-function serial interface ch.11/ ch.19 (transmission completed)						
32-bit ICU5/11 (fetching /measurement)	57	39	ICR41	318 _H	000FFF18 _H	41
A/D converter						
32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47/48/49/50/51/52/53/54/55/56/57/58/59/60/61/62/63						
32-bit OCU6/7/10/11 (match)	58	3A	ICR42	314 _H	000FFF14 _H	42
32-bit OCU8/9/12/13 (match)	59	3B	ICR43	310 _H	000FFF10 _H	43
Base timer 0 IRQ0	60	3C	ICR44	30C _H	000FFF0C _H	44
Base timer 0 IRQ1						
Base timer 1 IRQ0	61	3D	ICR45	308 _H	000FFF08 _H	45* ⁵
Base timer 1 IRQ1						
-						
-						
DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304 _H	000FFF04 _H	-
Delayed interrupt	63	3F	ICR47	300 _H	000FFF00 _H	-
System reserved (Used for REALOS)	64	40	-	2FC _H	000FFEFC _H	-
System reserved (Used for REALOS)	65	41	-	2F8 _H	000FFE8 _H	-
Used with the INT instruction.	66 255	42 FF	-	2F4 _H 000 _H	000FFE4 _H 000FFC00 _H	-

*: It does not support the DMA transfer request by the interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: The status of the multi-function serial interface does not support the DMA transfer by the I²C reception and FlexRay.

*2: The reload timer ch.4 to ch.7 does not support the DMA transfer by the interrupt.

*3: The PPG ch.24 to ch.87 does not support the DMA transfer by the interrupt.

*4: The clock calibration unit does not support the DMA transfer by the interrupt.

*5: The 32-bit free-run timer ch.3 to ch.10 does not support the DMA transfer by the interrupt.

*6: It does not support the DMA transfer by the external low-voltage detection interrupt.

*7: It does not support the DMA transfer by the FlexRay interrupt.

*8: It does not support the DMA transfer by the FlexRay timer interrupt.

MB91F52xY (416pin)

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Reset	0	0	-	3FC _H	000FFFFC _H	-
System reserved	1	1	-	3F8 _H	000FFFF8 _H	-
System reserved	2	2	-	3F4 _H	000FFFF4 _H	-
System reserved	3	3	-	3F0 _H	000FFFF0 _H	-
System reserved	4	4	-	3EC _H	000FFFE4 _H	-
FPU exception	5	5	-	3E8 _H	000FFFE8 _H	-
Exception of instruction access protection violation	6	6	-	3E4 _H	000FFFE4 _H	-
Exception of data access protection violation	7	7	-	3E0 _H	000FFFE0 _H	-
Data access error interrupt	8	8	-	3DC _H	000FFFD4 _H	-
INTE instruction	9	9	-	3D8 _H	000FFFD8 _H	-
Instruction break	10	0A	-	3D4 _H	000FFFD4 _H	-
System reserved	11	0B	-	3D0 _H	000FFFD0 _H	-
System reserved	12	0C	-	3CC _H	000FFFC4 _H	-
System reserved	13	0D	-	3C8 _H	000FFFC8 _H	-
Exception of illegal instruction	14	0E	-	3C4 _H	000FFFC4 _H	-
NMI request	15	0F	15(F _H) Fixed	3C0 _H	000FFFC0 _H	-
Error generation at internal bus diagnosis						
XBS RAM double-bit error detection						
Backup RAM double-bit error detection						
AHB RAM double-bit error detection						
TPU violation						
External interrupt 0-7	16	10	ICR00	3BC _H	000FFFB4 _H	0
External interrupt 8-15	17	11	ICR01	3B8 _H	000FFFB8 _H	1* ⁶
External low-voltage detection interrupt						
External interrupt 16-23	18	12	ICR02	3B4 _H	000FFFB4 _H	2* ²
Reload timer 0/1/4/5						
Reload timer 2/3/6/7	19	13	ICR03	3B0 _H	000FFFB0 _H	3* ²
Multi-function serial interface ch.0 (reception completed)	20	14	ICR04	3AC _H	000FFFA4 _H	4* ¹
Multi-function serial interface ch.0 (status)						
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	3A8 _H	000FFFA8 _H	5* ¹
Multi-function serial interface ch.1 (reception completed)	22	16	ICR06	3A4 _H	000FFFA4 _H	6* ¹
Multi-function serial interface ch.1 (status)						
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	3A0 _H	000FFFA0 _H	7* ¹
Multi-function serial interface ch.2 (reception completed)	24	18	ICR08	39C _H	000FFF9C _H	8* ¹
Multi-function serial interface ch.2 (status)						

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398 _H	000FFF98 _H	9* ¹
Multi-function serial interface ch.3 (reception completed)	26	1A	ICR10	394 _H	000FFF94 _H	10* ¹
Multi-function serial interface ch.3 (status)						
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390 _H	000FFF90 _H	11
Multi-function serial interface ch.4/ ch.12 (reception completed)	28	1C	ICR12	38C _H	000FFF8C _H	12* ¹
Multi-function serial interface ch.4/ ch.12 (status)						
Multi-function serial interface ch.4/ ch.12 (transmission completed)	29	1D	ICR13	388 _H	000FFF88 _H	13
Multi-function serial interface ch.5/ ch.13 (reception completed)	30	1E	ICR14	384 _H	000FFF84 _H	14* ¹
Multi-function serial interface ch.5/ ch.13 (status)						
Multi-function serial interface ch.5/ ch.13 (transmission completed)	31	1F	ICR15	380 _H	000FFF80 _H	15* ⁷
FlexRay0						
Multi-function serial interface ch.6/ ch.14 (reception completed)	32	20	ICR16	37C _H	000FFF7C _H	16* ¹
Multi-function serial interface ch.6/ ch.14 (status)						
FlexRay1	33	21	ICR17	378 _H	000FFF78 _H	17* ⁸
Multi-function serial interface ch.6/ ch.14 (transmission completed)						
FlexRay timer 0	34	22	ICR18	374 _H	000FFF74 _H	-
CAN0						
CAN3	35	23	ICR19	370 _H	000FFF70 _H	-
FlexRay timer 1						
CAN1						
RAM diagnosis completed						
RAM initialization completed						
Error generation at RAM diagnosis						
Backup RAM diagnosis completed						
Backup RAM initialization completed						
Error generation at Backup RAM diagnosis						
AHB RAM diagnosis completed						
AHB RAM initialization completed						
Error generation at AHB RAM diagnosis						
CAN4	36	24	ICR20	36C _H	000FFF6C _H	-
CAN2						
Up/down counter 0/2						
Up/down counter 1/3						
CAN5						
FlexRay PLL gear/FlexRay PLL alarm	37	25	ICR21	368 _H	000FFF68 _H	-
Real time clock						

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
Multi-function serial interface ch.7/ ch.15 (reception completed)	38	26	ICR22	364 _H	000FFF64 _H	22* ¹
Multi-function serial interface ch.7/ ch.15 (status)						
16-bit free-run timer 0 ("0" detection) / (compare clear)	39	27	ICR23	360 _H	000FFF60 _H	23
Multi-function serial interface ch.7/ ch.15 (transmission completed)						
PPG 0/1/10/11/20/21/30/31/40/41/50/51/60/61/70/71/80/81	40	28	ICR24	35C _H	000FFF5C _H	24* ³
16-bit free-run timer 1 ("0" detection) / (compare clear)						
PPG 2/3/12/13/22/23/32/33/42/43/52/53/62/63/72/73/82/83	41	29	ICR25	358 _H	000FFF58 _H	25* ³
16-bit free-run timer 2 ("0" detection) / (compare clear)						
PPG 4/5/14/15/24/25/34/35/44/45/54/55/64/65/74/75/84/85	42	2A	ICR26	354 _H	000FFF54 _H	26* ³
PPG 6/7/16/17/26/27/36/37/46/47/56/57/66/67/76/77/86/87	43	2B	ICR27	350 _H	000FFF50 _H	27* ³
PPG 8/9/18/19/28/29/38/39/48/49/58/59/68/69/78/79	44	2C	ICR28	34C _H	000FFF4C _H	28* ³
Multi-function serial interface ch.8/ ch.16 (reception completed)	45	2D	ICR29	348 _H	000FFF48 _H	29* ¹
Multi-function serial interface ch.8/ ch.16 (status)						
16-bit ICU 0 (fetching) / 16-bit ICU 1 (fetching)						
Main timer	46	2E	ICR30	344 _H	000FFF44 _H	30
Sub timer						
PLL timer						
Multi-function serial interface ch.8/ ch.16 (transmission completed)						
16-bit ICU 2 (fetching) / 16-bit ICU 3 (fetching)	47	2F	ICR31	340 _H	000FFF40 _H	31* ¹ * ⁴
Clock calibration unit (Sub oscillation)						
Multi-function serial interface ch.9/ ch.17 (reception completed)						
Multi-function serial interface ch.9/ ch.17 (status)	48	30	ICR32	33C _H	000FFF3C _H	32
A/D converter 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16/17/18/19/20/21/22/23/24/25/26/27/28/29/30/31						
Clock calibration unit (CR oscillation)	49	31	ICR33	338 _H	000FFF38 _H	33
Multi-function serial interface ch.9/ ch.17 (transmission completed)						
16-bit OCU 0 (match) / 16-bit OCU 1 (match)						
32-bit free-run timer 4/6/8/10	50	32	ICR34	334 _H	000FFF34 _H	34* ⁵
16-bit OCU 2 (match) / 16-bit OCU 3 (match)						
32-bit free-run timer 3/5/7/9	51	33	ICR35	330 _H	000FFF30 _H	35* ⁵
16-bit OCU 4 (match) / 16-bit OCU 5 (match)						
32-bit ICU6 (fetching /measurement)	52	34	ICR36	32C _H	000FFF2C _H	36* ¹
Multi-function serial interface ch.10/ ch.18 (reception completed)						
Multi-function serial interface ch.10/ ch.18 (status)						
32-bit ICU7 (fetching /measurement)	53	35	ICR37	328 _H	000FFF28 _H	37
Multi-function serial interface ch.10/ ch.18 (transmission completed)						

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN *
	Decimal	Hexa-decimal				
32-bit ICU8 (fetching /measurement)	54	36	ICR38	324 _H	000FFF24 _H	38* ¹
Multi-function serial interface ch.11/ ch.19 (reception completed)						
Multi-function serial interface ch.11/ ch.19 (status)						
32-bit ICU9 (fetching /measurement)	55	37	ICR39	320 _H	000FFF20 _H	39
WG dead timer underflow 0 / 1/ 2						
WG dead timer reload 0 / 1/ 2						
WG DTTI 0	56	38	ICR40	31C _H	000FFF1C _H	40
32-bit ICU4/10 (fetching /measurement)						
Multi-function serial interface ch.11/ ch.19 (transmission completed)						
32-bit ICU5/11 (fetching /measurement)	57	39	ICR41	318 _H	000FFF18 _H	41
A/D converter						
32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47/48/49/50/51/52/53/54/55/56/57/58/59/60/61/62/63						
32-bit OCU6/7/10/11 (match)	58	3A	ICR42	314 _H	000FFF14 _H	42
32-bit OCU8/9/12/13 (match)	59	3B	ICR43	310 _H	000FFF10 _H	43
Base timer 0 IRQ0	60	3C	ICR44	30C _H	000FFF0C _H	44
Base timer 0 IRQ1						
Base timer 1 IRQ0						
Base timer 1 IRQ1	61	3D	ICR45	308 _H	000FFF08 _H	45* ⁵
-						
-						
DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304 _H	000FFF04 _H	-
Delayed interrupt	63	3F	ICR47	300 _H	000FFF00 _H	-
System reserved (Used for REALOS)	64	40	-	2FC _H	000FFEFC _H	-
System reserved (Used for REALOS)	65	41	-	2F8 _H	000FFE8 _H	-
Used with the INT instruction.	66 255	42 FF	-	2F4 _H 000 _H	000FFE4 _H 000FFC00 _H	-

*: It does not support the DMA transfer request by the interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*1: The status of the multi-function serial interface does not support the DMA transfer by the I²C reception and FlexRay.

*2: The reload timer ch.4 to ch.7 does not support the DMA transfer by the interrupt.

*3: The PPG ch.24 to ch.87 does not support the DMA transfer by the interrupt.

*4: The clock calibration unit does not support the DMA transfer by the interrupt.

*5: The 32-bit free-run timer ch.3 to ch.10 does not support the DMA transfer by the interrupt.

*6: It does not support the DMA transfer by the external low-voltage detection interrupt.

*7: It does not support the DMA transfer by the FlexRay interrupt.

*8: It does not support the DMA transfer by the FlexRay timer interrupt.

11. Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage *1,*2	V_{CC}	$V_{SS}-0.3$	$V_{SS}+6.0$	V	
	V_{CCE}	$V_{SS}-0.3$	V_{CC}	V	
Analog power supply voltage *1,*2	AV_{CC}	$V_{SS}-0.3$	$V_{SS}+6.0$	V	$AVRH \leq AV_{CC} \leq V_{CC}$
Analog reference voltage *1	$AVRH$	$V_{SS}-0.3$	$V_{SS}+6.0$	V	$AVRH \leq AV_{CC}$
Input voltage *1	V_I	$V_{SS}-0.3$	$V_{CC}+0.3$	V	When V_{CCE} pin is a power supply *9
		$V_{SS}-0.3$	$V_{CCE}+0.3$		
Analog pin input voltage *1	V_{IA5}	$V_{SS}-0.3$	$V_{CC}+0.3$	V	
		$V_{SS}-0.3$	$V_{CCE}+0.3$	V	When V_{CCE} pin is a power supply *9
Output voltage *1	V_O	$V_{SS}-0.3$	$V_{CC}+0.3$	V	
Maximum clamp current	I_{CLAMP}	-	4.0	mA	*6
Total maximum clamp current	$\sum I_{CLAMP} $	-	20	mA	*6
"L" level maximum output current *3	I_{OL1}	-	15	mA	
	I_{OL2}	-	30	mA	
"L" level average output current *4	I_{OLAV1}	-	4	mA	*13
	I_{OLAV2}	-	12	mA	*14
"L" level total output current *5	$\sum I_{OL1}$	-	100	mA	
	$\sum I_{OL2}$	-	120	mA	
"H" level maximum output current*3	I_{OH1}	-	-15	mA	
	I_{OH2}	-	-30	mA	
"H" level average output current*4	I_{OHAV1}	-	-4	mA	*13
	I_{OHAV2}	-	-12	mA	*14
"H" level total output current *5	$\sum I_{OH1}$	-	-100	mA	
	$\sum I_{OH2}$	-	-120	mA	
Power consumption	$T_A: -40^\circ\text{C to } +105^\circ\text{C}$	P_D	-	990	mW *8
			-	990	mW *8, *10
			-	780	mW *8, *12
			-	755	mW *8, *11
Operating temperature	T_A	-40	+105	$^\circ\text{C}$	
		-40	+125	$^\circ\text{C}$	*7
Storage temperature	T_{stg}	-55	+150	$^\circ\text{C}$	

*1: These parameters are based on the condition that $V_{SS}=AV_{SS}=0.0V$

*2: Caution must be taken that AV_{CC} , $AVRH$ and V_{CCE} do not exceed V_{CC} upon power-on and under other circumstances.

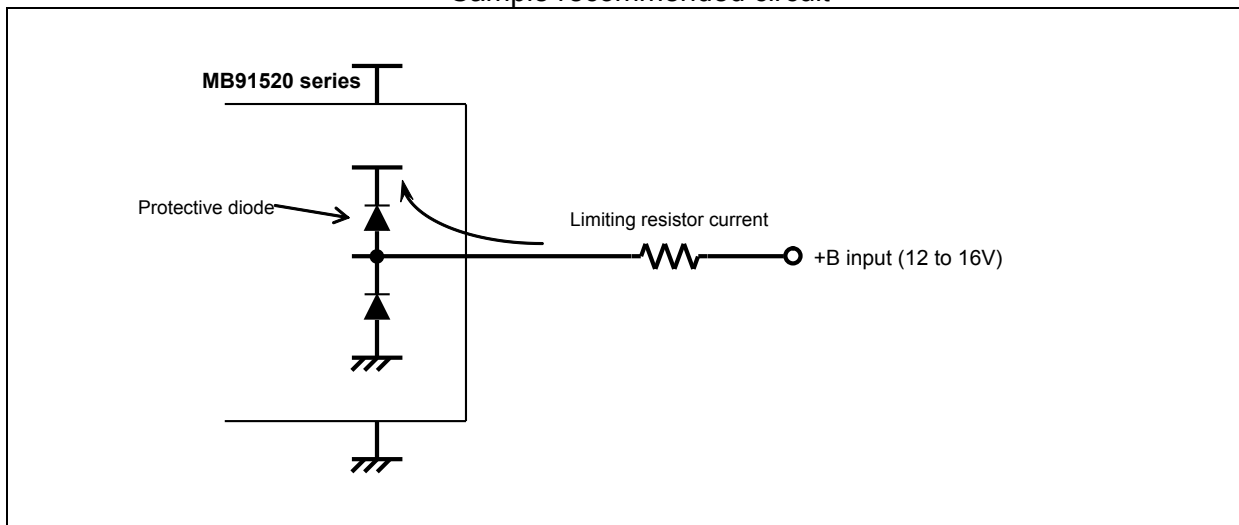
*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current \times the operation ratio.

*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

- *6: Corresponding pins: all general-purpose ports except P035, 041, 093, 122, P222, P227, P232 and P236.
- Use within recommended operating conditions.
 - Use at DC voltage (current).
 - The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.
 - The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.
 - Note that when the microcontroller drive current is low, such as in the low power consumption modes, the + B input potential can increase the potential at the V_{CC} pin via a protective diode, possibly affecting other devices.
 - Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
 - Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
 - Do not leave + B input pins open.
- *7: When it is used under this condition, contact your sales representative.
- *8: It is a standard when four-layer substrate is used.
- *9: Please see to the item of "Product lineup" for details.
- *10: It is a condition that can be used by limiting the product type of LES144, LEP176, LER208, and PAB416.
- *11: It is a condition that can be used by the package limitation of LQS144 and LQP176.
- *12: It is a condition that can be used by limiting the package of LQR208.
- *13: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106.
- *14: Corresponding pins: General-purpose ports of P103, P104, P105 and P106.

Sample recommended circuit



<WARNING>

Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

12. Recommended Operating Conditions

($V_{SS}=AV_{SS}=0.0V$)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	4.5	5.5	V	Recommended operation guarantee range (When 5.0V is used)
	V_{CCE}	3.0	3.6	V	Recommended operation guarantee range (When 3.3V is used)
	AV_{CC}	2.7	5.5	V	Operation guarantee range ^{*1}
Smoothing capacitor ^{*2}	C_S	4.7 (tolerance within $\pm 50\%$)		μF	Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than C_S as the smoothing capacitor on the VCC pin.
Operating temperature	T_A	-40	+105	°C	
		-40	+125	°C	*3

*1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative.

The initial detection voltage of the external low voltage detection is $2.8V \pm 8\%$ (2.576V to 3.024V).

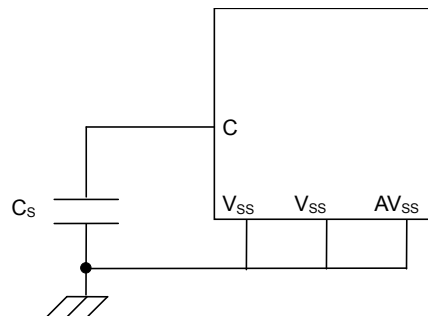
This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.

Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

*2: See the following diagram for details on the connection of smoothing capacitor C_S .

*3: When it is used under this condition, contact your sales representative.

·C Pin Connection Diagram



<WARNING>

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

13. DC Characteristics

(T_A: -40°C to +105°C, V_{CC}= AV_{CC}=5.0V±10%/ V_{CC}= AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I _{CC5}	VCC	Operating frequency F _{CP} =128MHz, F _{cpp} =32MHz, * ³ at normal operation	-	85	122	mA	
			Operating frequency F _{CP} =128MHz, F _{cpp} =32MHz, * ³ at Flash write * ²	-	95	135	mA	
			Operating frequency F _{CP} =128MHz, F _{cpp} =32MHz, * ³ at Flash erase * ²	-	95	135	mA	
			Operating frequency F _{CP} =80MHz, F _{cpp} =40MHz, at normal operation	-	80	117	mA	
			Operating frequency F _{CP} =80MHz, F _{cpp} =40MHz, at Flash write * ²	-	90	130	mA	
			Operating frequency F _{CP} =80MHz, F _{cpp} =40MHz, at Flash erase * ²	-	90	130	mA	
			Operating frequency F _{CP} =64MHz, F _{cpp} =32MHz, at normal operation	-	73	110	mA	
			Operating frequency F _{CP} =64MHz, F _{cpp} =32MHz, at Flash write * ²	-	83	123	mA	
			Operating frequency F _{CP} =64MHz, F _{cpp} =32MHz, at Flash erase * ²	-	83	123	mA	
			Operating frequency F _{CP} =48MHz, F _{cpp} =24MHz, at normal operation	-	53	100	mA	
			Operating frequency F _{CP} =48MHz, F _{cpp} =24MHz, at Flash write * ²	-	63	113	mA	
			Operating frequency F _{CP} =48MHz, F _{cpp} =24MHz, at Flash erase * ²	-	63	113	mA	
	I _{CCS5}		Operating frequency F _{CP} =80MHz, F _{cpp} =40MHz, at CPU sleep mode	-	57	94	mA	
	I _{CCBS5}		Operating frequency F _{CP} =80MHz, F _{cpp} =40MHz, at bus sleep mode	-	39	79	mA	
	I _{CC5}	Watch mode	When using crystal 4MHz T _A =+25°C* ¹	-	2000	3600	μA	
			When using built-in CR clock 50kHz, T _A =+25°C* ¹	-	640	2440		
			When using sub clock 32kHz, T _A =+25°C* ¹	-	660	2460		
	I _{CC5}	Stop mode	T _A =+25°C* ¹	-	640	2440	μA	

Parameter	Symbol	Pin name	Conditions		Value			Unit	Remarks
					Min	Typ	Max		
Power supply current	I _{CCT} 52	VCC	Watch mode (power off)	When using crystal 4MHz T _A =+25°C ^{*1}	-	1400	1600	μA	LVD/ RTC operation, Backup RAM 16KB retention
				When using built-in CR clock 50kHz , T _A =+25°C ^{*1}	-	63	203		
				When using sub clock 32kHz T _A =+25°C ^{*1}	-	80	220		
	I _{CCH} 52		Stop mode (power off)	T _A =+25°C ^{*1}	-	60	200	μA	Backup RAM 16KB retention

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.5V±10%/ V_{CC}= AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I _{CC5}	VCC	Operating frequency F _{CP} =128MHz, F _{cpp} =32MHz, * ³ at normal operation	-	85	122	mA	
			Operating frequency F _{CP} =128MHz, F _{cpp} =32MHz, * ³ at Flash write * ²	-	95	135	mA	
			Operating frequency F _{CP} =128MHz, F _{cpp} =32MHz, * ³ at Flash erase * ²	-	95	135	mA	
			Operating frequency F _{CP} =80MHz, F _{cpp} =40MHz, at normal operation	-	80	117	mA	
			Operating frequency F _{CP} =80MHz, F _{cpp} =40MHz, at Flash write * ²	-	90	130	mA	
			Operating frequency F _{CP} =80MHz, F _{cpp} =40MHz, at Flash erase * ²	-	90	130	mA	
			Operating frequency F _{CP} =64MHz, F _{cpp} =32MHz, at normal operation	-	73	110	mA	
			Operating frequency F _{CP} =64MHz, F _{cpp} =32MHz, at Flash write * ²	-	83	123	mA	
			Operating frequency F _{CP} =64MHz, F _{cpp} =32MHz, at Flash erase * ²	-	83	123	mA	
			Operating frequency F _{CP} =48MHz, F _{cpp} =24MHz, at normal operation	-	53	100	mA	
			Operating frequency F _{CP} =48MHz, F _{cpp} =24MHz, at Flash write * ²	-	63	113	mA	
			Operating frequency F _{CP} =48MHz, F _{cpp} =24MHz, at Flash erase * ²	-	63	113	mA	
	I _{CCS5}		Operating frequency F _{CP} =80MHz, F _{cpp} =40MHz, at CPU sleep mode	-	57	94	mA	
	I _{CCBS5}		Operating frequency F _{CP} =80MHz, F _{cpp} =40MHz, at bus sleep mode	-	39	79	mA	
	I _{CCT5}	Watch mode	When using crystal 4MHz T _A =+25°C* ¹	-	2000	3600	μA	
			When using built-in CR clock 50kHz T _A =+25°C* ¹	-	640	2440		
			When using sub clock 32kHz T _A =+25°C* ¹	-	660	2460		
	I _{CCH5}	Stop mode	T _A =+25°C* ¹	-	640	2440	μA	

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I _{CCT52}	VCC	Watch mode (power off)				μA	LVD/ RTC operation, Backup RAM 16KB retention
			When using crystal 4MHz T _A =+25°C ^{*1}	-	1400	1600		
			When using built-in CR clock 50kHz, T _A =+25°C ^{*1}	-	63	203		
			When using sub clock 32kHz T _A =+25°C ^{*1}	-	80	220		
	I _{CCH52}		Stop mode (power off)				μA	Backup RAM 16KB retention
			T _A =+25°C ^{*1}	-	60	200		

*1: It is a standard in BRAMSC (Backup RAM sleep control bit)=1(Enter the state of the sleep at the standby mode) condition.

*2: It is a prohibition two flash or more writing/erasing the flash and the WorkFlash for the internally stored program at the same time.

*3: There is a frequency limitation by the product type. Please see "4. AC Characteristics" for details.

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I _{IL}	All input pins	V _{CC} =AV _{CC} =5.5V V _{SS} <V _I <V _{CC}	-5	-	5	μA	
Input capacitance 1	C _{IN1}	Other than VCC, VCCE, VSS, AVCC, AVSS, C	-	-	5	15	pF	
Pull-up resistance	R _{UP1}	RSTX, NMIX	V _{CC} =5.0V±10 %	25	-	100	kΩ	
			V _{CC} =3.3V±0.3 V	45	-	140		
	R _{UP2}	P073,074,077	V _{CC} =5.0V±10 %	25	-	60	kΩ	
			V _{CC} =3.3V±0.3 V	33	-	90		
	R _{UP3}	Port pin other than P035,041,073,074,077, 093, 122,222,227, 232,236	V _{CC} =5.0V±10 %	25	-	100	kΩ	
			V _{CC} =3.3V±0.3 V	45	-	140		
“H” level output voltage *1	V _{OH1}	Normal output pin	V _{CC} =4.5V I _{OH} =-4.0mA	V _{CC} -0.5	-	V _{CC}	V	
			V _{CC} =3.0V I _{OH} =-2.0mA					
		P076,200,201, 204,205,210, 211,214,215, 220,221,225, 226,230,231, 234,235	V _{CC} =4.5V I _{OH} =-4.0mA	V _{CC} -0.5	-	V _{CC}	V	When I ² C function is non-selected
			V _{CC} =3.0V I _{OH} =-2.0mA					
	V _{OH2}	P073,074,077	V _{CC} =4.5V I _{OH} =-3.0mA	V _{CC} -0.5	-	V _{CC}	V	I ² C pin output
		P076,200,201, 204,205,210, 211,214,215, 220,221,225, 226,230,231, 234,235	V _{CC} =4.5V I _{OH} =-3.0mA	V _{CC} -0.5	-	V _{CC}	V	When I ² C function is non-selected
			V _{CC} =4.5V I _{OH} =-12.0mA	V _{CC} -0.5	-	V _{CC}	V	
	V _{OH3}	P103 to 106	V _{CC} =3.0V I _{OH} =-8.0mA					

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
“L” level output voltage	V _{OL1}	Normal output pin	V _{CC} =4.5V I _{OL} =4.0mA	0	-	0.4	V	
			V _{CC} =3.0V I _{OL} =2.0mA					
		P076,200,201, 204,205,210, 211,214,215, 220,221,225, 226,230,231, 234,235	V _{CC} =4.5V I _{OL} =4.0mA	0	-	0.4	V	When I ² C function is non-selected
			V _{CC} =3.0V I _{OL} =2.0mA					
	V _{OL2}	P073,074,077	V _{CC} =4.5V I _{OL} =3.0mA	0	-	0.4	V	I ² C pin output
		P076,200,201, 204,205,210, 211,214,215, 220,221,225, 226,230,231, 234,235	V _{CC} =4.5V I _{OH} =-3.0mA	0	-	0.4	V	When I ² C function is non-selected
“H” level input voltage *1	V _{IH1}	P000,002,003, 005,020,022, 024,026,035, 041,045,055, 057,071-077, 081,082,093, 096,097, 100-102, 111,115,116, 122,126,130, 134,150,151, 153,200-202, 204-206, 210-212, 214-216, 220-222, 225-227, 230-232, 234-236, TCK, TDI, TMS, TRST	CMOS hysteresis input level	0.7× V _{CC}	-	V _{CC}	V	
	V _{IH2}	P001,004,006, 007,010-017, 052,114,120, 123,155	CMOS hysteresis input level	0.7× V _{CC}	-	V _{CC}	V	
	V _{IH3}		Automotive input level	0.8× V _{CC}	-	V _{CC}	V	
	V _{IH4}	Port other than V _{IH1} , V _{IH2} , V _{IH3}	Automotive input level	0.8× V _{CC}	-	V _{CC}	V	
	V _{IH5}	RSTX, NMIX, MD0, MD1	CMOS hysteresis input level	0.8× V _{CC}	-	V _{CC}	V	
	V _{IHT}	DEBUGIF	TTL input level	2	-	V _{CC}	V	

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
“L” level input voltage*1	V_{IL1}	P000,002,003, 005,020,022, 024,026,035, 041,045,055, 057,071-077, 081,082,093, 096,097, 100-102,111, 115,116,122, 126,130,134, 150,151,153, 200-202, 204-206, 210-212, 214-216, 220-222, 225-227, 230-232, 234-236, TCK, TDI, TMS, TRST	CMOS hysteresis input level	V_{SS}	-	$0.3 \times V_{CC}$	V	
	V_{IL2}	P001,004,006, 007,010-017, 052,114,120, 123,155	CMOS hysteresis input level	V_{SS}	-	$0.3 \times V_{CC}$	V	
	V_{IL3}		Automotive input level	V_{SS}	-	$0.5 \times V_{CC}$	V	
	V_{IL4}	Port other than $V_{IH1}, V_{IH2}, V_{IH3}$	Automotive input level	V_{SS}	-	$0.5 \times V_{CC}$	V	
	V_{IL5}	RSTX,NMIX,MD0,MD1	CMOS hysteresis input level	V_{SS}	-	$0.2 \times V_{CC}$	V	
	V_{ILT}	DEBUGIF	TTL input level	V_{SS}	-	0.8	V	

*1: It is provided by V_{CCE} for the pin corresponding to the V_{CCE} power supply instead of V_{CC} . Please see "PRODUCT LINEUP" for details.

14. AC Characteristics

(1) Main Clock Timing

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F _C	X0, X1	-	-	4	16	MHz	
Source oscillation clock cycle time	t _{CYL}	X0, X1		62.5	250	-	ns	
Internal operating clock frequency ^{*1}	F _{CP}	-		2	-	128	MHz	CPU clock ^{*3}
	F _{CPP}			1		40		Peripheral bus clock
	F _{CPT}			1		40		External bus clock (When V _{CC} =5.0V is used) ^{*2}
				1		32		External bus clock (When V _{CC} =3.3V is used)
Internal operating clock cycle time ^{*1}	t _{CP}	-		7.82	-	500	ns	CPU clock ^{*4}
	t _{CPP}			25		1000		Peripheral bus clock
	t _{CPT}			25		1000		External bus clock (When V _{CC} =5.0V is used)
				31.25		1000		External bus clock (When V _{CC} =3.3V is used)
CAN PLL jitter (during lock)	t _{PJ}	-		-10	-	10	ns	F _{CP} =80MHz (4MHz×Multiplied by 20)
Built-in CR oscillation frequency	F _{CCR}	-		50	100	150	kHz	

*1: The maximum / minimum value is defined when using the main clock and PLL clock.

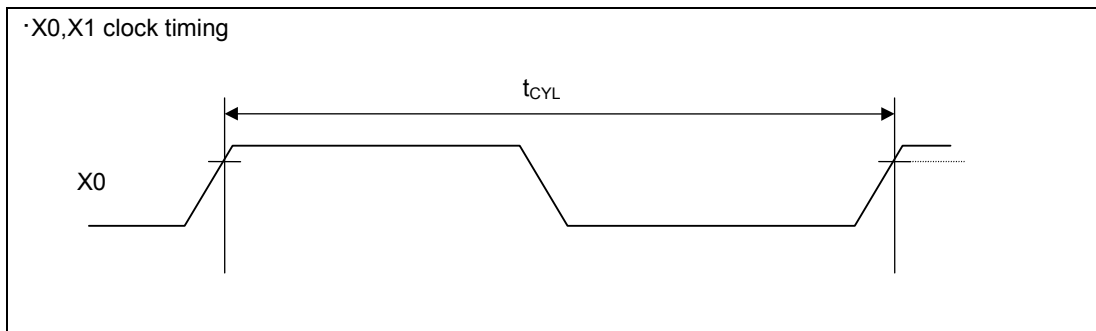
*2: Please use it with external load capacity 12pF or less for V_{CC}=3.3V±0.3V (40MHz operation).

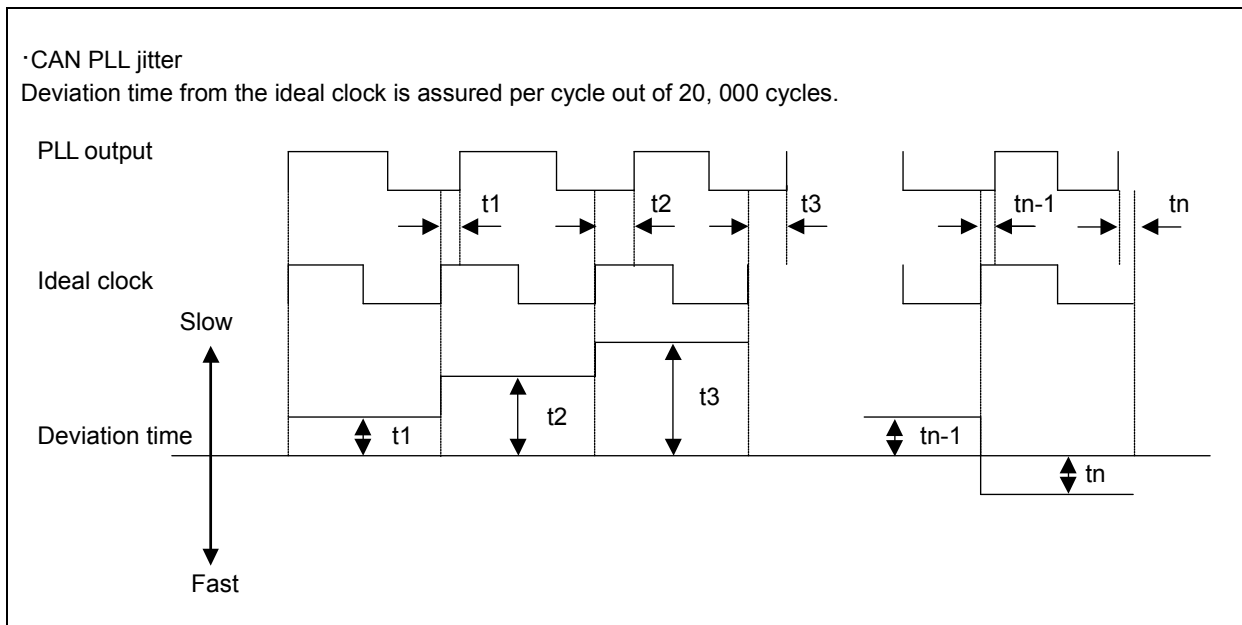
*3: MB91F52xR/MB91F52xU(LQS144/LQN144/LQP176) is 80MHz or less.

MB91F52xR/MB91F52xU(LES144/LEP176) and MB91F52xM/MB91F52xY is 128MHz or less.

*4: MB91F52xR/MB91F52xU(LQS144/LQN144/LQP176) is 12.5ns or more.

MB91F52xR/MB91F52xU(LES144/LEP176) and MB91F52xM/MB91F52xY is 7.82ns or more.

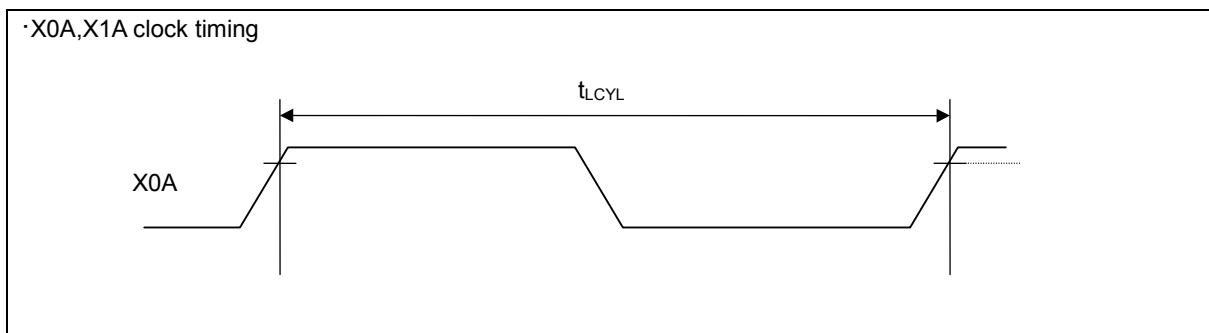




(1-2) Sub clock timing

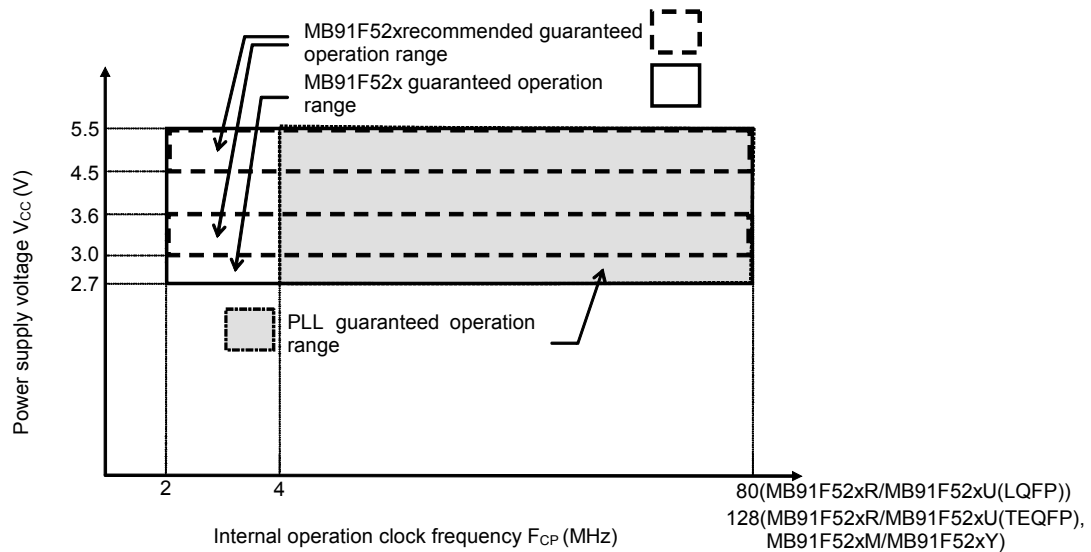
(T_A : -40°C to +125°C, $V_{CC}=AV_{CC}=5.0V \pm 10\%$, $V_{CC}=AV_{CC}=3.3V \pm 0.3V$, $V_{SS}=AV_{SS}=0.0V$)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_{CL}	X0A, X1A	-	-	32.768	-	kHz	
Source oscillation clock cycle time	t_{LCYL}	X0A, X1A		-	30.52	-	μs	



· Guaranteed operation range

Internal operation clock frequency vs. Power supply voltage

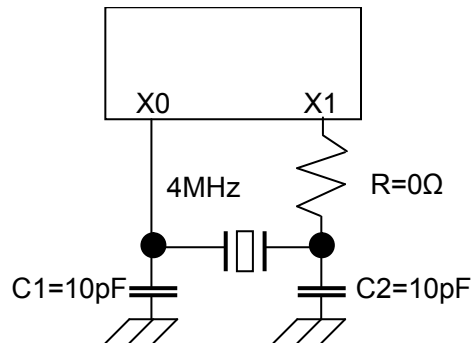


Note: The power supply voltage, which is the low-voltage detection setting voltage or lower, is in the reset state.

Oscillation clock frequency vs. Internal operation clock frequency

		Internal operation clock frequency							
		Main Clock	PLL clock						
			Multiplied by 1	Multiplied by 2	Multiplied by 3	Multiplied by 4	...	Multiplied by 31	Multiplied by 32
Oscillation clock frequency	4MHz	2MHz	4MHz	8MHz	12MHz	16MHz	...	124MHz	128MHz

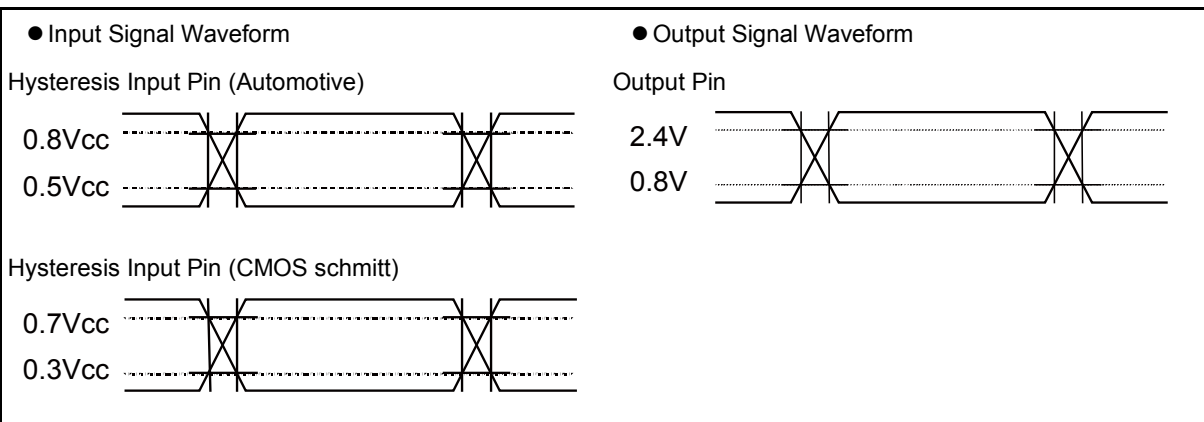
·Example of oscillation circuit



Note: As to the product with its clock supervisor's initial value is "ON", when the oscillator is unable to start within 20ms from the stop state the clock supervisor will detect the oscillation stop. As a result, the CPU moves to the fail safe operation.

Design your print circuit board so that the oscillator can start oscillation within 20ms. Moreover, it is recommended to be designed after the match evaluation of the circuit is requested to the departure pendulum maker when the oscillation circuit is composed.

AC characteristics are specified by the following measurement reference voltage values.



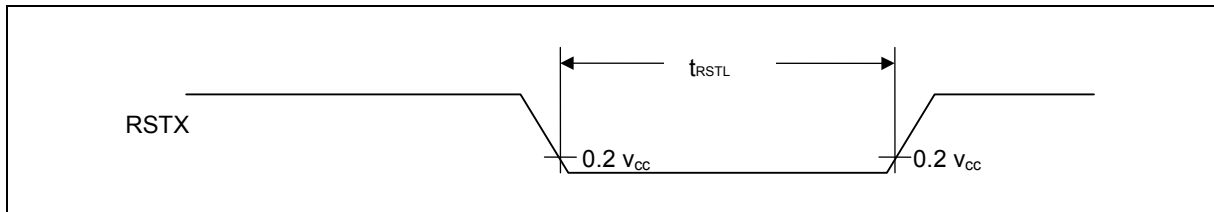
(2) Reset Input

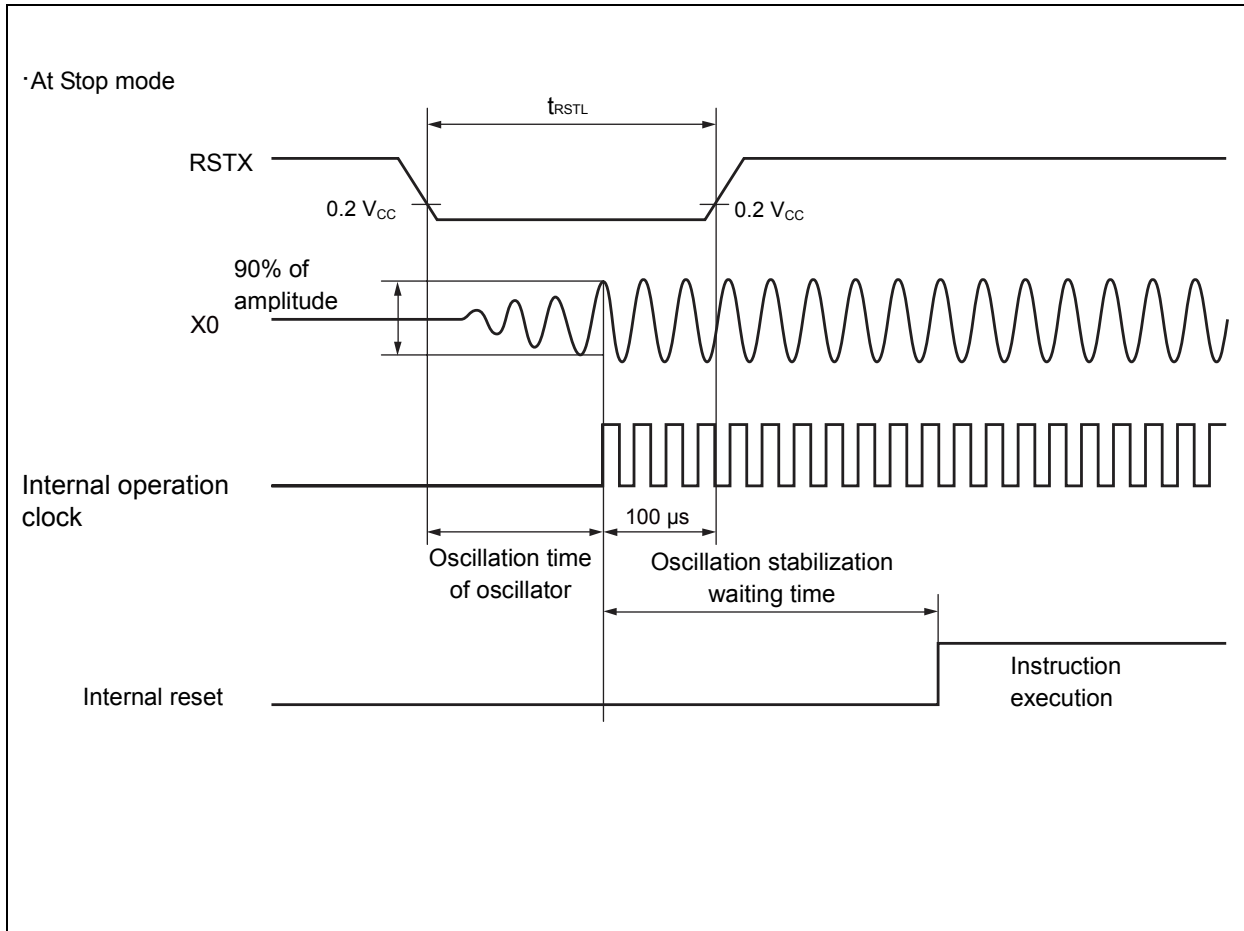
(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t _{RSTL}	RSTX	—	10	—	μs	When normal operation
				Oscillation time of oscillator* +100	—	μs	At Stop mode At Power-on ^{*2}
				100	—	μs	At Watch mode
Width for reset input removal				1	—	μs	

*1: The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred μs and several ms, and for an external clock, the time is 0 ms.

*2: In case of using MB91F52xxxD or MB91F52xxxE and corresponding to note in (3) Power-on Conditions of next subsection, assert RSTX with power-on.





(3) Power-on Conditions

(3-1) [MB9152xxxC/MB9152xxxD]

(T_A: -40°C to +125°C, V_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	—	V _{CC}	—	2.024	2.2	2.376	V	
Level detection hysteresis width	—	V _{CC}	—	—	100	—	mV	
Level detection time	—	—	—	—	—	30	μs	*1
Power off time	t _{OFF}	V _{CC}	—	50	—	—	ms	*2
Power ramp rate	dV/dt	V _{CC}	V _{CC} : 0.2V to 2.376V	—	—	4	mV/μs	*3
C pin voltage at Power-on	—	C	—	—	—	60	mV	*4

*1: This spec is at 4mV/μs of power ramp rate. If the power ramp rate is faster than 4mV/μs, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: V_{CC} must be held below 0.2V for a minimum period of t_{OFF}.

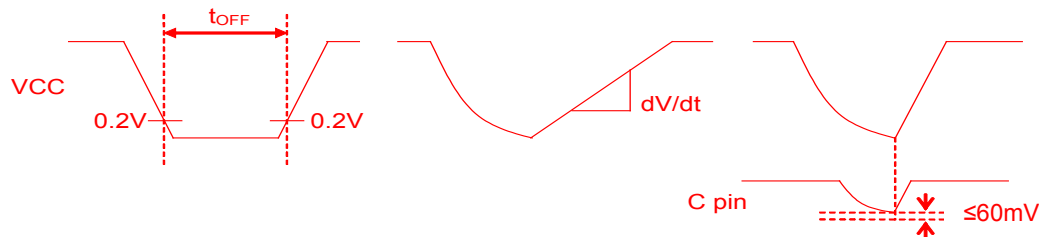
*3: Power-on can detect by satisfying power ramp rate when power off time is not satisfied.

*4: C-pin voltage is below 60 mV when V_{CC} is turned on again.

Note:

When using MB91F52xxxB/C, either *2 or *3 or *4 must be satisfied. When neither *2 nor *3 nor *4 can be satisfied, use MB91F52xxxD and assert external reset (RSTX) at power-up and at any brownout event.

• Power off time, Power ramp rate, C pin voltage at Power-on



(3-2) [MB9152xxxE]

(T_A: -40°C to +125°C, V_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	—	V _{CC}	—	2.024	2.2	2.376	V	
Level detection hysteresis width	—	V _{CC}	—	—	100	—	mV	
Level detection time	—	—	—	—	—	30	μs	*1
Power off time	t _{OFF1}	V _{CC}	V _{CC} ≤ 0.2V	50	—	—	ms	*2
	t _{OFF2}	V _{CC}	V _{CC} ≤ 1.3V	100	—	—	μs	*4
Power ramp rate	dV/dt	V _{CC}	V _{CC} : 0.2V to 2.376V (t _{OFF1} < 50ms)	—	—	50	mV/μs	*3
	dV/dt	V _{CC}	V _{CC} : 1.3V to 2.376V (t _{OFF2} ≥ 100μs)	—	—	1000	mV/μs	*4
C pin voltage at Power-on	—	C	—	—	—	60	mV	*5
Maximum ramp rate guaranteed to not generate power-on reset	dV/dt	V _{CC}	V _{CC} : Between 2.4V and 4.5V	—	—	50	mV/μs	*6

*1: The specified level detection time applies only for power ramp rate of 1000mV/μs or less.

*2: V_{CC} must be held below 0.2V for a minimum period of t_{OFF1}.

*3: Power-on can detect by satisfying power ramp rate when t_{OFF1} is not satisfied.

*4: V_{CC} must be held below 1.3V for a minimum period of t_{OFF2}.

Power ramp rate must be 1000mV/μs or less from 1.3V to 2.376V.

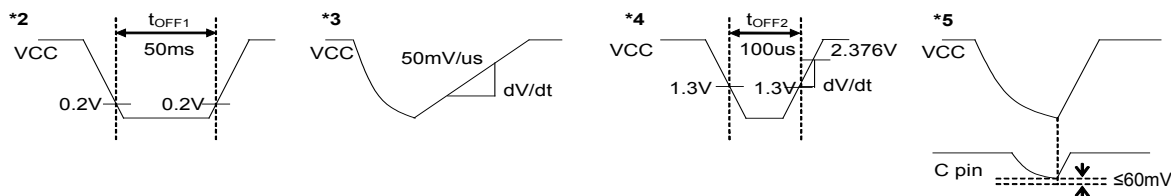
Power-on can detect by satisfying power ramp rate and power off time.

*5: C-pin voltage is below 60 mV when V_{CC} is turned on again.

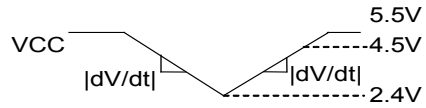
*6: This specification is specified the power supply fluctuation after power on detection. When V_{CC} voltage is between 2.4V and 4.5V, the power supply fluctuation is below 50mV/us, the detection of power-on is suppressed. The power-on does not detect in any power fluctuation between 4.5V and 5.5V.

Note: When using MB91F52xxxE, either *2 or *3 or *4 or *5 must be satisfied. When neither *2 nor *3 nor *4 nor *5 can be satisfied, assert external reset (RSTX) at power-up and at any brownout event.

• Power off time, Power ramp rate, C pin voltage at Power-on



- Maximum ramp rate guaranteed to not generate power-on reset



(4) Multi-function Serial

(4-1) CSIO timing

(4-1-1) Bit setting: SMR: MD2=0, SMR: MD1=1, SMR : MD0=0, SMR: SCINV=0, SCR:SPI=0

(TA: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Condi tions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t _{SCYC}	SCK0 to SCK19	-	4t _{CPP}	-	ns	Internal shift clock mode output pin : C _L =50pF
SCK ↓ → SOT delay time	t _{SLOVI}	SCK0 to SCK2, SCK5 to SCK19 SOT0 to SOT2, SOT5 to SOT19		-30	30	ns	
		SCK3, SCK4 SOT3, SOT4		-300	300	ns	
Valid SIN → SCK ↑ setup time	t _{IVSHI}	SCK0 to SCK2, SCK5 to SCK19 SIN0 to SIN2, SIN5 to SIN19		34	-	ns	
		SCK3, SCK4 SIN3, SIN4		300	-	ns	
SCK ↑ → Valid SIN hold time	t _{SHIXI}	SCK0 to SCK19 SIN0 to SIN19		0	-	ns	
Serial clock "H"pulse width	t _{SHSL}	SCK0 to SCK19	-	t _{CPP} +10	-	ns	External shift clock mode output pin: C _L =50pF
Serial clock "L" pulse width	t _{SLSH}			2t _{CPP} -10	-	ns	
SCK ↓ → SOT delay time	t _{SLOVE}	SCK0 to SCK2, SCK5 to SCK19 SOT0 to SOT2, SOT5 to SOT19		-	33	ns	
		SCK3, SCK4 SOT3, SOT4		-	300	ns	
Valid SIN → SCK ↑ setup time	t _{IVSHE}	SCK0 to SCK19 SIN0 to SIN19		10	-	ns	
SCK ↑ → Valid SIN hold time	t _{SHIXE}			20	-	ns	
SCK fall time	t _F	SCK0 to SCK19		-	5	ns	
SCK rise time	t _R	SCK0 to SCK19		-	5	ns	

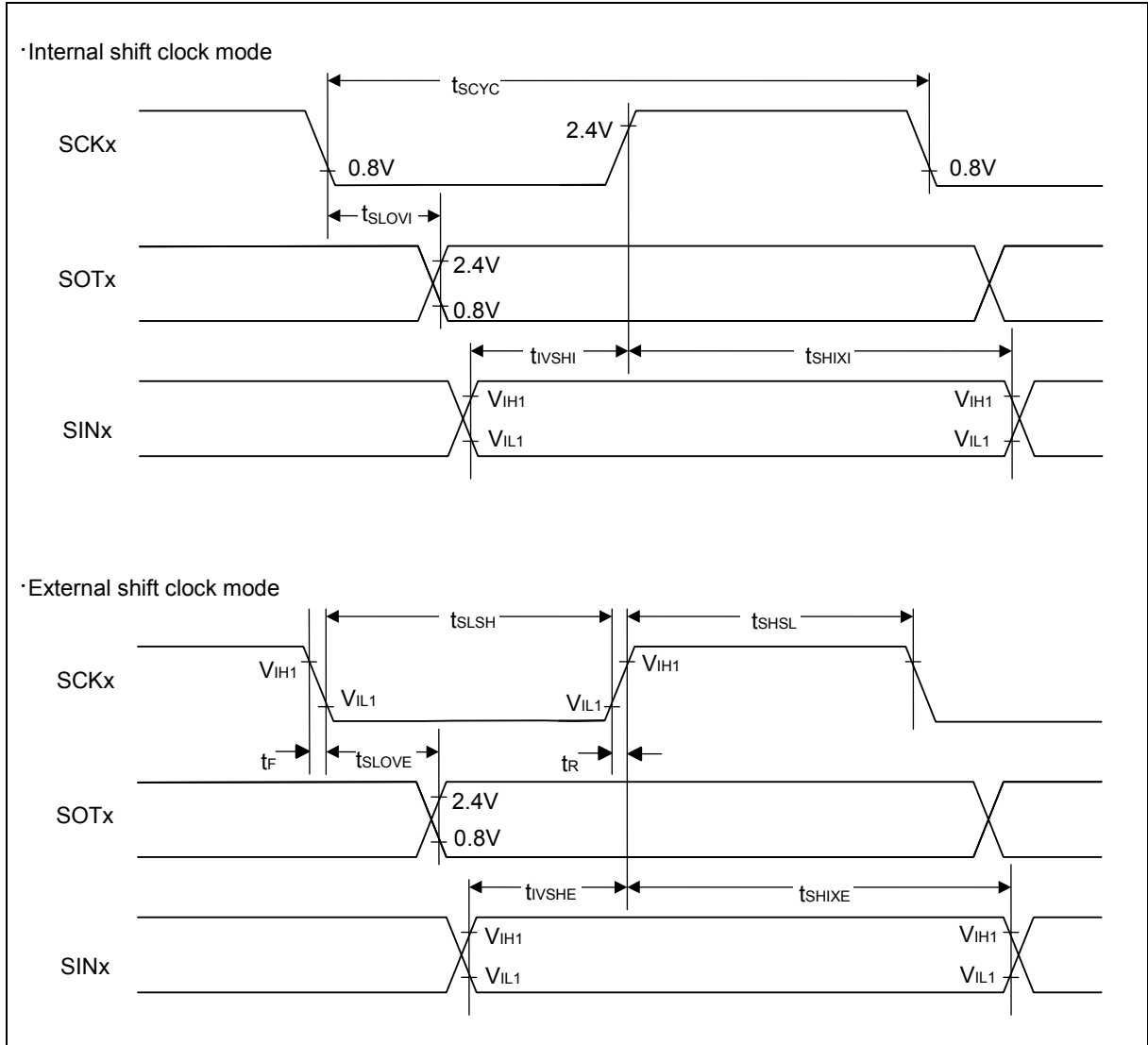
Notes:

AC characteristic in CLK synchronized mode.

C_L is the load capacitance applied to pins during testing.

The maximum baud rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.

See Hardware Manual for details.



(4-1-2) Bit setting: SMR: MD2=0, SMR: MD1=1, SMR : MD0=0, SMR: SCINV=1, SCR:SPI=0

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Condi tions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t _{SCYC}	SCK0 to SCK19	-	4t _{CPP}	-	ns	Internal shift clock mode output pin : C _L =50pF
SCK ↑ → SOT delay time	t _{SHOVI}	SCK0 to SCK2, SCK5 to SCK19 SOT0 to SOT2, SOT5 to SOT19		-30	30	ns	
		SCK3, SCK4 SOT3, SOT4		-300	300	ns	
Valid SIN → SCK ↓ setup time	t _{IVSLI}	SCK0 to SCK2, SCK5 to SCK19 SIN0 to SIN2, SIN5 to SIN19		34	-	ns	
		SCK3, SCK4 SIN3, SIN4		300	-	ns	
SCK ↓ → Valid SIN hold time	t _{SLIXI}	SCK0 to SCK19 SIN0 to SIN19		0	-	ns	
Serial clock "H"pulse width	t _{SHSL}	SCK0 to SCK19	-	t _{CPP} +10	-	ns	External shift clock mode output pin: C _L =50pF
Serial clock "L" pulse width	t _{SLSH}			2t _{CPP} -10	-	ns	
SCK ↑ → SOT delay time	t _{SHOVE}	SCK0 to SCK2, SCK5 to SCK19 SOT0 to SOT2, SOT5 to SOT19		-	33	ns	
		SCK3, SCK4 SOT3, SOT4		-	300	ns	
Valid SIN → SCK ↓ setup time	t _{IVSLE}	SCK0 to SCK19 SIN0 to SIN19		10	-	ns	
SCK ↓ → Valid SIN hold time	t _{SLIXE}			20	-	ns	
SCK fall time	t _F	SCK0 to SCK19		-	5	ns	
SCK rise time	t _R	SCK0 to SCK19		-	5	ns	

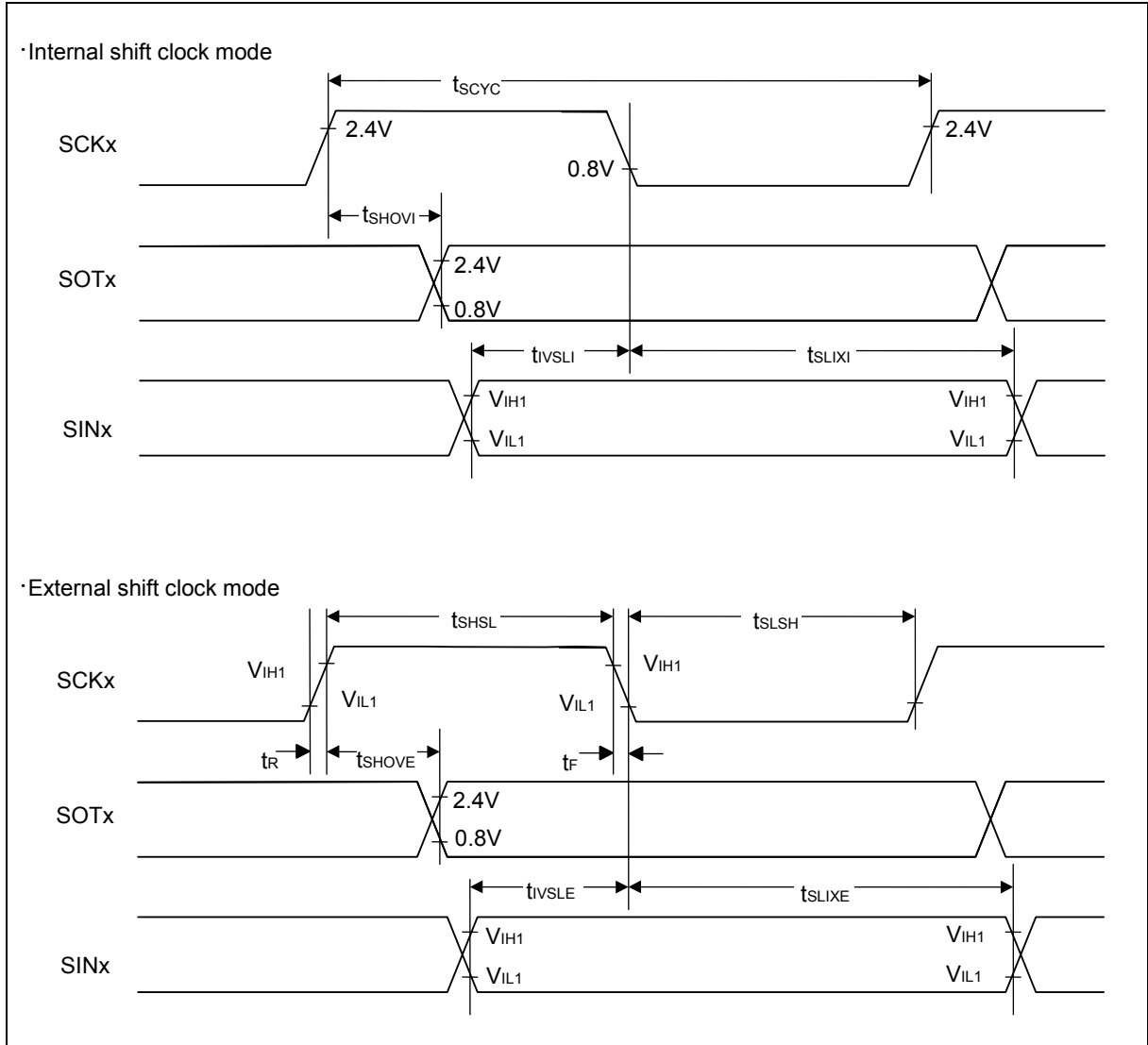
Notes:

AC characteristic in CLK synchronized mode.

C_L is the load capacitance applied to pins during testing.

The maximum baud rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.

See Hardware Manual for details.



(4-1-3) Bit setting: SMR : MD2=0, SMR:MD1=1, SMR : MD0=0, SMR:SCINV=0, SCR:SPI=1

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t _{SCYC}	SCK0 to SCK19	-	4t _{CPP}	-	ns	Internal shift clock mode output pin : C _L =50pF
SCK ↑ → SOT delay time	t _{SHOVI}	SCK0 to SCK2, SCK5 to SCK19 SOT0 to SOT2, SOT5 to SOT19		-30	30	ns	
		SCK3, SCK4 SOT3, SOT4		-300	300	ns	
Valid SIN → SCK ↓ setup time	t _{IVSLI}	SCK0 to SCK2, SCK5 to SCK19 SIN0 to SIN2, SIN5 to SIN19		34	-	ns	
		SCK3, SCK4 SIN3, SIN4		300	-	ns	
SCK ↓ → Valid SIN hold time	t _{SLIXI}	SCK0 to SCK19 SIN0 to SIN19		0	-	ns	
SOT→SCK↓ delay time	t _{SOVLI}	SCK0 to SCK19 SOT0 to SOT19		2t _{CPP} -30	-	ns	
Serial clock "H" pulse width	t _{SHSL}	SCK0 to SCK19	-	t _{CPP} +10	-	ns	External shift clock mode output pin: C _L =50pF
Serial clock "L" pulse width	t _{SLSH}			2t _{CPP} -10	-	ns	
SCK ↑ → SOT delay time	t _{SHOVE}	SCK0 to SCK2, SCK5 to SCK19 SOT0 to SOT2, SOT5 to SOT19		-	33	ns	
		SCK3, SCK4 SOT3, SOT4		-	300	ns	
Valid SIN → SCK ↓ setup time	t _{IVSHE}	SCK0 to SCK19 SIN0 to SIN19		10	-	ns	
SCK ↓ → Valid SIN hold time	t _{SLIXE}			20	-	ns	
SCK fall time	t _F	SCK0 to SCK19		-	5	ns	
SCK rise time	t _R	SCK0 to SCK19		-	5	ns	

Notes:

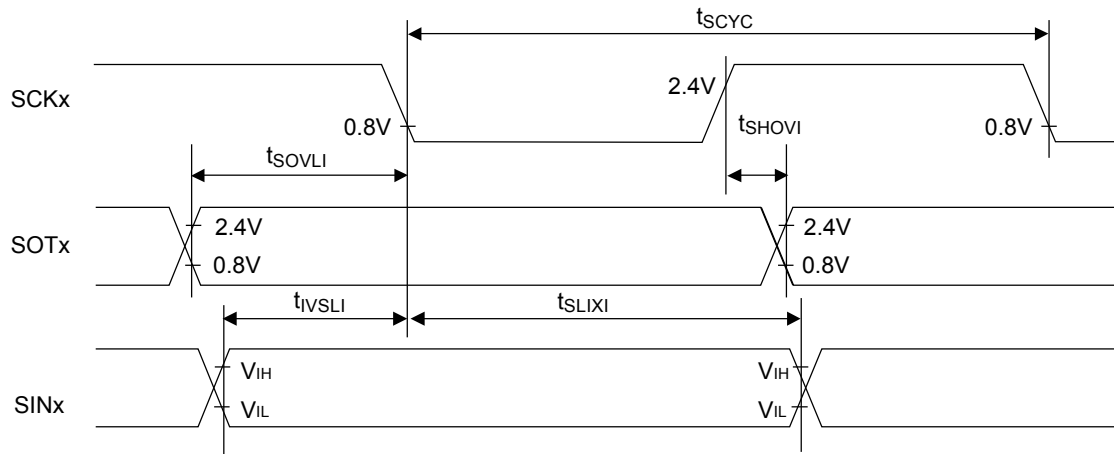
AC characteristic in CLK synchronized mode.

C_L is the load capacitance applied to pins during testing.

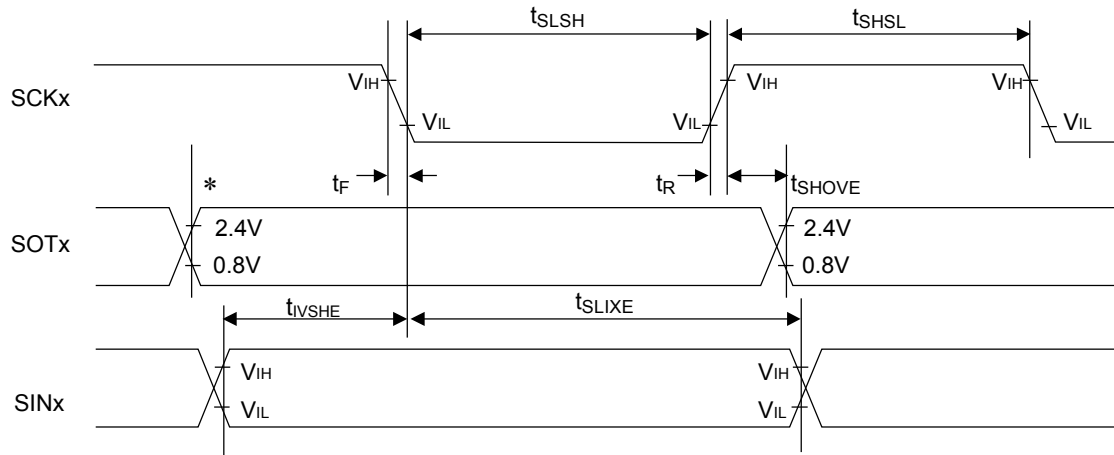
The maximum baud rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.

See Hardware Manual for details.

· Internal shift clock mode



· External shift clock mode



*: It writes in the TDR register and, then, it changes.

(4-1-4) Bit setting: SMR : MD2=0, SMR:MD1=1, SMR : MD0=0, SMR:SCINV=1, SCR:SPI=1

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Condition s	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t _{SCYC}	SCK0 to SCK19	-	4t _{CPP}	-	ns	Internal shift clock mode output pin : C _L =50pF
SCK↓→ SOT delay time	t _{SLOVI}	SCK0 to SCK2, SCK5 to SCK19 SOT0 to SOT2, SOT5 to SOT19		-30	30	ns	
		SCK3, SCK4 SOT3, SOT4		-300	300	ns	
Valid SIN → SCK↑setup time	t _{IVSHI}	SCK0 to SCK2, SCK5 to SCK19 SIN0 to SIN2, SIN5 to SIN19		34	-	ns	
		SCK3, SCK4 SIN3, SIN4		300	-	ns	
SCK↑→ Valid SIN hold time	t _{SHIXI}	SCK0 to SCK19 SIN0 to SIN19		0	-	ns	
SOT→SCK↑ delay time	t _{SOVHI}	SCK0 to SCK19 SOT0 to SOT19		2t _{CPP} -30	-	ns	
Serial clock "H"pulse width	t _{SHSL}	SCK0 to SCK19	-	t _{CPP} +10	-	ns	External shift clock mode output pin: C _L =50pF
Serial clock "L" pulse width	t _{SLSH}			2t _{CPP} -10	-	ns	
SCK↓→ SOT delay time	t _{SLOVE}	SCK0 to SCK2, SCK5 to SCK19 SOT0 to SOT2, SOT5 to SOT19		-	33	ns	
		SCK3, SCK4 SOT3, SOT4		-	300	ns	
Valid SIN → SCK↑setup time	t _{IVSHE}	SCK0 to SCK19 SIN0 to SIN19		10	-	ns	
SCK↑→ Valid SIN hold time	t _{SHIXE}			20	-	ns	
SCK fall time	t _F	SCK0 to SCK19		-	5	ns	
SCK rise time	t _R	SCK0 to SCK19		-	5	ns	

Notes:

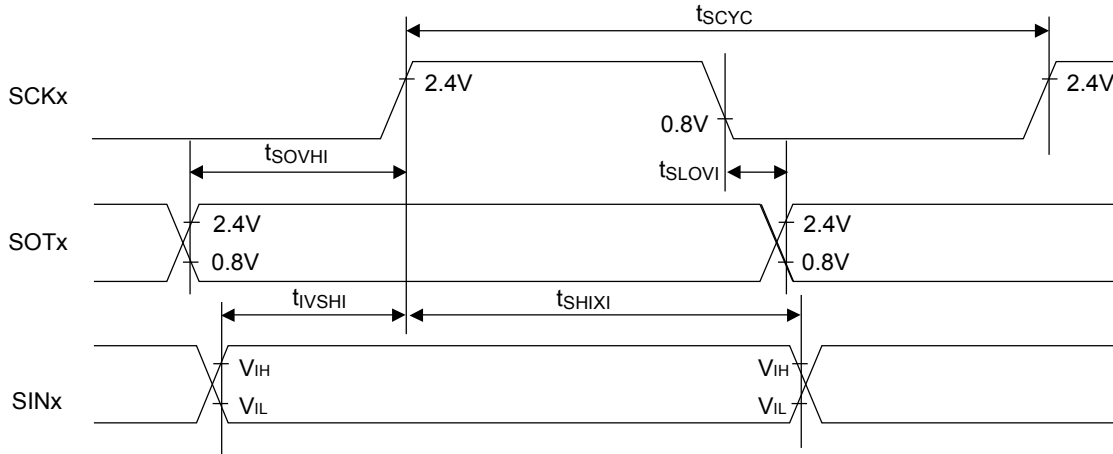
AC characteristic in CLK synchronized mode.

C_L is the load capacitance applied to pins during testing.

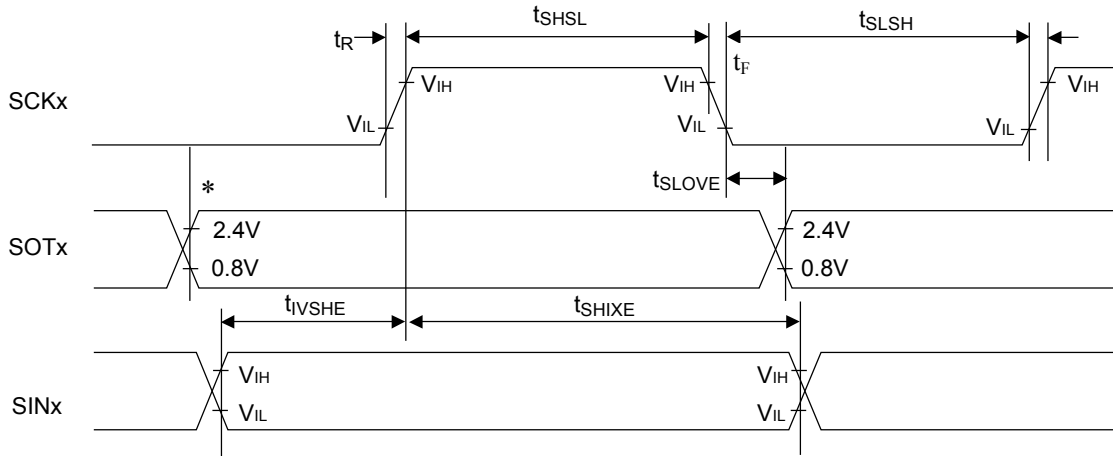
The maximum baud rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.

See Hardware Manual for details.

· Internal shift clock mode



· External shift clock mode



*: It writes in the TDR register and, then, it changes.

(4-1-5) Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,
When Serial chip select is used : SCSCR:CSEN=1,
Serial clock output mark level "H" : SMR,SCSFR:SCINV=0,
Serial chip select Inactive level "H" : SCSCR,SCSFR:CSLVL=1

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↓ setup time	t _{CSSI}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	t _{CSSU} -50 *1	t _{CSSU} +0 *1	ns	Internal shift clock mode output pin : C _L =50pF
		SCK3, SCK4 SCS3, SCS40 to SCS43		t _{CSSU} -50 *1	t _{CSSU} +300 *1	ns	
SCK↑→SCS↑ hold time	t _{CSHI}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19		t _{CSHD} -10 *2	t _{CSHD} +50 *2	ns	
		SCK3, SCK4 SCS3, SCS40 to SCS43		t _{CSHD} -300 *2	t _{CSHD} +50 *2	ns	
SCS deselect time	t _{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19		t _{CSDS} -50 *3	t _{CSDS} +50 *3	ns	
SCS↓→SCK↓ setup time	t _{CSSE}	SCK1 to SCK15, SCK18, SCK19 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	3t _{CPP} +30	-	ns	External shift clock mode output pin: C _L =50pF
SCK↑→SCS↑ hold time	t _{CSHE}			+0	-	ns	
SCS deselect time	t _{CSDE}			3t _{CPP} +30	-	ns	

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS \downarrow →SOT delay time	t_{DSE}	SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19 SOT1, SOT2, SOT5 to SOT15, SOT18, SOT19	-	-	40	ns	External shift clock mode output pin: C _L =50pF
		SCS3, SCS40 to SCS43 SOT3, SOT4		-	300	ns	
SCS \uparrow →SOT delay time	t_{DEE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19 SOT1 to SOT15, SOT18, SOT19	-	+0	-	ns	
SCK \downarrow →SCS \downarrow clock switch time	t_{SCC}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	3 t_{CPP} -10	3 t_{CPP} +50	ns	Internal shift clock mode Round operation output pin: C _L =50pF
		SCK3, SCK4 SCS3, SCS40 to SCS43		3 t_{CPP} -300	3 t_{CPP} +50	ns	

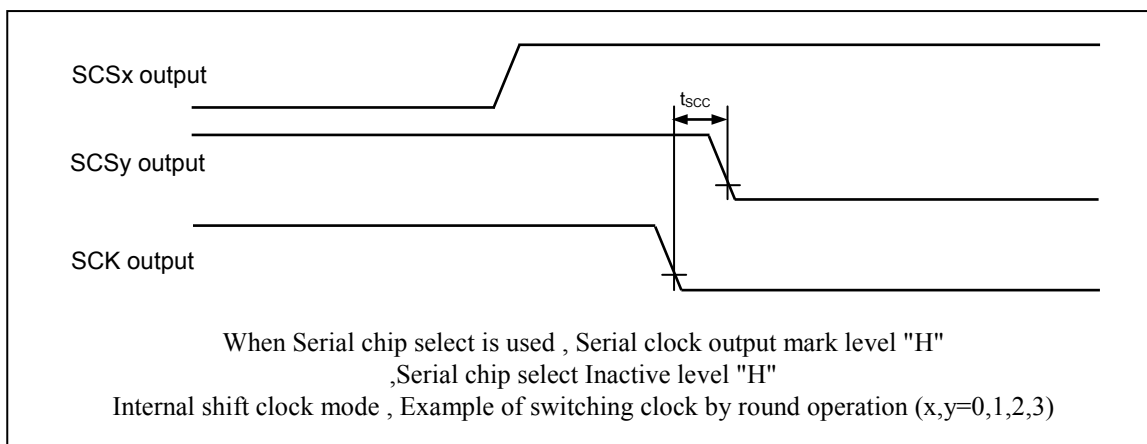
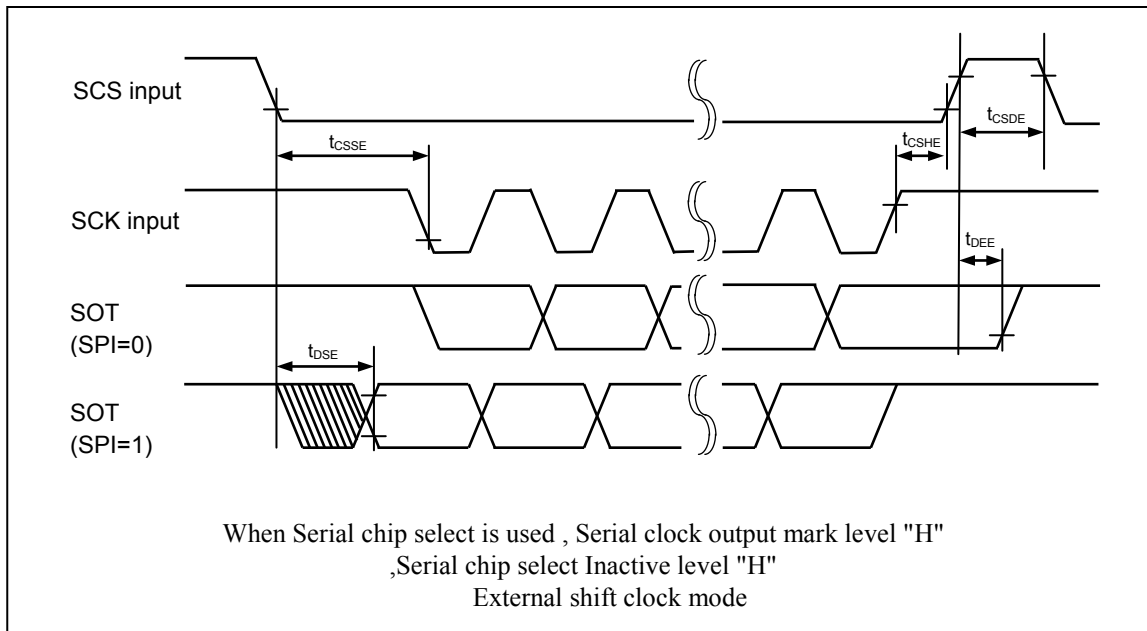
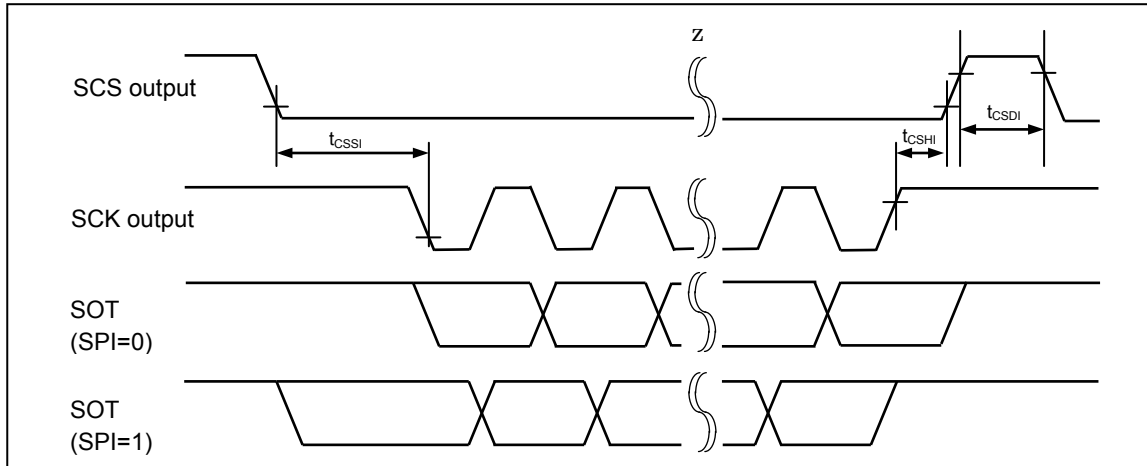
*1: t_{CSSU} = SCSTR:CSSU7-0 × Serial chip select timing operating clock

*2: t_{CSHD} = SCSTR:CSHD7-0 × Serial chip select timing operating clock

*3: t_{CSDS} = SCSTR:CSDS15-0 × Serial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again.

Please see the hardware manual for details of above-mentioned *1, *2, and *3.



(4-1-6) Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,

When Serial chip select is used : SCSCR:CSSEN=1,

Serial clock output mark level "L" : SMR,SCSFR:SCINV=1,

Serial chip select Inactive level "H" : SCSCR,SCSFR:CSLVL=1

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↑ setup time	t _{CSSI}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	t _{CSSU} -50 *1	t _{CSSU} +0 *1	ns	Internal shift clock mode output pin : C _L =50pF
		SCK3, SCK4 SCS3, SCS40 to SCS43		t _{CSSU} -50 *1	t _{CSSU} +300 *1	ns	
SCK↓→SCS↑ hold time	t _{CSHI}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19		t _{CSHD} -10 *2	t _{CSHD} +50 *2	ns	
		SCK3, SCK4 SCS3, SCS40 to SCS43		t _{CSHD} -300 *2	t _{CSHD} +50 *2	ns	
SCS deselect time	t _{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19		t _{CSDS} -50 *3	t _{CSDS} +50 *3	ns	
SCS↓→SCK↑ setup time	t _{CSSE}	SCK1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	3t _{CPP} +30	-	ns	External shift clock mode output pin: C _L =50pF
SCK↓→SCS↑ hold time	t _{CSHE}	SCS1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19		+0	-	ns	
SCS deselect time	t _{CSDE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19		3t _{CPP} +30	-	ns	

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS \downarrow →SOT delay time	t _{DSE}	SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19 SOT1, SOT2, SOT5 to SOT15, SOT18, SOT19	-	-	40	ns	External shift clock mode output pin: C _L =50pF
		SCS3, SCS40 to SCS43 SOT3, SOT4		-	300	ns	
SCS \uparrow →SOT delay time	t _{DEE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19 SOT1 to SOT15, SOT18, SOT19	-	+0	-	ns	
SCK \uparrow →SCS \downarrow clock switch time	t _{SCC}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	3t _{CPP} -10	3t _{CPP} +50	ns	Internal shift clock mode Round operation output pin: C _L =50pF
		SCK3, SCK4 SCS3, SCS40 to SCS43		3t _{CPP} -300	3t _{CPP} +50	ns	

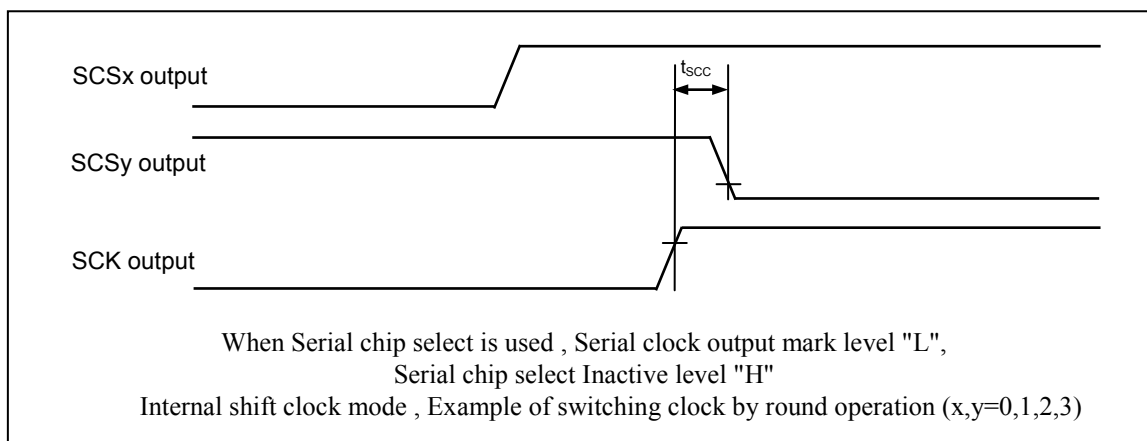
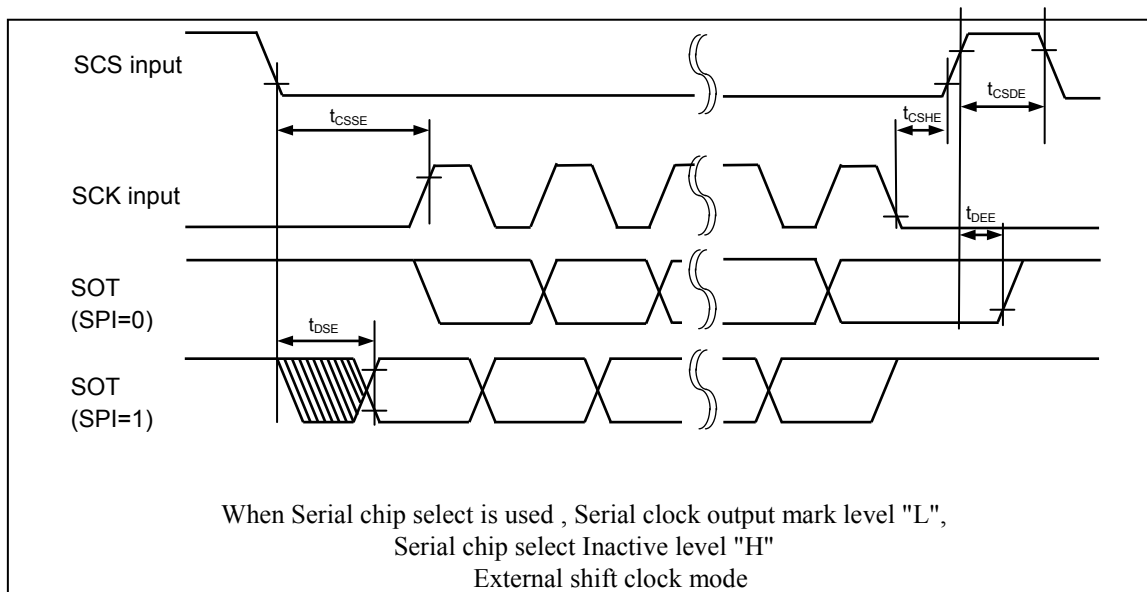
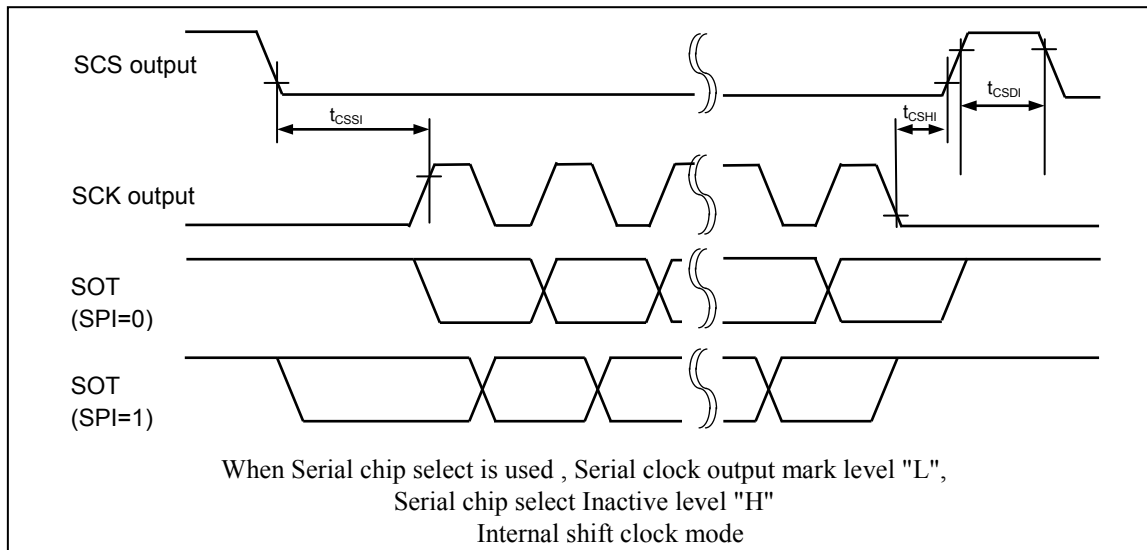
*1: t_{CSSU} = SCSTR:CSSU7-0 × Serial chip select timing operating clock

*2: t_{CSDH} = SCSTR:CSDH7-0 × Serial chip select timing operating clock

*3: t_{CSDS} = SCSTR:CSDS15-0 × Serial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again.

Please see the hardware manual for details of above-mentioned *1, *2, and *3



(4-1-7) Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,
When Serial chip select is used : SCSCR:CSEN=1,
Serial clock output mark level "H" : SMR,SCSFR:SCINV=0,
Serial chip select Inactive level "L" : SCSCR,SCSFR:CSLVL=0

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Condi tions	Value		Unit	Remarks
				Min	Max		
SCS↑→SCK↓ setup time	t _{CSSI}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	t _{CSSU} -50 *1	t _{CSSU} +0 *1	ns	Internal shift clock mode output pin : C _L =50pF
		SCK3, SCK4 SCS3, SCS40 to SCS43		t _{CSSU} -50 *1	t _{CSSU} +300 *1	ns	
SCK↑→SCS↓ hold time	t _{CSHI}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19		t _{CSHD} -10 *2	t _{CSHD} +50 *2	ns	
		SCK3, SCK4 SCS3, SCS40 to SCS43		t _{CSHD} -300 *2	t _{CSHD} +50 *2	ns	
SCS deselect time	t _{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19		t _{CSDS} -50 *3	t _{CSDS} +50 *3	ns	
SCS↑→SCK↓ setup time	t _{CSSE}	SCK1 to SCK15, SCK18, SCK19 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	3t _{CPP} +30	-	ns	External shift clock mode output pin: C _L =50pF
SCK↑→SCS↓ hold time	t _{CSHE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19		+0	-	ns	
SCS deselect time	t _{CSDE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19		3t _{CPP} +30	-	ns	

Parameter	Symbol	Pin name	Condi tions	Value		Unit	Remarks
				Min	Max		
SCS \uparrow →SOT delay time	t_{DSE}	SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCK18, SCK19 SOT1, SOT2, SOT5 to SOT15, SOT18, SOT19	-	-	40	ns	External shift clock mode output pin: $C_L=50pF$
		SCS3, SCS40 to SCS43 SOT3, SOT4		-	300	ns	
SCS \downarrow →SOT delay time	t_{DEE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15 SCK18, SCK19 SOT1 to SOT15, SOT18, SOT19	-	+0	-	ns	
SCK \downarrow →SCS \uparrow clock switch time	t_{SCC}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	$3t_{CPP}-10$	$3t_{CPP}+50$	ns	Internal shift clock mode Round operation output pin: $C_L=50pF$
		SCK3, SCK4 SCS3, SCS40 to SCS43		$3t_{CPP}-300$	$3t_{CPP}+50$	ns	

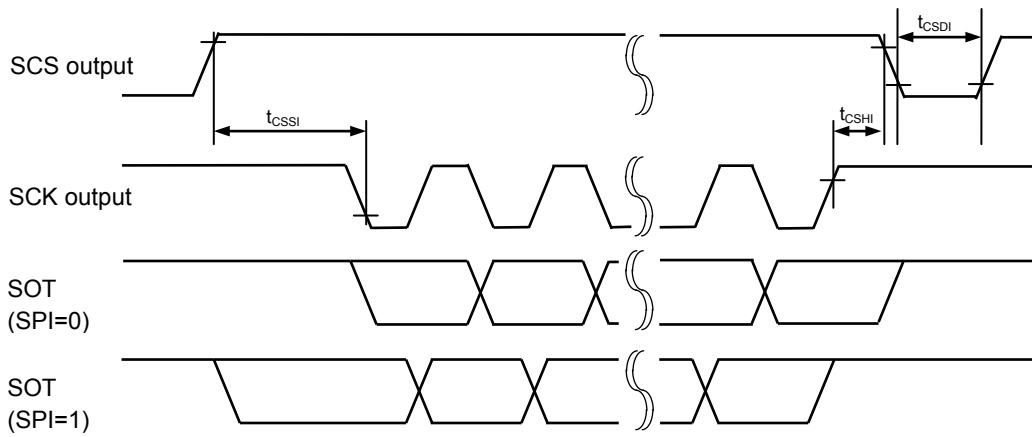
*1: $t_{CSSU} = SCSTR:CSSU7-0 \times$ Serial chip select timing operating clock

*2: $t_{CSHD} = SCSTR:CSHD7-0 \times$ Serial chip select timing operating clock

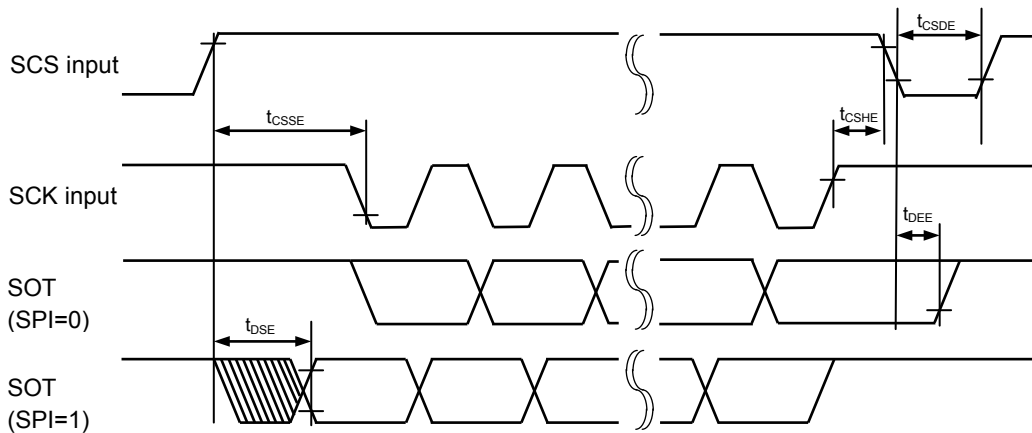
*3: $t_{CSDS} = SCSTR:CSDS15-0 \times$ Serial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again.

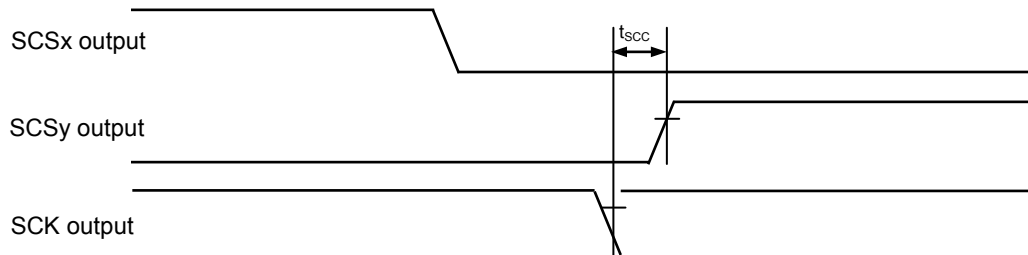
Please see the hardware manual for details of above-mentioned *1, *2, and *3.



When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
Internal shift clock mode



When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
External shift clock mode



When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

(4-1-8) Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,
When Serial chip select is used: SCSCR:CSEN=1,
Serial clock output mark level "L" : SMR,SCSFR:SCINV=1,
Serial chip select Inactive level "L" : SCSCR,SCSFR:CSLVL=0
(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↑→SCK↑ setup time	t _{CSSI}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11, SCS18, SCS19	-	t _{CSSU} -50 *1	t _{CSSU} +0 *1	ns	Internal shift clock mode output pin : C _L =50pF
		SCK3, SCK4 SCS3, SCS40 to SCS43		t _{CSSU} -50 *1	t _{CSSU} +300 *1	ns	
SCK↓→SCS↓ hold time	t _{CSHI}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11, SCS18, SCS19		t _{CSHD} -10 *2	t _{CSHD} +50 *2	ns	
		SCK3, SCK4 SCS3, SCS40 to SCS43		t _{CSHD} -300 *2	t _{CSHD} +50 *2	ns	
SCS deselect time	t _{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11, SCS18, SCS19		t _{CSDS} -50 *3	t _{CSDS} +50 *3	ns	
SCS↑→SCK↑ setup time	t _{CSSE}	SCK1 to SCK15, SCK18, SCK19 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	3t _{CPP} +30	-	ns	External shift clock mode output pin: C _L =50pF
SCK↓→SCS↓ hold time	t _{CSHE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19		+0	-	ns	
SCS deselect time	t _{CSDE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19		3t _{CPP} +30	-	ns	

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS \uparrow →SOT delay time	t _{DSE}	SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19 SOT1, SOT2, SOT5 to SOT15, SOT18, SOT19	-	-	40	ns	External shift clock mode output pin: C _L =50pF
		SCS3, SCS40 to SCS43 SOT3, SOT4		-	300	ns	
SCS \downarrow →SOT delay time	t _{DEE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19 SOT1 to SOT15, SOT18, SOT19	-	+0	-	ns	
SCK \uparrow →SCS \uparrow clock switch time	t _{SCC}	SCK1, SCK2, SCK5 to SCK15, SCK18, SCK19 SCS1, SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS15, SCS18, SCS19	-	3t _{CPP} -10	3t _{CPP} +50	ns	Internal shift clock mode Round operation output pin: C _L =50pF
		SCK3, SCK4 SCS3, SCS40 to SCS43		3t _{CPP} -300	3t _{CPP} +50	ns	

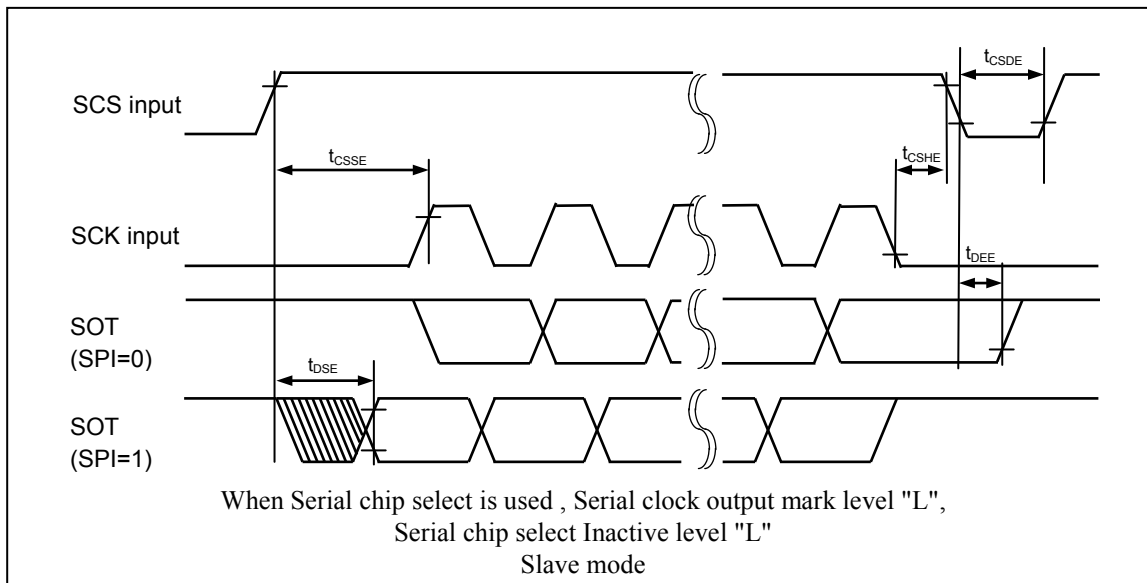
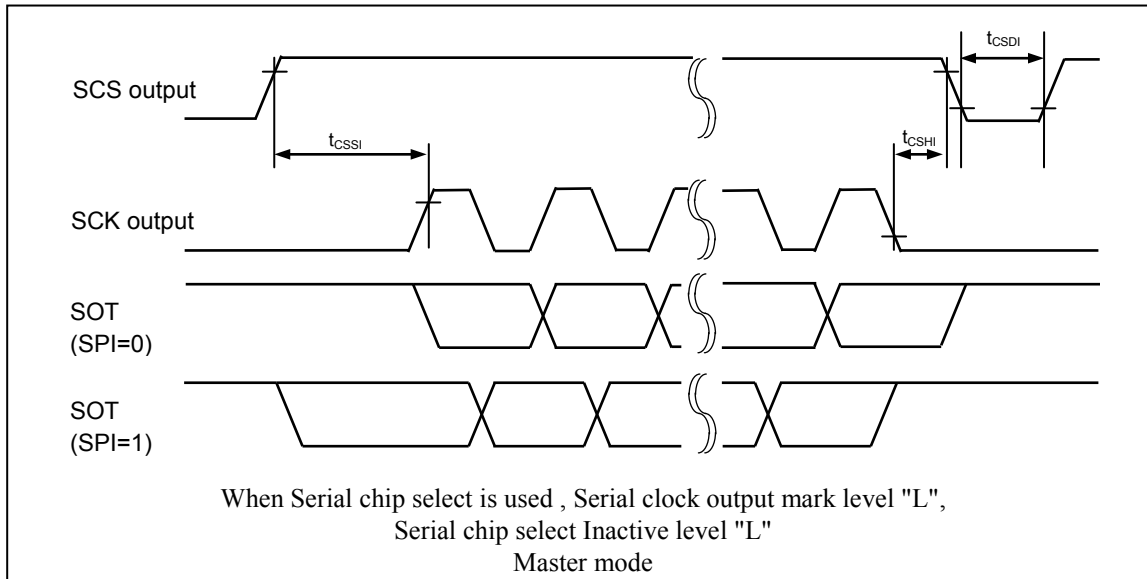
*1: t_{CSSU} = SCSTR:CSSU7-0 × Serial chip select timing operating clock

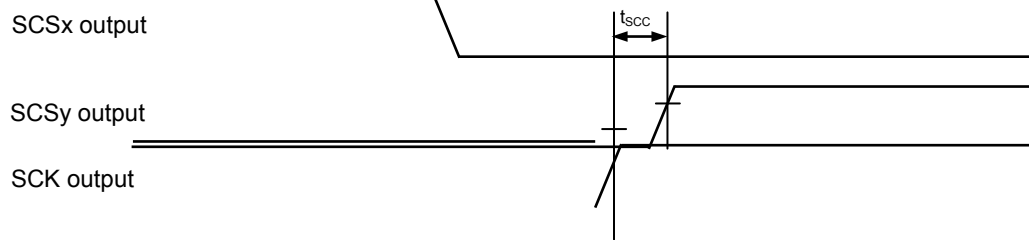
*2: t_{CSDH} = SCSTR:CSDH7-0 × Serial chip select timing operating clock

*3: t_{CSDS} = SCSTR:CSDS15-0 × Serial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again.

Please see the hardware manual for details of above-mentioned *1, *2, and *3.





When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "L"
Master mode, Example of switching clock by round operation (x,y=0,1,2,3)

(4-2) UART (Asynchronous serial interface) timing

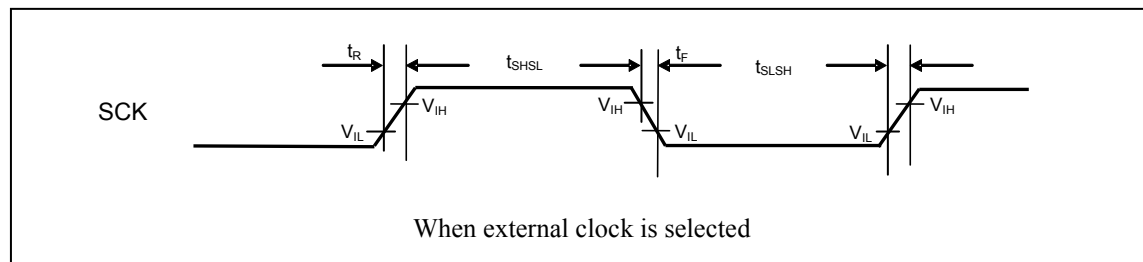
Bit setting: SMR : MD2=0, SMR:MD1=0, SMR : MD0=0

Bit setting: SMR : MD2=0, SMR:MD1=0, SMR : MD0=1

When external clock is selected (BGR:EXT=1)

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Condi tions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t _{SLSH}	SCK0 to SCK19	-	t _{CPP} +10	-	ns	output pin: C _L =50pF
Serial clock "H" pulse width	t _{SHSL}			t _{CPP} +10	-	ns	
SCK fall time	t _F			-	5	ns	
SCK rise time	t _R			-	5	ns	

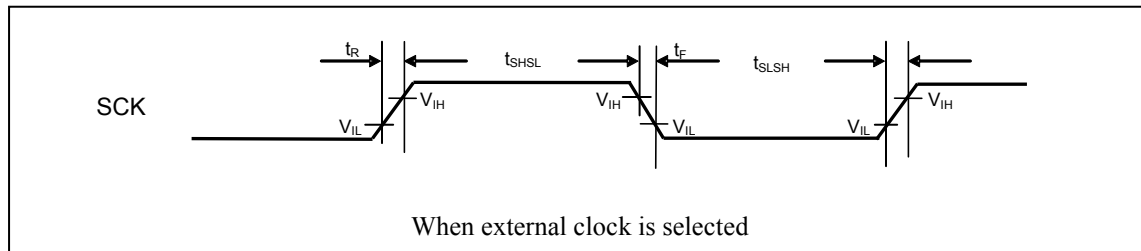


(4-3) LIN Interface (v2.1)(Asynchronous Serial Interface for LIN (v2.1)) timing

Bit setting: SMR : MD2=0, SMR:MD1=1, SMR : MD0=1

(T_A:-40°C to +125°C,V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t _{SLSH}	SCK0 to SCK19	-	t _{CPP} +10	-	ns	output pin: C _L =50pF
Serial clock "H"pulse width	t _{SHSL}			t _{CPP} +10	-	ns	
SCK fall time	t _F			-	5	ns	
SCK rise time	t _R			-	5	ns	



(4-4) I²C timing

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Condition s	Standard mode		Fast mode* ³		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f _{SCL}	SCK3 to SCK8, SCK11 to SCK19	C _L =50pF R= (V _P /I _{OL}) * ¹	0	100	0	400	kHz	
Repeat "start" condition hold time SDA ↓ → SCL ↓	t _{HDSTA}	SOT3 to SOT8, SOT11 to SOT19 (SDA), SCK3 to SCK8, SCK11 to SCK19 (SCL)		4.0	—	0.6	—	μs	
Period of "L" for SCL clock	t _{LOW}	SCK3 to SCK8, SCK11 to SCK19 (SCL)		4.7	—	1.3	—	μs	
Period of "H" for SCL clock	t _{HIGH}	SCK3 to SCK8, SCK11 to SCK19 (SCL)		4.0	—	0.6	—	μs	
Repeat "start" condition setup time SCL ↑ → SDA ↓	t _{SUSTA}	SCK3 to SCK8, SCK11 to SCK19 (SCL)		4.7	—	0.6	—	μs	
Data hold time SCL ↓ → SDA ↓ ↑	t _{HDDAT}	SOT3 to SOT8, SOT11 to SOT19 (SDA) SCK3 to SCK8, SCK11 to SCK19 (SCL)		0	3.45* ²	0	0.9* ³	μs	
Data setup time SDA ↓ ↑ → SCL ↑	t _{SUDAT}	SOT3 to SOT8, SOT11 to SOT19 (SDA) SCK3 to SCK8, SCK11 to SCK19 (SCL)		250	—	100	—	ns	
"Stop" condition setup time SCL ↑ → SDA ↑	t _{SUSTO}	SOT3 to SOT8, SOT11 to SOT19 (SDA) SCK3 to SCK8, SCK11 to SCK19 (SCL)		4.0	—	0.6	—	μs	
Bus-free time between "stop" condition and "start" condition	t _{BUF}	—		4.7	—	1.3	—	μs	
Noise filter	t _{SP}	—	—	2t _{CPP} * ⁴	—	2t _{CPP} * ⁴	—	ns	

Notes: Only ch.3, ch.4 and ch.12-ch.19 are standard mode/fast mode correspondence. In ch.5-ch.8 and ch.11, only a standard mode is correspondences.

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively.

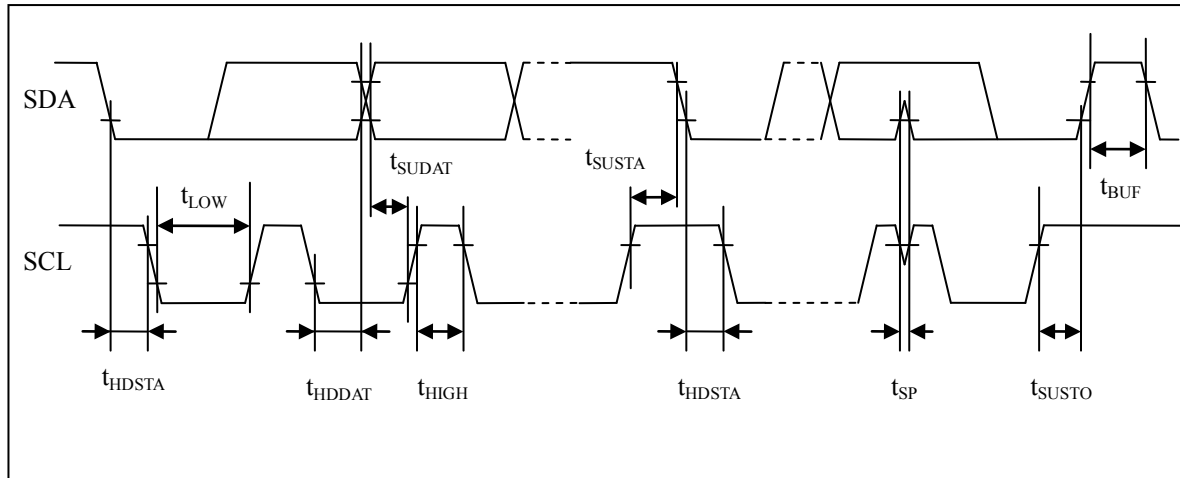
V_p shows that the power-supply voltage of the pull-up resistor and I_{OL} shows the V_{OL} guarantee current.

*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: A fast mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CPP} is the peripheral clock cycle time. Adjust the clock of the bus in the surrounding to 8MHz or more when use I²C.

·I²C timing



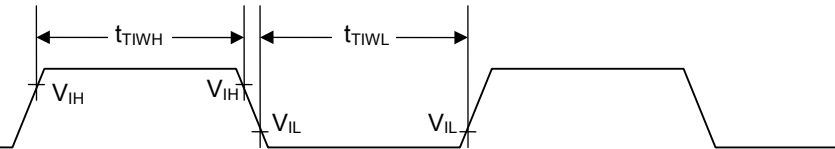
(5) Timer input timing

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t _{TIWH} , t _{TIWL}	TIN0 to TIN7, ICU0 to ICU11, FRCK0 to FRCK10, TIOA0, TIOA1, TIOB0, TIOB1, AIN0 to AIN3, BIN0 to BIN3, ZIN0 to ZIN3	—	4t _{CPP}	—	ns	

·Timer input timing

TINx,
ICUx,
FRCKx,
TIOAx,TIOBx
AINx,BINx,ZINx



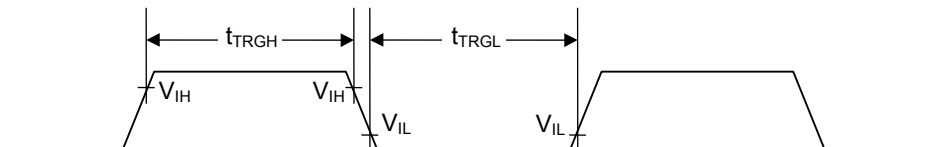
(6) Trigger input timing

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t _{TRGH} , t _{TRGL}	INT0 to INT23, ADTG0, ADTG1, RX0 to RX5	—	5t _{CPP}	—	ns	
				1	—	μs	At stop mode

·Trigger input timing

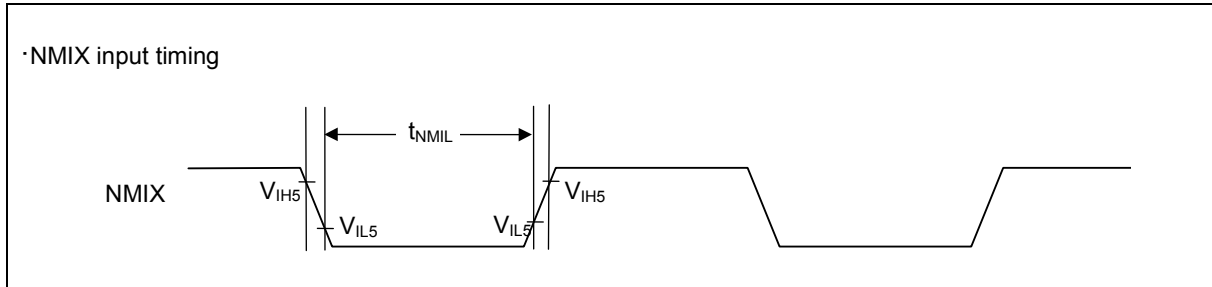
INTx
ADTG
RXx



(7) NMI input timing

(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V,V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t _{NMIL}	NMIX	—	4t _{CPP}	—	ns	



(8) Low voltage detection (External low-voltage detection)

 (T_A: -40°C to +125°C, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V _{DP5}	VCC	-	2.7	-	5.5	V	
Detection voltage ^{*3}	V _{DL}		*1	-8%	LVD5F_SEL [3:0]	+8%	V	LVD5F_SEL [3:0] are programmable. Refer to the hardware manual.
Hysteresis width	V _{HYS}		-	-	0.1	-	V	When power-supply voltage rises
Low voltage detection time	T _d	-	-	-	-	30	μs	
Power supply voltage regulation	-	VCC	-	-2	-	2	V/ms	*2

*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: Please suppress the change of the power supply within the range of the power-supply voltage regulation to do a low voltage detection by detecting voltage (V_{DL}).

*3: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V).

This LVD setting cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage (2.7V).

Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

(9) Low voltage detection (Internal low-voltage detection)

 (T_A: -40°C to +125°C, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V _{RDP5}	-	-	0.6	-	1.4	V	
Detection voltage ^{*2}	V _{RDL}		*1	0.8	0.9	1.0	V	When power-supply voltage falls
Hysteresis width	V _{RHYS}		-	-	0.1	-	V	When power-supply voltage rises
Low voltage detection time	-	-	-	-	-	30	μs	

*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: The detection voltage of the internal low voltage detection is 0.9V±0.1V.

This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage.

Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

(10) External bus I/F (synchronous mode) timing

(T_A: -40°C to +105°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}= AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

(external load capacitance 50pF)

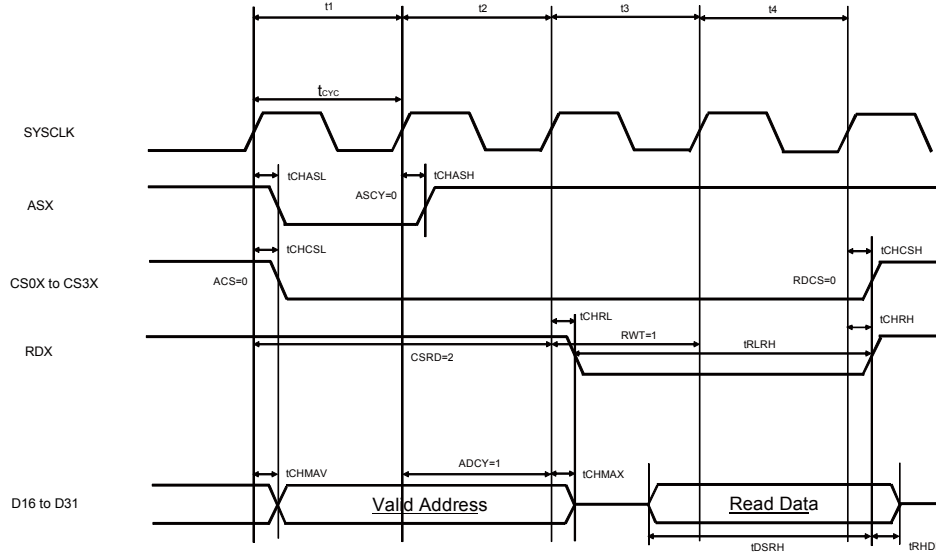
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Cycle time	t _{CYC}	SYSCLK	25	-	ns	V _{CC} =5.0V±10% ^{*1}
			31.25			V _{CC} =3.3V±0.3V
ASX delay time	t _{CHASL} , t _{CHASH}	SYSCLK, ASX	0.5	18	ns	
CS0X to CS3X delay time	t _{CHCSL} , t _{CHCSH}	SYSCLK, CS0X to CS3X	0.5	18	ns	
A00 to A21 delay time	t _{CHAV} , t _{CHAX}	SYSCLK, A00 to A21	0.5	18	ns	
RDX delay time	t _{CHRL} , t _{CHRH}	SYSCLK, RDX	0.5	18	ns	
RDX minimum pulse	t _{RLRH}	RDX	t _{CYC} × 2 - 20	-	ns	RWT=1, set RWT to 1 or more. ^{*2}
Data setup → RDX↑time	t _{DSRH}	RDX, D16 to D31	18+t _{CYC}	-	ns	Same as above
RDX↑→ data hold	t _{RHDH}		0	-	ns	
WRnX delay time	t _{CHWL} , t _{CHWH}	SYSCLK, WR0X, WR1X	0.5	18	ns	
WRnX minimum pulse	t _{WLWH}	WR0X, WR1X	t _{CYC} - 10	-	ns	WWT=0 ^{*2}
SYSCLK↑→ data output time	t _{CHDV}	SYSCLK, D16 to D31	0.5	18	ns	
SYSCLK↑→ data hold time	t _{CHDX}		-	18	ns	Set WRCS to 1 or more.

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
SYCLK↑→ address output time	t_{CHMAV}	SYCLK, D16 to D31	0.5	18	ns	
SYCLK↑→ address hold time	t_{CHMAX}		-	18	ns	In multiplex mode, set as follows: ·Set CSWR and CSRD to 2 or more. ·ASYC must satisfy the following conditions because of setting $ADCY > ASYC$ and protocol violation prevention. $ADCY + 1 \leq ACS + CSRD$ $ADCY + 1 \leq ACS + CSWR$ $ASYC + 1 \leq ACS + CSRD$ $ASYC + 1 \leq ACS + CSWR$ See Hardware Manual for details.

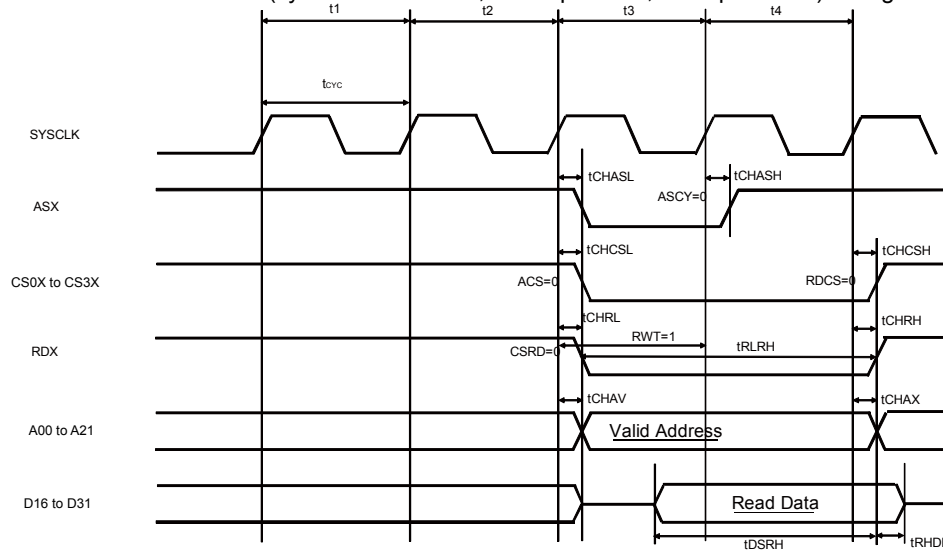
*1: Please use it with external load capacity 12pF or less for $V_{CC} = 3.3V \pm 0.3V$ (40MHz operation).

*2: If the bus is expanded by automatic wait insertion or RDY input, add time ($t_{CYC} \times$ the number of expanded cycles) to the rated value.

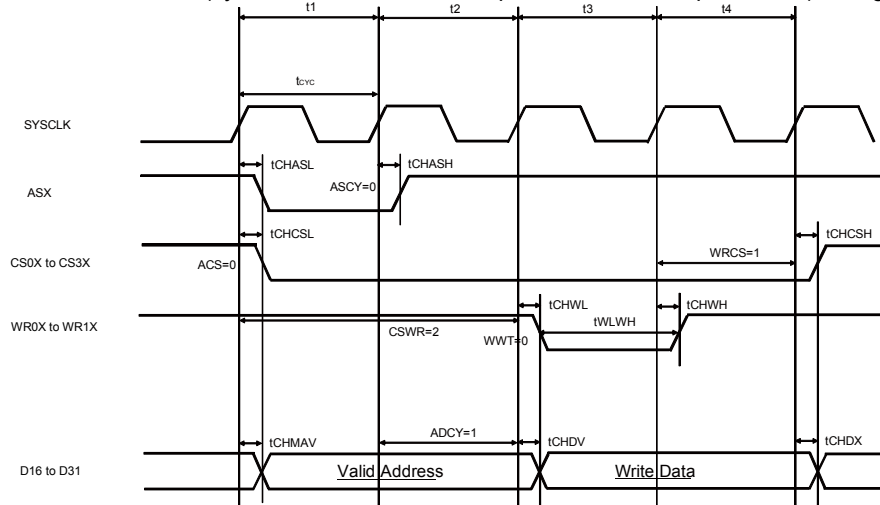
External bus I/F (synchronous mode, read operation, and multiplex mode) timing



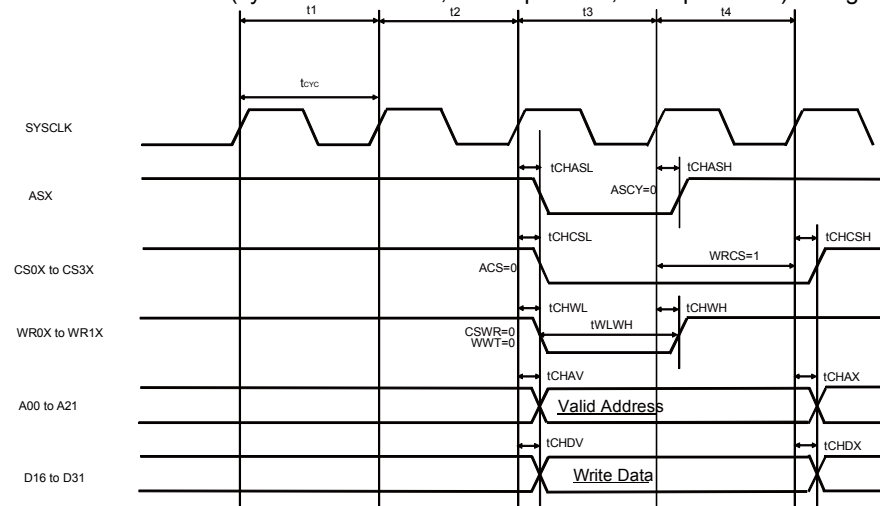
External bus I/F (synchronous mode, read operation, and split mode) timing



External bus I/F (synchronous mode, write operation, and multiplex mode) timing



External bus I/F (synchronous mode, write operation, and split mode) timing



(11) External bus I/F (asynchronous mode) timing

(T_A: -40°C to +105°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

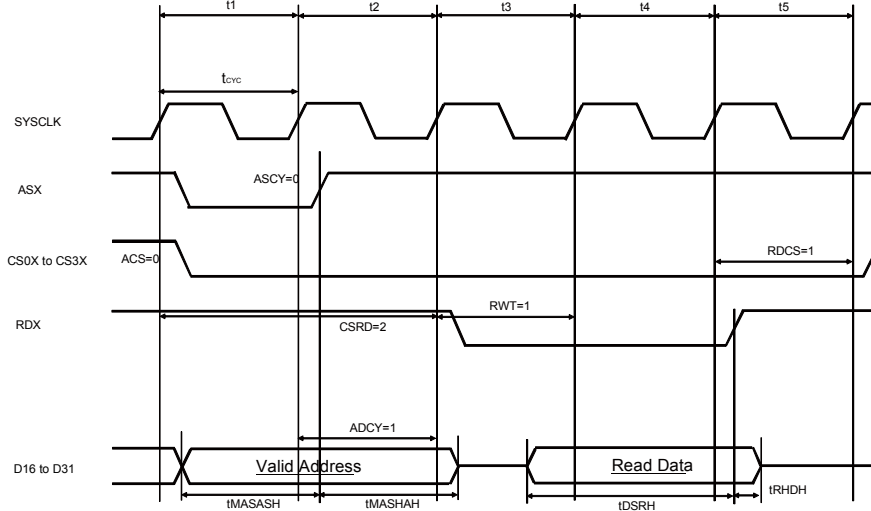
(external load capacitance 50pF)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Cycle time	t _{CYC}	SYSCLK	25	-	ns	V _{CC} =5.0V±10% ^{*1}
			31.25			V _{CC} =3.3V±0.3V
Address setup → RDX↑time	t _{ASRH}	RDX, A00 to A21	2×t _{CYC} - 12	2×t _{CYC} + 12	ns	RWT=1, set RWT to 1 or more. ^{*2}
RDX↑→ Address hold	t _{RHAH}		t _{CYC} - 12	t _{CYC} + 12	ns	Set RDCS to 1 or more.
Data setup→ RDX↑time	t _{DSRH}	RDX, D16 to D31	18 + t _{CYC}	-	ns	RWT=1, set RWT to 1 or more.
RDX↑→ Data hold	t _{RHDH}		0	-	ns	
Address setup→ WRnX↑time	t _{ASWH}	WR0X to WR1X, A00 to A21	t _{CYC} - 12	t _{CYC} + 12	ns	WWT=0 ^{*2}
WRnX↑→ Address hold	t _{WHAH}		t _{CYC} - 12	t _{CYC} + 12	ns	Set WRCS to 1 or more.
Data setup→ WRnX↑time	t _{DSWH}	WR0X to WR1X, D16 to D31	t _{CYC} - 16	t _{CYC} + 16	ns	WWT=0 ^{*2}
WRnX↑→ Data hold	t _{WHDH}		t _{CYC} - 16	t _{CYC} + 16	ns	Set WRCS to 1 or more.
Address setup → ASX↑time	t _{MASASH}	ASX, D16 to D31	t _{CYC} -16	t _{CYC} + 16	ns	ASCY=0
ASX↑→Address hold	t _{MASHAH}		t _{CYC} -16	t _{CYC} + 16	ns	In multiplex mode, set as follows: <input type="checkbox"/> Set CSWR and CSRD to 2 or more. <input type="checkbox"/> ASCY must satisfy the following conditions because of setting ADCY > ASCY and protocol violation prevention. ADCY + 1 ≤ ACS + CSRD ADCY + 1 ≤ ACS + CSWR ASCY + 1 ≤ ACS + CSRD ASCY + 1 ≤ ACS + CSWR See Hardware Manual for details.

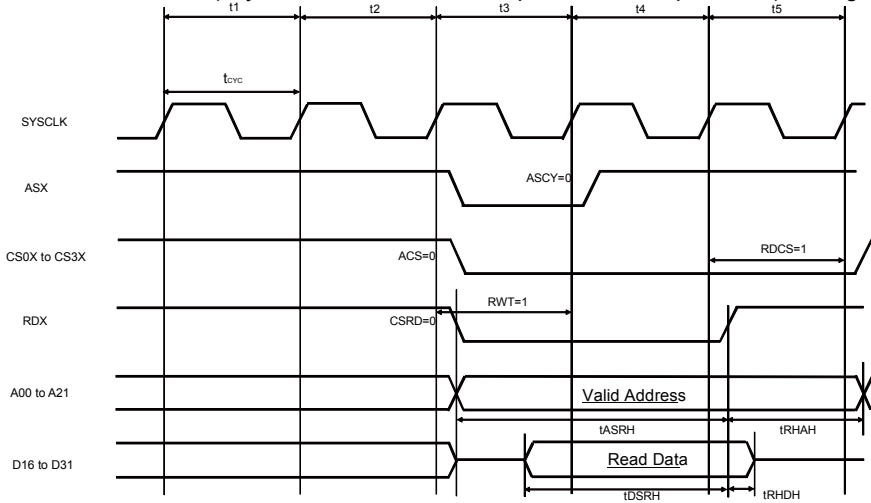
*1: Please use it with external load capacity 12pF or less for V_{CCE}=3.3V±0.3V (40MHz operation).

*2: If the bus is expanded by automatic wait insertion or RDY input, add time (t_{CYC} × the number of expanded cycles) to the rated value.

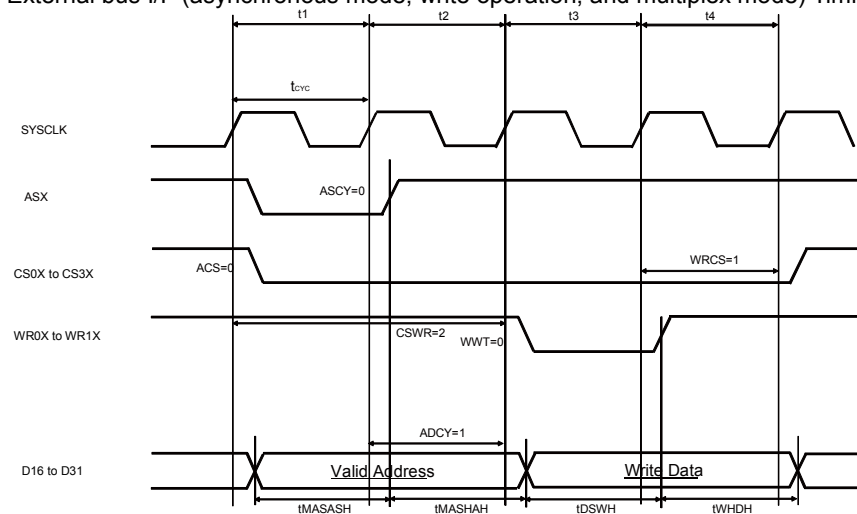
External bus I/F (asynchronous mode, read operation, and multiplex mode) Timing



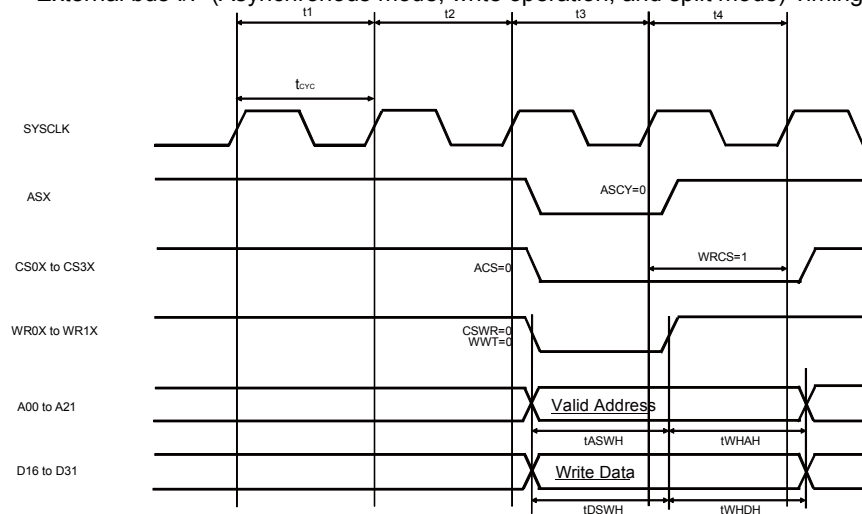
External bus I/F (asynchronous mode, read operation, and split mode) Timing



External bus I/F (asynchronous mode, write operation, and multiplex mode) Timing



External bus I/F (Asynchronous mode, write operation, and split mode) Timing

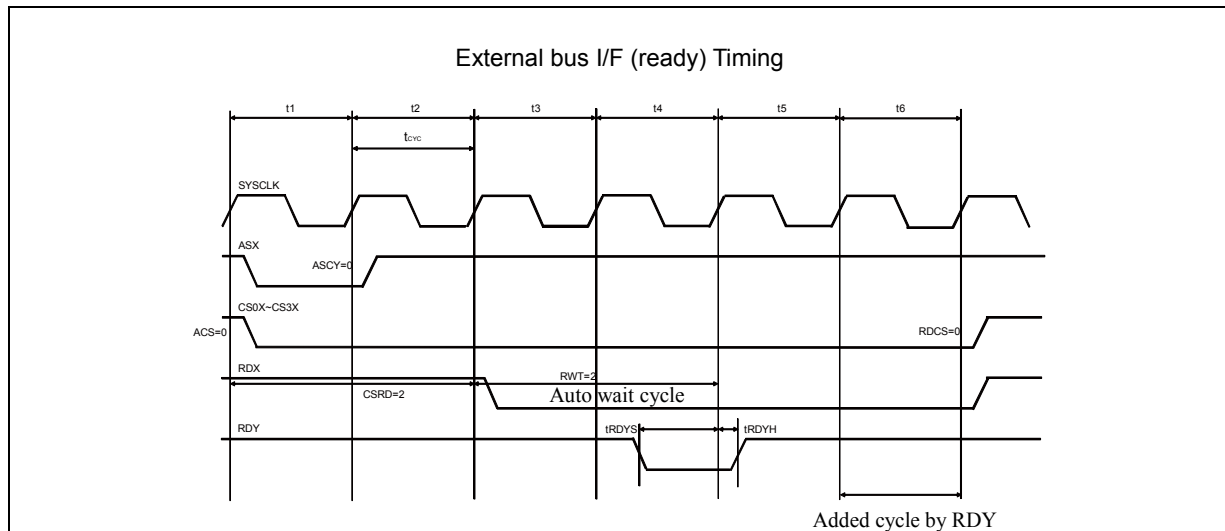


(12) External bus I/F (ready) Timing

(T_A: -40°C to +105°C, V_{CC}=AV_{CC}=5.0V ± 10%/V_{CC}= AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

(external load capacitance 50pF)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Cycle time	t _{CYC}	SYSCLK	50	-	ns	If using RDY, set SYSCLK to 20 MHz or less.
RDY setup time → SYSCLK↑	t _{RDYS}	SYSCLK, RDY	28	-	ns	
SYSCLK↑→ RDY hold time	t _{RDYH}	SYSCLK, RDY	0	-	ns	



12. A/D Converter

(1) 12-bit A/D Converter Electrical Characteristics

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V ± 10%/V_{CC}= AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Total error	-	-	-	-	±12	LSB	
Linearity error	-	-	-	-	± 4.0	LSB	
Differential linearity error	-	-	-	-	± 1.9	LSB	
Zero transition voltage	V _{OT}	AN0 to AN63	AVRL-11.5LSB	-	AVRL+12.5LSB	V	1LSB=(V _{FST} -V _{OT})/4094
Full-scale transition voltage	V _{FST}	AN0 to AN63	AVRH-13.5LSB	-	AVRH+10.5LSB	V	
Sampling time	t _{SMP}	-	0.7	-	-	μs	*1
Compare time	t _{CMP}	-	0.7	-	-	μs	*1
A/D conversion time	t _{CNV}	-	1.4	-	-	μs	*1
Analog port input current	I _{AIN}	AN0 to AN63	-1.0	-	+1.0	μA	V _{AVSS} ≤ V _{AIN} ≤ V _{AVCC}
Analog input voltage	V _{AIN}	AN0 to AN63	AVRL	-	AVRH	V	
Reference voltage	AVRH	AVRH	3.0	-	5.5	V	
	AVRL	AVSS/AVRL	-	0.0	-	V	
Power supply current	I _A	AVCC*3	-	0.47	0.63	mA	Per unit T _A : +105°C
			-	0.47	0.7	mA	Per unit T _A : +125°C
	I _{AH}		-	-	2.5	μA	*2
	I _R	AVRH	-	1	1.96	mA	Per unit
	I _{RH}		-	-	1.6	μA	*2
Variation between channels	-	AN0 to AN63	-	-	4	LSB	

*1: Time for each channel.

*2: Power supply current (V_{CC} = AV_{CC} = 5.0 V) is specified if A/D converter is not operating and CPU is stopped.

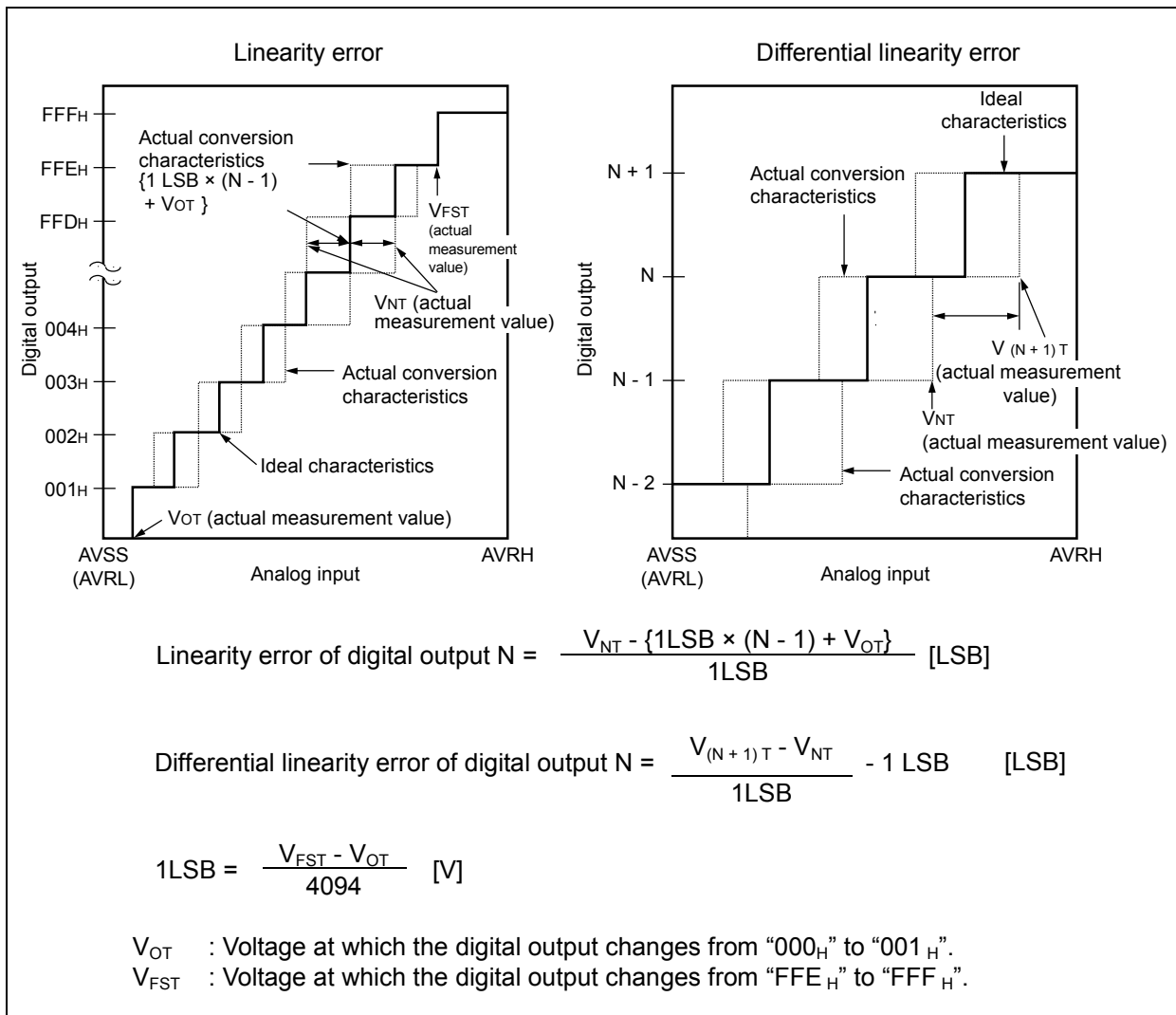
*3: The power supply current described only current value on A/D converter.

The total AV_{CC} current value must be calculated the power supply current for A/D converter and D/A converter.

Note: Please use the clock of 0.5MHz-20MHz for the output clock of A/D converter to guarantee accuracy.

(2) Definition of A/D Converter Terms

Resolution	: Analog variation that is recognized by an A/D converter.
Linearity error	: Deviation of the actual conversion characteristics from a straight line that connects the zero transition point ("0000 0000 0000" ← → "0000 0000 0001") to the full-scale transition point ("1111 1111 1110" ← → "1111 1111 1111").
Differential linearity error	: Deviation of the input voltage from the ideal value that is required to change the output code by 1LSB.

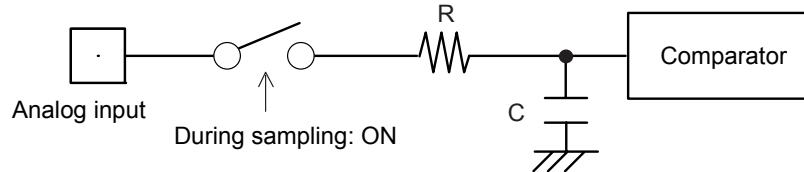


(3) Notes on Using A/D Converter

<About the output impedance of the analog input of external circuit>

- When the external impedance is too high, the sampling period for analog voltages may not be sufficient. In this case, it is recommended to connect the capacitor (approx. 0.1 μ F) to the analog input pin.

☐ Analog input circuit model



	R	C	
12bit A/D	1.9k Ω (Max)	8.30pF (Max)	(4.5V \leq AV _{CC} \leq 5.5V)
	4.3k Ω (Max)	8.30pF (Max)	(3.0V \leq AV _{CC} \leq 3.6V)

Note: Listed values must be considered as reference values.

15. Flash Memory

(1) Electrical Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	—	200	800	ms	8 Kbytes sector* ¹ , excluding internal preprogramming time
	—	300	1100	ms	8 Kbytes sector* ¹ , including internal preprogramming time
	—	400	2000	ms	64 Kbytes sector* ¹ , excluding internal preprogramming time
	—	700	3700	ms	64 Kbytes sector* ¹ , including internal preprogramming time
8-bit writing time	—	9	288	μs	Exclusive of overhead time at system level* ¹
16-bit writing time	—	12	384	μs	Exclusive of overhead time at system level* ¹
ECC writing time	—	9	288	μs	Exclusive of overhead time at system level* ¹
Erase cycle* ² / Data retain time	1,000 cycles/ 20 years, 10,000 cycles/ 10 years, 100,000 cycles/ 5 years	—	—	—	Average T _A =+85°C* ³

*1: The guaranteed value for erasure up to 100,000 cycles.

*2: Number of erase cycles for each sector.

*3: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

(2) Notes

While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited.

In the application system where V_{CC} might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function.

To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}), hold V_{CC} at 2.7V or more within the duration calculated by the following expression:

$$T_d [\mu s] + (\text{period of PCLK} [\mu s] \times 257) + 50 [\mu s]$$

*: See "4.AC Characteristics (8) Low-voltage detection (External low-voltage detection) "

16. D/A Converter

(T_A: -40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}= AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

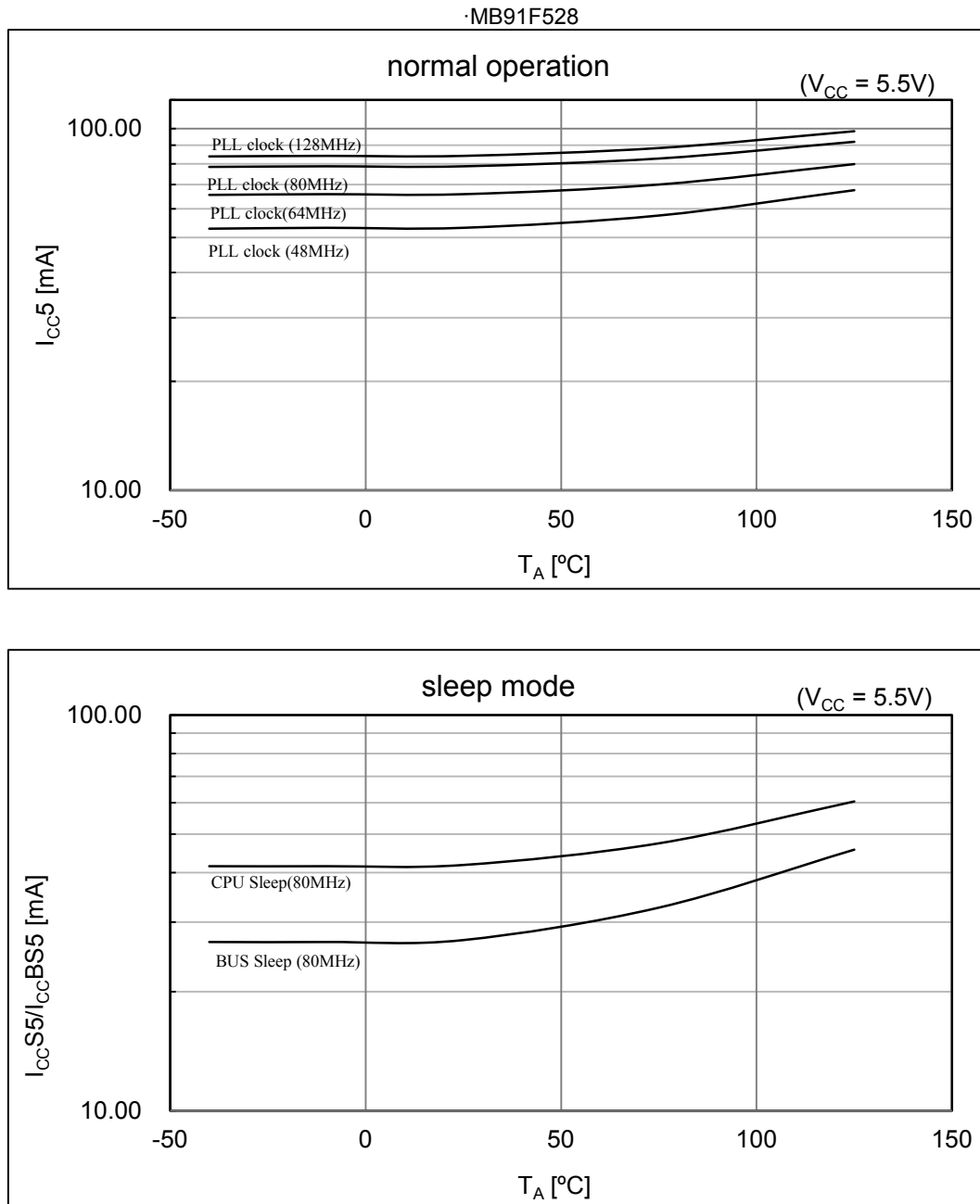
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	-	-	—	—	—	8	bit	
Differential linearity error	-	-	—	—	—	± 3.0	LSB	
Conversion time	-	-	—	0.47	0.58	0.69	μs	C _L =20
			—	2.37	2.90	3.43	μs	C _L =100
Output impedance	R _o	DA0, DA1	—	3.1	3.8	4.5	kΩ	
Power supply current ^{*1}	I _A	AVCC	—	—	475	580	μA	Each channel
	I _{AH}	AVCC	—	—	—	7.5	μA	When powerdown Each channel

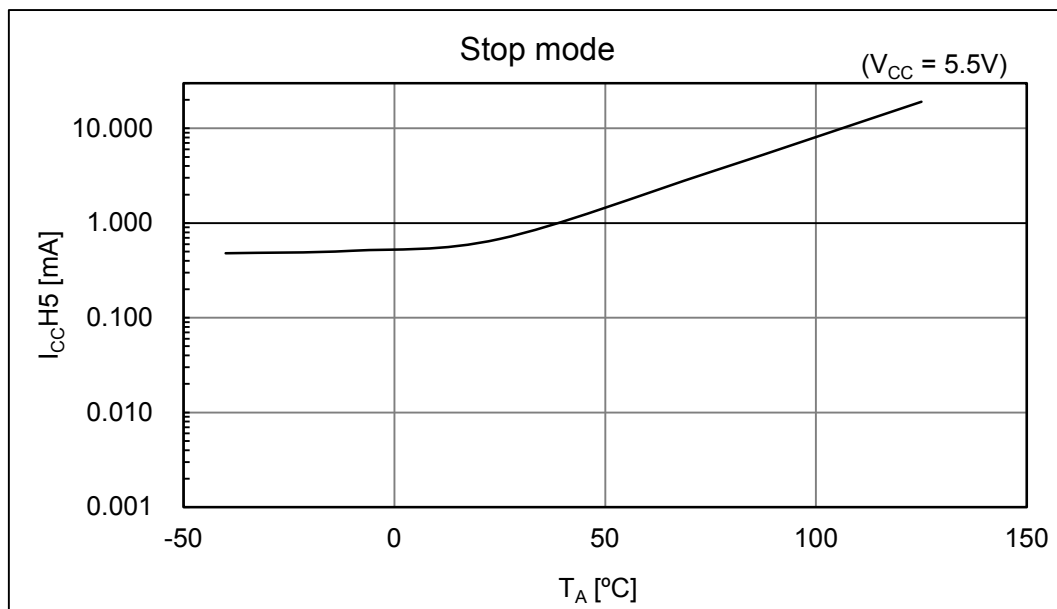
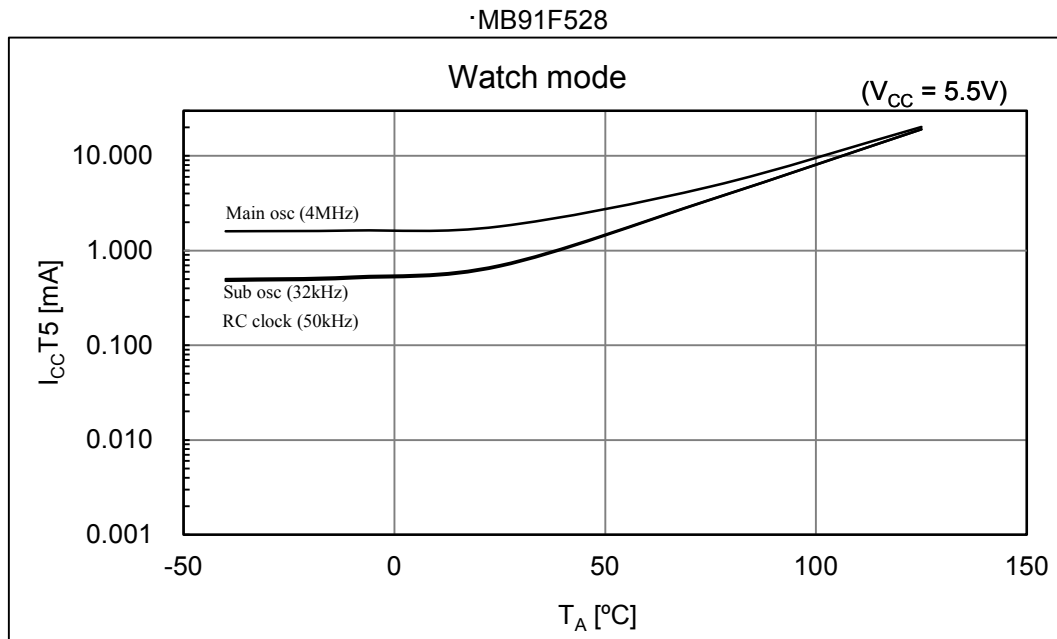
*1: The power supply current described only current value on D/A converter.

The total AV_{CC} current value must be calculated the power supply current for D/A converter and A/D converter.

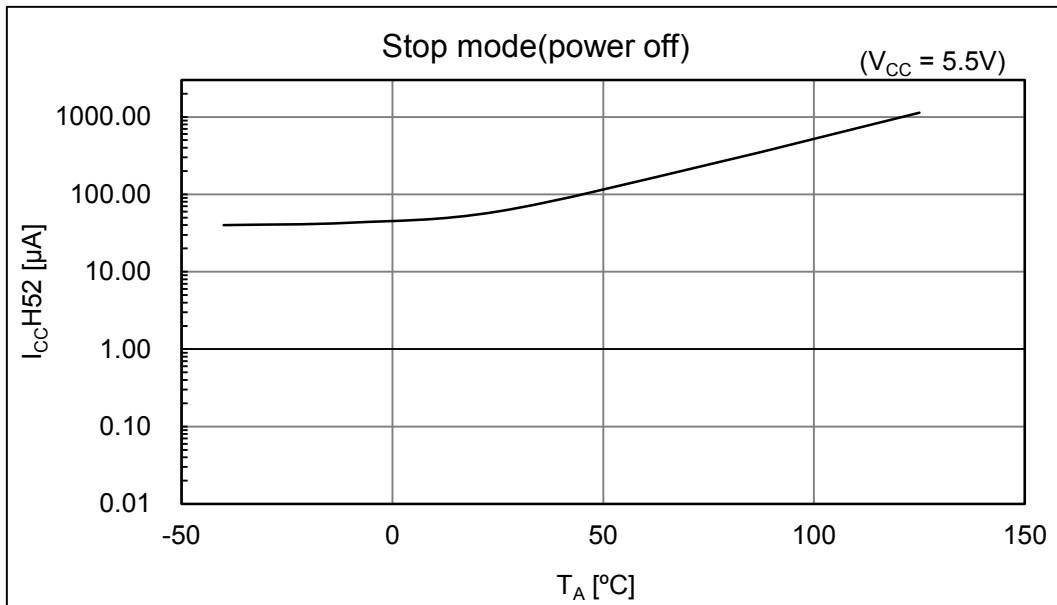
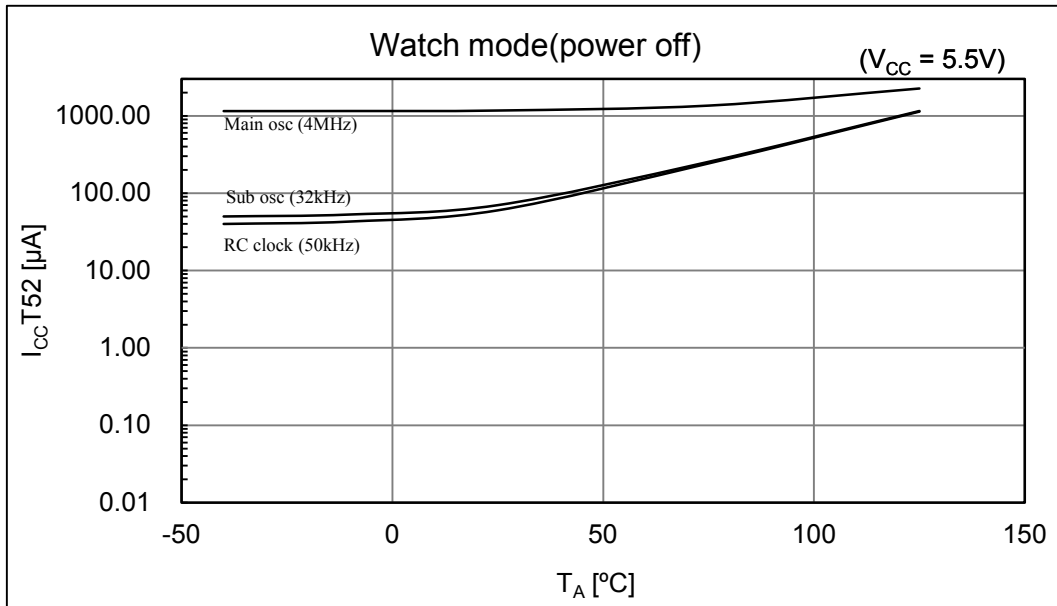
17. Example Characteristics

This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.





·MB91F528



18. Ordering Information MB91F52xxx^C*¹

Part number	Sub clock	CSV Initial value	LVD Initial value	Package* ²
MB91F528YWCPB	Yes	ON	ON	PAB•416 pin, Plastic
MB91F528YYCPB			OFF	
MB91F528YJCPB		OFF	ON	
MB91F528YLCPB			OFF	
MB91F527YWCPB		ON	ON	
MB91F527YYCPB			OFF	
MB91F527YJCPB		OFF	ON	
MB91F527YLCPB			OFF	
MB91F528YSCPB	None	ON	ON	
MB91F528YUCPB			OFF	
MB91F528YHCPB		OFF	ON	
MB91F528YKCPB			OFF	
MB91F527YSCPB		ON	ON	
MB91F527YUCPB			OFF	
MB91F527YHCPB		OFF	ON	
MB91F527YKCPB			OFF	
MB91F528MWCPMC	Yes	ON	ON	LQR•208 pin, Plastic
MB91F528MYCPMC			OFF	
MB91F528MJCPMC		OFF	ON	
MB91F528MLCPMC			OFF	
MB91F527MWCPMC		ON	ON	
MB91F527MYCPMC			OFF	
MB91F527MJCPMC		OFF	ON	
MB91F527MLCPMC			OFF	
MB91F528MSCPMC	None	ON	ON	
MB91F528MUCPMC			OFF	
MB91F528MHCPMC		OFF	ON	
MB91F528MKCPMC			OFF	
MB91F527MSCPMC		ON	ON	
MB91F527MUCPMC			OFF	
MB91F527MHCPMC		OFF	ON	
MB91F527MKCPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F528UWCPMC	Yes	ON	ON	LQP•176 pin, Plastic
MB91F528UYCPMC			OFF	
MB91F528UJCPMC		OFF	ON	
MB91F528ULCPMC			OFF	
MB91F527UWCPMC		ON	ON	
MB91F527UYCPMC			OFF	
MB91F527UJCPMC		OFF	ON	
MB91F527ULCPMC			OFF	
MB91F528USCPMC	None	ON	ON	
MB91F528UUCPMC			OFF	
MB91F528UHCPMC		OFF	ON	
MB91F528UKCPMC			OFF	
MB91F527USCPMC		ON	ON	
MB91F527UUCPMC			OFF	
MB91F527UHCPMC		OFF	ON	
MB91F527UKCPMC			OFF	
MB91F528RWCPMC	Yes	ON	ON	LQS•144 pin, (Lead pitch 0.5mm) Plastic
MB91F528RYCPMC			OFF	
MB91F528RJCPMC		OFF	ON	
MB91F528RLCPMC			OFF	
MB91F527RWCPMC		ON	ON	
MB91F527RYCPMC			OFF	
MB91F527RJCPMC		OFF	ON	
MB91F527RLCPMC			OFF	
MB91F528RSCPMC	None	ON	ON	
MB91F528RUCPMC			OFF	
MB91F528RHCPMC		OFF	ON	
MB91F528RKCPMC			OFF	
MB91F527RSCPMC		ON	ON	
MB91F527RUCPMC			OFF	
MB91F527RHCPMC		OFF	ON	
MB91F527RKCPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F528RWCPMC1	Yes	ON	ON	LQN•144 pin, (Lead pitch 0.4mm) Plastic
MB91F528RYCPMC1			OFF	
MB91F528RJCPMC1		OFF	ON	
MB91F528RLCPMC1			OFF	
MB91F527RWCPMC1		ON	ON	
MB91F527RYCPMC1			OFF	
MB91F527RJCPMC1		OFF	ON	
MB91F527RLCPMC1			OFF	
MB91F528RSCPMC1	None	ON	ON	
MB91F528RUCPMC1			OFF	
MB91F528RHCPMC1		OFF	ON	
MB91F528RKCPMC1			OFF	
MB91F527RSCPMC1		ON	ON	
MB91F527RUCPMC1			OFF	
MB91F527RHCPMC1		OFF	ON	
MB91F527RKCPMC1			OFF	
MB91F528MWCEQ	Yes	ON	ON	LER•208 pin, Plastic
MB91F528MYCEQ			OFF	
MB91F528MJCEQ		OFF	ON	
MB91F528MLCEQ			OFF	
MB91F527MWCEQ		ON	ON	
MB91F527MYCEQ			OFF	
MB91F527MJCEQ		OFF	ON	
MB91F527MLCEQ			OFF	
MB91F528MSCEQ	None	ON	ON	
MB91F528MUCEQ			OFF	
MB91F528MHCEQ		OFF	ON	
MB91F528MKCEQ			OFF	
MB91F527MSCEQ		ON	ON	
MB91F527MUCEQ			OFF	
MB91F527MHCEQ		OFF	ON	
MB91F527MKCEQ			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package* ²
MB91F528UWCEQ	Yes	ON	ON	LEP•176 pin, Plastic
MB91F528UYCEQ			OFF	
MB91F528UJCEQ		OFF	ON	
MB91F528ULCEQ			OFF	
MB91F527UWCEQ		ON	ON	
MB91F527UYCEQ			OFF	
MB91F527UJCEQ		OFF	ON	
MB91F527ULCEQ			OFF	
MB91F528USCEQ	None	ON	ON	
MB91F528UUCEQ			OFF	
MB91F528UHCEQ		OFF	ON	
MB91F528UKCEQ			OFF	
MB91F527USCEQ		ON	ON	
MB91F527UUCEQ			OFF	
MB91F527UHCEQ		OFF	ON	
MB91F527UKCEQ			OFF	
MB91F528RWCEQ	Yes	ON	ON	LEx•144 pin, Plastic
MB91F528RYCEQ			OFF	
MB91F528RJCEQ		OFF	ON	
MB91F528RLCEQ			OFF	
MB91F527RWCEQ		ON	ON	
MB91F527RYCEQ			OFF	
MB91F527RJCEQ		OFF	ON	
MB91F527RLCEQ			OFF	
MB91F528RSCEQ	None	ON	ON	
MB91F528RUCEQ			OFF	
MB91F528RHCEQ		OFF	ON	
MB91F528RKCEQ			OFF	
MB91F527RSCEQ		ON	ON	
MB91F527RUCEQ			OFF	
MB91F527RHCEQ		OFF	ON	
MB91F527RKCEQ			OFF	

*1: It is only supported for customers who have already adopted it now. We do not recommend adopting new products.

*2: For details of the package, see "■ PACKAGE DIMENSIONS".

19. Ordering Information MB91F52xxxD

Part number	Sub clock	CSV Initial value	LVD Initial value	Package* ¹
MB91F528YWDPB	Yes	ON	ON	PAB • 416 pin, Plastic)
MB91F528YJDPB		OFF	ON	
MB91F527YWDPB		ON	ON	
MB91F527YJDPB		OFF	ON	
MB91F528YSDPB	None	ON	ON	
MB91F528YHDPB		OFF	ON	
MB91F527YSDPB		ON	ON	
MB91F527YHDPB		OFF	ON	

MB91F528MWDPMC	Yes	ON	ON	LQR • 208 pin, Plastic
MB91F528MJDPMC		OFF	ON	
MB91F527MWDPMC		ON	ON	
MB91F527MJDPMC		OFF	ON	
MB91F528MSDPMC	None	ON	ON	
MB91F528MHDPMC		OFF	ON	
MB91F527MSDPMC		ON	ON	
MB91F527MHDPMC		OFF	ON	

MB91F528UWDPMC	Yes	ON	ON	LQP • 176 pin, Plastic
MB91F528UJDPMC		OFF	ON	
MB91F527UWDPMC		ON	ON	
MB91F527UJDPMC		OFF	ON	
MB91F528USDPMC	None	ON	ON	
MB91F528UHDPMC		OFF	ON	
MB91F527USDPMC		ON	ON	
MB91F527UHDPMC		OFF	ON	

MB91F528RWDPMC	Yes	ON	ON	LQS • 144 pin, (Lead pitch 0.5mm) Plastic
MB91F528RJDPMC		OFF	ON	
MB91F527RWDPMC		ON	ON	
MB91F527RJDPMC		OFF	ON	
MB91F528RSDPMC	None	ON	ON	
MB91F528RHDPMC		OFF	ON	
MB91F527RSDPMC		ON	ON	
MB91F527RHDPMC		OFF	ON	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package* ¹
MB91F528RWDPMC1	Yes	ON	ON	LQN • 144 pin, (Lead pitch 0.4mm) Plastic
MB91F528RJDPMC1		OFF	ON	
MB91F527RWDPMC1		ON	ON	
MB91F527RJDPMC1		OFF	ON	
MB91F528RSDPMC1	None	ON	ON	
MB91F528RHDPMC1		OFF	ON	
MB91F527RSDPMC1		ON	ON	
MB91F527RHDPMC1		OFF	ON	

MB91F528MWDEQ	Yes	ON	ON	LER • 208 pin, Plastic
MB91F528MJDEQ		OFF	ON	
MB91F527MWDEQ		ON	ON	
MB91F527MJDEQ		OFF	ON	
MB91F528MSDEQ	None	ON	ON	
MB91F528MHDEQ		OFF	ON	
MB91F527MSDEQ		ON	ON	
MB91F527MHDEQ		OFF	ON	

MB91F528UWDEQ	Yes	ON	ON	LEP • 176 pin, Plastic
MB91F528UJDEQ		OFF	ON	
MB91F527UWDEQ		ON	ON	
MB91F527UJDEQ		OFF	ON	
MB91F528USDEQ	None	ON	ON	
MB91F528UHDEQ		OFF	ON	
MB91F527USDEQ		ON	ON	
MB91F527UHDEQ		OFF	ON	

MB91F528RWDEQ	Yes	ON	ON	LES • 144 pin, Plastic
MB91F528RJDEQ		OFF	ON	
MB91F527RWDEQ		ON	ON	
MB91F527RJDEQ		OFF	ON	
MB91F528RSDEQ	None	ON	ON	
MB91F528RHDEQ		OFF	ON	
MB91F527RSDEQ		ON	ON	
MB91F527RHDEQ		OFF	ON	

20. Ordering Information MB91F52xxxE

Part number	Sub clock	CSV Initial value	LVD Initial value	Package* ¹
MB91F528YWEPB	Yes	ON	ON	PAB • 416 pin, Plastic)
MB91F528YJEPB		OFF	ON	
MB91F527YWEPB		ON	ON	
MB91F527YJEPB		OFF	ON	
MB91F528YSEPB	None	ON	ON	
MB91F528YHEPB		OFF	ON	
MB91F527YSEPB		ON	ON	
MB91F527YHEPB		OFF	ON	

MB91F528MWEPMC	Yes	ON	ON	LQR • 208 pin, Plastic
MB91F528MJEPMC		OFF	ON	
MB91F527MWEPMC		ON	ON	
MB91F527MJEPMC		OFF	ON	
MB91F528MSEPMC	None	ON	ON	
MB91F528MHEPMC		OFF	ON	
MB91F527MSEPMC		ON	ON	
MB91F527MHEPMC		OFF	ON	

MB91F528UWEPMC	Yes	ON	ON	LQP • 176 pin, Plastic
MB91F528UJEPMC		OFF	ON	
MB91F527UWEPMC		ON	ON	
MB91F527UJEPMC		OFF	ON	
MB91F528USEPMC	None	ON	ON	
MB91F528UHEPMC		OFF	ON	
MB91F527USEPMC		ON	ON	
MB91F527UHEPMC		OFF	ON	

MB91F528RWEPMC	Yes	ON	ON	LQS • 144 pin, (LeaE pitch 0.5mm) Plastic
MB91F528RJEPMC		OFF	ON	
MB91F527RWEPMC		ON	ON	
MB91F527RJEPMC		OFF	ON	
MB91F528RSEPMC	None	ON	ON	
MB91F528RHEPMC		OFF	ON	
MB91F527RSEPMC		ON	ON	
MB91F527RHEPMC		OFF	ON	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*1
MB91F528RWEPMC1	Yes	ON	ON	LQN • 144 pin, (LeaE pitch 0.4mm) Plastic
MB91F528RJEPMC1		OFF	ON	
MB91F527RWEPMC1		ON	ON	
MB91F527RJEPMC1		OFF	ON	
MB91F528RSEPMC1	None	ON	ON	
MB91F528RHEPMC1		OFF	ON	
MB91F527RSEPMC1		ON	ON	
MB91F527RHEPMC1		OFF	ON	

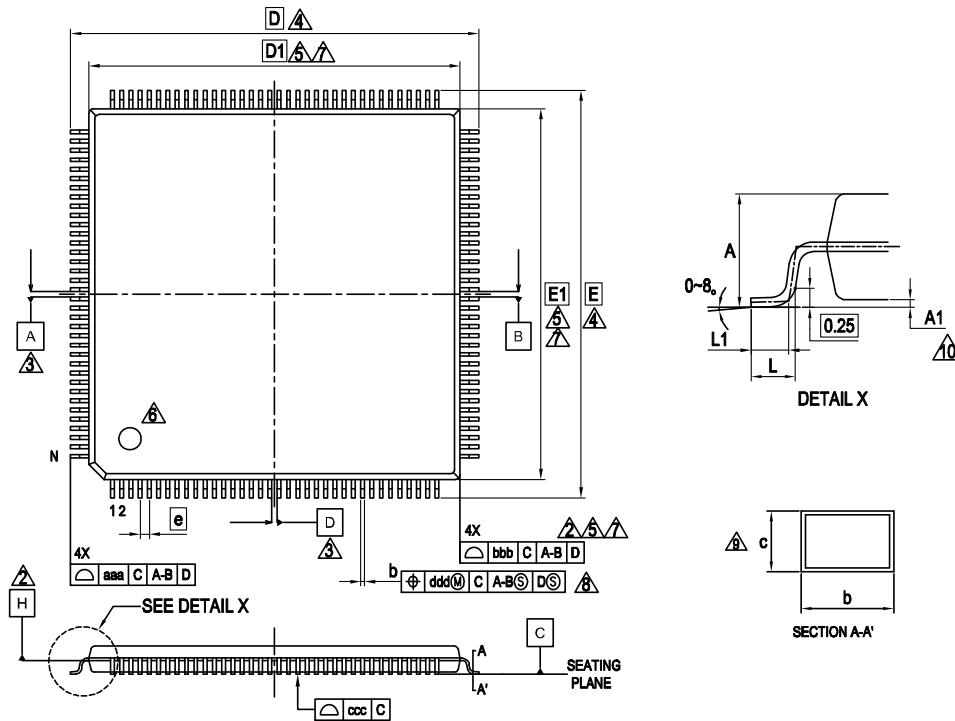
MB91F528MWEEQ	Yes	ON	ON	LER • 208 pin, Plastic
MB91F528MJEEQ		OFF	ON	
MB91F527MWEEQ		ON	ON	
MB91F527MJEEQ		OFF	ON	
MB91F528MSEEQ	None	ON	ON	
MB91F528MHIEQ		OFF	ON	
MB91F527MSEEQ		ON	ON	
MB91F527MHIEQ		OFF	ON	

MB91F528UWEEQ	Yes	ON	ON	LEP • 176 pin, Plastic
MB91F528UJIEQ		OFF	ON	
MB91F527UWEEQ		ON	ON	
MB91F527UJIEQ		OFF	ON	
MB91F528USEEQ	None	ON	ON	
MB91F528UHIEQ		OFF	ON	
MB91F527USEEQ		ON	ON	
MB91F527UHIEQ		OFF	ON	

MB91F528RWEEQ	Yes	ON	ON	LES • 144 pin, Plastic
MB91F528RJIEQ		OFF	ON	
MB91F527RWEEQ		ON	ON	
MB91F527RJIEQ		OFF	ON	
MB91F528RSEEQ	None	ON	ON	
MB91F528RHIEQ		OFF	ON	
MB91F527RSEEQ		ON	ON	
MB91F527RHIEQ		OFF	ON	

21. Package Dimensions

LQS144 , 144 Lead Plastic Low Profile Quad Flat Package



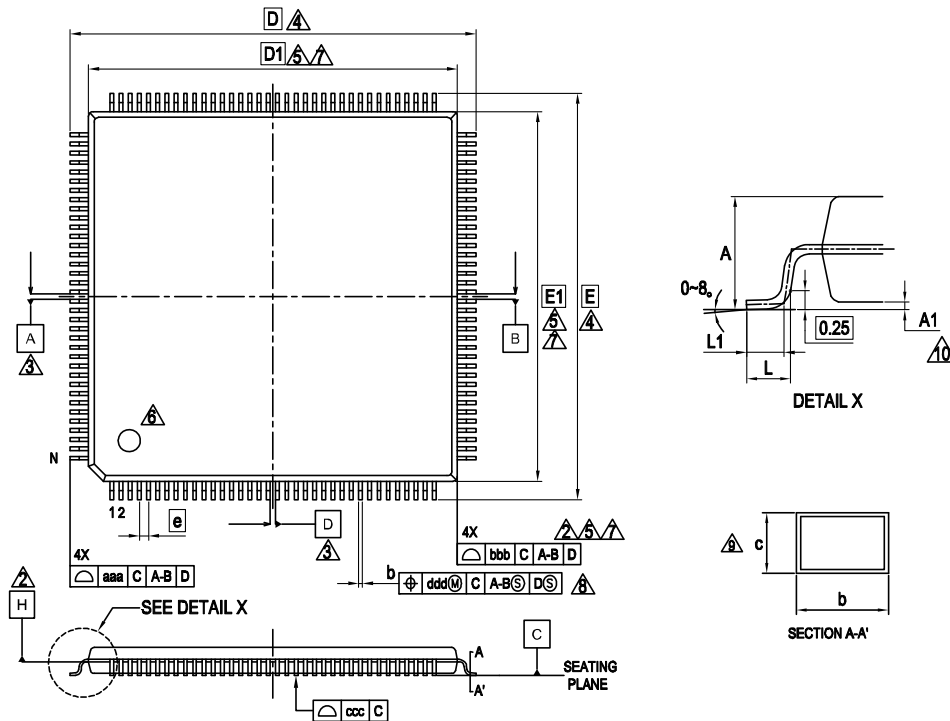
PACKAGE	LQS144		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.25
b	0.17	0.22	0.27
c	0.09	—	0.20
D	22.00 BSC.		
D1	20.00 BSC.		
e	0.50 BSC.		
E	22.00 BSC.		
E1	20.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	144		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
1. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
2. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
3. TO BE DETERMINED AT SEATING PLANE C.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
6. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
9. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

LQN144 , 144 Lead Plastic Low Profile Quad Flat Package



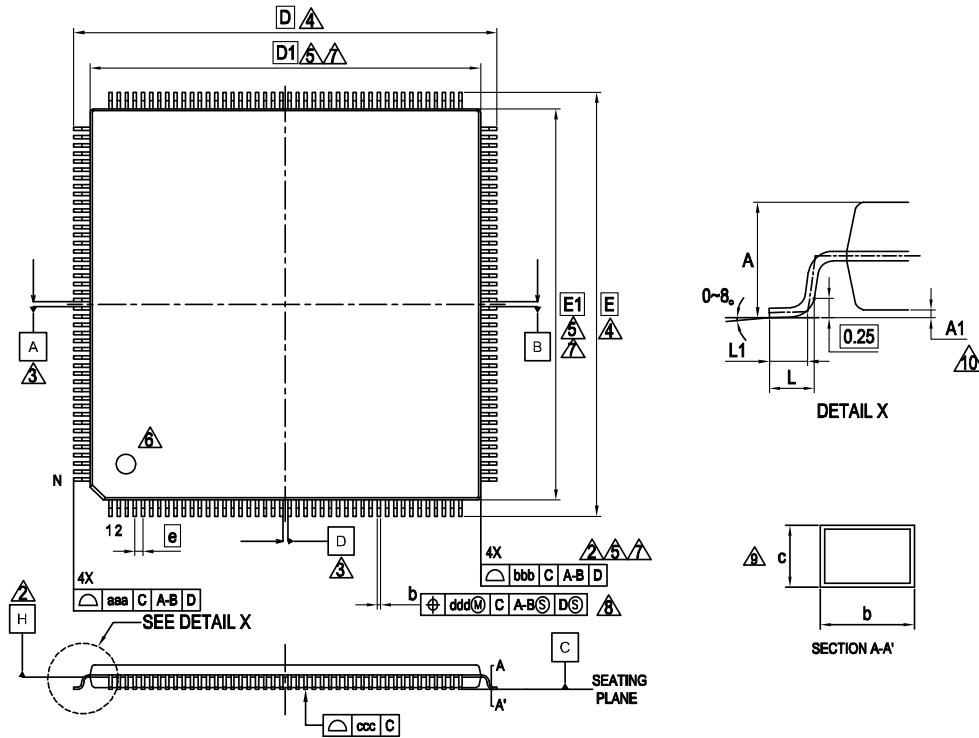
PACKAGE	LQN144		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.145	0.18	0.215
c	0.115	—	0.195
D	18.00 BSC.		
D1	16.00 BSC.		
e	0.40 BSC		
E	18.00 BSC.		
E1	16.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.07
N	144		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBER PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

LQP176 , 176 Lead Plastic Low Profile Quad Flat Package

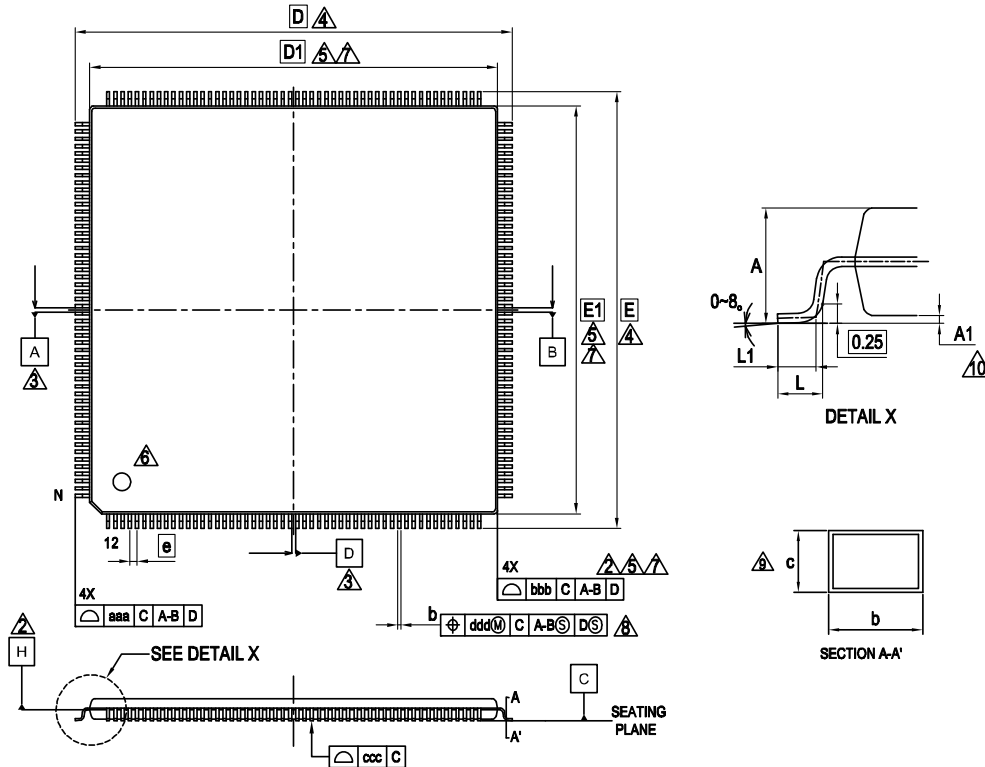


PACKAGE	LQP176		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.17	0.22	0.27
c	0.09	—	0.20
D	26.00 BSC.		
D1	24.00 BSC.		
e	0.50 BSC		
E	26.00 BSC.		
E1	24.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	176		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

LQR208 , 208 Lead Plastic Low Profile Quad Flat Package



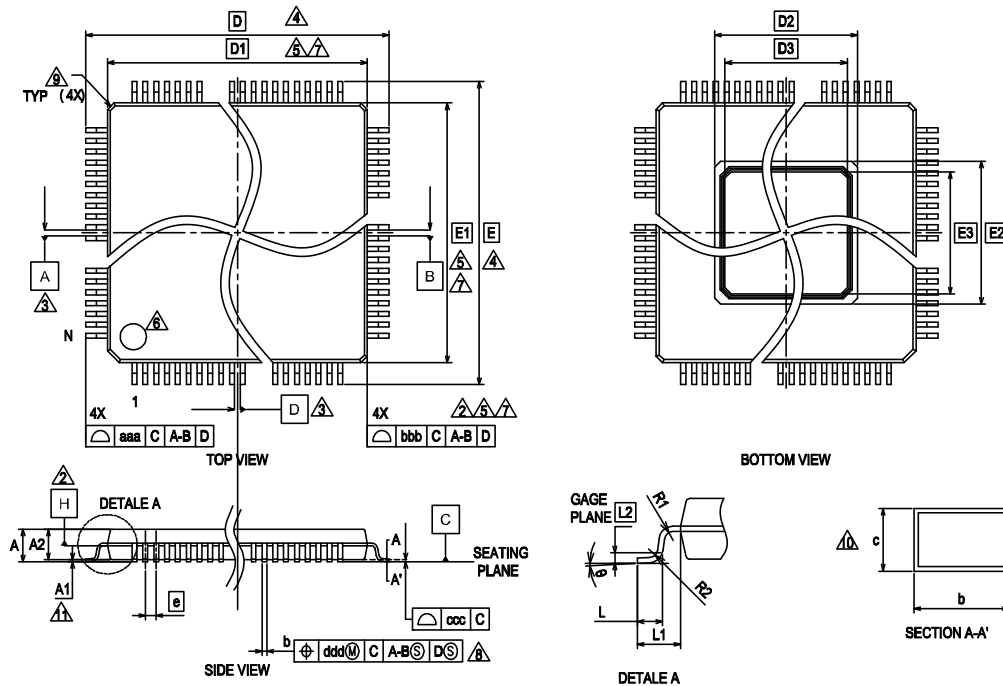
PACKAGE	LQR208		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	30.00 BSC.		
D1	28.00 BSC.		
e	0.50 BSC		
E	30.00 BSC.		
E1	28.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	208		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
- △ DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- △ DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- △ TO BE DETERMINED AT SEATING PLANE C.
- △ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- △ DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- △ REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- △ DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- △ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- △ A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.



LEP176 176PIN ExposedPAD Low Profile Quad Flat Package

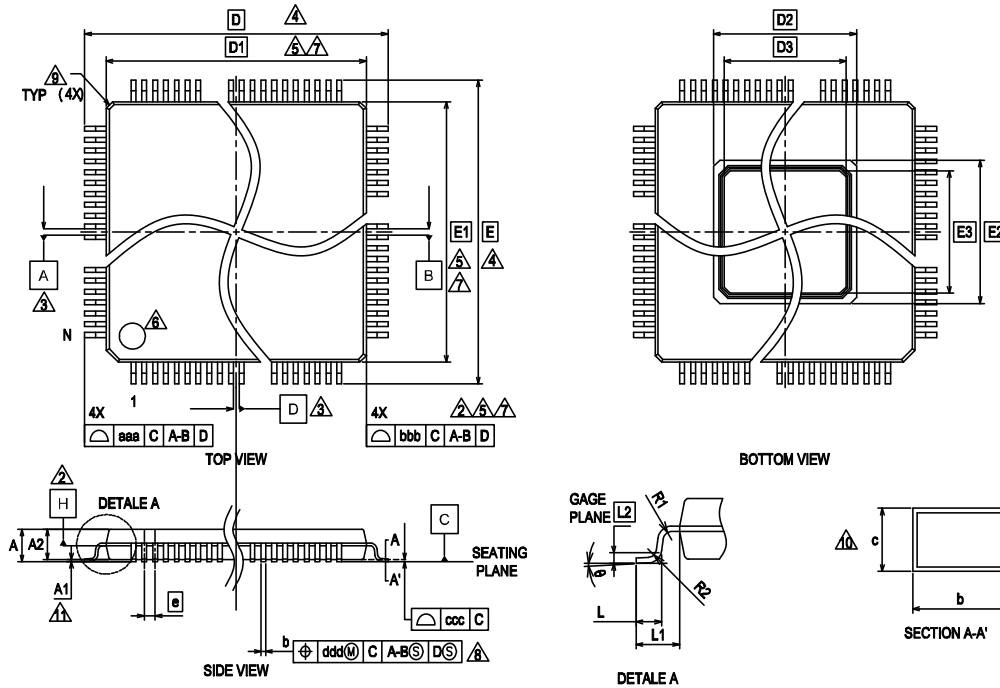


PACKAGE	LEP176			JEDEC	MO-108C		
SYMBOL	MIN.	NOM.	MAX.	SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70	aaa	0.20		
A1	0.00	—	0.20	bbb	0.10		
A2	1.35	1.40	1.45	ccc	0.08		
D	26.00 BSC.			ddd	0.08		
D1	24.00 BSC.			N	176		
D2	9.26 REF						
D3	8.06 REF						
E	26.00 BSC.						
E1	24.00 BSC.						
E2	9.26 REF						
E3	8.06 REF						
R1	0.08	—	—				
R2	0.08	—	0.20				
θ	0°	4°	8°				
c	0.12	—	0.20				
b	0.17	0.22	0.27				
L	0.45	0.60	0.75				
L ₁	1.00 REF						
L ₂	0.25						
e	0.50 BSC.						

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
- △ DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- △ DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- △ TO BE DETERMINED AT SEATING PLANE C.
- △ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- △ DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- △ REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- △ DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBER PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBER CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- △ EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
- △ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- △ A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. B

LER208 208PIN ExposedPAD Low Profile Quad Flat Package

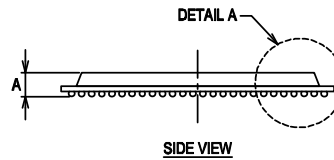
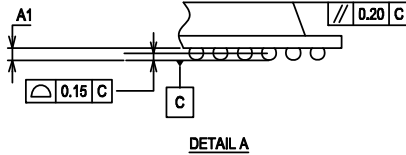
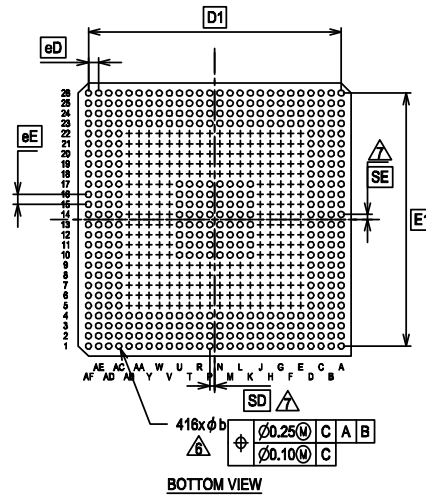
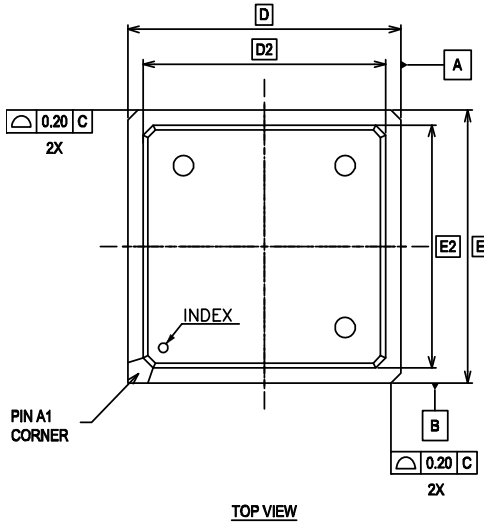


PACKAGE	LER208			JEDEC	MO-108C		
SYMBOL	MIN.	NOM.	MAX.	SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70	aaa	0.20		
A1	0.00	—	0.20	bbb	0.10		
A2	1.35	1.40	1.45	ccc	0.08		
D	30.00 BSC.			ddd	0.08		
D1	28.00 BSC.			N	208		
D2	9.26 REF						
D3	8.06 REF						
E	30.00 BSC.						
E1	28.00 BSC.						
E2	9.26 REF						
E3	8.06 REF						
R1	0.08	—	—				
R2	0.08	—	0.20				
θ	0°	4°	8°				
c	0.12	—	0.20				
b	0.17	0.22	0.27				
L	0.45	0.60	0.75				
L ₁	1.00 REF						
L ₂	0.25						
e	0.50 BSC.						

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBER PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBER CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

PAB416 416 BALL PLASTIC BALL GRID ARRAY PACKAGE



PACKAGE	PAB416			NOTE
SYMBOL	MIN.	NOM.	MAX.	
A	—	—	2.37	PROFILE
A ₁	0.40	0.50	0.60	TERMINAL HEIGHT
D	27.00 BSC			BODY SIZE
E	27.00 BSC			BODY SIZE
D ₂	24.00 BSC			MOLD SIZE
E ₂	24.00 BSC			MOLD SIZE
D ₁	25.00 BSC			MATRIX FOOTPRINT
E ₁	25.00 BSC			MATRIX FOOTPRINT
MD	26			MATRIX SIZE D DIRECTION
ME	26			MATRIX SIZE E DIRECTION
n	416			BALL COUNT
Φb	0.50	0.60	0.70	BALL DIAMETER
eD	1.00 BSC			BALL PITCH
eE	1.00 BSC			BALL PITCH
SD/SE	0.50			SOLDER BALL PLACEMENT
	E5-E22, F5-F22, G5-G22, H5-H22 J5-J22, K5-K9, L18-K22, L5-L9 L18-L22, M5-M9, N18-N22, N5-N9 N18-N22, P5-P9, P18-P22, R5-R9 R18-R22, T5-T9, T18, T22, U5-U9 U18-U22, V5-V22, W5-W22, Y5-Y22 AA5-AA22, AB5-AB22			DEPOPULATED SOLDER BALL LOCATIONS

- DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
- [e] REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2.
- "*" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

Rev. 0A

22. Errata

This section describes the errata for the MB91520 Series. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number
MB91F527R/U/M/Y, MB91F528R/U/M/Y

MB91F527/8 Qualification Status

Product Status: Production

Errata Summary

The following table defines the errata applicability to available MB91520 Series devices.

Items	Part Number	Silicon Revision	Fix Status
[1]. Power-on Conditions is not enough in the Datasheet Specification	MB91F527R/U/M/Y, MB91F528R/U/M/Y	C	Will be fixed in production silicon version D, E
[2]. Limitation for Watch mode (power off)		C, D, E	-

1. Power-on Conditions is not enough in the Datasheet Specification

■ Problem Definition

If the Power-On Reset and Internal Low Voltage Detection are not generated, some port functions will not be available.

■ Parameters Affected

t_{OFF} for Power off time on Power-on Conditions

VCC Power ramp rate on Power-on Conditions

■ Trigger Condition

When the power supply voltage to the MCU has been turned off but has not reached 0 V when the power supply voltage is turned on again, MCU does not generate an internal power-on-reset signal (Power-On reset or Internal LVD reset). Then, some port functions will not be available.

If below condition (1) or (2) or (3) is satisfied, Power-On Reset (Initialization-Reset signal) is generated and no problem occurs.

- (1) The VCC voltage is less than 200 mV for 50 ms or longer (t_{OFF})
- (2) VCC Power ramp rate less than 4 mV/ μ s (dV/dt) until a voltage level for a safe Power-On detection is reached
- (3) C-pin voltage is below 60 mV when VCC is turned on again

■ Scope of Impact

For the affected parts, when the Power-On Reset and Internal Low Voltage Detection are not generated, the MCU may set invalid package and sub clock option information. Therefore, the MCU may operate with an invalid pin configuration.

■ Workaround

For the affected parts, it is necessary to satisfy at least one of the Power-On Reset requirements for any Power-On event as given below:

- (1) The VCC voltage is less than 200 mV for 50 ms or longer (t_{OFF})
- (2) VCC Power ramp rate is less than 4 mV/ μ s (dV/dt) until a voltage level for a safe Power-On detection is reached
- (3) C-pin voltage is below 60 mV when VCC is turned on again

If the customer system does not satisfy the condition above-mentioned, Cypress will release new version D, so Cypress recommends the version D for MB91F52x. The new version prevents the limitation when an external reset signal is asserted at pin RSTX anytime the supply voltage (VCC) is turned on.

■ Fix Status

Will be fixed in production silicon version D, E

2. Limitation for Watch mode (power off)

■ Problem Definition

If the below all trigger conditions (1) to (3) are satisfied, the below registers will be initialized after MCU recovers from watch mode (power off).

■ Trigger Conditions

- (1) Using the watch mode (power off)
 - (2) Interrupt levels that are used as sources for recovering from the watch mode (power off) are '16' to '30', or using NMIX pin as source for recovering from the watch mode (power off)
 - (3) The sources for recovering from the watch mode (power off) are generated between PCLK 1 cycle and PMUCLK 3 cycles (*), after CPU state changes to the watch mode (power off)
- (*): In case of PCLK = 0.5 MHz and PMUCLK = 32 kHz, it is approx. 2 μ s to 100 μ s

■ Scope of Impact

If the all trigger conditions (1) to (3) are satisfied, the below registers will be initialized after MCU recovers from watch mode (power off).

WTCRH, WTCRM, WTCRL
CSELR.SCEN
CMONR.SCRDY
CCRTSELR.CST
CCRTSELR.CSC

■ Workaround

It is necessary to satisfy the below both conditions of (1) and (2).

- (1) Interrupt levels that are used as sources for recovering from the watch mode (power off) are '31', before CPU state changes to the watch mode (power off)
- (2) Don't use NMIX pin as source for recovering from the watch mode (power off)

■ Fix Status

Will not be planned

23. Major Changes

Spanion Publication Number: MB91F528_DS705-00016

Page	Section	Change Results
Revision 1.0		
—	—	Initial release
Cypress Document Number: 002-04669		
Rev *B		
1, 3	Features	Package description modified to JEDEC description.
6, 8, 10, 12	1. Product Lineup	Package description modified to JEDEC description.
53	6. Handling Devices ■ During power-on	<p>The following sentence modified as deleted from Interrupt (Error)</p> <p>To prevent a malfunction of the voltage step-down circuit built in the device, set the voltage rising time to have 50μs or longer (between 0.2V and 2.7V) during power-on.</p> <p>(Correct)</p> <p>To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic increasing during power-on.</p> <p>Power-on prohibits that the voltage goes up and down and voltage rising stops temporarily.</p>
146, 150, 154, 158	10. Interrupt Vector Table	<p>The following sentence deleted from Interrupt vector table.</p> <p>*number up corrected.</p> <p>(Error)</p> <p>*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</p>
160	11. Electrical Characteristics Absolute Maximum Ratings	*10 to *12: Package description modified to JEDEC description.
166	13. DC Characteristics Pull-up resistance	The following pin name deleted from R _{UP3} . P073, P074, P077
169	14. AC Characteristics (1) Main Clock Timing	*3 and *4: Package description modified to JEDEC description.
172	14. AC Characteristics (2) Reset Input	Added the At power-on ² condition to the remarks in Reset input time.
174	14. AC Characteristics (3) Power-on Conditions	<p>Deleted the Slope detection undetected specification.</p> <p>Added the Power ramp rate and C pin voltage at Power-on.</p> <p>*1, *2: Changed the sentence.</p> <p>Added *3, *4, Note, Figure at the Power off time, Power ramp rate, C pin voltage at Power-on.</p>
217 to 220	18. Ordering Information	Package description modified to JEDEC description.
221, 222	19. Ordering Information	<p>Added the following description.</p> <p>■ ORDERING INFORMATION MB91F52xxxD</p>
223 to 230	20. Package Dimensions	Package description modified to JEDEC description.

Page	Section	Change Results				
Rev *C						
5	Features Peripheral Functions	<p>The following sentence modified in I2C as following:</p> <p>(Error) < I2C > 10 channels (ch.3, ch.4, ch.12 to ch.19) Standard mode / High-speed mode supported</p> <p>Standard mode (Max. 100kbps) / High-speed mode (Max. 400kbps) supported</p> <p>(Correct) < I2C > 10 channels (ch.3, ch.4, ch.12 to ch.19) Standard mode / Fast mode supported</p> <p>Standard mode (Max. 100kbps) / Fast mode (Max. 400kbps) supported</p>				
5	1. Product Lineup	<p>The following *3 added as follows:</p> <p>(Error)</p> <table><tr><td>Multi-Function Serial</td><td>12 channels</td></tr></table> <p>(Correct)</p> <table><tr><td>Multi-Function Serial</td><td>12 channels *3</td></tr></table>	Multi-Function Serial	12 channels	Multi-Function Serial	12 channels *3
Multi-Function Serial	12 channels					
Multi-Function Serial	12 channels *3					
6	1. Product Lineup	<p>The following *4 added as follows:</p> <p>(Error)</p> <table><tr><td>Power supply</td><td>2.7 V to 5.5 V</td></tr></table> <p>(Correct)</p> <table><tr><td>Power supply</td><td>2.7 V to 5.5 V *4</td></tr></table>	Power supply	2.7 V to 5.5 V	Power supply	2.7 V to 5.5 V *4
Power supply	2.7 V to 5.5 V					
Power supply	2.7 V to 5.5 V *4					
6	1. Product Lineup	<p>The following sentence added as follows:</p> <p>(Correct) *3: Only channel 3 and channel 4 support the I²C (fast mode/standard mode). Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I²C (standard mode). *4: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.</p>				

Page	Section	Change Results				
7	1. Product Lineup	<p>The following *2 added as follows:</p> <p>(Error)</p> <table><tr><td>Multi-Function Serial</td><td>12 channels</td></tr></table> <p>(Correct)</p> <table><tr><td>Multi-Function Serial</td><td>12 channels *2</td></tr></table>	Multi-Function Serial	12 channels	Multi-Function Serial	12 channels *2
Multi-Function Serial	12 channels					
Multi-Function Serial	12 channels *2					
8	1. Product Lineup	<p>The following *3 added as follows:</p> <p>(Error)</p> <table><tr><td>Power supply</td><td>2.7 V to 5.5 V</td></tr></table> <p>(Correct)</p> <table><tr><td>Power supply</td><td>2.7 V to 5.5 V *3</td></tr></table>	Power supply	2.7 V to 5.5 V	Power supply	2.7 V to 5.5 V *3
Power supply	2.7 V to 5.5 V					
Power supply	2.7 V to 5.5 V *3					
8	1. Product Lineup	<p>The following sentence added as follows:</p> <p>(Correct)</p> <p>*2: Only channel 3 and channel 4 support the I²C (high-speed mode/standard mode). Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I²C (standard mode).</p> <p>*3: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.</p>				
9	1. Product Lineup	<p>The following *2 added as follows:</p> <p>(Error)</p> <table><tr><td>Multi-Function Serial</td><td>20 channels</td></tr></table> <p>(Correct)</p> <table><tr><td>Multi-Function Serial</td><td>20 channels *2</td></tr></table>	Multi-Function Serial	20 channels	Multi-Function Serial	20 channels *2
Multi-Function Serial	20 channels					
Multi-Function Serial	20 channels *2					
10	1. Product Lineup	<p>The following *3 added as follows:</p> <p>(Error)</p> <table><tr><td>Power supply</td><td>2.7 V to 5.5 V</td></tr></table> <p>(Correct)</p> <table><tr><td>Power supply</td><td>2.7 V to 5.5 V *3</td></tr></table>	Power supply	2.7 V to 5.5 V	Power supply	2.7 V to 5.5 V *3
Power supply	2.7 V to 5.5 V					
Power supply	2.7 V to 5.5 V *3					

Page	Section	Change Results				
10	1. Product Lineup	<p>The following sentence added as follows:</p> <p>(Correct)</p> <p>*2: Only channel 3, channel 4 and channel 12 to channel 19 support the I²C (high-speed mode/standard mode). Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I²C (standard mode)</p> <p>*3: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.</p>				
11	1. Product Lineup	<p>The following *1 added as follows:</p> <p>(Error)</p> <table><tr><td>Multi-Function Serial</td><td>20 channels</td></tr></table> <p>(Correct)</p> <table><tr><td>Multi-Function Serial</td><td>20 channels^{*1}</td></tr></table>	Multi-Function Serial	20 channels	Multi-Function Serial	20 channels ^{*1}
Multi-Function Serial	20 channels					
Multi-Function Serial	20 channels ^{*1}					
12	1. Product Lineup	<p>The following *2 added as follows:</p> <p>(Error)</p> <table><tr><td>Power supply</td><td>2.7 V to 5.5 V</td></tr></table> <p>(Correct)</p> <table><tr><td>Power supply</td><td>2.7 V to 5.5 V^{*2}</td></tr></table>	Power supply	2.7 V to 5.5 V	Power supply	2.7 V to 5.5 V ^{*2}
Power supply	2.7 V to 5.5 V					
Power supply	2.7 V to 5.5 V ^{*2}					
12	1. Product Lineup	<p>The following sentence added as follows:</p> <p>(Correct)</p> <p>*1: Only channel 3, channel 4 and channel 12 to channel 19 support the I²C (high-speed mode/standard mode). Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I²C (standard mode).</p> <p>*2: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.</p>				
13	1. Product Lineup	Added silicon version E				

Page	Section	Change Results
53	■During Power-on	<p>The following sentence modified as following:</p> <p>(Error) To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic increasing during power-on. Power-on prohibits that the voltage goes up and down and voltage rising stops temporarily.</p> <p>(Correct) To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic during power-on.</p>
163	12. Electrical Characteristics Recommended operating conditions	<p>The following sentence modified as following:</p> <p>(Error) *1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. Moreover, minimum value with an effective external low-voltage detection reset becomes a voltage until generating low-voltage detection reset.</p> <p>(Correct) *1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.</p>
178, 179	14. AC Characteristics	Added (3-2) Power-on Conditions for MB91F52xxxE

Page	Section	Change Results																																				
204	14. AC Characteristics (4) Multi-function Serial (4-4) I ² C timing	<p>The following sentence modified as following:</p> <p>(Error)</p> <table><tr><th colspan="2">High-speed mode^{*3}</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Max</th></tr><tr><td></td><td></td><td></td><td></td></tr></table> <p>Notes: Only ch.3, ch.4 and ch.12-ch.19 are standard mode/ high-speed mode correspondence.</p> <p>*3: A high-speed mode I²C bus device can be used</p> <p>(Correct)</p> <table><tr><th colspan="2">Fast mode^{*3}</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Max</th></tr><tr><td></td><td></td><td></td><td></td></tr></table> <p>Notes: Only ch.3, ch.4 and ch.12-ch.19 are standard mode/ fast mode correspondence.</p> <p>*3: A fast mode I²C bus device can be used</p>	High-speed mode ^{*3}		Unit	Remarks	Min	Max					Fast mode ^{*3}		Unit	Remarks	Min	Max																				
High-speed mode ^{*3}		Unit	Remarks																																			
Min	Max																																					
Fast mode ^{*3}		Unit	Remarks																																			
Min	Max																																					
208	14. AC Characteristics (8) Low voltage detection (External low-voltage detection)	<p>The following sentence modified in the Detection voltage as following:</p> <p>(Error)</p> <table><tr><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>2.7</td><td>-</td><td>5.5</td><td>V</td><td></td></tr><tr><td>-8%</td><td>2.8</td><td>+8%</td><td>V</td><td>When power-supply voltage falls and detection level is set initially</td></tr></table> <p>(Correct)</p> <table><tr><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>2.7</td><td>-</td><td>5.5</td><td>V</td><td></td></tr><tr><td>-8%</td><td>LVD5F SEL [3:0]</td><td>+8%</td><td>V</td><td>LVD5F_SEL[3:0] are programmable. Refer to the hardware manual.</td></tr></table>	Value			Unit	Remarks	Min	Typ	Max	2.7	-	5.5	V		-8%	2.8	+8%	V	When power-supply voltage falls and detection level is set initially	Value			Unit	Remarks	Min	Typ	Max	2.7	-	5.5	V		-8%	LVD5F SEL [3:0]	+8%	V	LVD5F_SEL[3:0] are programmable. Refer to the hardware manual.
Value			Unit	Remarks																																		
Min	Typ	Max																																				
2.7	-	5.5	V																																			
-8%	2.8	+8%	V	When power-supply voltage falls and detection level is set initially																																		
Value			Unit	Remarks																																		
Min	Typ	Max																																				
2.7	-	5.5	V																																			
-8%	LVD5F SEL [3:0]	+8%	V	LVD5F_SEL[3:0] are programmable. Refer to the hardware manual.																																		
208	14. AC Characteristics (9) Low voltage detection (RAM retention low-voltage detection)	<p>The following sentence modified as following:</p> <p>(Error)</p> <p>(9) Low voltage detection (Internal low-voltage detection)</p> <p>(Correct)</p> <p>(9) Low voltage detection (RAM retention low-voltage detection)</p>																																				

Page	Section	Change Results
231, 232	20. Ordering Information	Added the following description. ■ORDERING INFORMATION MB91F52xxxE
Rev *D		
2	Features	<p>The following sentence should be modified as follows:</p> <p>(Error) Conversion time : 1μs</p> <p>(Correct) Conversion time : 1.4μs</p>
6	1. Product Lineup	<p>The following sentence should be modified as follows:</p> <p>(Error) *4: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.</p> <p>(Correct) *4: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.</p>

Page	Section	Change Results
8, 10	1. Product Lineup	<p>The following sentence should be modified as follows:</p> <p>(Error)</p> <p>*3: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.</p> <p>*3: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.</p>
12	1. Product Lineup	<p>The following sentence should be modified as follows:</p> <p>(Correct)</p> <p>*2: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.</p> <p>*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.</p>

Page	Section	Change Results
163	12. Electrical Characteristics Recommended operating conditions	<p>The following sentence should be modified as follows:</p> <p>(Error)</p> <p>*1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.</p> <p>(Correct)</p> <p>*1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative. The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.</p>
168	11. Electrical Characteristics DC Characteristics	<p>Pin name of R_{UP3} should be modified as follows:</p> <p>(Error)</p> <p>Port pin other than P035,041,093,122,222,227,232,236</p> <p>(Correct)</p> <p>Port pin other than P035,041,073,074,077,093,122,222,227,232,236</p>
208	11. Electrical Characteristics (8) Low voltage detection (External low-voltage detection)	<p>Note of Detection voltage should be added as follows:</p> <p>(Correct)</p> <p>Detection voltage ^{*3}</p> <p>*3: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage (2.7V). Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.</p>

Page	Section	Change Results
208	11. Electrical Characteristics (9) Low voltage detection (Internal low-voltage detection)	<p>The following sentence modified as following:</p> <p>(Error) (9) Low voltage detection (RAM retention low-voltage detection)</p> <p>(Correct) (9) Low voltage detection (Internal low-voltage detection)</p>
		<p>The following symbol should be modified as follows:</p> <p>(Error) *</p> <p>(Correct) *1</p>
		<p>Note of Detection voltage should be added as follows:</p> <p>(Correct) Detection voltage *2</p> <p>*2: The detection voltage of the internal low voltage detection is 0.9V±0.1V. This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.</p>
241, 242	22. Errata	Limitation for Watch mode (power off) should be added in Errata.

Document History

**Document Title: MB91F527R/MB91F527U/MB91F527M/MB91F527Y/MB91F528R/MB91F528U/MB91F528M/MB91F528Y
32-bit FR81S Microcontroller**

Document Number: 002-04669

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	—	03/28/2014	Initial release
*A	5005210	JHMU	11/16/2015	Updated to Cypress template. Added the following note to the remarks of ""L" level average output current" and ""H" level average output current" in "Absolute Maximum Ratings" of "ELECTRICAL CHARACTERISTICS". *13: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106. *14: Corresponding pins: General-purpose ports of P103, P104, P105 and P106. Added Errata section.
*B	5107086	KUME	01/26/2016	For details, please see the chapter 21. Major Changes.
*C	5196361	KUME	04/28/2016	For details, please see the chapter 23. Major Changes.
*D	5318662	KUME	06/22/2016	For details, please see the chapter 23. Major Changes.



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