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Application Note

MB90560 -

Operation of Waveform Generator

History

18th Nov. 99	MSt	V1.0	New version
01th Mar. 00	MSt	V1.1	Detailed Explanation of STOP bit added

Introduction

The Waveform Generator of MB90560 series generate various waveforms, such as dead-time, GATE- and Timing mode.

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1 Waveform Generator

1.1 Register of Waveform Generator

The register of Waveform Generator are 3x 8-bit reload register, 3x 8 bit timer control register and 1 Waveform control register.

1.1.1 8-bit reload register(TMRR0/1/2)

The 8-bit reload registers are used to store the comparison value. The registers are reloaded when the 8-bit timer is started to operate.
In dead-time mode, these registers set the non-overlap time.
In timer mode, these registers are used to set the GATE time for PPG operation.
One register belongs to two OCU outputs (RTx). For example, TMRR0 to RT0/1.

1.1.2 8-bit timer control register (DTCR0/1/2)

The 8-bit timer control register are used to control the operation mode, interrupt request enable, interrupt request flag, PPG output enable, GATE signal enable and output level polarity the waveform generator.
With one register the settings of two RTs are chosen.

Bit10	Bit9	Bit8	
TMD2	**TMD1**	**TMD0**	**Operation mode bit**
0	0	0	Waveform generator is stopped
0	0	1	PPG timer output pulse while RT signals is ‘H’.
0	1	0	The rising edge of each RT signal will trigger 8 bit timer to start. PPG will run until the 8bit timer stopped(timer mode)
1	0	0	Generate non-overlapped signal by RT signal (dead-time timer mode)
1	1	1	RT signal acts as Gate signal for PPG timers. PPG generates non overlapped signals. (Dead-time timer mode)

Table 1: Note: Operation mode can only be chosen, if PPG in 16-bit mode

Bit11	
TMIE	**Interrupt request enable**
0	Disable interrupt when the 8-bit timer underflow
1	Enable interrupt when the 8-bit timer underflow

Bit12	**Interrupt request flag**	
TMIF	**Read**	**Write**
0	No counter underflow detected	Clear this bit
1	Counter underflow detected	No effect

Bit13	
PGEN	**PPG output enable bit**
0	Disable PPG output
1	Enable PPG out

Bit14	
GTEN	**GATE signal enable bit**
0	Disable GATE signal output (Asynchronous mode)
1	Enable GATE signal output (Synchronous mode)

Bit15	
DMOD	**Output polarity control bit**
0	Positive level output
1	Negative level output

1.1.3 Waveform Control Register (SIGCR)

In the Waveform Control Register the clock frequency, Noise cancelling function selection, DTTI input polarity , DTTI input enable and output selection (RTO,PPG) can be chosen

Bit1	Bit0	**Operation mode**	PPG0-5 output through RTO0-5 table					
PGS1	**PGS0**		**RTO0**	**RTO1**	**RTO2**	**RTO3**	**RTO4**	**RTO5**
0	0	8-bit x 6 ch.	PPG0	PPG1	PPG2	PPG3	PPG4	PPG5
0	1	8-bit x 3 ch.	PPG1	PPG1	PPG3	PPG3	PPG5	PPG5
1	0	8-bit x 2 ch.	PPG1	PPG3	PPG1	PPG3	PPG1	PPG3
1	1	8-bit x 1 ch.	PPG1	PPG1	PPG1	PPG1	PPG1	PPG1

Bit4	Bit3	Bit2	(16MHz clock cycle)
DCK2	**DCK1**	**DCK0**	**Operation clock selection bit**
0	0	0	62.5 ns
0	0	1	125 ns
0	1	0	250 ns
0	1	1	500 ns
1	0	0	1 us
1	0	1	2 us
1	1	0	4 us
1	1	1	Prohibited

Bit5	
NRSL	**Noise cancelling function selection bit**
0	DTTI input is not go thru the noise cancelling circuit
1	DTTI input go thru the noise cancelling circuit

Bit6	
DTIL	**DTTI input polarity selection bit**
0	‘0’ input
1	‘1’ input

Bit7	
DTIE	**DTTI input enable bit**
0	Disable DTTI input
1	Enable DTTI input

2 Operation Modes

2.1 Dead-Timer mode with output compare units

The dead-time control circuit will input the real-time output (RT1/3/5) and the selected PPG timer pulse output , and output an non-overlap signals (inverted signals) to external pins.

2.1.1 Settings

In this mode initialise:

- 16-bit Free-run timer
- Output compare unit
- Waveform Generator

Note: Only the necessary setting will be exclaimed. Standard settings, like internal or external clock is not described.

2.1.2 16-bit Free-run timer

Settings in Timer Control Register (TCCS):

Clock frequency must be set (CLK2-0)
Clear counter SCLR=1
Enable Counter STOP=1

Note: STOP bit should be set to ‘1’ (enable) when everything else is set, because counter start immediately after setting STOP-bit to ‘1’.

It is possible to decrease counting by a “compare clear”. The counter will be set to 0 when value in compare clear register (CPCLR) has matched.
Therefore the clear value is written in compare clear register CPCLR. In Timer Control Register the Compare clear interrupt ICLR=1 is enabled.

2.1.3 Output Compare Units

In dead-timer mode only the OCU1/3/5 are used.
In Compare Register the comparison value must be written.
In Compare control register OCSx the CMOD bit is set to ‘1’, to get the inverse signal.
Compare operation CSTx=1 and output bit OTEx=1 must be enabled.
Even only the RT1/3/5 are used to create dead- time mode. Output of RT0/2/4 have to be enabled. Because the output level are needed from the Waveform Generator.

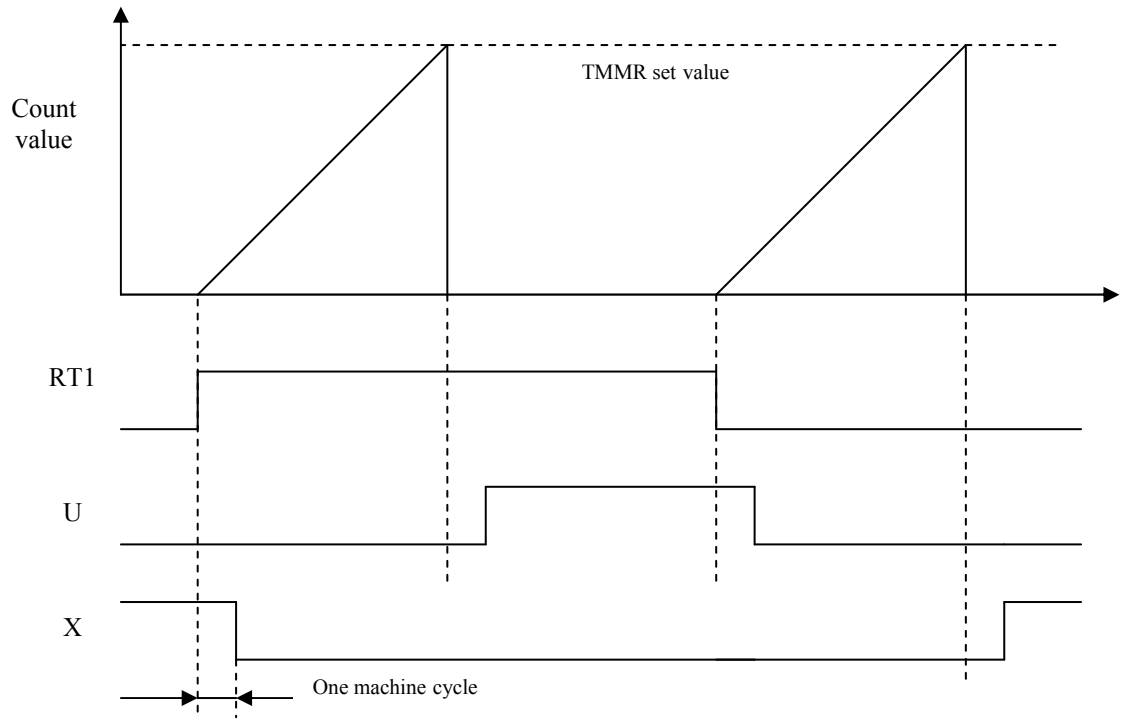
2.1.4 Waveform Generator

The 8-bit reload register must be set (TMRRx).

In Timer Control register (DTCRx) the GATE and PPG output must be disabled. (GTEN=0; PGEN=0).
With bit 15 DMOD positive or negative level output can be chosen. The operation mode Bit8-10 TMD0-2 must be set to 4. (Generate non-overlap signal by RT-signal.) TMD2=1;TMD1=0;TMD0=0;

In Waveform Control register the bits 7 to 5 can stay at initial values. Choose clock frequency by setting bit4 to 2 (DCK2-0).
Bit1 and bit 0 (PGS1, PGS0) can stay at initial values.

Making non-overlap signal by using RT1/3/5 (positive pulse)



Pin name	Output signal
U	Signal with is applied at RT1 rising edge
V	Signal with is applied at RT3 rising edge
W	Signal with is applied at RT5 rising edge
X	Signal with is applied at RT1 falling edge
Y	Signal with is applied at RT3 falling edge
Z	Signal with is applied at RT5 falling edge

Description:

Rising edge of the RT signal:
The 8-bit timer starts to count up. With a delay of one machine cycle the inverted output port (X) chance level to ‘low’.
When counter reach setting value the output pin U change level to ‘High’ with a delay of one machine clock cycle.

Falling edge of RT :
The 8-bit counter starts to count up the values.
With a delay-time of one machine clock cycle, the U signal change level to ‘Low”.
When counter reached compare value, the inverse signal X change level to ‘High’.
(with a delay-time of one machine cycle)

If the RT pulse width is smaller than the set non-overlap time, the 8-bit timer will restart counting from 00hex at the next RT’s edge.

2.2 Dead-Timer mode using PPG

It is possible to create a non-overlap signal by using the PPG.
The signals depend on rising and falling edges of PPG output signal

2.2.1 Settings

In this mode initialise:

- 16-bit free-run timer
- Output compare units
- PPG's
- Waveform Generator

2.2.2 16-bit Free-run timer

Settings in Timer Control Register (TCCS):

Clock frequency must be set (CLK2-0)
Clear counter SCLR=1
Enable Counter STOP=1

Note: STOP bit should be set to '1' (enable) when everything else is set, because counter start immediately after setting STOP-bit to '1'.

In this mode the 16-bit Free-run Timer is used to enable the OCU outport.

2.2.3 Output Compare Units

The output of the OCU's must be enabled, because they generate the output signals RTO0-5. Although only the PPG1/3/5 could be used in this mode, two OCU have to be initialised for each PPG. For example: Using PPG1, outputs of OCU0 and 1 must be enabled.
A compare value is not necessary.

Register settings:

Compare control register OCSx:
Bit12: CMOD=0;
Bit11: OTE1=1;
Bit10: OTE0=1;

2.2.4 PPG's

The PPG must be initialise, because the outputs RTOx depends on PPG-signal.

In PPG Reload Register (PRLH0-5, PRLL0-5) the reload values of the down counter are stored. In upper register PRLH0-5 'High' pulse width and in lower register PRLL0-5 'Low' pulse width is written (positive pulse).

PPG Control Register PPGC0-5:

Bit15: PEN1=1; start operation for PPG1/3/5, writing '0' to this bit will stop PPG
Bit14: SST1=0; PPG1/3/5 will operated when PEN1=1
Bit13: POE1=1; PPG output port for PPG1/3/5
Bit12: PIE1=0; Disable Interrupt request
Bit11: PUF1=0; clear interrupt request flag
Bit10-9: MOD1-0=0; 8-bit PPG, 2ch. independent mode
Bit8: reserved, when setting PPG, set '1' to this bit
Bit7: PEN0=1; start operation for PPG0/2/4, writing '0' to this bit will stop PPG
Bit6: SST0=0; PPG1/3/5 will operated when PEN0=1
Bit5: POE0=1; PPG output port for PPG0/2/4
Bit4: PIE0=0; Disable Interrupt request
Bit3: PUF0=0; clear interrupt request flag
Bit2: POS1=0; select pulse polarity PPG1/3/5('0':positive , '1': negative)
Bit2: POS0=0; select pulse polarity PPG0/2/4('0':positive , '1': negative)
Bit0: reserved, when setting PPG, set '1' to this bit

PPG Clock Control register PCS01/23/45:

The 8-bit PPG Clock Control Register are used to control the operation clock frequency for PPG0-5.In one register are clock settings of two PPG's.
Bit7-5: PC12-PC10 setting of operation clock for PPG1/3/5
Bit4-2: PC02-PC00 setting of operation clock for PPG0/2/4
Bit1, bit0 are not used

PC02	PC01	PC00	Operation clock for ch0/2/4
0	0	0	ϕ (62.5 ns ϕ = 16 MHz)
0	0	1	ϕ /2 (125 ns ϕ = 16 MHz)
0	1	0	ϕ /4 (50 ns ϕ = 16 MHz)
0	1	1	ϕ /8 (500 ns ϕ = 16 MHz)
1	0	0	ϕ /16 (1 µs ϕ = 16 MHz)
1	0	1	ϕ /32 (2 µs ϕ = 16 MHz)
1	1	0	ϕ /64 (4 µs ϕ = 16 MHz)
1	1	1	Input clock from timebase trimmer

PC12	PC11	PC10	Operation clock for ch1/3/5
0	0	0	ϕ (62.5 ns ϕ = 16 MHz)
0	0	1	ϕ /2 (125 ns ϕ = 16 MHz)
0	1	0	ϕ /4 (50 ns ϕ = 16 MHz)
0	1	1	ϕ /8 (500 ns ϕ = 16 MHz)
1	0	0	ϕ /16 (1 µs ϕ = 16 MHz)
1	0	1	ϕ /32 (2 µs ϕ = 16 MHz)
1	1	0	ϕ /64 (4 µs ϕ = 16 MHz)
1	1	1	Input clock from timebase trimmer

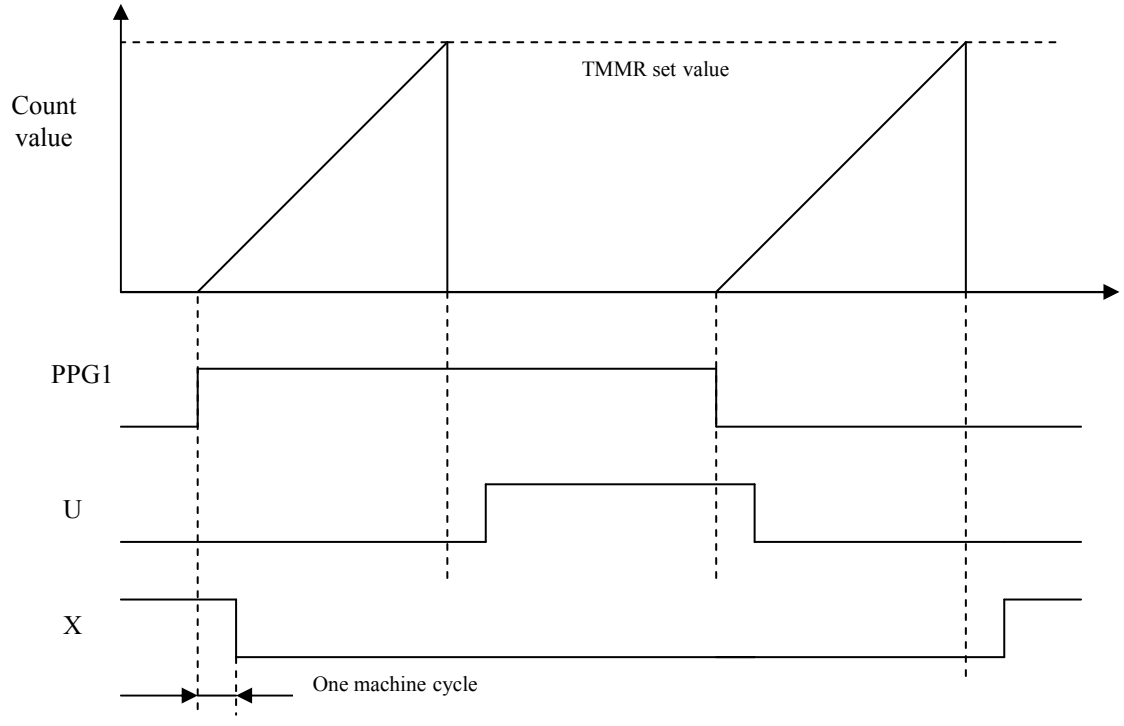
2.2.5 Waveform Generator

The 8-bit reload register must be set (TMRRx).

In Timer Control register (DTCRx) the GATE and PPG output must be enabled. (GTEN=1; PGEN=1).
With bit 15 DMOD positive or negative level output can be chosen. The operation mode Bit8-10 TMD0-2 must be set to ‘7’. (Generate non-overlap signal by PPG-signal.)
TMD2=1;TMD1=1;TMD0=1;

In Waveform Control register the bits 7 to 5 can stay at initial values. Choose clock frequency by setting bit4 to 2 (DCK2-0).
Bit1 and bit 0 (PGS1, PGS0) can stay at initial values.

Making non-overlap signal by using PPG1/3/5 (positive pulse)



Pin name	Output signal
U	Signal with is applied at PPG1 rising edge
V	Signal with is applied at PPG3 rising edge
W	Signal with is applied at PPG5 rising edge
X	Signal with is applied at PPG1 falling edge
Y	Signal with is applied at PPG3 falling edge
Z	Signal with is applied at PPG5 falling edge

Description:

Rising edge of the PPG signal:
The 8-bit timer starts to count up. With a delay of one machine cycle the inverted output port (X) chance level to ‘low’.
When counter reach setting value the output pin U change level to ‘High’ with a delay of one machine clock cycle.

Falling edge of PPG :
The 8-bit counter starts to count up the values.
With a delay-time of one machine clock cycle, the U signal change level to ‘Low”.
When counter reached compare value, the inverse signal X change level to ‘High’. (of course with an delay-time of one machine cycle)

If the PPG pulse width is smaller than the set non-overlap time, the 8-bit timer will restart counting from 00hex at the next edge of PPG.

3 Operation of PPG Output and GATE signal control circuit

It is possible to gate the PPG output. Two methods are available.

- using High-level of RT to gate PPG
- using 8-bit timer to gate PPG

3.1 Gate PPG with a “High’ level of RT

While a High level of RT the PPG signal will be outputted to RTO pin.
RT0 will gate PPG0, RT1 gates PPG1,…

3.1.1 Settings

In this mode initialise:

- 16-bit free-run timer
- Output compare units
- PPG’s
- Waveform Generator

3.1.2 16-bit Free-run timer

Settings in Timer Control Register (TCCS):

Clock frequency must be set (CLK2-0)
Clear counter SCLR=1
Enable Counter STOP=1

Note: STOP bit should be set to ‘1’ (enable) when everything else is set, because counter start immediately after setting STOP-bit to ‘1’.

It is possible to decrease counting by a compare clear. The counter will be set to 0 when value in compare clear register (CPCLR) has matched.
Therefore the clear value is written in compare clear register CPCLR. In Timer Control Register the Compare clear interrupt ICLR=1 is enabled.

3.1.3 Output Compare Units

The compare value must be written into Compare Registers OCCP0-5.

Register settings:

Compare control register OCSx:
Bit12: CMOD=0;
Bit11: OTE1=1;
Bit10: OTE0=1;

3.1.4 PPG's

In PPG Reload Register (PRLH0-5, PRLL0-5) the reload values of the down counter are stored. In upper register PRLH0-5 'High' pulse width and in lower register PRLL0-5 'Low' pulse width is written (positive pulse).

PPG Control Register PPGC0-5:

Bit15: PEN1=1; start operation for PPG1/3/5, writing '0' to this bit will stop PPG
Bit14: SST1=1; PPG1/3/5 will operated when GATE='H'
Bit13: POE1=1; PPG output port for PPG1/3/5
Bit12: PIE1=0; Disable Interrupt request
Bit11: PUF1=0; clear interrupt request flag
Bit10-9: MOD1-0=0; 8-bit PPG, 2ch. independent mode
Bit8: reserved, when setting PPG, set '1' to this bit
Bit7: PEN0=1; start operation for PPG0/2/4, writing '0' to this bit will stop PPG
Bit6: SST0=1; PPG0/2/4 will operated when GATE='H'
Bit5: POE0=1; PPG output port for PPG0/2/4
Bit4: PIE0=0; Disable Interrupt request
Bit3: PUF0=0; clear interrupt request flag
Bit2: POS1=0; select pulse polarity PPG1/3/5('0':positive , '1': negative)
Bit2: POS0=0; select pulse polarity PPG0/2/4('0':positive , '1': negative)
Bit0: reserved, when setting PPG, set '1' to this bit

PPG Clock Control register PCS01/23/45:

The 8-bit PPG Clock Control Register are used to control the operation clock frequency for PPG0-5.In one register are clock settings of two PPG's.
Bit7-5: PC12-PC10 setting of operation clock for PPG1/3/5
Bit4-2: PC02-PC00 setting of operation clock for PPG0/2/4
Bit1, bit0 are not used

PC02	PC01	PC00	Operation clock for ch0/2/4
0	0	0	ϕ (62.5 ns ϕ = 16 MHz)
0	0	1	ϕ /2 (125 ns ϕ = 16 MHz)
0	1	0	ϕ /4 (50 ns ϕ = 16 MHz)
0	1	1	ϕ /8 (500 ns ϕ = 16 MHz)
1	0	0	ϕ /16 (1 µs ϕ = 16 MHz)
1	0	1	ϕ /32 (2 µs ϕ = 16 MHz)
1	1	0	ϕ /64 (4 µs ϕ = 16 MHz)
1	1	1	Input clock from timebase trimmer

PC12	PC11	PC10	Operation clock for ch1/3/5
0	0	0	ϕ (62.5 ns ϕ = 16 MHz)
0	0	1	ϕ /2 (125 ns ϕ = 16 MHz)
0	1	0	ϕ /4 (50 ns ϕ = 16 MHz)
0	1	1	ϕ /8 (500 ns ϕ = 16 MHz)
1	0	0	ϕ /16 (1 µs ϕ = 16 MHz)
1	0	1	ϕ /32 (2 µs ϕ = 16 MHz)
1	1	0	ϕ /64 (4 µs ϕ = 16 MHz)
1	1	1	Input clock from timebase trimmer

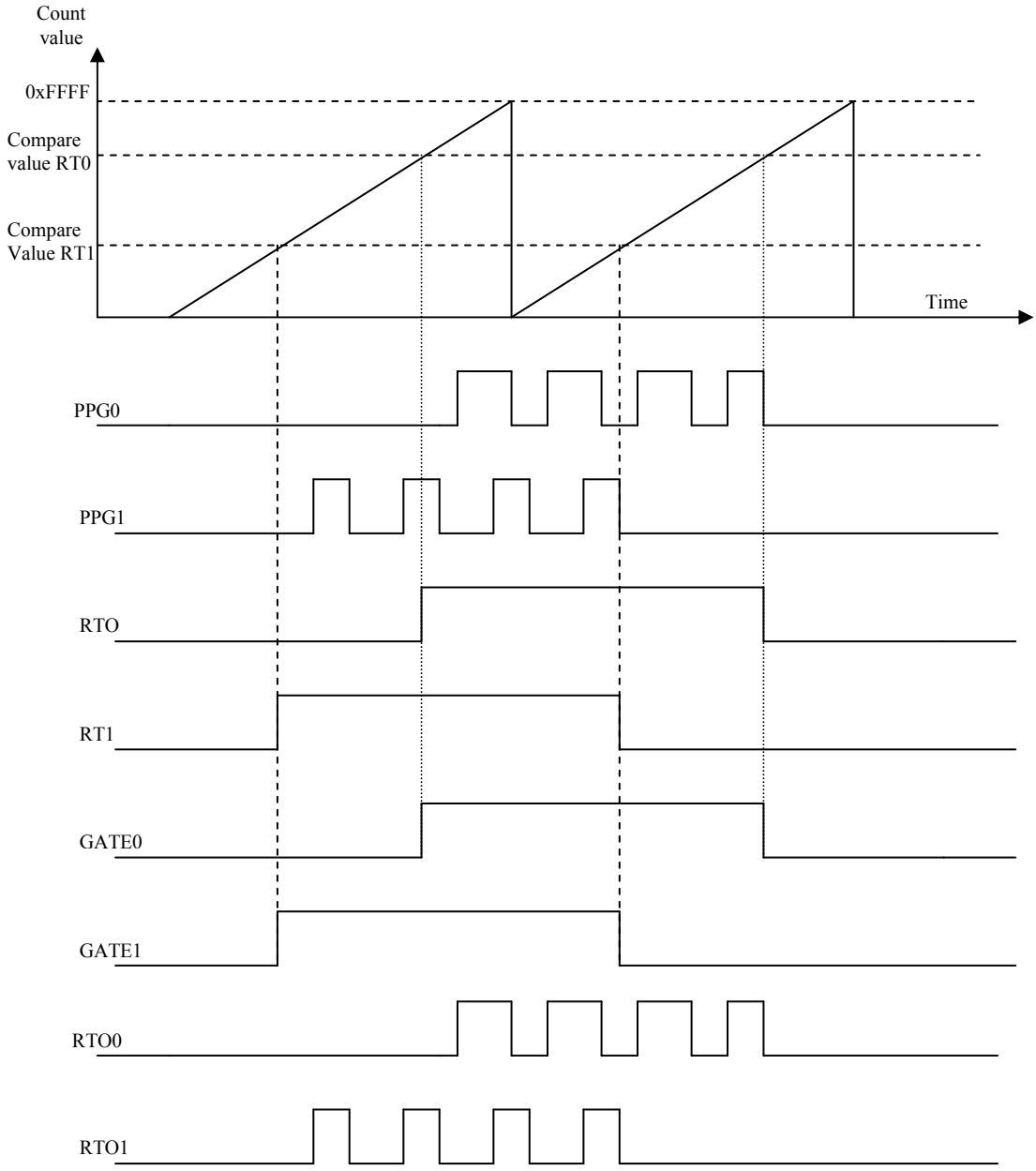
3.1.5 Waveform Generator

The 8-bit reload register must be set (TMRRx).

In Timer Control register (DTCRx) the GATE and PPG output must be enabled. (bit14 GTEN=1; bit13 PGEN=1).
With bit 15 DMOD positive(0) or negative(1) level output can be chosen.
The operation mode Bit8-10 TMD0-2 must be set to ‘1’. (PPG timer output pulse while RT signal is ‘H’)
TMD2=0;
TMD1=0;
TMD0=1;

In Waveform Control register the bits 7 to 5 can stay at initial values. Choose clock frequency by setting bit4 to 2 (DCK2-0).
Bit1 and bit 0 (PGS1, PGS0) can stay at initial values.

Generating a PPG output/GATE signal during each RT is a ‘H’ level



Description:

The 16-bit counter counts up continuously to 0xFFFF. If the written value in Compare registers of any output compare unit is matched with the counting value, the corresponding RT signal get ‘H’ level. (Next time match this value, RT gets low level) The depending GATE signal get the same level.
With a GATE ‘H’-level the PPG starts outputting signal, a ‘Low’-level stop PPG output.
The gated signals are outputted by RTOx pins.
Each PPG can be gated different.

3.2 Gate PPG with 8-bit Timer

Gating PPG, the three 8-bit timer of Waveform Generator can be used.
One Timer gates two PPG’s.

3.2.1 Settings

In this mode initialise:

- 16-bit free-run timer
- Output compare units
- PPG’s
- Waveform Generator

3.2.2 16-bit Free-run timer

Settings in Timer Control Register (TCCS):

Clock frequency must be set (CLK2-0)
Clear counter SCLR=1
Enable Counter STOP=1

It is possible to decrease counting by a compare clear. The counter will be set to 0 when value in compare clear register (CPCLR) has matched.
Therefore the clear value is written in compare clear register CPCLR. In Timer Control Register the Compare clear interrupt ICLR=1 is enabled.

3.2.3 Output Compare Units

The compare value must be written into Compare Registers OCCP0-5.

Register settings:

Compare control register OCSx:
Bit12: CMOD=0;
Bit11: OTE1=1;
Bit10: OTE0=1;

3.2.4 PPG's

In PPG Reload Register (PRLH0-5, PRLL0-5) the reload values of the down counter are stored. In upper register PRLH0-5 'High' pulse width and in lower register PRLL0-5 'Low' pulse width is written (positive pulse).

PPG Control Register PPGC0-5:

Bit15: PEN1=1; start operation for PPG1/3/5, writing '0' to this bit will stop PPG
Bit14: SST1=1; PPG1/3/5 will operated when GATE='H'
Bit13: POE1=1; PPG output port for PPG1/3/5
Bit12: PIE1=0; Disable Interrupt request
Bit11: PUF1=0; clear interrupt request flag
Bit10-9: MOD1-0=0; 8-bit PPG, 2ch. independent mode
Bit8: reserved, when setting PPG, set '1' to this bit
Bit7: PEN0=1; start operation for PPG0/2/4, writing '0' to this bit will stop PPG
Bit6: SST0=1; PPG0/2/4 will operated when GATE='H'
Bit5: POE0=1; PPG output port for PPG0/2/4
Bit4: PIE0=0; Disable Interrupt request
Bit3: PUF0=0; clear interrupt request flag
Bit2: POS1=0; select pulse polarity PPG1/3/5('0':positive , '1': negative)
Bit2: POS0=0; select pulse polarity PPG0/2/4('0':positive , '1': negative)
Bit0: reserved, when setting PPG, set '1' to this bit

PPG Clock Control register PCS01/23/45:

The 8-bit PPG Clock Control Register are used to control the operation clock frequency for PPG0-5.In one register are clock settings of two PPG's.
Bit7-5: PC12-PC10 setting of operation clock for PPG1/3/5
Bit4-2: PC02-PC00 setting of operation clock for PPG0/2/4
Bit1, bit0 are not used

PC02	PC01	PC00	Operation clock for ch0/2/4
0	0	0	ϕ (62.5 ns ϕ = 16 MHz)
0	0	1	ϕ /2 (125 ns ϕ = 16 MHz)
0	1	0	ϕ /4 (50 ns ϕ = 16 MHz)
0	1	1	ϕ /8 (500 ns ϕ = 16 MHz)
1	0	0	ϕ /16 (1 µs ϕ = 16 MHz)
1	0	1	ϕ /32 (2 µs ϕ = 16 MHz)
1	1	0	ϕ /64 (4 µs ϕ = 16 MHz)
1	1	1	Input clock from timebase trimmer

PC12	PC11	PC10	Operation clock for ch1/3/5
0	0	0	ϕ (62.5 ns ϕ = 16 MHz)
0	0	1	ϕ /2 (125 ns ϕ = 16 MHz)
0	1	0	ϕ /4 (50 ns ϕ = 16 MHz)
0	1	1	ϕ /8 (500 ns ϕ = 16 MHz)
1	0	0	ϕ /16 (1 µs ϕ = 16 MHz)
1	0	1	ϕ /32 (2 µs ϕ = 16 MHz)
1	1	0	ϕ /64 (4 µs ϕ = 16 MHz)
1	1	1	Input clock from timebase trimmer

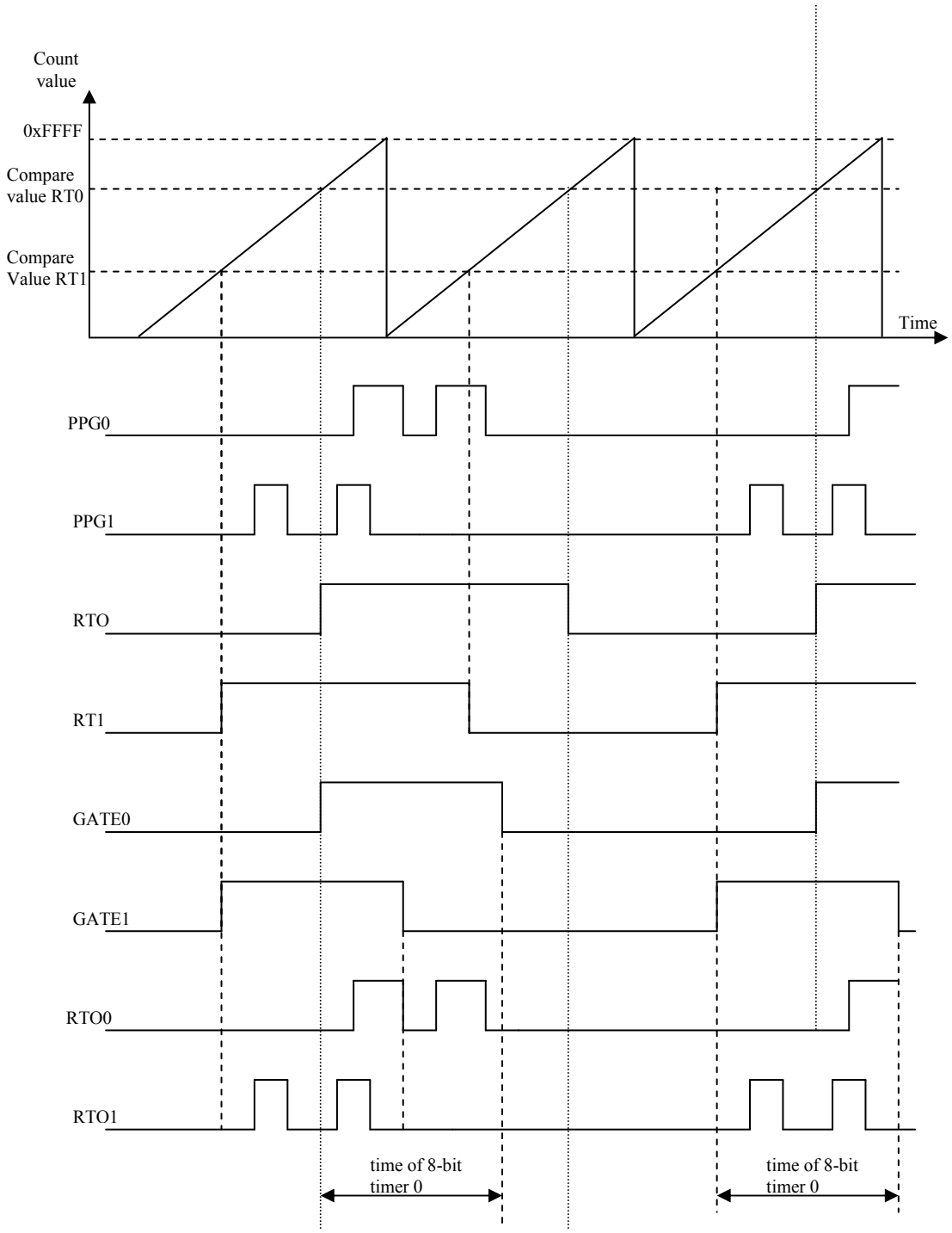
3.2.5 Waveform Generator

The 8-bit reload register must be set (TMRRx).

In Timer Control register (DTCRx) the GATE and PPG output must be enabled. (bit14 GTEN=1; bit13 PGEN=1).
With bit 15 DMOD positive(0) or negative(1) level output can be chosen.
The operation mode Bit8-10 TMD0-2 must be set to ‘2’. (PPG timer output pulse while RT signal is ‘H’)
TMD2=0;
TMD1=1;
TMD0=0;

In Waveform Control register the bits 7 to 5 can stay at initial values. Choose clock frequency by setting bit4 to 2 (DCK2-0).
Bit1 and bit 0 (PGS1, PGS0) can stay at initial values.

Generating a PPG output/GATE signal during each RT is a ‘H’ level



Description:

The 16-Bit Free-run timer counts up continuously. When written value in Compare Register is matched, the corresponding RT signal get a High-level.
The rising edge of RT will Start the 8-bit counter and GATE-signal get High-level.
The selected PPG starts outputting signal until the value of the 8 bit timer is matched with the value of 8-bit reload (TMRR) register. GATE signal gets Low.
Note: PPG0/1 depends on timer0
PPG2/3 depends on timer1
PPG4/5 depends on timer2