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F²MC-16LX 16-bit Microcontroller Datasheet

The MB90360E-series, loaded 1 channel FULL-CAN* interface and Flash ROM, is general-purpose Cypress 16-bit microcontroller designing for automotive and industrial applications. Its main feature is the on-board CAN Interfaces, which conform to Ver 2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal FULL-CAN approach. With the new 0.35 μ m CMOS technology, Cypress now offers on-chip Flash ROM program memory up to 64 Kbytes.

The power supply (3 V) is supplied to the MCU core from an internal regulator circuit. This creates a major advantage in terms of EMI and power consumption.

The internal PLL clock frequency multiplier provides an internal 42 ns instruction execution time from an external 4 MHz clock. Also, main and sub clock can be monitored independently using the clock supervisor function.

The unit features a 4-channel input capture unit 1 channel 16-bit free running timer, 2-channel LIN-UART, and 16-channel 8/10-bit A/D converter as the peripheral resource.

*: Controller Area Network (CAN) - License of Robert Bosch GmbH

Features

Clock

- Built-in PLL clock frequency multiplication circuit
- Selection of machine clocks (PLL clocks) is allowed among frequency division by 2 on oscillation clock and multiplication of 1 to 6 times of oscillation clock (for 4 MHz oscillation clock, 4 MHz to 24 MHz)
- Operation by sub clock : internal operating clock frequency: up to 50 kHz (for operating with 100 kHz oscillation clock divided two and devices without S-suffix only) is available
- Minimum execution time of instruction: 42 ns (when operating with 4-MHz oscillation clock and 6-time multiplied PLL clock)

Clock supervisor (MB90x367x only)

- Main clock or sub clock is monitored independently

Instruction system best suited to controller

- 16 Mbytes CPU memory space
- 24-bit internal addressing
- Wide choice of data types (bit, byte, word, and long word)
- Wide choice of addressing modes (23 types)
- Enhanced multiply-divide instructions with sign and RETI instructions
- Enhanced high-precision computing with 32-bit accumulator

Instruction system compatible with high-level language (C language) and multitask

- Employing system stack pointer
- Enhanced various pointer indirect instructions
- Barrel shift instructions

Increased processing speed

4-byte instruction queue

Powerful interrupt function

- Powerful 8-level, 34-condition interrupt feature
- Up to 8 channels external interrupts are supported

Automatic data transfer function independent of CPU

Expanded intelligent I/O service function (EI²OS) : up to 16 channels

Low power consumption (standby) mode

- Sleep mode (a mode that halts CPU operating clock)
- Main timer mode (timebase timer mode that is transferred from main clock mode)
- PLL timer mode (timebase timer mode that is transferred from PLL clock mode)
- Watch mode (a mode that operates sub clock and watch timer only, devices without S-suffix)
- Stop mode (a mode that stops oscillation clock and sub clock)
- CPU blocking operation mode

Process

CMOS technology

I/O port

General purpose input/output port (CMOS output) :
 - 34 ports (devices without S-suffix)
 - 36 ports (devices with S-suffix)

Sub clock pin (X0A and X1A)

- Provided (used for external oscillation), devices without S-suffix
- Not provided, devices with S-suffix

Timer

- Timebase timer, watch timer (device without S-suffix) ,
watchdog timer: 1 channel

- 8/16-bit PPG timer: 8-bit × 4 channels or 16-bit × 2 channels
- 16-bit reload timer: 2 channels
- 16-bit input/output timer
 - 16-bit free-run timer: 1 channel (FRT0: ICU 0/1/2/3)
 - 16-bit input capture: (ICU) : 4 channels

FULL-CAN interface: 1 channel

- Compliant with CAN specifications Version 2.0 Part A and B
- 16 message buffers are built in
- CAN wake-up function

LIN-UART: 2 channels

- Equipped with full-duplex double buffer
- Clock-asynchronous or clock-synchronous serial transmission is available

DTP/External interrupt: up to 8 channels, CAN wakeup: up to 1 channel

Module for activation of expanded intelligent I/O service (EI²OS) and generation of external interrupt by external input

Delay interrupt generator module

Generates interrupt request for task switching

8/10-bit A/D converter: 16 channels

- Resolution is selectable between 8-bit and 10-bit
- Activation by external trigger input is allowed
- Conversion time: 3 μs (at 24-MHz machine clock, including sampling time)

Address matching detection (program patch) function

Address matching detection for 6 address pointers

Low voltage/CPU operation detection reset (devices with T-suffix)

- Detects low voltage ($4.0\text{ V} \pm 0.3\text{ V}$) and resets automatically
- Resets automatically when program is runaway and counter is not cleared within interval time (approx. 262 ms: external 4 MHz)

Capable of changing input voltage for port

Automotive/CMOS-Schmitt input level (initial level is Automotive in single-chip mode)

Flash memory security function

Protects the content of Flash memory (MB90F362x, MB90F367x only)

Contents

Product Lineup	3	AC Characteristics	43
Pin Assignment	6	Clock Timing	43
Pin Description	7	Reset Standby Input	46
I/O Circuit Type	10	Power-on Reset	47
Handling Devices	13	LIN-UART0/1	48
Block Diagrams	16	Trigger Input Timing	52
Memory Map	20	Timer Related Resource Input Timing	53
I/O Map	21	Timer Related Resource Output Timing	53
CAN Controllers	28	A/D Converter	54
Interrupt Factors, Interrupt Vectors,		Definition of A/D Converter Terms	57
Interrupt Control Register	35	Flash Memory Program/Erase Characteristics	58
Electrical Characteristics	37	Ordering Information	59
Absolute Maximum Ratings	37	Package Dimension	60
Recommended Conditions	39	Major Changes	61
DC Characteristics	40		

1. Product Lineup

Features	MB90362E	MB90362TE	MB90362ES	MB90362TES	MB90V340E-101	MB90V340E-102
Type	MASK ROM product				Evaluation product	
CPU	F ² MC-16LX CPU					
System clock	PLL clock multiplier (× 1, × 2, × 3, × 4, × 6, 1/2 when PLL stops) Minimum instruction execution time: 42 ns (4 MHz oscillation clock, PLL × 6)					
Sub clock pin (X0A, X1A)	Yes		No		No	Yes
Clock supervisor	No					
ROM	MASK ROM, 64 Kbytes				External	
RAM capacitance	3 Kbytes				30 Kbytes	
CAN interface	1 channel				3 channels	
LIN-UART	2 channels					
Low voltage/CPU operation detection reset	No	Yes	No	Yes	No	
Package	LQFP-48P				PGA-299C	
Emulator-specific power supply *	—				Yes	
Corresponding evaluation product	MB90V340E-102		MB90V340E-101		—	

*: It is setting of Jumper switch (TOOL VCC) when emulator (MB2147-01) is used. Please refer to the Emulator hardware manual for the details.

Features	MB90F362E	MB90F362TE	MB90F362ES	MB90F362TES
Type	Flash memory product			
CPU	F ² MC-16LX CPU			
System clock	PLL clock multiplier (× 1, × 2, × 3, × 4, × 6, 1/2 when PLL stops) Minimum instruction execution time: 42 ns (4 MHz oscillation clock, PLL × 6)			
Sub clock pin (X0A, X1A)	Yes		No	
Clock supervisor	No			
ROM	Flash memory, 64 Kbytes			
RAM capacitance	3 Kbytes			
CAN interface	1 channel			
LIN-UART	2 channels			
Low voltage/CPU operation de- tection reset	No	Yes	No	Yes
Package	LQFP-48P			
Corresponding evaluation product	MB90V340E-102		MB90V340E-101	

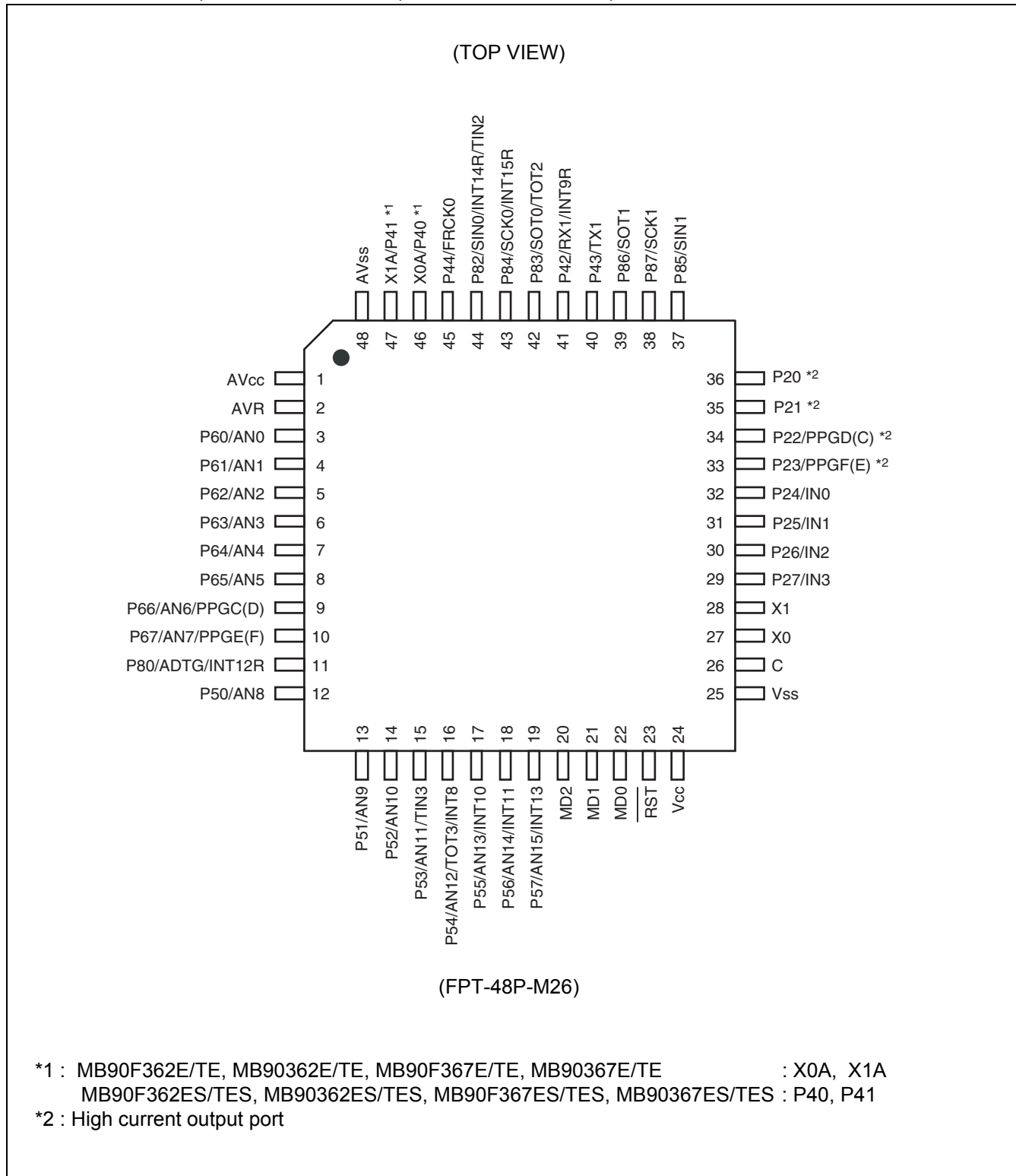
Features	MB90367E	MB90367TE	MB90367ES	MB90367TES	MB90V340E-103	MB90V340E-104
Type	MASK ROM product				Evaluation product	
CPU	F ² MC-16LX CPU					
System clock	PLL clock multiplier (× 1, × 2, × 3, × 4, × 6, 1/2 when PLL stops) Minimum instruction execution time: 42 ns (4 MHz oscillation clock, PLL × 6)					
Sub clock pin (X0A, X1A)	Yes		No			Yes
Clock supervisor	Yes					
ROM	MASK ROM, 64 Kbytes				External	
RAM capacitance	3 Kbytes				30 Kbytes	
CAN interface	1 channel				3 channels	
LIN-UART	2 channels					
Low voltage/CPU operation detection reset	No	Yes	No	Yes	No	
Package	LQFP-48P				PGA-299C	
Emulator-specific power supply *	—				Yes	
Corresponding EVA product	MB90V340E-104		MB90V340E-103		—	

*: It is setting of Jumper switch (TOOL VCC) when emulator (MB2147-01) is used. Please refer to the Emulator hardware manual for the details.

Features	MB90F367E	MB90F367TE	MB90F367ES	MB90F367TES
Type	Flash memory product			
CPU	F ² MC-16LX CPU			
System clock	PLL clock multiplier (× 1, × 2, × 3, × 4, × 6, 1/2 when PLL stops) Minimum instruction execution time: 42 ns (4 MHz oscillation clock, PLL × 6)			
Sub clock pin (X0A, X1A)	Yes		No	
Clock supervisor	Yes			
ROM	Flash memory, 64 Kbytes			
RAM capacitance	3 Kbytes			
CAN interface	1 channel			
LIN-UART	2 channels			
Low voltage/CPU operation detection reset	No	Yes	No	Yes
Package	LQFP-48P			
Corresponding EVA product	MB90V340E-104		MB90V340E-103	

2. Pin Assignment

■ MB90F362E/TE/ES/TES, MB90362E/TE/ES/TES, MB90F367E/TE/ES/TES, MB90367E/TE/ES/TES



3. Pin Description

Pin No.	Pin name	I/O circuit type*	Function
1	AV _{CC}	I	V _{CC} power input pin for analog circuit.
2	AVR	–	Power (V _{ref+}) input pin for A/D converter. It should be below V _{CC} .
3 to 8	P60 to P65	H	General-purpose I/O port.
	AN0 to AN5		Analog input pins for A/D converter.
9, 10	P66, P67	H	General-purpose I/O port.
	AN6, AN7		Analog input pins for A/D converter.
	PPGC (D), PPGE (F)		Output pins for PPG.
11	P80	F	General-purpose I/O port.
	ADTG		Trigger input pin for A/D converter.
	INT12R		External interrupt request input pin for INT12.
12 to 14	P50 to P52	H	General-purpose I/O port (P50 has different I/O circuit type from MB90V340E).
	AN8 to AN10		Analog input pins for A/D converter.
15	P53	H	General-purpose I/O port.
	AN11		Analog input pin for A/D converter.
	TIN3		Event input pin for reload timer 3.
16	P54	H	General-purpose I/O port.
	AN12		Analog input pin for A/D converter.
	TOT3		Output pin for reload timer 3
	INT8		External interrupt request input pin for INT8.
17 to 19	P55 to P57	H	General-purpose I/O port.
	AN13 to AN15		Analog input pins for A/D converter.
	INT10, INT11, INT13		External interrupt request input pins for INT10, INT11, INT13.
20	MD2	D	Input pin for operation mode specification.
21, 22	MD1, MD0	C	Input pins for operation mode specification.
23	RST	E	Reset input pin.
24	V _{CC}	–	Power input pin (3.5 V to 5.5 V).
25	V _{SS}	–	Power input pin (0 V).
26	C	I	Power supply stabilization capacitor pin. It should be connected to a higher than or equal to 0.1 μF ceramic condenser.

(Continued)

Pin No.	Pin name	I/O circuit type*	Function
27	X0	A	Oscillation input pin.
28	X1		Oscillation output pin.
29 to 32	P27 to P24	G	General-purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	IN3 to IN0		Event input pins for input capture 0 to 3.
33, 34	P23, P22	J	General-purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. High current output port.
	PPGF (E) , PPGD (C)		Output pins for PPG.
35, 36	P21, P20	J	General-purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. High current output port.
37	P85	K	General-purpose I/O port.
	SIN1		Serial data input pin for LIN-UART1.
38	P87	F	General-purpose I/O port.
	SCK1		Clock I/O pin for LIN-UART1.
39	P86	F	General-purpose I/O port.
	SOT1		Serial data output pin for LIN-UART1.
40	P43	F	General-purpose I/O port.
	TX1		TX output pin for CAN1 interface.
41	P42	F	General-purpose I/O port.
	RX1		RX input pin for CAN1 interface.
	INT9R		External interrupt request input pin for INT9 (Sub) .
42	P83	F	General-purpose I/O port.
	SOT0		Serial data output pin for LIN-UART0.
	TOT2		Output pin for reload timer 2.
43	P84	F	General-purpose I/O port.
	SCK0		Clock I/O pin for LIN-UART0.
	INT15R		External interrupt request input pin for INT15.

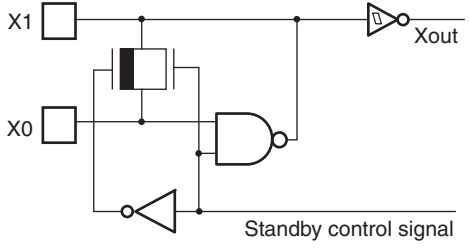
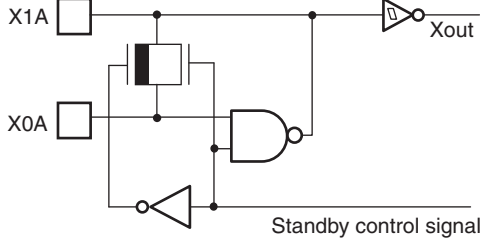
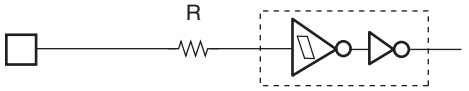
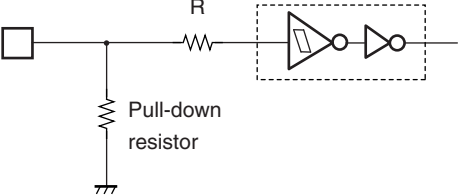
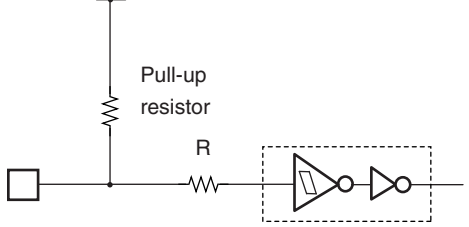
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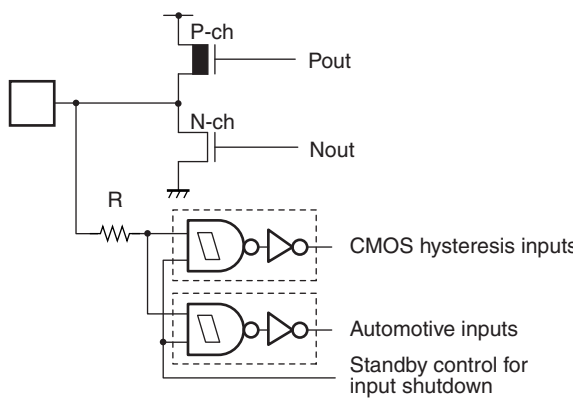
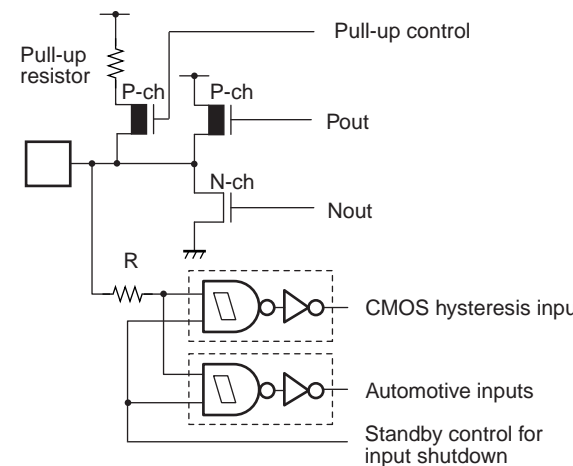
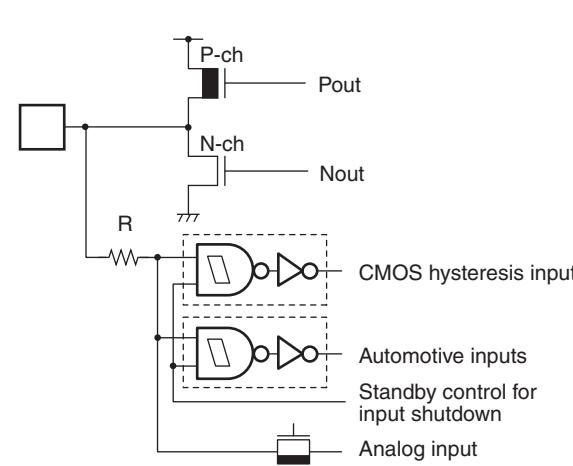
Pin No.	Pin name	I/O circuit type*	Function
44	P82	K	General-purpose I/O port.
	SIN0		Serial data input pin for LIN-UART0.
	INT14R		External interrupt request input pin for INT14.
	TIN2		Event input pin for reload timer 2.
45	P44	F	General-purpose I/O port (Different I/O circuit type from MB90V340E) .
	FRCK0		Free-run timer 0 clock pin.
46, 47	P40, P41	F	General-purpose I/O port (Devices with S-suffix and MB90V340E-101/103 only) .
	X0A, X1A	B	Oscillation pins for sub clock (Devices without S-suffix and MB90V340E-102/104 only) .
48	AV _{SS}	I	V _{SS} power input pin for analog circuit.

*: For the I/O circuit type, refer to “[I/O Circuit Type](#)”

4. I/O Circuit Type

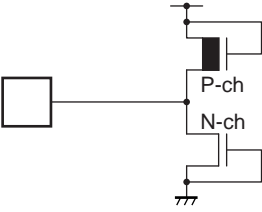
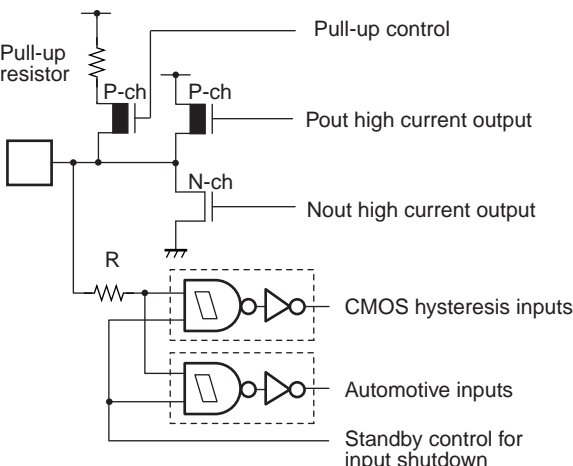
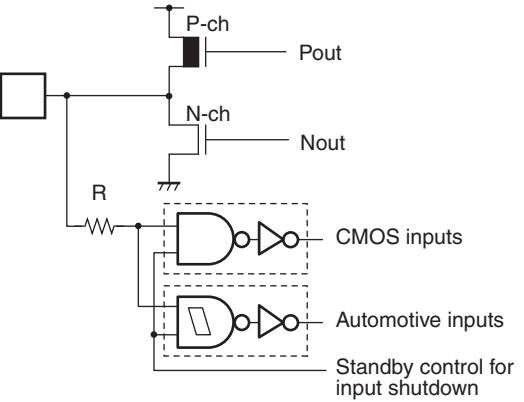
Type	Circuit	Remarks
A		<p>Oscillation circuit: High-speed oscillation feedback resistor = approx. 1 MΩ</p>
B		<p>Oscillation circuit: Low-speed oscillation feedback resistor = approx. 10 MΩ</p>
C		<ul style="list-style-type: none"> ■ MASK ROM product: CMOS hysteresis input pin ■ Flash memory product: CMOS input pin
D		<ul style="list-style-type: none"> ■ MASK ROM product: CMOS hysteresis input pin ■ Flash memory product: - CMOS input pin - No Pull-down
E		<p>CMOS hysteresis input pin</p>

(Continued)

Type	Circuit	Remarks
F		<ul style="list-style-type: none"> ■ CMOS level output ■ CMOS hysteresis inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function)
G		<ul style="list-style-type: none"> ■ CMOS level output ■ CMOS hysteresis inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function)
H		<ul style="list-style-type: none"> ■ CMOS level output ■ CMOS hysteresis inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function) ■ A/D analog input

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Type	Circuit	Remarks
I		Protection circuit for power supply input
J		<ul style="list-style-type: none"> ■ CMOS level output ■ CMOS hysteresis inputs (With the standby-time input shutdown function) ■ Automotive input (With the standby-time input shutdown function)
K		<ul style="list-style-type: none"> ■ CMOS level output ■ CMOS input (With standby-time input shutdown function) ■ Automotive input (With standby-time input shutdown function)

5. Handling Devices

1. Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} pin or lower than V_{SS} pin is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pin and V_{SS} pin.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

Use meticulous care not to exceed the rating.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC} , AVR) exceed the digital power-supply voltage.

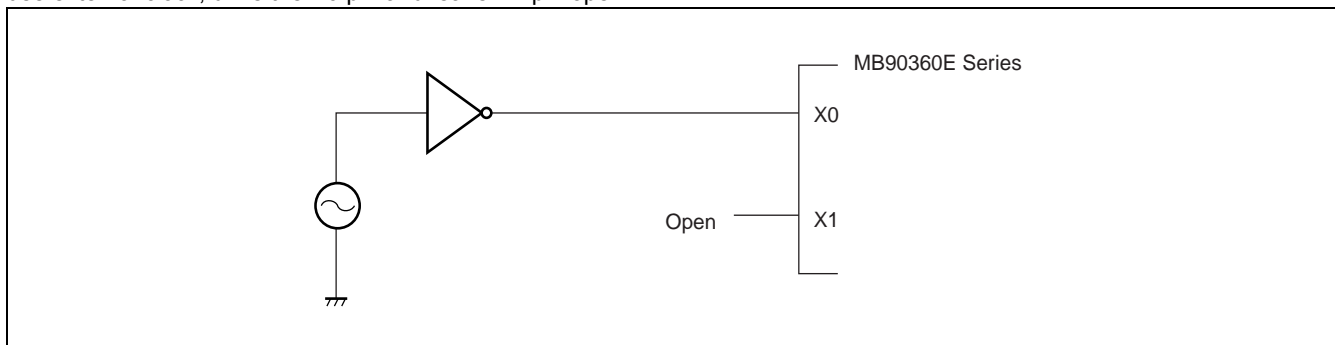
2. Treatment of unused pins

Leaving unused input pins open may result in permanent damage of the device due to misbehavior or latch-up. Therefore, they must be pulled up or pulled down through resistors. In this case, those resistors should be more than 2 k Ω .

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

3. Using external clock

To use external clock, drive the X0 pin and leave X1 pin open.



4. Precautions for when not using a sub clock signal

If you do not connect pins X0A and X1A to an oscillator, use pull-down handling on the X0A pin and leave the X1A pin open.

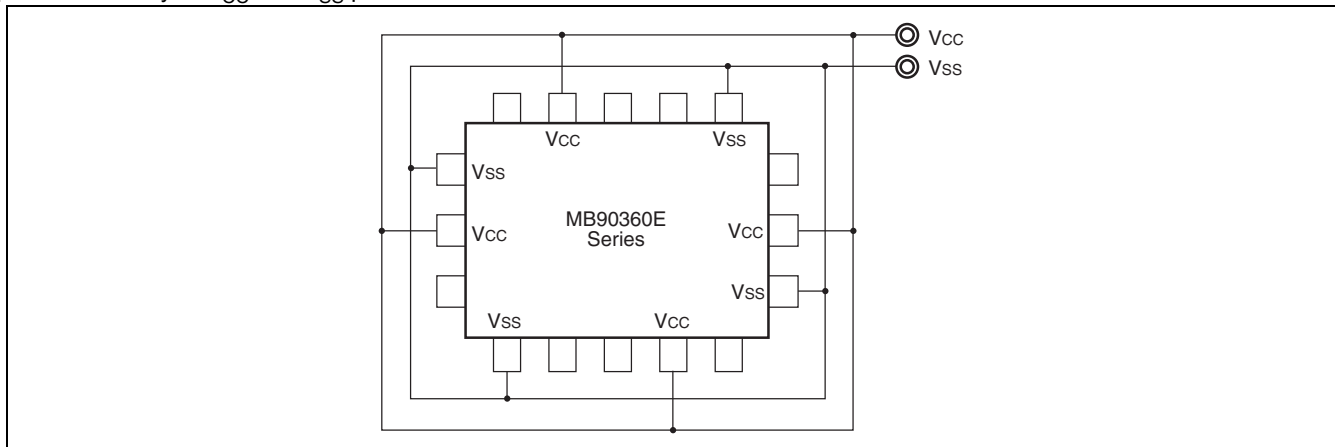
5. Notes on during operation of PLL clock mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Fujitsu will not guarantee results of operations if such failure occurs.

6. Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent malfunction such as latch-up.
To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally.
- Connect V_{CC} and V_{SS} pins to the device from the current supply source at a low impedance.

- As a measure against power supply noise, connect a capacitor of about 0.1 μF as a bypass capacitor between V_{CC} pin and V_{SS} pin in the vicinity of V_{CC} and V_{SS} pins of the device.



7. Pull-up/down resistors

The MB90360E Series does not support internal pull-up/down resistors (Port 2: built-in pull-up resistors) . Use external components where needed.

8. Crystal oscillator circuit

Noises around X0 or X1 pin may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board artwork surrounding X0 and X1 pins with a ground area for stabilizing the operation. Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

9. Turning-on sequence of power supply to A/D converter and analog inputs

Make sure to turn on the A/D converter power supply (AV_{CC} and AVR) and analog inputs ($AN0$ to $AN15$) after turning-on the digital power supply (V_{CC}) .

Turn-off the digital power after turning off the A/D converter power supply and analog inputs. In this case, make sure that the voltage does not exceed $AVRH$ or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

10. Connection of unused pins of A/D converter if A/D converter is not used

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVR = V_{SS}$.

11. Notes on energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 μs or more (0.2 V to 2.7 V) .

12. Stabilization of power supply voltage

A sudden change in the power supply voltage may cause the device to malfunction even within the specified V_{CC} power supply voltage operating guarantee range. Therefore, the V_{CC} power supply voltage should be stabilized.

For reference, the power supply voltage should be controlled so that V_{CC} ripple variations (peak-to-peak value) at commercial frequencies (50 Hz/60 Hz) fall below 10% of the standard V_{CC} power supply voltage and the coefficient of transient fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

13. Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, turn on the power again.

14. Notes on using CAN function

To use CAN function, please set '1' to DIRECT bit of CAN direct mode register (CDMR).

If DIRECT bit is set to '0' (initial value), wait states will be performed when accessing CAN registers.

Note: Please refer to Hardware Manual of "MB90360E series for detail of CAN Direct Mode Register".

15. Flash security function

The security bit is located in the area of the Flash memory.

If protection code 01_H is written in the security bit, the Flash memory is in the protected state by security.

Therefore, please do not write 01_H in this address if you do not use the security function.

Please refer to following table for the address of the security bit.

	Flash memory size	Address for security bit
MB90F362E MB90F362ES MB90F362TE MB90F362TES MB90F367E MB90F367ES MB90F367TE MB90F367TES	Embedded 512 Kbits Flash Memory	FF0001 _H

16. Correspondence with $T_A = +105\text{ }^{\circ}\text{C}$ or more

There is a restriction of reliability if the product is used exceeding $T_A = +105\text{ }^{\circ}\text{C}$.

Contact the sales or support representative.

It is ensured to write/erase data to the Flash memory between $T_A = -40\text{ }^{\circ}\text{C}$ and $+105\text{ }^{\circ}\text{C}$.

17. Serial communication

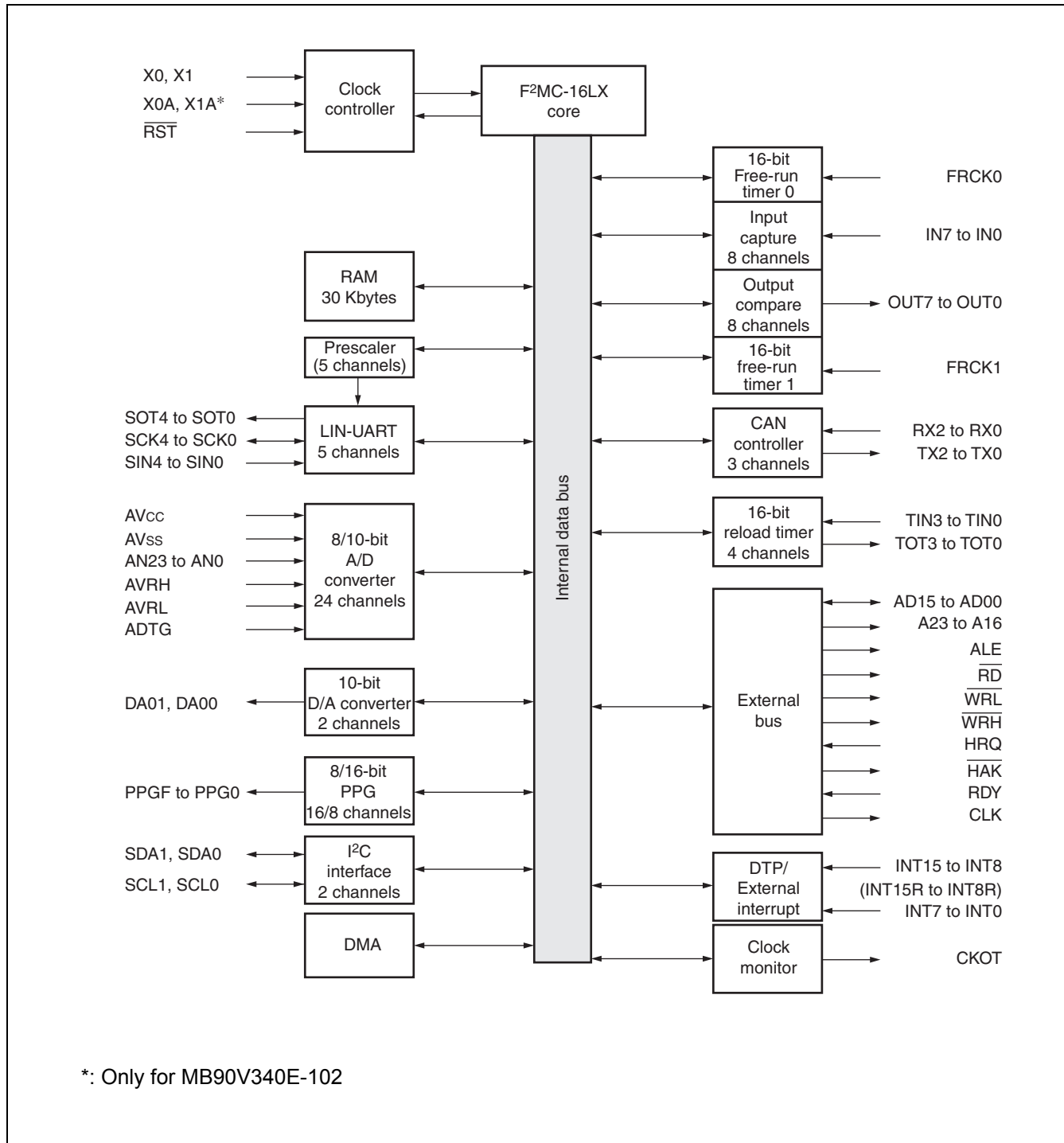
There is a possibility to receive wrong data due to the noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

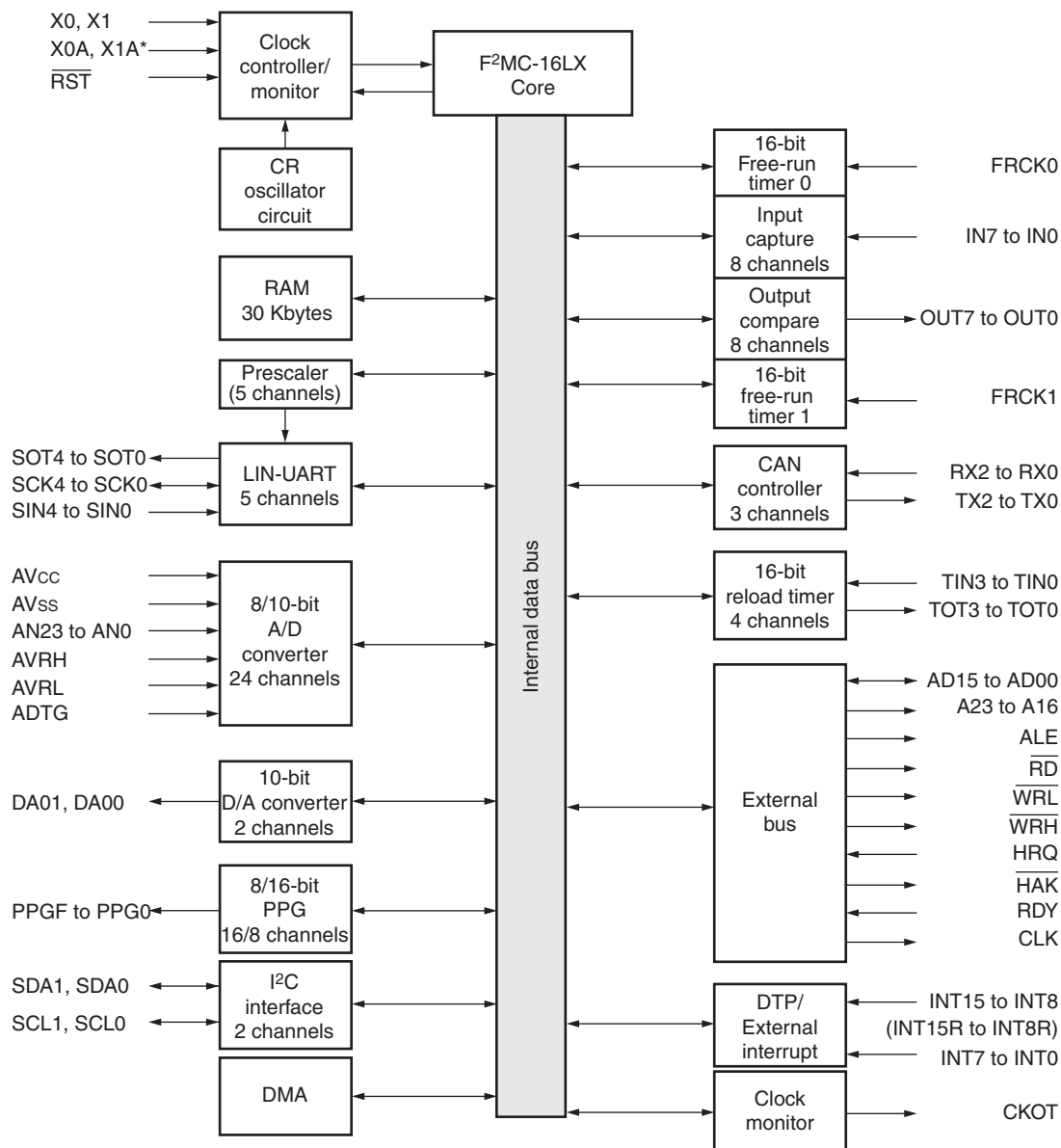
Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.

6. Block Diagrams

■ MB90V340E-101/102

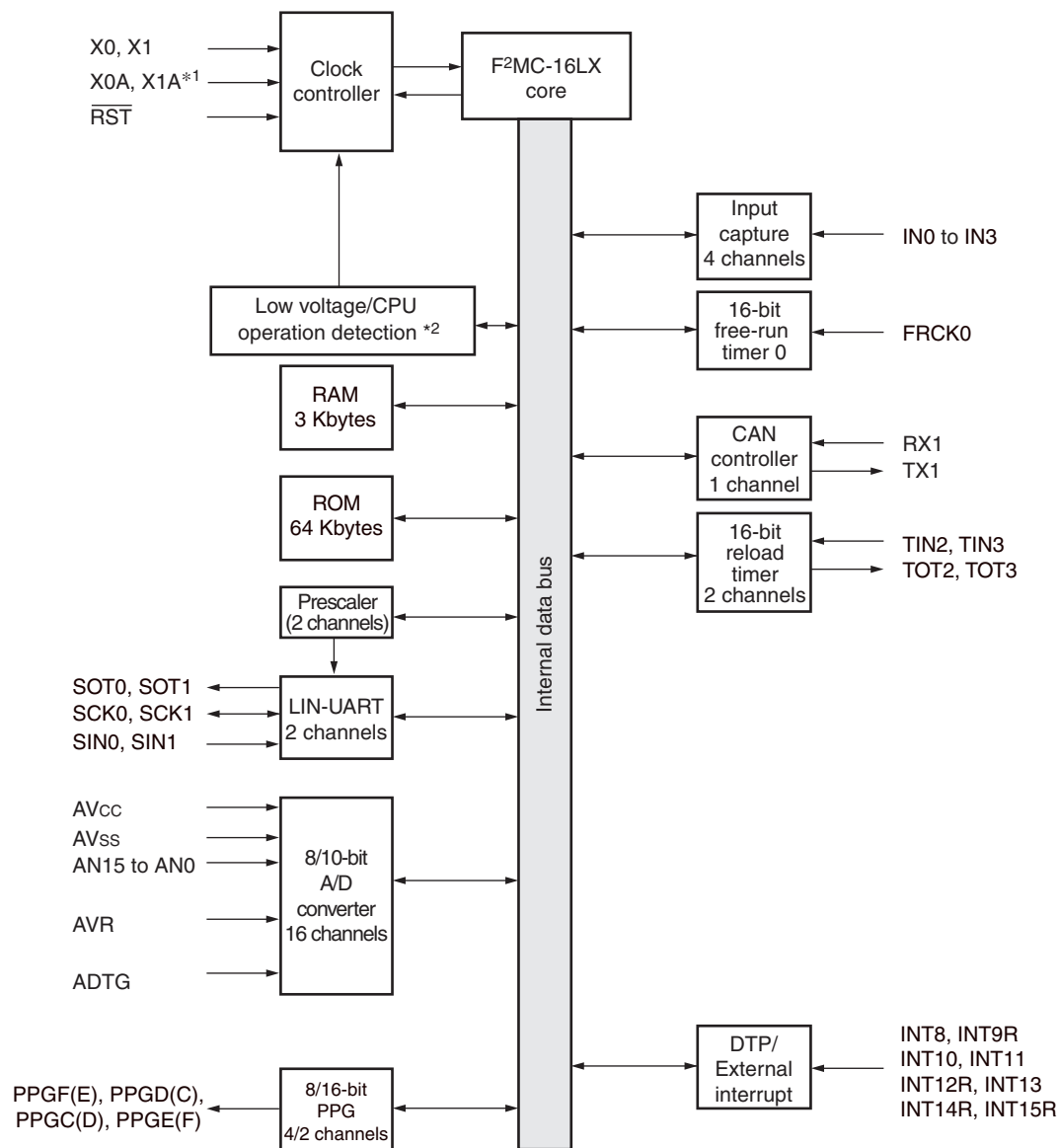


■ MB90V340E-103/104



*: Only for MB90V340E-104

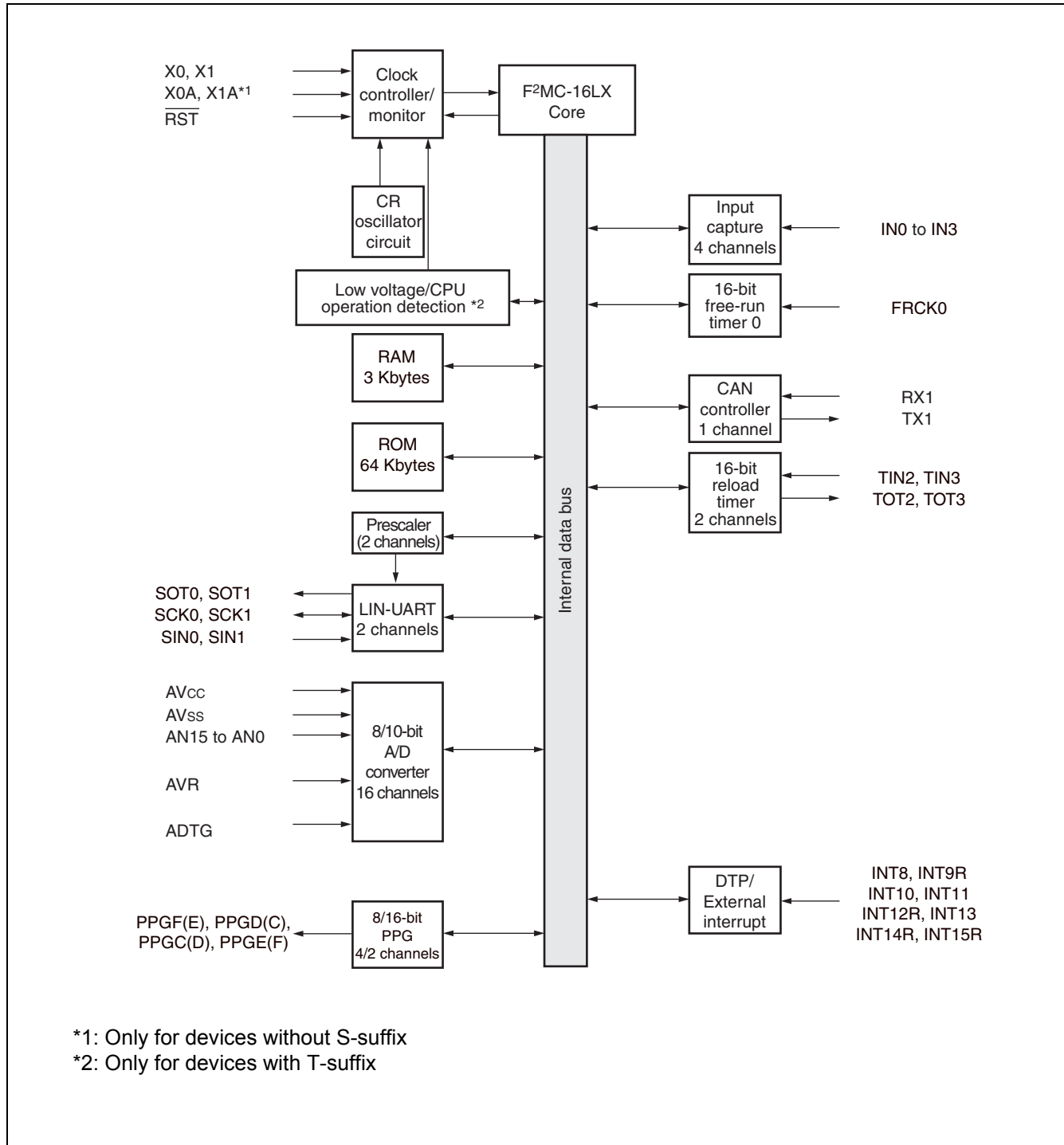
■ MB90F362E/TE/ES/TES, MB90362E/TE/ES/TES



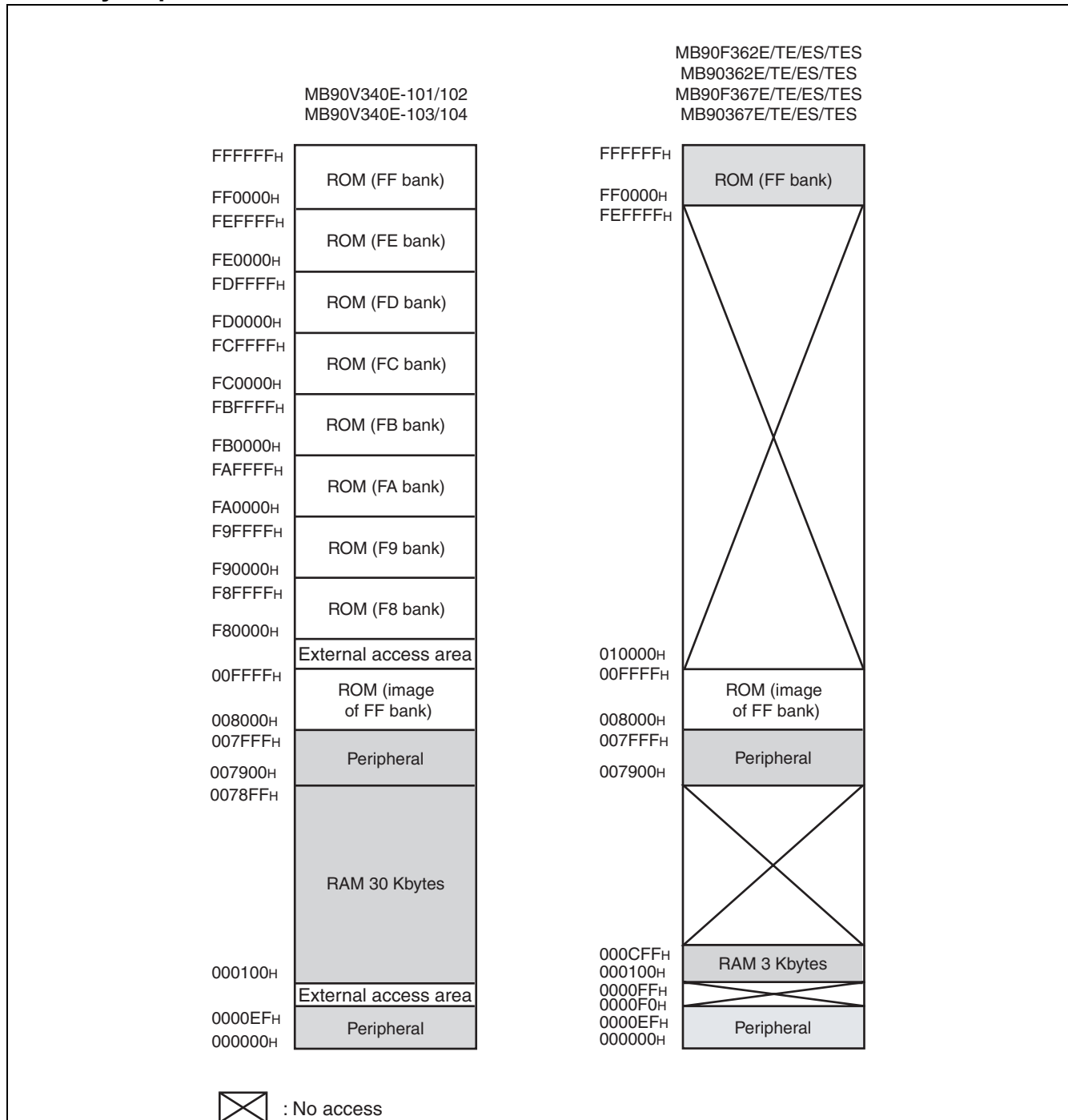
*1: Only for devices without S-suffix

*2: Only for devices with T-suffix

■ MB90F367E/TE/ES/TES, MB90367E/TE/ES/TES



7. Memory Map



Note: The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referred without using the far specification in the pointer declaration.

For example, an attempt to access 00C000_H practically accesses the value at FFC000_H in ROM.

The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.

The image between FF8000_H and FFFFFFF_H is visible in bank 00, while the image between FF0000_H and FF7FFF_H is visible only in bank FF.

8. I/O Map

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
000000 _H ,00 0001 _H	Reserved				
000002 _H	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXX _B
000003 _H	Reserved				
000004 _H	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXX _B
000005 _H	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXX _B
000006 _H	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXX _B
000007 _H	Reserved				
000008 _H	Port 8 Data Register	PDR8	R/W	Port 8	XXXXXXXX _B
000009 _H ,00 000A _H	Reserved				
00000B _H	Port 5 Analog Input Enable Register	ADER5	R/W	Port 5, A/D	1111111 _B
00000C _H	Port 6 Analog Input Enable Register	ADER6	R/W	Port 6, A/D	1111111 _B
00000D _H	Reserved				
00000E _H	Input Level Select Register	ILSR0	R/W	Ports	XXXX0XXX _B
00000F _H	Input Level Select Register	ILSR1	R/W	Ports	XXXXXXXX _B
000010 _H ,00 0011 _H	Reserved				
000012 _H	Port 2 Direction Register	DDR2	R/W	Port 2	0000000 _B
000013 _H	Reserved				
000014 _H	Port 4 Direction Register	DDR4	R/W	Port 4	XXX0000 _B
000015 _H	Port 5 Direction Register	DDR5	R/W	Port 5	0000000 _B
000016 _H	Port 6 Direction Register	DDR6	R/W	Port 6	0000000 _B
000017 _H	Reserved				
000018 _H	Port 8 Direction Register	DDR8	R/W	Port 8	000000X0 _B
000019 _H	Reserved				
00001A _H	Port A Direction Register	DDRA	W	Port A	XXX00XXX _B
00001B _H to 00001D _H	Reserved				
00001E _H	Port 2 Pull-up Control Register	PUCR2	R/W	Port 2	0000000 _B
00001F _H	Reserved				

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
000020 _H	Serial Mode Register 0	SMR0	W, R/W	LIN-UART0	00000000 _B
000021 _H	Serial Control Register 0	SCR0	W, R/W		00000000 _B
000022 _H	Reception/Transmission Data Register 0	RDR0/TDR0	R/W		00000000 _B
000023 _H	Serial Status Register 0	SSR0	R, R/W		00001000 _B
000024 _H	Extended Communication Control Register 0	ECCR0	R, W, R/W		000000XX _B
000025 _H	Extended Status/Control Register 0	ESCR0	R/W		00000100 _B
000026 _H	Baud Rate Generator Register 00	BGR00	R/W, R		00000000 _B
000027 _H	Baud Rate Generator Register 01	BGR01	R/W, R		00000000 _B
000028 _H	Serial Mode Register 1	SMR1	W, R/W	LIN-UART1	00000000 _B
000029 _H	Serial Control Register 1	SCR1	W, R/W		00000000 _B
00002A _H	Reception/Transmission Data Register 1	RDR1/TDR1	R/W		00000000 _B
00002B _H	Serial Status Register 1	SSR1	R, R/W		00001000 _B
00002C _H	Extended Communication Control Register 1	ECCR1	R, W, R/W		000000XX _B
00002D _H	Extended Status/Control Register 1	ESCR1	R/W		00000100 _B
00002E _H	Baud Rate Generator Register 10	BGR10	R/W, R		00000000 _B
00002F _H	Baud Rate Generator Register 11	BGR11	R/W, R		00000000 _B
000030 _H to 00003A _H	Reserved				
00003B _H	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	00000000 _B
00003C _H to 000047 _H	Reserved				
000048 _H	PPG C Operation Mode Control Register	PPGCC	W, R/W	16-bit PPG C/D	0X000XX1 _B
000049 _H	PPG D Operation Mode Control Register	PPGCD	W, R/W		0X000001 _B
00004A _H	PPG C/PPG D Count Clock Select Register	PPGCD	R/W		000000X0 _B
00004B _H	Reserved				
00004C _H	PPG E Operation Mode Control Register	PPGCE	W, R/W	16-bit PPG E/F	0X000XX1 _B
00004D _H	PPG F Operation Mode Control Register	PPGCF	W, R/W		0X000001 _B
00004E _H	PPG E/PPG F Count Clock Select Register	PPGEF	R/W		000000X0 _B
00004F _H	Reserved				

(Continued)

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
000050 _H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000 _B
000051 _H	Input Capture Edge 0/1	ICE01	R/W, R		XXX0X0XX _B
000052 _H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000 _B
000053 _H	Input Capture Edge 2/3	ICE23	R		XXXXXXXX _B
000054 _H to 000063 _H	Reserved				
000064 _H	Timer Control Status 2	TMCSR2	R/W	16-bit Reload Timer 2	00000000 _B
000065 _H	Timer Control Status 2	TMCSR2	R/W		XXXX0000 _B
000066 _H	Timer Control Status 3	TMCSR3	R/W	16-bit Reload Timer 3	00000000 _B
000067 _H	Timer Control Status 3	TMCSR3	R/W		XXXX0000 _B
000068 _H	A/D Control Status 0	ADCS0	R/W	A/D Converter	000XXXX0 _B
000069 _H	A/D Control Status 1	ADCS1	R/W, W		0000000X _B
00006A _H	A/D Data 0	ADCR0	R		00000000 _B
00006B _H	A/D Data 1	ADCR1	R		XXXXXX00 _B
00006C _H	ADC Setting 0	ADSR0	R/W		00000000 _B
00006D _H	ADC Setting 1	ADSR1	R/W		00000000 _B
00006E _H	Low Voltage/CPU Operation Detection Reset Control Register	LVRC	R/W, W	Low voltage/CPU operation detection reset	00111000 _B
00006F _H	ROM Mirror Function Select	ROMM	W	ROM Mirror	XXXXXXXX1 _B
000070 _H to 00007F _H	Reserved				
000080 _H to 00008F _H	Reserved for CAN Interface 1. Refer to “CAN Controllers”				
000090 _H to 00009D _H	Reserved				
00009E _H	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	00000000 _B
00009F _H	Delayed Interrupt/Release Register	DIRR	R/W	Delayed Interrupt generation module	XXXXXXXX0 _B
0000A0 _H	Low-power Consumption Mode Control Register	LPMCR	W, R/W	Low-Power consumption Control Circuit	00011000 _B
0000A1 _H	Clock Selection Register	CKSCR	R, R/W	Low-Power consumption Control Circuit	11111100 _B

(Continued)

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
0000A2 _H to 0000A7 _H	Reserved				
0000A8 _H	Watchdog Control Register	WDTC	R, W	Watchdog Timer	XXXXX111 _B
0000A9 _H	Timebase Timer Control Register	TBTC	W, R/W	Timebase Timer	1XX00100 _B
0000AA _H	Watch Timer Control register	WTC	R, R/W	Watch Timer	1X001000 _B
0000AB _H to 0000AD _H	Reserved				
0000AE _H	Flash Control Status (Flash Devices only. Otherwise reserved)	FMCS	R, R/W	Flash Memory	000X0000 _B
0000AF _H	Reserved				
0000B0 _H	Interrupt Control Register 00	ICR00	W, R/W	Interrupt Control	00000111 _B
0000B1 _H	Interrupt Control Register 01	ICR01	W, R/W		00000111 _B
0000B2 _H	Interrupt Control Register 02	ICR02	W, R/W		00000111 _B
0000B3 _H	Interrupt Control Register 03	ICR03	W, R/W		00000111 _B
0000B4 _H	Interrupt Control Register 04	ICR04	W, R/W		00000111 _B
0000B5 _H	Interrupt Control Register 05	ICR05	W, R/W		00000111 _B
0000B6 _H	Interrupt Control Register 06	ICR06	W, R/W		00000111 _B
0000B7 _H	Interrupt Control Register 07	ICR07	W, R/W		00000111 _B
0000B8 _H	Interrupt Control Register 08	ICR08	W, R/W		00000111 _B
0000B9 _H	Interrupt Control Register 09	ICR09	W, R/W		00000111 _B
0000BA _H	Interrupt Control Register 10	ICR10	W, R/W		00000111 _B
0000BB _H	Interrupt Control Register 11	ICR11	W, R/W		00000111 _B
0000BC _H	Interrupt Control Register 12	ICR12	W, R/W		00000111 _B
0000BD _H	Interrupt Control Register 13	ICR13	W, R/W		00000111 _B
0000BE _H	Interrupt Control Register 14	ICR14	W, R/W		00000111 _B
0000BF _H	Interrupt Control Register 15	ICR15	W, R/W		00000111 _B
0000C0 _H to 0000C9 _H	Reserved				
0000CA _H	External Interrupt Enable 1	ENIR1	R/W	External Interrupt 1	00000000 _B
0000CB _H	External Interrupt Source 1	EIRR1	R/W		XXXXXXXX _B
0000CC _H	Detection Level Setting 1	ELVR1	R/W		00000000 _B
0000CD _H					00000000 _B
0000CE _H	External Interrupt Source Select	EISSR	R/W		00000000 _B
0000CF _H	PLL/Sub clock Control Register	PSCCR	W	PLL	XXXX0000 _B

(Continued)

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
0000D0 _H to 0000FF _H	Reserved				
007900 _H to 007917 _H	Reserved				
007918 _H	Reload Register LC	PRLLC	R/W	16-bit PPG C/D	XXXXXXXX _B
007919 _H	Reload Register HC	PRLHC	R/W		XXXXXXXX _B
00791A _H	Reload Register LD	PRLLD	R/W		XXXXXXXX _B
00791B _H	Reload Register HD	PRLHD	R/W		XXXXXXXX _B
00791C _H	Reload Register LE	PRLLE	R/W	16-bit PPG E/F	XXXXXXXX _B
00791D _H	Reload Register HE	PRLHE	R/W		XXXXXXXX _B
00791E _H	Reload Register LF	PRLLF	R/W		XXXXXXXX _B
00791F _H	Reload Register HF	PRLHF	R/W		XXXXXXXX _B
007920 _H	Input Capture 0	IPCP0	R	Input Capture 0/1	XXXXXXXX _B
007921 _H	Input Capture 0	IPCP0	R		XXXXXXXX _B
007922 _H	Input Capture 1	IPCP1	R		XXXXXXXX _B
007923 _H	Input Capture 1	IPCP1	R		XXXXXXXX _B
007924 _H	Input Capture 2	IPCP2	R	Input Capture 2/3	XXXXXXXX _B
007925 _H	Input Capture 2	IPCP2	R		XXXXXXXX _B
007926 _H	Input Capture 3	IPCP3	R		XXXXXXXX _B
007927 _H	Input Capture 3	IPCP3	R		XXXXXXXX _B
007928 _H to 00793F _H	Reserved				
007940 _H	Timer Data 0	TCDT0	R/W	Free-run Timer 0	00000000 _B
007941 _H	Timer Data 0	TCDT0	R/W		00000000 _B
007942 _H	Timer Control Status 0	TCCSL0	R/W		00000000 _B
007943 _H	Timer Control Status 0	TCCSH0	R/W		0XXXXXXXX _B
007944 _H to 00794B _H	Reserved				
00794C _H	Timer 2/Reload 2	TMR2/TMRL R2	R/W	16-bit Reload Timer 2	XXXXXXXX _B
00794D _H			R/W		XXXXXXXX _B
00794E _H	Timer 3/Reload 3	TMR3/TMRL R3	R/W	16-bit Reload Timer 3	XXXXXXXX _B
00794F _H			R/W		XXXXXXXX _B
007950 _H to 00795F _H	Reserved				

(Continued)

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
007960 _H	Clock Supervisor Control Register	CSVCR	R, R/W	Clock supervisor	00011100 _B
007961 _H to 00796D _H	Reserved				
00796E _H	CAN Direct Mode Register (MB90V340E only)	CDMR	R/W	CAN clock sync	XXXXXXX0 _B
00796F _H to 0079DF _H	Reserved				
0079E0 _H	Detect Address Setting 0	PADR0	R/W	Address Match Detection 0	XXXXXXXX _B
0079E1 _H	Detect Address Setting 0	PADR0	R/W		XXXXXXXX _B
0079E2 _H	Detect Address Setting 0	PADR0	R/W		XXXXXXXX _B
0079E3 _H	Detect Address Setting 1	PADR1	R/W		XXXXXXXX _B
0079E4 _H	Detect Address Setting 1	PADR1	R/W		XXXXXXXX _B
0079E5 _H	Detect Address Setting 1	PADR1	R/W		XXXXXXXX _B
0079E6 _H	Detect Address Setting 2	PADR2	R/W		XXXXXXXX _B
0079E7 _H	Detect Address Setting 2	PADR2	R/W		XXXXXXXX _B
0079E8 _H	Detect Address Setting 2	PADR2	R/W		XXXXXXXX _B
0079E9 _H to 0079EF _H	Reserved				
0079F0 _H	Detect Address Setting 3	PADR3	R/W	Address Match Detection 1	XXXXXXXX _B
0079F1 _H	Detect Address Setting 3	PADR3	R/W		XXXXXXXX _B
0079F2 _H	Detect Address Setting 3	PADR3	R/W		XXXXXXXX _B
0079F3 _H	Detect Address Setting 4	PADR4	R/W		XXXXXXXX _B
0079F4 _H	Detect Address Setting 4	PADR4	R/W		XXXXXXXX _B
0079F5 _H	Detect Address Setting 4	PADR4	R/W		XXXXXXXX _B
0079F6 _H	Detect Address Setting 5	PADR5	R/W		XXXXXXXX _B
0079F7 _H	Detect Address Setting 5	PADR5	R/W		XXXXXXXX _B
0079F8 _H	Detect Address Setting 5	PADR5	R/W		XXXXXXXX _B
0079F9 _H to 007BFF _H	Reserved				
007C00 _H to 007CFF _H	Reserved for CAN Interface 1. Refer to “CAN Controllers”				
007D00 _H to 007DFF _H	Reserved for CAN Interface 1. Refer to “CAN Controllers”				

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Address	Register	Abbrevia- tion	Access	Resource name	Initial value
007E00 _H to 007FFF _H	Reserved				

- Notes:
- Initial value of "X" represents unknown value.
 - Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading "X".

9. CAN Controllers

- Conforms to CAN Specification Ver 2.0 Part A and Part B
 - Supports transmission/reception in standard frame and extended frame formats
- Supports transmitting of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
 - 29-bit ID and 8-byte data
 - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
 - 2 acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps/s to 2 Mbps/s (when input clock is at 16 MHz)

List of Control Registers (1)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
000080 _H	Message buffer valid register	BVALR	R/W	00000000 00000000 _B
000081 _H				
000082 _H	Transmit request register	TREQR	R/W	00000000 00000000 _B
000083 _H				
000084 _H	Transmit cancel register	TCANR	W	00000000 00000000 _B
000085 _H				
000086 _H	Transmission complete register	TCR	R/W	00000000 00000000 _B
000087 _H				
000088 _H	Receive complete register	RCR	R/W	00000000 00000000 _B
000089 _H				
00008A _H	Remote request receiving register	RRTRR	R/W	00000000 00000000 _B
00008B _H				
00008C _H	Receive overrun register	ROVRR	R/W	00000000 00000000 _B
00008D _H				
00008E _H	Reception interrupt enable register	RIER	R/W	00000000 00000000 _B
00008F _H				

List of Control Registers (2)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
007D00 _H	Control status register	CSR	R/W, W R/W, R	0XXXX0X1 00XXXX00 _B
007D01 _H				
007D02 _H	Last event indicator register	LEIR	R/W	000X0000 XXXXXXXX _B
007D03 _H				
007D04 _H	Receive and transmit error counter	RTEC	R	00000000 00000000 _B
007D05 _H				
007D06 _H	Bit timing register	BTR	R/W	11111111 X1111111 _B
007D07 _H				
007D08 _H	IDE register	IDER	R/W	XXXXXXXX XXXXXXXX _B
007D09 _H				
007D0A _H	Transmit RTR register	TRTRR	R/W	00000000 00000000 _B
007D0B _H				
007D0C _H	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX XXXXXXXX _B
007D0D _H				
007D0E _H	Transmit interrupt enable register	TIER	R/W	00000000 00000000 _B
007D0F _H				
007D10 _H	Acceptance mask select register	AMSR	R/W	XXXXXXXX XXXXXXXX _B
007D11 _H				XXXXXXXX XXXXXXXX _B
007D12 _H				
007D13 _H				
007D14 _H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXX _B
007D15 _H				XXXXXXXX XXXXXXXX _B
007D16 _H				
007D17 _H				
007D18 _H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXX _B
007D19 _H				XXXXXXXX XXXXXXXX _B
007D1A _H				
007D1B _H				

List of Message Buffers (ID Registers)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
007C00 _H to 007C1F _H	General-purpose RAM	–	R/W	XXXXXXXX _B to XXXXXXXX _B
007C20 _H	ID register 0	IDR0	R/W	XXXXXXXX XXXXXXXX _B
007C21 _H				
007C22 _H				XXXXXXXX XXXXXXXX _B
007C23 _H				
007C24 _H	ID register 1	IDR1	R/W	XXXXXXXX XXXXXXXX _B
007C25 _H				
007C26 _H				XXXXXXXX XXXXXXXX _B
007C27 _H				
007C28 _H	ID register 2	IDR2	R/W	XXXXXXXX XXXXXXXX _B
007C29 _H				
007C2A _H				XXXXXXXX XXXXXXXX _B
007C2B _H				
007C2C _H	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXX _B
007C2D _H				
007C2E _H				XXXXXXXX XXXXXXXX _B
007C2F _H				
007C30 _H	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXX _B
007C31 _H				
007C32 _H				XXXXXXXX XXXXXXXX _B
007C33 _H				
007C34 _H	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXX _B
007C35 _H				
007C36 _H				XXXXXXXX XXXXXXXX _B
007C37 _H				
007C38 _H	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXX _B
007C39 _H				
007C3A _H				XXXXXXXX XXXXXXXX _B
007C3B _H				
007C3C _H	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX _B
007C3D _H				
007C3E _H				XXXXXXXX XXXXXXXX _B
007C3F _H				

(Continued)

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Address	Register	Abbreviation	Access	Initial Value
CAN1				
007C40 _H	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXX _B
007C41 _H				
007C42 _H				XXXXXXXX XXXXXXXX _B
007C43 _H				
007C44 _H	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXX _B
007C45 _H				
007C46 _H				XXXXXXXX XXXXXXXX _B
007C47 _H				
007C48 _H	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXX _B
007C49 _H				
007C4A _H				XXXXXXXX XXXXXXXX _B
007C4B _H				
007C4C _H	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXX _B
007C4D _H				
007C4E _H				XXXXXXXX XXXXXXXX _B
007C4F _H				
007C50 _H	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXX _B
007C51 _H				
007C52 _H				XXXXXXXX XXXXXXXX _B
007C53 _H				
007C54 _H	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXX _B
007C55 _H				
007C56 _H				XXXXXXXX XXXXXXXX _B
007C57 _H				
007C58 _H	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXX _B
007C59 _H				
007C5A _H				XXXXXXXX XXXXXXXX _B
007C5B _H				
007C5C _H	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXX _B
007C5D _H				
007C5E _H				XXXXXXXX XXXXXXXX _B
007C5F _H				

List of Message Buffers (DLC Registers and Data Registers)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
007C60 _H	DLC register 0	DLCR0	R/W	XXXXXXXX _B
007C61 _H				
007C62 _H	DLC register 1	DLCR1	R/W	XXXXXXXX _B
007C63 _H				
007C64 _H	DLC register 2	DLCR2	R/W	XXXXXXXX _B
007C65 _H				
007C66 _H	DLC register 3	DLCR3	R/W	XXXXXXXX _B
007C67 _H				
007C68 _H	DLC register 4	DLCR4	R/W	XXXXXXXX _B
007C69 _H				
007C6A _H	DLC register 5	DLCR5	R/W	XXXXXXXX _B
007C6B _H				
007C6C _H	DLC register 6	DLCR6	R/W	XXXXXXXX _B
007C6D _H				
007C6E _H	DLC register 7	DLCR7	R/W	XXXXXXXX _B
007C6F _H				
007C70 _H	DLC register 8	DLCR8	R/W	XXXXXXXX _B
007C71 _H				
007C72 _H	DLC register 9	DLCR9	R/W	XXXXXXXX _B
007C73 _H				
007C74 _H	DLC register 10	DLCR10	R/W	XXXXXXXX _B
007C75 _H				
007C76 _H	DLC register 11	DLCR11	R/W	XXXXXXXX _B
007C77 _H				
007C78 _H	DLC register 12	DLCR12	R/W	XXXXXXXX _B
007C79 _H				
007C7A _H	DLC register 13	DLCR13	R/W	XXXXXXXX _B
007C7B _H				
007C7C _H	DLC register 14	DLCR14	R/W	XXXXXXXX _B
007C7D _H				
007C7E _H	DLC register 15	DLCR15	R/W	XXXXXXXX _B
007C7F _H				

(Continued)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
007C80 _H to 007C87 _H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXX _B to XXXXXXXX _B
007C88 _H to 007C8F _H	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX _B to XXXXXXXX _B
007C90 _H to 007C97 _H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX _B to XXXXXXXX _B
007C98 _H to 007C9F _H	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX _B to XXXXXXXX _B
007CA0 _H to 007CA7 _H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX _B to XXXXXXXX _B
007CA8 _H to 007CAF _H	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX _B to XXXXXXXX _B
007CB0 _H to 007CB7 _H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX _B to XXXXXXXX _B
007CB8 _H to 007CBF _H	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX _B to XXXXXXXX _B
007CC0 _H to 007CC7 _H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX _B to XXXXXXXX _B
007CC8 _H to 007CCF _H	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX _B to XXXXXXXX _B
007CD0 _H to 007CD7 _H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX _B to XXXXXXXX _B
007CD8 _H to 007CDF _H	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX _B to XXXXXXXX _B
007CE0 _H to 007CE7 _H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX _B to XXXXXXXX _B
007CE8 _H to 007CEF _H	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX _B to XXXXXXXX _B

(Continued)

(Continued)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
007CF0 _H to 007CF7 _H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX _B to XXXXXXXX _B
007CF8 _H to 007CFF _H	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX _B to XXXXXXXX _B

10. Interrupt Factors, Interrupt Vectors, Interrupt Control Register

Interrupt cause	EI ² OS corresponding	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N	#08	FFFFDC _H	–	–
INT9 instruction	N	#09	FFFFD8 _H	–	–
Exception	N	#10	FFFFD4 _H	–	–
Reserved	N	#11	FFFFD0 _H	ICR00	0000B0 _H
Reserved	N	#12	FFFFCC _H		
CAN 1 reception	N	#13	FFFFC8 _H	ICR01	0000B1 _H
CAN 1 transmission/node status	N	#14	FFFFC4 _H		
Reserved	N	#15	FFFFC0 _H	ICR02	0000B2 _H
Reserved	N	#16	FFFFBC _H		
Reserved	N	#17	FFFFB8 _H	ICR03	0000B3 _H
Reserved	N	#18	FFFFB4 _H		
16-bit reload timer 2	Y1	#19	FFFFB0 _H	ICR04	0000B4 _H
16-bit reload timer 3	Y1	#20	FFFFAC _H		
Reserved	N	#21	FFFFA8 _H	ICR05	0000B5 _H
Reserved	N	#22	FFFFA4 _H		
PPG C/D	N	#23	FFFFA0 _H	ICR06	0000B6 _H
PPG E/F	N	#24	FFFF9C _H		
Timebase timer	N	#25	FFFF98 _H	ICR07	0000B7 _H
External interrupt 8 to 11	Y1	#26	FFFF94 _H		
Watch timer	N	#27	FFFF90 _H	ICR08	0000B8 _H
External interrupt 12 to 15	Y1	#28	FFFF8C _H		
A/D converter	Y1	#29	FFFF88 _H	ICR09	0000B9 _H
16-bit free-run timer 0	N	#30	FFFF84 _H		
Reserved	N	#31	FFFF80 _H	ICR10	0000BA _H
Reserved	N	#32	FFFF7C _H		
Input capture 0 to 3	Y1	#33	FFFF78 _H	ICR11	0000BB _H
Reserved	N	#34	FFFF74 _H		
LIN-UART 0 reception	Y2	#35	FFFF70 _H	ICR12	0000BC _H
LIN-UART 0 transmission	Y1	#36	FFFF6C _H		
LIN-UART 1 reception	Y2	#37	FFFF68 _H	ICR13	0000BD _H
LIN-UART 1 transmission	Y1	#38	FFFF64 _H		

(Continued)

(Continued)

Interrupt cause	EI ² OS corresponding	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reserved	N	#39	FFFF60 _H	ICR14	0000BE _H
Reserved	N	#40	FFFF5C _H		
Flash memory	N	#41	FFFF58 _H	ICR15	0000BF _H
Delayed interrupt generation module	N	#42	FFFF54 _H		

Y1 : Usable

Y2 : Usable, with EI²OS stop function

N : Unusable

- Notes:
- The peripheral resources sharing the ICR register have the same interrupt level.
 - When the peripheral resources sharing the ICR register use extended intelligent I/O service, only one can use extended intelligent I/O service at a time.
 - When either of the 2 peripheral resources sharing the ICR register specifies extended intelligent I/O service, the other one cannot use interrupts.

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

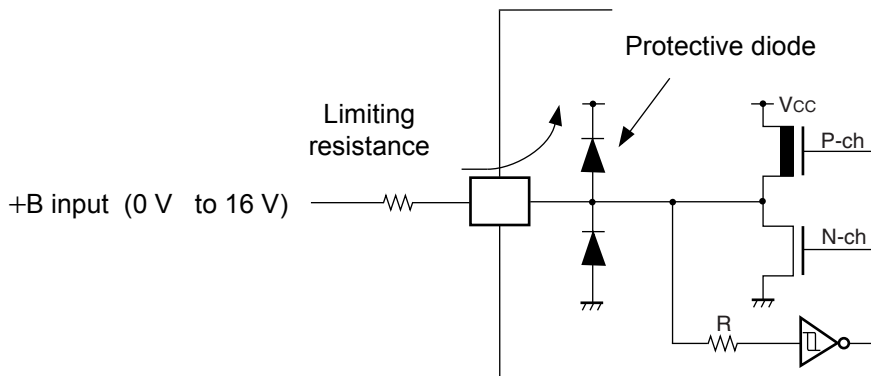
Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ *2
	AVR	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AVR$ *2
Input voltage*1	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Output voltage*1	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Maximum clamp current	I_{CLAMP}	-2.0	+2.0	mA	*6
Total Maximum clamp current	$\Sigma I_{CLAMP} $	—	40	mA	*6
“L” level maximum output current	I_{OL1}	—	15	mA	*4
	I_{OL2}	—	40	mA	*5
“L” level average output current	I_{OLAV1}	—	4	mA	*4
	I_{OLAV2}	—	30	mA	*5
“L” level maximum overall output current	ΣI_{OL1}	—	125	mA	*4
	ΣI_{OL2}	—	160	mA	*5
“L” level average overall output current	ΣI_{OLAV1}	—	40	mA	*4 $+105^\circ\text{C} < T_A \leq +125^\circ\text{C}$
	ΣI_{OLAV2}				*5 $+105^\circ\text{C} < T_A \leq +125^\circ\text{C}$
	ΣI_{OLAV1}	—	40	mA	*4 $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$
	ΣI_{OLAV2}				*5 $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$
“H” level maximum output current	I_{OH1}	—	-15	mA	*4
	I_{OH2}	—	-40	mA	*5
“H” level average output current	I_{OHAV1}	—	-4	mA	*4
	I_{OHAV2}	—	-30	mA	*5
“H” level maximum overall output current	ΣI_{OH1}	—	-125	mA	*4
	ΣI_{OH2}	—	-160	mA	*5
“H” level average overall output current	ΣI_{OHAV1}	—	-40	mA	*4 $+105^\circ\text{C} < T_A \leq +125^\circ\text{C}$
	ΣI_{OHAV2}				*5 $+105^\circ\text{C} < T_A \leq +125^\circ\text{C}$
	ΣI_{OHAV1}	—	-40	mA	*4 $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$
	ΣI_{OHAV2}				*5 $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$
Power consumption	P_D	—	308	mW	Flash memory update not performed
		—	390	mW	Flash memory update performed
Operating temperature	T_A	-40	+105	°C	
		-40	+125	°C	*7
Storage temperature	T_{STG}	-55	+150	°C	

(Continued)

(Continued)

- *1: This parameter is based on $V_{SS} = AV_{SS} = 0$ V.
- *2: Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.
- *3: V_I and V_O should not exceed $V_{CC} + 0.3$ V. V_I should not exceed the specified ratings. However, if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.
- *4: Applicable to pins : P24 to P27, P40 to P44, P50 to P57, P60 to P67, P80, P82 to P87
- *5: Applicable to pins : P20 to P23
- *6: Applicable to pins: P20 to P27, P40 to P44, P50 to P57, P60 to P67, P80, P82 to P87
 - Use within recommended operating conditions.
 - Use at DC voltage (current) .
 - The +B signal should always be applied a connecting limit resistance between the +B signal and the microcontroller.
 - The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
 - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
 - Note that if a +B signal is inputted when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
 - Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
 - Care must be taken not to leave the +B input pin open.
 - Recommended circuit sample:

• **Input/output equivalent circuits**



- *7: There is a restriction of reliability if the product is used exceeding $T_A = +105$ °C.
Contact the sales or support representative.
It is ensured to write/erase data to the Flash memory between $T_A = -40$ °C and $+105$ °C.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

11.2 Recommended Conditions

($V_{SS} = AV_{SS} = 0\text{ V}$)

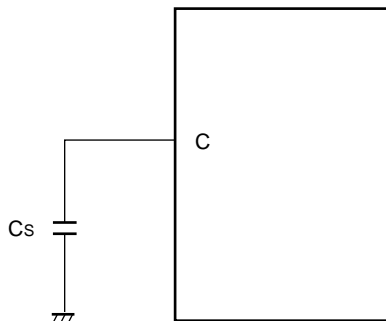
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation when not using the A/D converter and not Flash programming.
		3.0	–	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C_S	0.1	–	1.0	μF	Use a ceramic capacitor or comparable capacitor of the AC characteristics. Bypass capacitor at the V_{CC} pin should be greater than this capacitor.
Operating temperature	T_A	–40	–	+105	°C	
		–40	–	+125	°C	*

*: There is a restriction of reliability if the product is used exceeding $T_A = +105\text{ °C}$.

Contact the sales or support representative.

It is ensured to write/erase data to the Flash memory between $T_A = -40\text{ °C}$ and $+105\text{ °C}$.

• C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges.

Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

11.3 DC Characteristics

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "H" voltage	V_{IHS}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Pin inputs if CMOS hysteresis input levels are selected (except P82, P85)
	V_{IHA}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Pin inputs if Automotive input levels are selected
	V_{IHS}	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	P82, P85 inputs if CMOS input levels are selected
	V_{IHR}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	$\overline{\text{RST}}$ input pin (CMOS hysteresis)
	V_{IHM}	—	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	MD input pin
Input "L" voltage	V_{ILS}	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Pin inputs if CMOS hysteresis input levels are selected (except P82, P85)
	V_{ILA}	—	—	$V_{SS} - 0.3$	—	$0.5 V_{CC}$	V	Pin inputs if Automotive input levels are selected
	V_{ILS}	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	P82, P85 inputs if CMOS input levels are selected
	V_{ILR}	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	$\overline{\text{RST}}$ input pin (CMOS hysteresis)
	V_{ILM}	—	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	MD input pin
Output "H" voltage	V_{OH}	Other than P20 to P23	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
	V_{OHI}	P20 to P23	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -14.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output "L" voltage	V_{OL}	Other than P20 to P23	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
	V_{OLI}	P20 to P23	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 20.0\text{ mA}$	—	—	0.4	V	
Input leak current	I_{IL}	—	$V_{CC} = 5.5\text{ V}$, $V_{SS} < V_I < V_{CC}$	-1	—	+1	μA	
Pull-up resistance	R_{UP}	P20 to P27, $\overline{\text{RST}}$	—	25	50	100	$\text{k}\Omega$	

(Continued)

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Sym- bol	Pin	Condition		Value			Unit	Remarks	
					Min	Typ	Max			
Pull-down resistance	R _{DOWN}	MD2	–		25	50	100	kΩ	MB90362E, MB90362ES, MB90362TE, MB90362TES	
Power supply current*	I _{CC}	V _{CC}	V _{CC} = 5.0 V, Internal frequency: 24 MHz, At normal operation.		–	35	45	mA		
			V _{CC} = 5.0 V, Internal frequency: 24 MHz, At writing Flash memory.		–	50	60	mA	Flash memory devices	
			V _{CC} = 5.0 V, Internal frequency: 24 MHz, At erasing Flash memory.		–	50	60	mA	Flash memory devices	
	I _{CCS}		V _{CC} = 5.0 V, Internal frequency: 24 MHz, At sleep mode.		–	12	20	mA		
	I _{CTS}		V _{CC} = 5.0 V, Internal frequency: 2 MHz, At main timer mode		–	0.3	0.8	mA	Devices without T-suffix	
					–	0.4	1.0		Devices with T-suffix	
	I _{CTSPLL 6}		V _{CC} = 5.0 V, Internal frequency: 24 MHz, At PLL timer mode, External frequency = 4 MHz		–	4	7	mA		
	I _{CCL}		V _{CC} = 5.0 V Internal frequency: 8 kHz, At sub operation, T _A = +25°C		Stopping clock supervisor	–	40	100	μA	MB90F362E, MB90F367E, MB90362E, MB90367E
					Operating clock supervisor	–	60	150		MB90F367E, MB90367E
					Stopping clock supervisor	–	90	200		MB90F362TE, MB90F367TE, MB90362TE, MB90367TE
					Operating clock supervisor	–	110	250		MB90F367TE, MB90367TE
	I _{CCLS}		V _{CC} = 5.0 V Internal frequency: 8 kHz, At sub sleep, T _A = +25°C		Stopping clock supervisor	–	10	50	μA	MB90F362E, MB90F367E, MB90362E, MB90367E
					Operating clock supervisor	–	30	100		MB90F367E, MB90367E
					Stopping clock supervisor	–	60	150		MB90F362TE, MB90F367TE, MB90362TE, MB90367TE
					Operating clock supervisor	–	80	200		MB90F367TE, MB90367TE

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($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Sym- bol	Pin	Condition		Value			Unit	Remarks
					Min	Typ	Max		
Power supply current*	I_{CCT}	V_{CC}	$V_{CC} = 5.0\text{ V}$ Internal frequency: 8 kHz, At watch mode, $T_A = +25^{\circ}\text{C}$	Stopping clock supervisor	–	8	30	μA	MB90F362E, MB90F367E, MB90362E, MB90367E
				Operating clock supervisor	–	30	70		MB90F367E, MB90367E
				Stopping clock supervisor	–	60	130		MB90F362TE, MB90F367TE, MB90362TE, MB90367TE
				Operating clock supervisor	–	80	170		MB90F367TE, MB90367TE
	I_{CCH}	V_{CC}	$V_{CC} = 5.0\text{ V}$, At stop mode, $T_A = +25^{\circ}\text{C}$		–	5	25	μA	Devices without T-suffix
					–	50	130	μA	Devices with T-suffix
Input capacity	C_{IN}	Other than AV_{CC} , AV_{SS} , AVR, V_{CC} , V_{SS} , C	–		–	5	15	pF	

*: The power supply current is measured with an external clock.

11.4 AC Characteristics

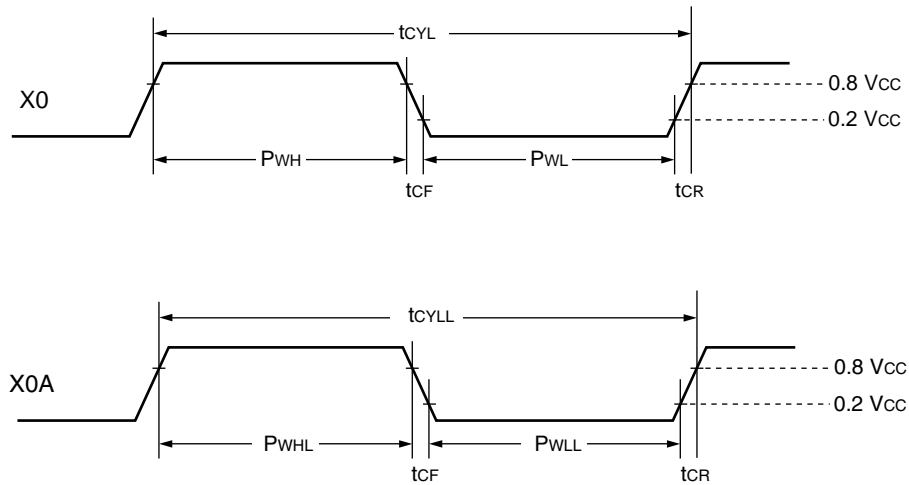
11.4.1 Clock Timing

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

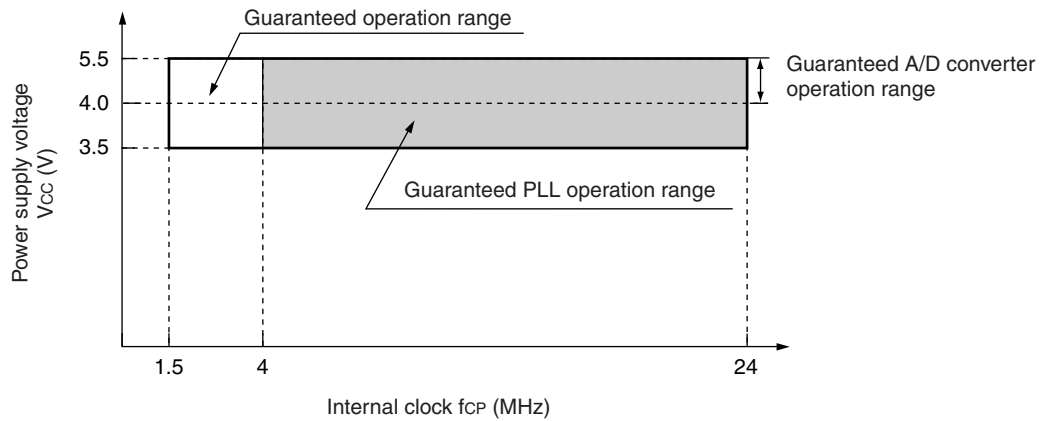
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency*	f_C	X0, X1	3	—	16	MHz	1/2 when PLL stops, When using an oscillation circuit
			4	—	16	MHz	PLL $\times 1$, When using an oscillation circuit
			4	—	12	MHz	PLL $\times 2$, When using an oscillation circuit
			4	—	8	MHz	PLL $\times 3$, When using an oscillation circuit
			4	—	6	MHz	PLL $\times 4$, When using an oscillation circuit
			4	—	4	MHz	PLL $\times 6$, When using an oscillation circuit
		X0, X1	3	—	24	MHz	1/2 when PLL stops, When using an external clock
			4	—	24	MHz	PLL $\times 1$, When using an external clock
			4	—	12	MHz	PLL $\times 2$, When using an external clock
			4	—	8	MHz	PLL $\times 3$, When using an external clock
			4	—	6	MHz	PLL $\times 4$, When using an external clock
			4	—	4	MHz	PLL $\times 6$, When using an external clock
	fCL	X0A, X1A	—	32.768	100	kHz	
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0, X1	41.67	—	333	ns	When using an external clock
	t_{CYLL}	X0A, X1A	10	30.5	—	μs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WHL}, P_{WLL}	X0A	5	15.2	—	μs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Internal operating clock frequency (machine clock)	f_{CP}	—	1.5	—	24	MHz	When using main clock
	f_{CPL}	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	41.67	—	666	ns	When using main clock
	t_{CPL}	—	20	122.1	—	μs	When using sub clock

*: When selecting the PLL clock, the range of clock frequency is limited. Use this product within range as mentioned in "Relation among external clock frequency and internal clock frequency".

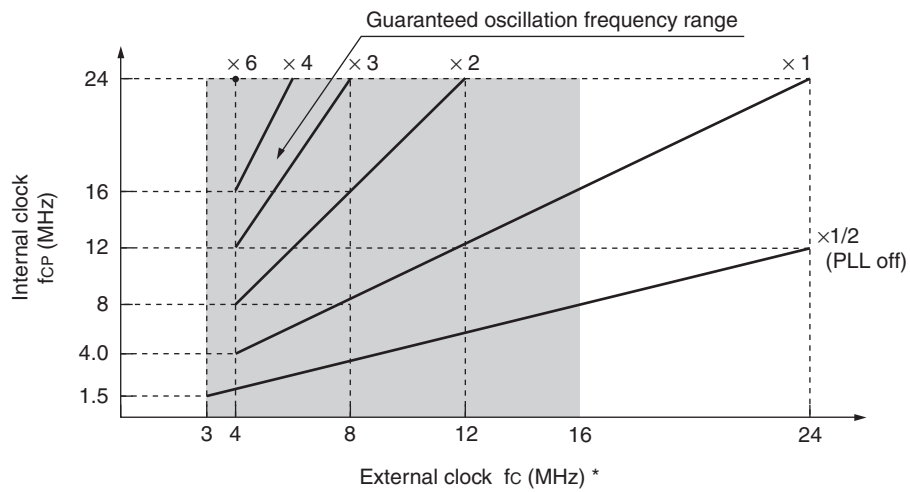
● **Clock Timing**



• **Guaranteed PLL Operation Range**



Guaranteed operation range of MB90360E series



*: When using the oscillation circuit, the maximum oscillation clock frequency is 16 MHz.

11.4.2 Reset Standby Input

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

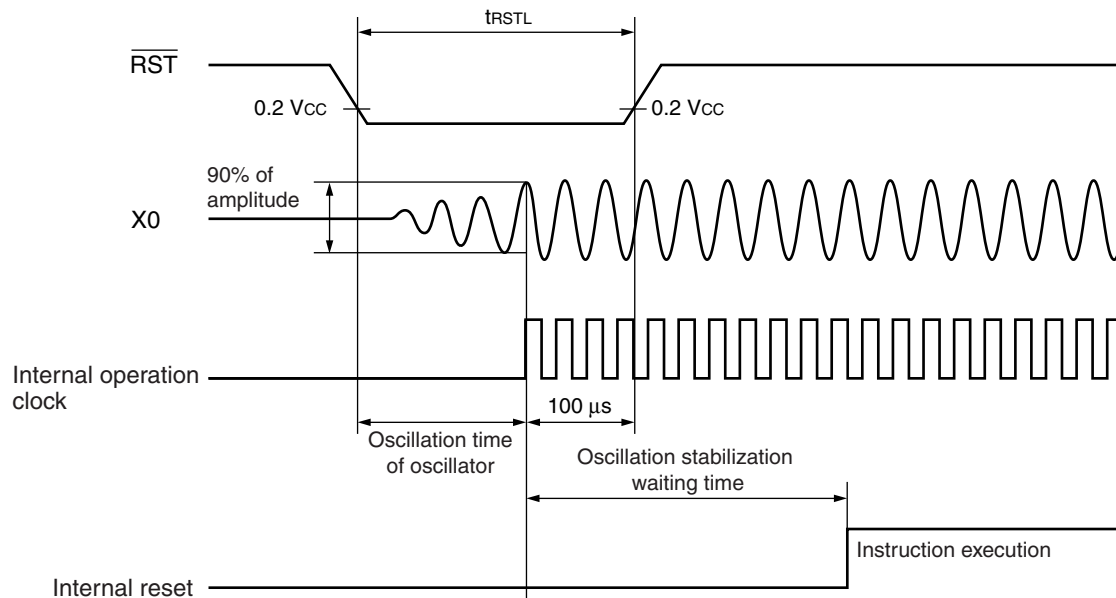
Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	\overline{RST}	500	—	ns	Under normal operation
			Oscillation time of oscillator* + 100 μs	—	μs	In stop mode, sub clock mode, sub sleep mode, and watch mode
			100	—	μs	In timebase timer mode

*: Oscillation time of oscillator is the time that the amplitude reaches 90%. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In ceramic oscillators, the oscillation time is between hundreds of μs and several ms. With an external clock, the oscillation time is 0 ms.

• Under normal operation:



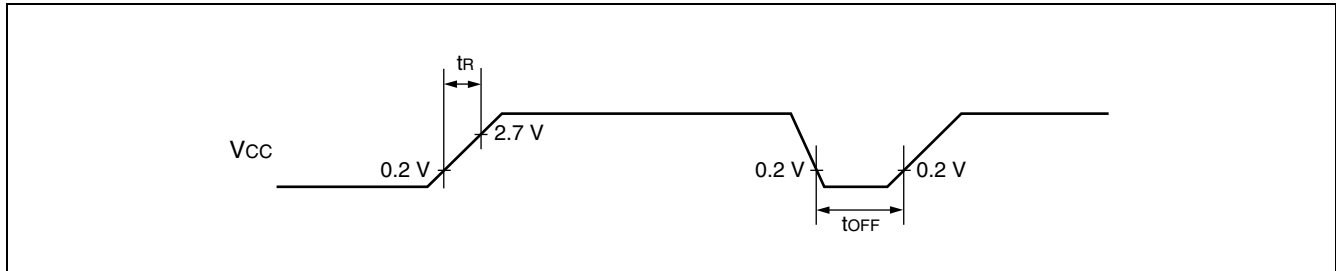
• In stop mode, sub clock mode, sub sleep mode, and watch mode:



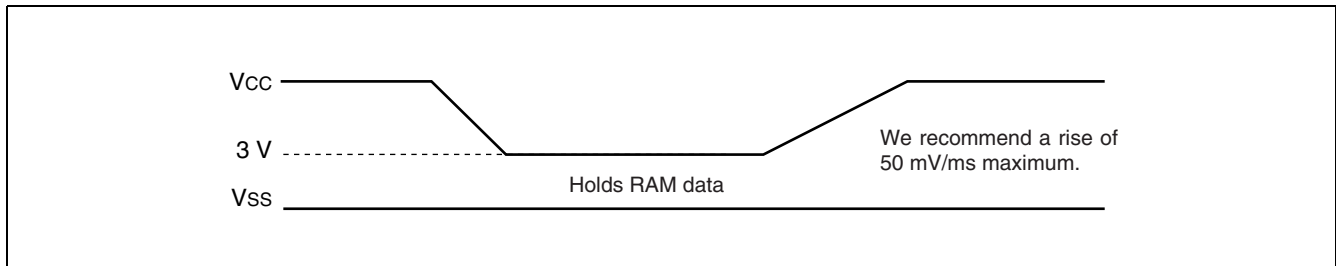
11.4.3 Power-on Reset

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		1	—	ms	Due to repetitive operation



Note: If you change the power supply voltage too rapidly, a power-on reset may occur. We recommend that you start up smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.



11.4.4 LIN-UART0/1

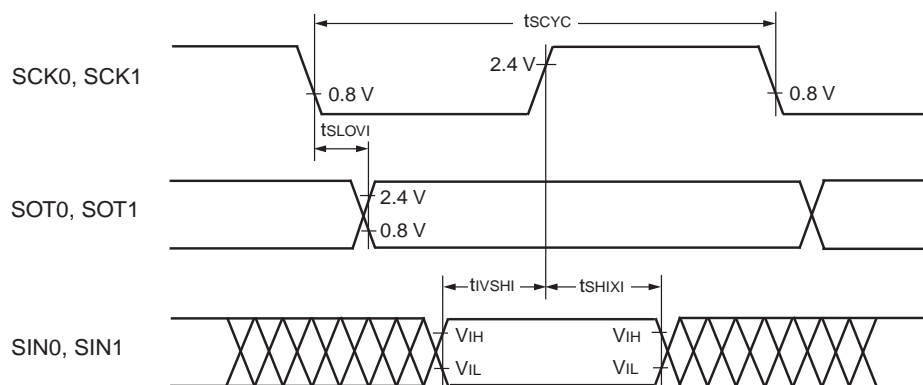
■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

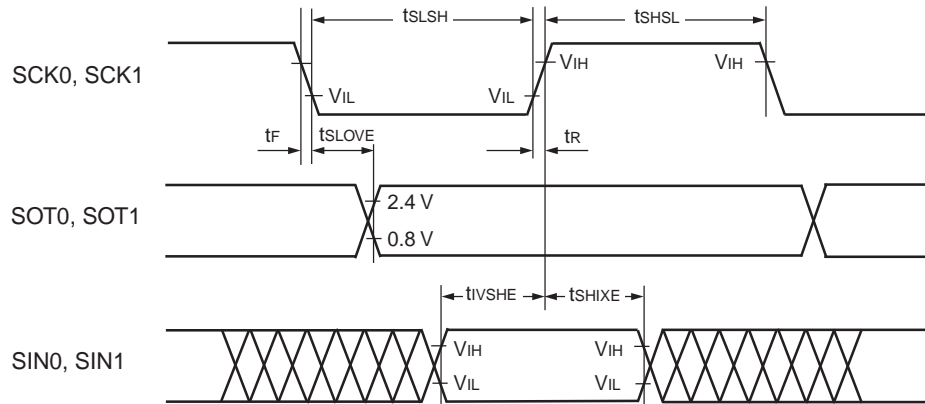
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0, SCK1	Internal shift clock mode output pins are $CL = 80\text{ pF} + 1\text{ TTL}$.	$5 t_{CP}$	–	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVI}	SCK0, SCK1, SOT0, SOT1		–50	+50	ns
Valid SIN \rightarrow SCK \uparrow	t_{IVSHI}	SCK0, SCK1, SIN0, SIN1		$t_{CP} + 80$	–	ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	t_{SHIXI}	SCK0, SCK1, SIN0, SIN1		0	–	ns
Serial clock “L” pulse width	t_{SHSL}	SCK0, SCK1	External shift clock mode output pins are $CL = 80\text{ pF} + 1\text{ TTL}$.	$3 t_{CP} - t_R$	–	ns
Serial clock “H” pulse width	t_{SLSH}	SCK0, SCK1		$t_{CP} + 10$	–	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVE}	SCK0, SCK1, SOT0, SOT1		–	$2 t_{CP} + 60$	ns
Valid SIN \rightarrow SCK \uparrow	t_{IVSHE}	SCK0, SCK1, SIN0, SIN1		30	–	ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	t_{SHIXE}	SCK0, SCK3, SIN0, SIN1		$t_{CP} + 30$	–	ns
SCK fall time	t_F	SCK0, SCK1		–	10	ns
SCK rise time	t_R	SCK0, SCK1		–	10	ns

- Notes:
- AC characteristic in CLK synchronized mode.
 - C_L is load capacity value of pins when testing.
 - t_{CP} is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.

• Internal Shift Clock Mode



• External Shift Clock Mode



■ Bit setting: ESCR:SCES = 1, ECCR:SCDE = 0

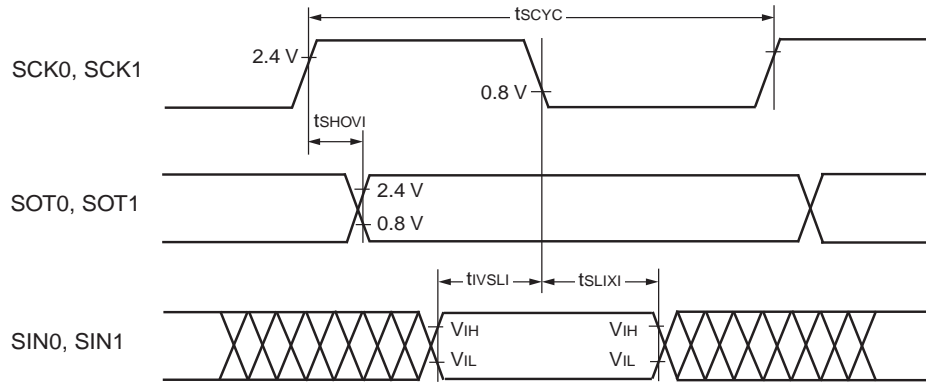
($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0, SCK1	Internal shift clock mode output pins are $CL = 80\text{ pF} + 1\text{ TTL}$.	$5 t_{CP}$	–	ns
SCK $\uparrow \rightarrow$ SOT delay time	t_{SHOVI}	SCK0, SCK1, SOT0, SOT1		–50	+50	ns
Valid SIN \rightarrow SCK \downarrow	t_{IVSLI}	SCK0, SCK1, SIN0, SIN1		$t_{CP} + 80$	–	ns
SCK $\downarrow \rightarrow$ Valid SIN hold time	t_{SLIXI}	SCK0, SCK1, SIN0, SIN1		0	–	ns
Serial clock “H” pulse width	t_{SHSL}	SCK0, SCK1	External shift clock mode output pins are $CL = 80\text{ pF} + 1\text{ TTL}$.	$3 t_{CP} - t_R$	–	ns
Serial clock “L” pulse width	t_{SLSH}	SCK0, SCK1		$t_{CP} + 10$	–	ns
SCK $\uparrow \rightarrow$ SOT delay time	t_{SHOVE}	SCK0, SCK1, SOT0, SOT1		–	$2 t_{CP} + 60$	ns
Valid SIN \rightarrow SCK \downarrow	t_{IVSLE}	SCK0, SCK1, SIN0, SIN1		30	–	ns
SCK $\downarrow \rightarrow$ Valid SIN hold time	t_{SLIXE}	SCK0, SCK1, SIN0, SIN1		$t_{CP} + 30$	–	ns
SCK fall time	t_F	SCK0, SCK1		–	10	ns
SCK rise time	t_R	SCK0, SCK1		–	10	ns

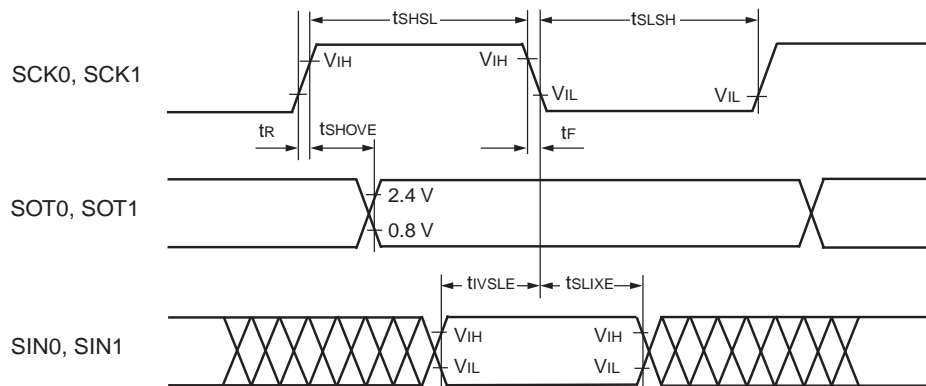
Notes:

- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.

• Internal Shift Clock Mode



• External Shift Clock Mode

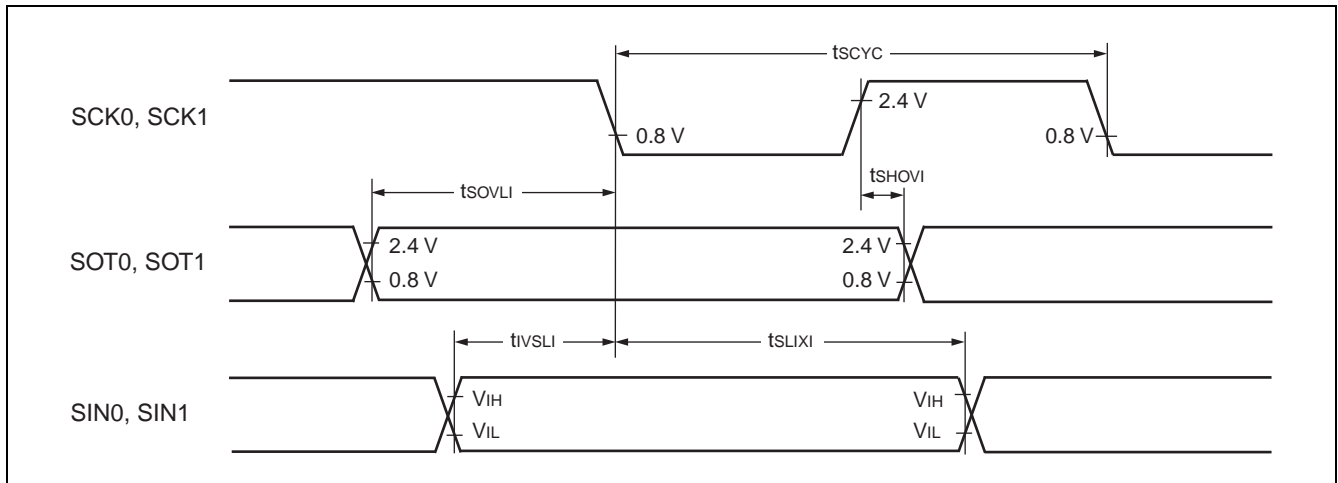


■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 1

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0, SCK1	Internal clock operation output pins are $CL = 80\text{ pF} + 1\text{ TTL}$.	$5\ t_{CP}$	—	ns
SCK $\uparrow \rightarrow$ SOT delay time	t_{SHOVI}	SCK0, SCK1, SOT0, SOT1		-50	+50	ns
Valid SIN \rightarrow SCK \downarrow	t_{IVSLI}	SCK0, SCK1, SIN0, SIN1		$t_{CP} + 80$	—	ns
SCK $\downarrow \rightarrow$ Valid SIN hold time	t_{SLIXI}	SCK0, SCK1, SIN0, SIN1		0	—	ns
SOT \rightarrow SCK \downarrow delay time	t_{SOVLI}	SCK0, SCK1, SOT0, SOT1		$3\ t_{CP} - 70$	—	ns

Notes: • C_L is load capacity value of pins when testing.
• t_{CP} is internal operating clock cycle time (machine clock) . Refer to "Clock Timing".

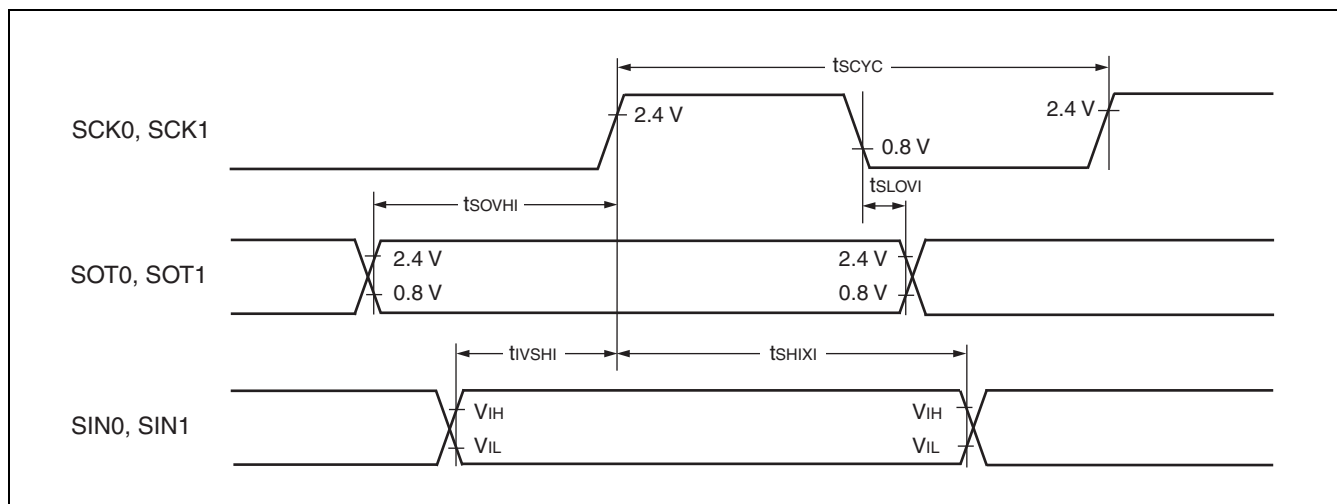


■ Bit setting: ESCR:SCES = 1, ECCR:SCDE = 1

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0, SCK1	Internal clock operation output pins are $CL = 80\text{ pF} + 1\text{ TTL}$.	$5 t_{CP}$	–	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVI}	SCK0, SCK1, SOT0, SOT1		–50	+50	ns
Valid SIN \rightarrow SCK \uparrow	t_{IVSHI}	SCK0, SCK1, SIN0, SIN1		$t_{CP} + 80$	–	ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	t_{SHIXI}	SCK0, SCK1, SIN0, SIN1		0	–	ns
SOT \rightarrow SCK \uparrow delay time	t_{SOVHI}	SCK0, SCK1, SOT0, SOT1		$3 t_{CP} - 70$	–	ns

- Notes:
- C_L is load capacity value of pins when testing.
 - t_{CP} is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.



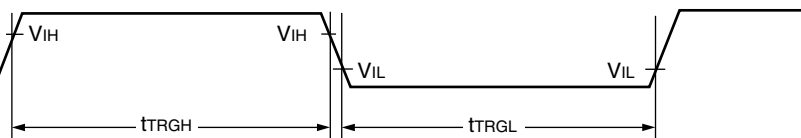
11.4.5 Trigger Input Timing

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	INT8, INT9R INT10, INT11 INT12R, INT13 INT14R, INT15R ADTG	–	$5 t_{CP}$	–	ns

Note: t_{CP} is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.

INT8, INT9R
INT10, INT11
INT12R, INT13
INT14R, INT15R
ADTG



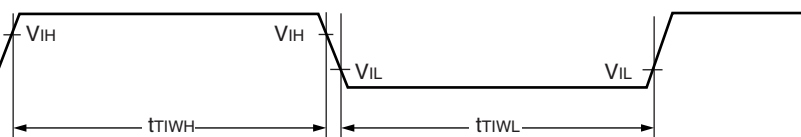
11.4.6 Timer Related Resource Input Timing

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH}	TIN2, TIN3 INO to IN3	—	$4 t_{CP}$	—	ns
	t_{TIWL}					

Note: t_{CP} is internal operating clock cycle time (machine clock) . Refer to “[Clock Timing](#)”.

TIN2, TIN3
INO to IN3



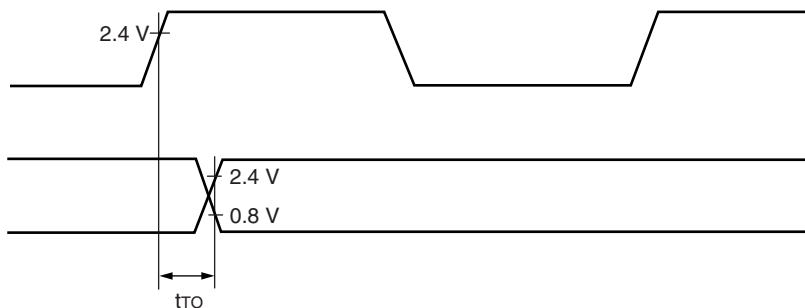
11.4.7 Timer Related Resource Output Timing

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
CLK \uparrow \rightarrow T_{OUT} change time	t_{TO}	TOT2, TOT3 PPGC to PPGF	—	30	—	ns

CLK

TOT2, TOT3
PPGC to PPGF



11.5 A/D Converter

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $3.0\text{ V} \leq AV_{SS}$, $V_{CC} = AV_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

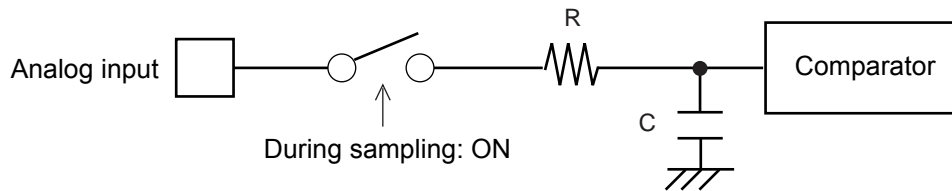
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	–	–	–	–	10	bit	
Total error	–	–	–	–	± 3.0	LSB	
Nonlinearity error	–	–	–	–	± 2.5	LSB	
Differential nonlinearity error	–	–	–	–	± 1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN15	$AV_{SS} - 1.5 \times \text{LSB}$	$AV_{SS} + 0.5 \times \text{LSB}$	$AV_{SS} + 2.5 \times \text{LSB}$	V	
Full scale reading voltage	V_{FST}	AN0 to AN15	$AVR - 3.5 \times \text{LSB}$	$AVR - 1.5 \times \text{LSB}$	$AVR + 0.5 \times \text{LSB}$	V	
Compare time	–	–	1.0	–	16500	μs	$4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$
			2.0				$4.0\text{ V} \leq AV_{CC} < 4.5\text{ V}$
Sampling time	–	–	0.5	–	∞	μs	$4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$
			1.2				$4.0\text{ V} \leq AV_{CC} < 4.5\text{ V}$
Analog port input current	I_{AIN}	AN0 to AN15	–0.3	–	+0.3	μA	
Analog input voltage range	V_{AIN}	AN0 to AN15	AV_{SS}	–	AVR	V	
Reference voltage range	–	AVR	$AV_{SS} + 2.7$	–	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	–	3.5	7.5	mA	
	I_{AH}	AV_{CC}	–	–	5	μA	*
Reference voltage supply current	I_R	AVR	–	600	900	μA	
	I_{RH}	AVR	–	–	5	μA	*
Offset between input channels	–	AN0 to AN15	–	–	4	LSB	

*: If A/D converter is not operating, a current when CPU is stopped is applicable ($V_{CC} = AV_{CC} = AVR = 5.0\text{ V}$).

• **About the external impedance of analog input and its sampling time**

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage changed to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. And, if the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

• **Analog input equivalent circuit model**



MB90F362E/TE/ES/TES, MB90F367E/TE/ES/TES

	R	C
$4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$	2.0 k Ω (Max)	16.0 pF (Max)
$4.0\text{ V} \leq AV_{CC} < 4.5\text{ V}$	8.2 k Ω (Max)	16.0 pF (Max)

MB90362E/TE/ES/TES, MB90367E/TE/ES/TES,
MB90V340E-101/102/103/104

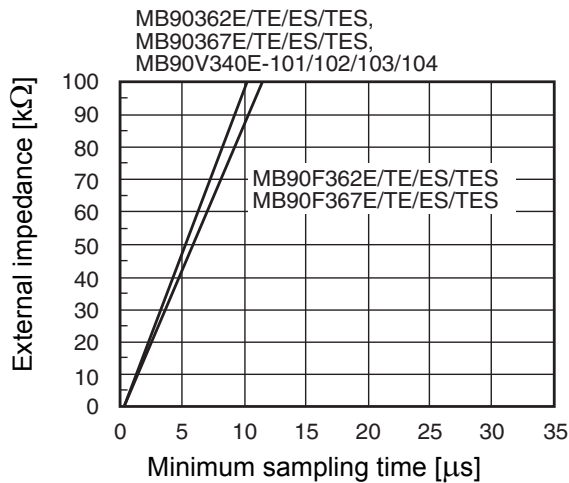
	R	C
$4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$	2.0 k Ω (Max)	14.4 pF (Max)
$4.0\text{ V} \leq AV_{CC} < 4.5\text{ V}$	8.2 k Ω (Max)	14.4 pF (Max)

Note: The values are reference values.

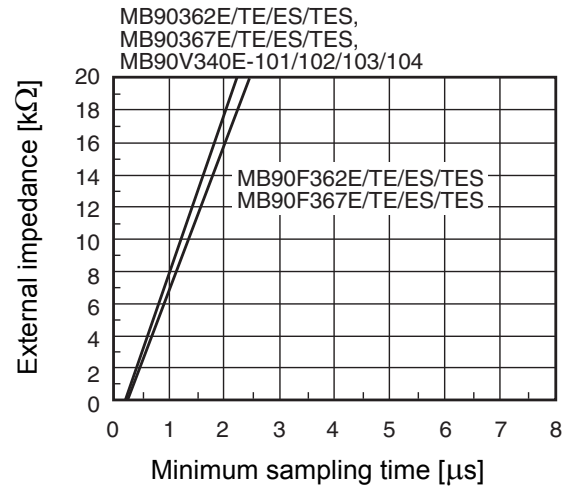
- The relationship between external impedance and minimum sampling time

- At $4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$

(External impedance = 0 kΩ to 100 kΩ)

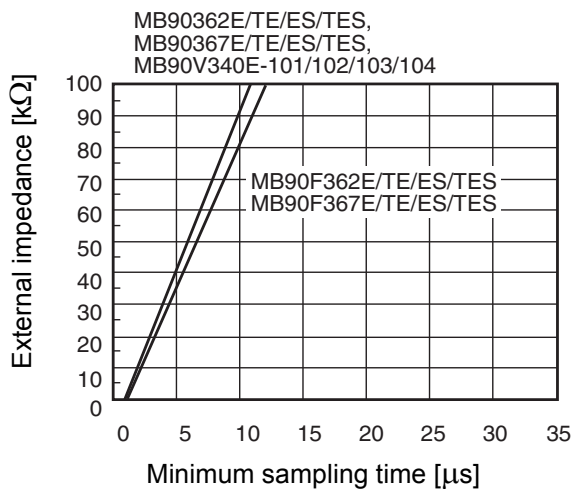


(External impedance = 0 kΩ to 20 kΩ)

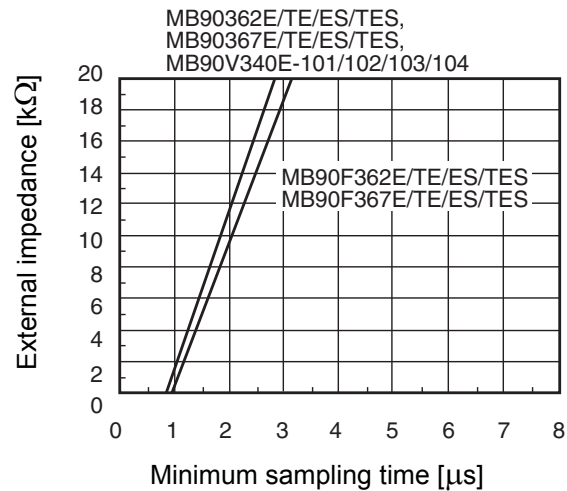


- At $4.0\text{ V} \leq AV_{CC} < 4.5\text{ V}$

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)

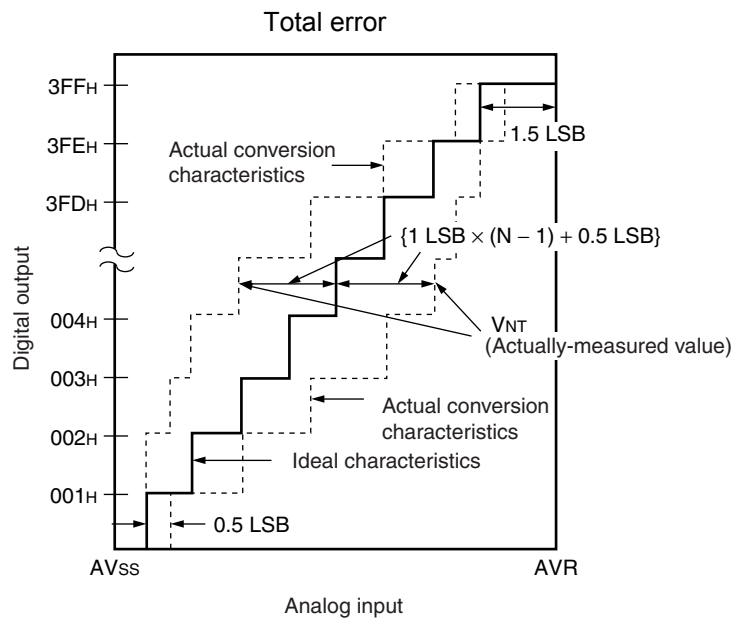


• About errors

As $|AVR - AV_{SS}|$ becomes smaller, values of relative errors grow larger.

11.6 Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Non linearity error : Deviation between a line across zero-transition line (“00 0000 0000_B” ← → “00 0000 0001_B”) and full-scale transition line (“11 1111 1110_B” ← → “11 1111 1111_B”) and actual conversion characteristics.
- Differential linearity error : Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error : Difference between an actual value and an theoretical value. A total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$1 \text{ LSB (Ideal value)} = \frac{AVR - AV_{SS}}{1024} \text{ [V]}$$

N: A/D converter digital output value

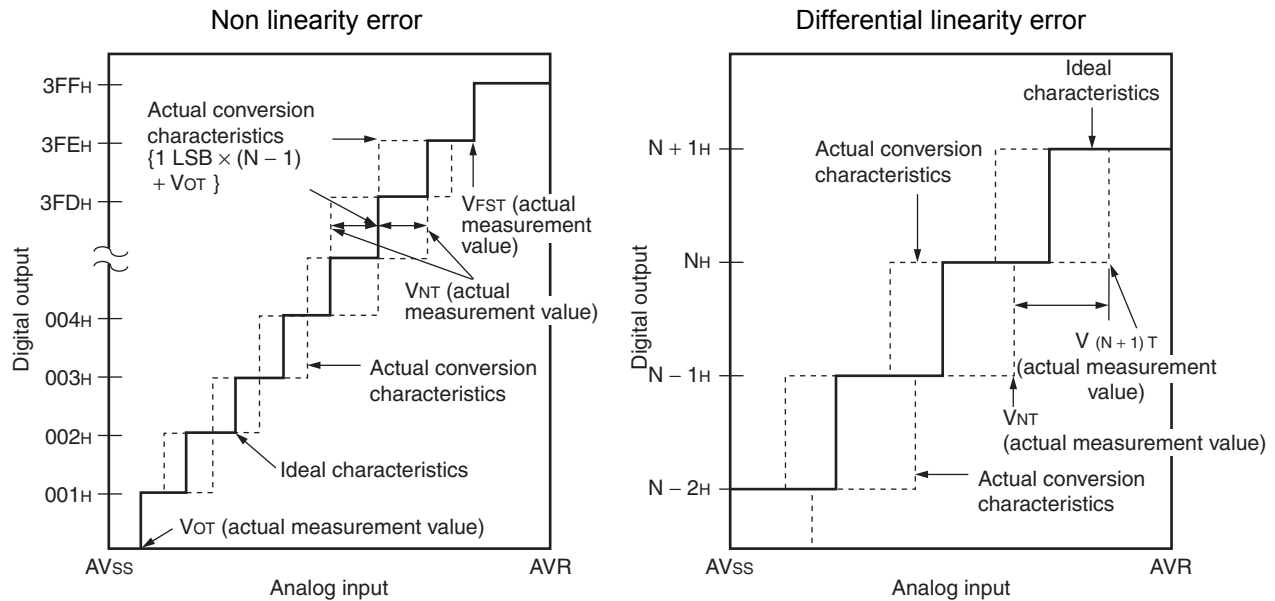
$$V_{OT} \text{ (Ideal value)} = AV_{SS} + 0.5 \text{ LSB [V]}$$

$$V_{FST} \text{ (Ideal value)} = AVR - 1.5 \text{ LSB [V]}$$

V_{NT} : A voltage at which digital output transits from (N - 1) to N.

(Continued)

(Continued)



$$\text{Non linearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \text{ LSB [LSB]}$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N : A/D converter digital output value

V_{OT}: Voltage at which digital output transits from “000_H” to “001_H.”

V_{FST}: Voltage at which digital output transits from “3FE_H” to “3FF_H.”

11.7 Flash Memory Program/Erase Characteristics

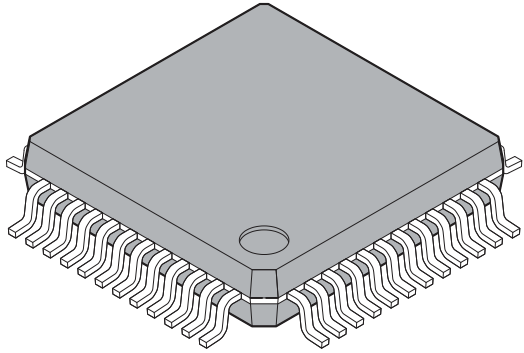
Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Chip erase time	T _A = -40 °C to +105 °C V _{CC} = 5.0 V	—	1	15	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	16	3600	μs	Except for the overhead time of the system level
Program/Erase cycle	—	10000	—	—	cycle	
Flash memory data retention time	Average T _A = +85 °C	20	—	—	year	*

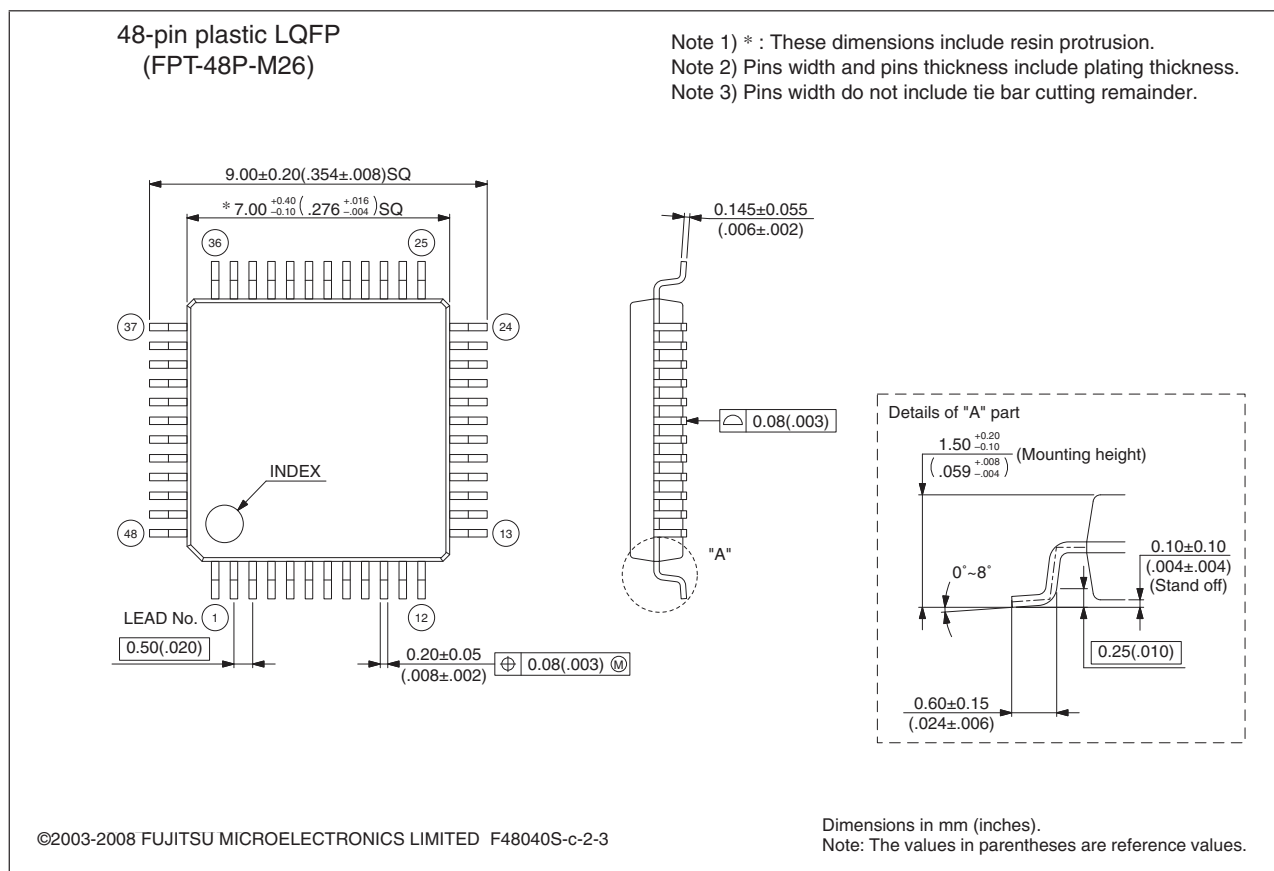
*: Corresponding value comes from the technology reliability evaluation result (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

12. Ordering Information

Part number	Package	Remarks
MB90F362EPMT	48-pin plastic LQFP (FPT-48P-M26)	
MB90F362TEPMT		
MB90F362ESPMT		
MB90F362TESPMT		
MB90F367EPMT		
MB90F367TEPMT		
MB90F367ESPMT		
MB90F367TESPMT		
MB90362EPMT		
MB90362TEPMT		
MB90362ESPMT		
MB90362TESPMT		
MB90367EPMT		
MB90367TEPMT		
MB90367ESPMT		
MB90367TESPMT		
MB90V340E-101CR	299-pin ceramic PGA (PGA-299C-A01)	For evaluation
MB90V340E-102CR		
MB90V340E-103CR		
MB90V340E-104CR		

13. Package Dimension

<p>48-pin plastic LQFP</p>  <p>(FPT-48P-M26)</p>	Lead pitch	0.50 mm
	Package width × package length	7 × 7 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.17 g
	Code (Reference)	P-LFQFP48-7×7-0.50



14. Major Changes

Spanion Publication Number: DS07-13746-3Et

Page	Section	Change Results
—	—	Changed are following names. UART → LIN-UART 16-bit I/O timer → 16-bit free-run timer
4, 5	Product Lineup	Added the row of LIN-UART.
15	Handling Devices	Added the item "17.Serial communication".
37	Electrical Characteristics Absolute Maximum Ratings	Changed the maximum rating values and Remarks on Ratings of Power consumption. 300 → 308 Flash memory updata not performed 390 Flash memory updata performed
48 to 52	AC Characteristics	Changed the characteristics of (4)LIN-UART0/1. (4) UART0/UART1 → (4)LIN-UART0/1
55	A/D Converter	Changed the items of "Zero reading voltage" and "Full scale reading voltage".
61	Ordering Information	Changed the part numbers; MB90V340E-101 → MB90V340E-101CR MB90V340E-102 → MB90V340E-102CR MB90V340E-103 → MB90V340E-103CR MB90V340E-104 → MB90V340E-104CR

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: MB90360E Series F ² MC-16LX 16-bit Microcontroller Datasheet Document Number: 002-04496				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	AKIH	11/16/2006	Migrated to Cypress and assigned document number 002-04496. No change to document contents or format.
*A	5223311	AKIH	04/19/2016	Updated to Cypress template

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