

MERUS™ 2x200W Class D Amplifier, with Analog Inputs and Integrated 24.4mΩ R_{DS(ON)} Output Stage

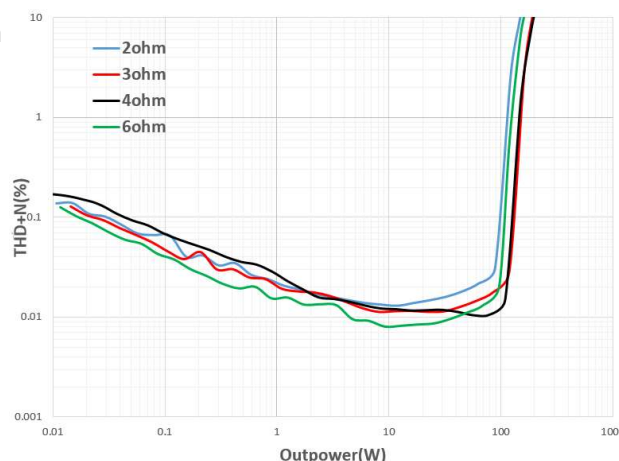
Features

- Integrated output stage with 24.4mΩ R_{DS(ON)}
- 2 x 200W P_{OUT} in stereo mode (4Ω, THD=10%)
- 1 x 400W P_{OUT} in mono mode (8Ω, THD=10%)
- Supports both single and split supplies
 - Split supply operational range: ±22 – ±40V
 - Single supply Operational range: +44 – +80V
- 95% full load efficiency into 4Ω
- >70% idle mode efficiency
- Open-drain flag indicators for clipping and fault conditions
- Multiple configuration: single-ended, BTL & PSE (Parallel Single Ended)
- Programmable power up delay timer (CSD)
 - Click and pop free startup and shutdown
- Integrated protection: OCP, OTP & UVLO
- Pin to pin compatible to MA53x2 family
- Available in QFN 7m x7m – 42 pin



Applications

- Multi-channel home theatre
- Studio monitors
- Active speakers
- Soundbar subwoofer
- Marine amplifiers
- Aftermarket car audio
- General-purpose power amplifiers



Total Harmonic Distortion

Product validation

Qualified for standard applications according to the relevant tests of J-STD-020 and JESD47.

Product type	Package
MA5332MS	7x7mm PG- IQFN-42

Description

The MA5332MS provides output power that is equivalent to or greater than monolithic alternatives, while occupying 50% less space and requiring little or no heatsink. This is achieved through the integration of a 2-channel PWM controller, a high voltage gate driver, and 4 low RDS(ON) MOSFETs in a multi-chip module (MCM) solution. Similar to its predecessor, the IR43x2M, the MA5332MS includes standard Class D protection features that ensure reliable operation across various environmental conditions. With its small 7x7 mm PG-IQFN-42 package, the MA5332MS represents a powerful upgrade over the IR43x2M and other monolithic alternatives, delivering high power density and the benefits of heatsink-less operation.

Topology	Half-bridge / Full bridge
MA5332MS Output power (Half-bridge, THD+N=10%)	*150 W at 2 Ω / 300 W at 4 Ω *200 W at 4 Ω / 400 W at 8 Ω *160 W at 6 Ω / 320W at 12 Ω
Residual noise (AES-17, IHF-A)	*250 μ Vrms
THD+N (1kHz, 70W, 4 Ω)	*0.01 %

**Typical application*

Table of contents

1

Features	1
Applications.....	1
Product validation	1
Description	2
Table of contents.....	3
1 Qualification Information.....	5
2 Device Comparison Table	6
3 Pin Configuration	7
3.1 Lead assignments.....	7
3.2 Lead Definitions.....	8
4 Specifications	9
4.1 Absolute Maximum Ratings	9
4.2 Recommended Operating Conditions.....	10
4.3 Electrical Characteristics	11
4.4 Audio Characteristics (SE).....	16
4.5 Audio characteristics (BTL)	16
4.6 Audio Characteristics (PSE).....	17
4.7 Typical Audio Characteristics (SE).....	18
4.7.1 Power vs. THD+N	18
4.7.2 Frequency vs. THD+N	19
4.7.3 Frequency Response	19
4.7.4 Noise Floor.....	20
4.7.5 Efficiency	20
4.8 Typical Audio Characteristics (BTL).....	21
4.8.1 Power vs. THD+N	21
4.8.2 Frequency vs. THD+N	22
4.8.3 Frequency Response	22
4.8.4 Noise Floor.....	23
4.9 Typical Audio Characteristics (PSE).....	24
4.9.1 Power vs. THD+N	24
4.9.2 Frequency vs. THD+N	25
4.9.3 Frequency Response	25
4.9.4 Noise Floor.....	26
5 Thermal Information	27
5.1 Peak Power Duration Thermal Information.....	27
5.2 Heatsink Information	31
6 Functional Block Diagram	32
7 Typical Implementation.....	33
8 Input / Output Pin Equivalent Circuit Diagrams	36
9 PWM Modulator Design	37
9.1 Input Section	37
9.2 Control Loop Design.....	38
9.3 PWM Frequency	38
9.4 Clock Synchronization	39

Table of contents

9.5	Click Noise Elimination	40
9.6	Differential Input	41
10	Operational Mode.....	42
10.1	Self-oscillation Start-up Condition	42
11	Protections.....	43
11.1.1	Self-Reset Protection	44
11.1.2	Designing Ct.....	45
11.1.3	Shutdown Input	45
11.1.4	Latched Protection.....	46
11.1.5	Interfacing with System Controller	46
11.2	Over Current Protection (OCP)	47
11.3	Over Temperature Protection (OTP)	48
11.4	Under Voltage Protection (UVP)	48
12	Status Output	49
12.1	Fault Output	49
12.2	CLIP Output	50
13	Power Supply Design	51
13.1	Supplying VAA and VSS	51
13.2	Supplying VCC and VB	51
13.2.1	Choosing Bootstrap Capacitance.....	52
13.2.2	Choosing Bootstrap Diode.....	52
13.2.3	Charging V_{BS} Prior to Start.....	52
13.3	Power Supply Sequence	54
14	Package details.....	55
15	Board mounting, part marking, and ordering information	58

1 Qualification Information

Qualification Level (1)		Standard (2)
		Qualified for standard applications according to the relevant tests of J-STD-020 and JESD22
Moisture Sensitivity Level (MSL) (3)		MSL3 (per IPC/JEDEC J-STD-020)
ESD	Charge Device Model	Class C2a (per JEDEC standard JS-002)
	Human Body Model	Class 1B (per JEDEC standard JS-001)
IC Latch-Up Test		Class I, Level A (per JESD78)
RoHS Compliant		Yes

Note:

1. Qualification standards can be found at Infineon's web site <http://www.infineon.com>
2. Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.
3. Higher MSL ratings may be available for the specific package types listed here. Please contact your Infineon sales representative for further information.

2 Device Comparison Table

Table 1

Device Name	Description
MA5302MS	200W (2 Ω)*2 channel integrated analog input Class D audio Amplifier
MA5342MS	200W (8 Ω)*2 channel integrated analog input Class D audio Amplifier
MA5332MS	200W (4 Ω)*2 channel integrated analog input Class D audio Amplifier
IR4302M	130W (4 Ω)*2 channel integrated analog input Class D audio Amplifier
IR4322M	100W (2 Ω)*2 channel integrated analog input Class D audio Amplifier
IR4321M	135W (2 Ω) single-channel integrated analog input Class D audio Amplifier
IR4301M	160W (4 Ω) single-channel integrated analog input Class D audio Amplifier

3 Pin Configuration

3.1 Lead assignments

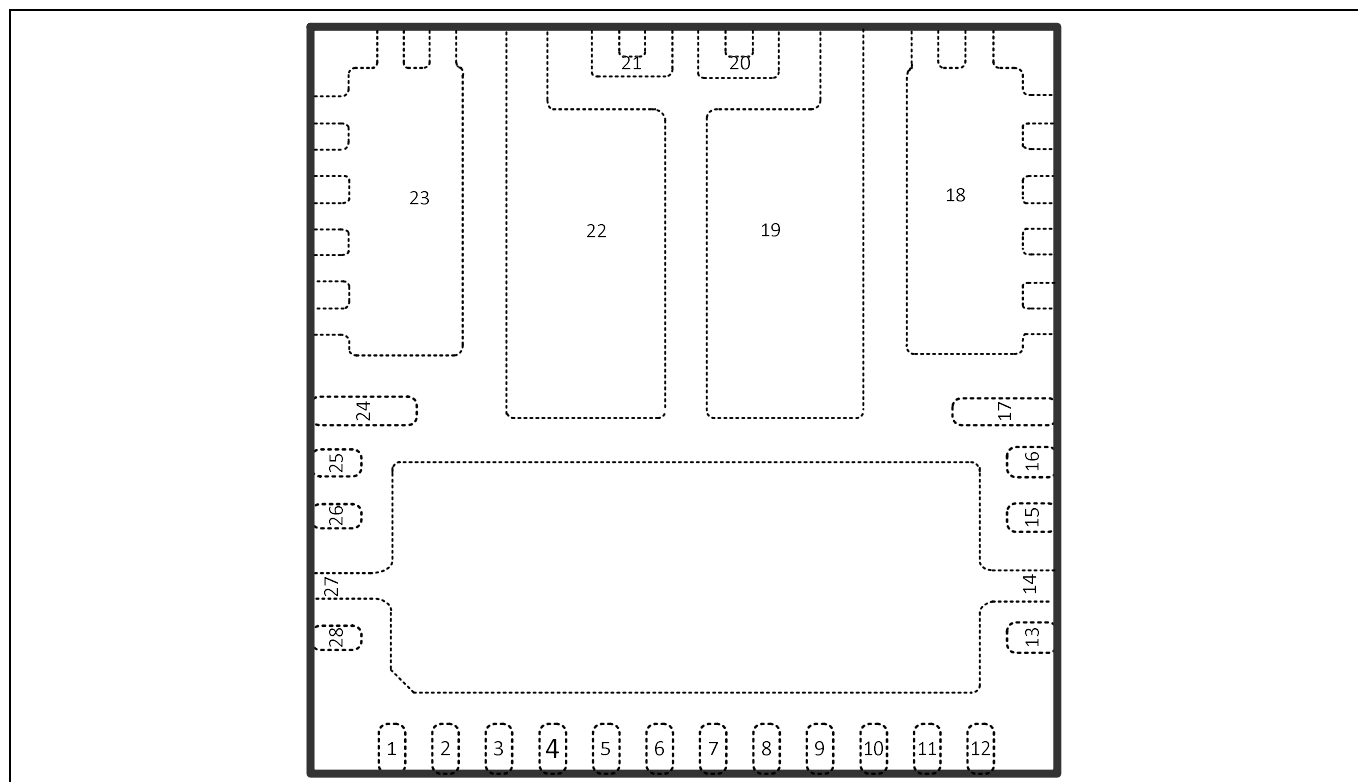


Figure 1 Lead assignment

3.2 Lead Definitions

Pin #	Symbol	Description
1	CLIP	Clipping detection output, open drain, referenced to GND
2	COMP2	CH2 PWM comparator input
3	IN-2	CH2 Analog inverting input
4	IN+2	CH2 Analog non-inverting input
5	GND	GND for internal shunt zener diodes to VAA and VSS, a reference to FAULT and CLIP outputs.
6	VSS	Floating input negative supply
7	VAA	Floating input positive supply
8	IN+1	CH1 Analog non-inverting input
9	IN-1	CH1 Analog inverting input
10	COMP1	CH1 PWM comparator input
11	CSD	Shutdown timing capacitor / shutdown input
12	FAULT	Fault reporting output, open drain, referenced to GND
13	VCC	Low side supply
14	COM	Low side supply return, internally connected to pin 27
15	CSH1	CH1 High side over current sensing input, referenced to VS1
16	VB1	CH1 High side floating supply
17	VS1	CH1 PWM output, internally connected to pin 19
18	VP1	CH1 Positive power supply
19	VS1	CH1 PWM output
20	VN1	CH1 Negative power supply, connect to COM externally
21	VN2	CH2 Negative power supply, connect to COM externally
22	VS2	CH2 PWM output, internally connected to pin 24
23	VP2	CH2 Positive power supply
24	VS2	CH2 PWM output
25	VB2	CH2 High side floating supply
26	CSH2	CH2 High side over current sensing input, referenced to VS2
27	COM	Low side supply return, internally connected to pin 14
28	NC	

4 Specifications

4.1 Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM=VN1=VN2; all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min	Max	Units
V_{Pn}	Positive power supply rail voltage, n=1-2	-	100	
V_{Bn}	High side floating supply voltage	-0.3	115	
V_{Sn}	High side floating supply voltage ⁽²⁾ , n=1-2	$V_{Bn} - 15$	$V_{Bn} + 0.3$	
V_{CSHn}	CSH pin input voltage, n=1-2	$V_{Sn} - 0.3$	$V_{Bn} + 0.3$	
V_{CC}	Low side supply voltage ⁽²⁾	-0.3	15	
V_{AA}	Floating input positive supply voltage ⁽²⁾	-0.3	110	
V_{SS}	Floating input negative supply voltage ⁽²⁾	-1 (See I_{SSZ})	GND + 0.3	
V_{IN+n}	Floating input supply ground voltage, n=1-2	$V_{SS} - 0.3$	$V_{AA} + 0.3$	
I_{INn}	Input current between IN- and IN+ pins ⁽¹⁾ , n=1-2	-	±3	mA
V_{CSD}	CSD pin input voltage	$V_{SS} - 0.3$	$V_{AA} + 0.3$	
V_{COMPn}	COMP pin input voltage, n=1-2	$V_{SS} - 0.3$	$V_{AA} + 0.3$	V
V_{CLIP}	CLIP pin input voltage	GND - 0.3	$V_{AA} + 0.3$	
I_{CLIP}	CLIP pin sinking current	-	5	mA
V_{FAULT}	FAULT pin input voltage	GND - 0.3	$V_{AA} + 0.3$	V
I_{FAULT}	FAULT pin sinking current	-	5	
I_{AAZ}	Floating input supply zener clamp current ⁽²⁾	-	20	
I_{SSZ}	Floating input negative supply zener clamp current ⁽²⁾	-	20	mA
I_{CCZ}	Low side supply zener clamp current ⁽²⁾	-	20	
I_{BSZn}	Floating supply zener clamp current ⁽²⁾ , n=1-2	-	20	
dV_{Sn}/dt	Allowable V_S voltage slew rate, n=1-2	-	50	V/ns
dV_{SS}/dt	Allowable V_{SS} voltage slew rate ⁽³⁾	-	50	V/ms
$I_{D@25^{\circ}C}$	Continuous output current, from VPn to VS _n , VS _n to VN _n , $V_{CC}=10V$, $V_{Bn}-V_{Sn}=10V$	-	16	
$I_{D@100^{\circ}C}$	Continuous output current, from VPn to VS _n , VS _n to VN _n , $V_{CC}=10V$, $V_{Bn}-V_{Sn}=10V$	-	10	A
I_{DM}	Pulsed output current, from VPn to VS _n , VS _n to VN _n , $V_{CC}=10V$, $V_{Bn}-V_{Sn}=10V$ ⁽⁵⁾	-	64	
P_d	Power dissipation ⁽⁴⁾ @ $T_c = 25^{\circ}C$	-	25	W
R_{thJC}	Thermal resistance, junction to case ⁽⁴⁾	-	5	$^{\circ}C/W$
T_{JIC}	Control IC junction temperature	-	150	
T_{JFET}	FET junction temperature	-	150	$^{\circ}C$

T_S	Storage Temperature	-55	150
T_L	Lead temperature (Soldering, 10 seconds)	-	300

Note:

1. $IN-$ and $IN+$ contain clamping diodes between the two pins.
2. $V_{AA}-V_{SS}$, $V_{CC}-COM$ and $V_{Bn}-V_{Sn}$ contain internal shunt zener diodes. Note that the voltage ratings of these can be limited by the clamping current.
3. For the rising and falling edges of step signal of 10V. $V_{SS}=15V$ to $100V$.
4. Per MOSFET.
5. Repetitive rating, pulse width limited by maximum junction temperature.

4.2 Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions below. The V_{SS} and V_{Sn} offset ratings are tested with supplies biased at $COM=VN1=VN2$, $V_{AA}-V_{SS}=9.6V$, $V_{CC}=12V$ and $V_{Bn}-V_{Sn}=12V$. All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead.

Symbol	Definition		Min	Max	Units
V_{Pn}	Positive power supply voltage, n=1-2, without heatsink	MA5332MS	-	60	
	Positive power supply voltage, n=1-2, with heatsink	MA5332MS	-	80	
V_{Bn}	High side floating supply absolute voltage, n=1-2		$V_{Sn} + 10$	$V_{Sn} + 14$	V
V_{Sn}	High side floating supply offset voltage, n=1-2	MA5332MS	⁽⁶⁾	100	
V_{AA}	Floating input positive supply voltage ⁽⁷⁾		$V_{SS} + 9.0$	$V_{SS} + 9.8$	
V_{SS}	Floating input negative supply voltage ⁽⁷⁾	MA5332MS	0	100	
I_{AAZ}	Floating input supply zener clamp current ⁽⁷⁾		1	15	mA
I_{SSZ}	Floating input negative supply zener clamp current ⁽⁷⁾		1	15	
V_{CC}	Low side fixed supply voltage		10	15	V
V_{IC}	$IN-$ and $IN+$ pins common mode input voltage		$V_{SS} + 2$	$V_{AA} - 2$	
V_{IN-n}	Inverting input voltage, n=1-2		$V_{IN+} - 0.5$	$V_{IN+} + 0.5$	
V_{CSD}	CSD pin input voltage		V_{SS}	V_{AA}	
V_{COMPn}	COMP pin input voltage, n=1-2		V_{SS}	V_{AA}	nF
C_{COMPn}	COMP pin phase compensation capacitor to GND, n=1-2		1	-	
V_{CSHn}	CSH pin input voltage, n=1-2		V_{Sn}	V_{Bn}	V
f_{SW}	Switching frequency		-	500	kHz
T_{J_IC}	Junction temperature of controller IC		-40	100	°C

Note:

6. Logic operational for V_s equal to $-5V$ to $+100V$. Logic state held for V_s equal to $-5V$ to $-V_{BS}$.
7. GND input voltage is limited by I_{AAZ} and I_{SSZ} .

Specifications

4.3 Electrical Characteristics

Unless otherwise specified, the following apply:

- $V_{CC}, V_{BS} = 12\text{ V}$
- $V_{SS} = V_{S1} = V_{S2} = V_{N1} = V_{N2} = \text{COM} = 0\text{ V}$
- $V_{AA} = 9.6\text{ V}$
- $T_A = 25^\circ\text{C}$

Table 2 Electrical characteristics

Symbol	Definition	Min	Typ	Max	Units	Test conditions
Low-side supply						
UV_{CC+}	V _{CC} supply UVLO positive threshold	8.4	8.9	9.4	V	
UV_{CC-}	V _{CC} supply UVLO negative threshold	8.2	8.7	9.2	V	
UV_{CCHYS}	UV _{CC} hysteresis	-	0.2	-	V	
I_{QCC}	Low side quiescent current	-	-	3	mA	
I_{CC}	Low side supply current	-	10	-	mA	f=400kHz
$V_{CLAMPLN}$	Low side zener diode clamp voltage, n=1-2	14.7	15.3	16.2	V	I _{CC} =5mA
High-side floating supply						
UV_{BS+n}	High side well UVLO positive threshold, n=1-2	8.0	8.5	9.0	V	
UV_{BS-n}	High side well UVLO negative threshold, n=1-2	7.8	8.3	8.8	V	
UV_{BSHYSn}	UV _{BS} hysteresis, n=1-2	-	0.2	-	V	
I_{QBSn}	High side quiescent current, n=1-2	-	-	2.4	mA	
$I_{QBSn_OFF-CSH}$	High side quiescent current, with CSH pin open n=1-2	350	500	650	uA	
$V_{CLAMPHn}$	High side zener diode clamp voltage, n=1-2	14.7	15.3	16.2	V	I _{BS} =5mA
Floating input supply						
UV_{AA+}	VA+, VA- floating supply UVLO positive threshold from V _{SS}	8.2	8.7	9.2	V	V _{SS} =0V, GND pin floating
UV_{AA-}	VA+, VA- floating supply UVLO negative threshold from V _{SS}	7.7	8.2	8.7	V	V _{SS} =0V, GND pin floating
UV_{AAHYS}	UV _{AA} hysteresis	-	0.5	-	V	V _{SS} =0V, GND pin floating
I_{QAA0}	Floating Input positive quiescent supply current	-	1.5	3	mA	V _{AA} =9.6V, V _{SS} =0V, V _{CSD} =V _{SS}
I_{QAA1}	Floating Input positive quiescent supply current	-	4	6	mA	V _{AA} =9.6V, V _{SS} =0V, V _{CSD} =V _{AA}

Specifications

I_{QAA2}	Floating Input positive quiescent supply current	-	5	7.5	mA	$V_{AA}=9.6V$, $V_{SS}=0V$, $V_{CSD}=GND$
I_{LKM}	Floating input side to Low side leakage current	-	-	50	μA	$V_{AA}=V_{SS}=V_{GND}=100V$
V_{CLAMP+}	V_{AA} floating supply zener diode clamp voltage, positive, with respect to GND	4.9	5.1	5.4	V	$I_{AA}=5mA$, $I_{SS}=5mA$, $V_{GND}=0V$, $V_{CSD}=V_{SS}$
V_{CLAMP-}	V_{SS} floating supply zener diode clamp voltage, negative, with respect to GND	-5.4	-5.1	-4.9	V	$I_{AA}=5mA$, $I_{SS}=5mA$, $V_{GND}=0V$, $V_{CSD}=V_{SS}$

Audio input ($V_{GND}=0$, $V_{AA}=4.8V$, $V_{SS}=-4.8V$)

V_{OSn}	Input offset voltage, n=1-2	-18	0	18	mV	
I_{BINn}	Input bias current, n=1-2	-	-	40	nA	
GBWn	Small signal bandwidth in OTA, n=1-2	-	9	-	MHz	$C_{COMP}=2nF$, $R_f=0$
g_{mn}	OTA transconductance, n=1-2	-	10	-	mS	$V_{IN+}=0V$, $V_{IN-}=10mV$
G_{Vn}	OTA gain, n=1-2	50	-	-	dB	
V_{Nrmsn}	CHn OTA input noise voltage, n=1-2	-	200	330	mVrms	

PWM

$V_{th_{PWM}}$	PWM comparator threshold in COMP	-	$(V_{AA} - V_{SS})/2$	-	V	
f_{OTAn}	COMP pin start-up local oscillation frequency, n=1-2	0.7	1.0	1.5	MHz	$V_{CSD}=GND$
T_{on_n}	COMP to VS rising edge propagation delay, n=1-2	-	370	-	ns	
T_{off_n}	COMP to VS trailing edge propagation delay, n=1-2	-	320	-	ns	
DTn	Deadtime: Low-side turn-off to High-side turn-on (DT_{LO-HO}) & High-side turn-off to Low-side turn-on (DT_{HO-LO}), n=1-2	-	50	-	ns	$V_P=30V$, $V_N=-30V$,

Power MOSFET (FET1, FET2, FET3, FET4)

At $T_j=25^\circ C$, unless otherwise specified

$V_{(BR)DSS}^{(8)}$	Drain-to-Source breakdown voltage	100	-	-	V	$V_{GS}=0V$, $I_D=1mA$
$R_{DS(ON)}$	FET on resistance	-	24.4	30.5	m Ω	$I_D=3.3A$, $V_{GS}=10V$
Qg	Total gate charge	-	12.7	19	nC	$V_{GS}=10V$
I_{LK0}	VP leakage current, $V_S=V_N$	-	-	20	μA	$V_P=100V^{(8)}$, $V_{CSD}=V_{SS}$

Protection

Specifications

I_{OCPn}	Over current detection Positive threshold, n=1-2 ⁽⁸⁾	-	40	-	A	
I_{OCNn}	Over current detection Negative threshold, n=1-2 ⁽⁹⁾	-	-40	-	A	
V_{th1}	CSD pin shutdown release threshold	$0.62 \times V_{AA}$	$0.70 \times V_{AA}$	$0.78 \times V_{AA}$	V	
V_{th2}	CSD pin self-reset threshold	$0.26 \times V_{AA}$	$0.30 \times V_{AA}$	$0.34 \times V_{AA}$	V	
I_{CSD+}	CSD pin discharge current	70	100	130	μA	$V_{CSD} = V_{SS} + 4.8V$
I_{CSD-}	CSD pin charge current	70	100	130	μA	$V_{CSD} = V_{SS} + 4.8V$
t_{SDn}	Shutdown propagation delay from $V_S < V_{th1}$ to Shutdown, n=1-2	-	-	250	ns	COMP = V_{SS}
t_{OCPn}	CHn propagation delay time from $I_{On} > I_{OCPn}$ to Shutdown, n=1-2	-	-	500	ns	COMP = V_{SS}
t_{OCNn}	CHn propagation delay time from $I_{On} < I_{OCNn}$ to Shutdown, n=1-2	-	-	500	ns	COMP = V_{SS}
$V_{th+CLIP}$	Clip detection positive threshold in COMP	$0.85 \times V_{AA}$	$0.90 \times V_{AA}$	$0.95 \times V_{AA}$	V	
$V_{th-CLIP}$	Clip detection negative threshold in COMP	$0.05 \times V_{AA}$	$0.10 \times V_{AA}$	$0.15 \times V_{AA}$	V	
t_{CLIP}	Clipping detection propagation delay	-	40	-	ns	
$t_{CLIPmin}$	Clipping detection minimum output duration	-	3	-	μs	
T_{SD}	Over-temperature shutdown threshold in controller IC	100	-	-	°C	
T_{SDHYS}	Over-temperature shutdown threshold hysteresis	-	7	-	°C	

Specifications

4.4 Audio Characteristics (SE)

Table 3

Parameter	Test conditions	Typ	Unit
Po Power output per channel ⁽¹⁰⁾	RL= 6Ω, 10%THD+N, V _{bus} = ± 40 V	160	W
	RL= 4Ω, 10%THD+N, V _{bus} = ± 36.5 V	200	
	RL= 3Ω, 10%THD+N, V _{bus} = ± 31.5 V	190	
	RL= 2Ω, 10%THD+N, V _{bus} = ± 23 V	150	
	RL= 6Ω, 1%THD+N, V _{bus} = ± 40 V	120	
	RL= 4Ω, 1%THD+N, V _{bus} = ± 36.5 V	150	
	RL= 3Ω, 1%THD+N, V _{bus} = ± 31.5 V	140	
	RL= 2Ω, 1%THD+N, V _{bus} = ± 23V	110	
Residual noise(AES-17, IHF-A, typical)	EVAL_AUDAMP25, V _{bus} = ± 36.5 V, RL= 4Ω	250	uV
Idling supply current	EVAL_AUDAMP25, V _{bus} = ± 36.5 V, RL= 4Ω	+55	mA
		-80	
Efficiency ⁽¹¹⁾	EVAL_AUDAMP25, V _{bus} = ± 36.5 V, Pout=200W, RL= 4Ω	95	%

Note:

8. V_p changes over temperature at a rate of 50mV/K compared to T_j=25°C.9. Over-current protection threshold measured under T_j=25°C condition.

10. Tested with heatsink (digikey part number: V8818V)

11. Class D stage only

4.5 Audio characteristics (BTL)

Table 4

Parameter	Test conditions	Typ	Unit
Po Power output per channel ⁽⁹⁾	RL= 8Ω, 10%THD+N, V _{bus} = ± 36.5 V	400	W
	RL= 6Ω, 10%THD+N, V _{bus} = ± 31.5 V	380	
	RL= 4Ω, 10%THD+N, V _{bus} = ± 23 V	300	
	RL= 8Ω, 1%THD+N, V _{bus} = ± 36.5 V	300	
	RL= 6Ω, 1%THD+N, V _{bus} = ± 31.5 V	280	
	RL= 4Ω, 1%THD+N, V _{bus} = ± 23V	220	
Residual noise(AES-17, IHF-A, typical)	EVAL_AUDAMP25, V _{bus} = ± 36.5 V, RL= 4Ω	350	uV
Idling supply current	EVAL_AUDAMP25, V _{bus} = ± 36.5 V, RL= 8Ω	+55	mA
		-80	
Efficiency ⁽¹⁰⁾	EVAL_AUDAMP25, V _{bus} = ± 36.5 V, RL= 8Ω	95	%

Specifications

4.6 Audio Characteristics (PSE)

Table 5

Parameter	Test conditions	Typ	Unit
Po Power output per channel ⁽⁹⁾	RL= 2Ω, 10%THD+N, V _{bus} = ± 36.5 V	400	W
	RL= 2Ω, 1%THD+N, V _{bus} = ± 36.5V	300	
Residual noise(AES-17, IHF-A, typical)	EVAL_AUDAMP25 , V _{bus} = ± 36.5 V ,RL= 4Ω	250	uV
Idling supply current	EVAL_AUDAMP25 , V _{bus} = ± 36.5 V ,RL= 4Ω	+55	mA
		-80	
Efficiency ⁽¹⁰⁾	EVAL_AUDAMP25 , V _{bus} = ± 36.5 V ,RL= 4Ω	95	%

Specifications

4.7 Typical Audio Characteristics (SE)

Test conditions:

All Measurements taken at Sine wave frequency= 1 kHz, AES17+ AUX-0025 measurement filters.

$V_{bus} = \pm 40\text{ V}$, Load impedance = $6\ \Omega$, $F_{PWM} = 400\text{ kHz}$

$V_{bus} = \pm 36.5\text{ V}$, Load impedance = $4\ \Omega$, $F_{PWM} = 400\text{ kHz}$

$V_{bus} = \pm 31.5\text{ V}$, Load impedance = $3\ \Omega$, $F_{PWM} = 400\text{ kHz}$

$V_{bus} = \pm 23\text{ V}$, Load impedance = $2\ \Omega$, $F_{PWM} = 400\text{ kHz}$

4.7.1 Power vs. THD+N

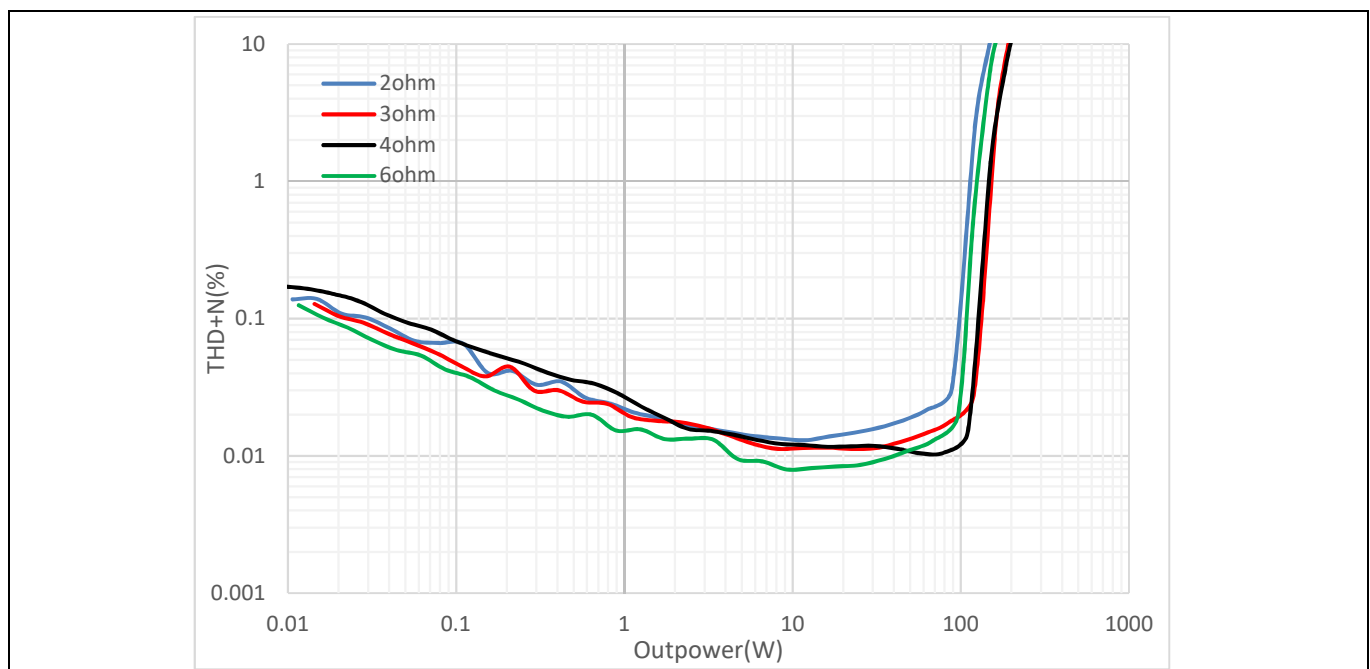
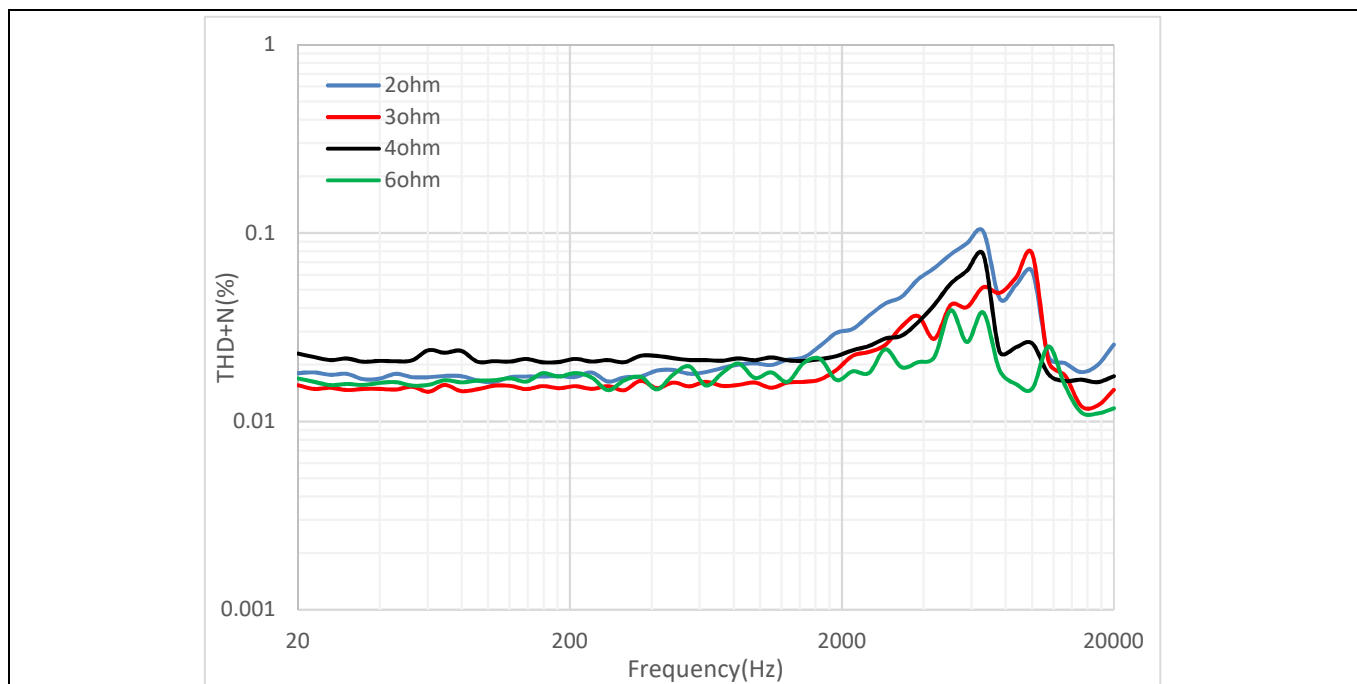


Figure 2 Power vs. THD+N

Specifications

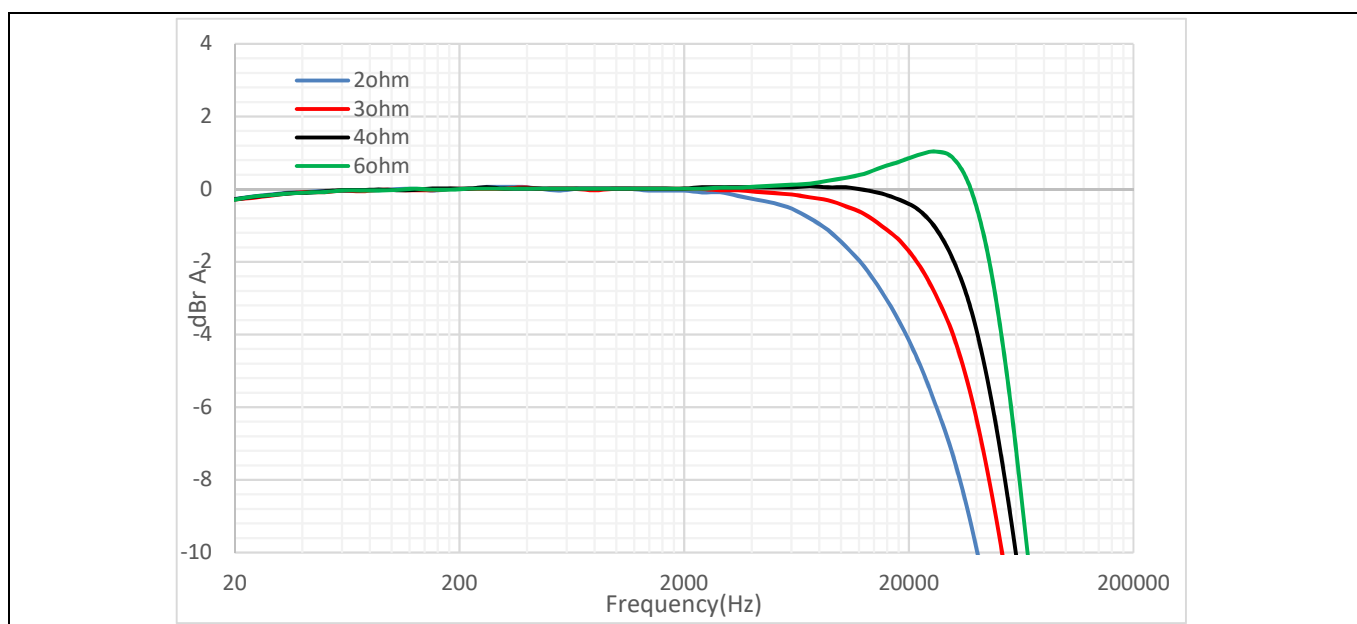
4.7.2 Frequency vs. THD+N

**Figure 3** Frequency vs. THD+N @1W

4.7.3 Frequency Response

Test conditions:

Output power = 1 W, LPF = 22uH+0.47uF

**Figure 4** Frequency response

4.7.4 Noise Floor

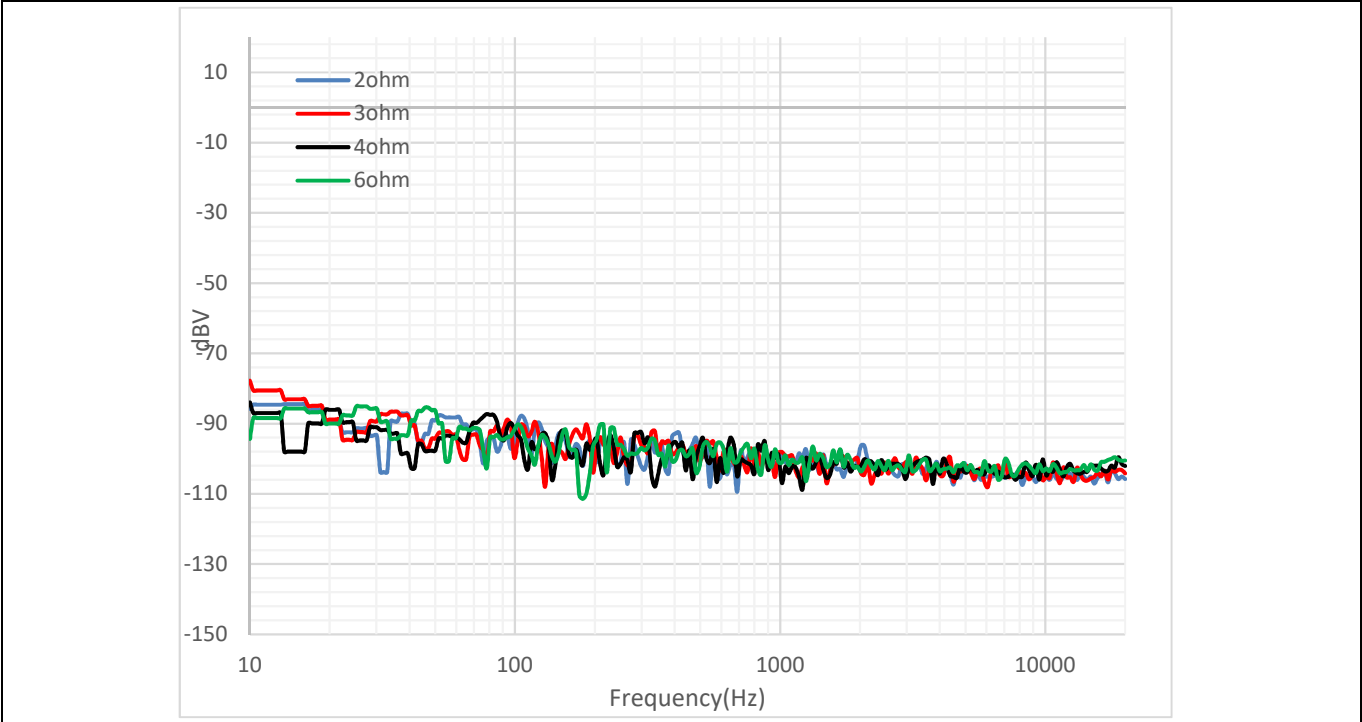


Figure 5 Noise floor

4.7.5 Efficiency

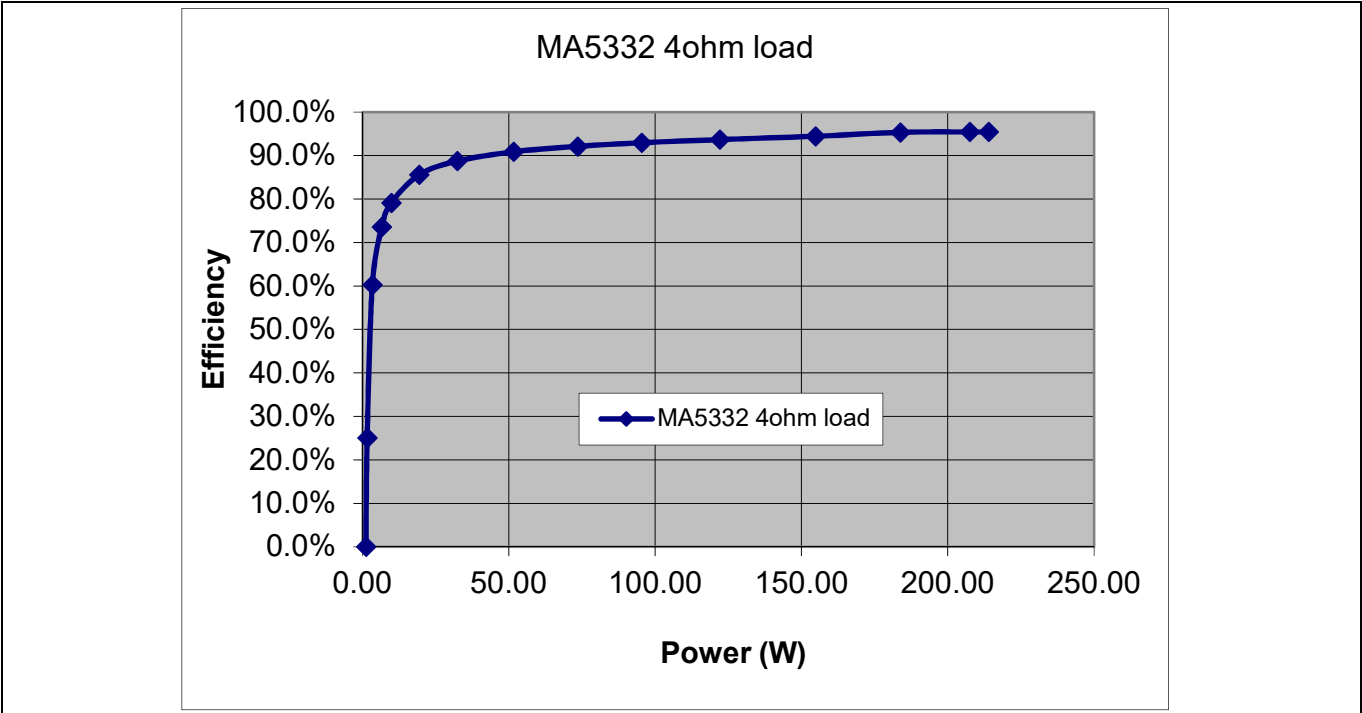


Figure 6 Efficiency 4 Ω load

Specifications

4.8 Typical Audio Characteristics (BTL)

Test conditions:

All Measurements taken at Sine wave frequency= 1 kHz, AES17+ AUX-0025 measurement filters.

$V_{bus} = \pm 40\text{ V}$, Load impedance = $8\ \Omega$, $F_{PWM} = 400\text{ kHz}$

$V_{bus} = \pm 31.5\text{ V}$, Load impedance = $6\ \Omega$, $F_{PWM} = 400\text{ kHz}$

$V_{bus} = \pm 23\text{ V}$, Load impedance = $4\ \Omega$, $F_{PWM} = 400\text{ kHz}$

4.8.1 Power vs. THD+N

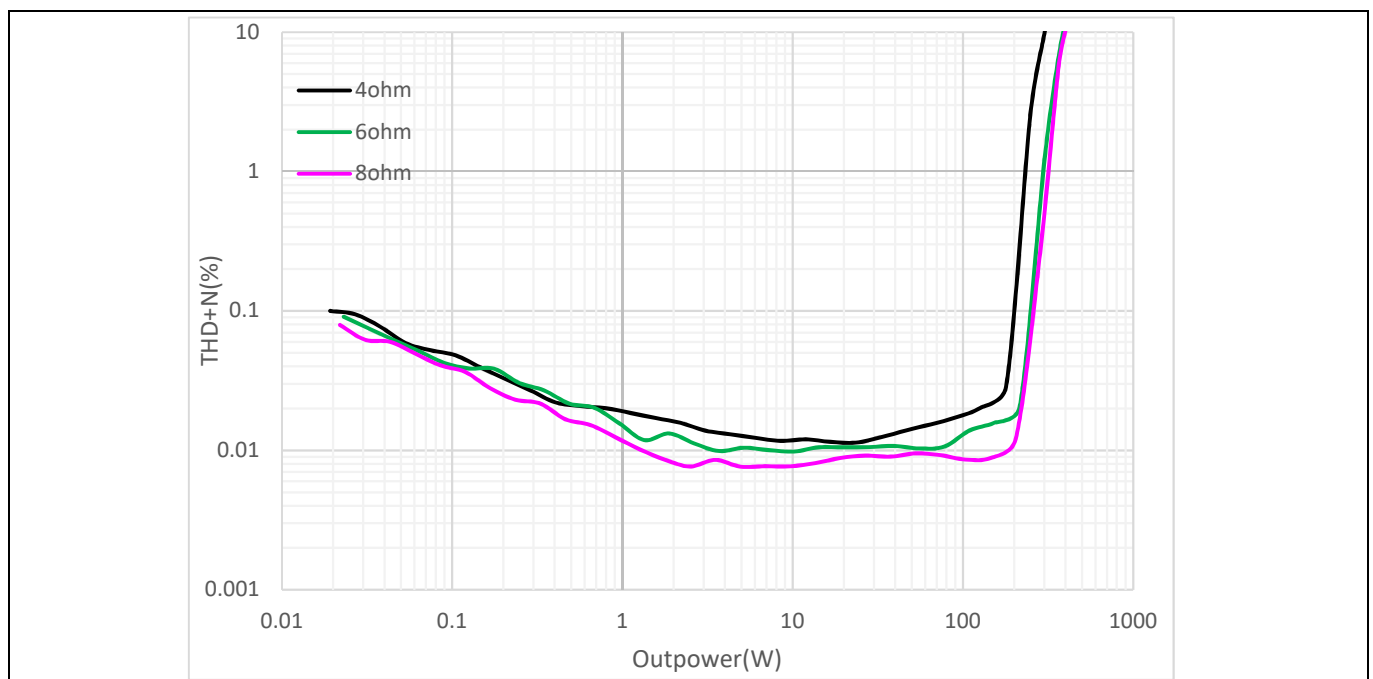


Figure 7 Power vs. THD+N

Specifications

4.8.2 Frequency vs. THD+N

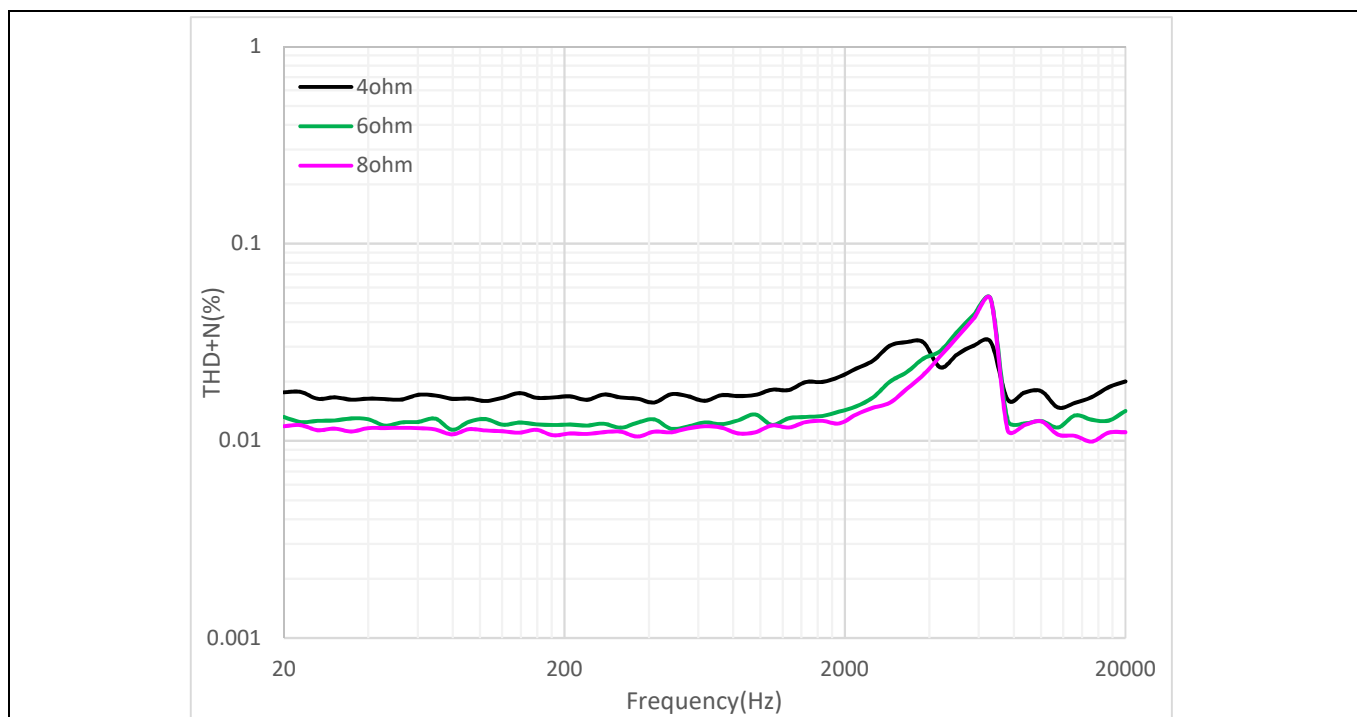


Figure 8 Frequency vs. THD+N @1W

4.8.3 Frequency Response

Test conditions:

Output power = 1 W, fixed LPF 22uH+0.47uF

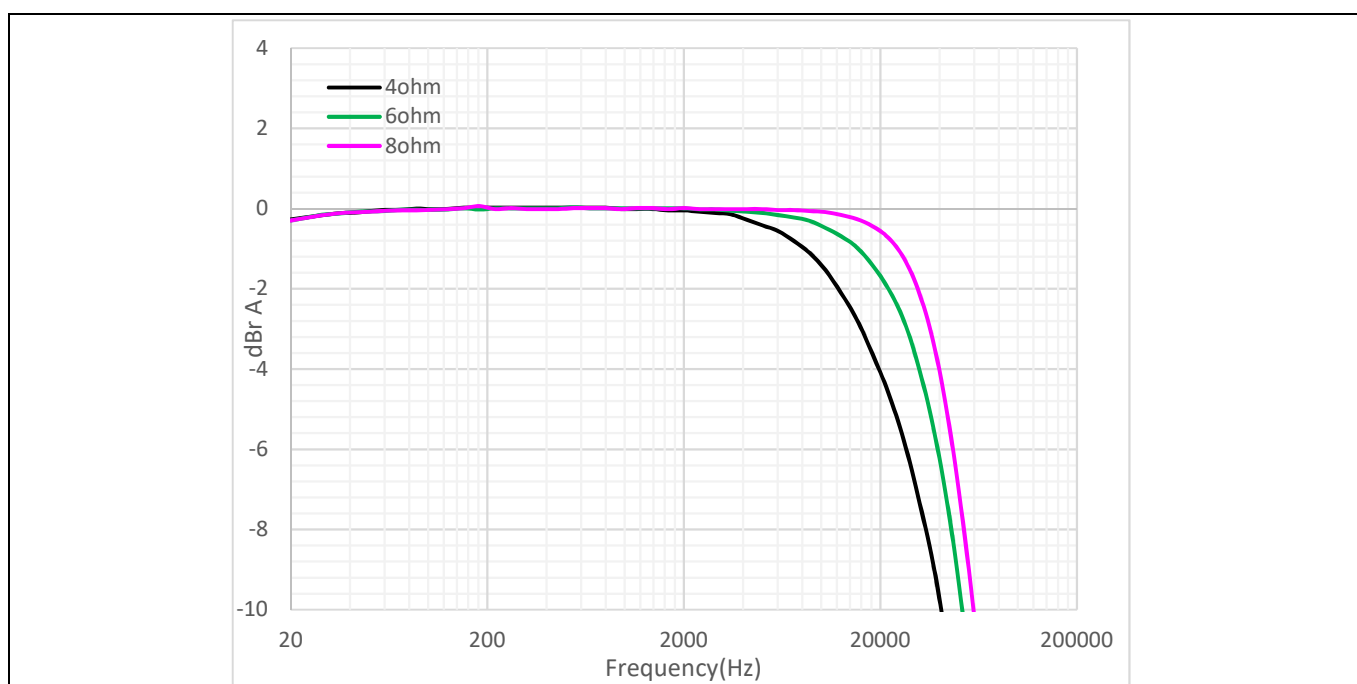


Figure 9 Frequency response

Specifications**4.8.4 Noise Floor**

Test conditions:

No input signal

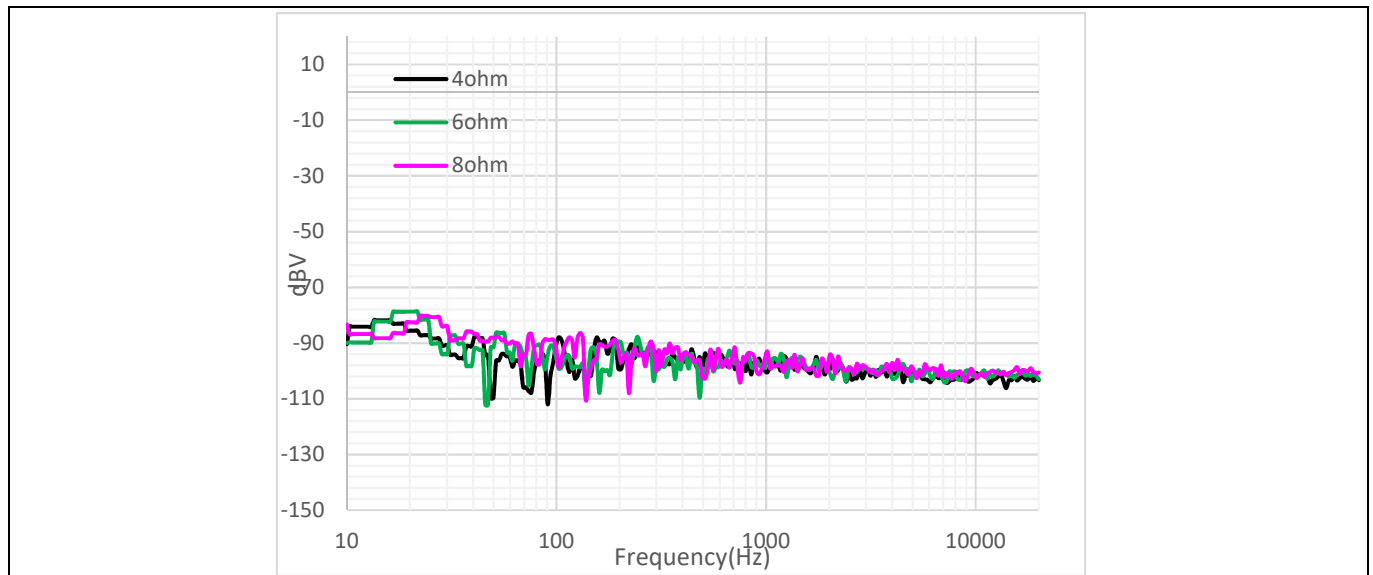


Figure 10 Noise floor

Specifications

4.9 Typical Audio Characteristics (PSE)

Test conditions:

All Measurements taken at Sine wave frequency= 1 kHz, AES17+ AUX-0025 measurement filters.

$V_{bus} = \pm 36.5\text{ V}$, Load impedance = $2\ \Omega$, $F_{PWM} = 400\text{ kHz}$

4.9.1 Power vs. THD+N

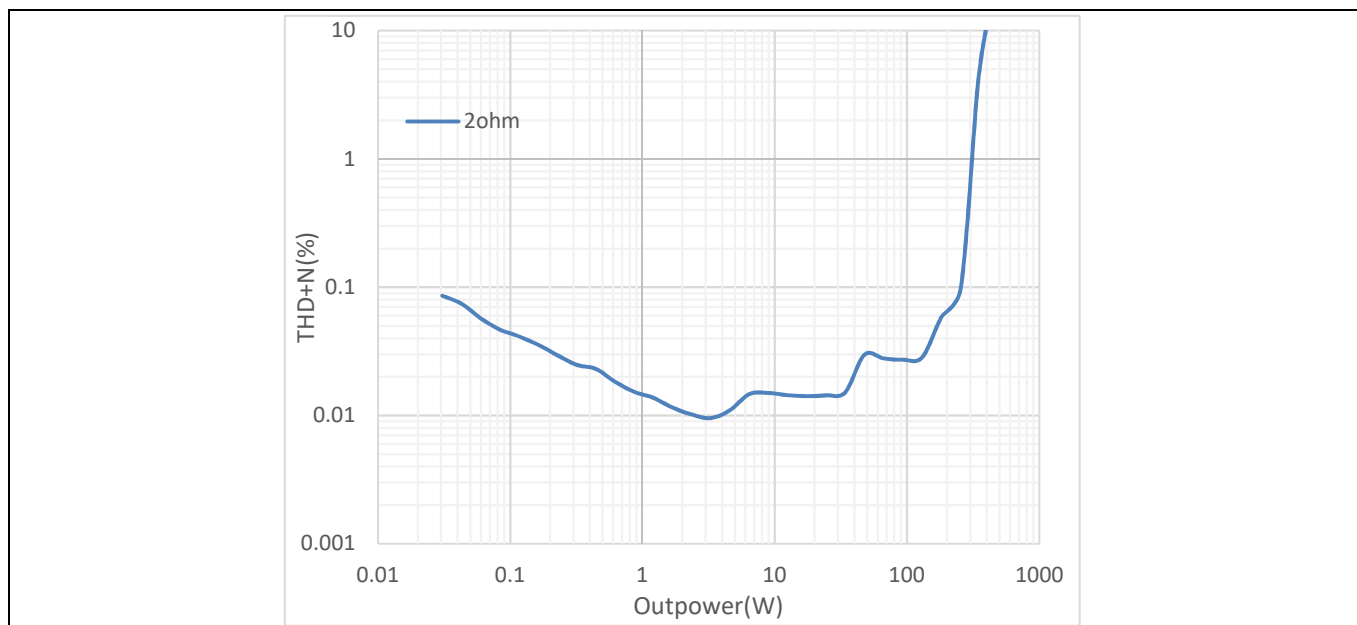


Figure 11 Power vs. THD+N

4.9.2 Frequency vs. THD+N

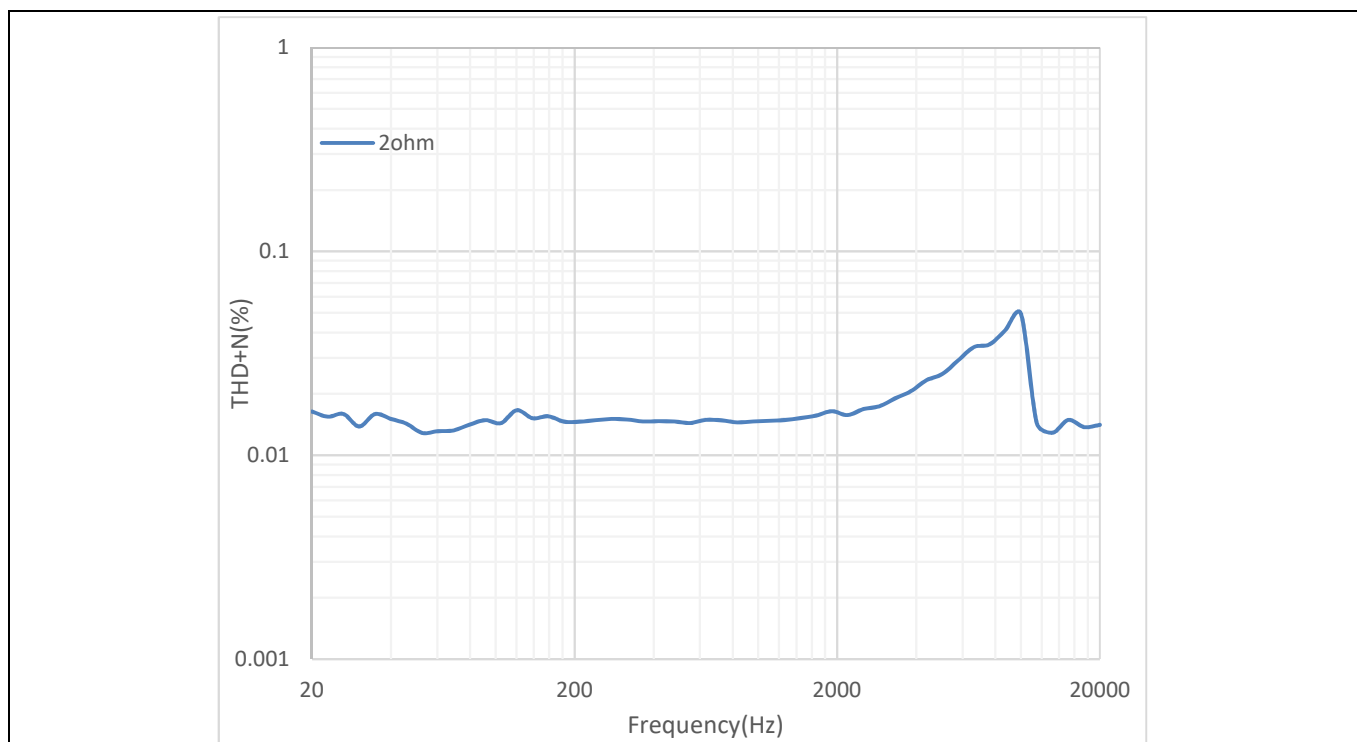


Figure 12 Frequency vs. THD+N @1W

4.9.3 Frequency Response

Test conditions:

Output power = 1 W, fixed LPF 22 μ H+0.47 μ F

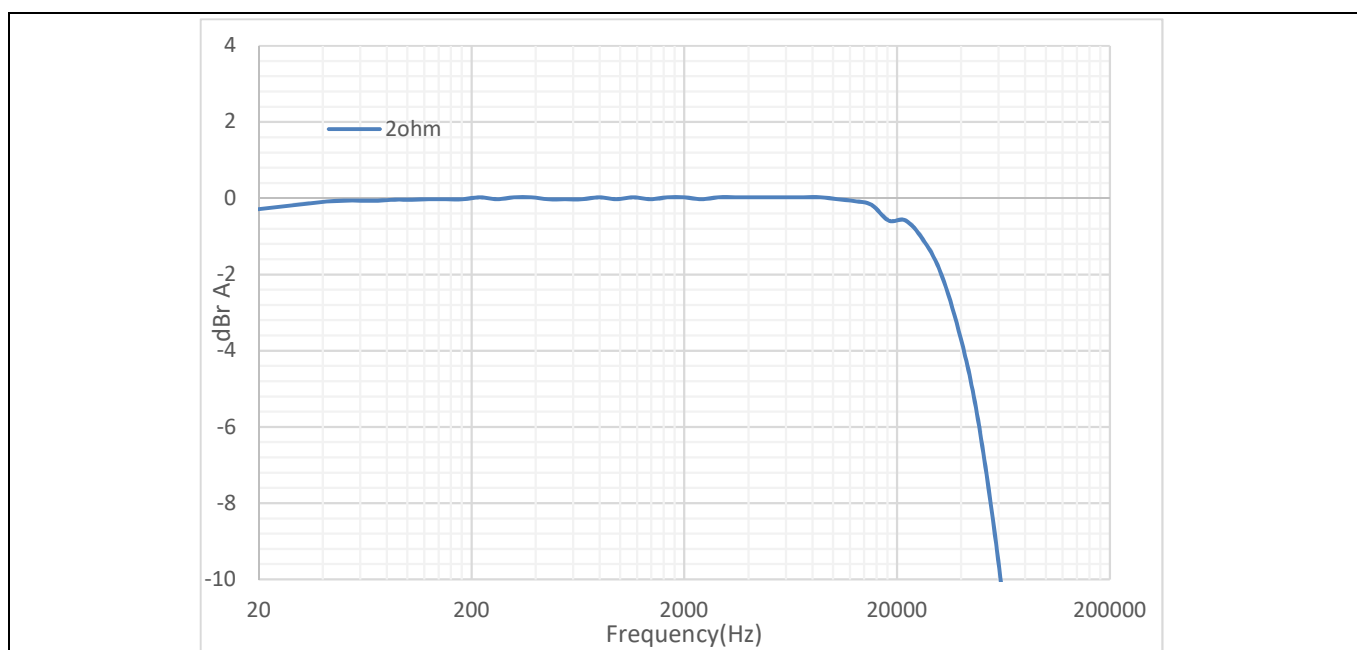


Figure 13 Frequency response

Specifications

4.9.4 Noise Floor

Test conditions:

No input signal

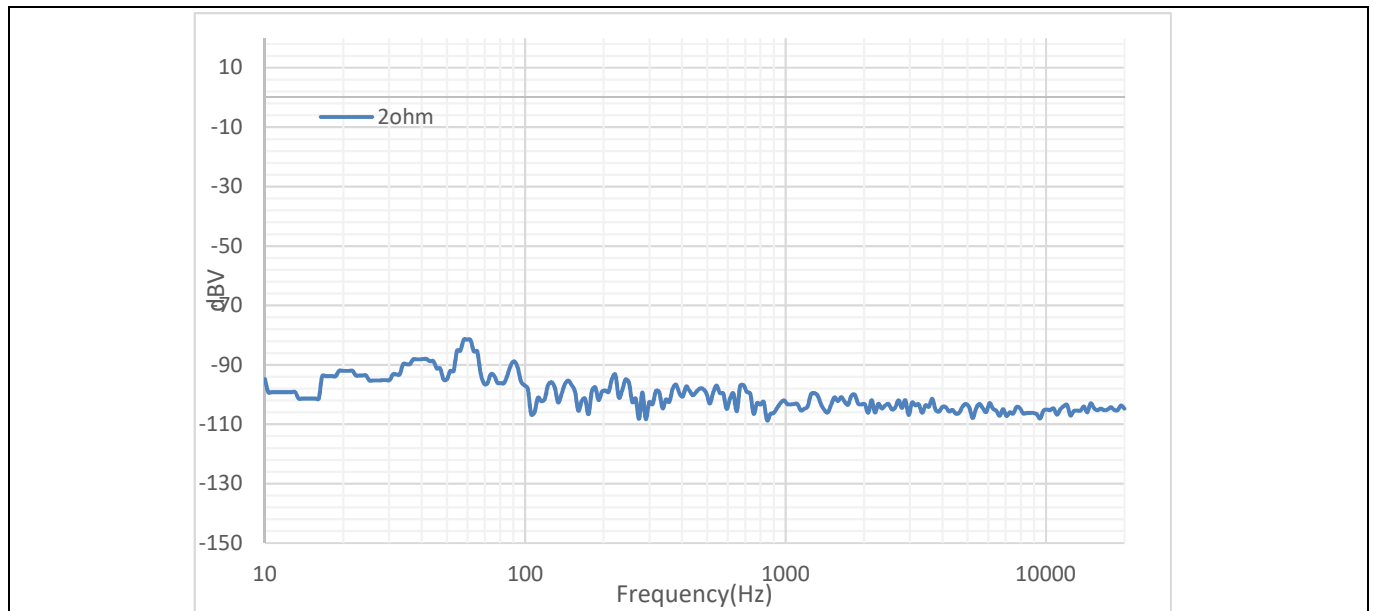


Figure 14 Noise floor

5 Thermal Information

MA5332MS benefits from a unique co-packaging technique and superior MOSFET technology, resulting in best-in-class thermal performance and peak power duration. It is capable of delivering 100W x 2 at 4Ω even without requiring a heatsink

5.1 Peak Power Duration Thermal Information

Test conditions:

All Measurements are taken at sinewave frequency= 1 kHz, AES17+ AUX-0025 measurement filters. Input signal = 1 kHz, $F_{PWM} = 400$ kHz.

Tests are based on Eval_AUDAMP25 board when both channels are driven.

Table 6 Peak power with heatsink

Load (Ω)	$\pm V_{bus}$ (V)	10 percent THD+N power (W)	Duration
6	40	160	More than 1 minute without thermal shutdown
4	36.5	200	
3	31.5	190	
2	23	150	

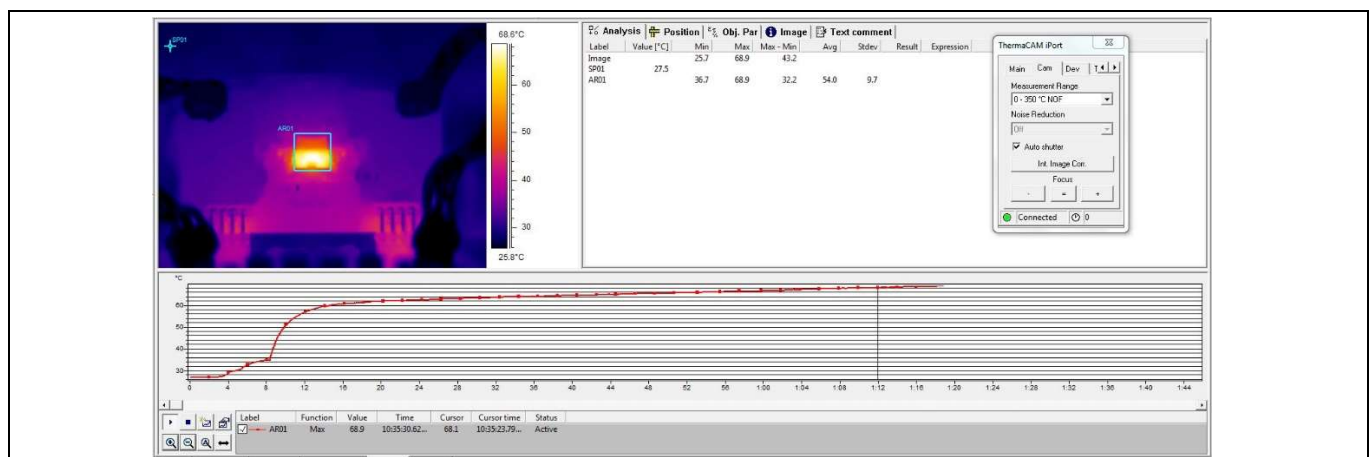


Figure 15 Peak power $P_{out} = 164$ W with 6 Ω load ± 40 V

Maximum temperature 68.9°C at 1 minute.

Note:

Thermal information

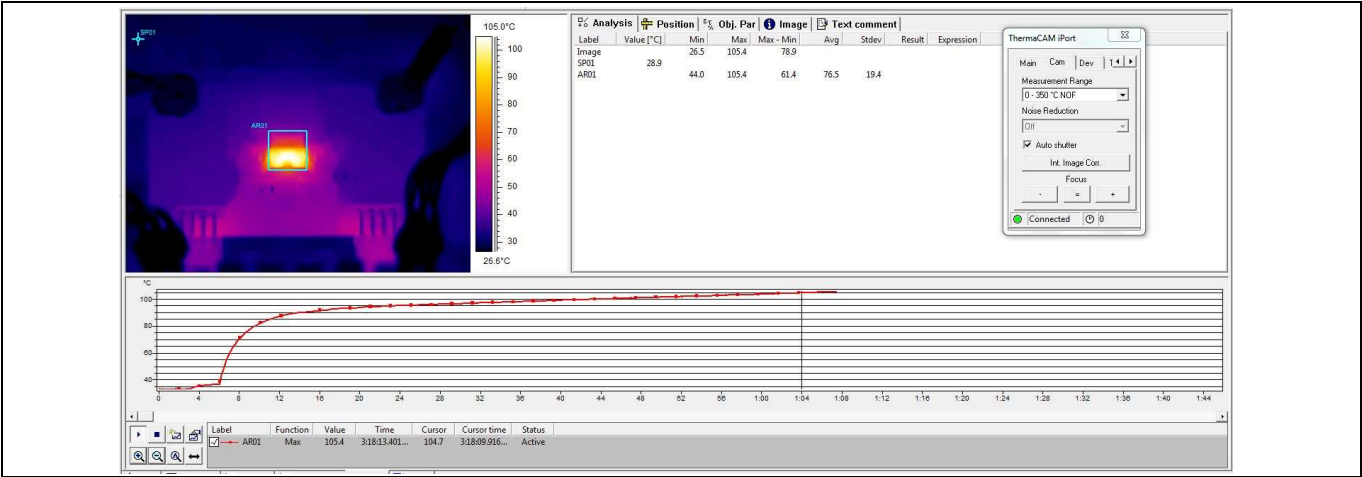


Figure 16 Peak power $P_{out} = 200\text{ W}$ with $4\ \Omega$ load $\pm 36.5\text{ V}$

Note: Maximum temperature 105°C at 1 minute.

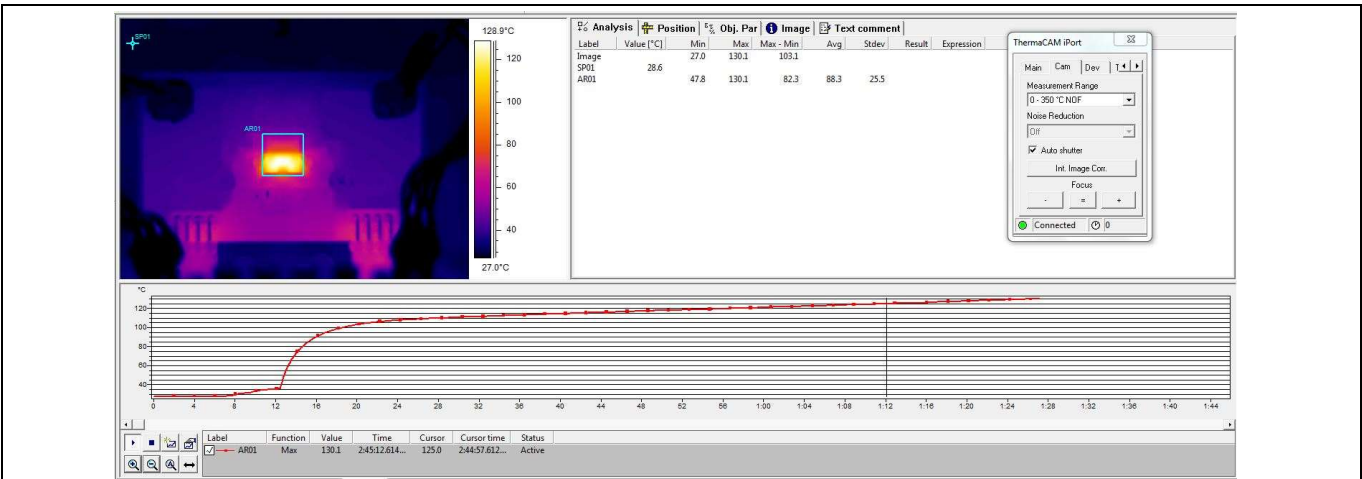


Figure 17 Peak power $P_{out} = 194\text{ W}$ with $3\ \Omega$ load $\pm 31.5\text{ V}$

Note: Maximum temperature 130°C at 1 minute.

Thermal information

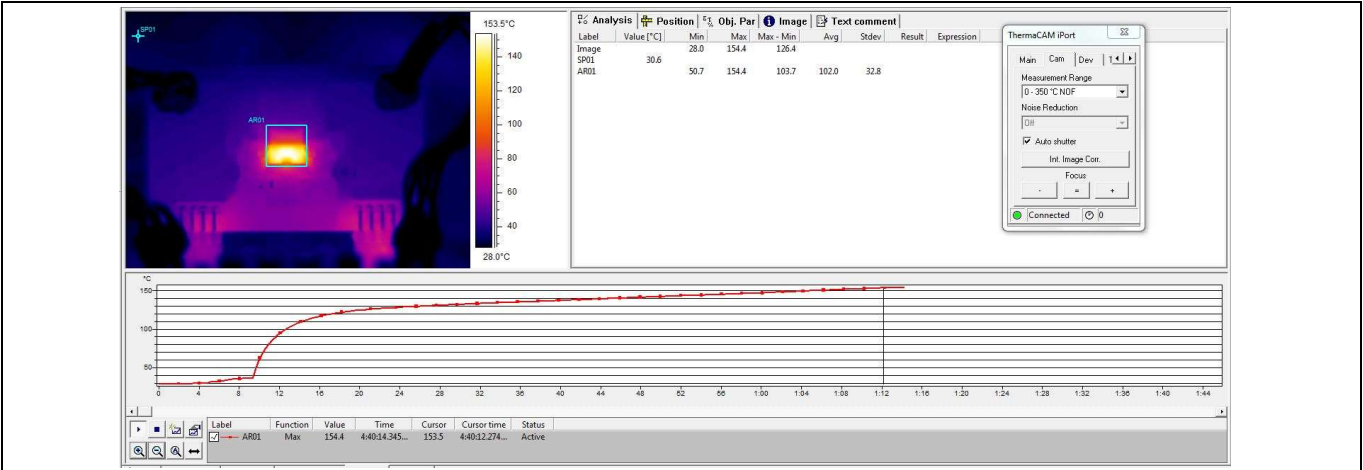


Figure 18 Peak power $P_{out} = 150\text{ W}$ with $2\ \Omega$ load $\pm 23\text{ V}$

Note: Maximum temperature 154°C at 1 minute.

Table 7 Peak power without heatsink

Load (Ω)	$\pm V_{bus}$ (V)	10 percent THD+N power (W)	Duration
4	26.5	100	More than 1 minute without thermal shutdown
2	13.7	50	

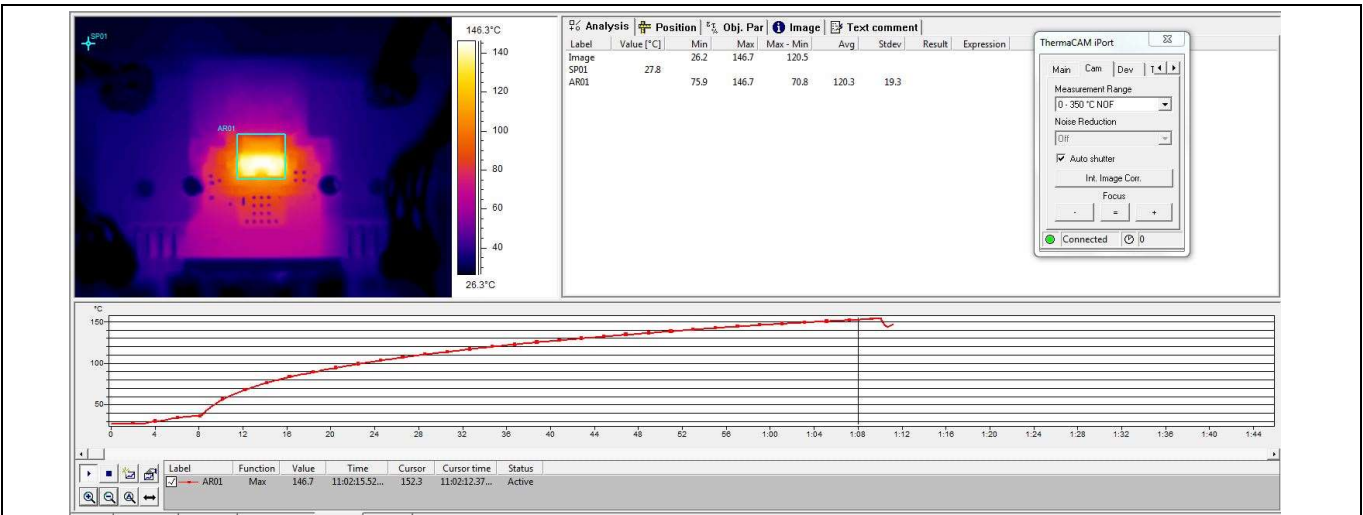


Figure 19 Peak power $P_{out} = 102\text{ W}$ with $4\ \Omega$ load $\pm 26.5\text{ V}$

Note: Maximum temperature 146.7°C at 1 minute.

Thermal information

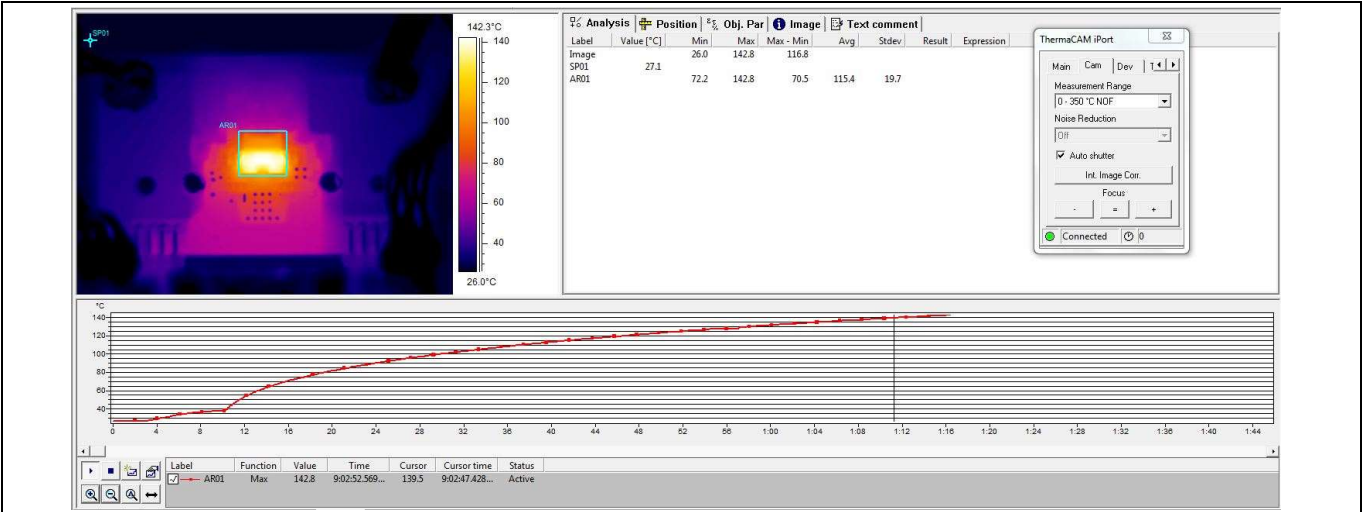


Figure 20 Peak power $P_{out} = 55\text{ W}$ with $2\ \Omega$ load $\pm 13.7\text{ V}$

Note: Maximum temperature 142.8°C at 1 minute.

Table 8 1/8 power test with heatsink

Load (Ω)	$\pm V_{bus}$ (V)	Max. T-case ($^\circ\text{C}$)	1/8 power (W)	Duration (minutes)
6	40	71.6	16.5	30
4	36.5	85.6	19.8	30
3	31.5	87.2	19.7	30
2	23	84.8	15	30

Table 9 1/8 power test without heatsink

Load (Ω)	$\pm V_{bus}$ (V)	Max. T-case ($^\circ\text{C}$)	1/8 power (W)	Duration (minutes)
4	22.7	84.6	7.12	30
2	13.7	76.1	4.88	30

5.2 Heatsink Information

Heatsink: V8818V

Thermal pad: BER161-ND



Figure 21 Heatsink installation

6 Functional Block Diagram

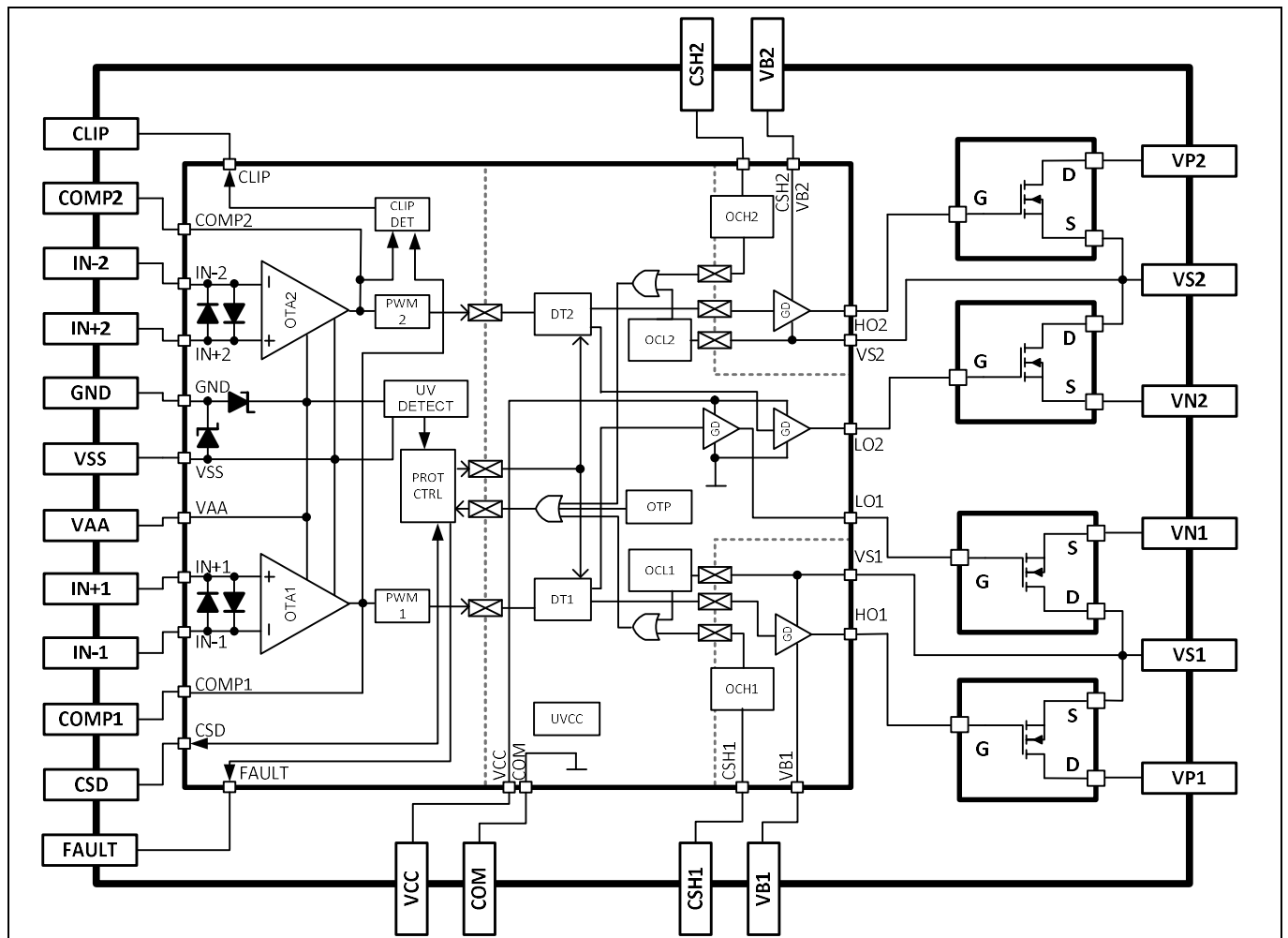


Figure 22 Block diagram

7 Typical Implementation

The MA5332MS offers versatile design options and can be configured as single-ended, BTL, or parallel single-ended (PSE) output using a single or split power supply. Below are some examples of typical configurations. A single-ended input with a split power supply serves as the base example, with the frontend section referring to GND, which is common to the speaker output GND.

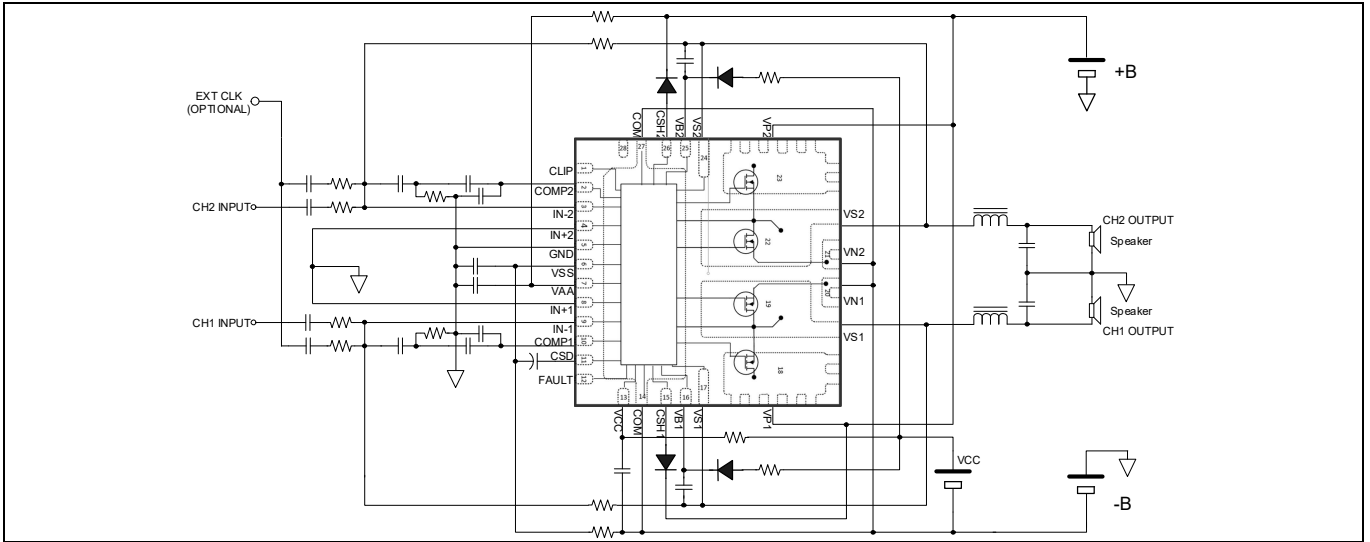


Figure 23 Inverting amplifier with Split Power Supply

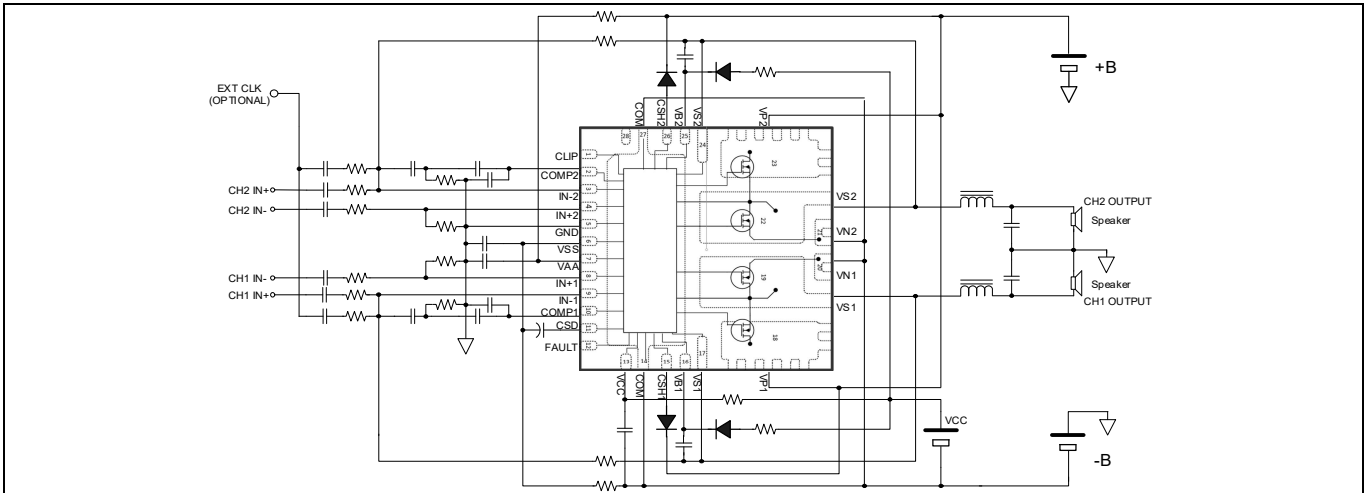


Figure 24 Differential amplifier with Split Power Supply

Typical implementation

The single-supply configuration uses a virtual GND which sits in the middle of the power supply rail. The front-end section of the amplifier refers to the virtual GND as a reference. This method uses differential input to receive an input signal from a different voltage potential. It is recommended to allow input capacitors to fully settle to steady-state values before releasing the CSD pin to start PWM oscillation. The load current and inductor ripple current flow through the bus splitting capacitor.

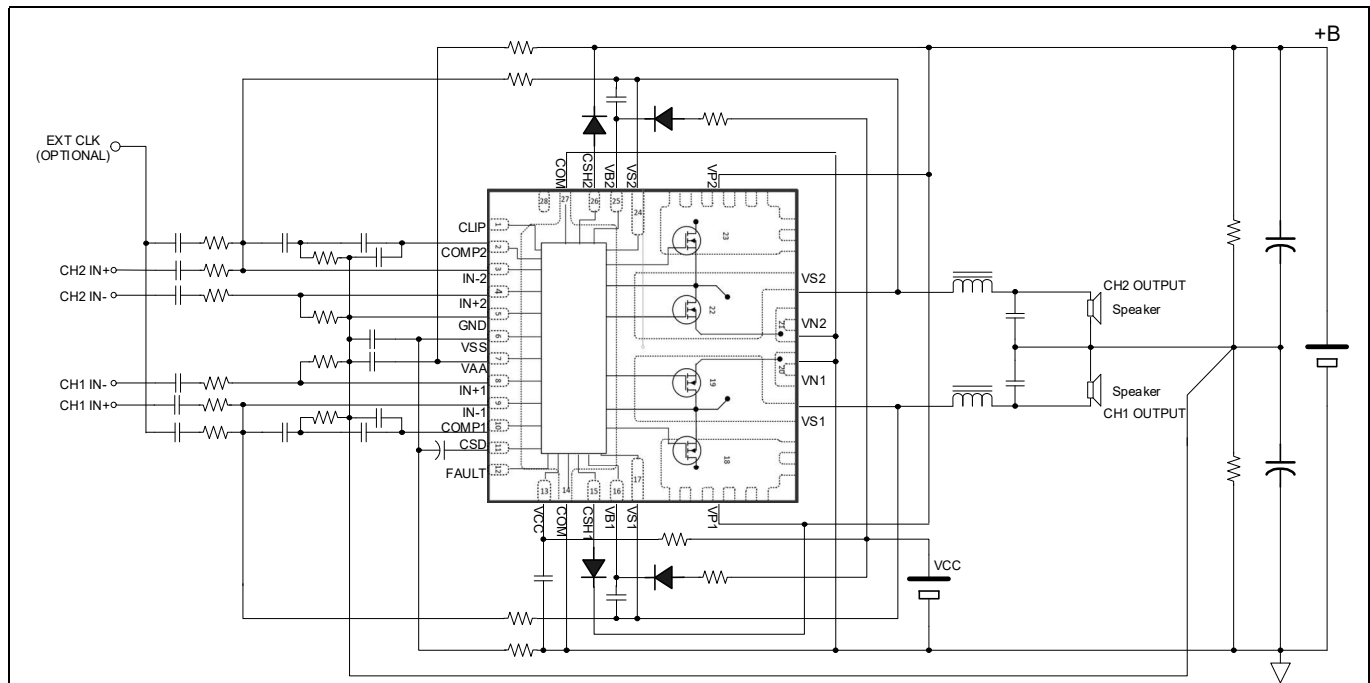


Figure 25 Typical Application Circuit with Single Power Supply

Balanced Tied Load (BTL) output takes two output legs for speaker output. It doubles output power with double load impedance. Any load current does not flow through supply dividing capacitor; therefore BTL configuration is free from GND fluctuations. Also, the bus splitting capacitor can be much smaller. Higher output power and absence of GND fluctuation make BTL suitable for subwoofer applications.

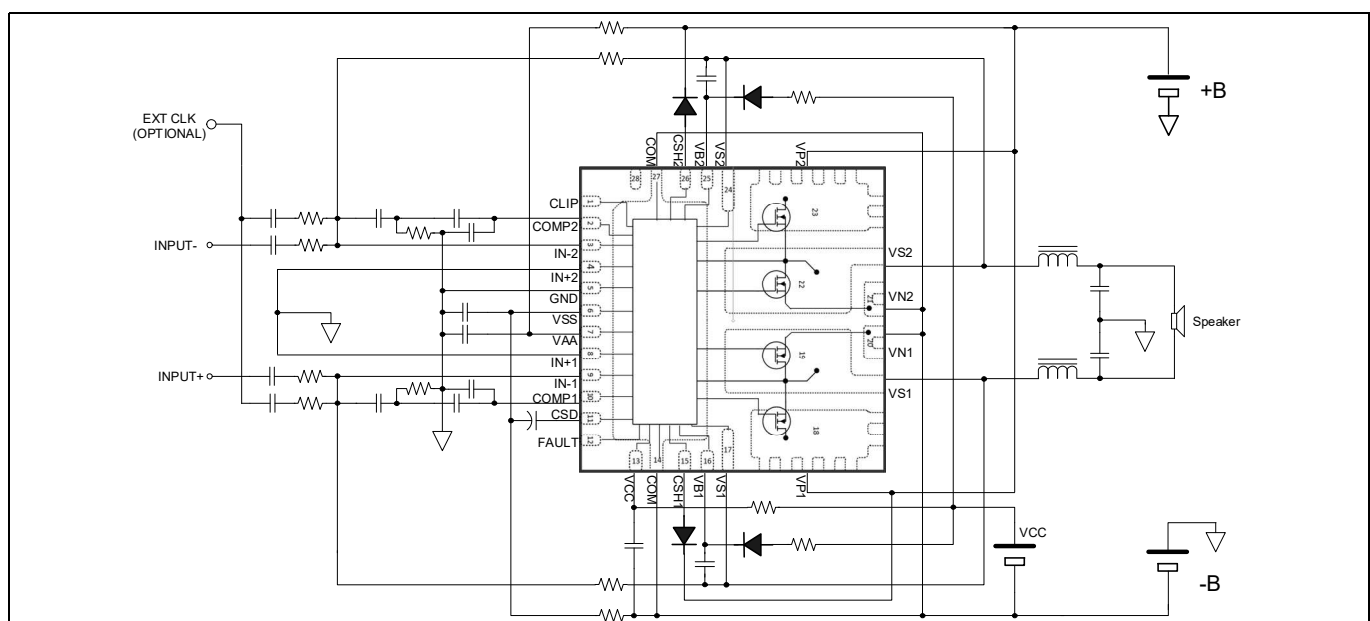


Figure 26 Typical Bridged Tied Load (BTL) Output Application with Split Power Supply

Typical implementation

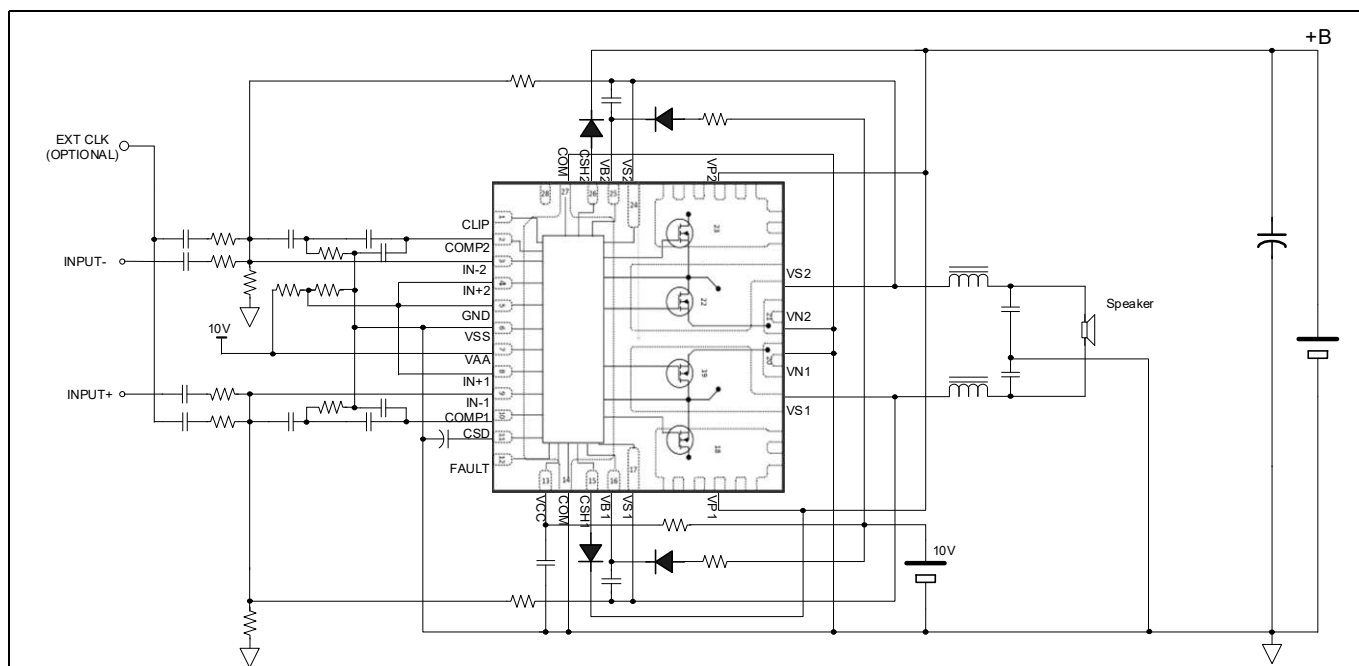


Figure 27 Typical Bridged Tied Load (BTL) Output Application with Single Power Supply

Parallel Single Ended (PSE) output parallels two channels' output legs for one speaker output. It doubles output current and makes it easier to drive a low impedance load. Higher output current with lower bus voltage makes PSE suitable for subwoofer applications.

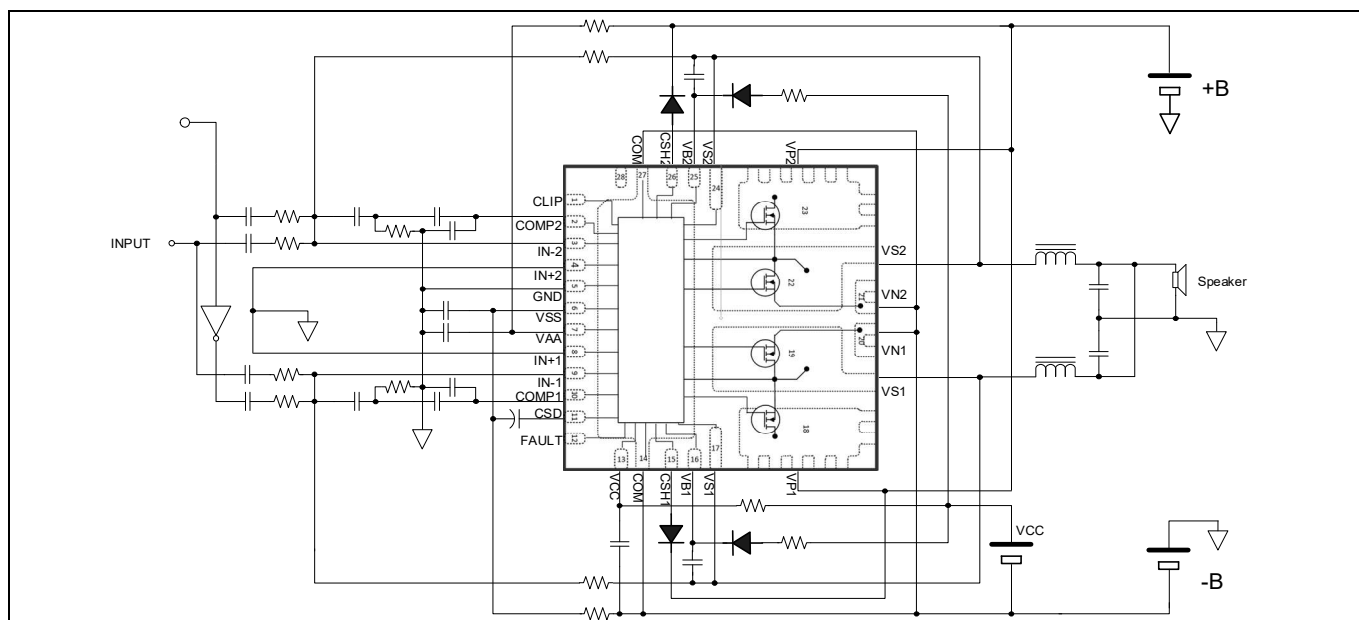


Figure 28 PSE amplifier with Split Power Supply

8 Input / Output Pin Equivalent Circuit Diagrams

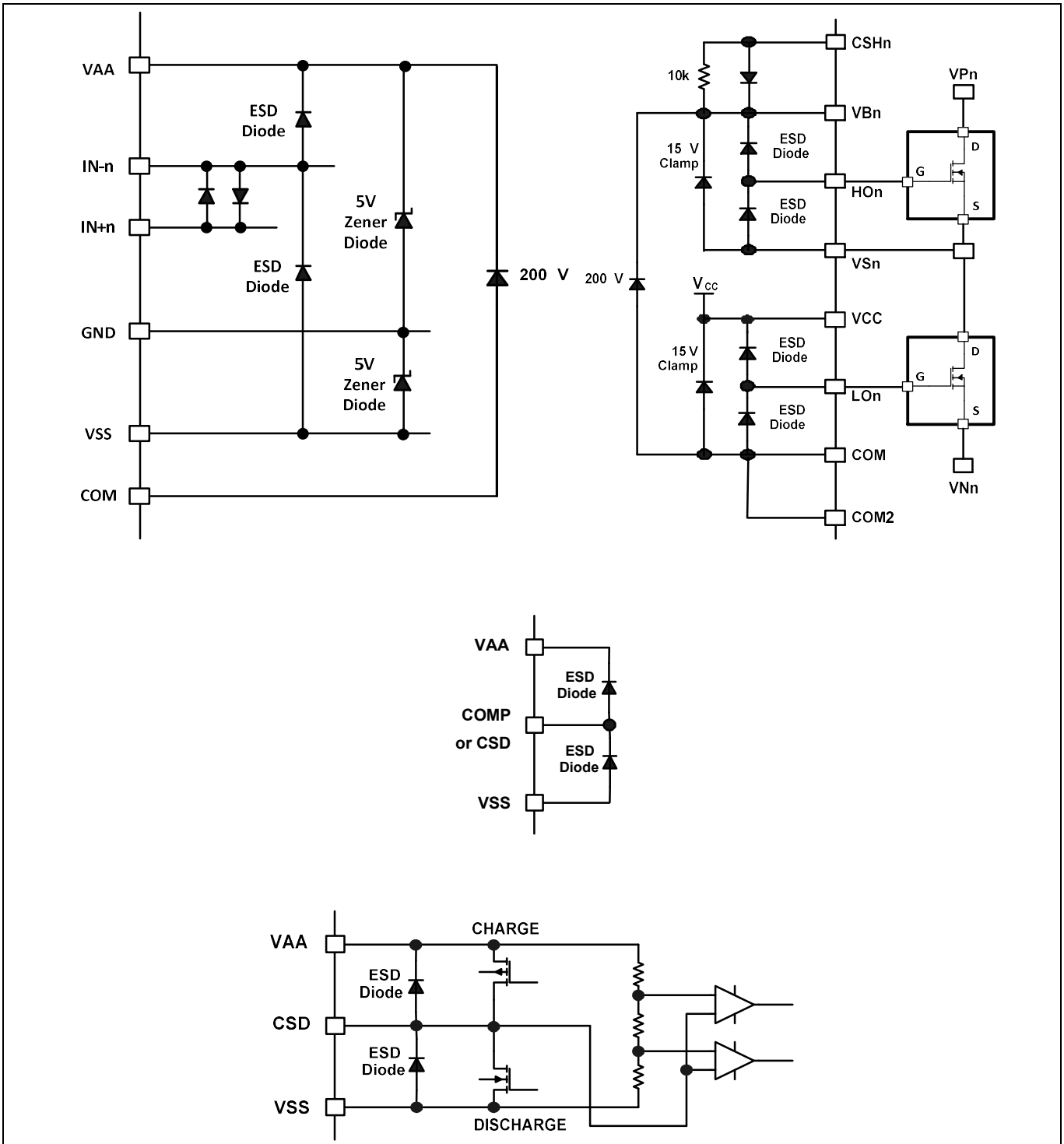


Figure 29 Input/output pin equivalent circuit diagrams

9 PWM Modulator Design

The open-access front-end configuration of MA5332MS enables many ways to implement a PWM modulator. This section explains how PWM modulation works based on an example of a self-oscillating PWM modulator in a typical application.

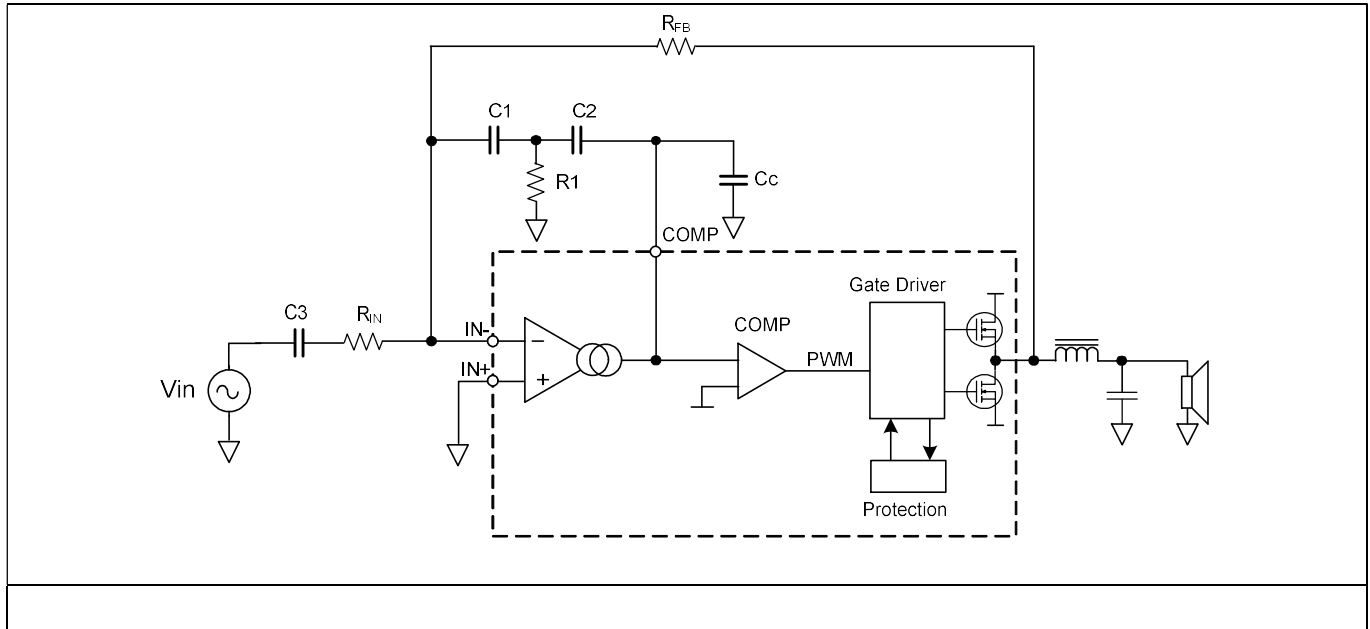


Figure 30 MA5332MS Typical Control Loop Design

9.1 Input Section

The audio input stage of MA5332MS forms an inverting error amplifier. The voltage gain of the amplifier, G_v , is determined by the ratio between input resistor R_{IN} and feedback resistor R_{FB} .

$$G_v = \frac{R_{FB}}{R_{IN}}$$

Since the feedback resistor R_{FB} is part of an integrator time constant, which determines switching frequency, changing the overall voltage gain by R_{IN} is simpler and therefore recommended. Note that the input impedance of the amplifier is equal to the input resistor R_{IN} .

A DC blocking capacitor $C3$ should be connected in series with R_{IN} to minimize the DC offset voltage on the output. Due to potential distortion, a ceramic capacitor is not recommended. Minimizing the DC offset is essential to minimize the audible noise during power-ON and -OFF.

The connection of the non-inverting input $IN+$ is a reference for the error amplifier, and thus is crucial for audio performance. Connect $IN+$ to the signal reference ground in the system, which has the same potential as the negative terminal of the speaker output.

9.2 Control Loop Design

The MA5332MS allows the user to choose from numerous methods of PWM modulator implementations. In this section, all the explanations are based on a typical application circuit of a self-oscillating

9.3 PWM Frequency

Choosing the switching frequency entails making a trade-off between many aspects. At lower switching frequency, conduction losses in the MOSFET stage increases due to higher inductor ripple current. The output carrier leakage in the speaker output increases. At higher switching frequency, the efficiency degrades due to higher switching losses. Higher switching frequency supports wider audio bandwidth. The inductor ripple decreases yet core loss might increase. For these reasons, 400kHz is chosen for a typical design example.

Self-oscillating frequency has little influence from the bus voltage and input resistance R_{IN} . Note that the nature of a self-oscillating PWM is for the switching frequency to decrease as PWM modulation deviates from idling.

Table 10 summarizes suggested values of components for a given target self-oscillating frequency. The front-end operational transconductance amplifier (OTA) output has limited voltage and current compliances. This set of component values ensures that OTA operates within its linear region for optimal THD+N performance. In case the target frequency is somewhere in between the frequencies listed in Table 10, simply adjust the frequency by tweaking R_1 .

Table 10 External Component Values vs. Self-Oscillation Frequency

Target Self-Oscillation Frequency (kHz)	C1=C2 (nF)	R1 (ohms)
500	2.2	200
450	2.2	165
400	2.2	141
350	2.2	124
300	2.2	115
250	2.2	102
200	4.7	41.2
150	10	20.0
100	10	14.0
70	22	4.42

9.4 Clock Synchronization

In the PWM control loop design example, the self-oscillating frequency can be set and synchronized to an external clock. Through a set of resistors and a capacitor, the external clock injects periodic pulsating charges into the integrator, forcing oscillation to lock up to the external clock frequency. A typical setup with 5 Vp-p 50% duty clock signal uses $R_{CK}=22\text{ k}\Omega$ and $C_{CK}=100\text{ pF}$ in Figure 31. To maximize audio performance, the self-running frequency without clock injection should be 20 to 30% higher than the external clock frequency.

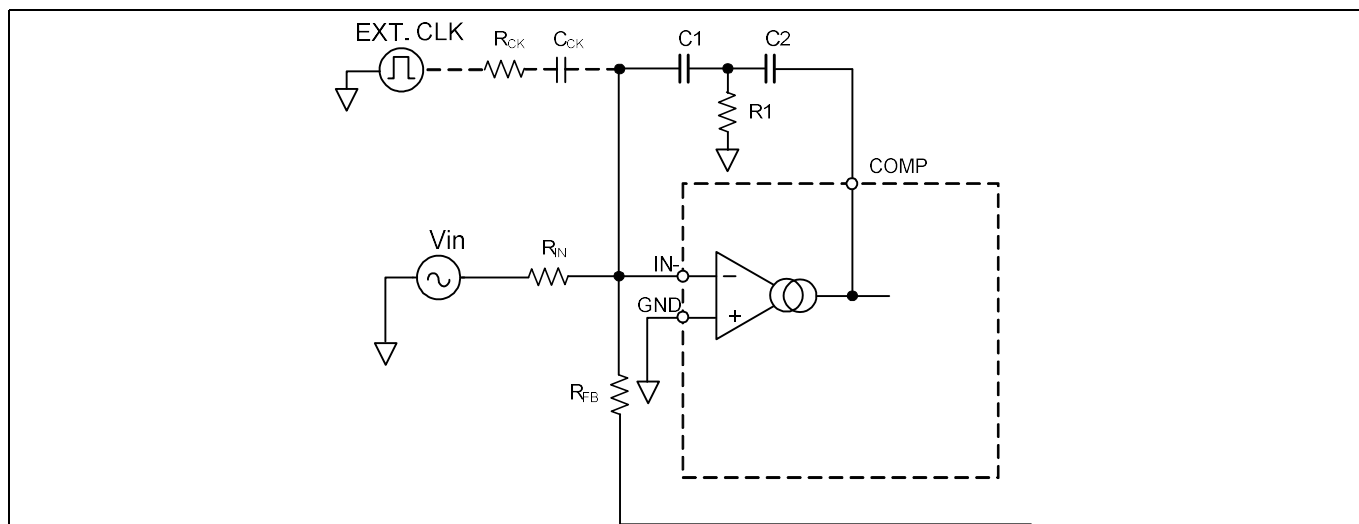


Figure 31 External Clock Synchronization

Figure 32 shows how a self-oscillating frequency locks up to an external clock frequency. A design of a 400 kHz self-oscillating frequency synchronizes to an external clock whose frequency is within the red border lines.

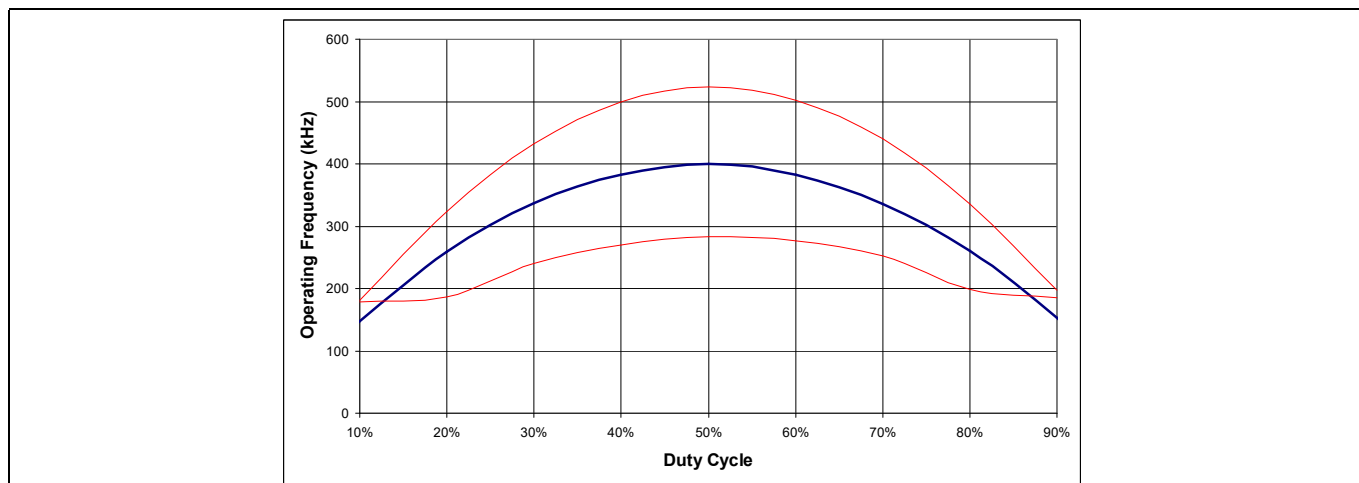


Figure 32 Typical Lock Range to External Clock ($R_{CK}=22\text{ k}\Omega$ and $C_{CK}=100\text{ pF}$)

9.5 Click Noise Elimination

The MA5332MS has a unique feature that minimizes power-ON and -OFF audible click noise. When CSD is in between V_{th1} and V_{th2} during start-up, an internal closed loop around the OTA enables an oscillation that generates voltages at COMP and IN-, bringing them to steady-state values. It runs at around 1 MHz, independent from the switching oscillation.

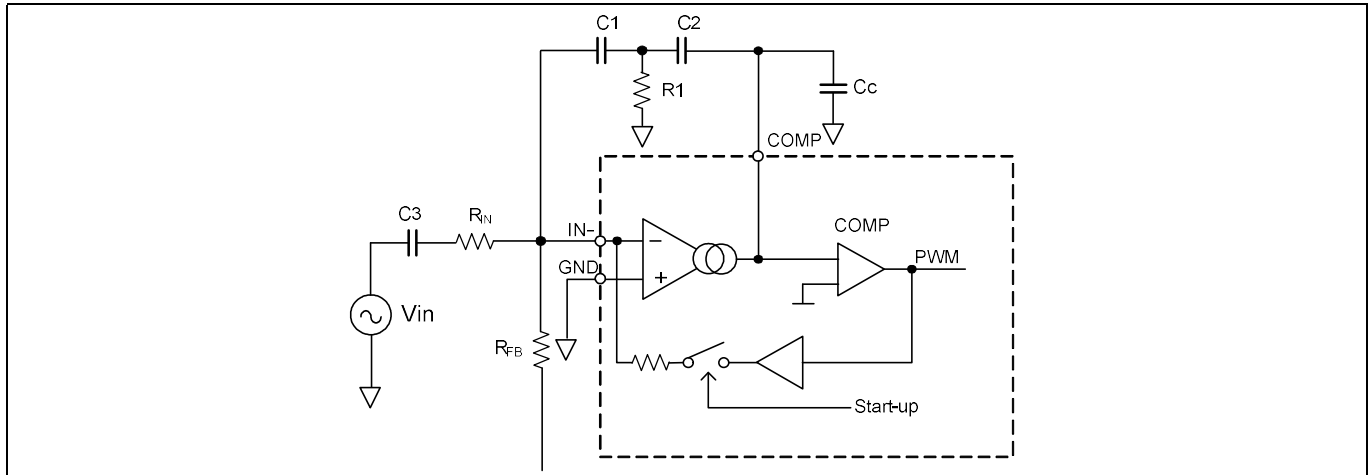


Figure 33 Audible Click Noise Elimination

As a result, all capacitive components connected to COMP and IN- pins, such as C1, C2, C3 and Cc in Figure 33, are pre-charged to their steady-state values during the start-up sequence. This allows instant settling of closed-loop PWM operation.

To utilize the click noise reduction function, the following conditions must be met.

1. CSD pin has slow enough ramp up from V_{th1} to V_{th2} such that the voltages in the capacitors can settle to their target values.
2. High-side bootstrap power supply needs to be charged up prior to starting oscillation.
3. Audio input has to be zero.
4. For internal local loop to override external feedback during the startup period, DC offset at speaker output prior to shutdown release has to satisfy the following condition.

9.6 Differential Input

Figure 34 shows an example of a differential input configuration. This design is useful in a single supply configuration. Use $R_{IN1}=R_{IN2}$, $R_{FB1}=R_{FB2}$, $C3=C4$.

Voltage gain is given by a ratio between R_{IN} and R_{FB} .

$$G_V = \frac{R_{FB}}{R_{IN}}$$

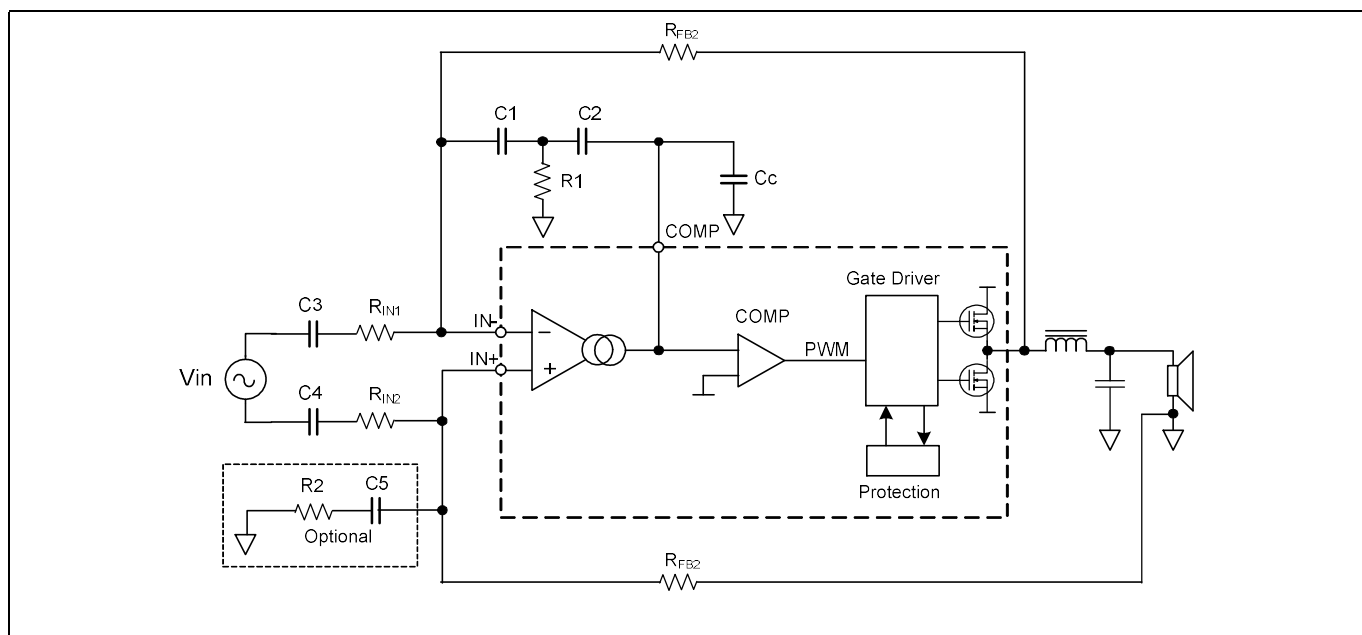


Figure 34 Differential Input

Although component values in the feedback network are balanced between inverting and non-inverting inputs, the integration capacitor path in the non-inverting input creates unbalance at high frequencies, causing slightly higher distortion compared to an unbalanced input configuration. To improve the THD degradations, place optional RC network $R2=R1$ and $C5=C1$.

10 Operational Mode

The CSD pin determines the operational mode of the MA5332MS as shown in Figure 35. The OTA has three operational modes: shutdown, pop-less startup and normal operation; while the gate driver section has two modes: shutdown and normal operation.

When $V_{CSD} < V_{th2}$, the IC is in shutdown mode and the input OTA is cut off. When $V_{th2} < V_{CSD} < V_{th1}$, the output MOSFETs are still in shutdown mode. The OTA is activated and starts local oscillation for pop-less start-up which pre-biases all the capacitive components in the error amplifier. When $V_{CSD} > V_{th1}$, the MA5332MS enters normal operation mode and PWM operation starts.

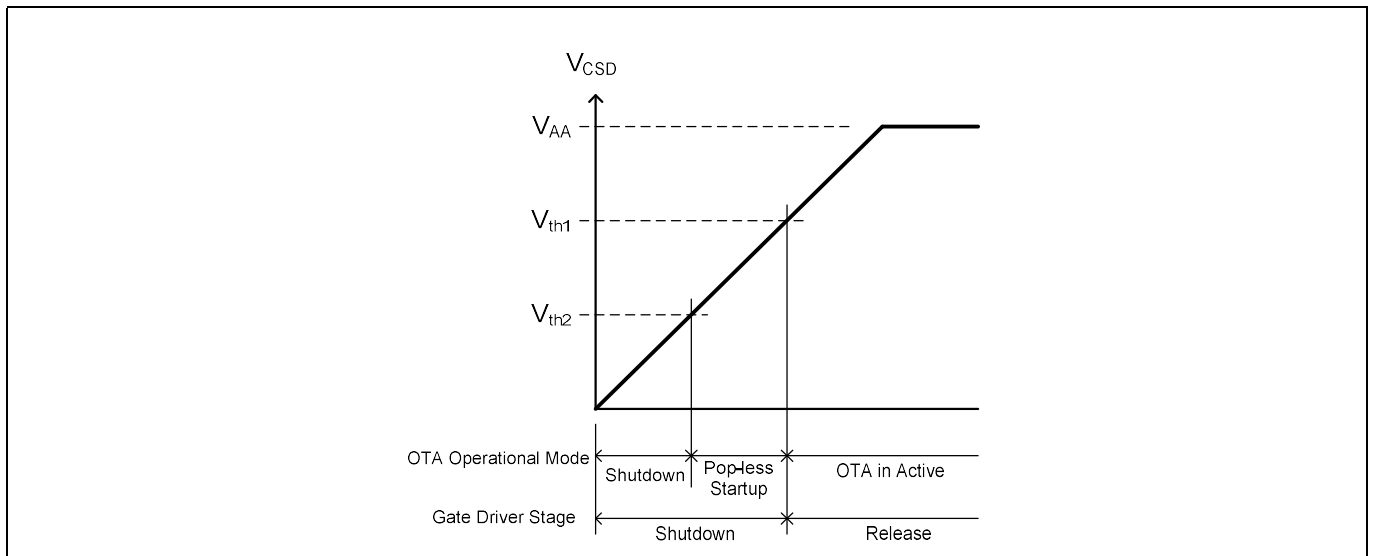


Figure 35 V_{CSD} and Operational Mode

10.1 Self-oscillation Start-up Condition

The MA5332MS requires the following conditions in order for pop-less startup to work properly.

- All the control power supplies, VAA, VSS, VCC and VBS are above the under-voltage lockout thresholds.
- CSD pin voltage is over V_{th1} threshold.
- $|i_{IN}| < |i_{FB}|$

$$\text{Where } i_{IN} = \frac{V_{IN}}{R_{IN}}, i_{FB} = \frac{V_{+B}}{R_{FB}}.$$

- The duration CSD voltage transitioning from V_{th2} to V_{th1} is long enough to pre-charge input and integration capacitors around OTA section.

11 Protections

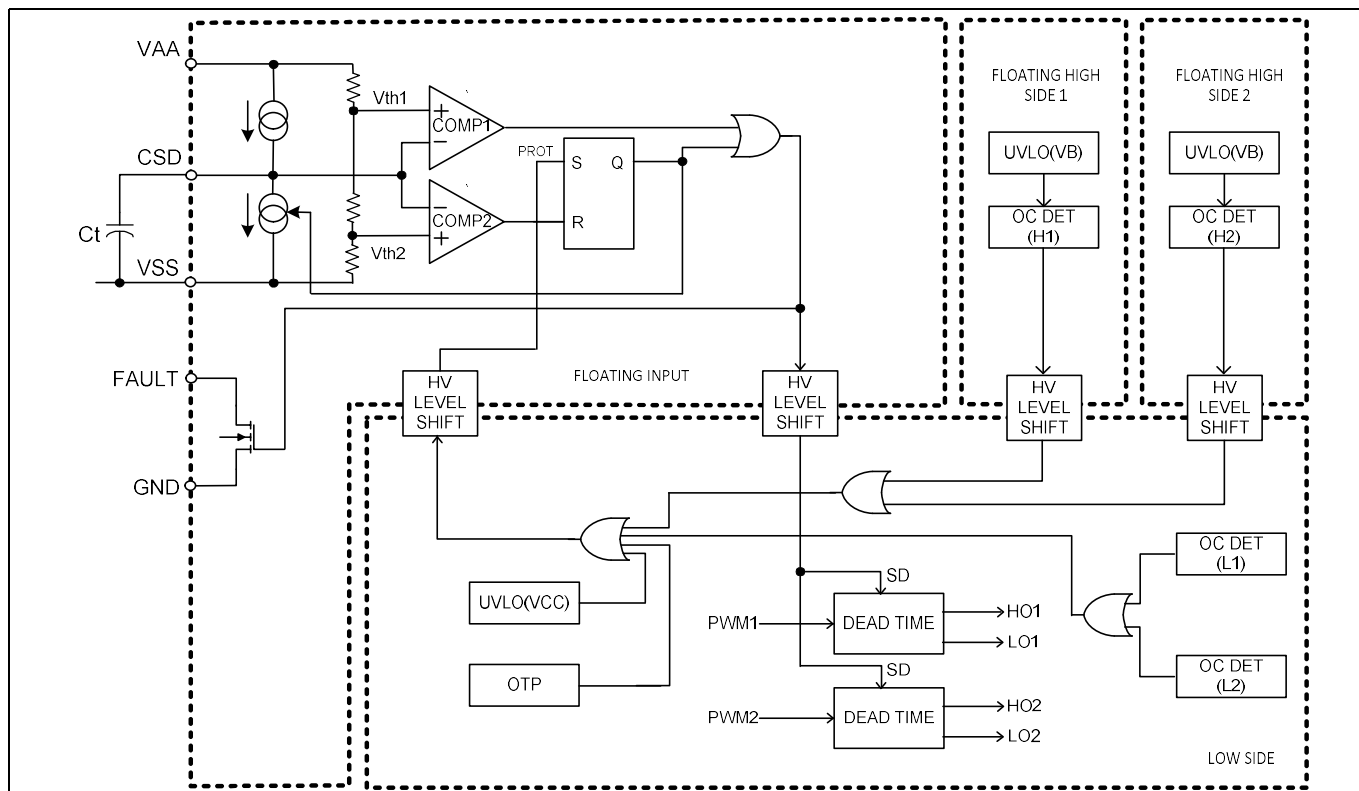


Figure 36 Protection Functional Block Diagram

The internal protection control block dictates the operational modes, normal or shutdown, using the input of the CSD pin. In shutdown mode, the controller IC turns off internal power MOSFETs.

The CSD pin provides five functions.

1. Power up delay timer
2. Self-reset timer
3. Shutdown input
4. Latched protection configuration
5. Shutdown status output (host I/F)

The CSD pin cannot be paralleled with another MA5332MS directly.

The operating statuses of the protection features are shown in Table 11.

Table 11 Events and Actions of CSD and FAULT

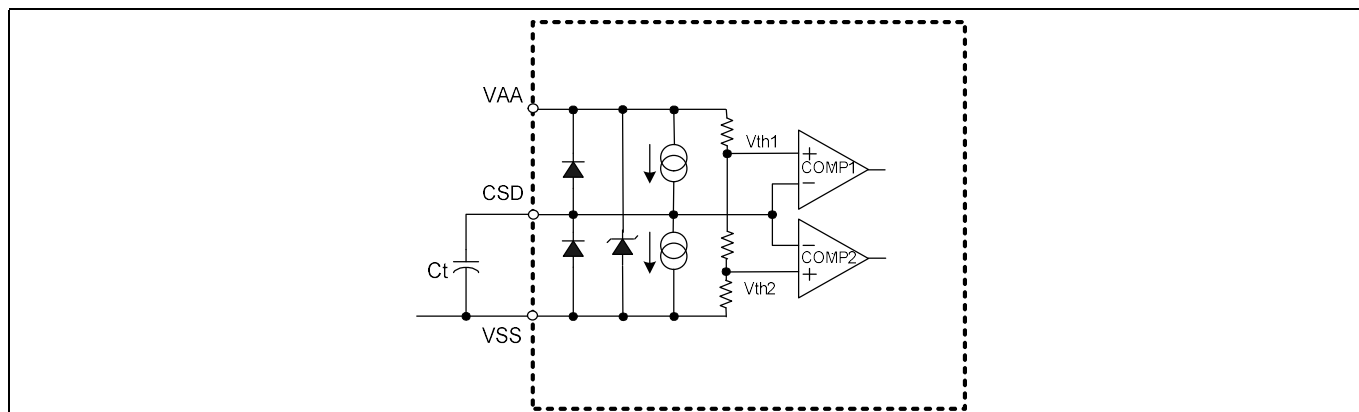
Event	CSD	FAULT
UVCC, rising edge	Recycle	L until CSD>Vth1
UVCC, falling edge	n/a	n/a
UVAA, rising edge	n/a	L at VAA<UVAA
UVAA, falling edge	n/a	L at VAA<UVAA
UVBS, rising edge	n/a	n/a
UVBS, falling edge	n/a	n/a
Over Current Protection	Keep recycling until OCP is reset	Held L until OCP is reset
Clip Detection	n/a	n/a
Over Temperature Protection	Keep recycling until OTP is reset	Held L until OTP is reset

*CSD recycle: CSD pin voltage discharges down to Vth2 and charges back to VAA, if CSD pin is configured as self reset protection.

11.1.1 Self-Reset Protection

Attaching a capacitor between CSD and V_{SS} configures the MA5332MS self-reset protection mode.

Upon an OCP event, the CSD pin discharges the external capacitor voltage V_{CSD} down to the lower threshold V_{th2} to reset the internal shutdown latch. Then, the CSD pin begins to charge the external capacitor, C_t, in an attempt to resume operation. Once the voltage of the CSD pin rises above the upper threshold, V_{th1}, the IC resumes normal operation.

**Figure 37 Self-Reset Protection Configuration**

11.1.4 Latched Protection

Connecting CSD to V_{AA} through a 10 k Ω or less resistor configures latched protection mode. The internal shutdown latch stays in shutdown mode after the overcurrent is detected. An external reset switch brings CSD below the lower threshold V_{th2} for a minimum of 200 ns and resets the latch. At first power-up, a reset signal to the CSD pin is required to release the IC from shutdown mode.

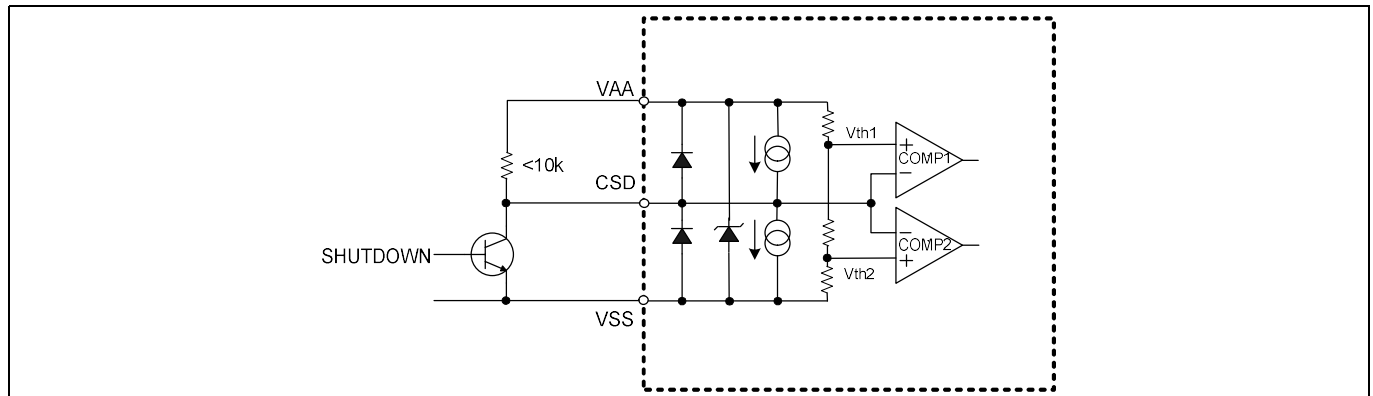


Figure 39 Latched Protection with Reset Input

11.1.5 Interfacing with System Controller

The MA5332MS can communicate with an external system controller through a simple interfacing circuit shown in Figure 40. A generic PNP transistor, U1, detects the sink current at the CSD pin during protection event and outputs a shutdown flag signal to an external system controller. Another generic NPN transistor, U2, can then reset the internal protection logic by pulling the CSD voltage below the lower threshold V_{th2} . After the first power-up sequence, a reset signal to the CSD pin is required to release the IC from shutdown mode.

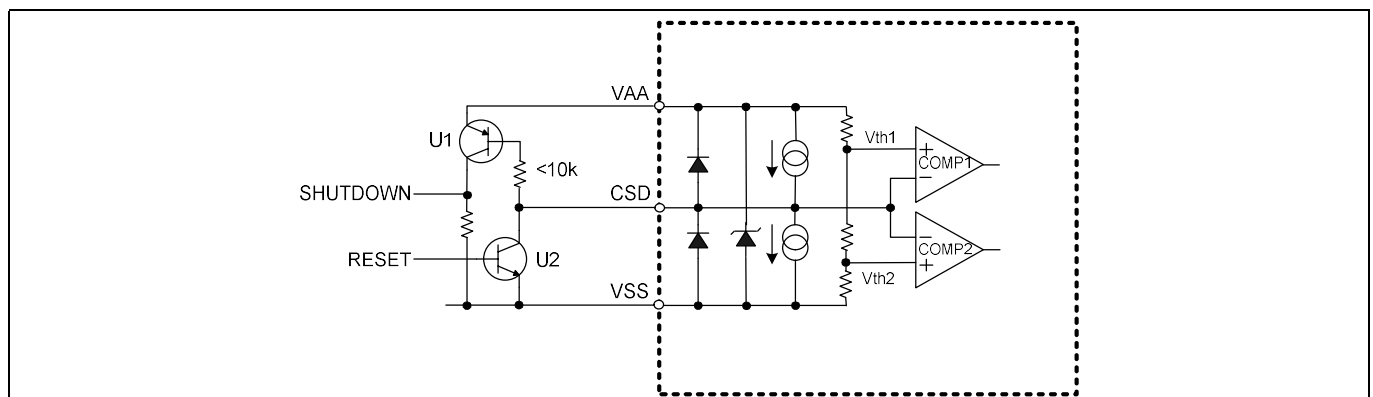


Figure 40 Interfacing CSD with System Controller

11.2 Over Current Protection (OCP)

The MA5332MS features over current protection to protect the internal power MOSFETs during abnormal load conditions. The control logic diagrams are in Figure 41. As soon as either the high-side or low-side current sensing block detects over current, the following sequence will occur.

1. The shutdown latch flips its logic states from normal operational mode to shutdown mode.
2. Low-side and high-side MOSFETs go into an off state condition.
3. The CSD pin starts discharging the external capacitor C_t .
4. When voltage across C_t falls below the lower threshold V_{th2} , COMP2 resets the shutdown latch to normal mode.
5. The CSD pin starts charging the external capacitor C_t .
6. When V_{CSD} goes above the upper threshold V_{th1} , the logic on COMP1 toggles and the IC resumes operation.

Figure 41 summarizes the above. As long as the over current condition exists, the IC will repeat the over current protection sequence at a repetitive rate set by the CSD capacitor.

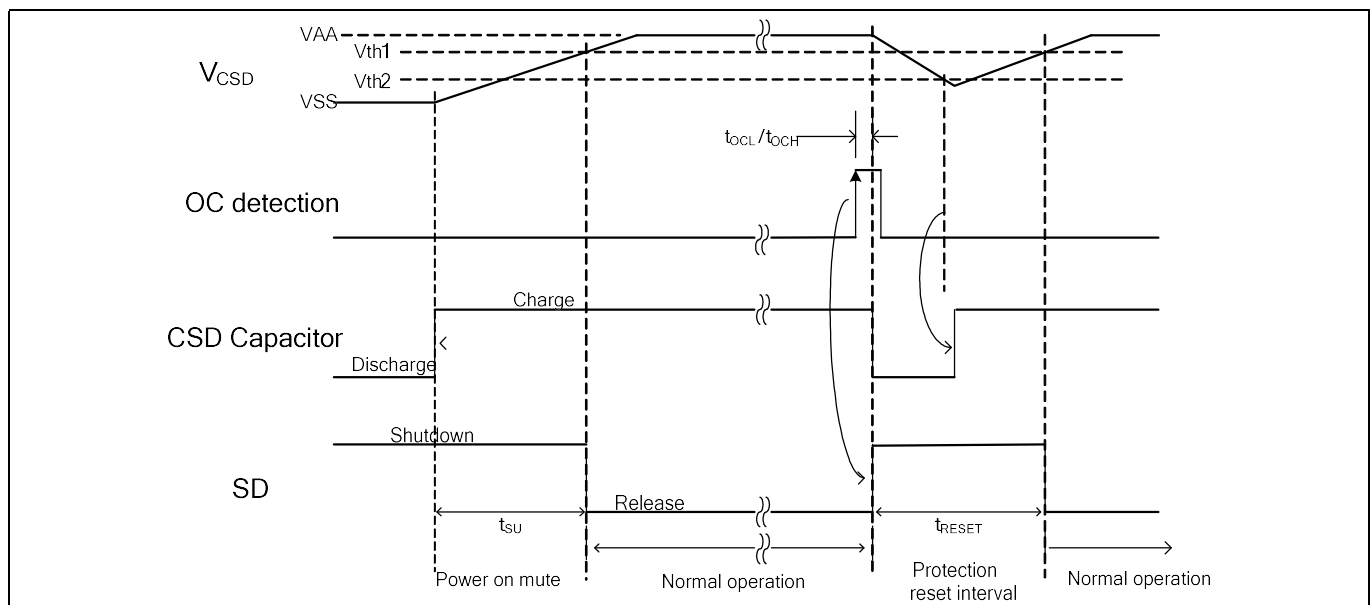


Figure 41 Overcurrent Protection Timing Chart

11.3 Over Temperature Protection (OTP)

If the junction temperature T_J of the controller IC exceeds the on-chip thermal shutdown threshold, T_{SD} , the on-chip over temperature protection shuts down the PWM.

11.4 Under Voltage Protection (UVP)

In order to prevent a partial on-state of the internal MOSFET, under-voltage protection monitors the low side and high side gate bias supplies, VCC and VB. When VCC is below UVLO, both high and low side MOSFETs are turned off. When the high side supply V_{BS} is below the UVLO threshold, the high side output is disabled, while the low side works normally.

12 Status Output

12.1 Fault Output

FAULT output is an open drain output referenced to GND to report whether the MA5332MS is in shutdown mode or in normal operating mode. If the FAULT pin is open, the MA5332MS is in normal operation mode, i.e. the output MOSFETs are active. The following conditions trigger shutdown internally and pulls the FAULT pin down to GND.

- Over Current Protection
- Over Temperature Protection
- Shutdown mode from CSD pin voltage

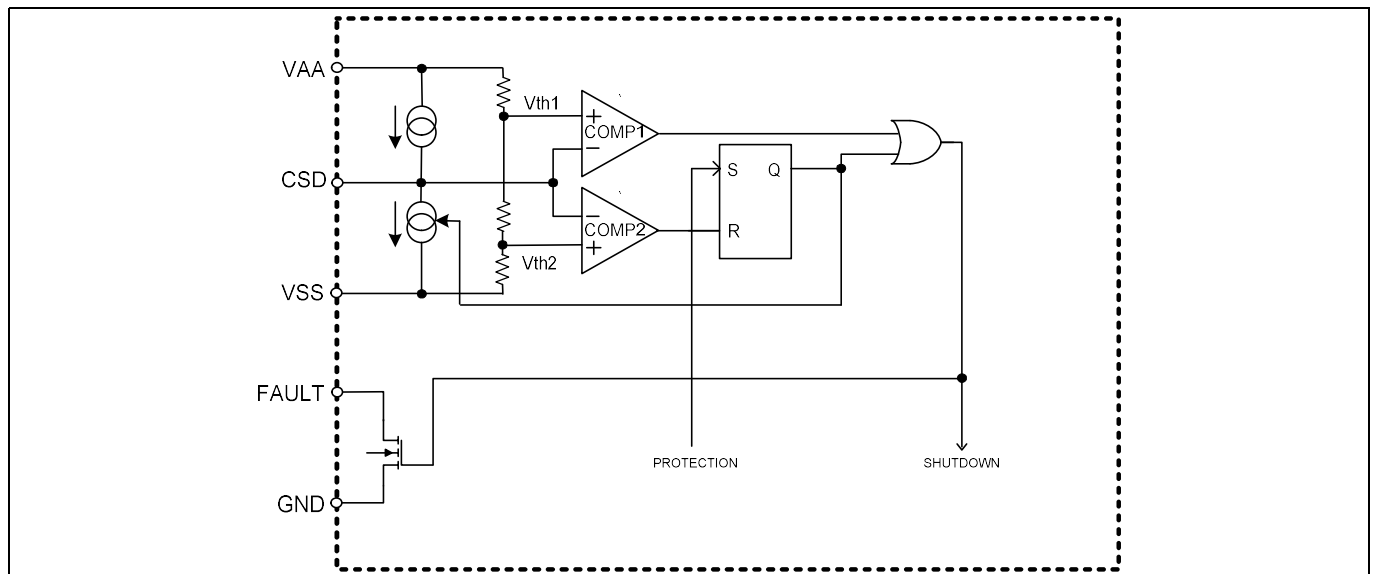


Figure 42 Fault Output

12.2 CLIP Output

When the output of the amplifier loses track of an expected target value, the amplifier enters into clipping condition.

The CLIP detection block monitors the COMP pin voltage with a window comparator. The CLIP pin is pulled to GND when a clipping condition is detected. The detection thresholds in the COMP pin are at 10% and 90% of VAA-VSS. The CLIP outputs are disabled in shutdown mode.

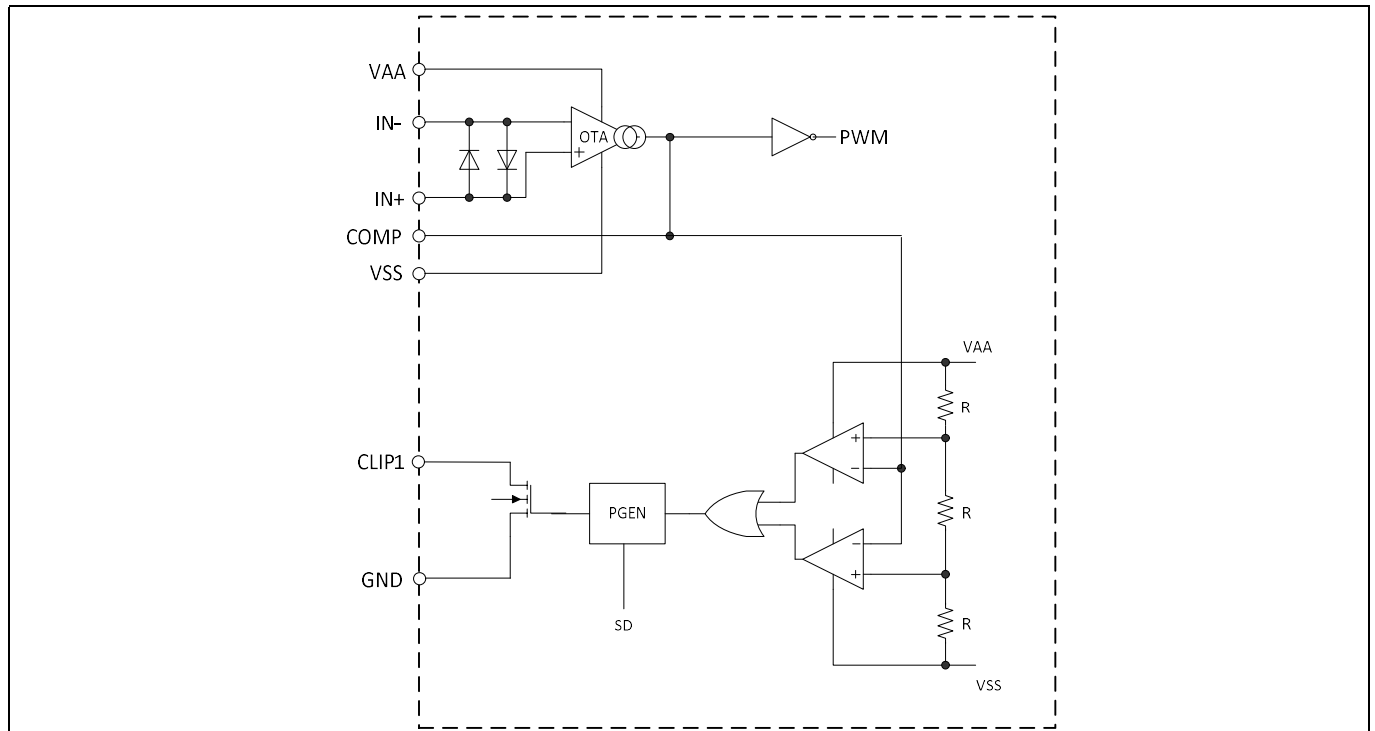


Figure 43 CLIP Detection

13 Power Supply Design

13.1 Supplying VAA and VSS

VAA and VSS are supply voltages to the front-end of the analog section, hence are noise sensitive. For best audio performance, use regulated power supplies for VAA and VSS.

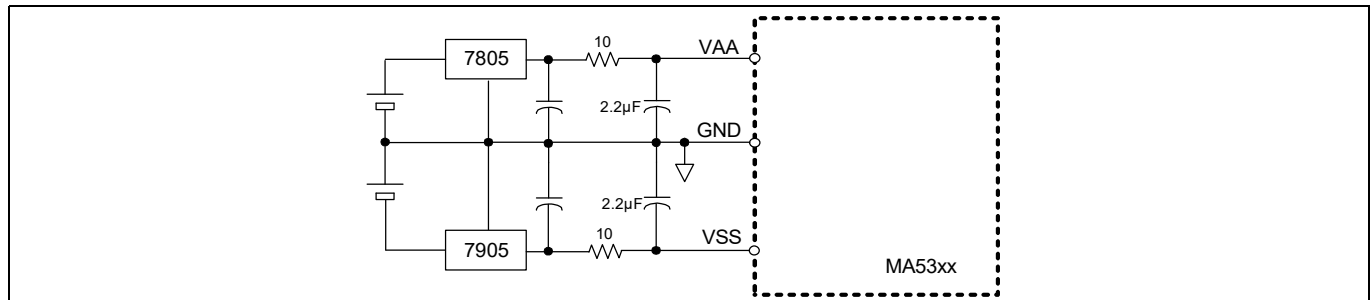


Figure 44 Supplying VAA and VSS with External Voltage Regulators

When switched-mode regulators are used as supply voltages for VAA and VSS, place a two-stage R-C noise filter in the supply lines as shown in Figure 45.

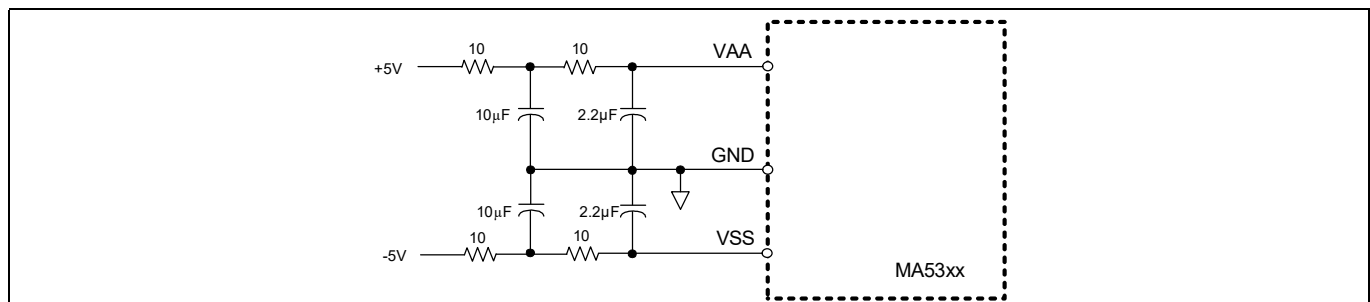


Figure 45 Supplying VAA and VSS from Switched Mode Power Supply

13.2 Supplying VCC and VB

Figure 46 shows the recommended power supply configuration for gate driver power supplies. The gate driver stage has three power supply inputs:

1. VCC-COM: low side gate drive supply
2. VB1-VS1: CH1 high side gate drive supply
3. VB2-VS2: CH2 high side gate drive supply

The low-side power supply, VCC, feeds the internal gate drive logic and low side gate driver. In order to protect VCC from switching noise generated by the VS node, it is recommended to insert a few ohms of R_{VBS} in the bootstrap charging path.

The high-side driver requires a floating supply VB_n referenced to the respective switching node VS_n where the source of the output MOSFET is connected. A charge pump method (floating bootstrap power supply) eliminates the need for a floating power supply and thus is used in the typical application circuit. The floating bootstrap power supply charges the bootstrap capacitor C_{BS} from the low-side power supply VCC during the low-side MOSFET ON period. When the high-side MOSFET is ON, the diode cuts off and floats the VBS supply. C_{BS} retains its VB supply voltage for the rest of the high-side ON duration.

$$I_{VCC} \approx I_{QCC} + I_{QBS} + 2(Q_G \cdot f_{PWM}) \text{ /per channel}$$

Recommend to have minimum 20% design margin for I_{VCC} .

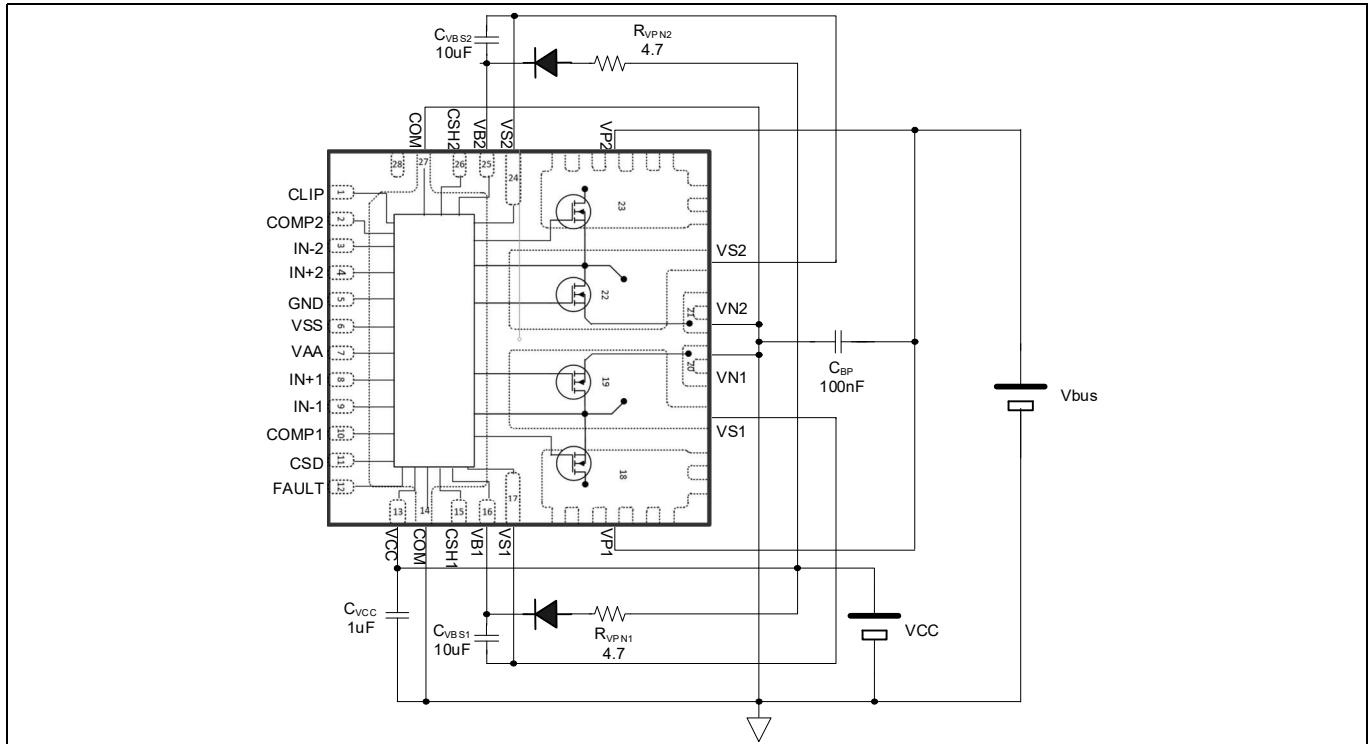


Figure 46 Recommended Power Supply Configurations for Output Stage

13.2.1 Choosing Bootstrap Capacitance

Often MA5332MS uses hard clipping condition. The continuous high-side ON duration could continue as long as half of the lowest audio frequency, tens of milliseconds. A typical application uses a 22 uF C_{BS} to support low audio frequency clipping. A ceramic capacitor (X7R, X5R or X5S type) or aluminum electrolytic capacitor with 25 V or higher voltage rating is recommended.

13.2.2 Choosing Bootstrap Diode

Use a bootstrap charging diode with voltage rating of 1.5 x the maximum bus voltage. In order to charge the bootstrap capacitor in a very short low-side ON period with a high PWM modulation ratio, a fast recovery diode type ($t_{rr} < 50\text{ns}$) is recommended.

13.2.3 Charging V_{BS} Prior to Start

For proper start-up, pre-charging the bootstrap supply V_{BS} prior to PWM start-up is necessary for self-oscillating PWM modulator topologies. A charging resistor, R_{CHARGE} , inserted between the positive supply bus and V_{BS} , charges C_{BS} prior to switching start as shown in Figure 47. The minimum resistance of R_{CHARGE} is limited by the maximum PWM modulation index of the system. When the high-side MOSFET is on, R_{CHARGE} drains the bootstrap power supply together with the quiescent current, I_{QBS} , so it reduces the holding time, resulting in maximum continuous high-side on time.

The maximum resistance of R_{CHARGE} is limited by the current charge capability of the resistor during startup.

Power supply design

Pre-charging current flows into the speaker load. In order to startup without the load connected, a dummy load R_{dummy} in parallel with the speaker output provides a pre-charging current path.

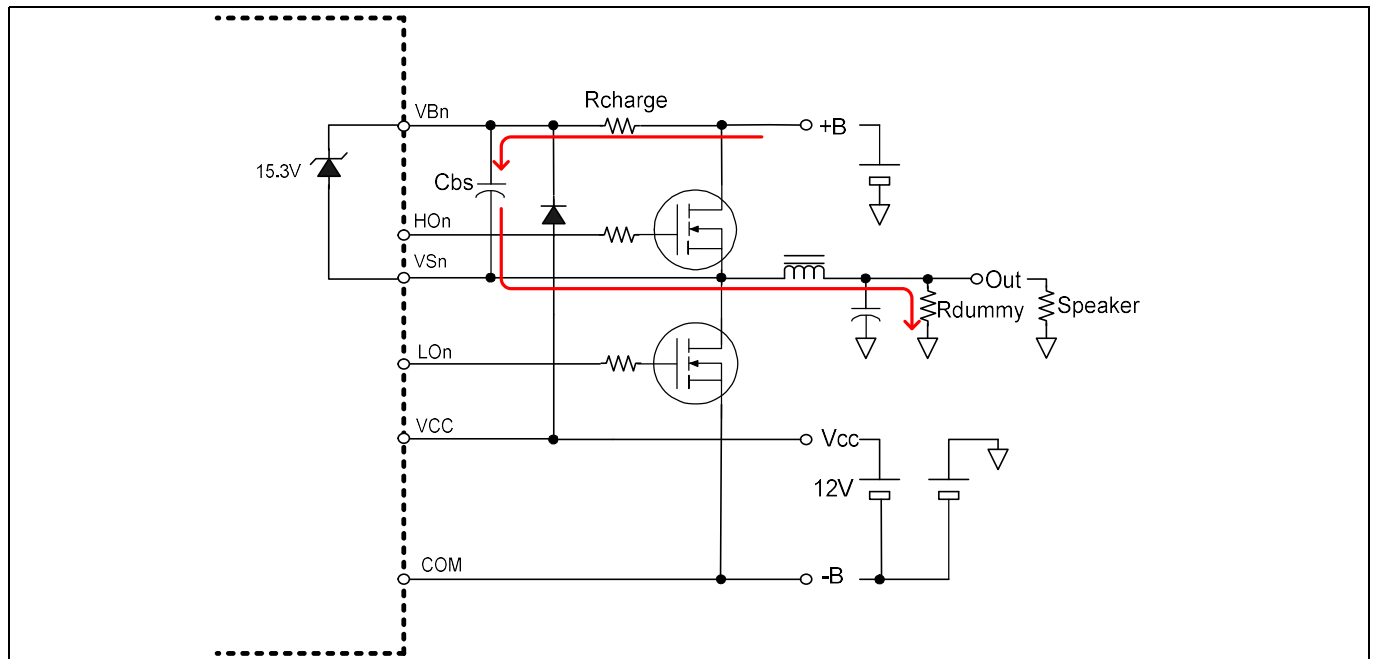


Figure 47 Bootstrap Supply Pre-Charging

13.3 Power Supply Sequence

The protection control block in the MA5332MS monitors the status of V_{AA} and V_{CC} to ensure that both voltage supplies are above their respective UVLO (under voltage lockout) thresholds before starting normal operation. If either V_{AA} or V_{CC} is below the under voltage threshold, the output MOSFETs are disabled in shutdown mode until both V_{AA} and V_{CC} rise above their voltage thresholds. As soon as V_{AA} or V_{CC} falls below its UVLO threshold, protection logic in the MA5332MS turns off high-side and low-side.

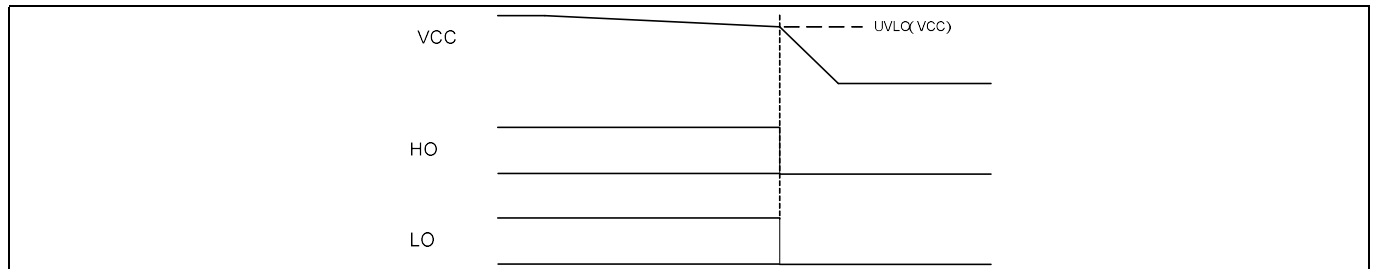


Figure 48 MA5332MS UVLO Timing Chart

14 Package details

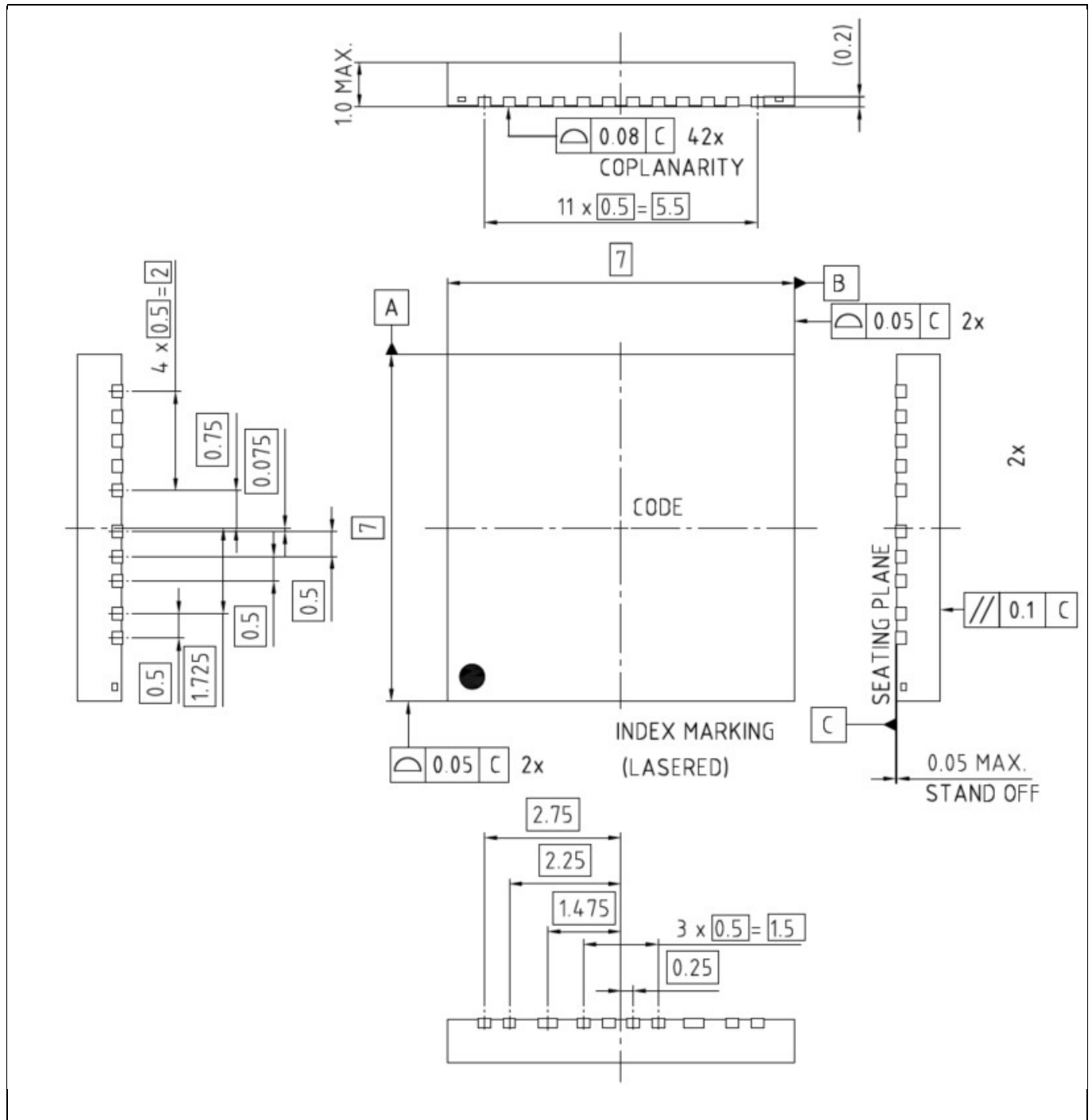


Figure 49 Package details

Package details

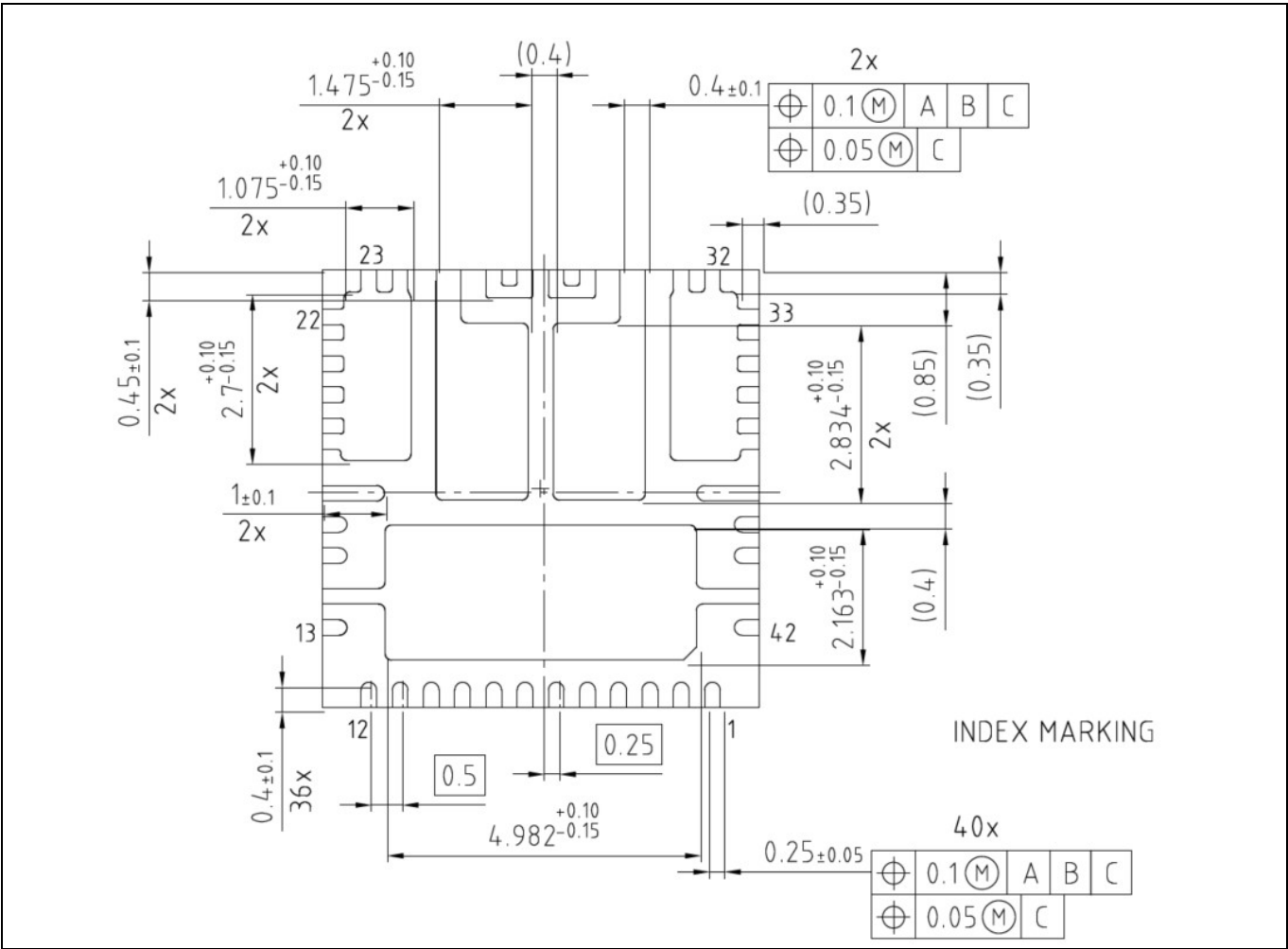


Figure 50 Package details; Bottom metallization detail view

Package details

Dimension Table				
Thickness Symbol	V			Note
	Minimum	Normal	Maximum	
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3	---	0.20 Ref	---	
b1	0.20	0.25	0.30	5
b2	0.35	0.40	0.45	5
D	7.00 BSC			
E	7.00 BSC			
D1	2.013	2.163	2.263	
E1	4.832	4.892	5.082	
D2	2.55	2.700	2.800	
E2	0.925	1.075	1.175	
D3	2.684	2.834	2.934	
E3	1.325	1.475	1.575	
L1	0.30	0.40	0.50	
L2	0.90	1.00	1.10	
L3	0.35	0.45	0.55	
aaa	0.05			
bbb	0.10			
ccc	0.10			
ddd	0.05			
eee	0.08			
N	42			3
Notes	1,2			

Figure 51 Dimension table

15 Board mounting, part marking, and ordering information

Reliability of products in the PQFN package is subject to the board mounting process. The Soldering process is critical. Refer to Application Note AN-1170 Audio IC Board Mounting Application Note for specific footprint design and soldering methods.

Device outline

Figure 52 shows the outline for these devices. The relative pad positions are controlled to an accuracy of $\pm 0.050\text{mm}$. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

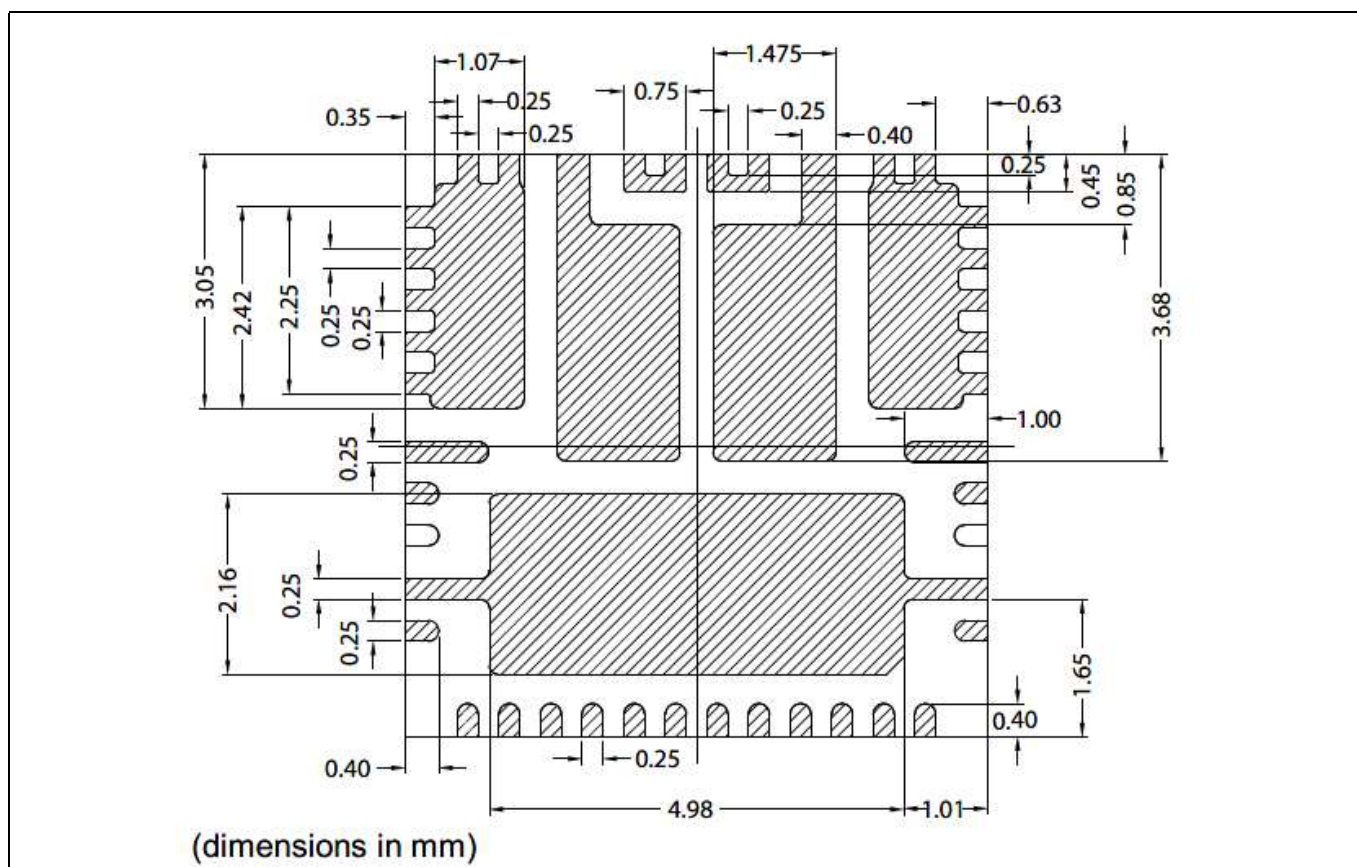


Figure 52 42-lead 7x7 device outline

Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure 53 and Figure 54

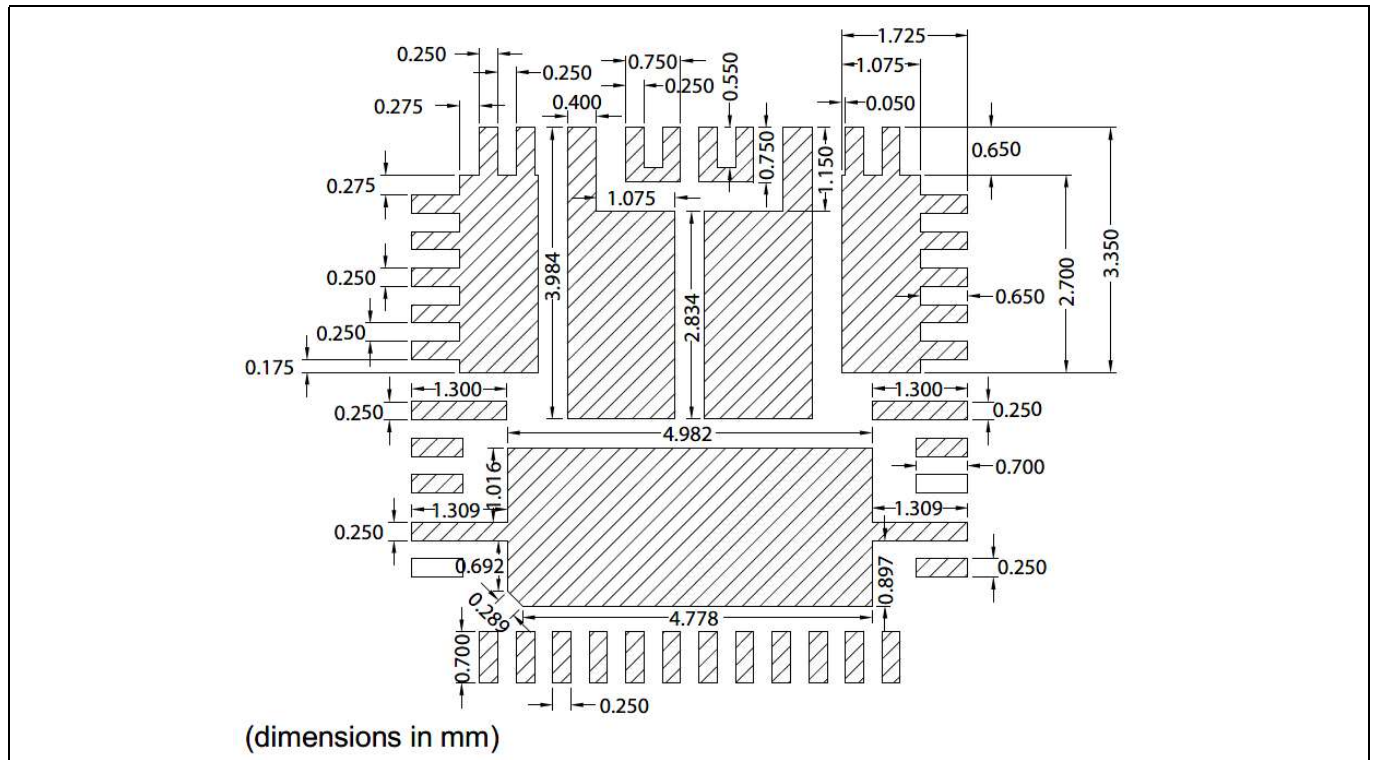


Figure 53 42-lead 7x7 substrate /PCB layout_1

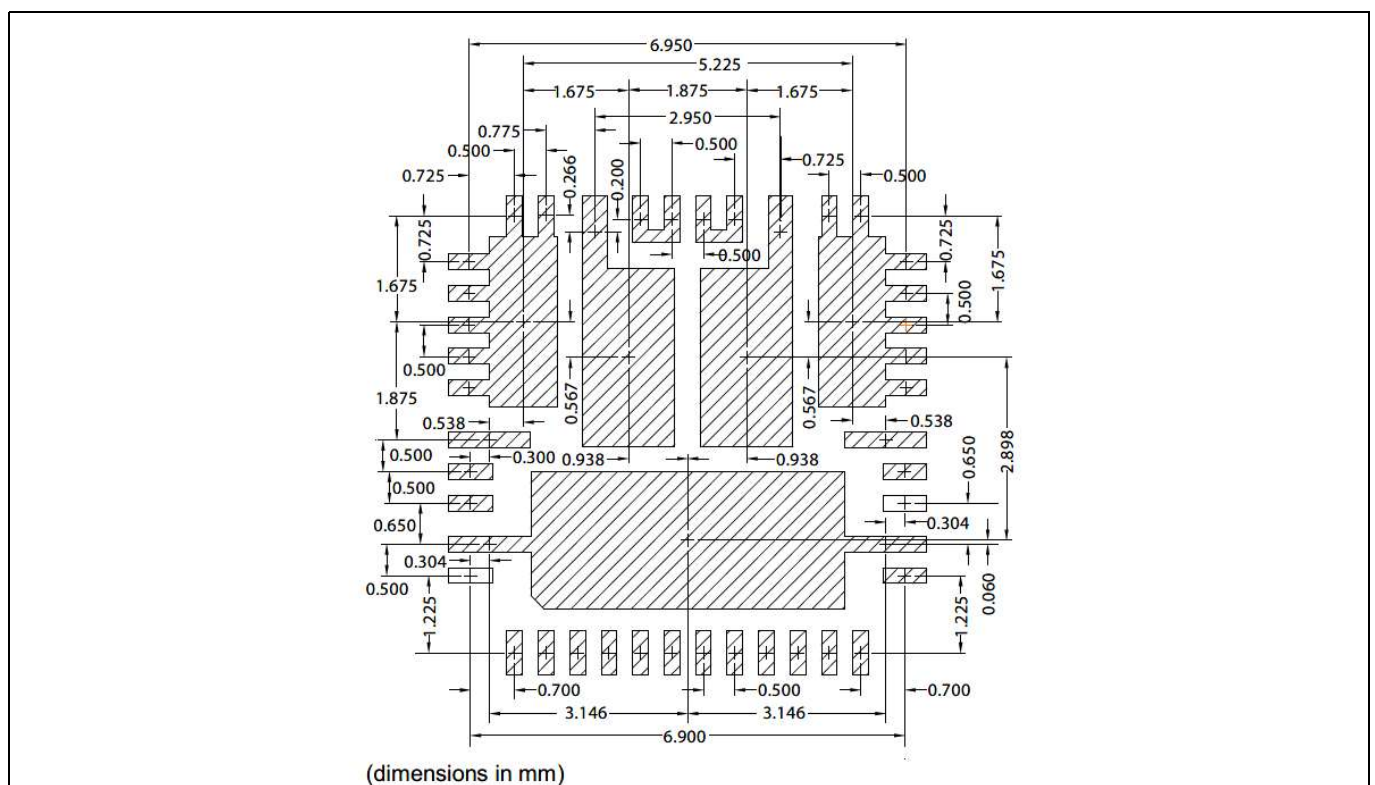


Figure 54 42-lead 7x7 substrate /PCB layout_2

Stencil Design

Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure 55-58.

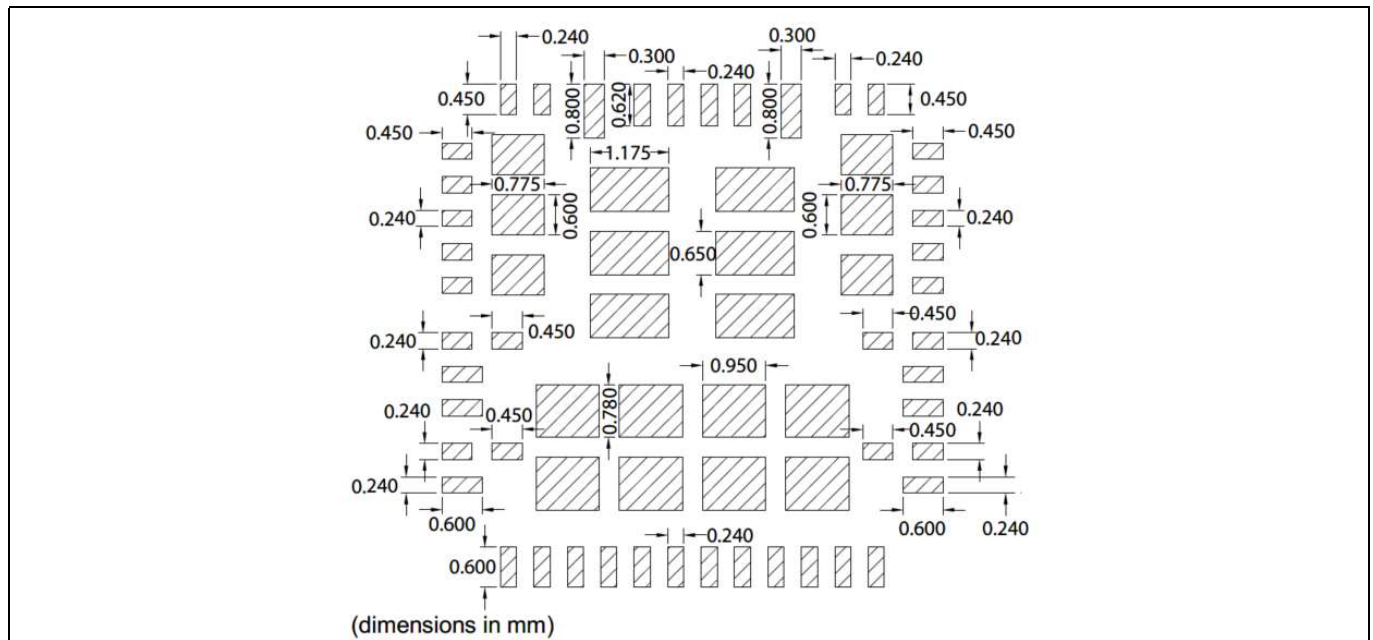


Figure 55 42-lead 7x7 stencil design_1

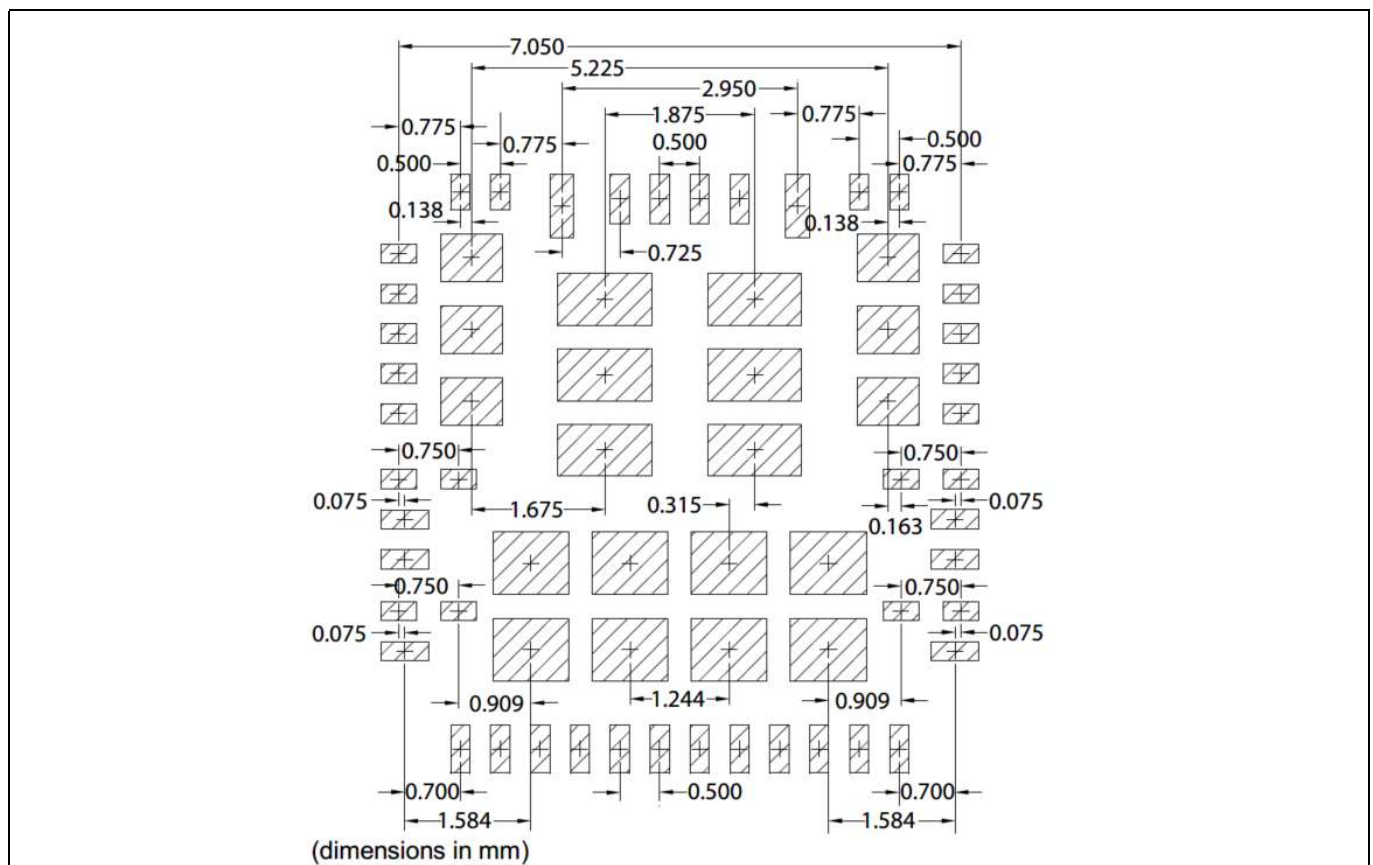


Figure 56 42-lead 7x7 stencil design_2

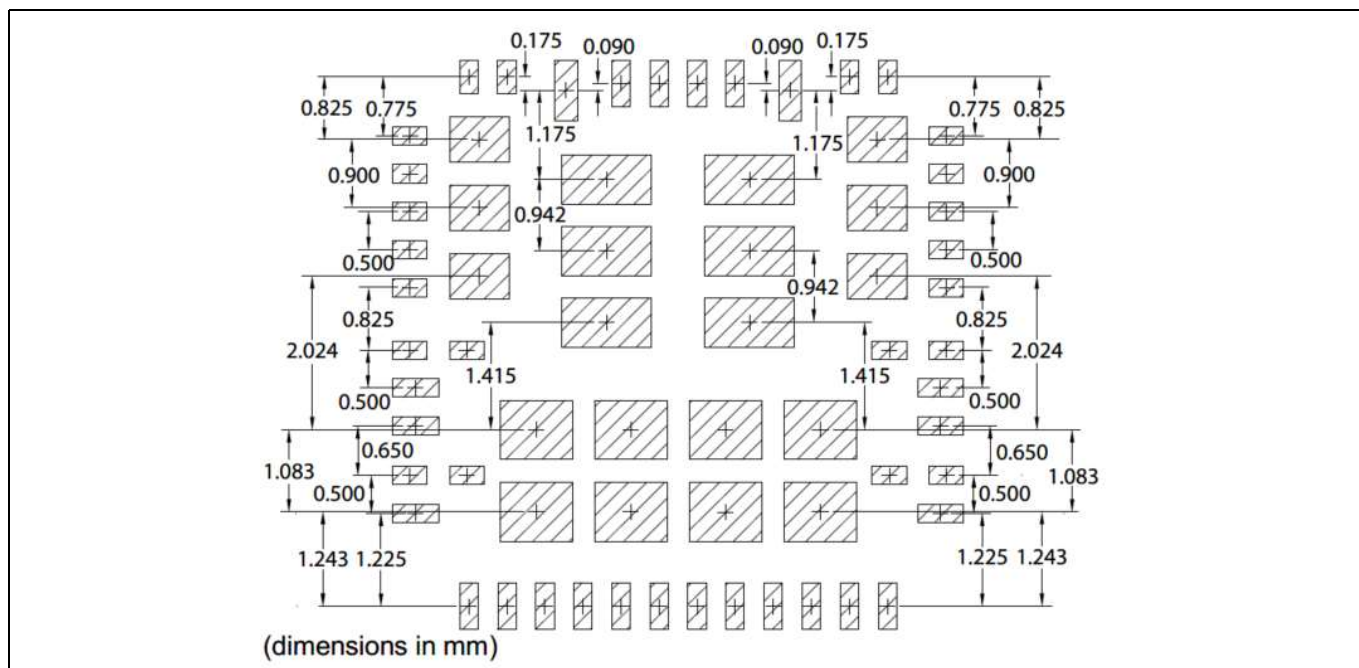


Figure 57 42-lead 7x7 stencil design_3

Note: This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses. All soldering conditions are necessary to ensure reliability. More details please refer to Application Note AN-1170 Audio Power Quad Flat No-Lead (PQFN) Board Mounting Application

Part marking

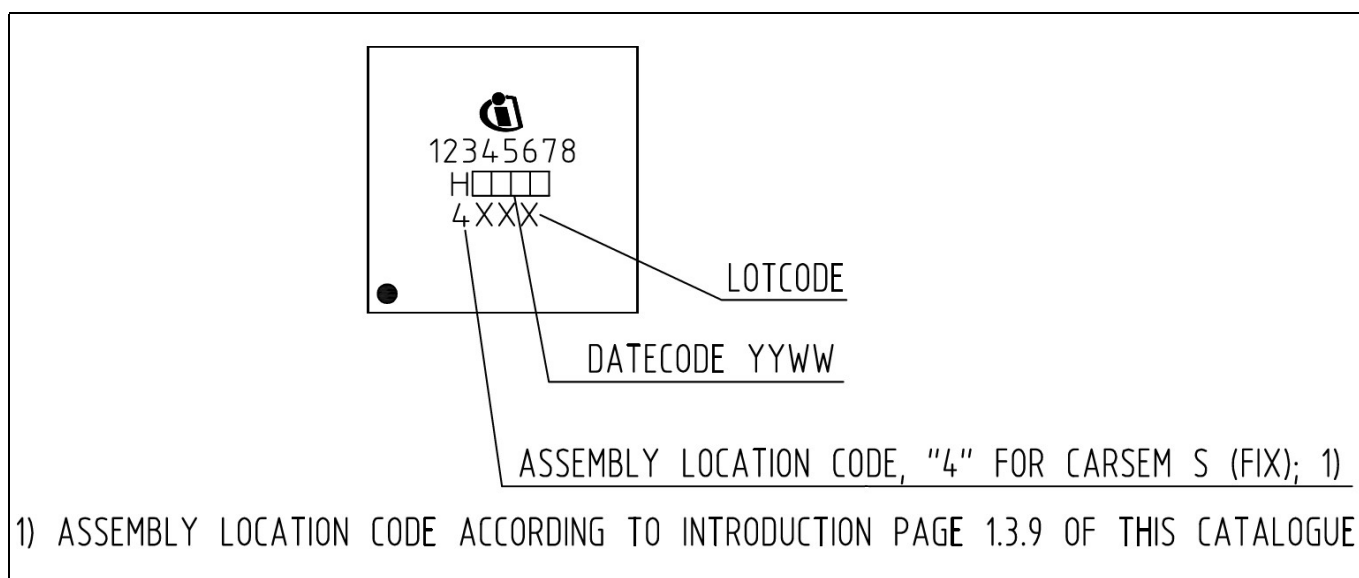


Figure 58 Part marking

MERUS™ Integrated Class D Amplifier

MA5332MS

Board mounting, part marking, ordering information

Ordering information

Base part number	Package type	Standard pack		Complete part number
		Form	Quantity	
MA5332MS	7x7mm PG- IQFN-42	Tape and Reel	3000	MA5332MS

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2021-09-21

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2025 Infineon Technologies AG.

All Rights Reserved.

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology delivery terms and conditions and prices please contact your nearest Infineon Technologies office (www.infineon.com).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.

Revision history

MA5332MS

Revision 2025-11-03, Rev. 2.2

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2021-09-25	Release of final version
2.1	2024-11-18	gm test condition: Ccomp = 1 nF -> 2 nF -Section 7 figure updates
2.2	2025-11-03	Added MERUS trademark

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Published by Infineon Technologies AG, 81726 Munich, Germany
Copyright (c) 2025 Infineon Technologies AG and its affiliates. All Rights Reserved.

Important notice

Products which may also include samples and may be comprised of hardware or software or both ("Product(s)") are sold or provided and delivered by Infineon Technologies AG and its affiliates ("Infineon") subject to the terms and conditions of the frame supply contract or other written agreement(s) executed by a customer and Infineon or, in the absence of the foregoing, the applicable Sales Conditions of Infineon. General terms and conditions of a customer or deviations from applicable Sales Conditions of Infineon shall only be binding for Infineon if and to the extent Infineon has given its express written consent.

For the avoidance of doubt, Infineon disclaims all warranties of non-infringement of third-party rights and implied warranties such as warranties of fitness for a specific use/purpose or merchantability.

Infineon shall not be responsible for any information with respect to samples, the application or customer's specific use of any Product or for any examples or typical values given in this document.

The data contained in this document is exclusively intended for technically qualified and skilled customer representatives. It is the responsibility of the customer to evaluate the suitability of the Product for the intended application and the customer's specific use and to verify all relevant technical data contained in this document in the intended application and the customer's specific use. The customer is responsible for properly designing, programming, and testing the functionality and safety of the intended application, as well as complying with any legal requirements related to its use.

Unless otherwise explicitly approved by Infineon, Products may not be used in any application where a failure of the Products or any consequences of the use thereof can reasonably be expected to result in personal injury. However, the foregoing shall not prevent the customer from using any Product in such fields of use that Infineon has explicitly designed and sold it for, provided that the overall responsibility for the application lies with the customer.

Infineon expressly reserves the right to use its content for commercial text and data mining (TDM) according to applicable laws, e.g. Section 44b of the German Copyright Act (UrhG).

If the Product includes security features: Because no computing device can be absolutely secure, and despite security measures implemented in the Product, Infineon does not guarantee that the Product will be free from intrusion, data theft or loss, or other breaches ("Security Breaches"), and Infineon shall have no liability arising out of any Security Breaches.

If this document includes or references software:

The software is owned by Infineon under the intellectual property laws and treaties of the United States, Germany, and other countries worldwide. All rights reserved. Therefore, you may use the software only as provided in the software license agreement accompanying the software. If no software license agreement applies, Infineon hereby grants you a personal, non-exclusive, non-transferable license (without the right to sublicense) under its intellectual property rights in the software (a) for software provided in source code form, to modify and reproduce the software solely for use with Infineon hardware products, only internally within your organization, and (b) to distribute the software in binary code form externally to end users, solely for use on Infineon hardware products. Any other use, reproduction, modification, translation, or compilation of the software is prohibited.

For further information on the Product, technology, delivery terms and conditions, and prices, please contact your nearest Infineon office or visit <https://www.infineon.com>.