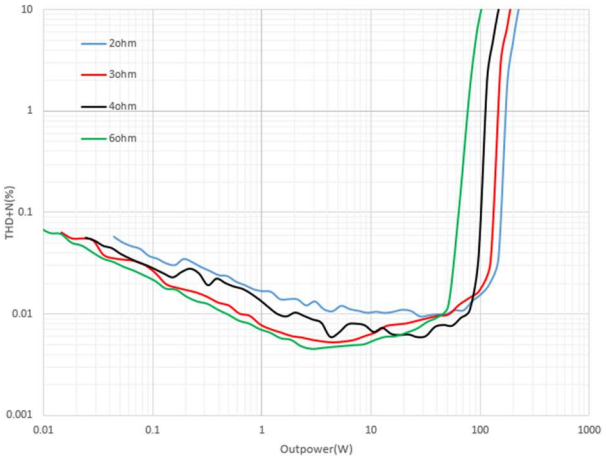
MERUS™ 2x200W Class-D Amplifier, Analog Input, with Integrated 16mΩ $R_{DS(ON)}$ Output Stage

Features

PG-IQFN-42

- Integrated output stage with 16mΩ typical $R_{DS(ON)}$
- 2 x 200W P_{OUT} in stereo mode (2Ω, THD=10%)
- 1 x 400W P_{OUT} in mono mode (4Ω, THD=10%)
- Supports both single and split supplies
    - Split supply operational range: ±17 – ±32V
    - Single supply Operational range: +32 – +64V
- 95% full load efficiency into 2Ω
- >70% idle mode efficiency
- Open-drain flag indicators for clipping and Fault conditions
- Multiple configuration: single-ended, BTL & PSE (Parallel Single Ended)
- Programmable power up delay timer (CSD)
    - Click and pop free startup and shutdown
- Integrated protection: OCP, OTP & UVLO
- Pin to pin compatible to MA53x2 family
- Available in QFN 7m x7m – 42 pin



Total Harmonic Distortion

Applications

- Multi-channel home theatre
- Studio monitor
- Active speaker
- Subwoofer
- Marine amplifiers
- Aftermarket car audio
- General-purpose audio power amplifier

Product validation

Qualified for standard applications according to the relevant tests of J-STD-020 and JESD47.

Product type	Package
MA5302MS	7x7mm PG- IQFN-42

Description

The MA5302MS provides output power that is equivalent to or greater than monolithic alternatives, while occupying 50% less space and requiring little or no heatsink. This is achieved through the integration of a 2-channel PWM controller, a high voltage gate driver, and 4 low RDS(ON) MOSFETs in a multi-chip module (MCM) solution. Similar to its predecessor, the IR43x2M, the MA5302MS includes standard Class D protection features that ensure reliable operation across various environmental conditions. With its small 7x7 mm PG-IQFN-42 package, the MA5302MS represents a powerful upgrade over the IR43x2M and other monolithic alternatives, delivering high power density and the benefits of heatsink-less operation.

Topology	Half-bridge / Full bridge
MA5302MS output power (THD+N=10%)	*220 W/ 2 Ω / 440 W in 4 Ω *195 W/ 3 Ω / 390 W in 6 Ω *150 W/ 4 Ω / 300 W in 8 Ω
Residual noise (AES-17, IHF-A)	*170 µVrms
THD+N (1kHz, 75W, 2 Ω, AES-17)	*0.01 %

*Typical applications

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1 Qualification Information

Qualification Level (1)		Standard (**2**) Qualified for standard applications according to the relevant tests of J-STD-020 and JESD47
Moisture Sensitivity Level (MSL) (3)		MSL3 (per IPC/JEDEC J-STD-020)
ESD	**Charge Device Model**	Class C2a (per JEDEC standard JS-002)
	Human Body Model	Class 1B (per JEDEC standard JS-001)
IC Latch-Up Test		Class I, Level A (per JESD78)
RoHS Compliant		Yes

Note:

1. *Qualification standards can be found at Infineon's web site http://www.infineon.com/*
2. *Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon Technologies sales representative for further information.*
3. *Higher MSL ratings may be available for the specific package types listed here. Please contact your Infineon Technologies sales representative for further information.*

2 Device Comparison Table

Table 1

Device Name	Description
MA5302MS	200W (2 Ω)*2 channel integrated analog input Class D audio Amplifier
MA5342MS	200W (8 Ω)*2 channel integrated analog input Class D audio Amplifier
MA5332MS	200W (4 Ω)*2 channel integrated analog input Class D audio Amplifier
IR4302M	130W (4 Ω)*2 channel integrated analog input Class D audio Amplifier
IR4322M	100W (2 Ω)*2 channel integrated analog input Class D audio Amplifier
IR4301M	160W (4 Ω) single-channel integrated analog input Class D audio Amplifier
IR4321M	135W (2 Ω) single-channel integrated analog input Class D audio Amplifier

3 Pin Configuration

3.1 Lead assignments

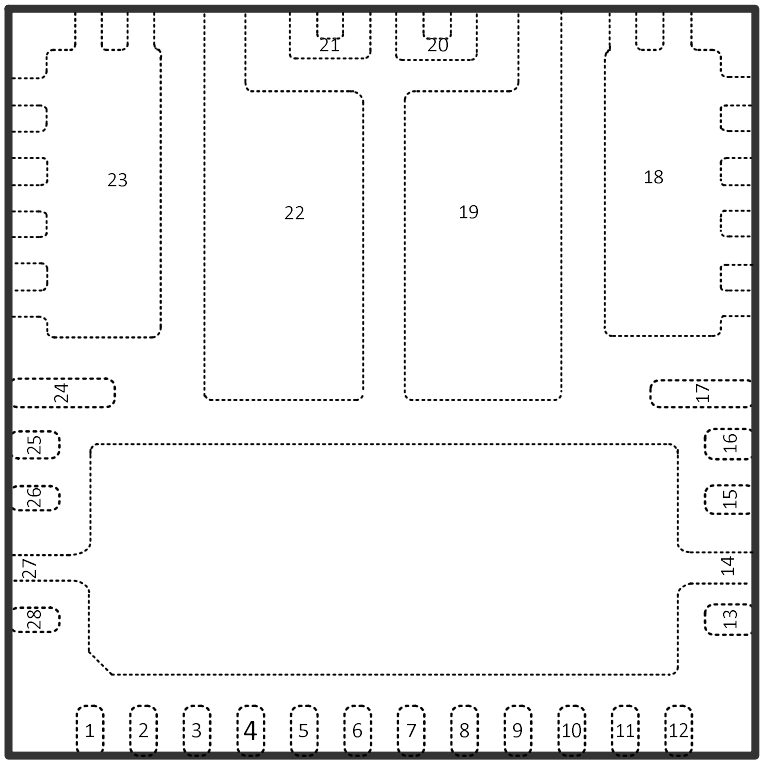

Figure 1 Lead assignments (top view)

3.2 Lead definitions

Pin #	Symbol	Description
1	CLIP	Clipping detection output, open drain, referenced to GND
2	COMP2	CH2 PWM comparator input
3	IN-2	CH2 Analog inverting input
4	IN+2	CH2 Analog non-inverting input
5	GND	GND for internal shunt zener diodes to VAA and VSS, a reference to FAULT and CLIP outputs.
6	VSS	Floating input negative supply
7	VAA	Floating input positive supply
8	IN+1	CH1 Analog non-inverting input
9	IN-1	CH1 Analog inverting input
10	COMP1	CH1 PWM comparator input
11	CSD	Shutdown timing capacitor / shutdown input
12	FAULT	Fault reporting output, open drain, referenced to GND
13	VCC	Low side supply
14	COM	Low side supply return, internally connected to pin 27
15	CSH1	CH1 High side over current sensing input, referenced to VS1

16	VB1	CH1 High side floating supply
17	VS1	CH1 PWM output, internally connected to pin 19
18	VP1	CH1 Positive power supply
19	VS1	CH1 PWM output
20	VN1	CH1 Negative power supply, connect to COM externally
21	VN2	CH2 Negative power supply, connect to COM externally
22	VS2	CH2 PWM output, internally connected to pin 24
23	VP2	CH2 Positive power supply
24	VS2	CH2 PWM output
25	VB2	CH2 High side floating supply
26	CSH2	CH2 High side over current sensing input, referenced to VS2
27	COM	Low side supply return, internally connected to pin 14
28	NC	

4 Specifications

4.1 Absolute maximum ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM=VN1=VN2; all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min	Max	Units
V_{Pn}	Positive power supply rail voltage, n=1-2	-	80	
V_{Bn}	High side floating supply voltage	-0.3	95	
V_{Sn}	High side floating supply voltage(2), n=1-2	V_{Bn} -15	V_{Bn} +0.3	
V_{CSHn}	CSH pin input voltage, n=1-2	V_{Sn} -0.3	V_{Bn} +0.3	
V_{CC}	Low side supply voltage(2)	-0.3	15	
V_{AA}	Floating input positive supply voltage(2)	-0.3	90	
V_{SS}	Floating input negative supply voltage(2)	-1 (See I_{SSZ})	GND +0.3	
V_{IN+n}	Floating input supply ground voltage , n=1-2	V_{SS} -0.3	V_{AA} +0.3	
I_{INn}	Input current between IN- and IN+ pins(1), n=1-2	-	±3	mA
V_{CSD}	CSD pin input voltage	V_{SS} -0.3	V_{AA} +0.3	
V_{COMPn}	COMP pin input voltage, n=1-2	V_{SS} -0.3	V_{AA} +0.3	V
V_{CLIP}	CLIP pin input voltage	GND -0.3	V_{AA} +0.3	
I_{CLIP}	CLIP pin sinking current	-	5	mA
V_{FAULT}	FAULT pin input voltage	GND -0.3	V_{AA} +0.3	V
I_{FAULT}	FAULT pin sinking current	-	5	
I_{AAZ}	Floating input supply zener clamp current(2)	-	20	
I_{SSZ}	Floating input negative supply zener clamp current(2)	-	20	mA
I_{CCZ}	Low side supply zener clamp current(2)	-	20	
I_{BSZn}	Floating supply zener clamp current(2), n=1-2	-	20	
dV_{Sn}/dt	Allowable Vs voltage slew rate, n=1-2	-	50	V/ns
dV_{SS}/dt	Allowable Vss voltage slew rate(3)	-	50	V/ms
$Id_{@\ 25°C}$	Continuous output current, from VPn to VSn, VSn to VNn, V_{CC}=10V, V_{Bn}-V_{Sn}=10V	-	38	
$Id_{@\ 100°C}$	Continuous output current, from VPn to VSn, VSn to VNn, V_{CC}=10V, V_{Bn}-V_{Sn}=10V	-	24	A
I_{DM}	Pulsed output current, from VPn to VSn, VSn to VNn, V_{CC}=10V, V_{Bn}-V_{Sn}=10V(5)	-	152	
Pd	Power dissipation(4)@ T_C = 25°C	-	25	W
Rth_{JC}	Thermal resistance, junction to case(4)	-	5	°C/W
T_J	Junction temperature	-	150	°C

T_S	Storage Temperature	-55	150	
T_L	Lead temperature (Soldering, 10 seconds)	-	300	

Note:

1. *IN- and IN+ contain clamping diodes between the two pins.*
2. *V_{AA} -V_{SS}, Vcc-COM and VBn-VSn contain internal shunt zener diodes. Note that the voltage ratings of these can be limited by the clamping current.*
3. *For the rising and falling edges of step signal of 10V. Vss=15V to 100V.*
4. *Per MOSFET.*
5. *Repetitive rating, pulse width limited by maximum junction temperature.*

4.2 Recommended operating conditions

For proper operation, the device should be used within the recommended conditions below. The Vss and Vsn offset ratings are tested with supplies biased at COM=VN1=VN2, V_{AA}-V_{SS}=9.6V, V_{CC}=12V and V_{Bn}-V_{Sn}=12V. All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead.

Symbol	Definition		Min	Max	Units
V_{Pn}	Positive power supply voltage, n=1-2, without heatsink	MA5302MS	-	64	V
	Positive power supply voltage, n=1-2, with heatsink	MA5302MS	-	64	
V_{Bn}	High side floating supply absolute voltage, n=1-2		V_{Sn} +10	V_{Sn} +14	
V_{Sn}	High side floating supply offset voltage, n=1-2	MA5302MS	(6)	80	
V_{AA}	Floating input positive supply voltage(7)		V_{SS} +9.0	V_{SS} + 9.8	
V_{SS}	Floating input negative supply voltage(7)	MA5302MS	0	80	
I_{AAZ}	Floating input supply zener clamp current(7)		1	15	mA
I_{SSZ}	Floating input negative supply zener clamp current(7)		1	15	
V_{CC}	Low side fixed supply voltage		10	15	V
V_{IC}	IN- and IN+ pins common mode input voltage		V_{SS} + 2	V_{AA} - 2	
V_{IN-n}	Inverting input voltage, n=1-2		V_{IN+} -0.5	V_{IN+} +0.5	
V_{CSD}	CSD pin input voltage		V_{SS}	V_{AA}	
V_{COMPn}	COMP pin input voltage, n=1-2		V_{SS}	V_{AA}	
C_{COMPn}	COMP pin phase compensation capacitor to GND , n=1-2		1	-	nF
V_{CSHn}	CSH pin input voltage, n=1-2		V_{Sn}	V_{Bn}	V
f_{SW}	Switching frequency		-	500	kHz
T_J	Junction temperature(8)		-40	85	°C

Note:

6. *Logic operational for Vs equal to –5V to +80V. Logic state held for Vs equal to –5V to –V_{BS}.*
7. *GND input voltage is limited by I_{AAZ} and I_{SSZ}.*
8. *Long term average temperature. The device is operational up to T_{J_IC} 100 ℃.*

4.3 Electrical characteristics

Unless otherwise specified, the following apply:

- V_{CC},V_{BS}= 12 V
- V_{SS}=V_{S1}=V_{S2}=V_{N1}=V_{N2}=COM=0V
- V_{AA}=9.6V
- T_A=25°C

Table 2 Electrical characteristics

Symbol	Definition	Min	Typ	Max	Units	Test conditions
Low-side supply						
UV_{CC+}	Vcc supply UVLO positive threshold	8.4	8.9	9.4	V	
UV_{CC-}	Vcc supply UVLO negative threshold	8.2	8.7	9.2	V	
UV_{CCHYS}	UV_{CC} hysteresis	-	0.2	-	V	
I_{QCC}	Low side quiescent current	-	-	3	mA	
I_{CC}	Low side supply current	-	10	-	mA	f=400kHz
V_{CLAMPL}n	Low side zener diode clamp voltage, n=1-2	14.7	15.3	16.2	V	I_{CC}=5mA
High-side floating supply						
UV_{BS+n}	High side well UVLO positive threshold, n=1-2	8.0	8.5	9.0	V	
UV_{BS-n}	High side well UVLO negative threshold, n=1-2	7.8	8.3	8.8	V	
UV_{BSHYSn}	UV_{BS} hysteresis, n=1-2	-	0.2	-	V	
I_{QBSn}	High side quiescent current, n=1-2	-	-	2.4	mA	
$I_{QBSn\_OFF-CSH}$	High side quiescent current, with CSH pin open n=1-2	350	500	650	uA	
$V_{CLAMPHn}$	High side zener diode clamp voltage, n=1-2	14.7	15.3	16.2	V	I_{BS}=5mA
Floating input supply						
UV_{AA+}	VA+, VA- floating supply UVLO positive threshold from V_{SS}	8.2	8.7	9.2	V	V_{SS} =0V, GND pin floating
UV_{AA-}	VA+, VA- floating supply UVLO negative threshold from V_{SS}	7.7	8.2	8.7	V	V_{SS} =0V, GND pin floating
UV_{AAHYS}	UV_{AA} hysteresis	-	0.5	-	V	V_{SS} =0V, GND pin floating
I_{QAA0}	Floating Input positive quiescent supply current	-	1.5	3	mA	V_{AA}=9.6V, V_{SS} =0V, V_{CSD} =VSS
I_{QAA1}	Floating Input positive quiescent supply current	-	4	6	mA	V_{AA}=9.6V, V_{SS} =0V, V_{CSD} =VAA

I_{QAA2}	Floating Input positive quiescent supply current	-	5	7.5	mA	V_{AA}=9.6V, V_{SS} =0V, V_{CSD} =GND
I_{LKM}	Floating input side to Low side leakage current	-	-	50	µA	V_{AA}=V_{SS}=V_{GND}= 100V
$V_{CLAMPM+}$	V_{AA} floating supply zener diode clamp voltage, positive, with respect to GND	4.9	5.1	5.4	V	I_{AA}=5mA, I_{SS}=5mA, V_{GND}=0V, V_{CSD} =VSS
$V_{CLAMPM-}$	V_{SS} floating supply zener diode clamp voltage, negative, with respect to GND	-5.4	-5.1	-4.9	V	I_{AA}=5mA, I_{SS}=5mA, V_{GND}=0V, V_{CSD} =VSS
Audio input (V_{GND}=0, V_{AA}=4.8V, V_{SS}=-4.8V)						
V_{OSn}	Input offset voltage, n=1-2	-18	0	18	mV	
I_{BINn}	Input bias current, n=1-2	-	-	40	nA	
GBWn	Small signal bandwidth in OTA, n=1-2	-	9	-	MHz	C_{COMP}=2nF, Rf=0
g_{mn}	OTA transconductance, n=1-2	-	10	-	mS	V_{IN+}=0V, V_{IN-} =10mV
G_{Vn}	OTA gain, n=1-2	50	-	-	dB	
V_{Nrmsn}	CHn OTA noise voltage, n=1-2	-	200	330	mVrms	
PWM						
Vth_{PWM}	PWM comparator threshold in COMP	-	(V_{AA} - V_{SS})/2	-	V	
f_{OTAn}	COMP pin star-up local oscillation frequency, n=1-2	0.7	1.0	1.5	MHz	V_{CSD} =GND
Ton_n	COMP to VS rising edge propagation delay, n=1-2	-	370	-	ns	
Toff_n	COMP to VS trailing edge propagation delay, n=1-2	-	320	-	ns	
DTn	Deadtime: Low-side turn-off to High-side turn-on (DT_{LO-HO}) & High-side turn-off to Low-side turn-on (DT_{HO-LO}) , n=1-2	-	50	-	ns	VP=30V, VN=-30V,
Power MOSFET (FET1, FET2, FET3, FET4) (MA5302MS)						
At Tj=25°C, unless otherwise specified						
$V_{(BR)DSS}$[8]	Drain-to-Source breakdown voltage	80	-	-	V	V_{GS}=0V, I_D=1mA
$R_{DS(ON)}$	FET on resistance	-	16	19	mΩ	I_D=3.3A, V_{GS}=10V
Qg	Total gate charge	-	15.8		nC	V_{GS}=10V
I_{LK0}	VP leakage current, VS=VN	-	-	20	µA	V_P=80V[8], V_{CSD} =VSS

Protection

I_{OCPn}	Over current detection Positive threshold, n=1-2[8]	-	60	-	A	
I_{OCNn}	Over current detection Negative threshold, n=1-2[9]	-	-60	-	A	
Vth1	CSD pin shutdown release threshold	0.62xV_{AA}	0.70xV_{AA}	0.78xV_{AA}	V	
Vth2	CSD pin self-reset threshold	0.26xV_{AA}	0.30xV_{AA}	0.34xV_{AA}	V	
I_{CSD+}	CSD pin discharge current	70	100	130	µA	V_{CSD} = V_{SS} +4.8V
I_{CSD-}	CSD pin charge current	70	100	130	µA	V_{CSD} = V_{SS} +4.8V
t_{SDn}	Shutdown propagation delay from V_S < Vth1 to Shutdown, n=1-2	-	-	250	ns	COMP = V_{SS}
t_{OCPn}	CHn propagation delay time from I_{On} > I_{OCPn} to Shutdown, n=1-2	-	-	500	ns	COMP = V_{SS}
t_{OCNn}	CHn propagation delay time from I_{On} < I_{OCNn} to Shutdown, n=1-2	-	-	500	ns	COMP = V_{SS}
$Vth+_{CLIP}$	Clip detection positive threshold in COMP	0.85xV_{AA}	0.90xV_{AA}	0.95xV_{AA}	V	
$Vth-_{CLIP}$	Clip detection negative threshold in COMP	0.05xV_{AA}	0.10xV_{AA}	0.15xV_{AA}	V	
t_{CLIP}	Clipping detection propagation delay	-	40	-	ns	
$t_{CLIPmin}$	Clipping detection minimum output duration	-	3	-	us	
T_{SD}	Over-temperature shutdown threshold in controller IC	100	-	-	°C	
T_{SDHYS}	Over-temperature shutdown threshold hysteresis	-	7	-	°C	

4.4 Audio characteristics (SE)

Table 3

Parameter	Test conditions	Typ	Unit
Po Power output per channel[10]	R_L= 6Ω, 10%THD+N, V_{bus} = ± 32 V	100	W
	R_L= 4Ω, 10%THD+N, V_{bus} = ± 32 V	150	
	R_L= 3Ω, 10%THD+N, V_{bus} = ± 32V	198	
	R_L= 2Ω, 10%THD+N, V_{bus} = ± 28.5 V	220	
	R_L= 6Ω, 1%THD+N, V_{bus} = ± 32 V	90	
	R_L= 4Ω, 1%THD+N, V_{bus} = ± 32 V	110	
	R_L= 3Ω, 1%THD+N, V_{bus} = ± 32 V	147	
	R_L= 2Ω, 1%THD+N, V_{bus} = ± 28.5V	175	
Residual noise(AES-17, IHF-A, typical)	EVAL_MA5302MS_200Wx2, V_{bus} = ± 32 V ,R_L= 4Ω	170	uV
Idling supply current	EVAL_MA5302MS_200Wx2, V_{bus} = ± 32 V ,R_L= 4Ω	+45	mA
		-75	
Efficiency[11]	EVAL_MA5302MS_200Wx2, V_{bus} = ± 28.5 V ,R_L= 2Ω	94	%

Note:

9. V_p changes over temperature at a rate of 50mV/K compared to Tj=25°C.
10. Over-current protection threshold measured under Tj=25°C condition.
11. Tested with heatsink (digikey part number: V8818V)
12. Class D stage only

4.5 Audio characteristics (BTL)

Table 4

Parameter	Test conditions	Typ	Unit
Po Power output per channel[9]	RL= 8Ω, 10%THD+N, V_{bus} = ± 32 V	300	W
	RL= 6Ω, 10%THD+N, V_{bus} = ± 32 V	396	
	RL= 4Ω, 10%THD+N, V_{bus} = ± 28.5 V	440	
	RL= 8Ω, 1%THD+N, V_{bus} = ± 32 V	220	
	RL= 6Ω, 1%THD+N, V_{bus} = ± 32 V	294	
	RL= 4Ω, 1%THD+N, V_{bus} = ± 28.5V	350	
Residual noise(AES-17, IHF-A, typical)	EVAL_MA5302MS_200Wx2, V_{bus} = ± 32 V ,RL= 4Ω	250	uV
Idling supply current	EVAL_MA5302MS_200Wx2, V_{bus} = ± 32 V ,RL= 8Ω	+45	mA
		-75	
Efficiency[10]	EVAL_MA5302MS_200Wx2, V_{bus} = ± 28.5 V ,RL= 4Ω	94	%

4.6 Audio characteristics (PSE)

Table 5

Parameter	Test conditions	Typ	Unit
Po Power output per channel[9]	RL= 1Ω, 10%THD+N, V_{bus} = ± 28.5 V	440	W
	RL= 1Ω, 1%THD+N, V_{bus} = ± 28.5V	350	
Residual noise(AES-17, IHF-A, typical)	EVAL_MA5302MS_200Wx2, V_{bus} = ± 28.5 V ,RL= 1Ω	115	uV
Idling supply current	EVAL_MA5302MS_200Wx2, V_{bus} = ± 28.5 V ,RL= 1Ω	+45	mA
		-75	
Efficiency[10]	EVAL_MA5302MS_200Wx2, V_{bus} = ± 28.5 V ,RL= 1Ω	94	%

4.7 Typical Audio characteristics (SE)

Test conditions:

All Measurements taken at Sine wave frequency= 1 kHz, AES17+ AUX-0025measurementfilters.

V_{bus} = ± 32 V, Load impedance = 6 Ω, F_{PWM} = 400 kHz

V_{bus} = ± 32 V, Load impedance = 4 Ω, F_{PWM} = 400 kHz

V_{bus} = ± 32 V, Load impedance = 3 Ω, F_{PWM} = 400 kHz

V_{bus} = ± 28.5 V, Load impedance = 2 Ω, F_{PWM} = 400 kHz

4.7.1 Power vs. THD+N

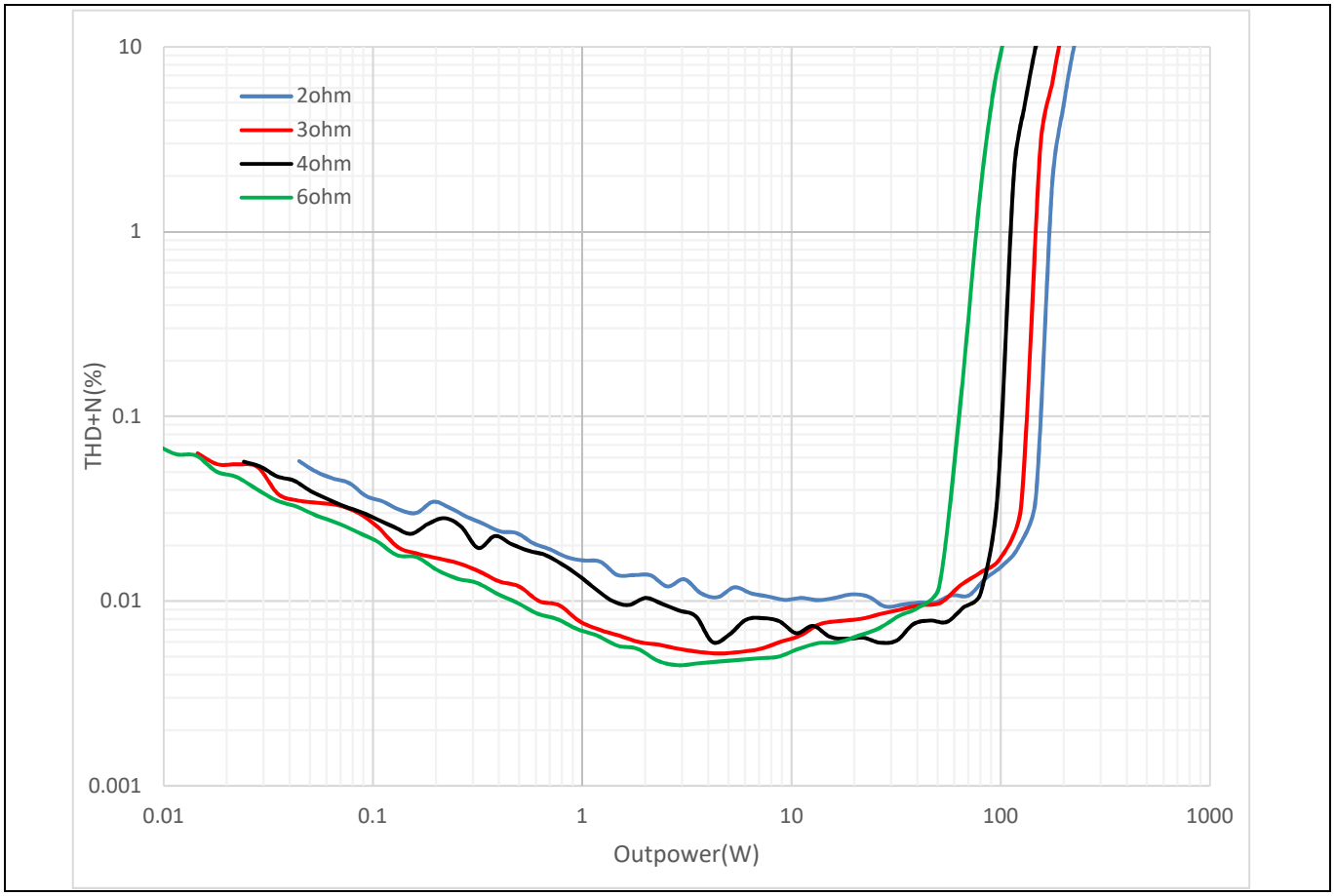

Figure 2 Power vs. THD+N

4.7.2 Frequency vs. THD+N

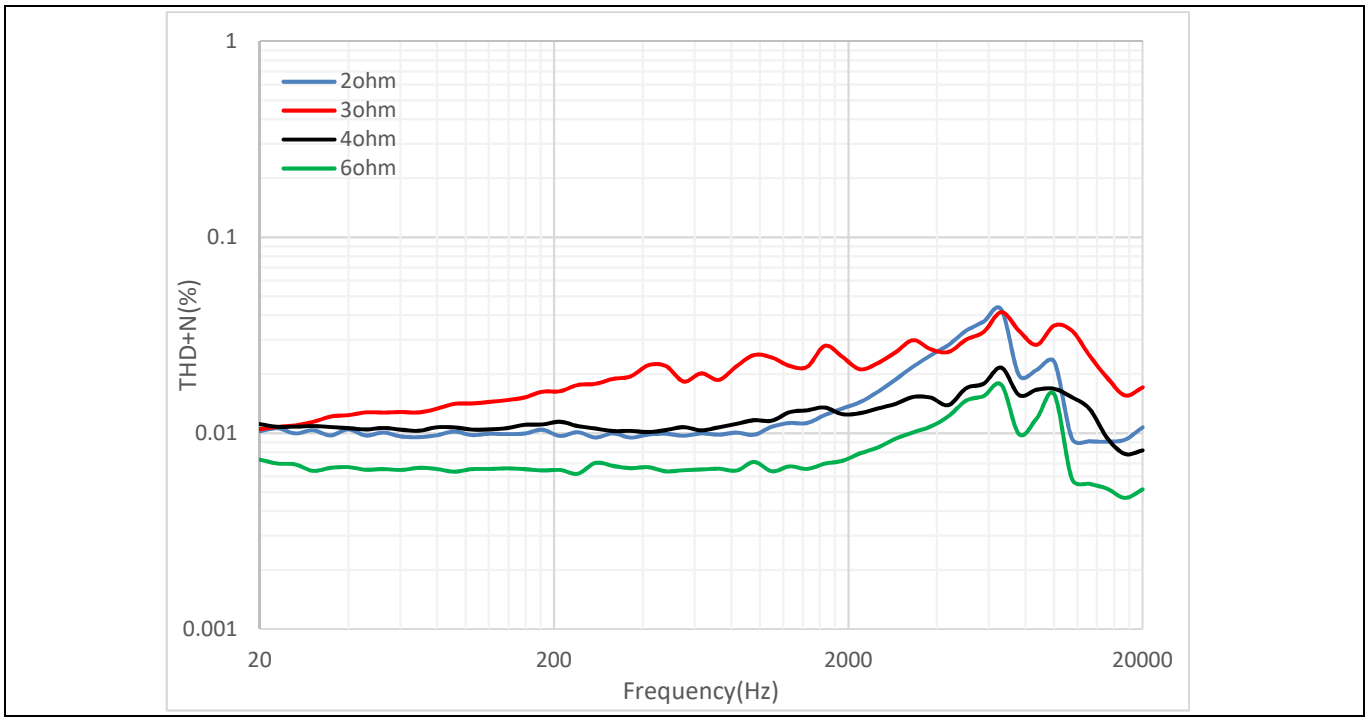

Figure 3 Frequency vs. THD+N @1W

4.7.3 Frequency response

Test conditions:

Output power = 1 W, fixed LPF 10uH+1uF

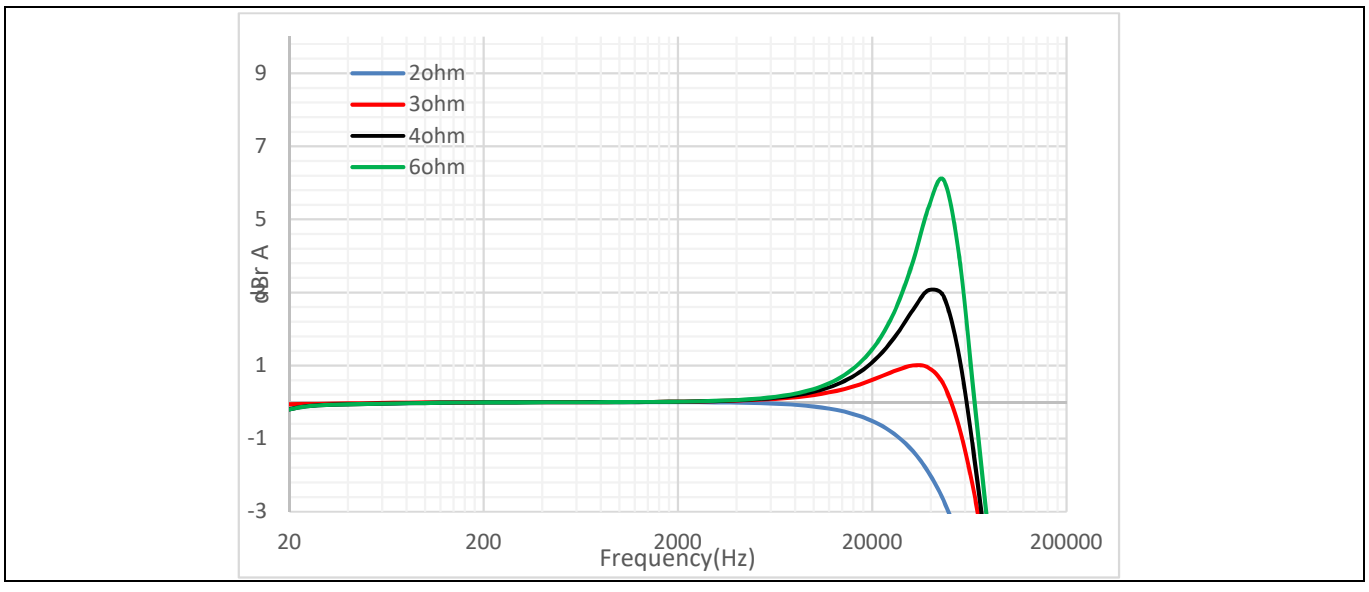

Figure 4 Frequency response

4.7.4 Noise floor

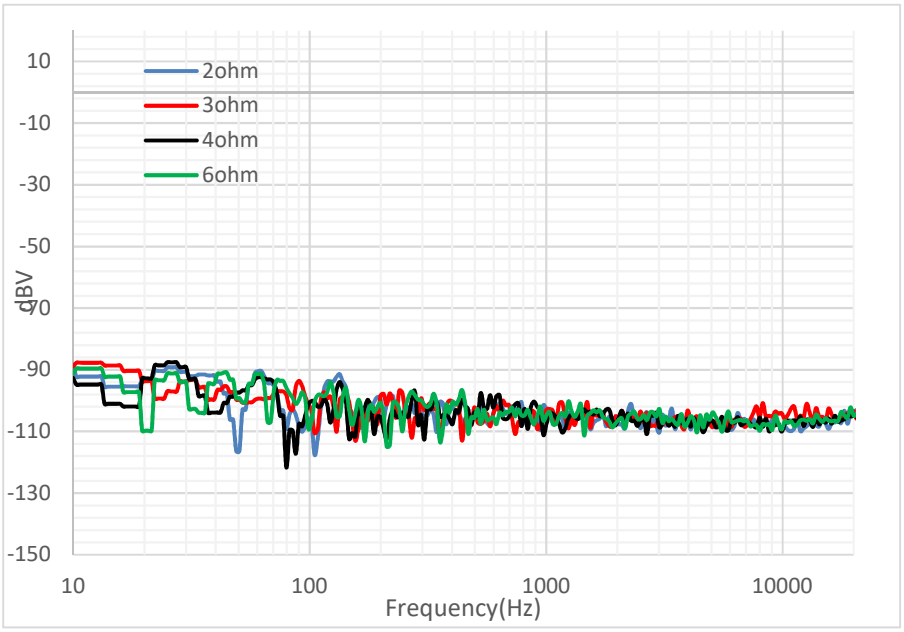

Figure 5 Noise floor

4.7.5 Efficiency

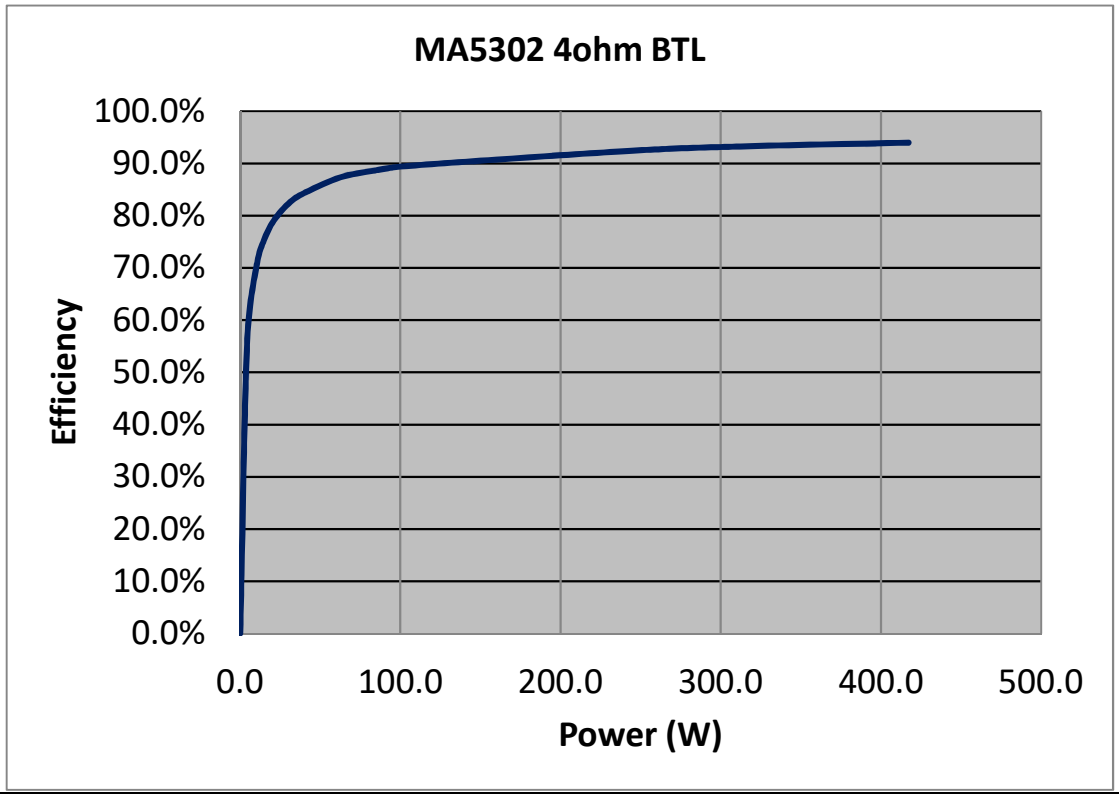

Figure 6 Efficiency 4 Ω BTL

4.8 Typical Audio characteristics (BTL)

Test conditions:

All Measurements taken at Sine wave frequency= 1 kHz, AES17+ AUX-0025 measurement filters.

V_{bus} = ± 32 V, Load impedance = 8 Ω, F_{PWM} = 400 kHz

V_{bus} = ± 32 V, Load impedance = 6 Ω, F_{PWM} = 400 kHz

V_{bus} = ± 28.5 V, Load impedance = 4 Ω, F_{PWM} = 400 kHz

4.8.1 Power vs. THD+N

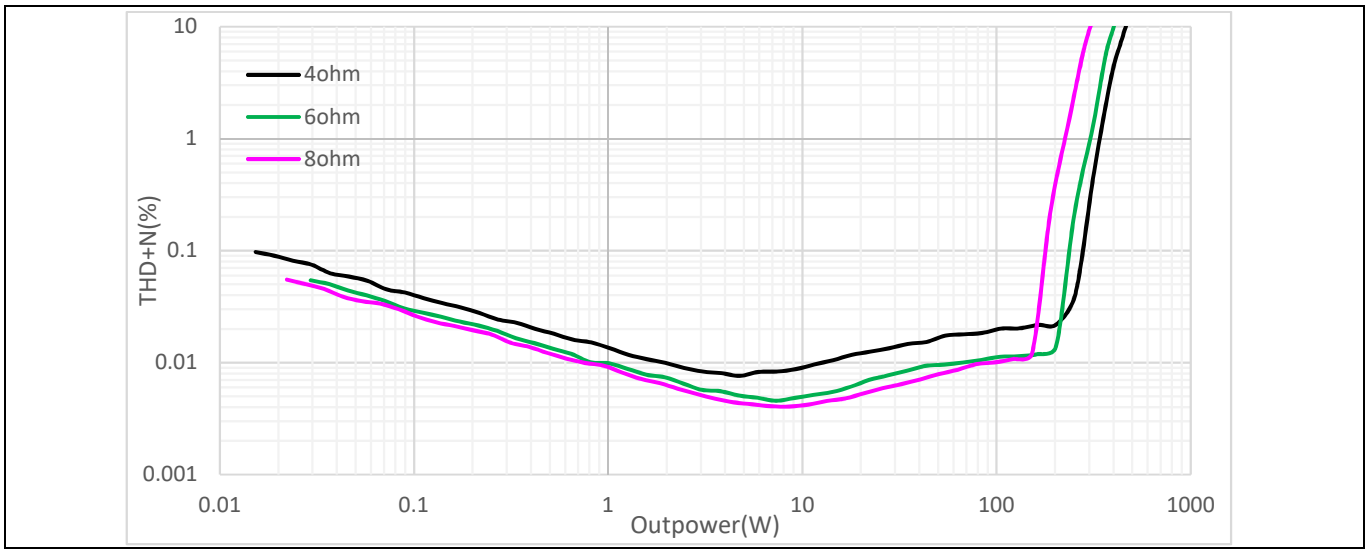

Figure 7 Power vs. THD+N

4.8.2 Frequency vs. THD+N

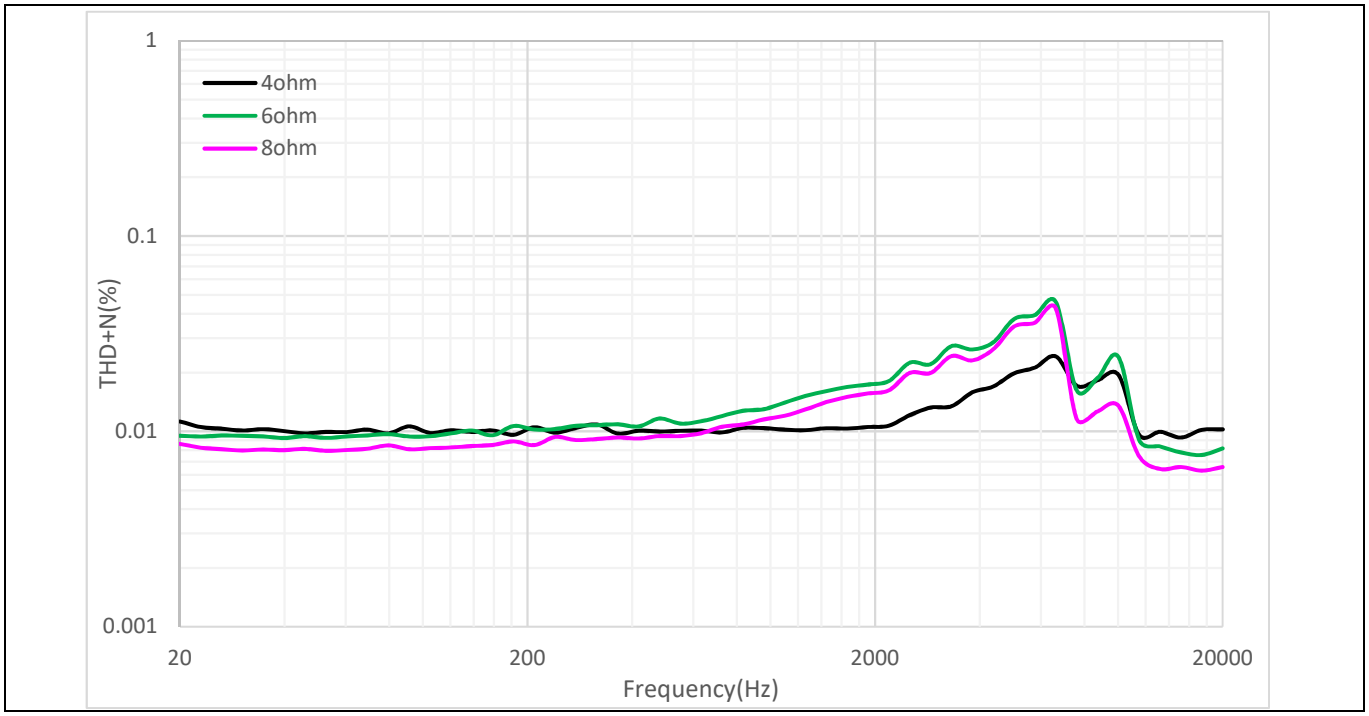

Figure 8 Frequency vs. THD+N @1W

4.8.3 Frequency response

Test conditions:

Output power = 1 W, fixed LPF 10uH+1uF

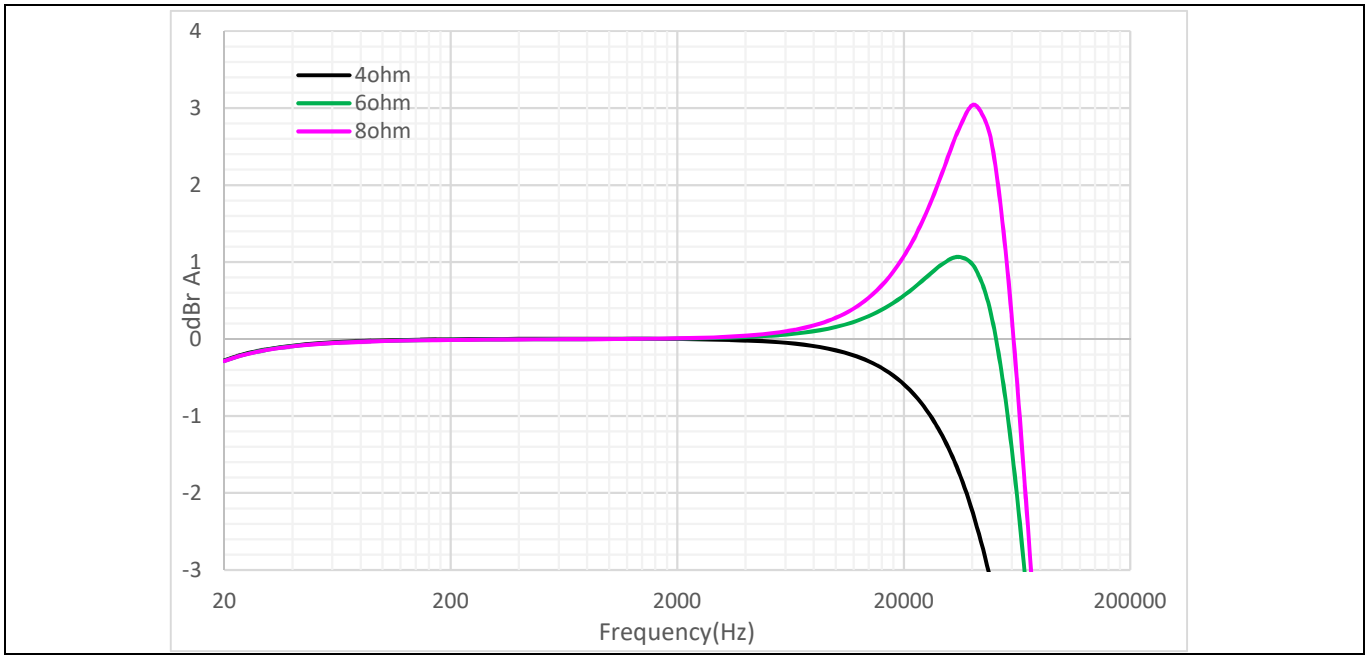

Figure 9 Frequency response

4.8.4 Noise floor

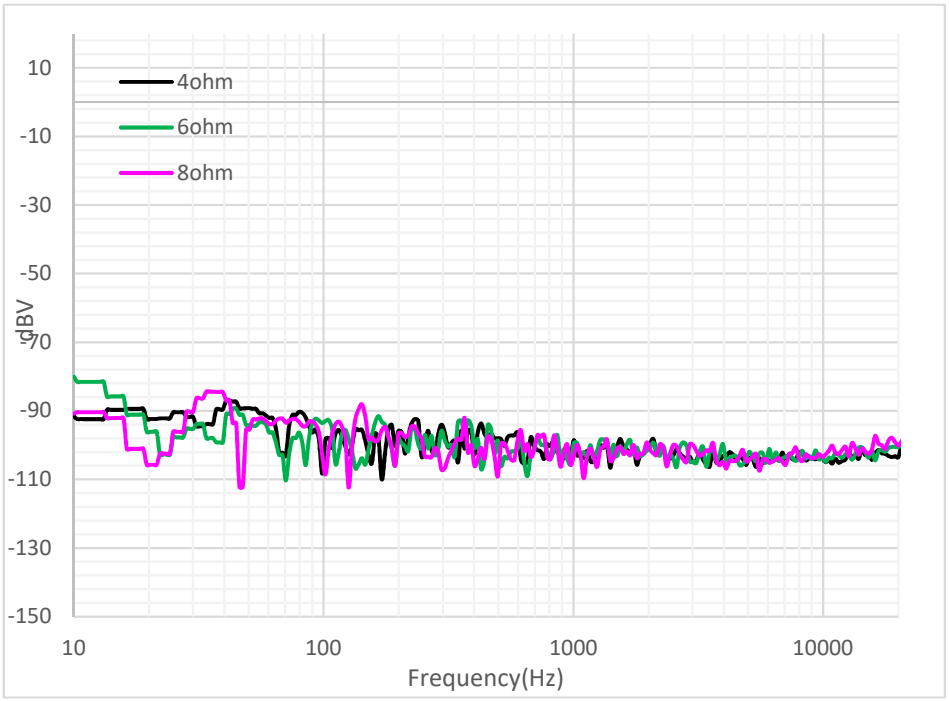

Figure 10 Noise floor

4.9 Typical Audio characteristics (PSE)

Test conditions:

All Measurements taken at Sine wave frequency= 1 kHz, AES17+ AUX-0025 measurement filters.

V_{bus} = ± 28.5 V, Load impedance = 1 Ω, F_{PWM} = 400 kHz

4.9.1 Power vs. THD+N

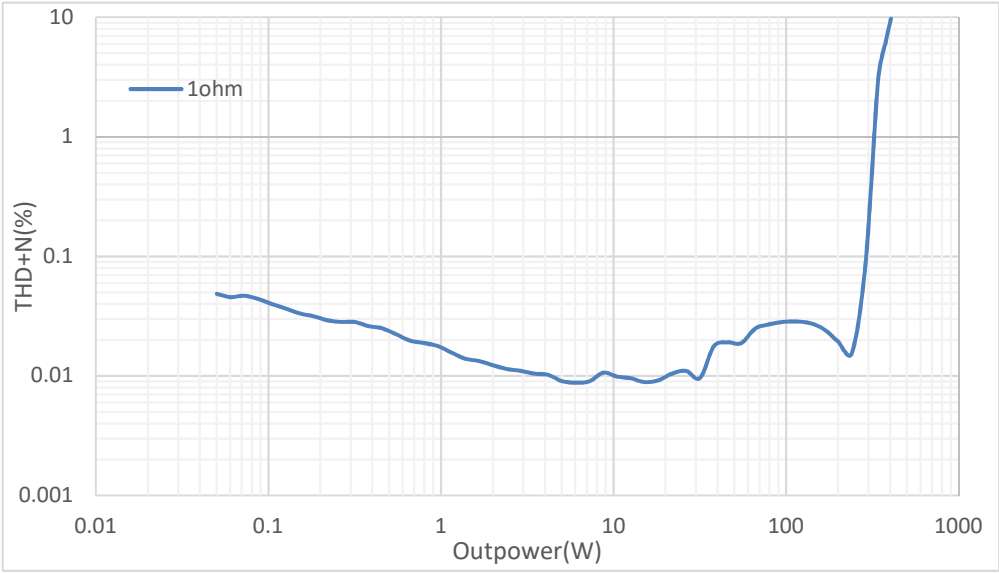

Figure 11 Power vs. THD+N

4.9.2 Frequency vs. THD+N

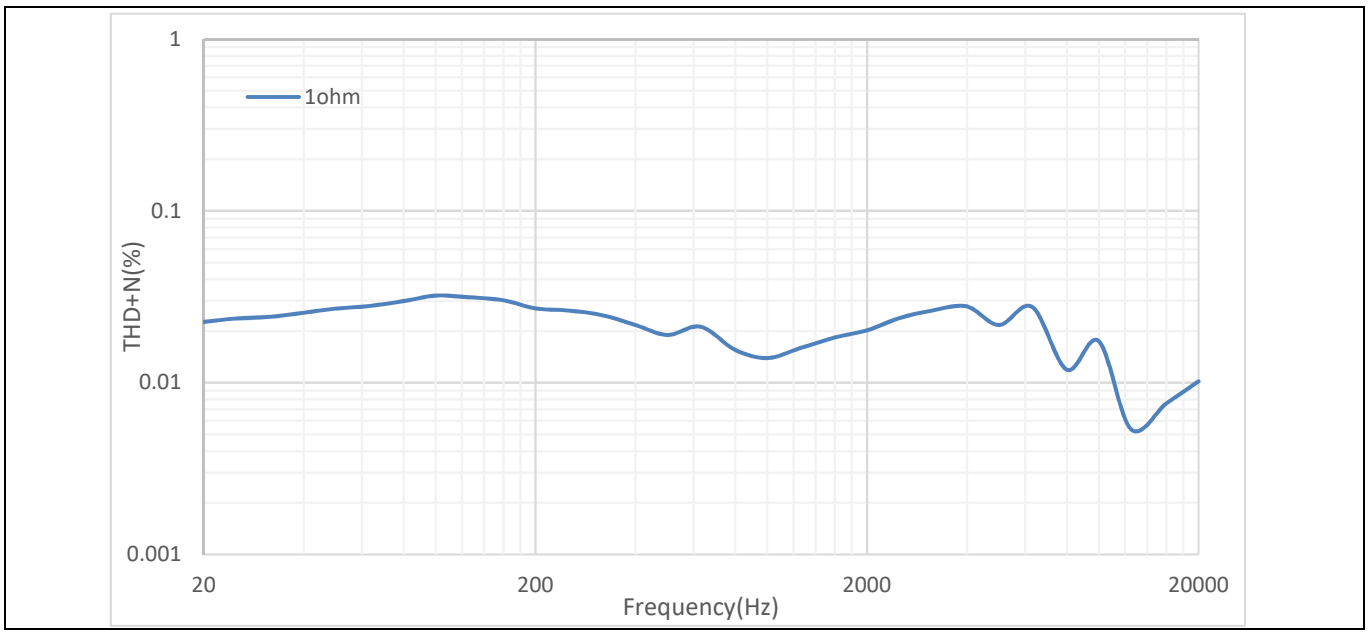

Figure 12 Frequency vs. THD+N @1W

4.9.3 Frequency response

Test conditions:

Output power = 1 W, fixed LPF 10uH+1.0uF

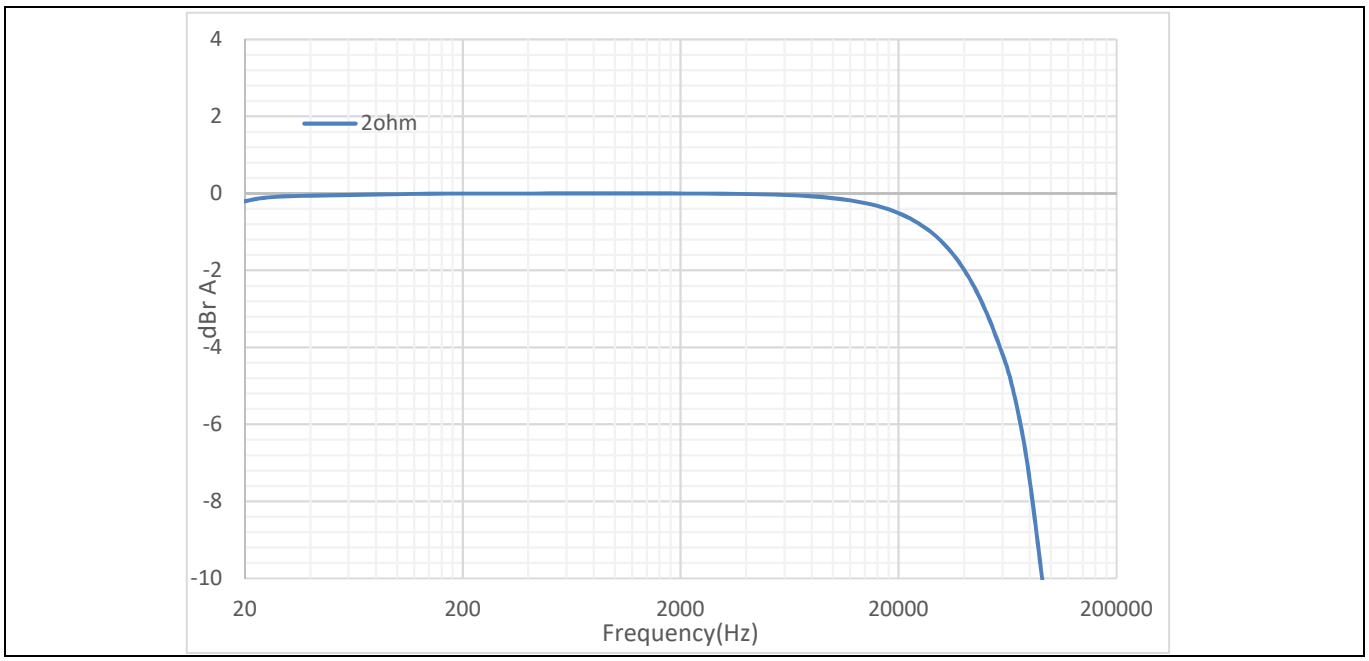

Figure 13 Frequency response

4.9.4 Noise floor

Test conditions:

No input signal

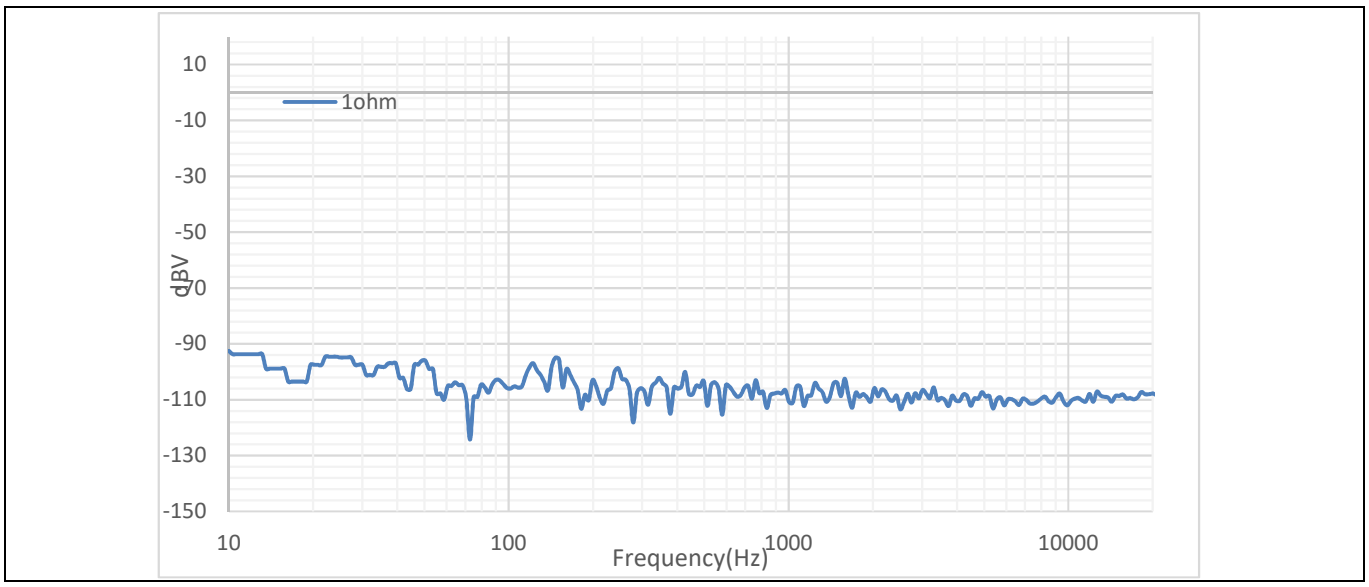

Figure 14 Noise floor

5 Thermal information

MA5302MS benefits from a unique co-packaging technique and superior MOSFET technology, resulting in best-in-class thermal performance and peak power duration. It is capable of delivering 100W x 2 at 2Ω even without requiring a heatsink

5.1 Maximum Wrms Duration Thermal Information

Test conditions:

All Measurements are taken at Sinewave frequency= 1 kHz, AES17+ AUX-0025 measurement filters. Input signal = 1 kHz, F_{PWM} = 400 kHz.

Tests are based on EVAL_MA5302MS_200Wx2 board when both channels are driven

Table 6 Peak power with heatsink

Load (Ω)	±V_{bus} (V)	10 percent THD+N power (W)	Duration
4	32	150	More than 1 minute no thermal shutdown
3	32	195	
2	28.5	220	

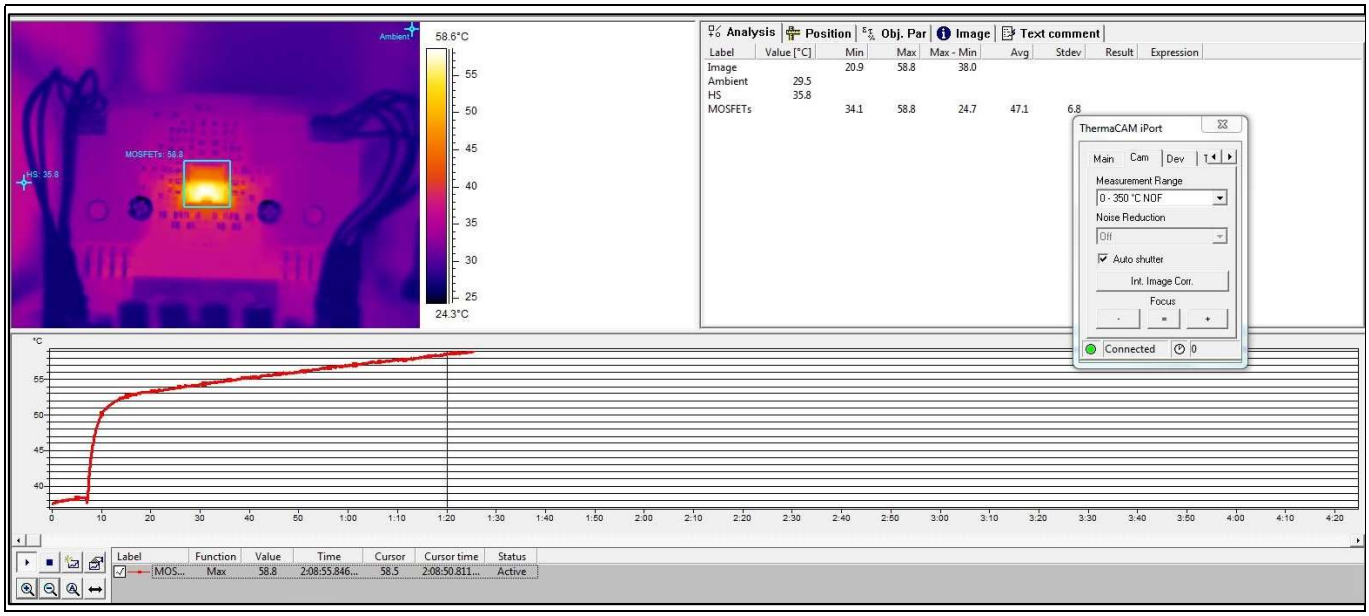

Figure 15 Peak power P_{out} = 151 W with 4 Ω load ±32 V

Note: Maximum temperature 58°C at 1 minute.

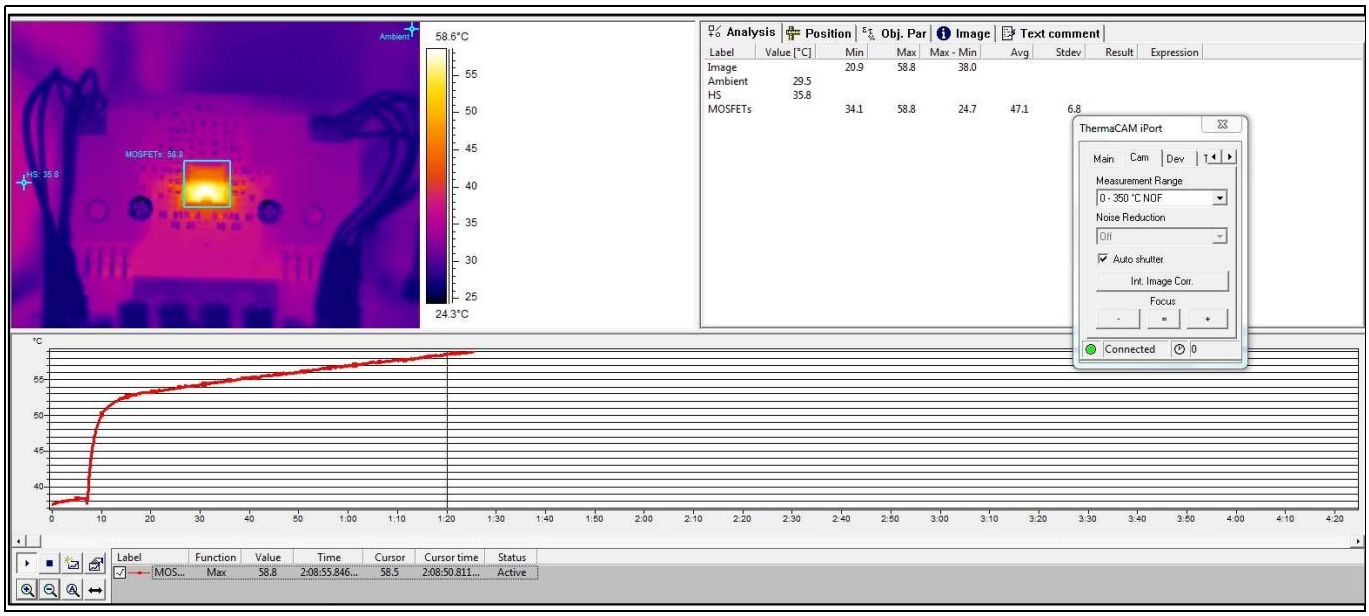

Figure 16 Peak power P_{out} = 198 W with 3 Ω load ±32 V

Note: Maximum temperature 79°C at 1 minute.

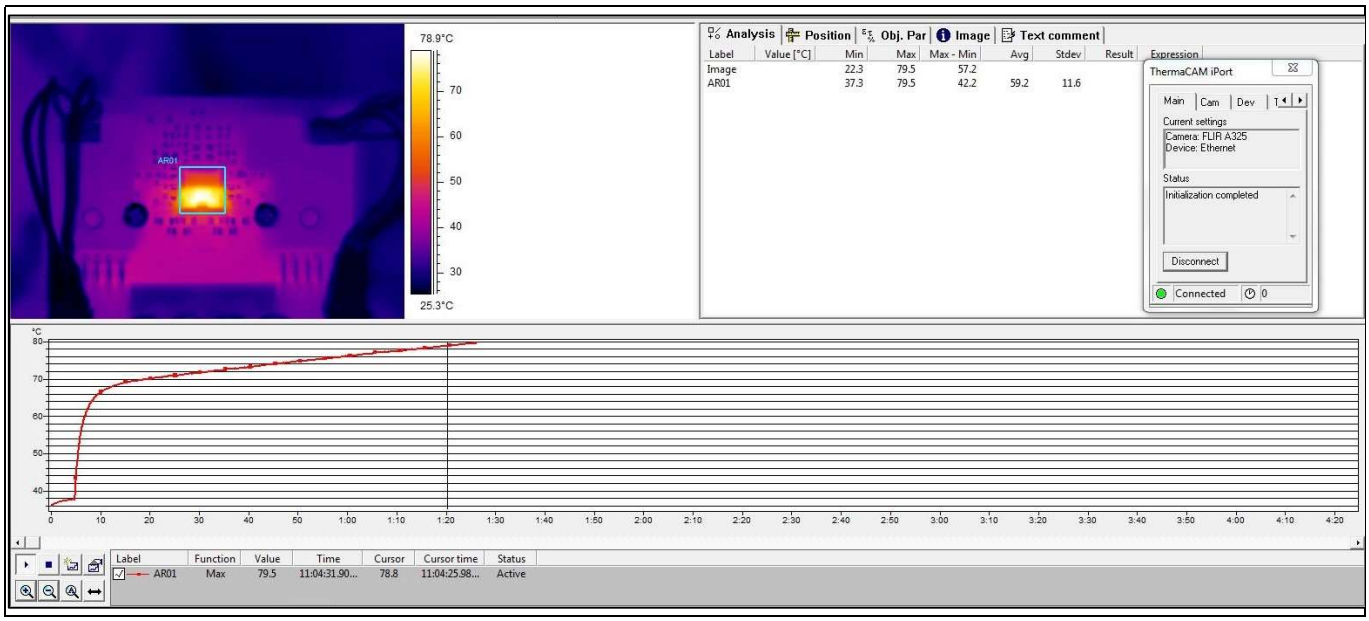

Figure 17 Peak power P_{out} = 226 W with 2 Ω load ±28.5 V

Note: Maximum temperature 121°C at 1 minute.

Table 7 Peak power without heatsink

Load (Ω)	$\pm V_{bus}$ (V)	10 percent THD+N power (W)	Duration
4	32	136	More than 1 minute no thermal shutdown
2	13.7	100	

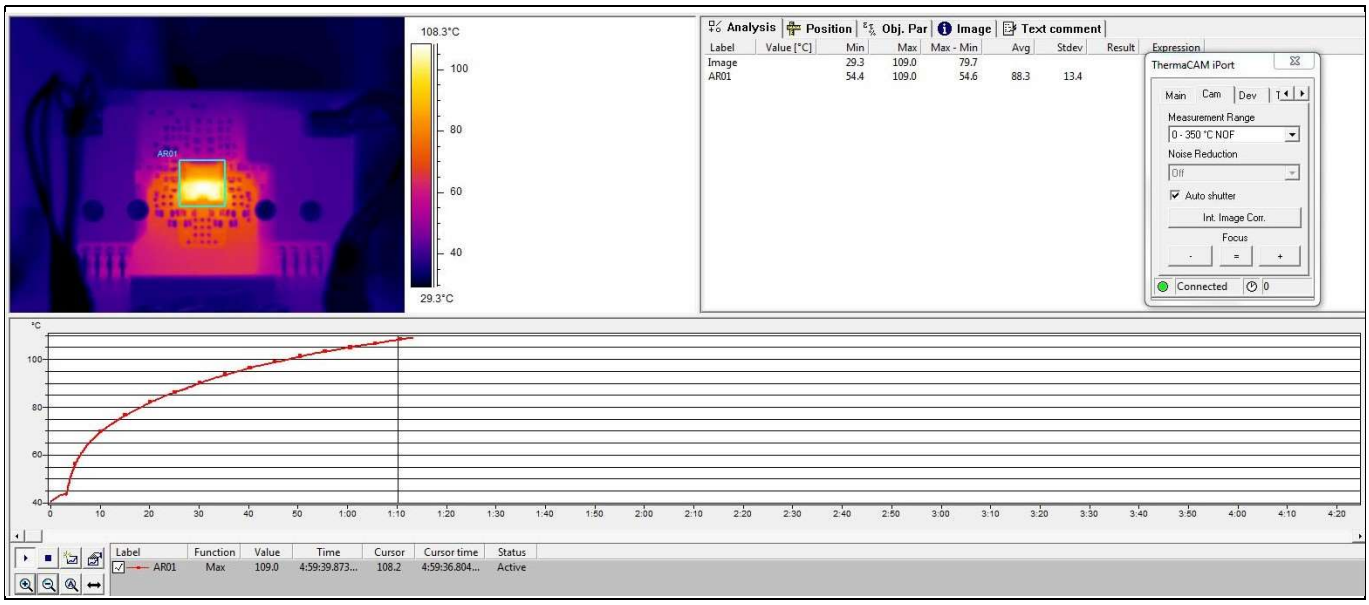

Figure 18 Peak power P_{out} = 136 W with 4 Ω load ±30 V

Note: Maximum temperature 108°C at 1 minute.

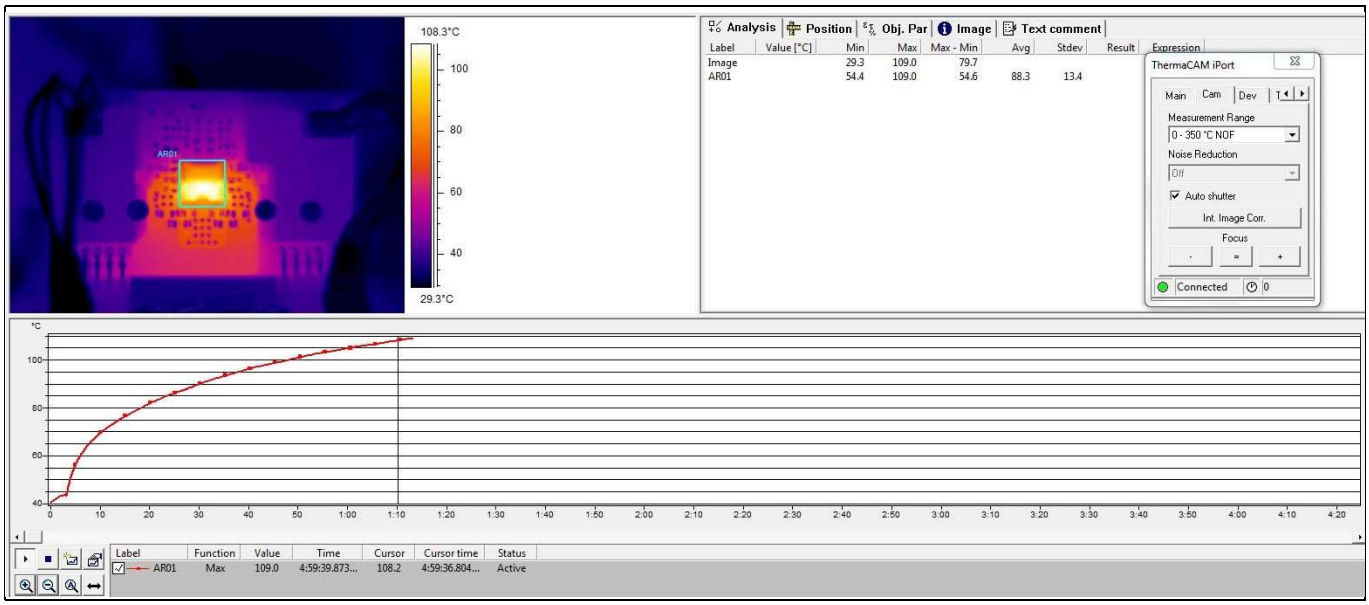

Figure 19 Peak power P_{out} = 100 W with 2 Ω load ±19 V

Note: Maximum temperature 132°C at 1 minute.

Table 8 1/8 power test with heatsink

Load (Ω)	$\pm V_{bus}$ (V)	Max. T-case (°C)	1/8 power (W)	Duration (minutes)
6	32	51	10	30
4	32	60	14	30
3	32	72	19	30
2	28.5	87	22	30

Table 9 1/8 power test without heatsink

Load (Ω)	$\pm V_{bus}$ (V)	Max. T-case (°C)	1/8 power (W)	Duration (minutes)
4	30	84	13	30
2	19	82	9	30

5.2 Heatsink Information

Heatsink: V8818V

Thermal pad: BER161-ND

Figure 20 Heatsink installation

6 Functional Block Diagram

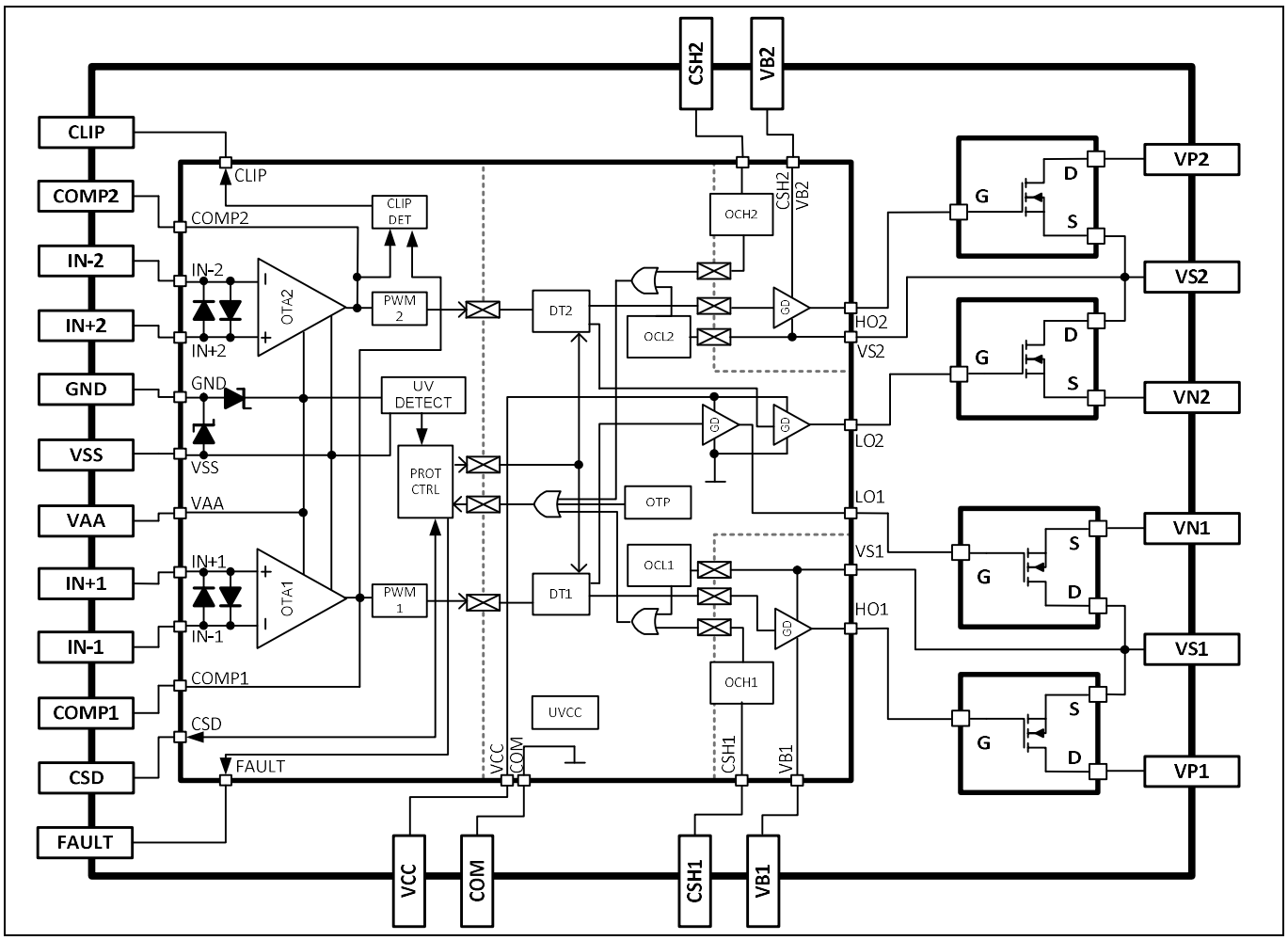

Figure 21 Block diagram

7 Typical Implementation

The MA5302MS can be designed as single-ended BTL or PSE output, using a single or split power supply. Here are examples of typical configurations.

A configuration for single-ended input with split power supply sets the base example. The front end section refers to GND which is common to speaker output GND.

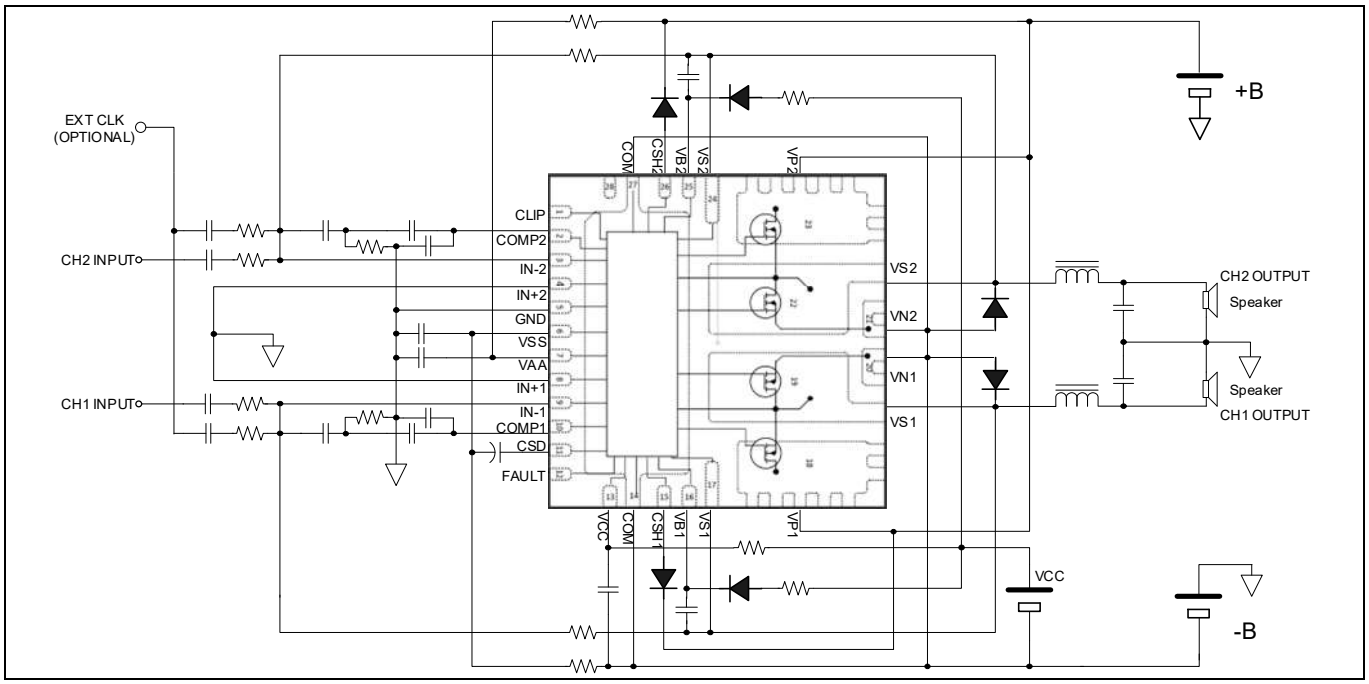

Figure 22 Inverting amplifier with Split Power Supply

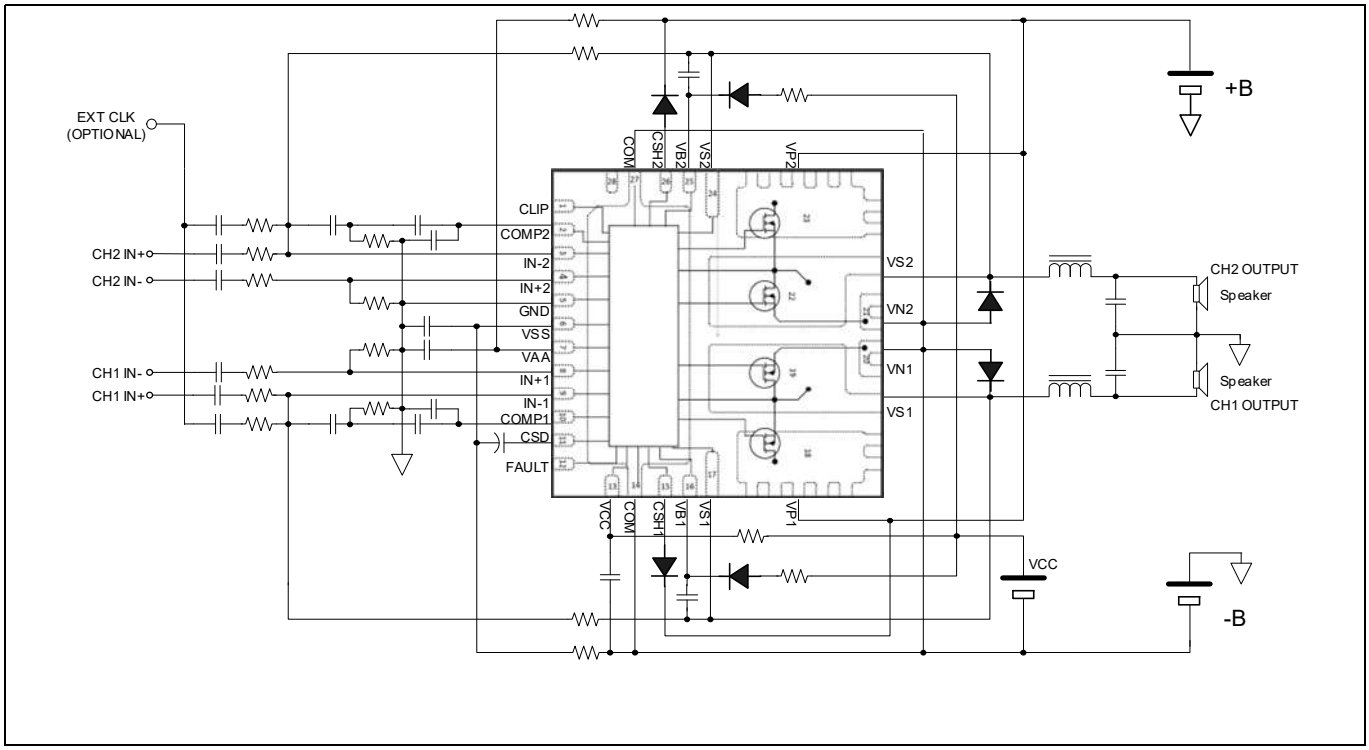

Figure 23 Differential amplifier with Split Power Supply

The single-supply configuration uses a virtual GND which sits in the middle of the power supply rail. The front-end section of the amplifier refers to the virtual GND as a reference. This method uses differential input to receive an input signal from a different voltage potential. It is recommended to allow input capacitors to fully settle to steady-state values before releasing the CSD pin to start PWM oscillation. The load current and inductor ripple current flow through the bus splitting capacitor.

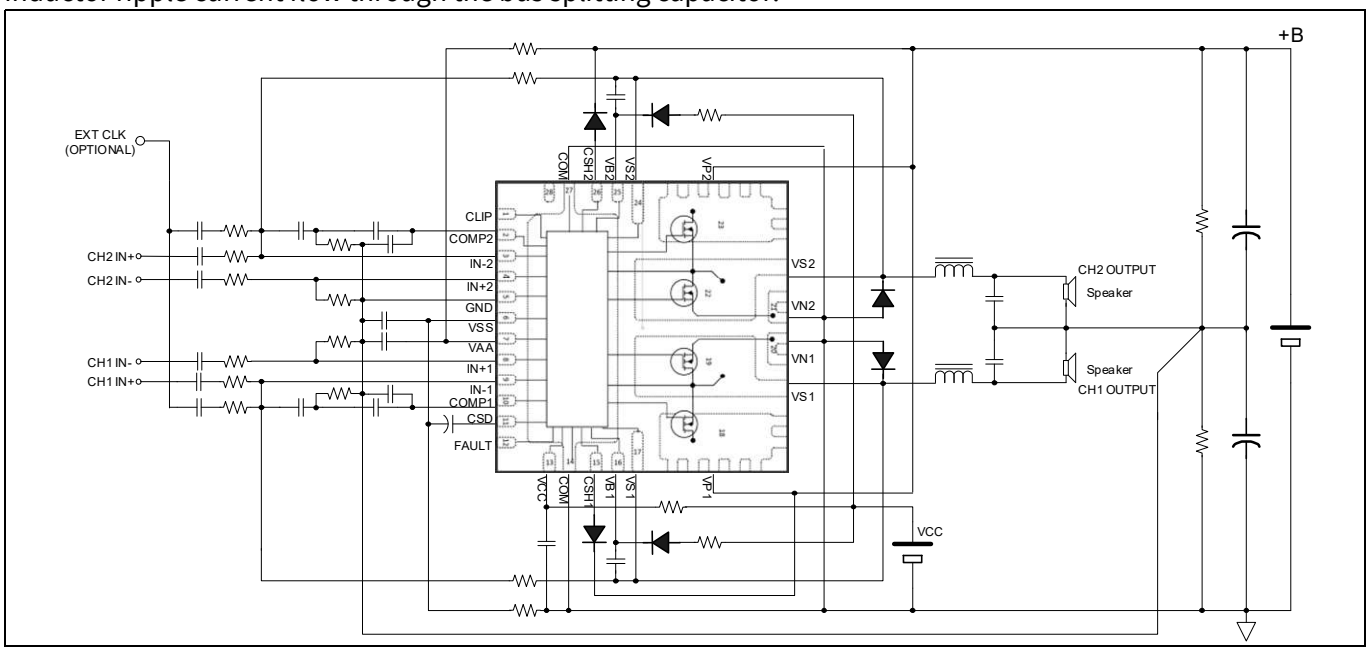

Figure 24 Typical Application Circuit with Single Power Supply

Balanced Tied Load (BTL) output takes two output legs for speaker output. It doubles output power with double load impedance. Any load current does not flow through supply dividing capacitor; therefore BTL configuration is free from GND fluctuations. Also, the bus splitting capacitor can be much smaller. Higher output power and absence of GND fluctuation make BTL suitable for subwoofer applications.

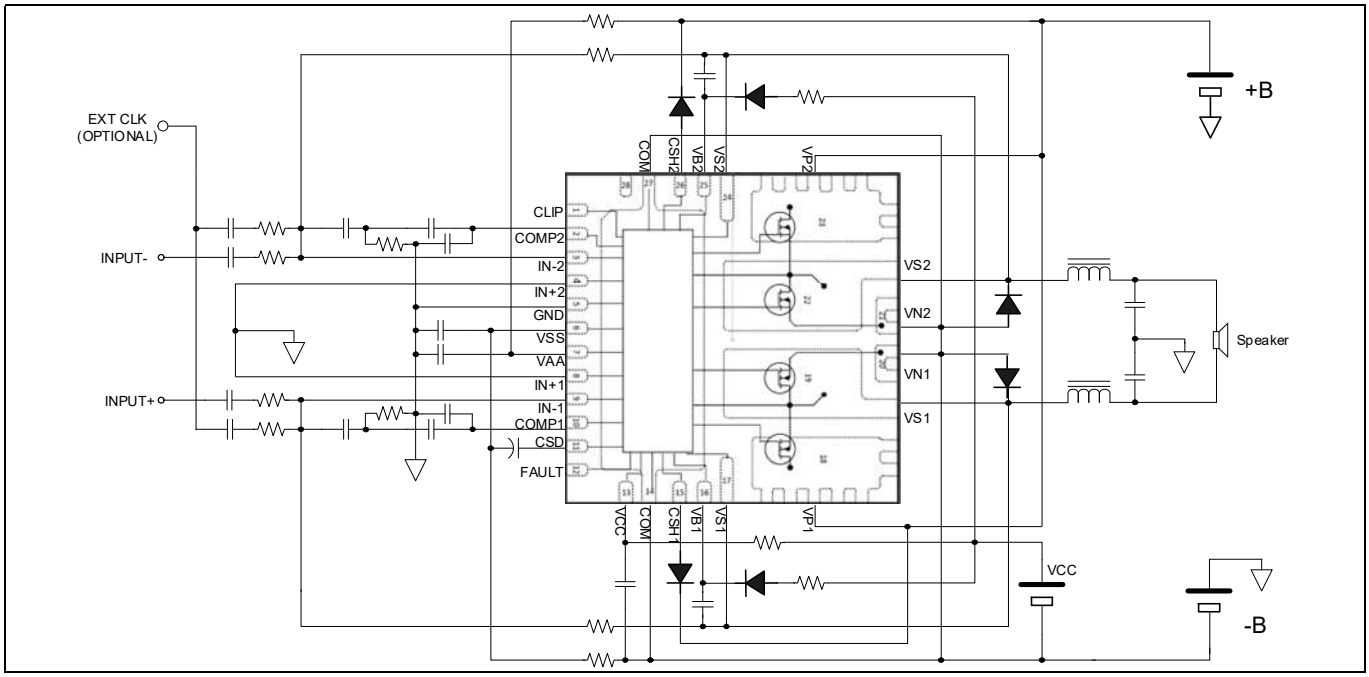

Figure 25 Typical Bridged Tied Load (BTL) Output Application with Split Power Supply

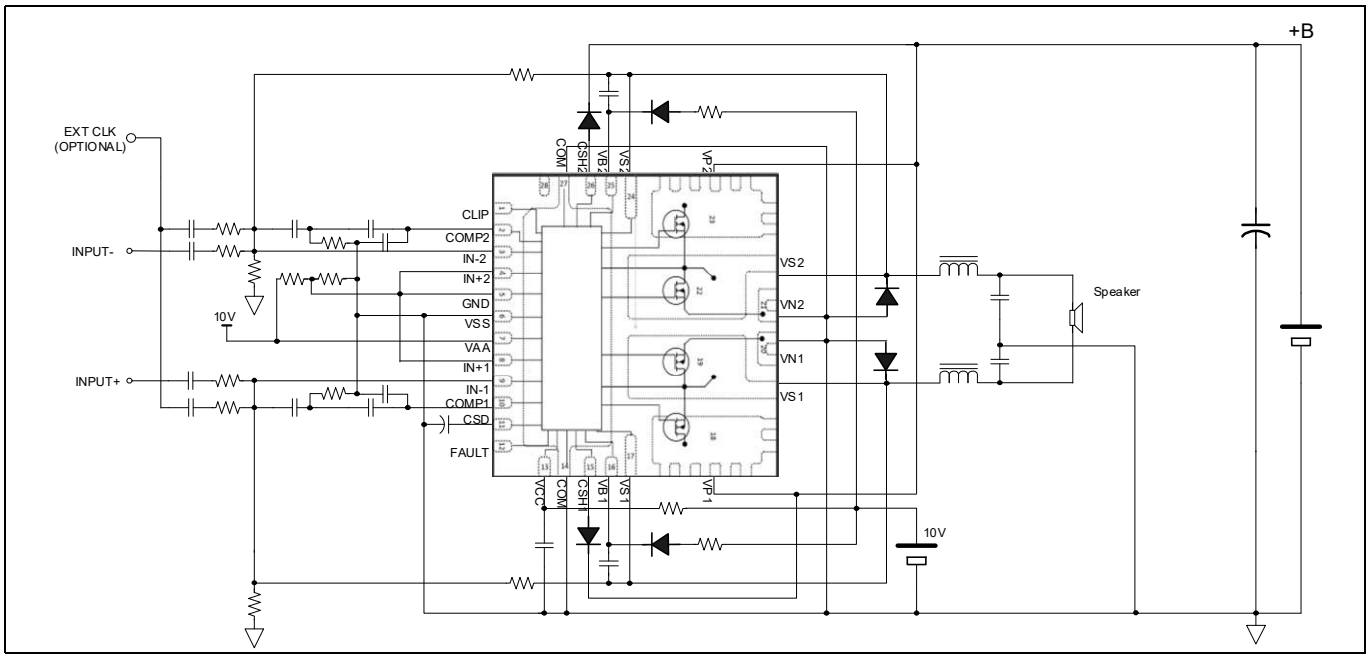

Figure 26 Typical Bridged Tied Load (BTL) Output Application with Single Power Supply

Parallel Single Ended (PSE) output parallels two channels' output legs for one speaker output. It doubles output current and makes it easier to drive a low impedance load. Higher output current with lower bus voltage makes PSE suitable for subwoofer applications.

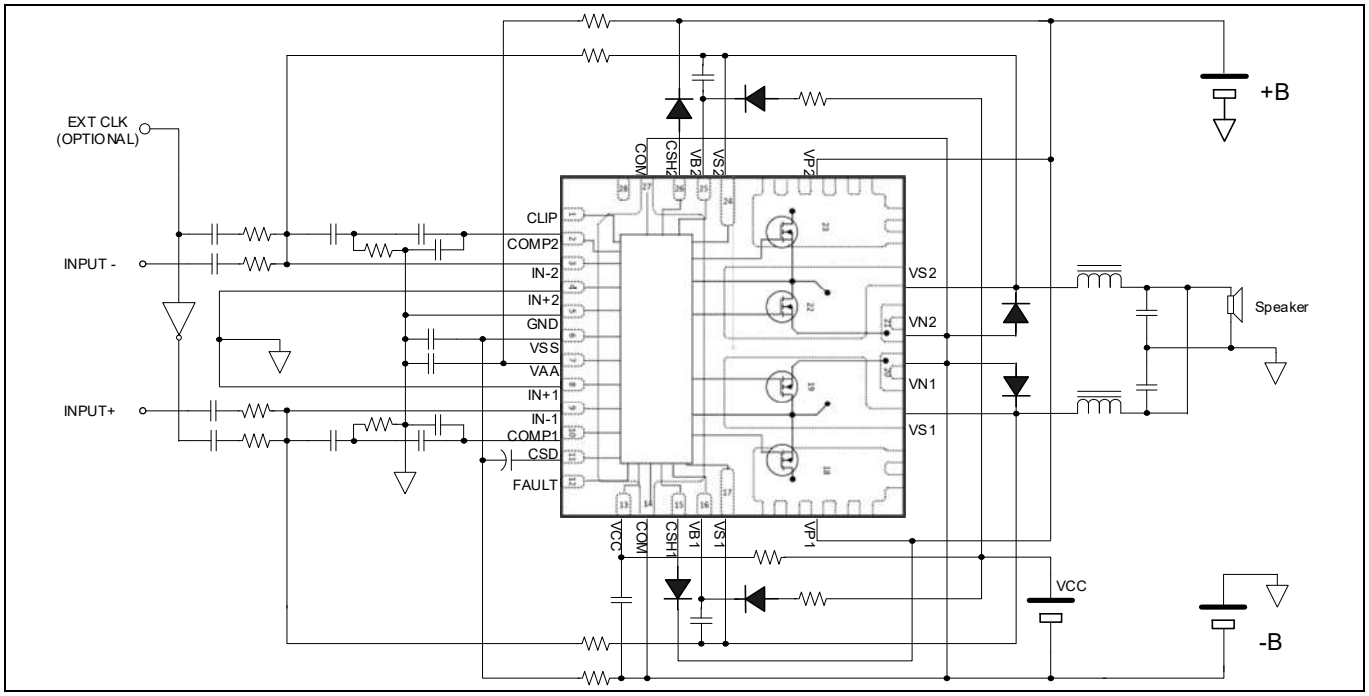

Figure 27 PSE amplifier with Split Power Supply

8 Input / Output Pin Equivalent Circuit Diagrams

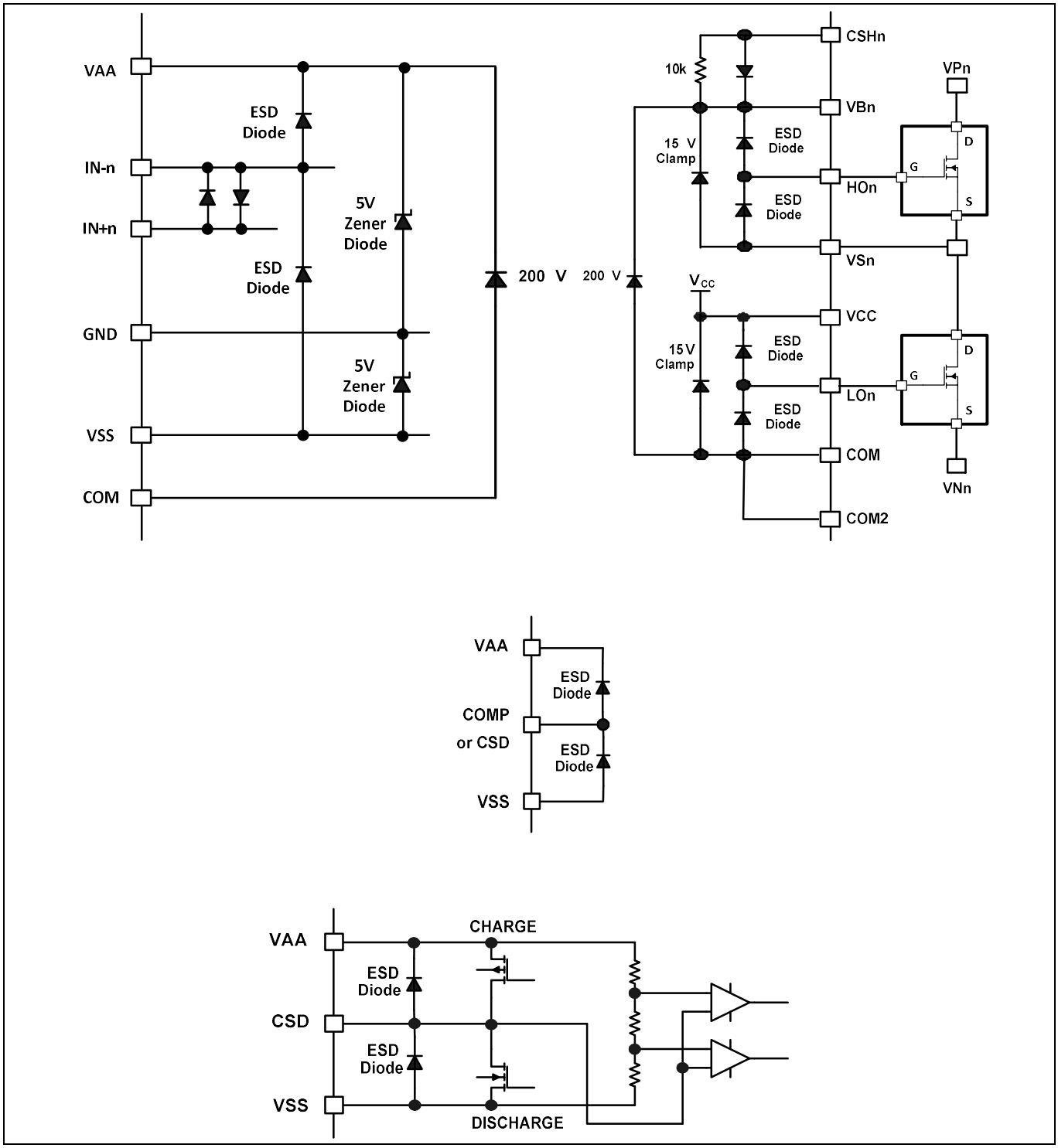

Figure 28 Input/output pin equivalent circuit diagrams

9 PWM Modulator Design

The open-access front-end configuration of MA5302MS enables many ways to implement a PWM modulator. This section explains how PWM modulation works based on an example of a self-oscillating PWM modulator in a typical application.

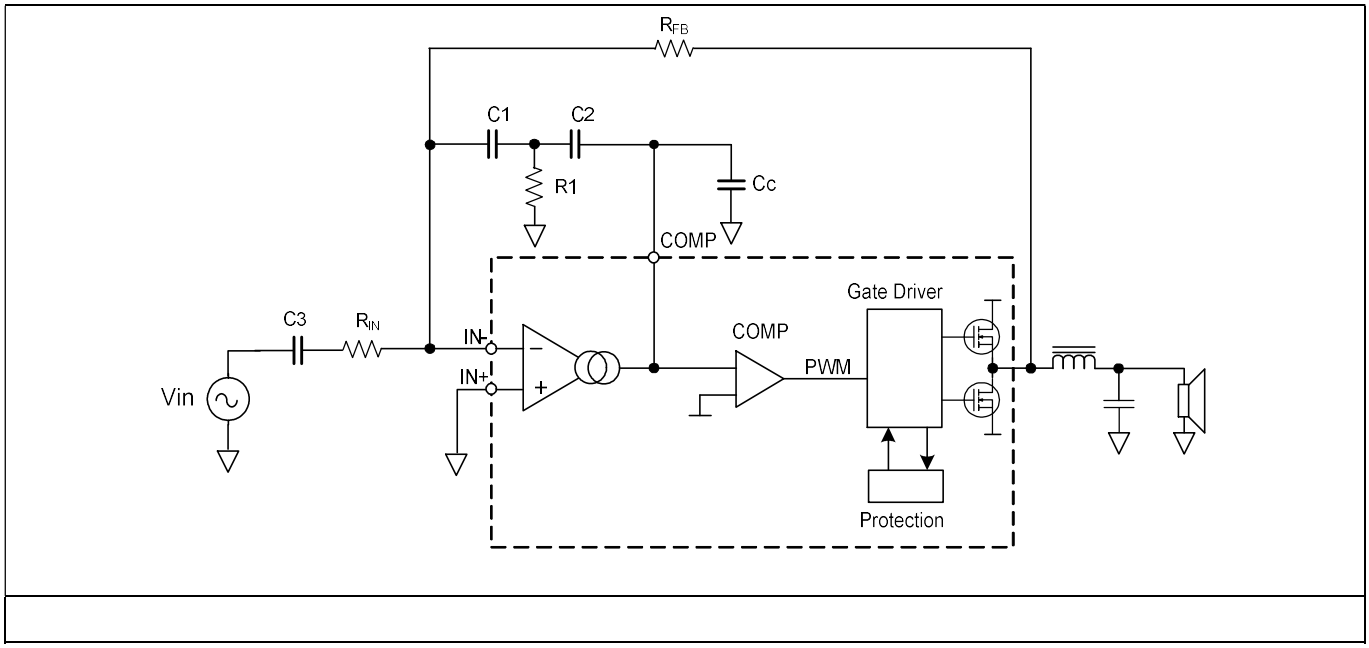

Figure 29 MA5302MS Typical Control Loop Design

9.1 Input Section

The audio input stage of MA5302MS forms an inverting error amplifier. The voltage gain of the amplifier, G_V, is determined by the ratio between input resistor R_{IN} and feedback resistor R_{FB}.

$$G_V = \frac{R_{FB}}{R_{IN}}$$

Since the feedback resistor R_{FB} is part of an integrator time constant, which determines switching frequency, changing the overall voltage gain by R_{IN} is simpler and therefore recommended. Note that the input impedance of the amplifier is equal to the input resistor R_{IN}.

A DC blocking capacitor C3 should be connected in series with R_{IN} to minimize the DC offset voltage on the output. Due to potential distortion, a ceramic capacitor is not recommended. Minimizing the DC offset is essential to minimize the audible noise during power-ON and -OFF.

The connection of the non-inverting input IN+ is a reference for the error amplifier, and thus is crucial for audio performance. Connect IN+ to the signal reference ground in the system, which has the same potential as the negative terminal of the speaker output.

9.2 Control Loop Design

The MA5302MS allows the user to choose from numerous methods of PWM modulator implementations. In this section, all the explanations are based on a typical application circuit of a self-oscillating

9.3 PWM Frequency

Choosing the switching frequency entails making a trade-off between many aspects. At lower switching frequency, conduction losses in the MOSFET stage increases due to higher inductor ripple current. The output carrier leakage in the speaker output increases. At higher switching frequency, the efficiency degrades due to higher switching losses. Higher switching frequency supports wider audio bandwidth. The inductor ripple decreases yet core loss might increase. For these reasons, 400kHz is chosen for a typical design example.

Self-oscillating frequency has little influence from the bus voltage and input resistance RIN. Note that the nature of a self-oscillating PWM is for the switching frequency to decrease as PWM modulation deviates from idling.

Table 6 summarizes suggested values of components for a given target self-oscillating frequency. The front-end operational transconductance amplifier (OTA) output has limited voltage and current compliances. This set of component values ensures that OTA operates within its linear region for optimal THD+N performance. In case the target frequency is somewhere in between the frequencies listed in Table 6, simply adjust the frequency by tweaking R1.

Table 10 External Component Values vs. Self-Oscillation Frequency

Target Self-Oscillation Frequency (kHz)	C1=C2 (nF)	R1 (ohms)
500	2.2	200
450	2.2	165
400	2.2	141
350	2.2	124
300	2.2	115
250	2.2	102
200	4.7	41.2
150	10	20.0
100	10	14.0
70	22	4.42

9.4 Clock Synchronization

In the PWM control loop design example, the self-oscillating frequency can be set and synchronized to an external clock. Through a set of resistors and a capacitor, the external clock injects periodic pulsating charges into the integrator, forcing oscillation to lock up to the external clock frequency. A typical setup with 5 Vp-p 50% duty clock signal uses R_{CK}=22 kΩ and C_{CK}=100 pF in Figure 30. To maximize audio performance, the self-running frequency without clock injection should be 20 to 30% higher than the external clock frequency.

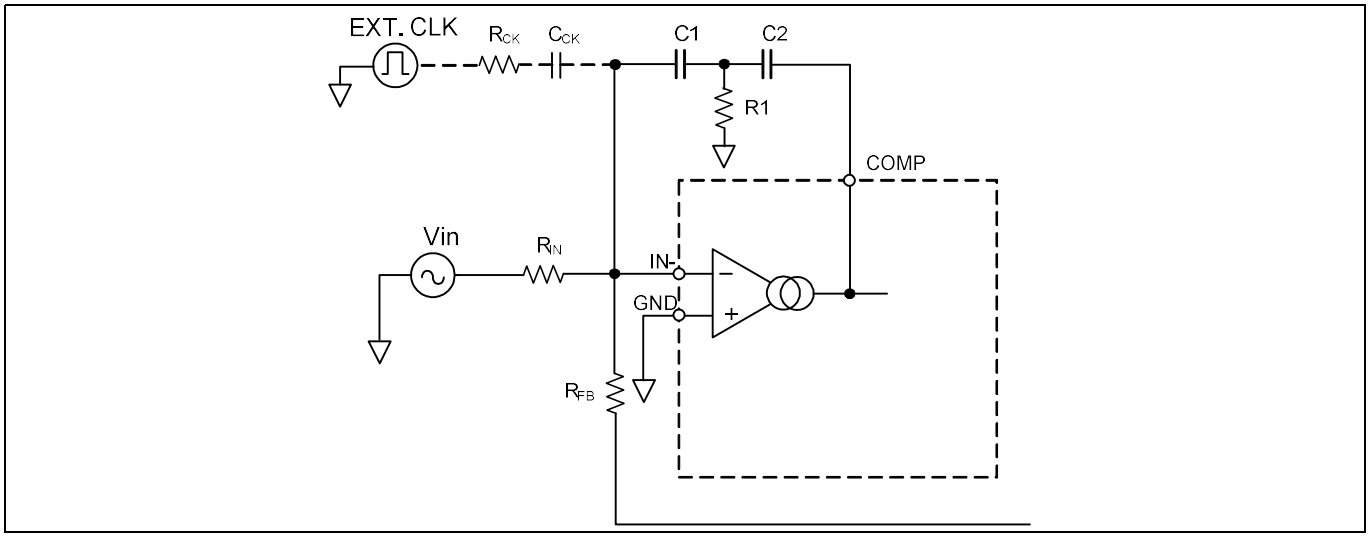

Figure 30 External Clock Synchronization

Figure 31 shows how a self-oscillating frequency locks up to an external clock frequency. A design of a 400 kHz self-oscillating frequency synchronizes to an external clock whose frequency is within the red border lines.

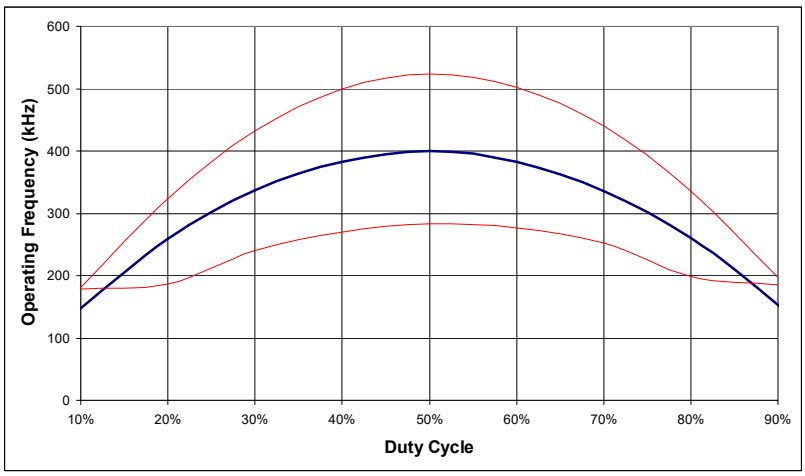

Figure 31 Typical Lock Range to External Clock

9.5 Click Noise Elimination

The MA5302MS has a unique feature that minimizes power-ON and -OFF audible click noise. When CSD is in between Vth1 and Vth2 during start-up, an internal closed loop around the OTA enables an oscillation that generates voltages at COMP and IN-, bringing them to steady-state values. It runs at around 1 MHz, independent from the switching oscillation.

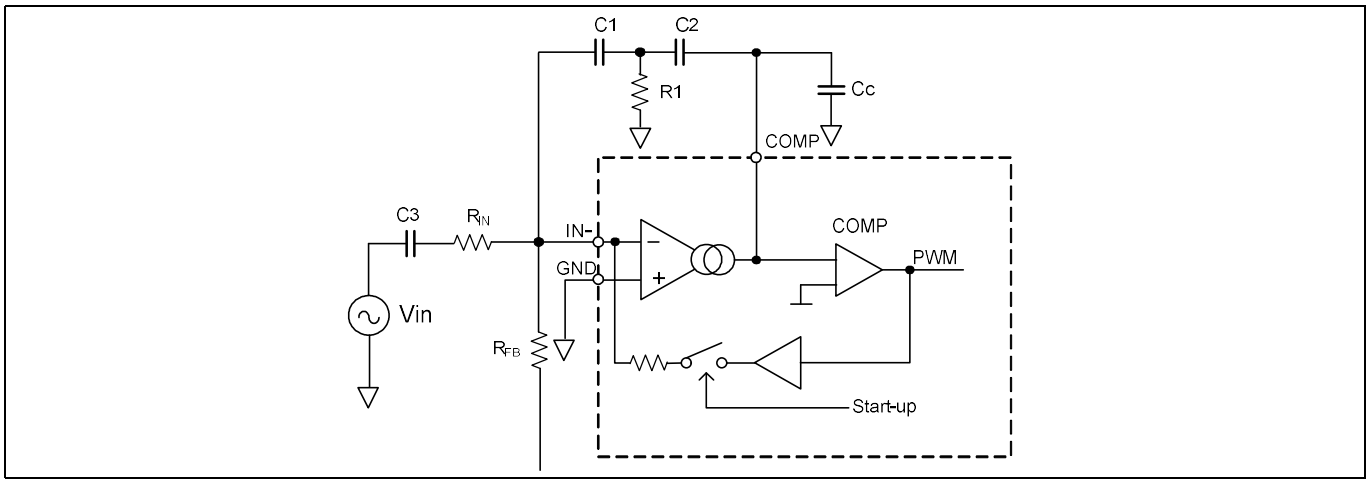

Figure 32 Audible Click Noise Elimination

As a result, all capacitive components connected to COMP and IN- pins, such as C1, C2, C3 and Cc in Figure 32, are pre-charged to their steady-state values during the start-up sequence. This allows instant settling of closed-loop PWM operation.

To utilize the click noise reduction function, the following conditions must be met.

1. CSD pin has slow enough ramp up from Vth1 to Vth2 such that the voltages in the capacitors can settle to their target values.
2. High-side bootstrap power supply needs to be charged up prior to starting oscillation.
3. Audio input has to be zero.
4. For internal local loop to override external feedback during the startup period, DC offset at speaker output prior to shutdown release has to satisfy the following condition.

$$DCoffset \quad < 30\ \mu A \cdot R_{FB}$$

9.6 Differential Input

Figure 33 shows an example of a differential input configuration. This design is useful in a single supply configuration. Use R_{IN1}=R_{IN2}, R_{FB1}=R_{FB2}, C3=C4.

Voltage gain is given by a ratio between R_{IN} and R_{FB}.

$$G_V = \frac{R_{FB}}{R_{IN}}$$

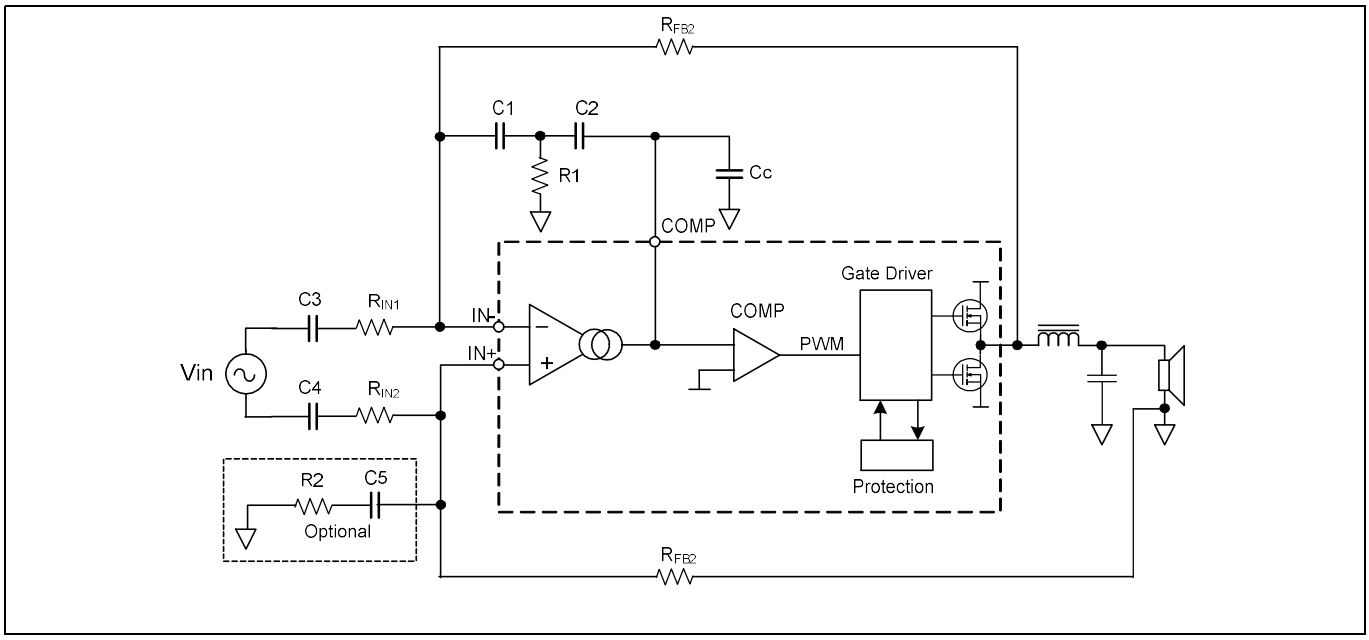

Figure 33 Differential Input

Although component values in the feedback network are balanced between inverting and non-inverting inputs, the integration capacitor path in the non-inverting input creates unbalance at high frequencies, causing slightly higher distortion compared to an unbalanced input configuration. To improve the THD degradations, place optional RC network R2=R1 and C5=C1.

10 Operational Mode

The CSD pin determines the operational mode of the MA5302MS as shown in Figure 34. The OTA has three operational modes: shutdown, pop-less startup and normal operation; while the gate driver section has two modes: shutdown and normal operation.

When V_{CSD} < Vth2, the IC is in shutdown mode and the input OTA is cut off. When Vth2< V_{CSD} < Vth1, the output MOSFETs are still in shutdown mode. The OTA is activated and starts local oscillation for pop-less start-up which pre-biases all the capacitive components in the error amplifier. When V_{CSD}>Vth1, the MA5302MS enters normal operation mode and PWM operation starts.

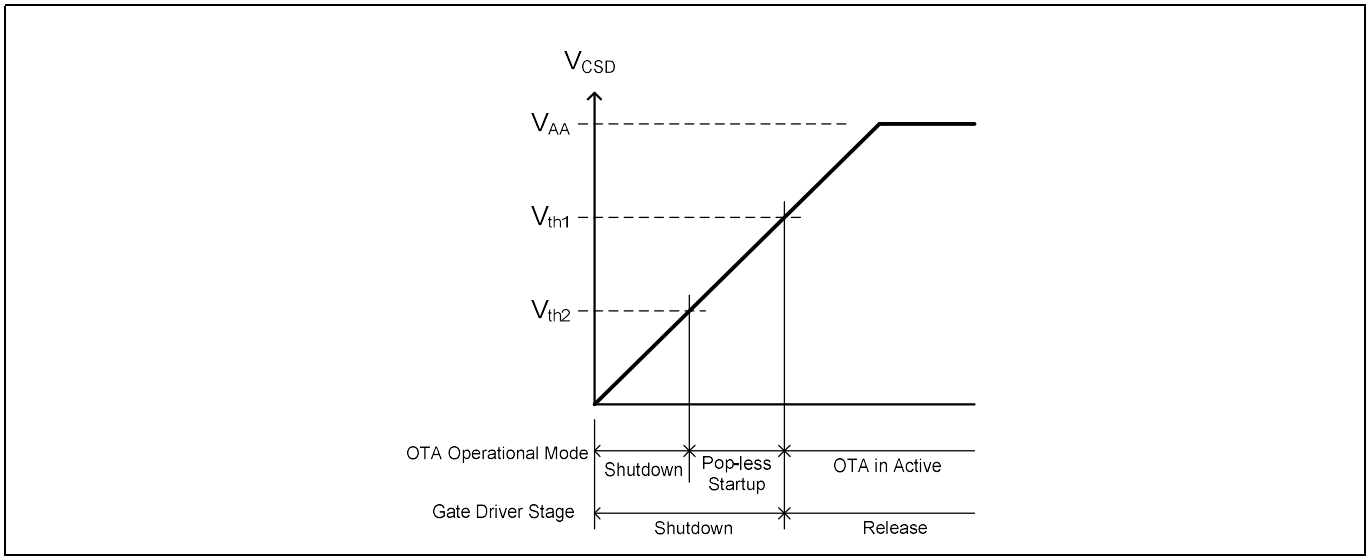

Figure 34 V_{CSD} and Operational Mode

10.1 Self-oscillation Start-up Condition

The MA5302MS requires the following conditions in order for pop-less startup to work properly.

- All the control power supplies, VAA, VSS, VCC and VBS are above the under-voltage lockout thresholds.
- CSD pin voltage is over Vth1 threshold.
- $|i_{IN}| < |i_{FB}|$

  Where $i_{IN} = \frac{V_{IN}}{R_{IN}}$, $i_{FB} = \frac{V_{+B}}{R_{FB}}$.
- The duration CSD voltage transitioning from Vth2 to Vth1 is long enough to pre-charge input and integration capacitors around OTA section.

11 Protections

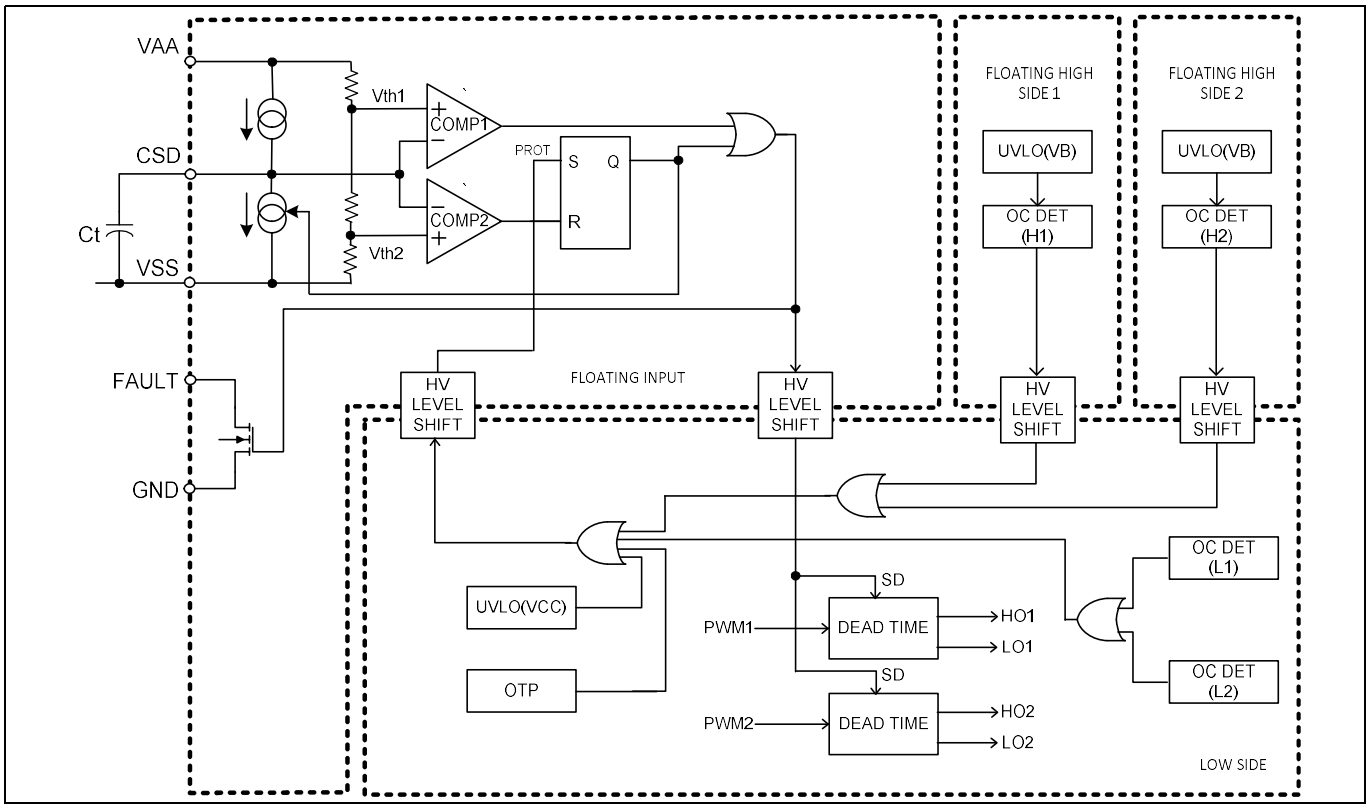

Figure 35 Protection Functional Block Diagram (MA5302MS)

The internal protection control block dictates the operational modes, normal or shutdown, using the input of the CSD pin. In shutdown mode, the controller IC turns off internal power MOSFETs.

The CSD pin provides five functions.

1. Power up delay timer
2. Self-reset timer
3. Shutdown input
4. Latched protection configuration
5. Shutdown status output (host I/F)

The CSD pin cannot be paralleled with another MA5302MS directly.

The operating statuses of the protection features are shown in Table 2.

Table 11 Events and Actions of CSD and FAULT

Event	CSD	FAULT
UVCC, rising edge	Recycle	L until CSD>Vth1
UVCC, falling edge	n/a	n/a
UVAA, rising edge	n/a	L at VAA<UVAA
UVAA, falling edge	n/a	L at VAA<UVAA
UVBS, rising edge	n/a	n/a
UVBS, falling edge	n/a	n/a

Over Current Protection	Keep recycling until OCP is reset	Held L until OCP is reset
DC Protection	Held L until DCP is reset	Held L until DCP is reset
Clip Detection	n/a	n/a
OTP1-3 Inputs	Keep recycling until OTP is reset	Held L until OTP is reset

*CSD recycle: CSD pin voltage discharges down to Vth2 and charges back to VAA, if CSD pin is configured as self reset protection.

11.1.1 Self-Reset Protection

Attaching a capacitor between CSD and V_{SS} configures the MA5302MS self-reset protection mode.

Upon an OCP event, the CSD pin discharges the external capacitor voltage V_{CSD} down to the lower threshold V_{th2} to reset the internal shutdown latch. Then, the CSD pin begins to charge the external capacitor, Ct, in an attempt to resume operation. Once the voltage of the CSD pin rises above the upper threshold, V_{th1}, the IC resumes normal operation.

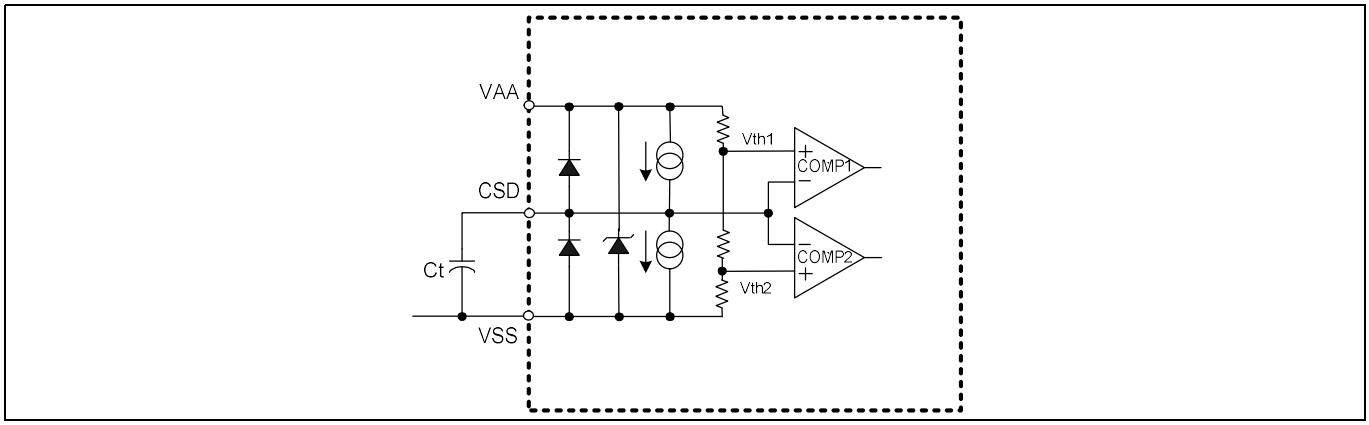

Figure 36 Self-Reset Protection Configuration

11.1.2 Designing Ct

The external timing capacitor, Ct, programs self-reset timings: t_{RESET} and t_{SU}.

- t_{RESET} is the time that elapses from when the IC enters the shutdown mode to the time when the IC resumes operation. t_{RESET} should be long enough to avoid over heating the MOSFETs from the repetitive sequence of shutting down and resuming operation during over-current conditions. In most applications, the minimum recommended time for t_{RESET} is 0.1 seconds.
- t_{SU} is the time between powering up the IC in shutdown mode to the moment the IC releases shutdown to begin normal operation.

The Ct determines t_{RESET} and t_{SU} as following equations:

$$t_{RESET} = \frac{Ct \cdot V_{AA}}{1.1 \cdot I_{CSD}} \quad [s]$$

$$t_{SU} = \frac{Ct \cdot V_{AA}}{0.7 \cdot I_{CSD}} \quad [s]$$

where I_{CSD}: the charge/discharge current at the CSD pin
V_{AA}: the floating input supply voltage with respect to V_{SS}.

11.1.3 Shutdown Input

During normal operation, pulling the CSD pin below the upper threshold Vth1 forces the IC into shutdown mode. Figure 37 shows how to add an external discharging path to shutdown the PWM.

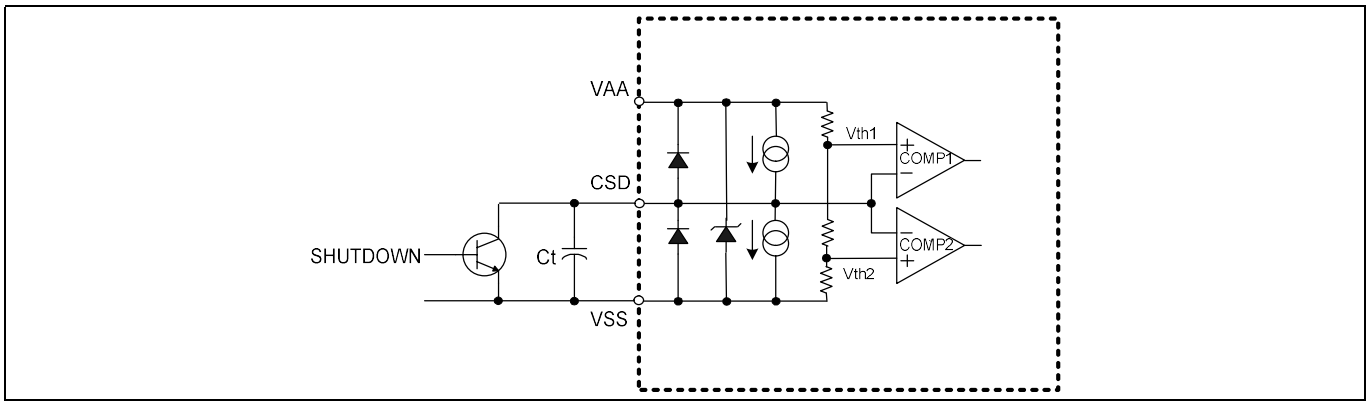

Figure 37 Shutdown Input

11.1.4 Latched Protection

Connecting CSD to V_{AA} through a 10 kΩ or less resistor configures latched protection mode. The internal shutdown latch stays in shutdown mode after the overcurrent is detected. An external reset switch brings CSD below the lower threshold Vth2 for a minimum of 200 ns and resets the latch. At first power-up, a reset signal to the CSD pin is required to release the IC from shutdown mode.

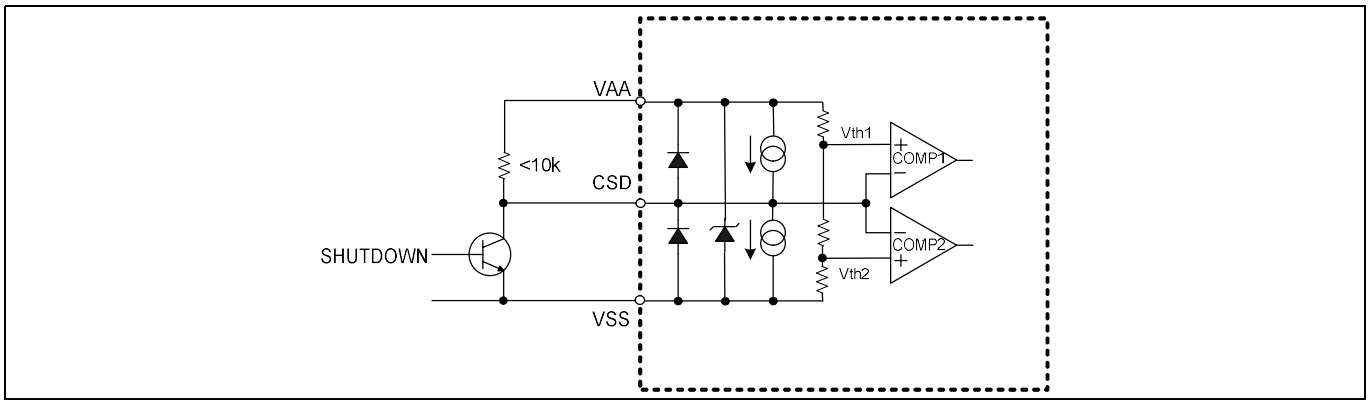

Figure 38 Latched Protection with Reset Input

11.1.5 Interfacing with System Controller

The MA5302MS can communicate with an external system controller through a simple interfacing circuit shown in Figure 39. A generic PNP transistor, U1, detects the sink current at the CSD pin during protection event and outputs a shutdown flag signal to an external system controller. Another generic NPN transistor, U2, can then reset the internal protection logic by pulling the CSD voltage below the lower threshold Vth2. After the first power-up sequence, a reset signal to the CSD pin is required to release the IC from shutdown mode.

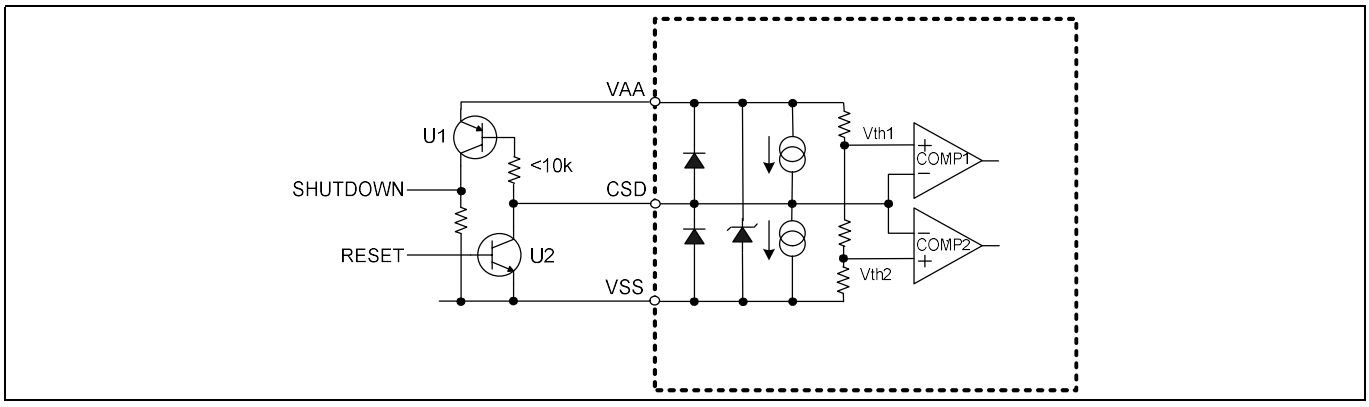

Figure 39 Interfacing CSD with System Controller

11.2 Over Current Protection (OCP)

The MA5302MS features over current protection to protect the internal power MOSFETs during abnormal load conditions. The control logic diagrams are in Figure 40. As soon as either the high-side or low-side current sensing block detects over current, the following sequence will occur.

1. The shutdown latch flips its logic states from normal operational mode to shutdown mode.
2. Low-side and high-side MOSFETs go into an off state condition.
3. The CSD pin starts discharging the external capacitor Ct.
4. When voltage across Ct falls below the lower threshold Vth2, COMP2 resets the shutdown latch to normal mode.
5. The CSD pin starts charging the external capacitor Ct.
6. When V_{CSD} goes above the upper threshold Vth1, the logic on COMP1 toggles and the IC resumes operation.

Figure 40 summarizes the above. As long as the over current condition exists, the IC will repeat the over current protection sequence at a repetitive rate set by the CSD capacitor.

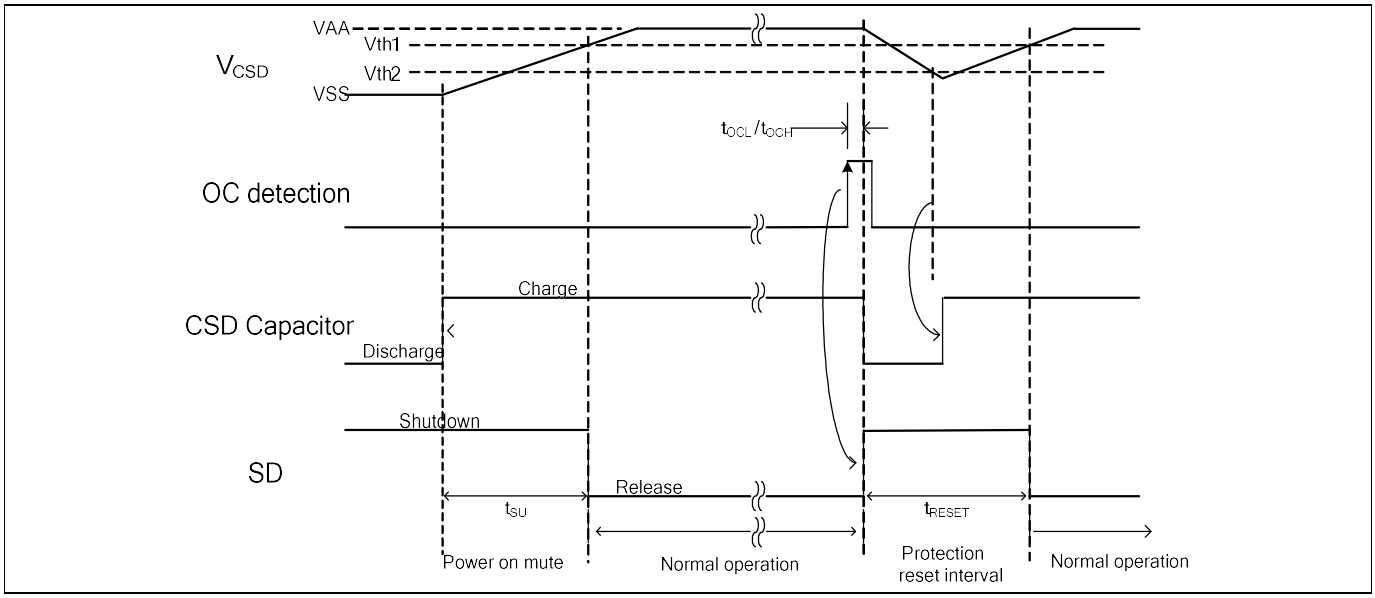

Figure 40 Overcurrent Protection Timing Chart

11.3 Over Temperature Protection (OTP)

If the junction temperature T_J of the controller IC exceeds the on-chip thermal shutdown threshold, T_{SD}, the on-chip over temperature protection shuts down the PWM.

11.4 Under Voltage Protection (UVP)

In order to prevent a partial on-state of the internal MOSFET, under-voltage protection monitors the low side and high side gate bias supplies, VCC and VB. When VCC is below UVLO, both high and low side MOSFETs are turned off. When the high side supply V_{BS} is below the UVLO threshold, the high side output is disabled, while the low side works normally.

12 Status Output

12.1 Fault Output

FAULT output is an open drain output referenced to GND to report whether the MA5302MS is in shutdown mode or in normal operating mode. If the FAULT pin is open, the MA5302MS is in normal operation mode, i.e. the output MOSFETs are active. The following conditions trigger shutdown internally and pulls the FAULT pin down to GND.

- Over Current Protection
- Over Temperature Protection
- Shutdown mode from CSD pin voltage

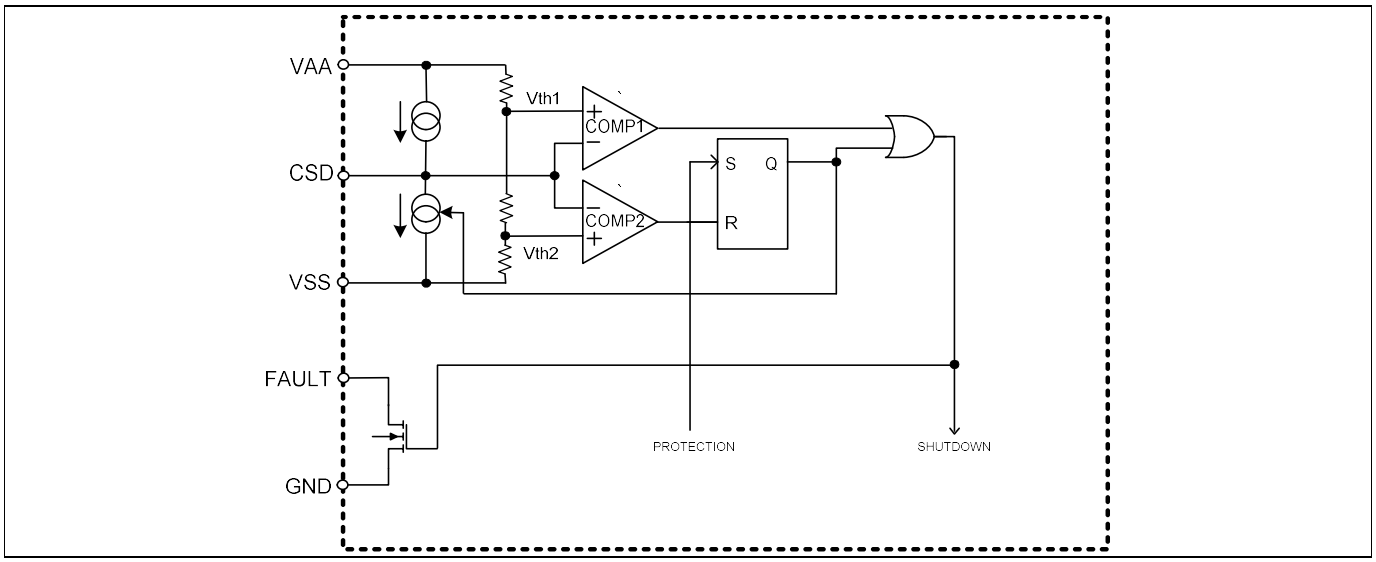

Figure 41 Fault Output

12.2 CLIP Output

When the output of the amplifier loses track of an expected target value, the amplifier enters into clipping condition.
The CLIP detection block monitors the COMP pin voltage with a window comparator. The CLIP pin is pulled to GND when a clipping condition is detected. The detection thresholds in the COMP pin are at 10% and 90% of VAA-VSS. The CLIP outputs are disabled in shutdown mode.

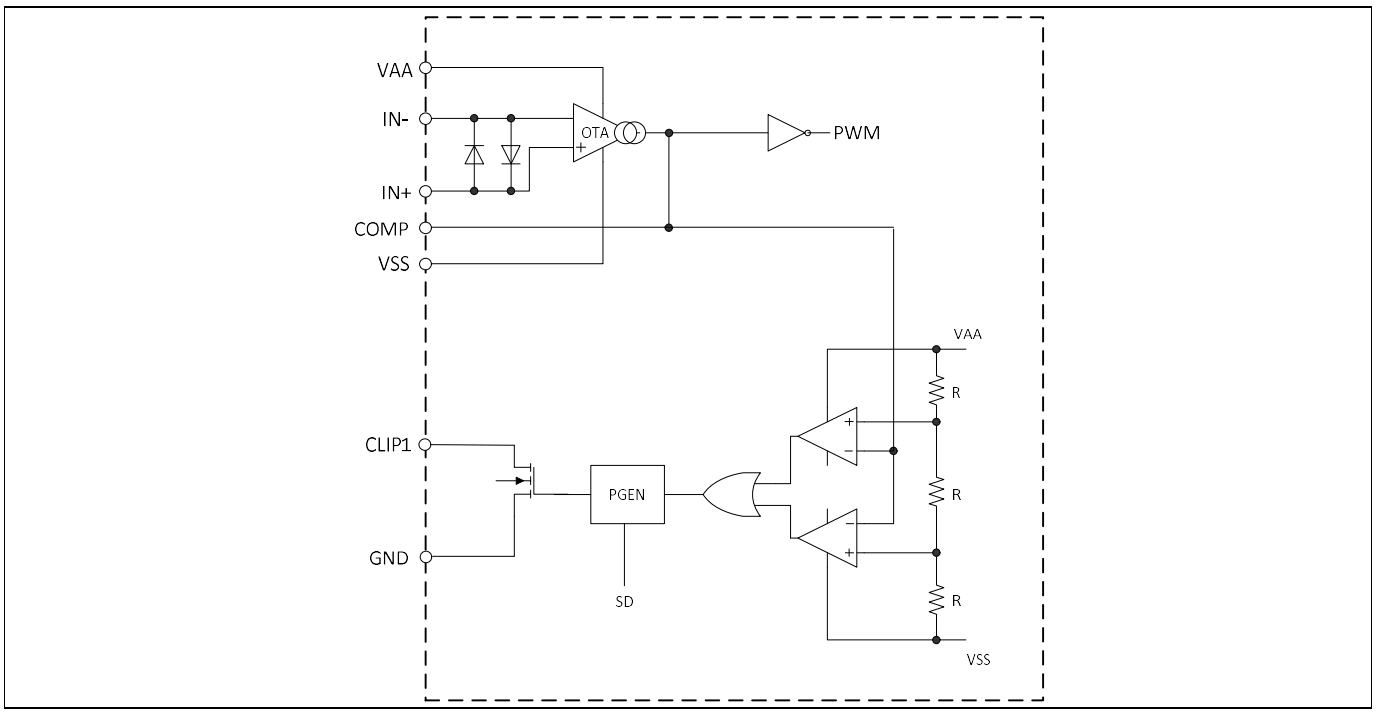

Figure 42 CLIP Detection

13 Power Supply Design

13.1 Supplying VAA and VSS

VAA and VSS are supply voltages to the front-end of the analog section, hence are noise sensitive. For best audio performance, use regulated power supplies for VAA and VSS.

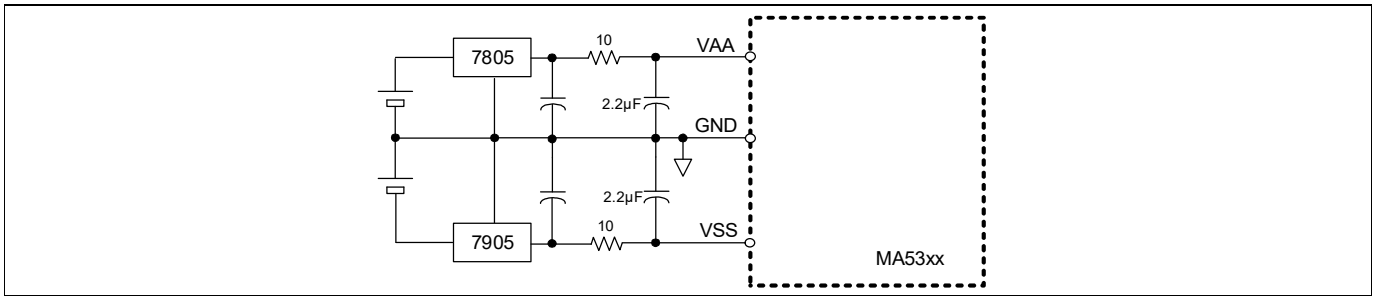

Figure 43 Supplying VAA and VSS with External Voltage Regulators

When switched-mode regulators are used as supply voltages for VAA and VSS, place a two-stage R-C noise filter in the supply lines as shown in Figure 44.

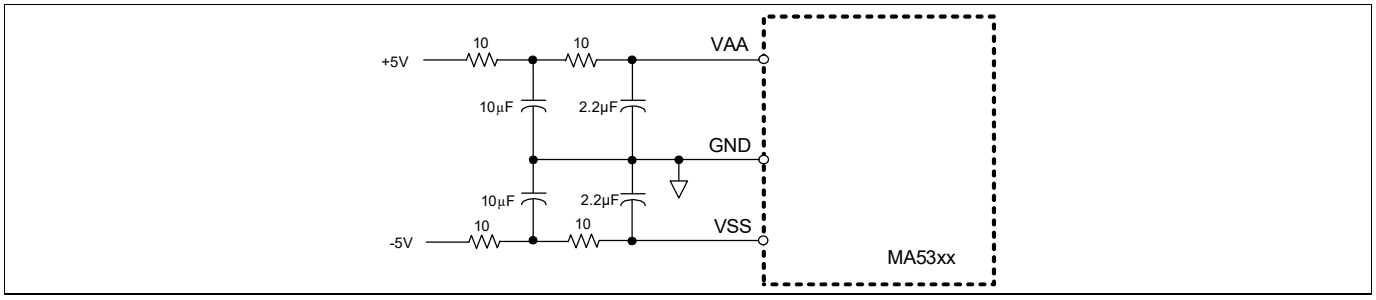

Figure 44 Supplying VAA and VSS from Switched Mode Power Supply

13.2 Supplying VCC and VB

Figure 45 shows the recommended power supply configuration for gate driver power supplies. The gate driver stage has three power supply inputs:

1. VCC-COM: low side gate drive supply
2. VB1-VS1: CH1 high side gate drive supply
3. VB2-VS2: CH2 high side gate drive supply

The low-side power supply, VCC, feeds the internal gate drive logic and low side gate driver. In order to protect VCC from switching noise generated by the VS node, it is recommended to insert a few ohms of R_{VBS} in the bootstrap charging path.

The high-side driver requires a floating supply VBn referenced to the respective switching node VSn where the source of the output MOSFET is connected. A charge pump method (floating bootstrap power supply) eliminates the need for a floating power supply and thus is used in the typical application circuit. The floating bootstrap power supply charges the bootstrap capacitor C_{BS} from the low-side power supply VCC during the low-side MOSFET

ON period. When the high-side MOSFET is ON, the diode cuts off and floats the VBS supply. C_{BS} retains its VB supply voltage for the rest of the high-side ON duration.

$$I_{VCC} \approx I_{QCC} + I_{QBS} + 2(Q_G \cdot f_{PWM}) \quad \text{/per channel}$$

Recommend to have minimum 20% design margin for Ivcc.

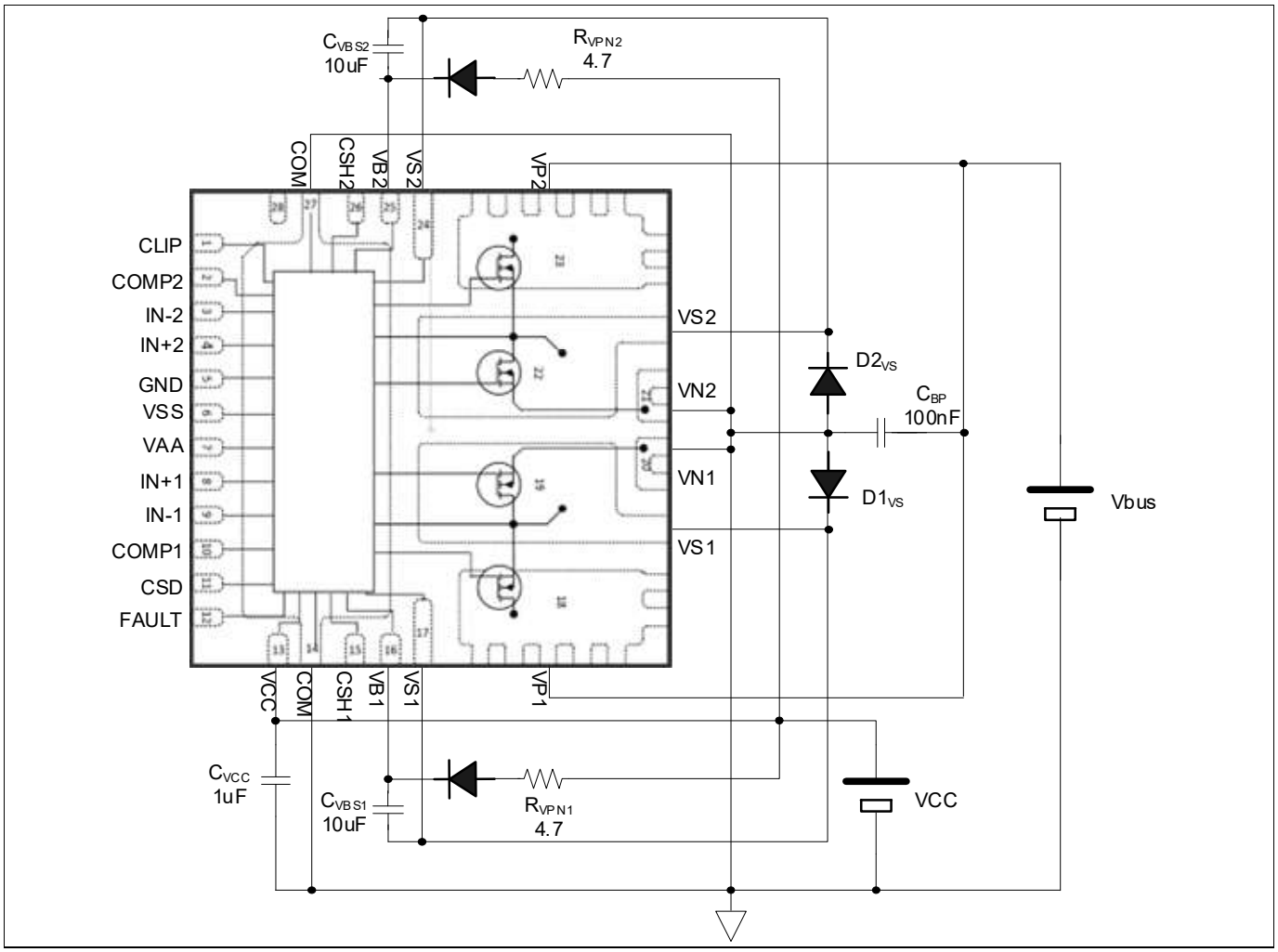

Figure 45 Recommended Power Supply Configurations for Output Stage

13.2.1 Choosing Vs Diode

To prevent excessive negative spiking across low side MOSFET during output short circuit event, add $D1_{vs}$ and $D2_{vs}$ across VS1-VN1 and VS2-VN2. Diode type Schottky 200V/1A is recommended.

13.2.2 Choosing Bootstrap Diode

Use a bootstrap charging diode with voltage rating of 1.5 x the maximum bus voltage. In order to charge the bootstrap capacitor in a very short low-side ON period with a high PWM modulation ratio, a fast recovery diode type with trr of <50ns and Ct of <10pF at 0V is recommended.

13.2.3 Charging V_{BS} Prior to Start

For proper start-up, pre-charging the bootstrap supply V_{BS} prior to PWM start-up is necessary for self-oscillating PWM modulator topologies. A charging resistor, $R_{CHARGE,}$ inserted between the positive supply bus and $V_{B,}$ charges C_{BS} prior to switching start as shown in Figure 46. The minimum resistance of R_{CHARGE} is limited by the maximum PWM modulation index of the system. When the high-side MOSFET is on, R_{CHARGE} drains the bootstrap power supply together with the quiescent current, $I_{QBS,}$ so it reduces the holding time, resulting in maximum continuous high-side on time.

The maximum resistance of R_{CHARGE} is limited by the current charge capability of the resistor during startup.

Pre-charging current flows into the speaker load. In order to startup without the load connected, a dummy load R_{dummy} in parallel with the speaker output provides a pre-charging current path.

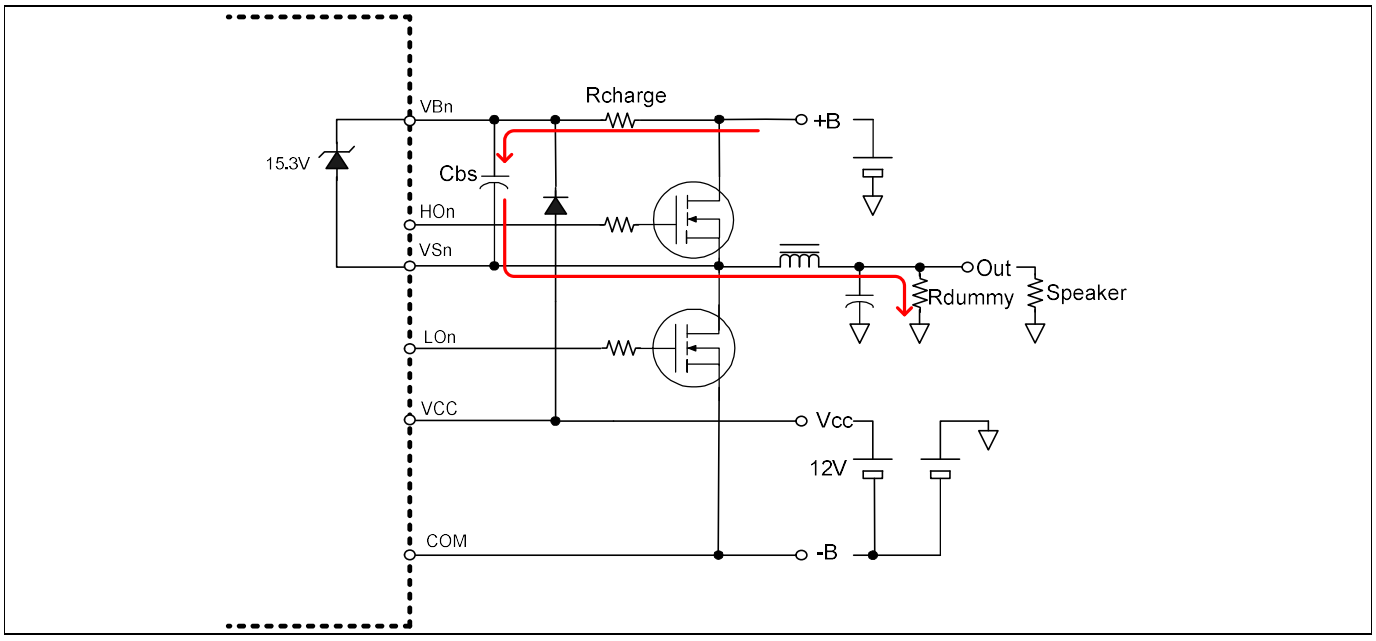

Figure 46 Bootstrap Supply Pre-Charging

13.3 Power Supply Sequence

The protection control block in the MA5302MS monitors the status of V_{AA} and V_{CC} to ensure that both voltage supplies are above their respective UVLO (under voltage lockout) thresholds before starting normal operation. If either V_{AA} or V_{CC} is below the under voltage threshold, the output MOSFETs are disabled in shutdown mode until both V_{AA} and V_{CC} rise above their voltage thresholds. As soon as V_{AA} or V_{CC} falls below its UVLO threshold, protection logic in the MA5302MS turns off high-side and low-side.

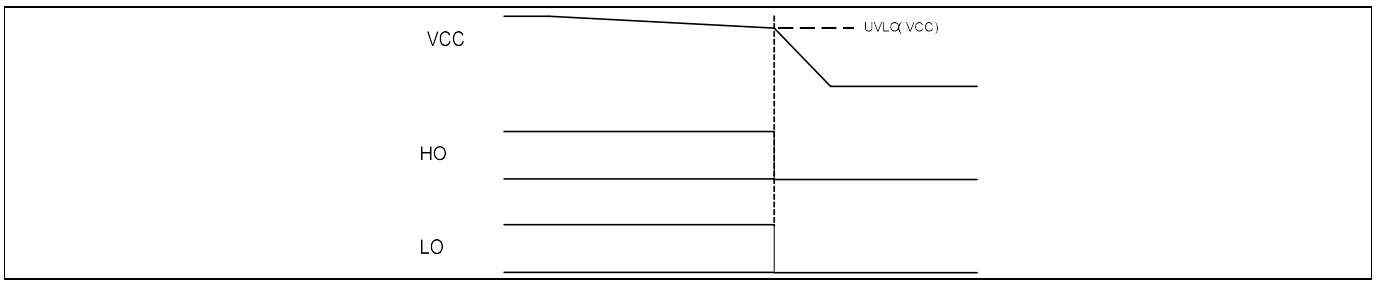

Figure 47 MA5302MS UVLO Timing Chart

14 Package details

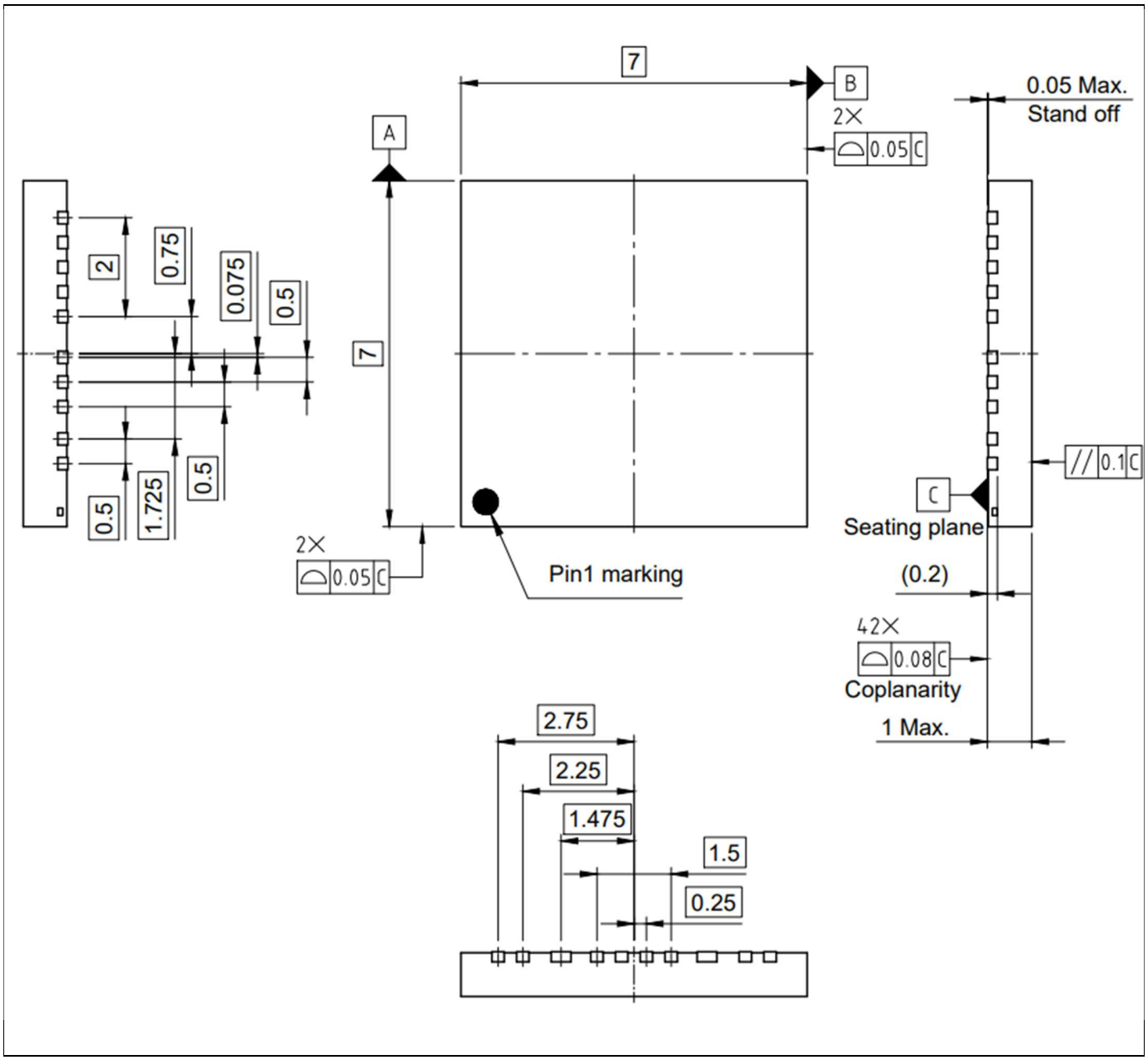

Figure 48 Package details

All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⇹]
Drawing according to ISO 8015, general tolerances ISO 2768-mK

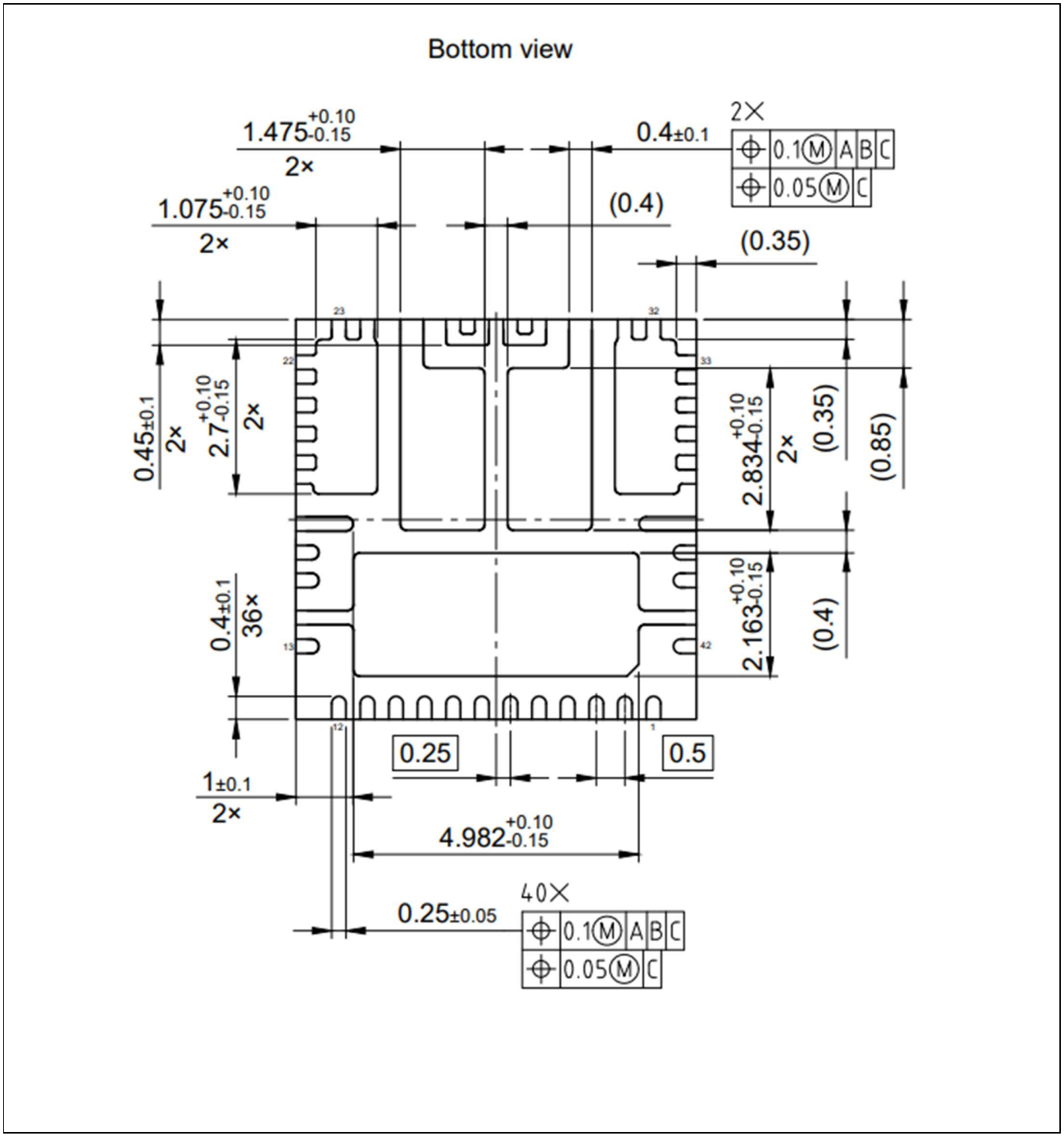

Figure 49 Package details; Bottom metallization detail view

All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⇹]
Drawing according to ISO 8015, general tolerances ISO 2768-mK

15 Board mounting, part marking, and ordering information

Reliability of products in the PQFN package is subject to the board mounting process. The Soldering process is critical. Refer to Application Note AN-1170 Audio IC Board Mounting Application Note for specific footprint design and soldering methods.

Device outline

Figure 50 shows the outline for these devices. The relative pad positions are controlled to an accuracy of ±0.050mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

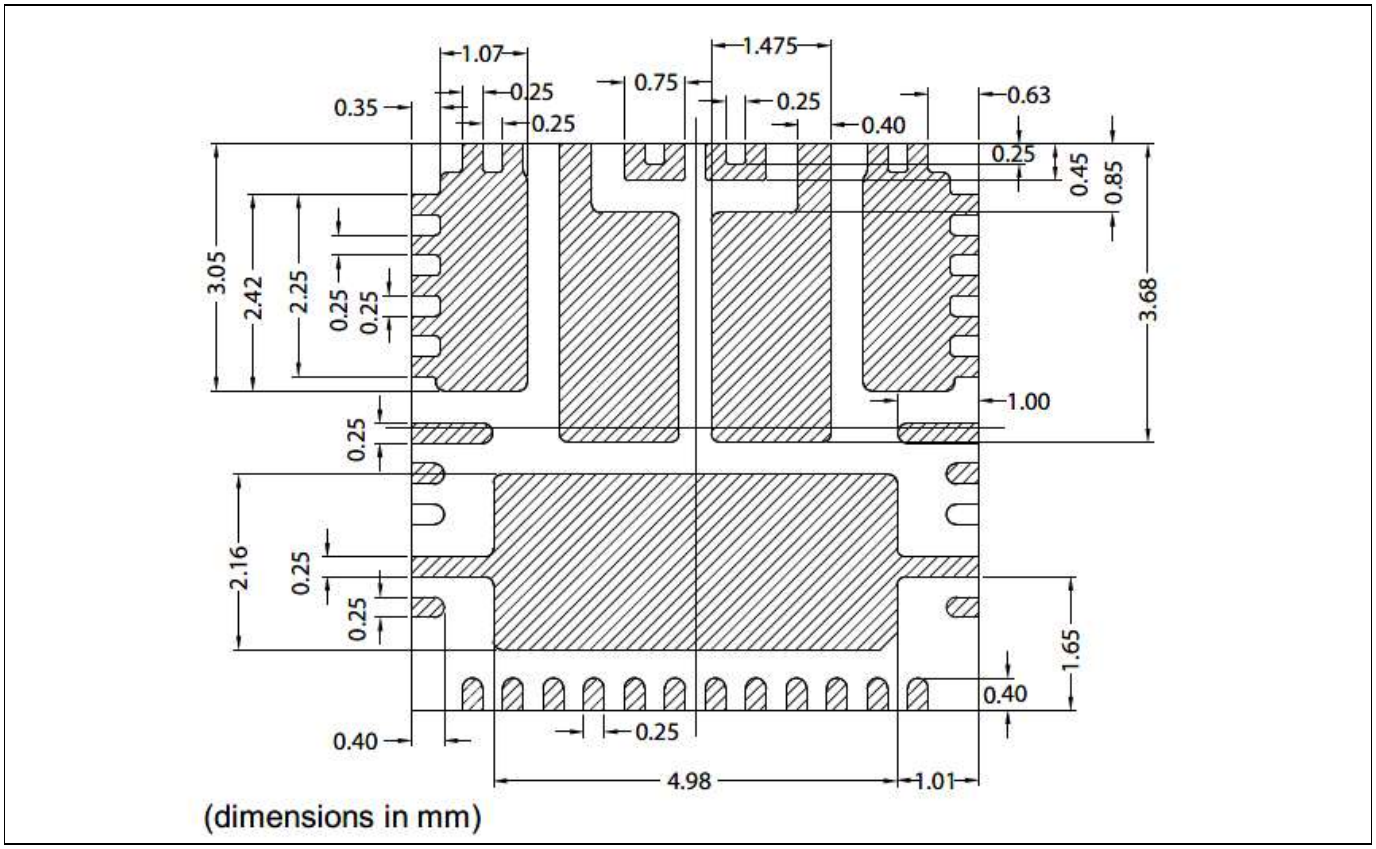

Figure 50 42-lead 7x7 device outline

Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure 51 and Figure 52

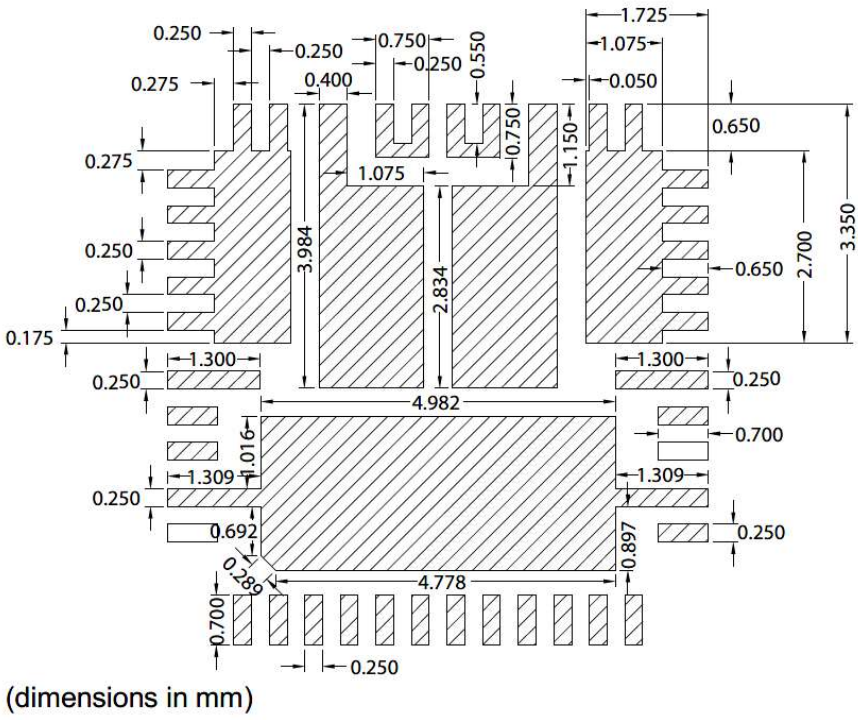

Figure 51 42-lead 7x7 substrate /PCB layout_1

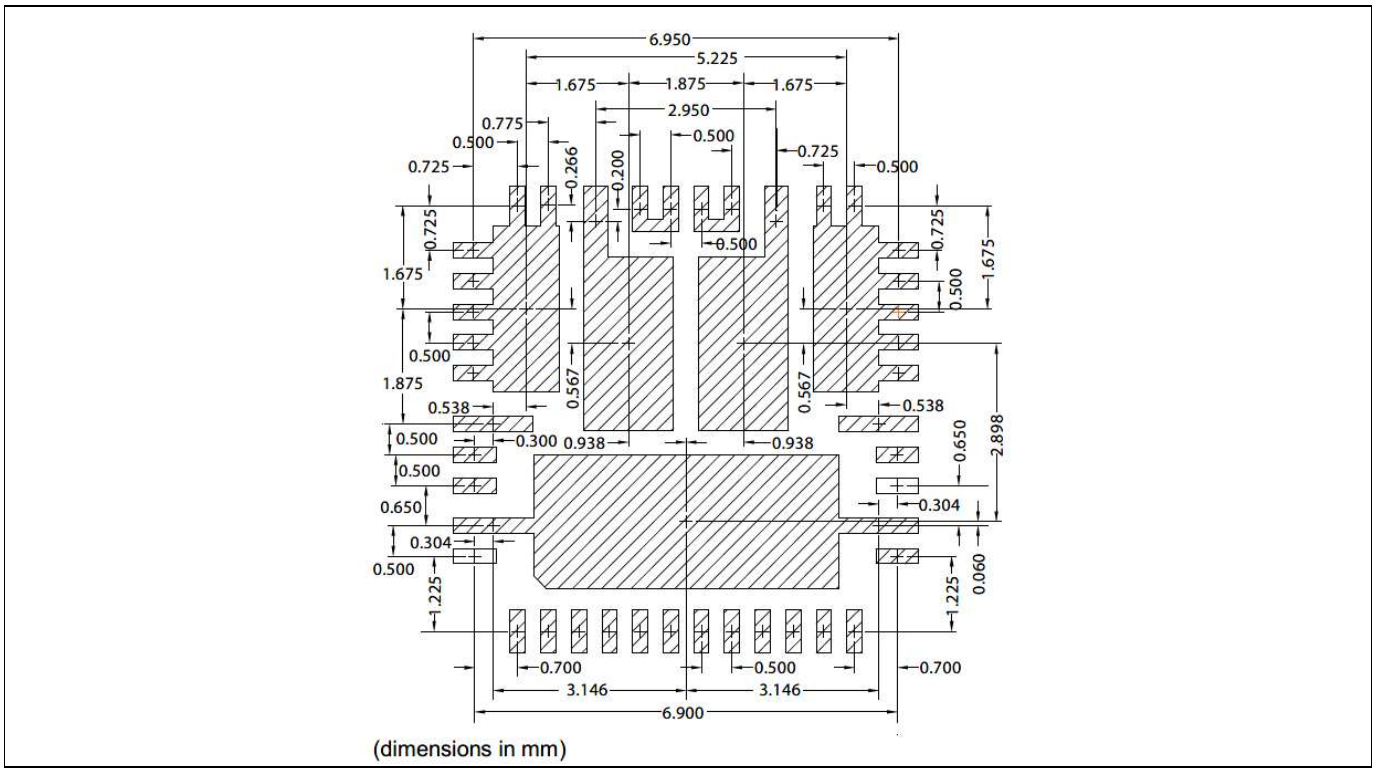

Figure 52 42-lead 7x7 substrate /PCB layout_2

Stencil Design

Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure 53-55.

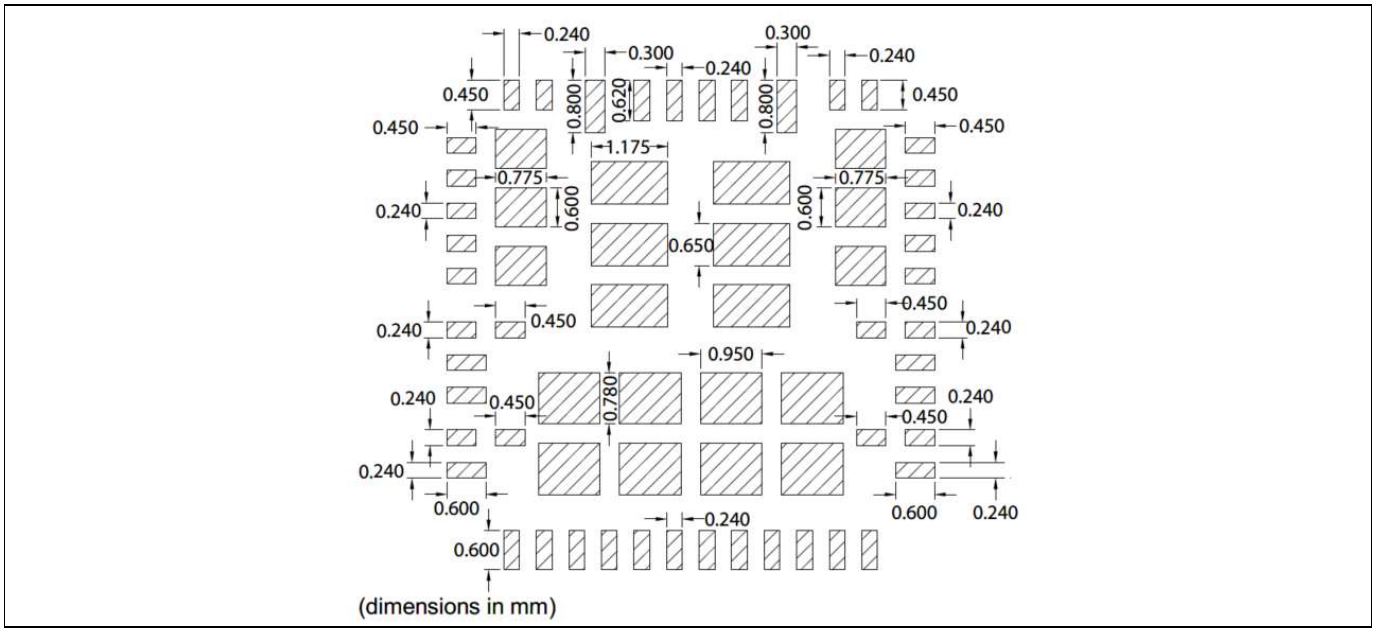

Figure 53 42-lead 7x7 stencil design_1

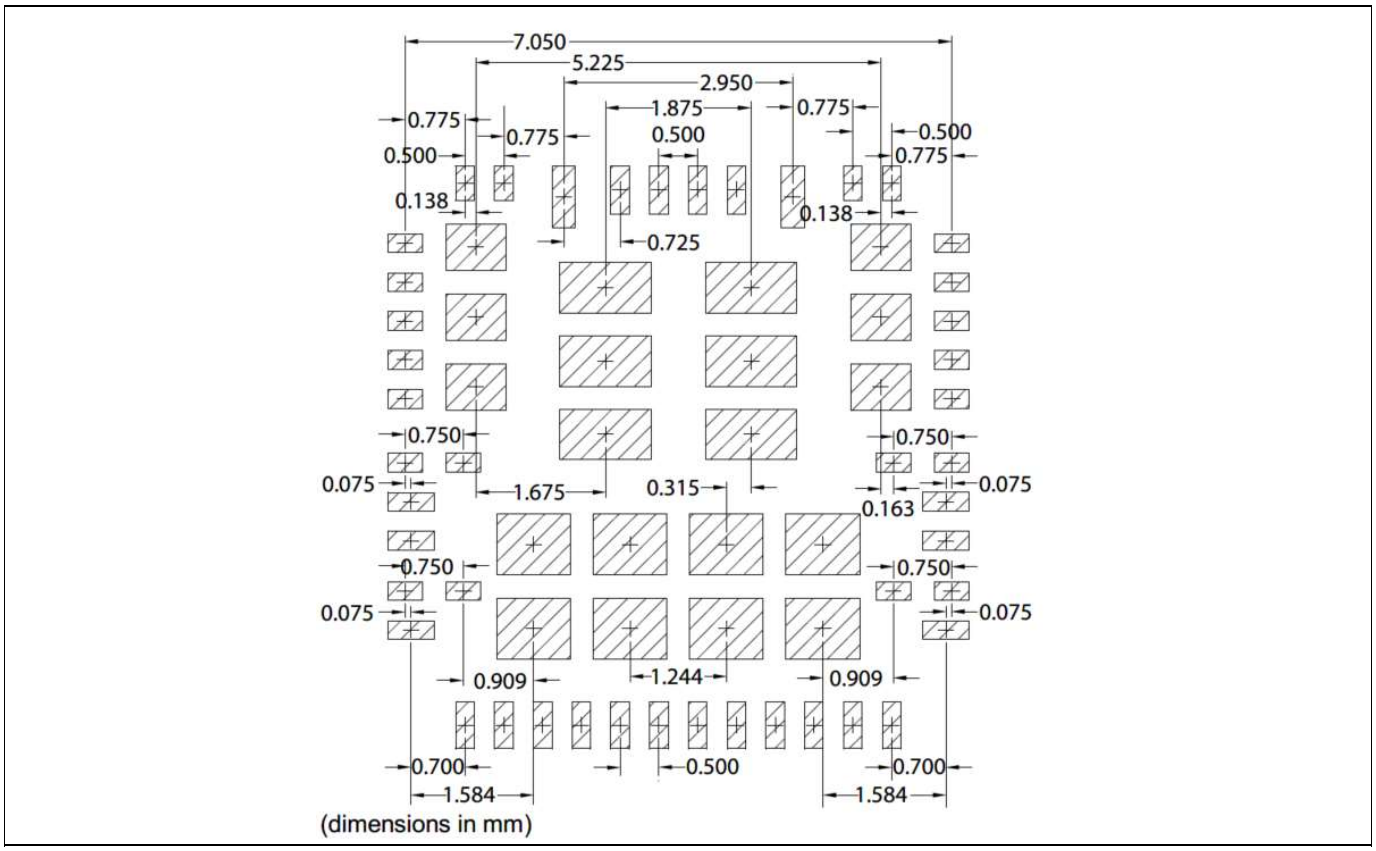

Figure 54 42-lead 7x7 stencil design_2

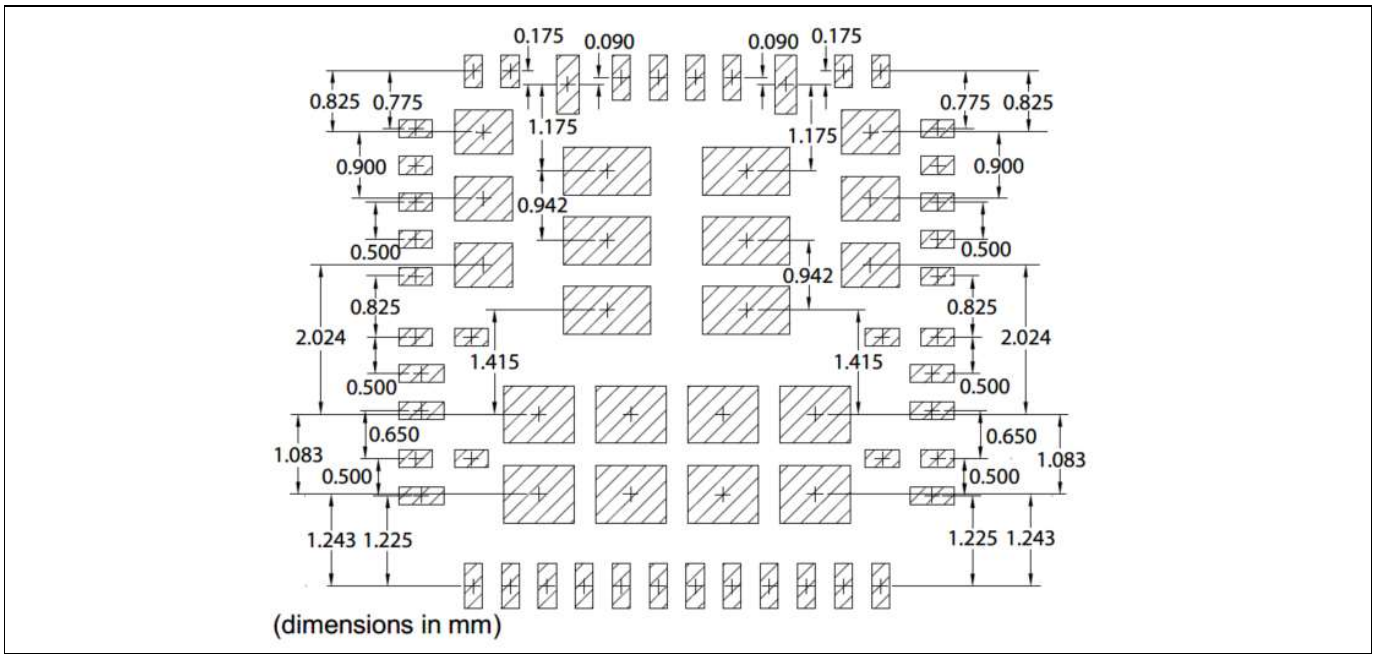

Figure 55 42-lead 7x7 stencil design_3

Note: This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses. All soldering conditions are necessary to ensure reliability. More details please refer to Application Note AN-1170 Audio Power Quad Flat No-Lead (PQFN) Board Mounting Application

Part marking

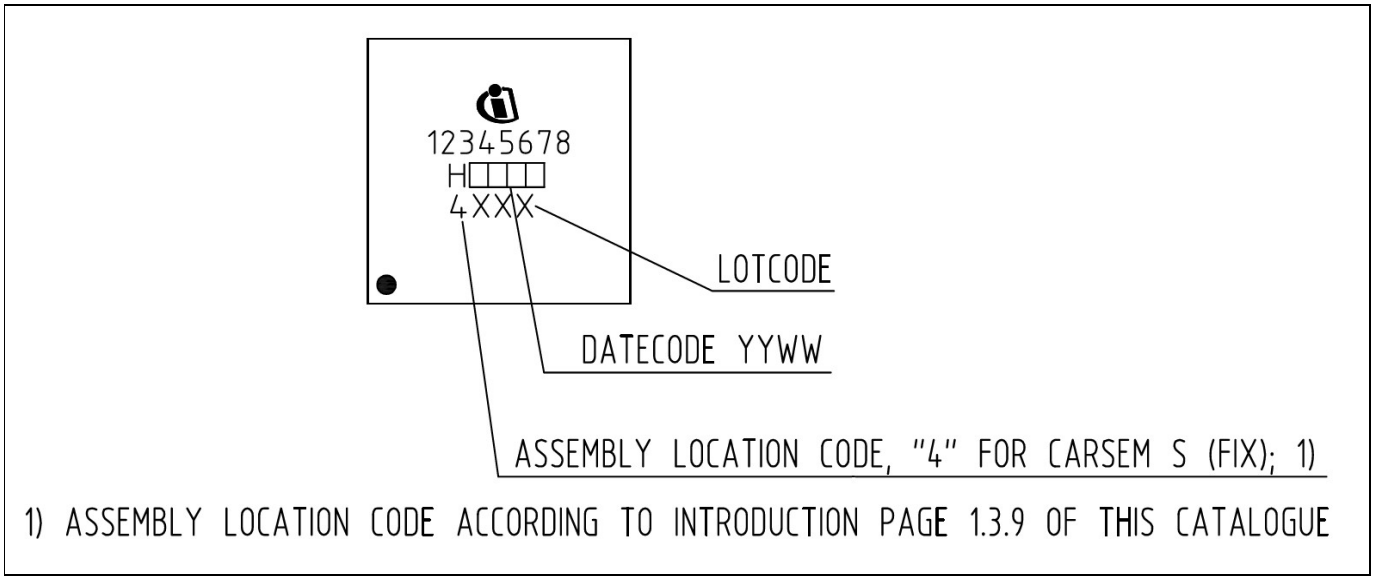

Figure 56 Part marking

Ordering information

Base part number	Package type	Standard pack		Complete part number
		Form	Quantity	
MA5302MS	PQFN42 7x7mm	Tape and Reel	3000	MA5302MS

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Edition 2022-02-07

Published by

Infineon Technologies AG

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Revision history

MA5302MS

Revision 2025-11-03, Rev. 2.3

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2023-10-23	Release of final version
2.1	2023-11-21	Editorial Edits
2.2	2024-11-11	Section 7 figure updates
2.3	2025-11-03	Added MERUS trademark

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