Loss-optimized active neutral-point clamped inverter in a low-inductive power-module design

Andressa C. Schittler, Christian R. Müller
Infineon Technologies AG, Germany

Corresponding author: Andressa C. Schittler, andressa.colveroschittler@infineon.com

Abstract

The ANPC topology is becoming the dominant solution in solar applications due to its increased flexibility with respect to modulation strategies and consequently to the energy flow. Combining the advantages of 1200 V CoolSiC™ MOSFET technology with 950 V TRENCHSTOP™ IGBT7 in a low-inductive power-module design, a new ANPC inverter is implemented in an Easy3B package. This solution prevents parasitic effects such as IGBT forward recovery, and allows higher switching speed by reducing the stray inductance in the main commutation loop. Consequently, the system-power density increases, while less sophisticated modulation strategies can be utilized.

1 Introduction

Within the last few years, the active neutral-point clamped (ANPC) topology is becoming the dominant solution in solar applications due to its increased level of flexibility with respect to modulation strategies, e.g. pulse-width modulation (PWM), and, thus, power factor control and energy flow [1]. Two main approaches can be identified. In the first case, fast-switching devices are implemented close to the inputs, and conduction-loss optimized devices close to the output. In the second case, the fast-switching devices are used close to the output and, for all other switches, conduction-loss optimized low static loss devices are utilized [1], [2].

A trend is being observed in the solar market towards 1500 V system voltage in power plants, due to their higher energy-processing capability [3] and the need to withstand grid faults as LVRT (low-voltage ride through) and HVRT (high-voltage ride through) [4], [5].

At the same time, fast-switching power-semiconductor devices mainly focus on applications like solar because an increase of switching frequency enables high power density, and reduces the effort with respect to power filters.

Aiming the 1500-V solar market, there are two different approaches at the device level if 3-level inverters are used: on the one hand, highly optimized Si-based devices such as 950 V TRENCHSTOP™ IGBT7 and RAPID diodes have been introduced, which allow application-specific improvements in terms of efficiency [6]. On the other hand, wide bandgap technologies such as 1200 V CoolSiC™ MOSFET are established and enable fast switching, which in combination with a low-inductive setup, reduce switching losses.

This work is an extension of [2], where three different ANPC variants have been presented and analyzed, focusing on the comparison between PWM 1 and PWM 2. In this paper, a hybrid-based, low-inductive power-module design for 1500 V PV inverter will be presented, utilizing optimized power semiconductors for each commutation path, operating in active and reactive power. The disadvantages of each modulation strategy are thus minimized, and an overall performance increase is expected at a very promising cost-performance ratio.

2 Layout optimization as key factor

During the design phase of a power module, a deep understanding of application requirements is essential to provide an optimized solution. One key factor is to reduce module stray inductance to enable the usage of fast-switching devices, and to lower switching losses. Figure 1 (a) shows the dependency of typical switching parameters like dv/dt during diode recovery and peak voltage V_{peak} during IGBT turn-off versus gate resistor R_G for different total stray inductances $L_{\sigma,total}$. As an example, in a 650 V topology, higher $L_{\sigma,total}$ leads to significantly larger values of dv/dt and V_{peak}, which might damage the devices if the switching speed is not limited by increasing R_G. Consequently, this higher R_G leads to increased switching losses of IGBT, and thus limits the system efficiency. Figure 1 (b) displays this impact for two scenarios: in the first one, R_G is reduced to

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a minimum for both $L_{\sigma,total}$ values shown. Here, it becomes clear that an optimization of $L_{\sigma,total}$ allows a reduction of IGBT losses and diode losses by 18% and 7%, respectively, with a maximum operating current of 200 A. Alternatively, with an optimized $L_{\sigma,total}$, the devices can be switched slower, and a maximum operating current of 300 A is achieved before device-critical operation conditions are reached. It is worth mentioning also in this case that the total losses of IGBT and diode are smaller compared to the non-optimized design.

3 Improved ANPC topology

According to the impact of $L_{\sigma,total}$ on the switching losses, it is clear that highest efficiency and system performance are reached only if an optimized power-module design together with the most appropriate semiconductor combination are used.

Figure 2 gives an overview on the existing ANPC solutions. In solar applications, variants A and D are widely used. Variant A uses fast-switching Si devices in the main commutation path, and SiC MOSFETs are utilized as main switches in variant D. On the one hand, variant A is less expensive but generates higher switching losses for the same output power, and thus is less efficient compared to variant D. On the other hand, the commutation path of variant D is significantly longer compared to variant A. Hence, limitations with respect to maximum switching speed have to be taken into account. In addition, forward-recovery losses have to be considered for variants C and D as well; an effect that is not present in variants A and B [2].

To overcome these disadvantages, variant B is proposed in this paper, which consists of a hybrid combination of SiC MOSFETs, SiC Schottky diodes, fast-switching Si-based IGBTs close to the inputs, and conduction-loss optimized IGBTs close to the output. This setup features an advantageous design with very low $L_{\sigma,total}$ [3], and consequently enables switching of SiC MOSFETs at higher speeds. In addition, IGBT forward-recovery losses are prevented by design, which ultimately results in minimized overall losses. The usage of SiC Schottky diodes guarantees minimum diode-recovery losses during regular operation at the same time.

During LVRT operation, the fast-switching Si-based IGBTs provide a perfect trade-off between cost and performance; in turn, usage of SiC MOSFETs in the LVRT commutation path is not required. If HVRT failure occurs, the current will flow through the SiC MOSFETs body-diode or synchronous rectification can be implemented. Another possibility is to implement additional Si diodes in parallel to the SiC MOSFETs, as the state-of-the-art for the realization with Si IGBTs (Variant A).

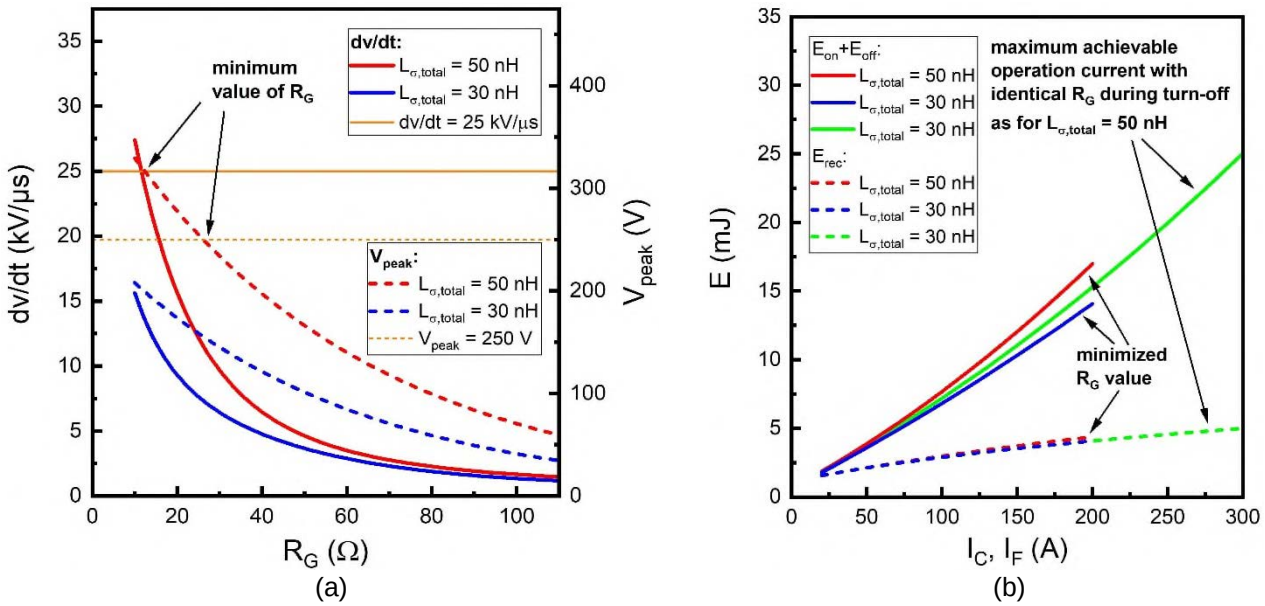

Fig. 1: Characteristic switching parameters dv/dt and V_{peak} versus gate resistor (a) and switching losses versus device current (b) for different stray-inductance values. For this comparison, 400 A fast-switching, 650 V TRENCHSTOP™ 5 and 225 A emitter-controlled diodes were used. V_{peak} and dv/dt were determined at I_C = 200 A and I_F = 20 A, respectively, at T = 25 °C.

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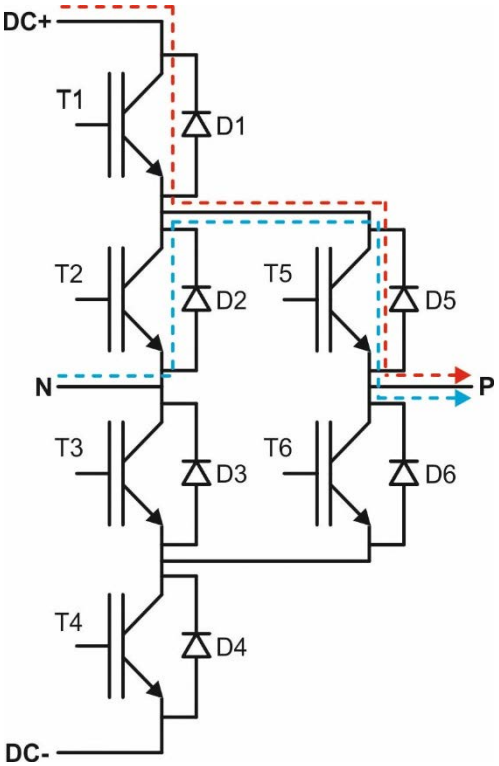
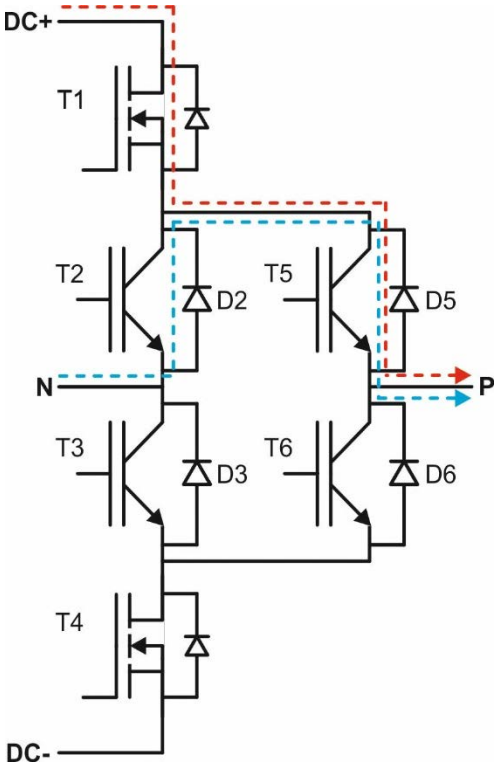
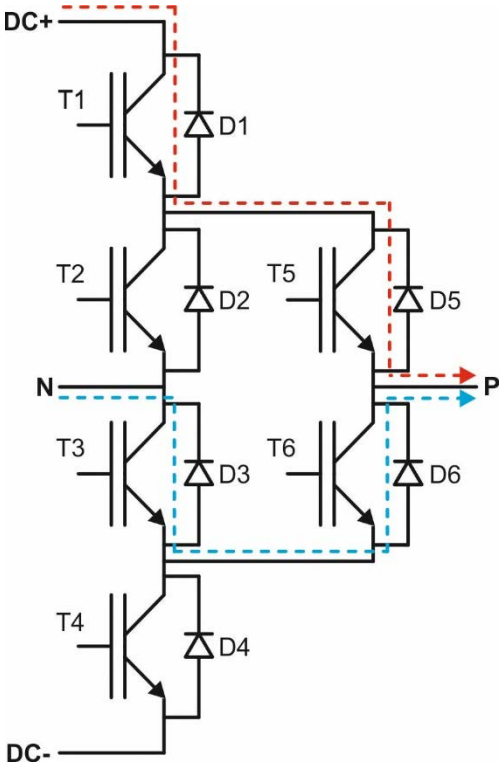


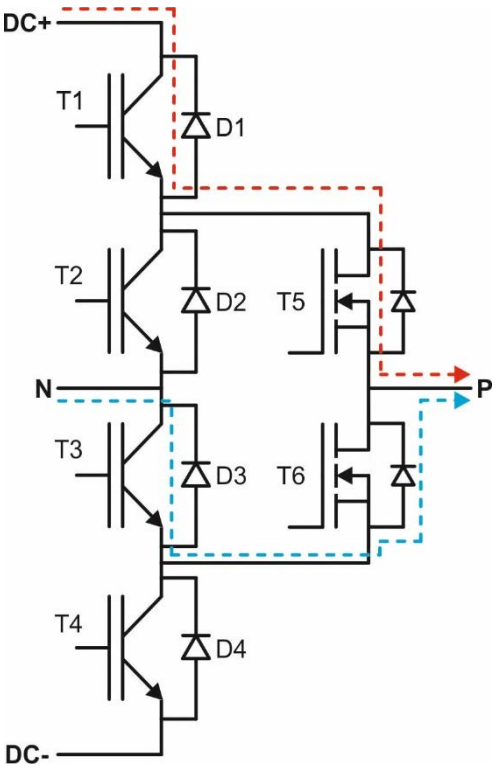
(a) Variant A, PWM 1: IGBT-based ANPC



(b) Variant B, PWM 1: Si-SiC-hybrid ANPC



(c) Variant C: PWM 2 IGBT-based ANPC



(d) Variant D, PWM 2: Si-SiC-hybrid ANPC

Fig. 2: ANPC Variants with their respective main commutation loops indicated for I and V > 0.

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3.1 Performance comparison of PWM 1 and PWM 2 topologies

As presented above, the improved ANPC topology (variant B) provides benefits in terms of usability and efficiency, which is confirmed by Figure 3. As a first example, a 140 kW 3-phase inverter is used (RMS output current = 120 A).

Figure 3 (a) shows a comparison of the total semiconductor losses for the four ANPC variants from Fig. 2. The losses on the active switch (T1/T4 for PWM 1 and T5/T6 for PWM 2) are presented in Fig. 3 (b).

Variant A is the ANPC where the fast-switching devices (T1/T4) are 950 V TRENCHSTOP™ IGBT7 and PWM 1 would be implemented. Here Si or SiC diodes can be implemented in D2/D3, with the latter option being more appropriate in terms of lower switching losses.

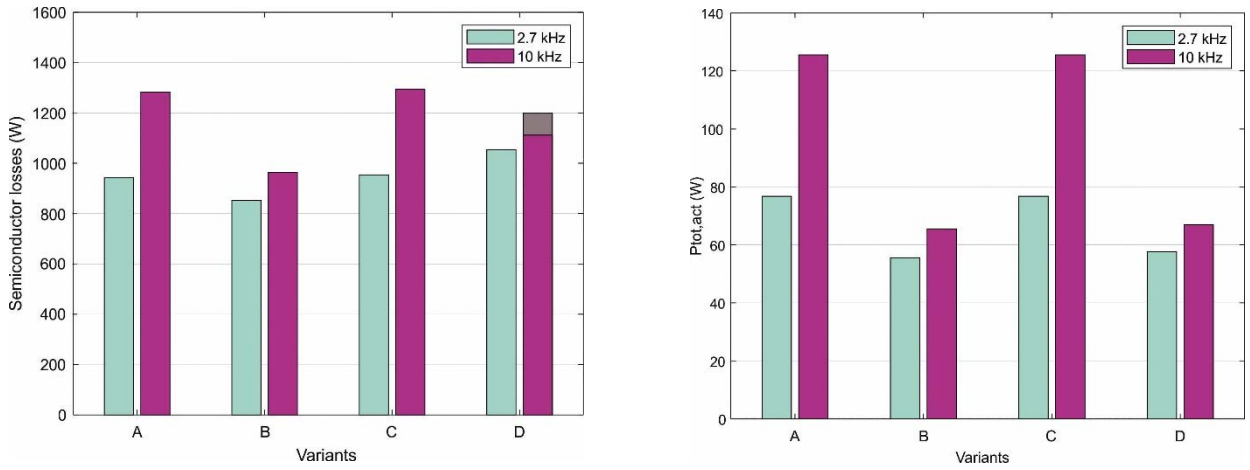
Variant B is proposed in this paper, where the fast-switching devices (T1/T4) are 1200 V CoolSiC™ MOSFETs. It is also implemented with PWM 1.

Variant C is shown for comparison, where the fast-switching devices (T5/T6) are 950 V TRENCHSTOP™ IGBT7 and PWM 2 would be implemented. In this case, due to an additional IGBT in the main commutation loop, forward recovery effects from this component also appear during the commutation of T5/T6. The forward recovery is responsible for increasing the overvoltage of T5/T6 and, consequently the turn-off losses. Such increase of the overvoltage can lead to a limitation of the switching speed, which leads to more turn-off losses if R_G has to be increased.

Variant D is an optimized and more widely used version with PWM 2, as 1200 V CoolSiC™ MOSFETs are implemented [7]. Also in this case, the switching losses are influenced by the additional elements in the commutation loop, which will affect even more the turn-off losses, due to the higher sensitivity of these losses regarding the overvoltage. If there were no forward recovery losses, the total semiconductor losses would be what is shown in violet. However, these losses occur (visualized as additional losses on top; exemplarily only for 10 kHz), and they lead to an increase of about 20% on the total semiconductor losses, depending on the operation point and/or switching frequency.

It is clear that the total losses of variant B are smaller than those of variants A, C and D. This is directly related to the implementation of SiC MOSFETs and SiC Schottky diodes.

The fast switching enabled by the 1200 V CoolSiC™ MOSFETs and the near absence of forward recovery lead to less power losses at the system level. Consequently, variant B might be operated at higher switching frequencies allowing an additional reduction of power-filter effort. A more detailed investigation of variants A and B is presented in the next section.



(a) (b)

Fig. 3: Comparison among PWM 1 and PWM 2 ANPC PWM patterns. Variants A and C are Si-based. Variants B and D are hybrid-Si-SiC. (a) Total semiconductor losses versus ANPC variant for two switching frequencies; (b) Total losses at the active switch versus ANPC variant (f_{sw} = 10 kHz)

3.2 Improved ANPC topology with PWM1

Based on experimental results on module level, the 3-phase ANPC inverter with variants A and B have been simulated in PLECS.

Table 1 shows the components built up on each module variant (same implemented currents as shown in [6]), and Fig. 4 illustrates the main input and output pins of the ANPC implementation in the Easy3B package.

Variant B has the same area covered with CoolSiC™ MOSFETs as variant A has with TRENCHSTOP™ IGBT7, optimized for fast switching, at T1/T4.

At turn-on, both variants A and B have similar dv/dt for $R_{G,on}$ = 5 Ω, and in the first example, the same R_G is used for turn-on and turn-off.

Firstly, both variants are compared at identical operation conditions, i.e., same R_G. According to Fig. 5 (a), at an RMS output current of 120 A, variant B (R_G = 5 Ω) shows around 2% fewer losses at 2.7 kHz, 3% fewer losses at 5 kHz, and 5% fewer losses at 10 kHz compared to variant A. However, this does not represent typical application conditions. In the application, each variant will be operated with an optimized R_G.

Secondly, in this comparison, variant B is operated with an improved R_G, i.e., R_G = 2 Ω. By this optimization, around 10% fewer losses are achieved at 10 kHz compared to variant A.

If the setup does not allow variant A to be switched at 5 Ω due to high V_{peak}, the $R_{G,off}$ has to be increased to, e.g., 10 Ω. In this case, variant B with R_G = 2 Ω provides up to 20% fewer losses compared to variant A.

If the RMS output current is increased to 150 A, the conduction losses become more relevant in comparison to the total semiconductor losses, as shown in Fig. 5 (b). In general, this results in an advantage for variant A as bipolar Si-based switches typically provide lower conduction losses at a given current than unipolar SiC-based switches. This means that if the setup layout is optimized and suitable for operation at maximum switching speed, variant A with low R_G (in this case $R_{G,off}$ = 5 Ω) can be utilized and still provides nearly

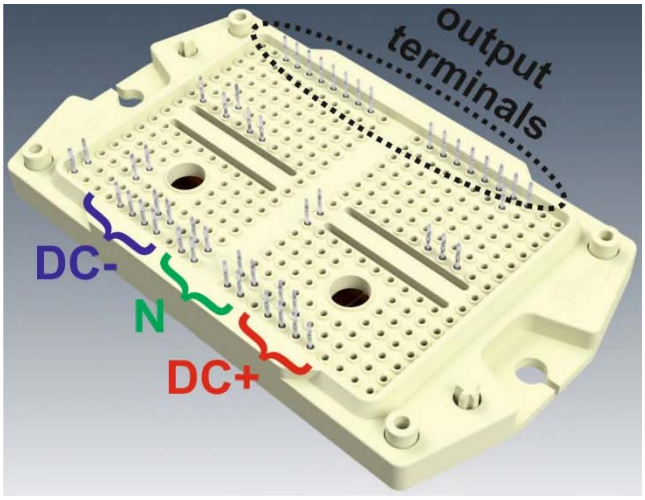


Fig. 4: ANPC implementation in Easy3B package, with main nodes highlighted.

the same losses as variant B. Variant A would then have much likely better cost-benefit than variant B.

In reality, this is rather untypical. Whereas the turn-off of a SiC MOSFET can be easily controlled by R_G and, thus, V_{peak} is directly affected, IGBTs provide an intrinsically controlled turn-off [8]. Thus, V_{peak} is not controlled by R_G in the intrinsic turn-off regime, and, consequently, a controlling of V_{peak} by R_G occur only for large RG values. So, if a limitation of switching speed is required during turn-off, this changes the situation significantly. Whereas variant B can be operated with R_G = 2 Ω and still provides the low losses, variant A has to be slowed down during turn-off with $R_{G,on}$ = 5 Ω and $R_{G,off}$ = 20 Ω. This leads to a remarkable increase of the total semiconductor losses and, finally, to total losses that are slightly higher than for variant B.

Figure 6 shows the turn-on losses versus dv/dt, which is directly controllable by $R_{G,on}$. Because both variants use the same SiC Schottky diodes configuration, the overall appearance of turn-on losses versus dv/dt is similar. The observed offset between both curves is attributed to the different di/dt values of both variant during turn-on at identical operation conditions.

The turn-off losses as a function of the di/dt are shown in Fig. 7. While the SiC MOSFETs can be

Table 1: Description of variants A and B

Variant	T1/T4	D2/D3	T5/T6
A	TRENCHSTOP™ IGBT7, optimized for fast switching	1200 V CoolSiC	TRENCHSTOP™ IGBT7, optimized for low conduction losses
B	1200 V CoolSiC™ MOSFET	1200 V CoolSiC	TRENCHSTOP™ IGBT7, optimized for low conduction losses

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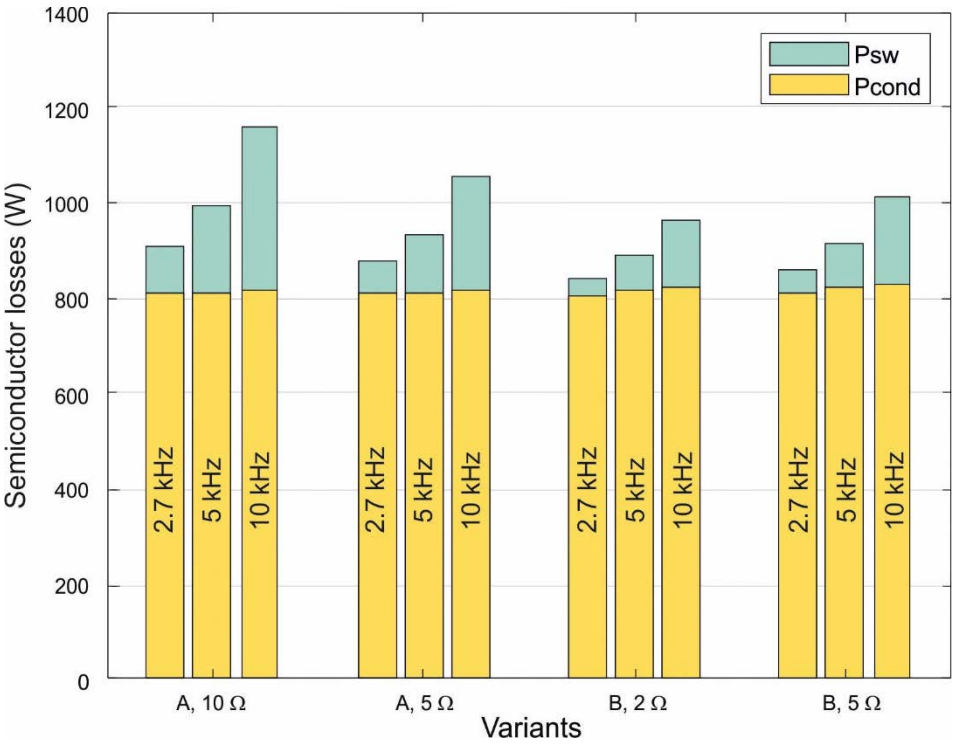
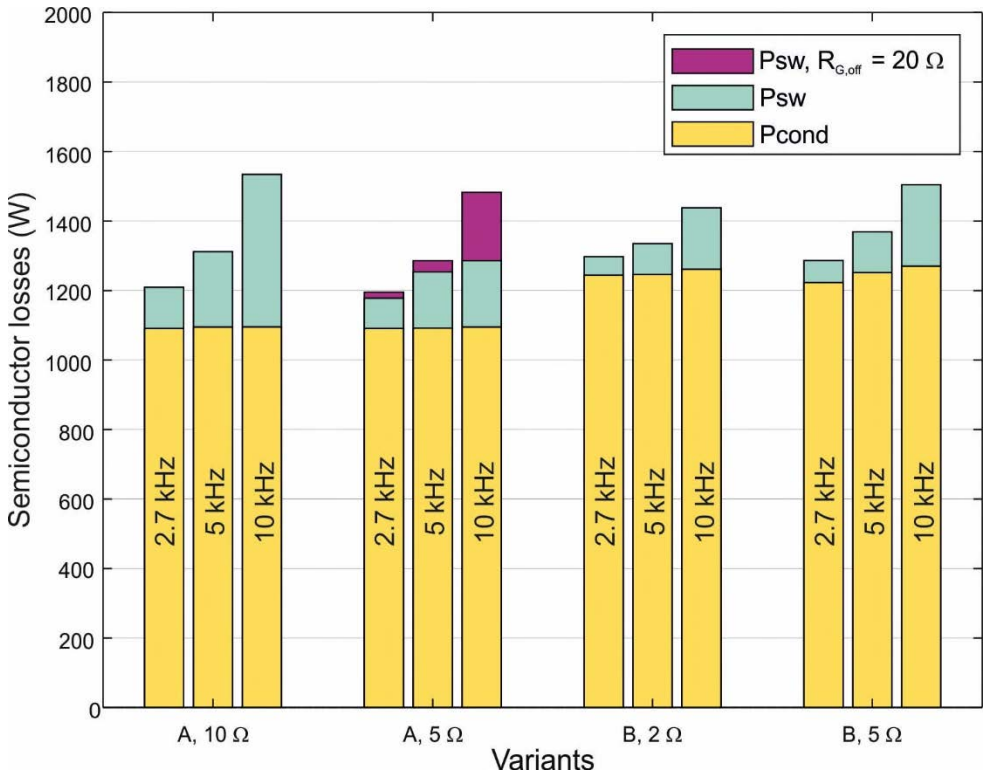


(a) RMS Output current = 120 A



(b) RMS Output current = 150 A

Fig. 5: Comparison of Variants A and B with different switching speeds, different switching frequencies and different RMS output currents, (a) 120 A, (b) 150 A

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controlled within a wide range only by changing the $R_{G,off}$, the IGBTs are limited to a maximum di/dt and can only be controlled in a limited area due to their intrinsic turn-off [8]. Focusing on turn-off, due to the MOSFET controllability, even lower switching losses can be obtained with variant B if RG is decreased.

4 Conclusion

In this paper a comparison between two ANPC variants working with PWM1 has been presented, with the goal of finding the optimized version of this inverter topology for a defined output power.

A hybrid-based, low-inductive power-module design for 1500-V PV inverter was introduced, utilizing optimized power semiconductors for each commutation path, operating in active and reactive power. The disadvantages of each modulation strategy are thus minimized, and an overall performance increase is expected at a very promising cost-performance ratio.

For RMS output currents up to 150 A, it has been shown that variant B (with CoolSiC™ at T1/T4) is the most promising choice in the Easy3B package, reaching up to 20% fewer losses if compared to variant A using fast-switching IGBTs.

Bipolar Si-based switches typically provide lower conduction losses at a given current than unipolar SiC-based switches. Consequently, for currents higher than 150 A, the conduction losses become dominant if compared to the total semiconductor losses, and the advantages of variant B become less significant.

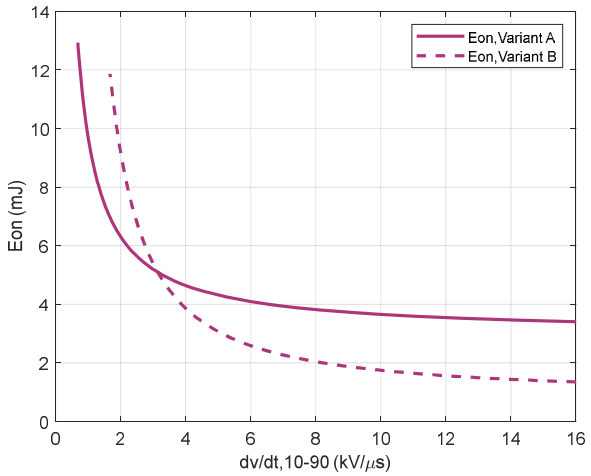

Fig. 6: Turn-on losses as a function of dv/dt for variants A and B. I_C = 200 A, T = 125°C.

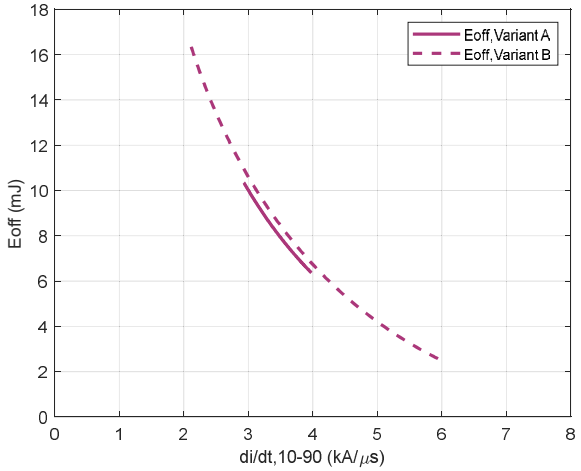

Fig. 7: Turn-off losses as a function of di/dt for variants A and B. I_C = 200 A, T = 125°C.

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