Frequently Asked Questions

Product Name: System Basis Chips (SBCs) **Date:** September 2018
Application: Automotive ECUs **Datasheet:** TLE94x1(-3)ES
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Lite SBC

Question 1: Chapter 3	What's exactly means **n.c.** pin?
Answer:	**n.c.** pin means "not connected pin". It is a high impedance pin and internally not bonded to the chip. These pins can be left floating. It is recommended to connect to GND to improve thermal behavior.
Question 2: Chapter 3.3	How shall I connect the unused pins?

Answer:	Please refer to the following recommendations:
	• WK/VSENSE: connect to GND and disable WK input via SPI
	• CANH / CANL / TXDCAN / RXDCAN: leave open
	• FO/GPIO: leave open or connect to GND
	• INTN, RSTN: leave open
	• TEST:
	  ○ To activate SBC Development Mode, connect to VCC1 during power-up
	  ○ For normal operations, leave open or connect to GND
	• VCAN: connect to VCC1
	• GNDCAN (Pin 22): connect to
	• VCC2: leave open and keep disabled
	• VCP: leave open

Question 3: Chapter 4.1	What does this mean: "VCC2 is short-to-battery protected"?
Answer:	Regulators with a maximum output voltage rating less than the battery voltage (e.g. 5V) will be damaged in case of a short to the battery. The VCC2 output pin of the Lite SBC can withstand a voltage up to 28V, and temporarily up to 40V for load dump. Therefore this SBC will not be damaged even if the output pin is shorted to the battery (or to GND over long cable).
Question 4: Chapter 4.4	What is the current consumption adder during cyclic sense in SBC Stop or Sleep Mode?
Answer:	The current consumption adder for cyclic sense (CS) with high-side switch (GPIO) in SBC Stop Mode can be calculated using following equation: $I_{Stop,CS}$ = 20µA + (400µA *ton-time/Tperiod). The same applies for SBC Sleep Mode.
Question 6: Chapter 4.4	Is "the VCC2 low power mode current consumption in SBC stop mode" the same to the VCC2 current consumption in SBC sleep mode?
Answer:	The VCC2 current is the same for SBC Stop and for SBC Sleep Mode. Please refer to (P_4.4.18) and (P_4.4.19). Note: You do not have to enable VCC2 for SBC Stop or SBC Sleep Mode for the CAN wake capable mode.

Frequently Asked Questions

Question 7: **Chapter 4.4**	What is the contribution of the watchdog operation to the SBC current consumption during SBC stop mode?
Answer:	Additional 20µA typ. is required at 25°C. For more details, please refer to the datasheet, (P_4.4.24) and (P_4.4.25).
Question 8: **Chapter 4.4**	What is the High-Side Switch (GPIO) current consumption value in SBC Stop Mode without cyclic sense?
Answer:	The difference on the HSS current consumptions with and without cyclic sense is that the current consumption in cyclic sense is reduced by the duty cycle (ton/Tperiod). See also the footnotes of the datasheet parameters (P_4.4.20 -23).
Question 9: **Chapter 5.1**	Is the transition from SBC Init Mode to SBC Normal Mode automatic, or do we have to send a SPI command?
Answer:	The transition from SBC Init Mode to SBC Normal Mode is triggered by **ANY** SPI command, sent by the microcontroller. A recommendation is to use the first watchdog trigger command, which is sent with the watchdog timing chosen. In this case no additional SPI command must be sent for entering the SBC Normal Mode.
Question 10: **Chapter 5.1.1**	What is the watchdog mode after power-up (window watchdog or time-out/standard watchdog?
Answer:	The default watchdog mode is time-out watchdog.
Question 11: **Chapter 5.1.1.2**	Do you have some recommendation for the sequence of initial settings?
Answer:	After the Power-On Reset (POR), the SBC is in SBC Init Mode. Then following actions are recommended: • Watchdog trigger and watchdog (WD) settings • Clear the POR bit for proper diagnosis • All other initializations of the SBC peripherals (CAN, FO/GPIO, WK/VSENSE, etc.) The actual sequence and timing of the commands depend on the application and other boundary conditions (e.g. microcontroller, drivers, functional safety requirements, etc.).
Question 12: **Chapter 5.1.4**	SBC Stop Mode is used for our application in low-power mode of the ECU. There is a concern to accidentally enter SBC Sleep Mode (VCC1 OFF) by single point failure. Is there any suggestion to reduce this risk?
Answer:	One suggestion is to set a wake-flag as “1” and leave it intentionally (just after SBC initialization) because SBC Sleep Mode access is prevented when wake-flags are still set. One possibility would be following configuration after power-up: • Create an internal wake-event (TIMER_WU) from an unused timer (Timer 1 or Timer 2) using cyclic wake • Keep this bit set (do not clear in the register). Only then, set other wake sources before entering SBC Stop Mode. • In case other wake sources are set and the register needs to be cleared, the procedure should be repeated. As explained in Chapter 5.1.4, to enter SBC Sleep Mode successfully, all wake source signalization flags from WK_STAT_0 and WK_STAT_1 must be cleared. A failure to do so results in an immediate wake-up from SBC Sleep Mode (going via SBC Restart to Normal Mode).
Question 13:	What is the output voltage and the current capability of VCP?

Frequently Asked Questions

Chapter 5.3	
Answer:	Output voltage of VCP: • The output voltage of VCP depends on the input voltage and the VCP current and is about double the input voltage (P_5.3.1/2/3). Current capability of VCP: • VCP is designed to drive n-channel MOSFET transistors with a current of min. 200µA and max. 1200µA (P_5.3.4).
Question 14: **Chapter 6.2**	Is it possible to increase the current limit of VCC1 for large peak loads?
Answer:	The default typical value is 0.75A, though it is possible to set the typical current limit to 1A through SPI (ICC1_LIM_ADJ).
Question 15: **Chapter 6.2.4**	What are the recommended inductor/capacitor values for VCC1 as DC/DC (TLE947x)?
Answer:	It is recommended to use an inductor of 10µH and a low ESR capacitor of 22µF. Values beyond those of Table 15 can be used, but stability must be checked.
Question 16: **Chapter 5.3**	When VCP is used to control a MOSFET, it is possible to turn it on and off?
Answer:	Yes, however if the CFG_LOCK_0 bit is set, it must be cleared before. If VCP shall be switched off in SBC Stop, Sleep, restart or Fail-Safe Mode, it must be done before entering the respective mode.
Question 17: **Chapter 8.3**	What is the internal link between the CAN transceiver and VCC2?
Answer:	The CAN transceiver and VCC2 are independent. CAN is supplied by the dedicated VCAN supply input pin. Any 5V supply can be used (e.g. VCC1, VCC2 or an external voltage regulator).
Question 18: **Chapter 8.4**	Can we disable VCC2 in SBC Stop Mode while keeping the CAN transceiver in wake capable mode?
Answer:	An internal supply derived from VS is active during CAN wake capable to supply the wake receiver. Therefore, VCC2 does not need to be active during SBC Stop or Sleep, i.e. it can be switched off during CAN wake capable mode.
Question 19: **Chapter 8.2.4**	How can the microcontroller detect a wake-up on CAN in SBC Stop Mode?
Answer:	There are two signalizations how a CAN wake-up is detected: 1. The INTN pin is pulled low for t_{INT}. 2. RXDCAN is pulled low until the CAN mode is changed via SPI. The microcontroller can use either signal as wake-up detection. Please refer to the datasheet Chapter 8.2.4 “CAN wake Capable Mode” for the details.
Question 20: **Chapter 8.6**	1. What max. voltage can be applied to the WK/VSENSE pin and how large is the current flowing into the pin? 2. Must the current be limited if a pin voltage of >40V is applied?
Answer:	1. The maximum voltage on the WK/VSENSE pin can be 40V (P_4.1.7). 2. In general, voltages of >40V are not allowed because of the break through voltage of the ESD diode. Since ESD diodes can withstand a high (>1mA) current only for a very short

Frequently Asked Questions

	period, an external capacitor of 10nF and a 10k series resistor are suitable to limit the pulse current into the pin (500 μA max).
Question 21: **Chapter 5.1.7**	1. Is there an internal pull-down resistor at the TEST pin? 2. Do we need to add an external pull-down for the productive application?
Answer:	1. Yes, there is an internal pull-down resistor (R_{TEST}) implemented at the TEST pin, which is activated only during the power-up phase of the SBC. It is used to detect, whether the SBC Development Mode shall be activated or not. The SBC Software Development Mode is entered, if the TEST pin is set and kept HIGH during SBC Init Mode. The voltage level monitoring is started as soon as VS > $V_{POR,r}$. The SBC Development Mode is configured and maintained, if the SBC Init Mode is left by sending any SPI command while TEST is HIGH. The Software Development Mode is NOT configured, if the TEST level is LOW for longer than t_{TEST} during the monitoring period. 2. After the power-up phase the internal pull-down resistor is disabled, if the SBC Development Mode has been entered successfully. Otherwise it stays connected.
Question 22: **Chapter 12**	Do VCC1 and VCC2 have an under-voltage detection feature?
Answer:	• VCC1: an under voltage pre-warning detection, a configurable under-voltage reset, a short circuit detection, and an over voltage detection are implemented. • VCC2: an under-voltage detection is implemented. An SPI bit is set, but no reset is generated Please refer to the datasheet Section 12.5 – 12.7 for further information.
Question 23: **Chapter 10.1**	What happens to VCC1, if VCC2 enters thermal shutdown and is turned off?
Answer:	There are independent temperature sensors for each voltage regulator and other power stages. Therefore VCC1 continues to operate independently from the VCC2 condition, as long as the temperature is below the thermal shutdown threshold of VCC1.
Question 24: **Chapter 10.2.4**	Would you provide the information on the VS min voltage to release reset (RSTN is L to H) surely during VS ramp-up?
Answer:	It depends on the load at VCC1 and is based on the following calculation (no load, default Vrt1): Vr_min = Vrt,f_min + Vrt,hys_min = 4.52V
Question 25: **Chapter 11.1**	How long is the reset pulse width for the WD time-out?
Answer:	The reset delay time (t_{RD1}) is typ. 2ms typ. In case of a watchdog trigger reset the RSTN pin is pulled low for this time. For other events, e.g. under voltage reset, the RSTN is pulled down for at least the 2ms but as long as VCC1 is below the reset threshold. *Note: A WD time-out can also end up in the Fail-Safe-Mode (see datasheet table 5)*
Question 26: **Chapter 11.3**	1. Are the SPI registers exactly the same among TLE9461/71 family? 2. What happens in case of programming a register associated to a non-available function?
Answer:	1. All members of the Lite-SBC family are fully software compatible between each other. 2. The respective control bits behave like other reserved bits, i.e. they read as '0' and are also tied to '0'. No control or configuration is possible. No SPI_FAIL bit is set.
Question 27: **Chapter 12.3**	A reserved bit in the configuration register has to be written as 0. Will it trigger a raise of SPI_FAIL flag, if programmed as 1?

Frequently Asked Questions

Answer:	Nothing will happen, when trying to write a '1' to a reserved bit because there is no real digital registers for reserved bits, The read back value is always '0' for reserved bits. The SPI_FAIL flag is not set.. *Note: For the details of the invalid SPI Commands leading to SPI_FAIL, please refer to the datasheet Chapter 13.2.*
Question 28: **Chapter 13**	Are there any internal pull-ups or pull-downs at SPI pins?
Answer:	• CSN pin: there is a pull-up resistor (40kΩ typ.) • SDI and CLK pin: each pin has a pull down resistor (40kΩ typ.). • SDO pin: there is no pull-up or pull-down resistor. It is a push-pull output stage. Please refer to (P_16.7.5) and (P_16.7.6).
Question 29: **Chapter 13**	What is the transition time for SBC mode changes triggered via SPI?
Answer:	The mode transition time is max. 6µs. Please refer to (P_16.7.23).
Question 30: **Chapter 3**	Which pins have which internal structures?
Answer:	Please see datasheet chapter ***3.2 Pin Definitions and Functions***