Lighting the Way to Less Complex Electronic Ballasts

ICs targeted at electronic ballasts have become a key element of fluorescent lighting design as manufacturers look to simplify circuitry, reduce development time, improve efficiency and keep overall cost to a minimum. As a result, the variety of ICs available to lighting designers now ranges from simple self-oscillating half bridge drivers to highly integrated, low pin-count devices with comprehensive control features such as soft-start functionality and frequency control for preheat, ignition and run mode. Ongoing advances in semiconductor technology have also seen a growing number of integrated protection features, including both below resonance protection and over-temperature protection.

Until now, however, qualifying ballasts – those with power ratings higher than 25W in Europe and 40W in the US – still require a separate power factor correction (PFC) stage, with associated increases in component count, complexity and cost. At the same time, thanks to their slimmer form factor and higher efficiency, T5 HO (high-output) lamps are becoming increasingly popular. However, these create new challenges that demand further increases in component count and external circuitry.

T5 HO Lamp Challenges

The two key issues for engineers designing T5 HO lamp applications relate to ignition voltage and end-of-life (EOL) protection. Ignition voltage for such lamps increases significantly when the gas temperature is low. To ensure that the lamp ignites across a wide range of temperatures, traditional ballast control methods require that the overvoltage threshold is set high. And if it is set too high then the ballast over-voltage shutdown protection can be compromised.

Because of this, the ideal way to drive T5 HO lamps is to apply a constant-voltage ignition feature. During the sweep from the preheat to run frequency, the output voltage is sensed and compared with a preset threshold. Should the voltage exceed the threshold, an ignition regulation circuit increases the frequency slightly by pulsing the VCO voltage down. This cycle-by-cycle feedback will adjust the frequency each cycle, therefore limiting the amplitude of the output voltage to a high, constant level for a programmable time until either the lamp is ignited, or the circuit is shut down automatically protecting the lamp in the event of an over-voltage/over-current condition.

End-of-life protection becomes mandatory for T5 lamps because of their slim size, which means that the filaments are closer to the glass tube exterior. Because of this it is necessary to prevent the caps of the lamp from becoming too hot as the lamp reaches EOL. According to IEC standard 61347-2-3, the

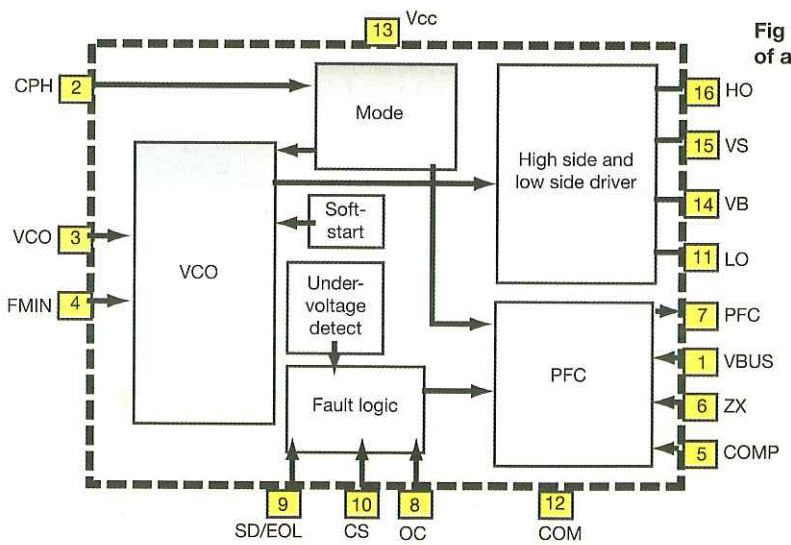

Fig 1 Key Functional Blocks of a Ballast Control IC

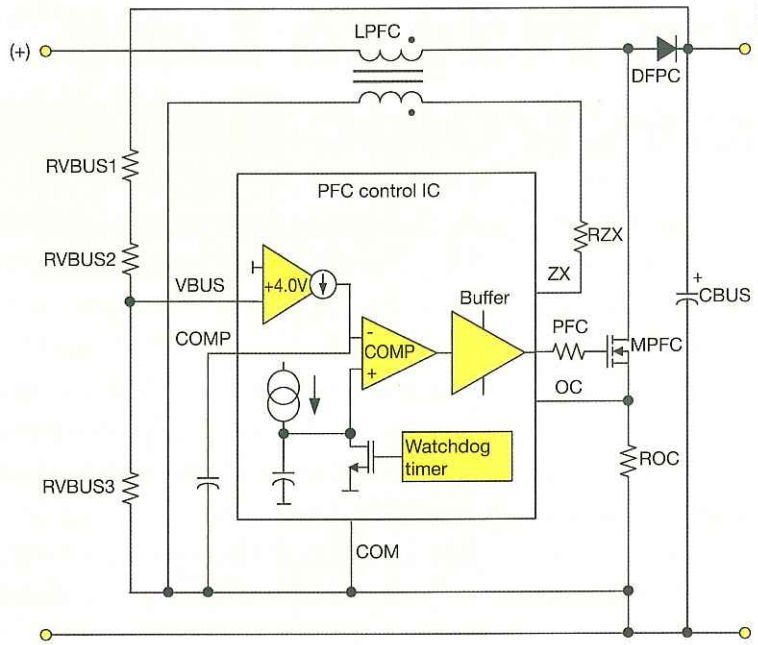

Fig 2 PFC Circuit Topology

T5 (and, indeed, T4) ballasts must pass at least one of three EOL tests to be qualified. To pass these tests – which include an asymmetric pulse test, asymmetric power detection, and an open filament test – traditional current or voltage sensing methods are inadequate. Therefore, new forms of protection are needed.

HVIC Technology

The ultimate goal for the designer is to be able to select a single device that addresses all of these control, PFC and protection requirements. The challenge of creating such a device lies in the integration of high-voltage driver functionality with CMOS-compatible, low-voltage capabilities. Fortunately, semiconductor processes such as the GEN5 high-voltage IC (HVIC) technology are helping to make these highly integrated devices a reality.

The Gen5 HVIC process allows improvements in device capabilities, tighter specifications, temperature stability, and the integration of previously unavailable features. High-voltage level-shifting and termination technology, for example, delivers 600V floating gate drivers and bootstrap diodes with high level of electrical over-stress protection and field reliability. Meanwhile the CMOS-compatible, low-voltage process enables monolithic integration of accurate analog references, control and feedback circuits, and comprehensive protection features. Finally, a wafer-level trimming technique ensures highly accurate critical design parameters that are independent of temperature and process variation. This trimming technique does not require additional pins on the package, making it particularly attractive for low-cost ballast control IC applications where the number of I/O pins is limited.

Single-Chip Device Implementation

Using the GEN5 technology, a fully integrated, fully protected 600V ballast control IC with an on-board PFC feature that is suited to T5 lamp requirements has been developed. Fig 1 illustrates the building blocks of such a device, which is supplied in a compact, 16-lead package. The IC has many programmable features including those for preheat time, preheat frequency, run frequency, and ignition ramp. Protection features are provided for half-bridge over-current, PFC over-current, lamp failure-to strike, and filament failures in addition to other protection features such as closed-loop ignition current regulation, DC bus under-voltage reset and an automatic restart function. The IC also features an integrated bootstrap diode, fixed internal 1.6μs half-bridge deadtime, voltage-controlled oscillator (VCO), end-of-life window comparator pin, lamp removal/auto-restart shutdown pin and an internal 15.6V Zener diode clamp on Vcc.

As Fig 1 illustrates, the heart of the ballast controller includes a VCO, the output of which is amplified and level-shifted to drive the half-bridge MOSFETs of the resonant converter. VCO frequency can be swept according to lamp driving requirements. Comprehensive protection circuitry and

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The Discrete Approach

The discrete approach to handling EMI typically takes the form of RC or LC filter networks using ceramic surface-mount components. The problem with this approach is that, as the number of discrete components in each network increases, so too does the likelihood of encountering quality issues. Solder joints for all the individual components have to be inspected, further adding to the cost and time needed for overall production. The individual size of discrete components is small, but when a network is required to counteract EMI, the overall PCB space increases. The biggest issue here is that the use of discrete components increases the chances of parasitics.

The purpose of EMI filters is to reject or take away signals or interferences generated by clock signals or data lines that may pollute mobile signals or frequencies. The frequencies at which special care is required with mobile phones are in the range of 1 to 2GHz; and most mobile phones and wireless networks operate within this range.

HiPAC Solutions

An existing silicon-copper technology for passive integration has been extended to integrate passive and active elements on a highly resistive Si-substrate. With this extended Si-technology, filters with low insertion loss and high harmonic suppression are also realized. A number of protection technologies that are optimized for different application frequencies have been implemented.

High-performance passives and actives on chip (HiPAC) are integrated solutions which provide system immunity to contact discharge of up to 15kV, exceeding the level-4 requirements specified in IEC61000-4-2. The HiPAC filters introduce low parasitics, providing superior filtering performance at frequencies of up to several GHz.

This kind of integrated solution allows customers to squeeze ESD/EMI protection into one chip with enhanced performance. The HiPAC also reduces board space usage. With fewer solder joints, reliability issues have also decreased, as well as the final bill of materials. This in turn enables the customer to benefit from cost savings. ■

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frequency regulation circuitry are also included in the ballast controller. The core of the PFC controller is a separate VCO regulated for the critical conduction mode (CCM) boost converter. A closed-loop control method yields the best power factor (PF) and minimum total harmonic distortion (THD). In order to design for a high-precision analog IC, a trimmed band-gap voltage reference circuit is applied. This circuit provides accurate threshold voltages for the VCO, protection circuits, and PFC controller.

Fig 2 illustrates the closed-loop topology of the integrated PFC controller, which requires just five pins to deliver the necessary functionality. Unlike the ballast controller VCO, the critical design consideration of the PFC oscillator is to ensure minimum THD by providing an adaptive on/off time for the PFC gate driver. The IC continuously compares the DC bus voltage to a target value, with the difference providing the input for regulation of PFC oscillator on-time. The on-time regulation loop operates with higher gain during preheat and ignition modes for rapid boost of DC bus level, and with lower gain in run mode for slower loop speed. PFC oscillator off-time is determined by the time it takes the inductor current to discharge to zero. The zero current level is detected by a secondary winding through an external current liming resistor. The IC compares the voltage level to internal voltage references (generated by band-gap voltage) to determine the beginning and end of off-time. The result is a system where the PFC oscillator is constantly regulating from a high frequency near the zero crossing of the AC input line voltage to a lower frequency at its peak. ■

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