

Getting Started - Infineon Designer

LITIX™ Power TLD5190

About this document

Scope and purpose

This document outlines LITIX™ Power **TLD5190** main features by means of its digital twin, referred as simulation model, in typical application setups aiming to be an easy, time efficient and cost reduction solution for exploring device capabilities and integration in complex applications.

Information covered in this document does not substitute datasheet content and shall be regarded as complementary to it. For a more precise description of the device and its features, please consult the datasheet.

Intended audience

This application note along with the simulation model itself offers an interactive solution targeted for anybody who aims to explore the functionality and “what if” scenarios for **TLD5190** device.

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1 LITIX™ Power TLD5190

The LITIX™ Power **TLD5190** is a synchronous MOSFET H-Bridge DC/DC controller with built in protection features. This concept of a synchronous and seamless buck-boost regulation provides a very efficient solution for circuits where the output (load) voltage is on the same level as the input voltage, e.g. in short chains with 2 to 3 high power LEDs or laser diodes connected to a 12 V electrical system.

The available online circuits are listed below:

- 12V Automotive LED synchronous H-Bridge topology with LITIX™ Power controller TLD5190 (input voltage ramping)
- 12V Automotive LED synchronous H-Bridge topology with LITIX™ Power controller TLD5190 (soft start PWM dimming)
- 12V Automotive LED synchronous H-Bridge topology with LITIX™ Power controller TLD5190 (slow switch)

[Click here to open the circuits.](#)

2 Simulation model features

- Perform transient simulations: observe and analyze transient device response to different stimuli. The number of stimuli and probes is unlimited.
- Measure the device electrical parameters in typical conditions with increased precision at small resolution (e.g. 100 ns/1 uV/1 uA).
- Integrate the simulation model in complex application and explore new possibilities.
- Explore main features of the real device (for more details consult the datasheet): shortest time to obtain results, zero error cost (no harm to physical components), can be done by anyone (engineers, students, etc.):
 - Regulation loops
 - Digital and analog PWM
 - Soft start behavior
- Simulation model does not cover all features of the real device in order to keep the usability and simulation speed in a reasonable range:
 - BST1,2 and SWN1,2 pins not available (no real external MOSFETs, only ideal switches)
 - LDO output (no IVCC/IVCC_ext pins available)
 - Thermal Network and self-heating not available
 - Fault reporting and handling not available (except short 2 ground detection possible via EF1 pin)
 - External clock sync (no FREQ_SYNC pin, frequency controlled via model parameter)
 - Limp home not implemented
 - Spread spectrum not implemented
 - Current consumption of the IC not considered (no realistic power efficiency calculation possible)
 - No ESD, EMC, AC, DC and Monte Carlo analysis simulation capability
 - Possible convergence issues for using DC sources, steep ramps or high frequency sources within the setup.

Details on the implementation

Gate drivers controlling the four external MOSFETs in H-Bridge configuration provides ideal 0 V to 5 V logic signals independent of switching nodes levels **SWN1,2**. Due to this, it is only possible to drive ideal switches instead of real MOSFETs. This in turn reduces the number of calculations per cycle and highly improves the total simulation time. Therefore, bootstrap pins **BST1,2** and **SWN1,2** are not present on the symbol. Dead time between low side and high side switching is implemented and for the ideal switches the ON threshold, $R_{DS(ON)}$ and body diode have been considered.

Internal oscillator has not been modeled as in the real device hence the **FREQ_SYNC** pin is not present in the symbol. The main reason is to reduce the complexity of the model and have the speed performance under control. Instead, the frequency of the controller is specified directly in [Hz] units via the model parameter **{frequency}** available on the test bench. External clock synchronization is not possible.

Internal LDO has not been modeled therefore **IVCC** and **IVCC_EXT** pins are not present in the symbol.

3 Model performance

3.1 Input voltage ramping – transient

This test bench shows how the regulator reacts to changes in the input voltage (V_{IN}) while the circuit is in steady state. Output current is monitored while the regulator tries to compensate for input voltage variation below or above the nominal output voltage. The load is fixed formed by 4 LEDs driven by 1 A average current.

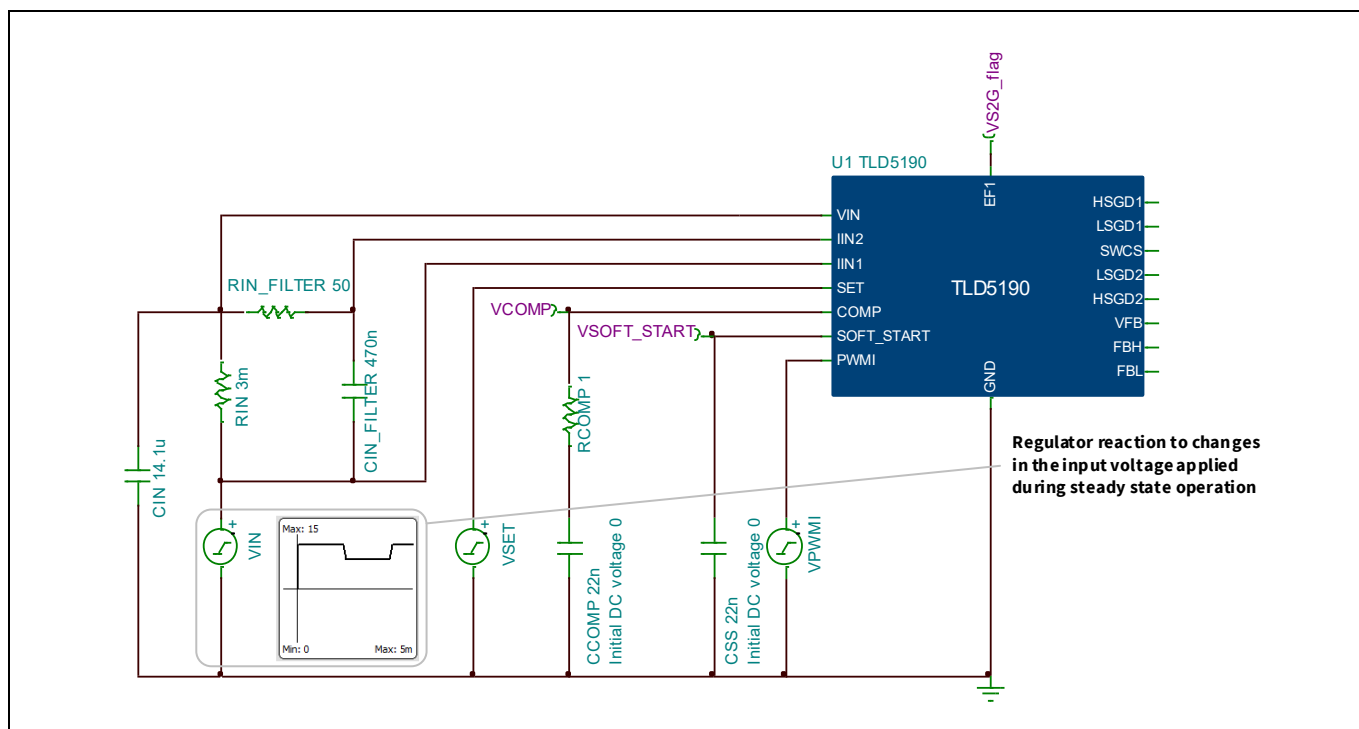


Figure 1 Test setup for input voltage ramping [click to open](#)

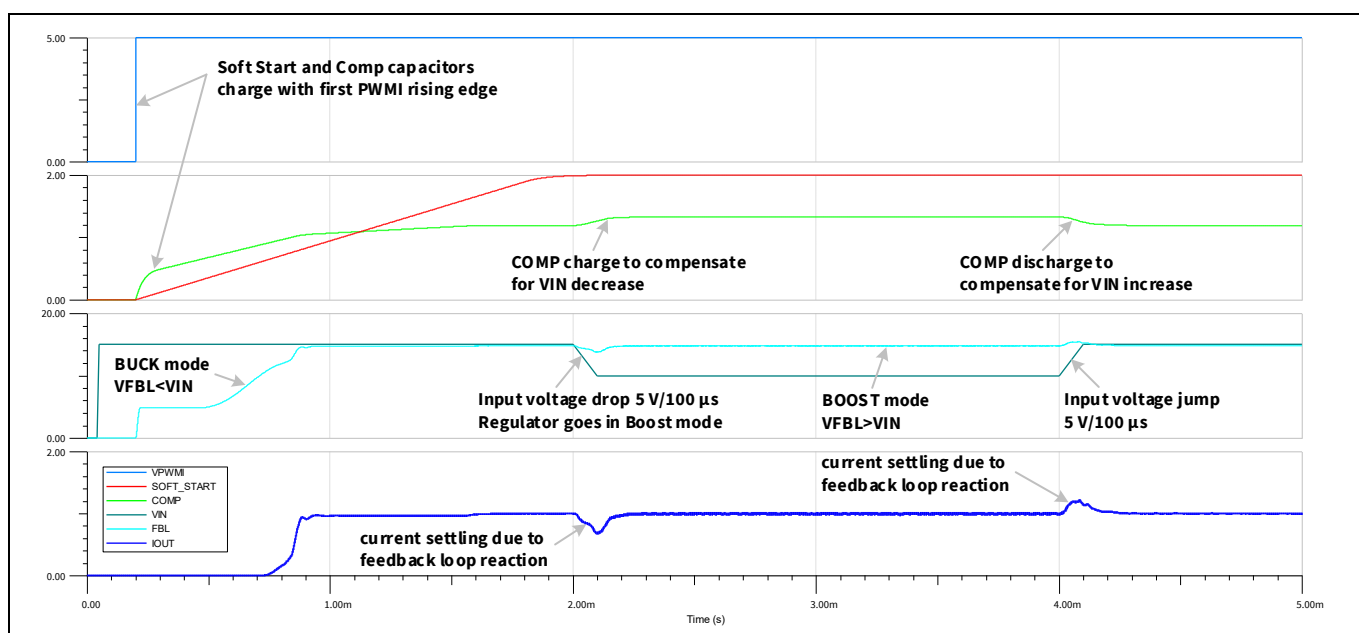


Figure 2 Simulation results

3.2 Soft start, analog and digital dimming – transient

This test bench shows the following features:

- **Soft start:** capacitors connected to SOFT_START and COMP inputs are chosen in order to see the impact of soft start in the start-up until the circuit reaches steady-state. If charging ramp at COMP pin is faster than ramp at SOFT_START pin and they move away by more than 0.7 V, then the ramp at COMP pin will be limited.
- **Output current control via SET pin (analog dimming):** R_{FB} is set to 150 mΩ in order to have 1 A at the output. SET pin is decreased from 1.4 V (100% analog dimming) to 0.8 V (50% analog dimming).
- **Output current control via PWM pin (digital dimming):** when PWM pin is set to logic low, the output current will drop to 0 A and the output capacitor starts to discharge (digital dimming).

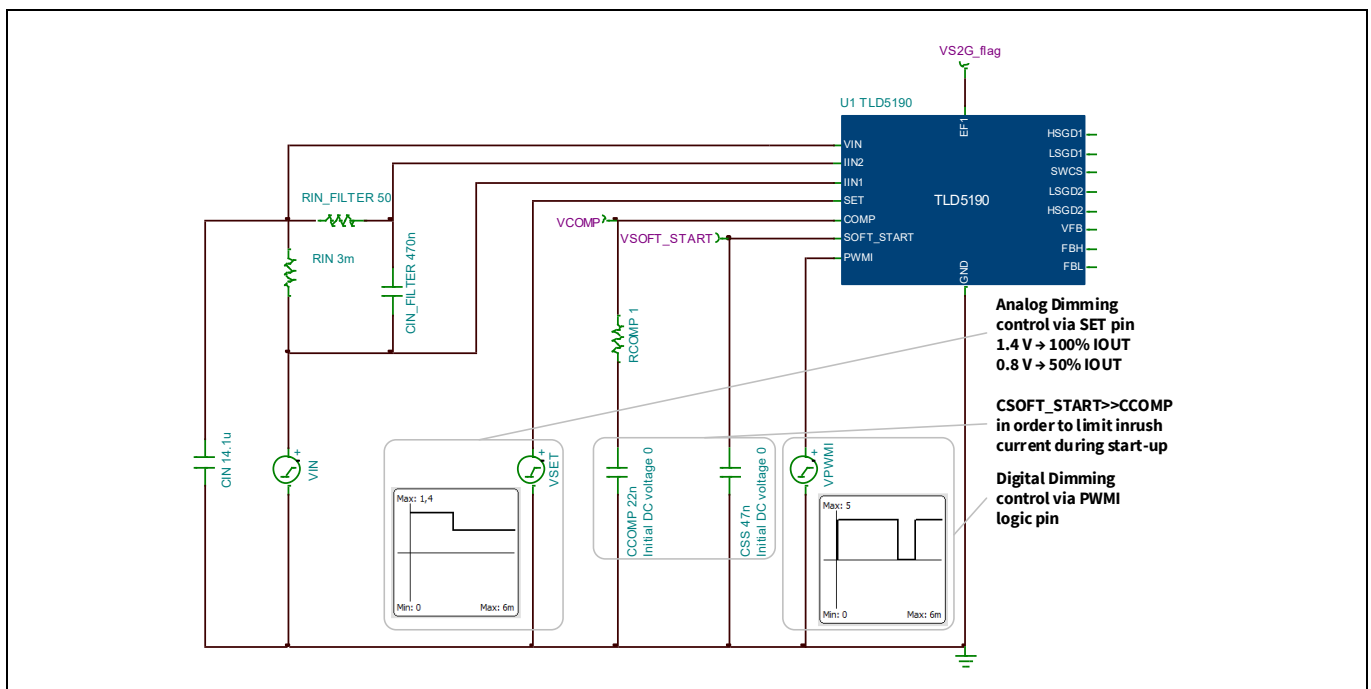


Figure 3 Test setup for soft start, analog and digital dimming [click to open](#)

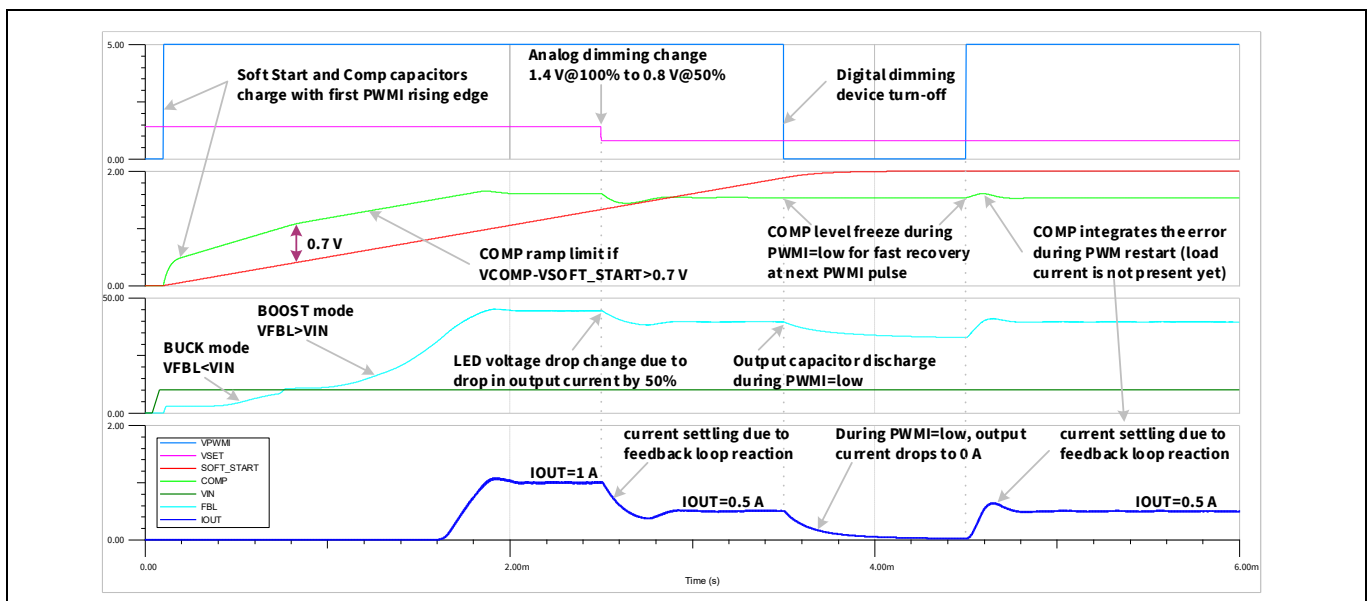


Figure 4 Simulation results

4 Revision history

Document version	Date of release	Description of changes
Rev.1.00	16.04.2020	Initial version created

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Edition 2020-04-16

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference

Z8F68847812

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