Non-isolated two-stage boost PFC plus current-regulated buck LED driver

IRXLED10

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About this document

Scope and purpose

The purpose of this document is to provide a comprehensive functional description of and guide to using the IRXLED10 two-stage PFC boost and buck LED driver evaluation board based on the IRS2505L and IRS2982. It describes the operation and covers technical aspects essential to the design process, including calculation of external component values, MOSFET selection and PCB layout optimization, as well as additional protection circuitry that may be added if needed. Test results and waveforms are also included.

Intended audience

Power supply design engineers, applications engineers, students.

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1 Introduction

The IRXLED10 reference design is a 75 W rated two-stage non-dimmable LED driver solution. The topology consists of a Power Factor Correction (PFC) boost converter front end based on the IRS2505L controller IC, followed by a tightly regulated Constant Current (CC) regulated buck LED driver based on the IRS2982. The IRS2505L is a Critical Conduction Mode (CrCM) PFC controller IC primarily intended for front-end PFC pre-regulators and typically used in power supply and lighting applications up to 150 W. The IRS2505L-based boost PFC pre-converter is able to meet the requirements of EN 61000-3-2, including class C limits for lighting applications. In some cases it is also appropriate to use this controller in other SMPS topologies such as buck, buck-boost and flyback. The back-end buck stage in this LED driver is configured for CC regulation using the IRS2982 controller operating in CrCM. The IRS2982 LED driver IC provides an accurately controlled current and protects the LEDs against damage from over-load.

The design procedure for the PFC stage based on the IRS2505L differs slightly from the procedure used for industry-standard 8-pin CrCM PFC control ICs, and will be explained in detail here. In order for the circuit to produce optimum performance care must be taken to select the correct component values and ratings. The PCB must also be designed according to correct practices for SMPS design, for which guidelines are provided, to avoid ground loops and noise susceptibility.

Figure 1 IRXLED10 two-stage LED driver board

2 Evaluation board specifications

Input and output at normal operation

- AC input voltage 90 V AC up to 265 V AC (55 to 65 Hz)
- Output voltage range at 360 mA +/-1.5 mA output 60 to 200 V DC
- Maximum output continuous power 75 W
- PF greater than 0.9 at maximum load, 90 to 265 V AC input voltage
- Total Harmonic Distortion (iTHD) less than 20 percent at maximum load, 90 to 265 V AC input voltage
- Efficiency greater than 90 percent at maximum load, 115 and 230 V AC input voltage
- Start-up time to reach the secondary nominal output voltage during full-load condition and 115 and 230 V AC input voltage less than 1.2 s

Protection features

- Primary output Over Voltage Protection (OVP) at V_{OUT} less than or equal to 255 V DC
- Cycle-by-cycle primary Over Current Protection (OCP)

No-load operation

- Burst mode during no-load condition
- Max. power losses during no-load condition less than 500 mW, 120 and 230 V AC input voltage

Max. component temperature

During worst-case scenario (ambient temperature 60°C) the max. allowed component temperature is:

- Resistor less than 100°C
- Ceramic capacitor, film capacitor and electrolytic capacitor less than 85°C
- Flyback transformer and chokes less than 100°C
- MOSFET, transistor and diodes less than 100°C
- IC less than 100°C

Dimensions of evaluation board

- Max. width 5.75 inches (146.0 mm), max. length 1.48 inches (37.8 mm)

WARNING!

OUTPUT IS NOT ISOLATED! Risk of electric shock!
The board should be tested only by qualified engineers and technicians.

3 Schematic

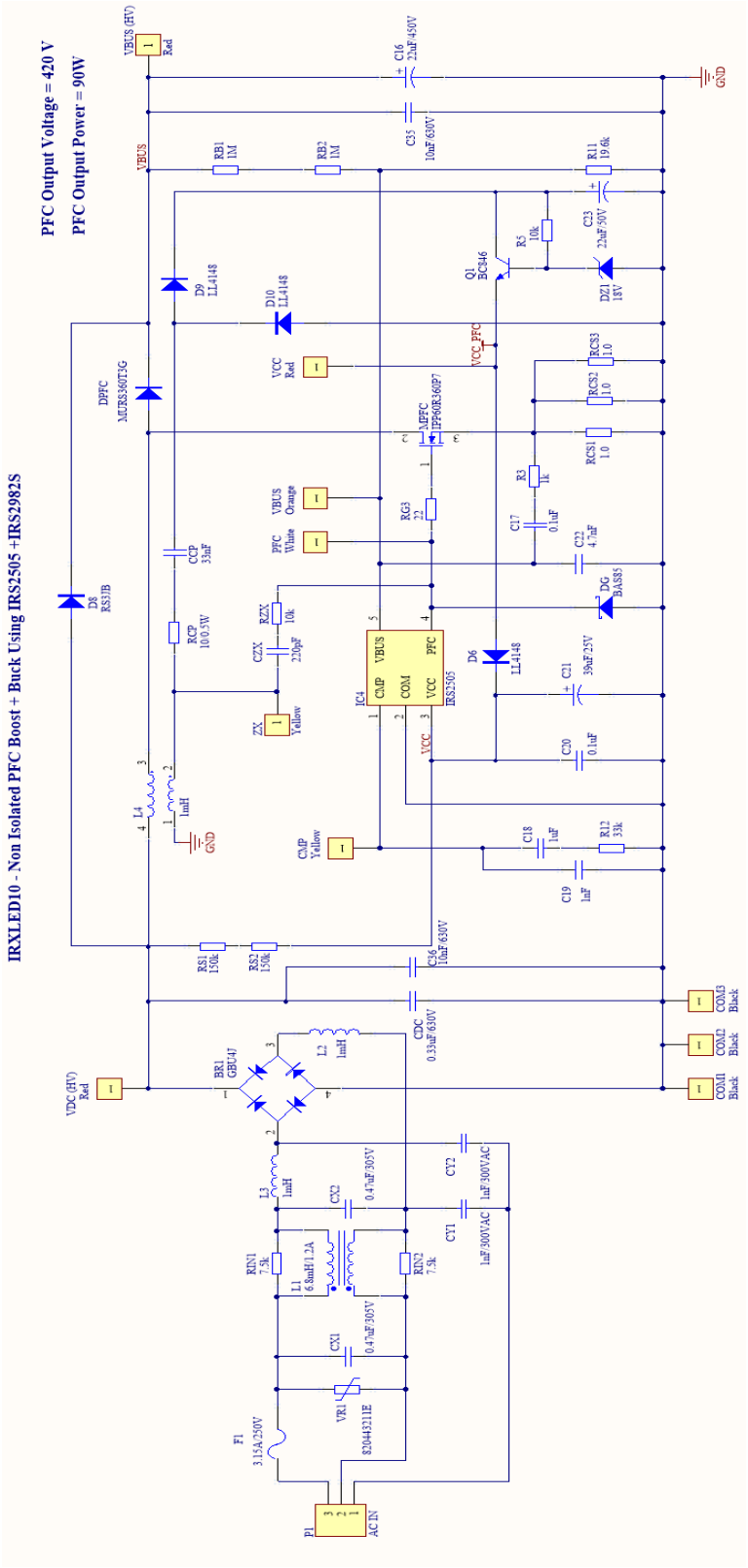


Figure 2 IRXLED10 front-end schematic (PFC boost)

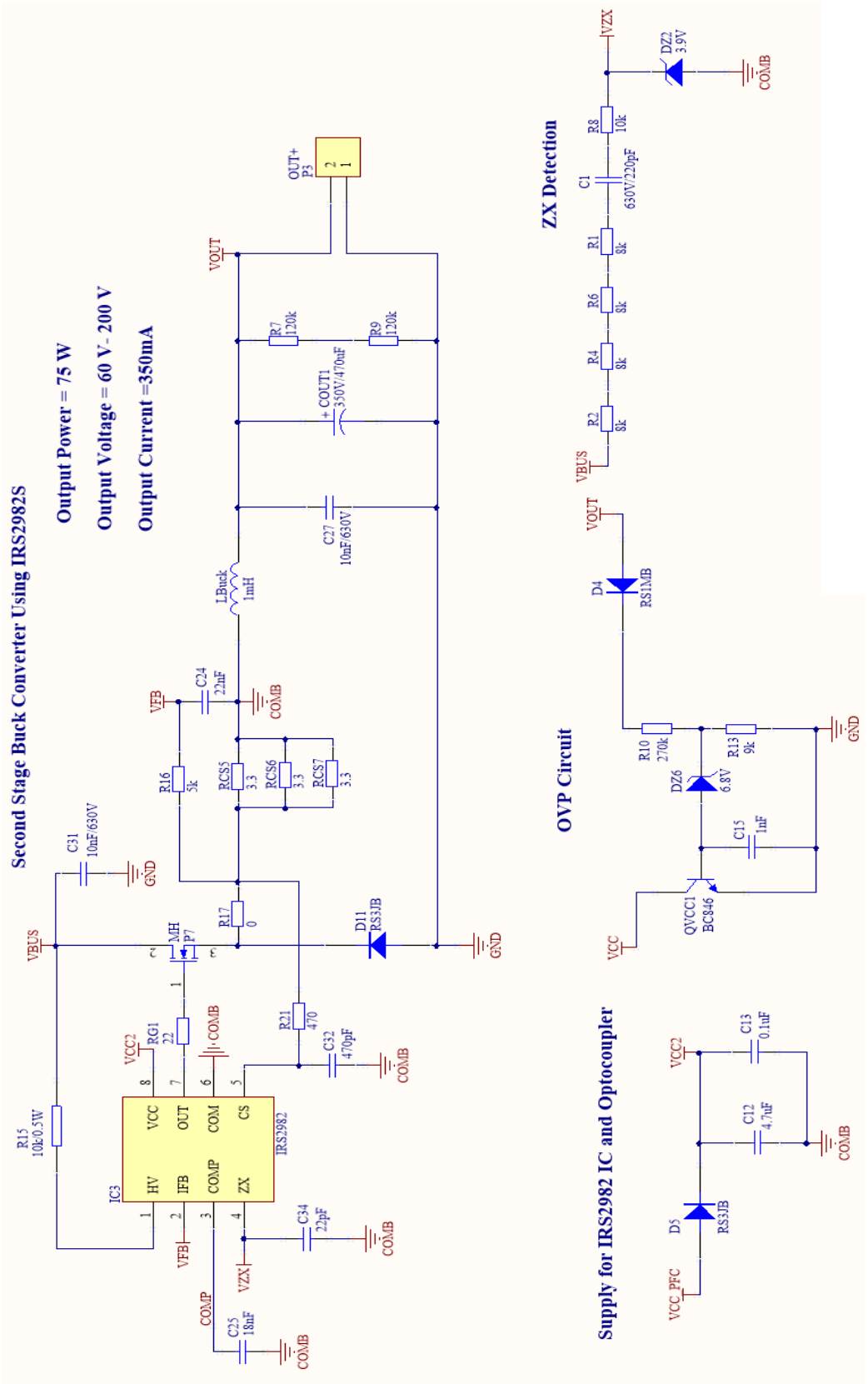


Figure 3 IRXLED10 back-end schematic (buck)

4 IRS2505L functional overview

The IRS2505L is a CrCM boost PFC controller IC. All of the functionality for controlling the PFC pre-converter is integrated into the SOT23-5 package. This low pin count solution operates by using multi-functional V_{BUS} and PFC pins so that the cycle-by-cycle Current Sense (CS) input is combined with the output voltage feedback at the V_{BUS} pin and the Zero Crossing (ZC) sensing function is combined with the gate drive at the PFC pin.
At the start of each switching cycle the PFC pin gate drive output pulls the PFC pin voltage high and the external MOSFET turns on, where the on-time duration is set by the (CMP) pin voltage. The internal PFC control loop regulates the CMP pin voltage, which determines the on-time such that if the DC bus voltage increases then the CMP pin voltage and on-time will decrease, and vice versa. Decreasing the on-time reduces the peak inductor current, transferring less energy per switching cycle and causing the DC bus voltage to decrease. If the DC bus voltage decreases below the desired level the CMP pin voltage, on-time will increase to compensate. This negative feedback control loop regulates the DC bus to a constant voltage over AC-line voltage or output load variations. The speed of regulation is determined by the internal OTA trans-conductance and compensation capacitor C_{CMP}.
At the end of each on-time period, the PFC pin gate drive circuit pulls the PFC pin to COM and the external PFC MOSFET turns off. After a short initial switch-off delay (t_{PD}), the IRS2505L internal gate drive pull-down turns off and the PFC pin is then weakly pulled up and clamped at approximately one diode forward voltage drop (V_{PFCOFF}), which is well below the gate threshold of the MOSFET (M_{PFC}), ensuring that it is not able to switch on. During the off-time the PFC inductor current discharges through the boost diode into the DC output capacitor and load. When the inductor current falls to zero, the drain voltage falls from the level of the output voltage plus the output diode forward voltage, and transitions negatively. During this transition current flows through the MOSFET parasitic gate-to-drain capacitance C_{GD}, overcoming the internal weak pull-up and causing the gate voltage to drop below the threshold V_{PFCZC-}. After remaining below this threshold for a period of $t_{ZCBLANK}$, the PFC gate drive is turned on again to begin the next switching cycle. To ensure ZC Detection (ZCD) a minimum voltage headroom of 60 to 70 V is needed between the peak line voltage at high-line and the output voltage. This value depends on the MOSFET C_{GD} and C_{GS} values. To operate with smaller headroom a 500 V minimum rated capacitor of low value in the tens of pF range may be added between drain and gate with a 100 Ω series resistor to provide some additional -dv/dt coupling to the gate.
Since the loop speed is slow with respect to the line frequency, the on-time is essentially constant over the entire half-cycle of the line input voltage, producing a peak inductor current that naturally follows the sinusoidal shape of the line input voltage. The filtered, averaged line input current is in phase with the line input voltage (neglecting a small displacement caused by the input filter X-capacitors) to provide high power factor. However some harmonic distortion of the current is still present, mostly due to cross-over distortion occurring near the ZCs of the line input voltage. To achieve very low harmonics within the limits of international standards and to meet general market requirements, on-time modulation is included in the IRS2505L, which dynamically increases the on-time as the line input voltage nears the ZCs. The peak LPFC current and therefore the smoothed line input current increase slightly near the ZCs of the line input voltage. This reduces the amount of cross-over distortion in the line input current and improves the shape of the current, reducing the iTHD and harmonics to low levels.
The V_{BUS} input includes output OVP. Should the average feedback voltage at the V_{BUS} pin exceed the internal OVP threshold (V_{BUSOV+}) then the PFC gate drive will turn off until the V_{BUS} pin voltage again falls below the OV restart threshold (V_{BUSOV-}) to resume normal operation. As well as sensing the output voltage feedback, the V_{BUS} input also includes a cycle-by-cycle, AC-coupled, OCP function. An internal OCP circuit detects the difference between the peak and average of the composite signal such that if the triangular-shaped voltage peak at the V_{BUS} input exceeds V_{BUSREG} by a delta of V_{BUSOC+} the gate drive is immediately driven low. Capacitor C_{VBUS} is included in the feedback network to make the CS signal more triangular rather than a discontinuous ramp. This is so that the peak value will be close to half the average.

The composite voltage and current feedback signal appearing at the V_{BUS} input is shown below:

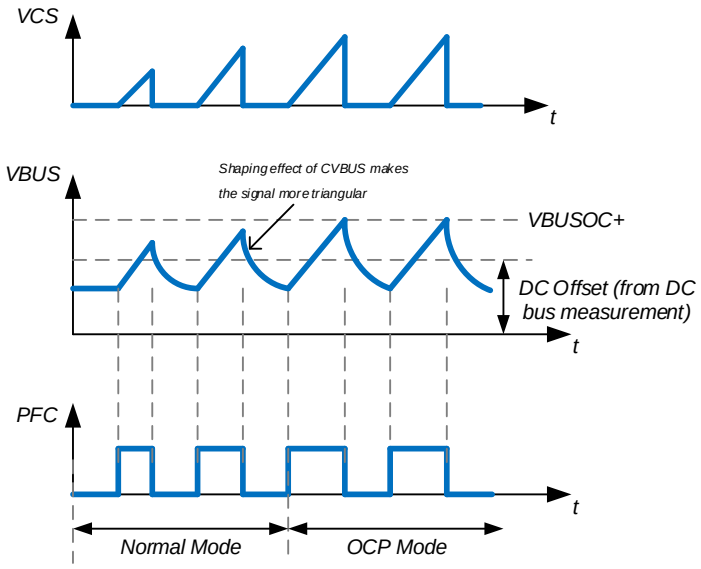
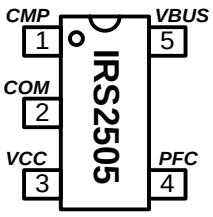


Figure 4 V_{BUS} input signal

The IRS2505L uses an SOT23-5 package, as shown below:



Pin	Name	Description
1	***CMP***	HV start-up input
2	***COM***	Feedback input
3	***V_{CC}***	Compensation and averaging capacitor input
4	***PFC***	ZC and OV detection input
5	***V_{BUS}***	CS input

Figure 5 IRS2505L pin assignments

5 IRS2982S functional overview

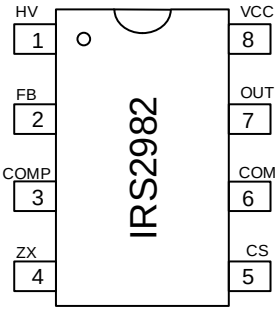
The IRS2982S is comprised of the following functional blocks:

1. *HV start-up cell*
   The IC internal functional blocks remain disabled in low-power mode until V_{CC} first rises above the V_{CCUV+} Under Voltage Lockout (UVLO) threshold, continuing to operate while V_{CC} remains above V_{CCUV-}. V_{CC} is initially supplied through the integrated HV start-up cell, which supplies a controlled current from the HV input provided a voltage greater than V_{HVSMIN} is present. The current supplied is limited to I_{HV_CHARGE}, reducing to less than I_{HVS_OFF} when V_{CC} reaches the cut-off threshold V_{HVS_OFF1}. The HV start-up cell switches over from start-up mode to support mode after the feedback input at FB has exceeded V_{REG} for the first time. In this mode the cut-off threshold becomes V_{HVS_OFF2}. During steady-state operation under all line-load conditions V_{CC} is supplied through an auxiliary winding on the flyback transformer with V_{CC} high enough so that the HV start-up cell does not supply current. If the auxiliary supply were unable to maintain V_{CC}, the HV start-up cell operating in support mode would supply current to assist.

2. *PWM controller*
   The SMPS control section operates in voltage mode where the gate drive output on-time is proportional to the error amplifier output voltage appearing at the compensation output COMP. An external capacitor C_{COMP} (shown in Figure 4) connected to 0 V (ground) acts with the trans-conductance characteristic of the error amplifier to provide loop compensation and stability. Minimum on-time is reached when V_{COMP} falls to $V_{COMPOFF}$, below which the gate drive is disabled. Under very light-load conditions V_{COMP} transitions above and below $V_{COMPOFF}$ to produce burst-mode operation. Off-time is determined by the demagnetization signal received at the ZC input, which is derived from the auxiliary transformer winding that supplies V_{CC} through a resistor divider. Internal logic limits the minimum off-time to t_{OFFMIN}, therefore the system transitions from CrCM to Discontinuous Conduction Mode (DCM) at light loads. If the ZC input signal fails to provide triggering the next cycle will start automatically after a re-start period of t_{WD}.

3. *Protection*
   The IRS2982S includes cycle-by-cycle primary OCP, which causes the gate drive to switch off if the voltage detected at the CS exceeds the threshold V_{CSTH}. This prevents the possibility of transformer saturation at low-line under heavy load, but does not protect against output over-load or short-circuit.

OVP is also provided through the ZC input, which provides a voltage proportional to the output voltage. This disables the gate drive output and pulls the COMP voltage below the $V_{COMPOFF}$ threshold. The error amplifier then starts to charge C_{COMP} until the gate drive starts up again at minimum on-time. Under an open-circuit output condition the OVP causes the converter to operate in burst mode, preventing the output voltage from rising too high. The IRS2982S uses an SO-8 package, as shown below:



Pin	Name	Description
1	***HV***	HV start-up input
2	***FB***	Feedback input
3	***COMP***	Compensation and averaging capacitor input
4	***ZC***	ZC and OV detection input
5	***CS***	CS input
6	***COM***	IC power and signal ground
7	***OUT***	Gate driver output
8	***V_{CC}***	Logic and low-side gate driver supply

Figure 6 IRS2982S pin assignments

6 Dimensioning

6.1 Boost PFC stage

The boost converter is designed for PFC with low AC-line current iTHD. The MOSFET used is an IPP60R360P7 600 V CoolMOS™ device with 360 mΩ on-resistance, 13 nC gate charge and very low parasitic capacitances in a TO-220 package. The output diode MURS360T3G (SMC package) has typically 75 ns reverse recovery and a forward voltage drop less than 1.25 V at a maximum rated current of 3 A at 25°C. The blocking voltage is 600 V, which is enough to withstand the maximum output voltage. The parameters of the MOSFET and output diode contribute to the overall high efficiency of the converter.
The boost inductor consists of two windings; the main energy transfer winding and the auxiliary, which supplies V_{CC} and provides the required de-magnetization signal. The auxiliary winding has 18 turns to ensure a good start-up at the lowest input AC voltage. In steady-state operation the IRS2505L (IC2) V_{CC} is supplied from a charge pump comprised of R5, C23, D9 and D10 through a series transistor Q1, which clamps the voltage according to DZ to protect IC4 from damage due to excess voltage. PFC output voltage feedback is provided through the RB1, RB2 and R11 divider network.

Switching cycle peak current limiting is set by shunt resistors RCS1, RCS2 and RCS3, which are 1 Ω each, setting the peak current to 2.68 A according to the threshold V_{BUSOC+} of 0.56 V. This prevents PFC inductor saturation at low-line and high load.

6.1.1 PFC inductor and CS resistor

The PFC inductor is calculated to produce an off-time of 15 µs at the peak of the AC-line at nominal line input voltage, which has been selected as 230 V AC. This provides optimum iTHD reduction where it is most needed in the 220 to 230 V AC range. The IRS2505L introduces on-time modulation to compensate for cross-over distortion when the off-time falls below 7 µs. This means that with the correct value of LPFC the on-time modulation will begin to take effect as the line voltage drops from the peak and approaches the ZC. The on-time is thereby increased as necessary to compensate for the cross-over distortion which causes iTHD degradation at high-line in PFC circuits. The desired inductance is calculated from the following formula:

$$LPFC = \frac{15.10^{-6}\left(VBUS-\sqrt{2}\cdot VAC_{NOM(RMS)}\right)\cdot VAC_{NOM(RMS)}\cdot\eta}{2\sqrt{2}\cdot P_{OUT}} \quad [H] \quad [1]$$

$$\frac{15.10^{-6}.\left(420-\sqrt{2}\cdot 230\right)\cdot 230\cdot 0.95}{2\sqrt{2}\cdot 90} = 1.2\ mH$$

The peak inductor current is then calculated from:

$$IPFC_{MAX} = \frac{2\sqrt{2}\cdot POUT}{VAC_{MIN}\cdot\eta} \quad [A] \quad [2]$$

$$\frac{2\sqrt{2}\cdot 90}{90\cdot 0.95} = 2.98\ A$$

The CS resistor (R_{CS}) is then calculated:

$$RCS = \frac{2 \cdot V_{BUSOC+}}{IPFC_{MAX}} \quad [\Omega] \quad [3]$$

$$RCS = \frac{2 \cdot 0.56\,V}{2.98\,A} = 0.38\,\Omega$$

In this case a parallel combination with a combined resistance of 0.33 Ω has been used.

6.1.2 Voltage feedback and loop compensation

The DC output bus voltage is regulated using a resistor divider to provide feedback to the error amplifier through the V_{BUS} input. The cycle-by-cycle CS signal is also superimposed onto this DC voltage; however, this can be ignored for the purposes of calculating the voltage divider. This is because the voltage feedback and CS signals are separated within the IRS2505L. The internal reference for the error amplifier V_{BUSREG} is nominally 4.1 V. The resistor divider values are calculated as follows, where two equal series resistors R39 and R31 are used for the upper branch of the divider.

RB1 and RB2 are selected as 1 MΩ for minimal power dissipation:

$$P_{RB1} = P_{RB2} \approx \frac{V_{BUS}^2}{2 \cdot (R_{B1} + R_{B2})} \quad [W] \quad [4]$$

$$\frac{420^2}{2 \cdot (1 \cdot 10^6 + 1 \cdot 10^6)} \approx 44\,mW$$

Therefore:

$$R_{VBUS} = \frac{VBUSREG \cdot (R_{B1} + R_{B2})}{VBUS - VBUSREG} \quad [\Omega] \quad [5]$$

$$\frac{4.1 \cdot (1 \cdot 10^6 + 1 \cdot 10^6)}{420 - 4.1} = 19.7\,k\Omega$$

In order for the converter to provide high power factor and low iTHD the loop response must be slow enough that the on-time remains effectively constant (except for on-time modulation) throughout each line frequency half-cycle. Since the AC-line frequency is 50 to 60 Hz the error amplifier gain has to roll off at a lower frequency. The recommended value for this cut-off frequency (or bandwidth) is 20 Hz to give the acceptable loop response without degrading the power factor. The loop speed is determined by the compensation capacitor C18, whose value is calculated from the trans-conductance of the error amplifier g_m (approximately 100 $\mu\Omega^{-1}$) as follows:

$$C_{18} = \frac{g_m}{2\pi \cdot f_c} = \frac{100}{2\pi \cdot 20} = 0.796 \quad [\mu F] \quad [6]$$

A C18 value of 1 µF is used in the IRXLED10 evaluation board PFC combined with a 33 kΩ series resistor (R12) and a 1 nF (C19) capacitor parallel to both. The series resistor enables V_{COMP} to jump almost instantly to approximately 1 V when V_{CC} first crosses V_{CCUV+}. This reduces the time required for C18 to charge above V_{CMPON} (1.5 V) to enable the gate drive. This reduces the time during which V_{CC} is supplied through C20 and C21 before the auxiliary winding can provide current. The compensation network discussed changes the frequency response of the error amplifier introducing a zero at 7.1 Hz and a pole at 4.8 kHz, while maintaining a gain of approximately 10 dB between these two frequencies. This has the effect of reducing settling time at start-up or after a change in line or load.

6.1.3 Output capacitor calculation

The output bulk capacitor (C_{BUS}) can be a single capacitor rated at 450 V for nominal output voltages up to 420 V. This ensures that under start-up and transient conditions the output voltage will not exceed the maximum voltage rating. This value can be calculated according to:

$$C_{BUS} = \frac{P_{OUT}}{2 \cdot \pi \cdot f_{IN(MIN)} \cdot \Delta_{RIPPLE} \cdot V_{BUS}^2} \quad [F] \quad [7]$$

Where $f_{IN(MIN)}$ is the minimum line input frequency set at 50 Hz and Δ_{RIPPLE} is the fraction of V_{BUS} acceptable as peak-to-peak ripple amplitude. This should not exceed 16 percent to avoid false triggering of OVP. In this case a value of 7.1 percent is used corresponding to 30 V_{pp}.

$$\frac{90}{2 \cdot \pi \cdot 50 \cdot 0.071 \cdot 420^2} = 22\ \mu F$$

6.2 Buck stage

A non-synchronous buck converter consists of a high-side MOSFET and a low-side diode in the half-bridge configuration. The system efficiency is directly influenced by several system parameters such as operating frequency, load current and input voltage. The buck stage is designed using the IRS2982 in a high-side floating buck configuration.
On the IRXLED10 evaluation board a MOSFET is used as high-side switch and a fast recovery diode is used as the low-side switch. Shoot-through current transients caused by reverse recovery of the low-side diode are a major contributor to switching losses when working from a PFC output bus voltage in the 400 V range. To eliminate the reverse recovery of the low-side diode, the buck stage is designed to operate in CrCM. This will provide Zero Voltage Switching (ZVS) for the high-side MOSFET. The downside of this approach is that inductor current ripple will be much higher compared to a CCM inductor current ripple, and this causes higher conduction losses in the MOSFET and diode.

Dimensioning

On this evaluation board, the IRS2982 is used in a floating configuration referenced to the source of the high-side MOSFET. The FB pin of the IRS2982 compares the average output CS signal supplied through the filter of R16 and C24 with the 0.4 V internal reference and adjusts the duty cycle in order to regulate the output load current. This configuration provides a very tight current regulation over a wide load range (50 to 200 V). The ZC of the inductor current is detected from the DC bus voltage using a configuration formed by R1-C1-R8-DZ2.

The inductance required for the buck inductor in CrCM can be calculated from the following formula:

$$L_{BUCK} < \frac{V_{OUT}}{2 \cdot f_{SW} \cdot i_{OUT}} \cdot \frac{(V_{BUS} - V_{OUT})}{V_{BUS}} \quad [H] \quad [8]$$

For 350 mA output current:

$$\frac{200}{2 \cdot 100 \cdot 0.35} \cdot \frac{(420 - 200)}{420} = 1.49\ mH$$

The IRXLED10 evaluation board uses a 1 mH inductor with a peak current rating of 1.2 A. This inductor value ensures that the buck always operates in CrCM within the desired switching frequency range. Bench measurements show that the peak inductor current of the buck stage does not exceed 750 mA. It is essential that there is enough margin for the peak current rating in order to ensure the inductor does not saturate.

The CS resistor value for a desired average output current is therefore calculated from the maximum LED load voltage, as follows:

$$R_{CS(BUCK)} = \frac{VFB(TH)}{I_{OUT}} \quad [\Omega] \quad [9]$$

For 350 mA the required CS resistor is calculated as :

$$R_{CS(BUCK)} = \frac{0.4}{0.35} = 1.14\ \Omega$$

This is provided by the parallel combination of RCS5-7, which is equal to 1.1 Ω.

V_{CC} to the buck stage is supplied from the PFC stage using the diode D5, C12, C13.

6.2.1 MOSFET selection

The CoolMOS™ IPD60R360P7 and MURS360T3S are also used for the buck converter stage. Since blocking voltages exist up to the DC bus voltage of 420 V, 600 V rated devices provide a comfortable safety margin. The CoolMOS™ P7 series is the latest CoolMOS™ product family providing high-performance optimizing key parameters (C_{oss}, E_{oss}, Q_g, C_{iss} and $V_{GS(th)}$). A Zener diode is also included for ESD protection. The 600 V CoolMOS™ P7 is suitable for both soft- and hard-switching topologies, including PFC, flyback, LLC and TTF.

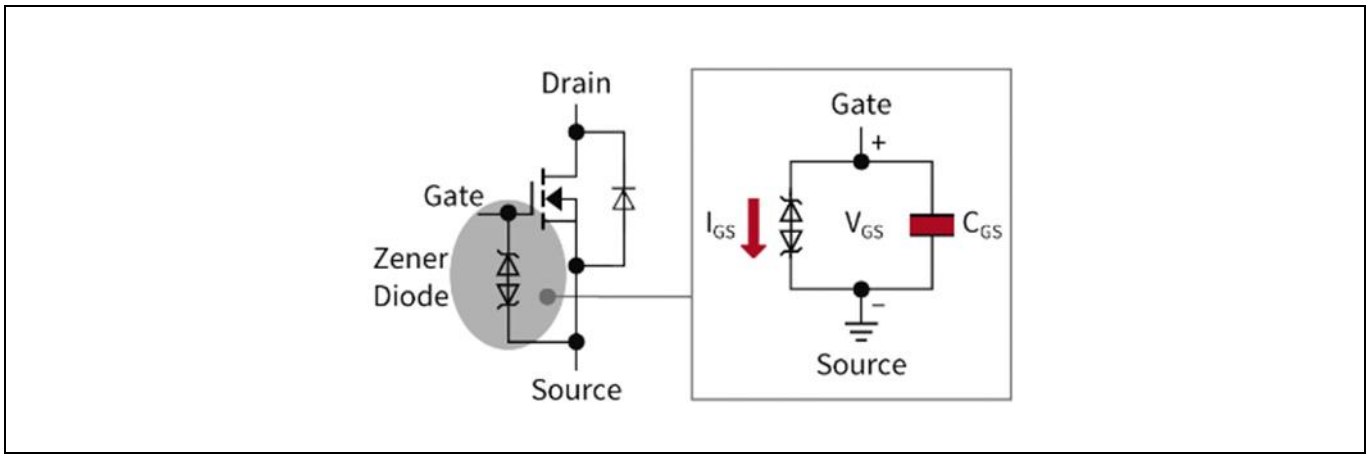


Figure 7 Switching MOSFET parasitics

6.2.2 OV protection

The output terminal DC voltage is limited to 257 V by the OVP circuit. The OVP is provided by D4, R10, R13, DZ6 and Q_{VCC1}. The output capacitor used on this board is 47 µF/350 V. This voltage rating can be lower than the PFC bus voltage since the OVP circuit limits the output to 257 V. The output is non-isolated, therefore a HV potential with respect to ground and associated electric shock risk exists from either output terminal.
If no LED load is connected to clamp the output voltage between P3 terminals 1 and 2, this voltage will rise until the voltage across R13 reaches 7.5 V, which turns on the NPN transistor Q_{VCC1}, thereby disabling the V_{CC} bias for the IRS2505L and shutting off the PFC gate drive. The IRS2982 bias supply is also removed and thus goes into burst mode. In this way the PFC and the buck stage enter hiccup mode during an open-load condition to limit the output to no more than 257 V.

6.2.3 ZCD

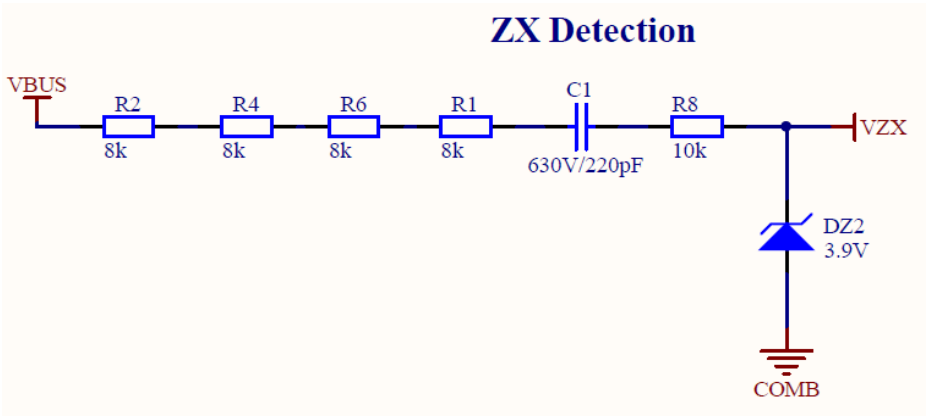


Figure 8 ZCD

Figure 8 shows the ZCD method used on the LED10 demo board for the buck stage.The ZC of the buck inductor current is detected using the drain-to-source voltage of the high-side MOSFET. R1, R2, R4 and R6 are used to limit the current and reduce the PFC bus voltage to a LV value. C1 is used to remove the DC offset. DZ2 will clamp the voltage at the ZC pin of the IRS2982 to 3.9 V. The scaled-down version of the V_{DS} signal given to the IRS2982 ZC pin indicates that all of the energy stored in the buck inductor has been transferred to the output. This triggers the start of the next switching cycle. This new method eliminates the use of an extra auxiliary winding to perform the ZCD.

6.2.4 Auxiliary charge pump supply

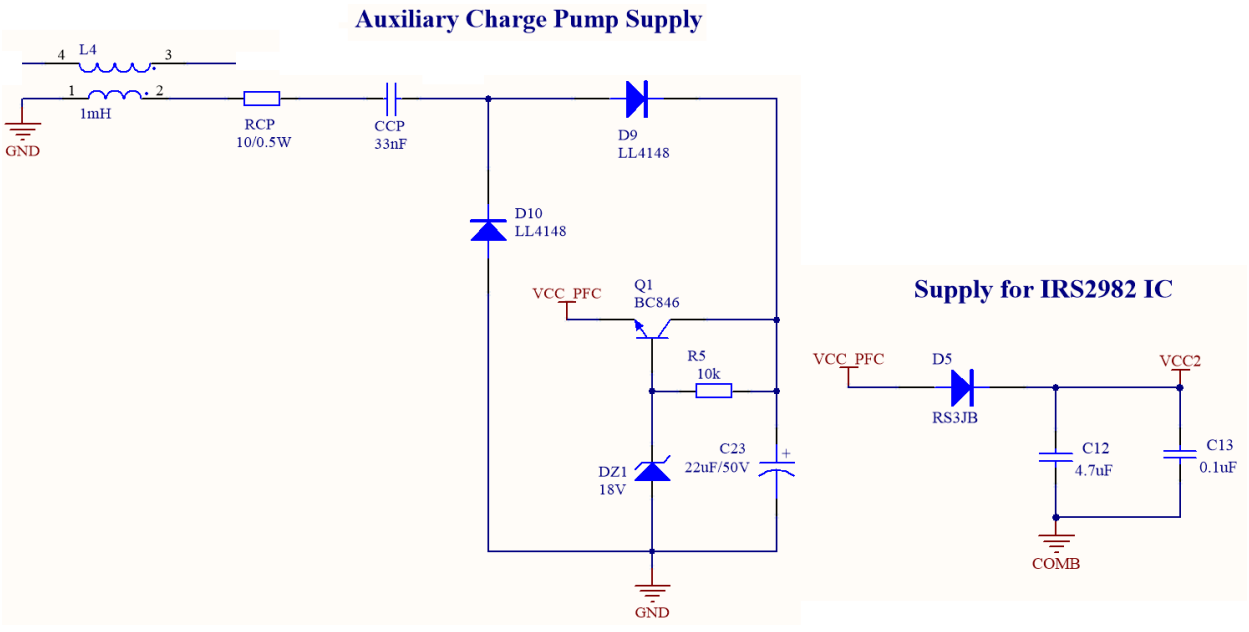


Figure 9 Auxiliary charge pump supply

Dimensioning

The boost inductor consists of two windings; the main energy transfer winding and the auxiliary, which supplies V_{CC} and provides the required de-magnetization signal. In steady-state operation the IRS2505L (IC4) V_{CC} is supplied from a charge pump comprised of RCP, CCP, D10 and D9 through a series transistor Q1, which clamps the voltage according to DZ1 to protect IC4 from damage due to excess voltage. The V_{CC} supply to the IRS2982 (IC3) is supplied through the same charge pump connected to the auxiliary PFC inductor winding. An important point to note here is that the capacitors C12 and C13 are connected with respect to the floating COMB. The diode D5 will be forward biased and the capacitors C12 and C13 will be charged only during the off-time of the buck switching period when the low-side diode of the buck stage turns on, pulling the COMB to ground. When the COMB is at the DC bus voltage of roughly 400 V, the diode D5 will be reverse biased. A floating supply for the IRS2982 is therefore provided on the C12 and C13 capacitors.

7 Bill of Materials (BOM)

Designator	Manufacturer	Part number	Quantity	Value/Rating
BR1	Vishay	GBU4J-E3/51	1	600 V/4 A
C1	TDK	C3216CH2J221J060AA	1	220 pF/630 V/ 1206
C2	Rubycon	450BXW22MEFR12.5X20	1	22 µF/450 V/20%
C12	Samsung Electro-Mechanics	CL31B475KAHVPNE	1	4.7 µF/25 V/X7R/1206
C13	Samsung Electro-Mechanics	CL21B104KACNNNC	1	0.1 µF/25 V/X7R/0805
C15, C19	Kemet, TDK	C0805C102K3GEC, C2012X7R2E102K085AA	2	1 nF/25 V/C0G/10%, 1 nF/250 V/0805/10%
C17, C20	TDK	C2012X7R1H104K085AA	2	0.1 µF/50 V/0805/10%
C18	TDK	C2012X7R1E105K125AB	1	1 µF/25 V/0805/10%
C21	Panasonic	EEU-FC1E390	1	39 µF/25 V
C22	TDK	C2012X7R2E472K085AA	1	4.7 nF/250 V/0805/10%
C23	Panasonic	EEU-EB1H220S	1	22 µF/50 V
C24	Kemet	C0805C223K3GEC	1	22 nF/25 V/C0G/10%
C25	Kemet	C0805C183J3GAC7800	1	0.018 µF/25 V/NP0/0805
C27, C31, C35, C36	TDK	C3216X7R2J103K115AA	4	10 nF/630 V/1206/X7R
C32	Yageo	CC0805KRX7R8BB471	1	470 pF/25 V/X7R/0805
C34	Kemet	C0805C220J5GACTU	1	22 pF/50 V/C0G/0805
CCP	TDK	C3216CH1H333K085AA	1	33 nF/50 V/1206/10%
CDC	Panasonic	ECQ-E6334JF	1	0.33 µF/630 V/5%
CMP, ZC	Keystone	5004	2	0.04 inch diameter yellow
COM1, COM2, COM3	Keystone	5001	3	0.04 inch diameter black
COUT1	Nichicon	UCY2V470MHD1TO	1	47 µF/350 V
CX1, CX2	Epcos	B32922C3474M	2	0.47 µF/305 V AC/X2
CY1, CY2	Vishay	VY2102M29Y5US63V7, VY2102M29Y5UG63V7	2	1 nF/300 V AC/Y2
CZC	TDK	CGA4C2C0G2A221J060AA	1	220 pF/100 V/0805/5%
D4	Diodes Inc.	RS1MB-13-F	1	1000 V/1 A/SMB
D5	Diodes Inc.	RS1MB-13-F	1	1000 V/1 A/SMB
D6, D9, D10	Diodes Inc.	LL4148-13	3	75 V/0.15 A/MiniMELF
D8, D11	Diodes Inc.	RS3JB-13-F	2	600 V/3 A/SMB
DG	Vishay	BAS85-GS08	1	30 V/200 mA/SOD80
DPFC	ON Semi	MURS360T3G	1	600 V/3 A
DZ1	Micro Commercial Co.	BZV55C18-TP	1	18 V/0.5 W/MiniMELF
DZ2	Central Semiconductor Corp.	CLL5228B TR	1	3.9 V/500 mW/SOD80
DZ6	Nexperia USA Inc.	BZV55-C6V8,115	1	6.8 V/0.5 W/MiniMELF
F1	Bel Power	RST 3.15	1	250 V/3.15 A
IC3	Infineon	IRS2982S	1	IC controller
IC4	Infineon	IRS2505L	1	PFC control IC

L1	Epcos	B82721A2122N20	1	6.8 mH/1.2 A
L2	Bourns	2124-V-RC	1	1 mH/1.3 A
L4	Yu Jing Energy Technology Co., Ltd.		1	1.2 mH/QP2520 core
LBuck			1	
MH	Infineon	IPD60R360P7	1	600 V/9 A/DPAK
MPFC	Infineon	IPP60R360P7	1	600 V/9 A/TO-220
P1	Phoenix Contact	1985205	1	3-position 3.5 mm green
P3	Phoenix Contact	1985195	1	2-position 3.5 mm green
PFC	Keystone	5002	1	0.04 inch diameter white
Q1, QVCC1	Micro Commercial Co.	BC846B	2	65 V/0.1 A/NPN/SOT-23
R1, R2, R4, R6	Panasonic	ERJ-14YJ822U	4	8.2 kΩ/0.5 W/1210/5%
R3	Panasonic	ERJ-6GEYJ103V	1	10 kΩ/0.125 W/0805/5%
R5, RZC	Panasonic	ERJ-6GEYJ103V	2	10 kΩ/0.125 W/0805/5%
R7, R9	Panasonic	ERJ-6GEYJ124V	2	120 Ω/0.125 W/0805/5%
R8	Stackpole Electronics Inc.	RMCF1206FT10K0	1	10 kΩ/0.25 W/1206/1%
R10	TE Connectivity Passive Product	CRGCQ1206F270K	1	270 kΩ/0.25 W/1206/1%
R11	Panasonic	ERJ-8ENF-1962V	1	19.6 kΩ/0.25 W/1206/1%
R12	Panasonic	ERJ-6GEYJ333V	1	33 kΩ/0.125 W/0805/5%
R13	Vishay	Y16309K00000B9R	1	9 kΩ/0.25 W/1206/0.1%
R15	Yageo	CFR-50JB-52-10K	1	10 kΩ/0.5 W/5%
R16	Vishay Dale	CRCW08055K00FKTA	1	5 kΩ/0.125 W/0805/1%
R17			1	
R21	Panasonic	ERJ-6GEYJ471V	1	470 Ω/0.125 W/0805/5%
RB1, RB2	Panasonic	ERJ-8GEYJ105V	2	1 MΩ/0.25 W/1206/5%
RCP	Panasonic	ERJ-14YJ100U	1	10 Ω/0.5 W/1210/5%
RCS1, RCS2, RCS3	Panasonic	ERJ-8BQJ1R0V	3	1.0 Ω/0.5 W/1206/5%
RCS5, RCS6, RCS7	Stackpole Electronics Inc.	RMCF1206FT3R30	3	3.3 Ω/0.25 W/1206/1%
RG1, RG3	Panasonic	ERJ-8GEYJ220V	2	22 Ω/0.25 W/1206/5%
RIN1, RIN2	Panasonic	ERJ-8GEYJ752V	2	7.5 kΩ/0.25 W/1206/5%
RS1, RS2	Panasonic	ERJ-8GEYJ154V	2	150 kΩ/0.25 W/1206/5%
V_{BUS}	Keystone	5003	1	0.04 inch diameter orange
V_{BUS} (HV), VCC, VDC (HV)	Keystone	5000	3	0.04 inch diameter red
VR1	Wurth	820443211E	1	320 V AC/418 V DC/6 kA
BR1	Vishay	GBU4J-E3/51	1	600 V/4 A
C1	TDK	C3216CH2J221J060AA	1	220 pF/630 V/1206
C2	Rubycon	450BXW22MEFR12.5X20	1	22 µF/450 V/Radial
C12	Samsung Electro-Mechanics	CL31B475KAHVPNE	1	4.7 µF/25 V/X7R/1206

C13	Samsung Electro-Mechanics	CL21B104KACNNNC	1	0.1 µF/25 V/X7R/0805
C15, C19	Kemet, TDK	C0805C102K3GEC, C2012X7R2E102K085AA	2	1 nF/25 V/0805/10%, 1 nF/250 V/0805/10%
C17, C20	TDK	C2012X7R1H104K085AA	2	0.1 µF/50 V/0805/10%
C18	TDK	C2012X7R1E105K125AB	1	1 µF/25 V/0805/10%
C21	Panasonic	EEU-FC1E390	1	39 µF/25 V
C22	TDK	C2012X7R2E472K085AA	1	4.7 nF/250 V/0805/10%
C23	Panasonic	EEU-EB1H220S	1	22 µF/50 V
C24	Kemet	C0805C223K3GEC	1	22 nF/25 V/0805/10%
C25	Kemet	C0805C183J3GAC7800	1	0.018 µF/25 V/0805/1%
C27, C31, C35, C36	TDK	C3216X7R2J103K115AA	4	10 nF/630 V/1206/10%
C32	Yageo	CC0805KRX7R8BB471	1	470 pF/25 V/0805/10%
C34	Kemet	C0805C220J5GACTU	1	22 pF/50 V/0805/1%
CCP	TDK	C3216CH1H333K085AA	1	33 nF/50 V/1206/10%
CDC	Panasonic	ECQ-E6334JF	1	0.33 µF/630 V/5%

8 Inductor specifications

8.1 PFC inductor

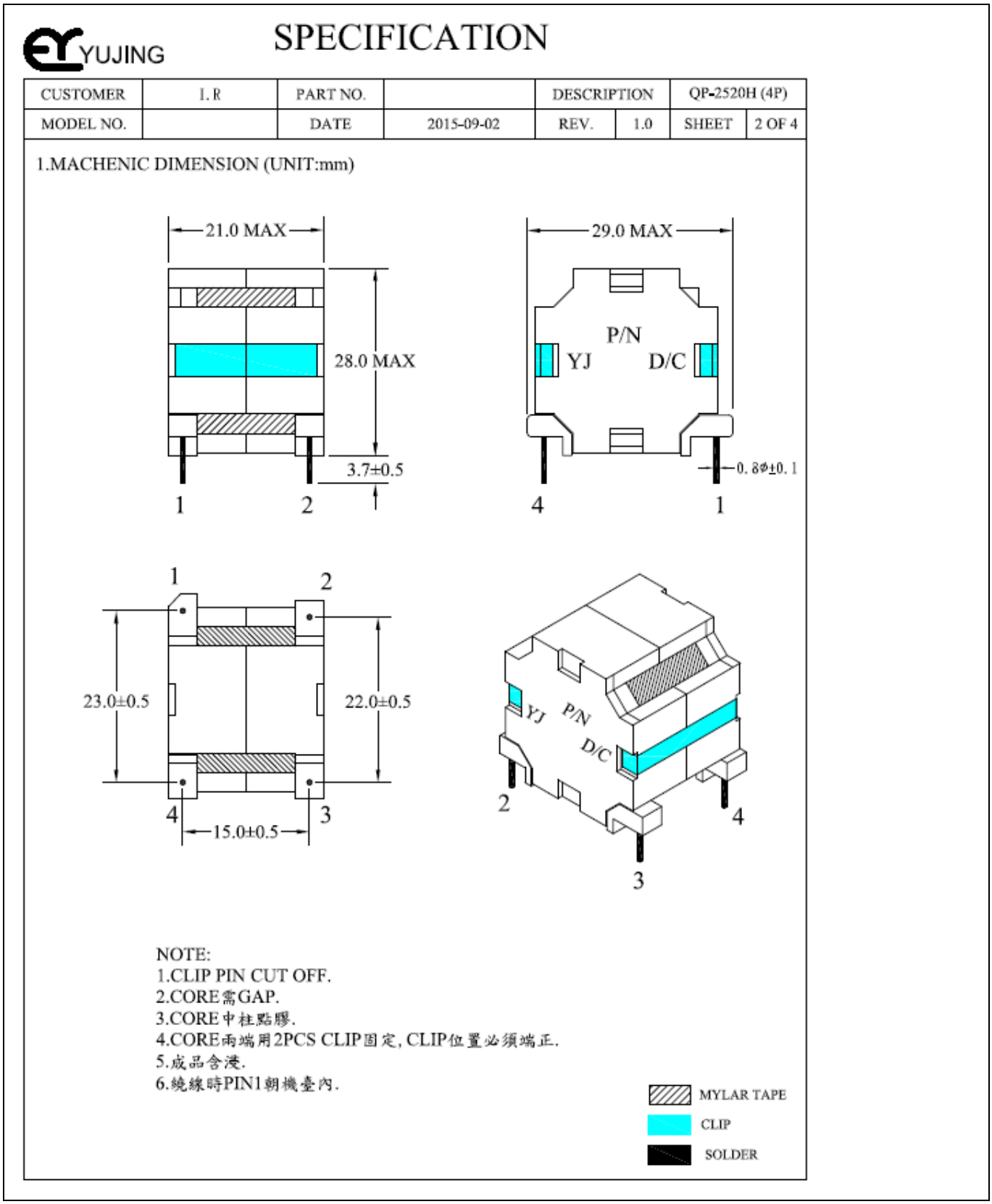


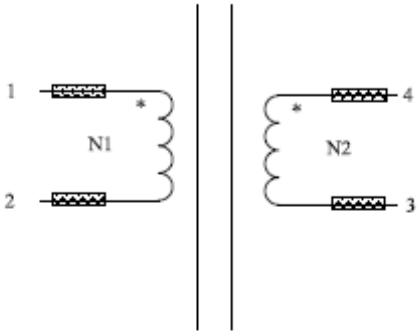
Figure 10 Boost PFC inductor specification

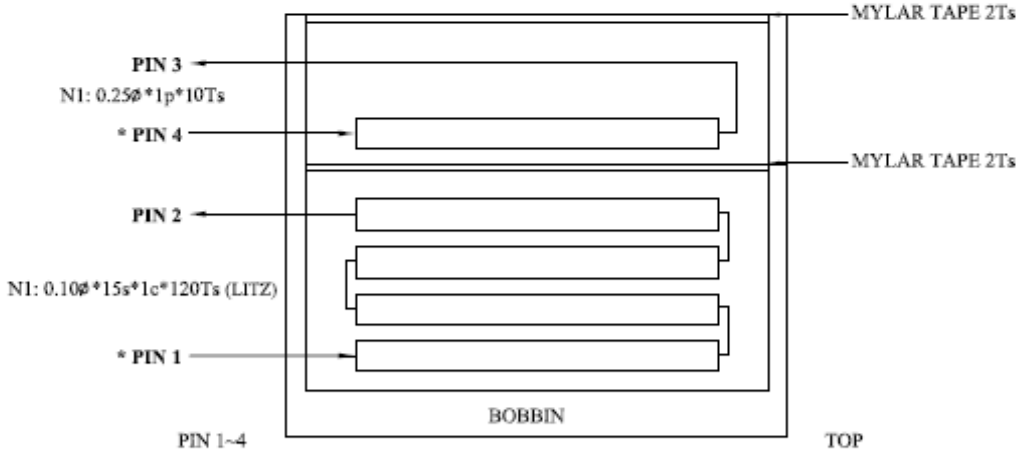
YUJING

SPECIFICATION

CUSTOMER	I. R	PART NO.		DESCRIPTION		QP-2520H (4P)	
MODEL NO.		DATE	2015-09-02	REV.	1.0	SHEET	3 OF 4

2.WINDING ORDER





NOTE:
套入線頭加TEFLON TUBE.

透明 TUBE

Figure 11 Boost PFC inductor specification

YUJING

SPECIFICATION

CUSTOMER	I. R	PART NO.		DESCRIPTION		QP-2520H (4P)	
MODEL NO.		DATE	2015-09-02	REV.	1.0	SHEET	4 OF 4

3.ELECTRICAL SPECIFICATION

HP: 4284A ZENTECH:WK5235, 502A , F = 10KHz V =1V AT 25°C

NO.	START	FINISH	WIRE	COLOR	TURNS	INDUCTANCE	DCR (mΩ)
L1	1	2	0.10ø*15s*1c(LITZ)	Y	120±0.5	1.2 mH±10%	1250 Max
L2	4	3	0.25ø*1c	Y	10±0.5		

4.DIELECTRIC STRENGTH

WITHSTANDING VOLTAGE: 1.0KV/3SEC/AC/ 3 mA , WINDING TO CORE
1.0KV/3SEC/AC/ 3 mA , WINDING TO WINDING

5.MATERIAL LIST

NO.	ITEM	TYPE	SUPPLIER	UL FILE NO.
1	BOBBIN	PM-9820/PM-9630	SUMITOMO BAKELITE CO., LTD.	E41429
2	CORE	QP25 3C94	FERROXCUBE	
		QP25 MB4	JFE	
3	WIRE	MW 75-C/UEW-4@	JUNG SHING WIIRE CO., LTD.	E174837
		MW 75-C/UEW/U@	PACIFIC ELECTRIC WIRE &CABLE (SHENZHEN) CO.,LTD	E201757
		MW 75-C/xUEW	FENG CHING METAL CORPORATION	E172395
4	WINDING TAPE	1350F-1	3M COMPANY	E17385
5	TUBE	TFL	GREAT HOLDING INDUSTRIAL CO.,LTD.	E156256
		TFL	FLUOTECH INDUSTRIAL CO.,LTD.	E175982(S)
		TFL	CHANG YUAN ELECTRONIC(SHENZHEN) CO., LTD.	E180908
6	ADHESIVE	ES2044P	CANADA SILICONE INC.	E223694
		3300ZH	EATTO ELECTRONIC MATERIAL CO., LTD.	E218090
7	VARNISH	WP-2952F-2G	HITACHI CHEMICAL CO., LTD.	E72979
8	CLIP	SK7	SHANGHAI DIAN QIANG PRODUCTS SUPPLYING CO.,LTD	

Figure 12 Boost PFC inductor specification

9 PCB layout

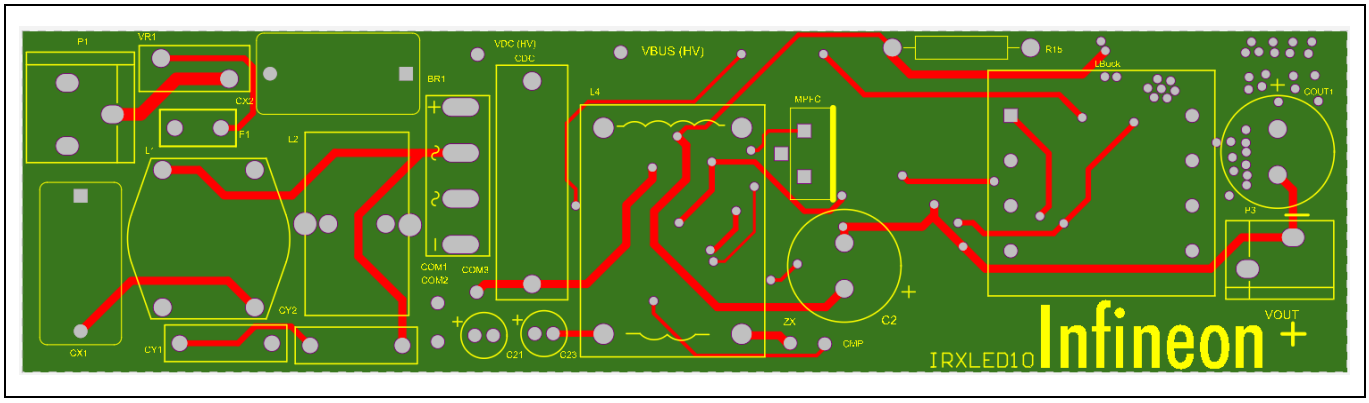


Figure 13 PCB top-side components and traces

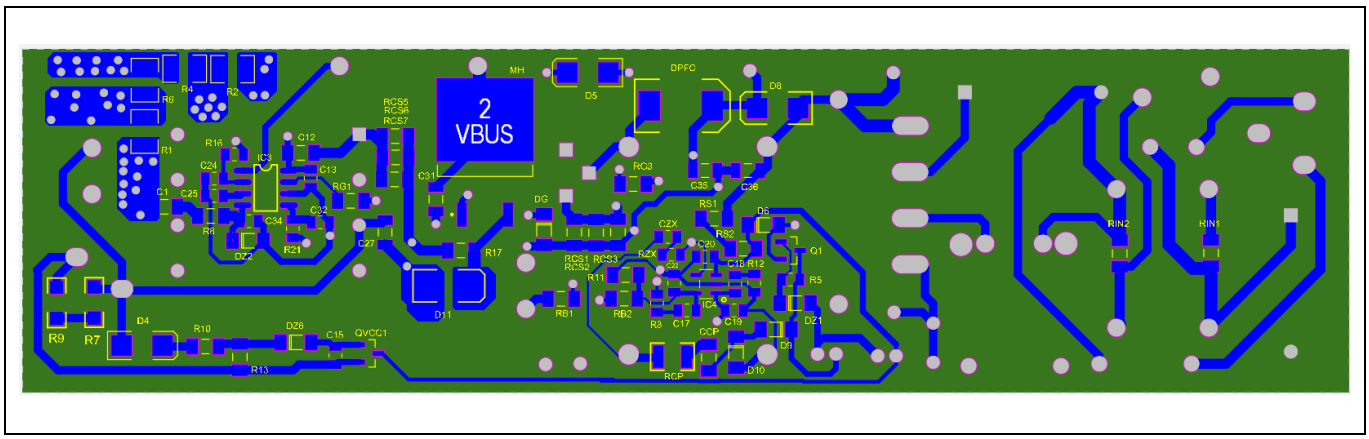


Figure 14 PCB bottom-side components and traces

9.1 PCB layout guidelines for system optimization

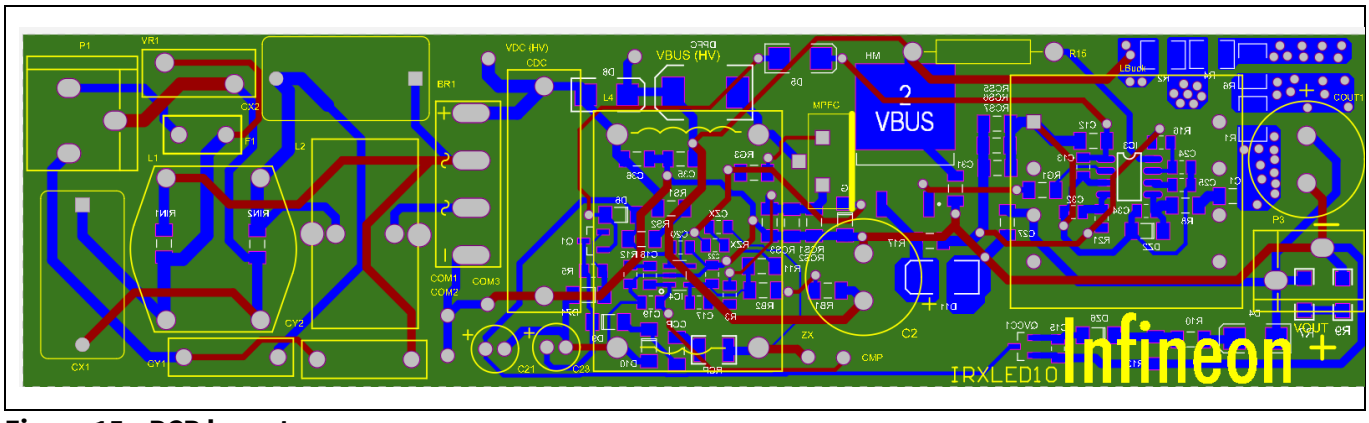


Figure 15 PCB layout

The primary loop on the left side of the board originates from the CDC connecting first to the PFC inductor (L4). The other side of the main winding is connected to the drain of the MOSFET (MPFC). To minimize EMI this trace is kept as short as possible and the loop is minimized. The CS resistors RCS1-3 are located such that the

connection to the High Frequency (HF) 0 V bus return of the CDC is as short as possible within the constraints of the PCB form factor. The other end of RCS1-3 is connected to the source of MPFC through a very short trace. The second PFC HF current loop also originates from L4 and the drain of MPFC, connecting through a short trace to DPFC, which then connects through another very short trace to C35. The negative side of C35 returns directly back to CDC through the shortest possible trace, providing the tightest HF current loop that the form factor allows. The layout techniques described minimize EMI emitted by the PFC pre-converter stage as far as possible.

The HF source capacitor is C31 for the second-stage buck converter. Here the same rules apply, keeping the HF switching loop as short as possible. The first HF AC loop is formed by C31, MH, LBuck and C27. The second HF AC loop is formed by D11, LBuck and C27. Therefore, in order to keep the layout very tight, these HF AC loop components are placed close to each other, thereby minimizing the loop area. This translates to lower EMI. Again the PCB form factor restricts layout optimization; however, since the buck stage is operating in forced CCM with ZVS, it is possible to meet conducted emission standards within these constraints.

Aside from EMI considerations, it is also essential to design the PCB so that PFC and buck controller ICs are able to operate correctly without suffering from potential interference caused by noise or incorrect grounding. It is also essential that decoupling capacitors C20 and C13 be located right next to IC3 and IC4 with direct connections to the V_{CC} and COM/0 V pins.

As in all switching power supplies, the signal and power grounds must be kept separate and join together only at the star points, which are at the negative side of the HF capacitor CDC for the PFC section and C31 for the buck section. Signal and power grounds are always kept separated, joining only at a point as close as possible to the negative side of the CS resistors.

Noise-sensitive components at the CMP inputs of IC4 and IFB inputs of IC3 need to be located close to the ICs with short connections to the signal grounds.

10 Test results

10.1 Operation under different line and load conditions

Table 1 Input 115 V AC, load 350 mA

Load (V)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	η	PF	iTHD	I_{OUTRP} (I_{pp})
200	73.43	201	0.365	79.65	92.19%	0.997	3.77%	21
190	69.68	190.7	0.365	75.43	92.37%	0.997	3.76%	19.9
180	66.24	181.6	0.365	70.09	94.51%	0.996	3.67%	18.5
170	62.20	170.4	0.365	66.79	93.12%	0.996	3.93%	16.5
160	58.84	161.2	0.365	63.88	92.11%	0.996	3.90%	16.1
150	54.57	149.5	0.365	59.44	91.80%	0.995	3.88%	15.3
140	51.06	139.9	0.365	55.75	91.59%	0.994	4.11%	14.8
130	47.49	130.1	0.365	51.89	91.51%	0.993	4.33%	14.7
120	43.98	120.5	0.365	48.17	91.31%	0.992	4.53%	13.1
110	40.19	110.1	0.365	44.15	91.02%	0.991	4.59%	14.40
100	36.76	100.7	0.365	40.52	90.71%	0.990	6.64%	14.40
90	32.85	90	0.365	36.36	90.35%	0.987	4.00%	15.80
80	29.31	80.3	0.365	32.56	90.02%	0.985	3.40%	16.77
70	25.84	70.8	0.365	28.86	89.54%	0.981	3.89%	17.67
60	21.99	60.25	0.365	24.79	88.71%	0.974	6.75%	18.77

Table 2 Input 230 V AC, load 350 mA

Load (V)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	η	PF	iTHD	I_{OUTRP} (I_{pp})
200	73.09	200.40	0.365	77.34	94.50%	0.95	7.32%	22.02
190	69.57	190.6	0.365	73.68	94.42%	0.947	6.48%	22.12
180	66.17	181.5	0.365	70.42	93.97%	0.943	6.67%	21.36
170	61.94	169.7	0.365	65.98	93.88%	0.937	6.4%	18.96
160	58.84	161.2	0.365	62.85	93.62%	0.932	7.53%	19
150	54.57	149.5	0.365	58.47	93.33%	0.925	6.72%	18.5
140	50.92	139.5	0.365	54.80	92.92%	0.917	7.14%	17.6
130	47.49	130.10	0.365	51.21	92.73%	0.908	7.28%	17
120	43.98	120.50	0.365	47.62	92.36%	0.897	8.13%	16.5
110	40.33	110.2	0.365	43.81	92.06%	0.883	8.55%	16.0
100	36.65	100.4	0.365	40.11	91.36%	0.867	9.41%	16.91
90	32.81	89.90	0.365	36.09	90.92%	0.845	9.96%	17.31
80	29.31	80.30	0.365	32.44	90.35%	0.82	10.42%	17.6
70	25.81	70.70	0.365	28.80	89.60%	0.789	11.50%	19.11
60	21.97	60.19	0.365	24.92	88.16%	0.747	12%	20

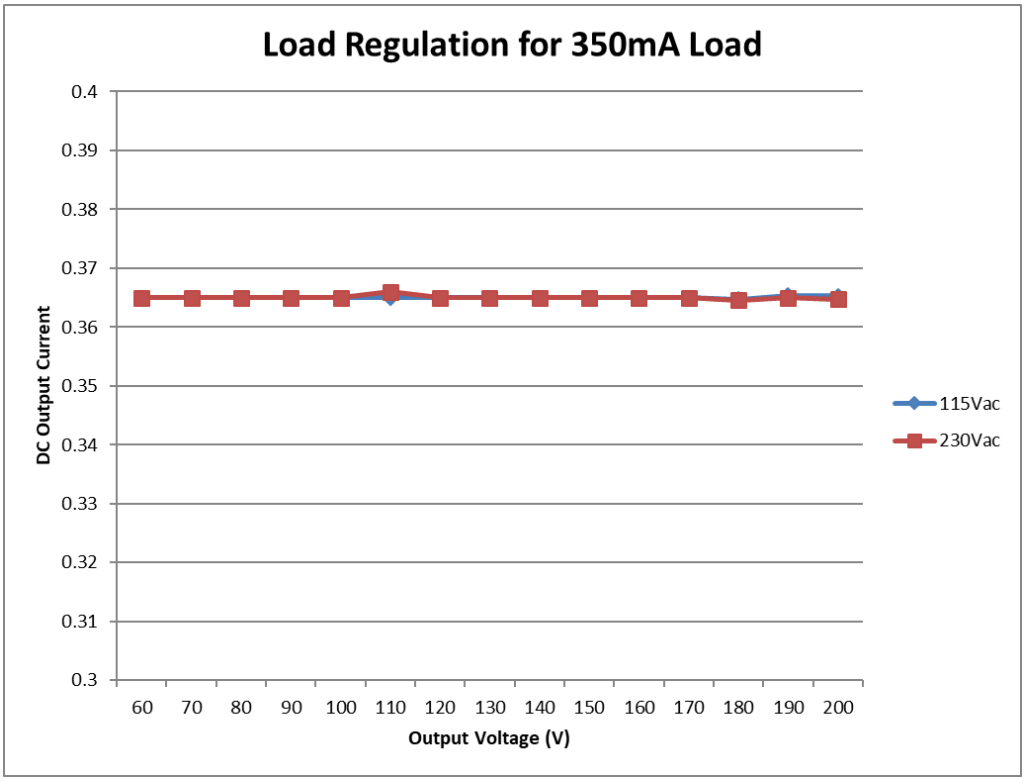


Figure 16 Load regulation at 350 mA output

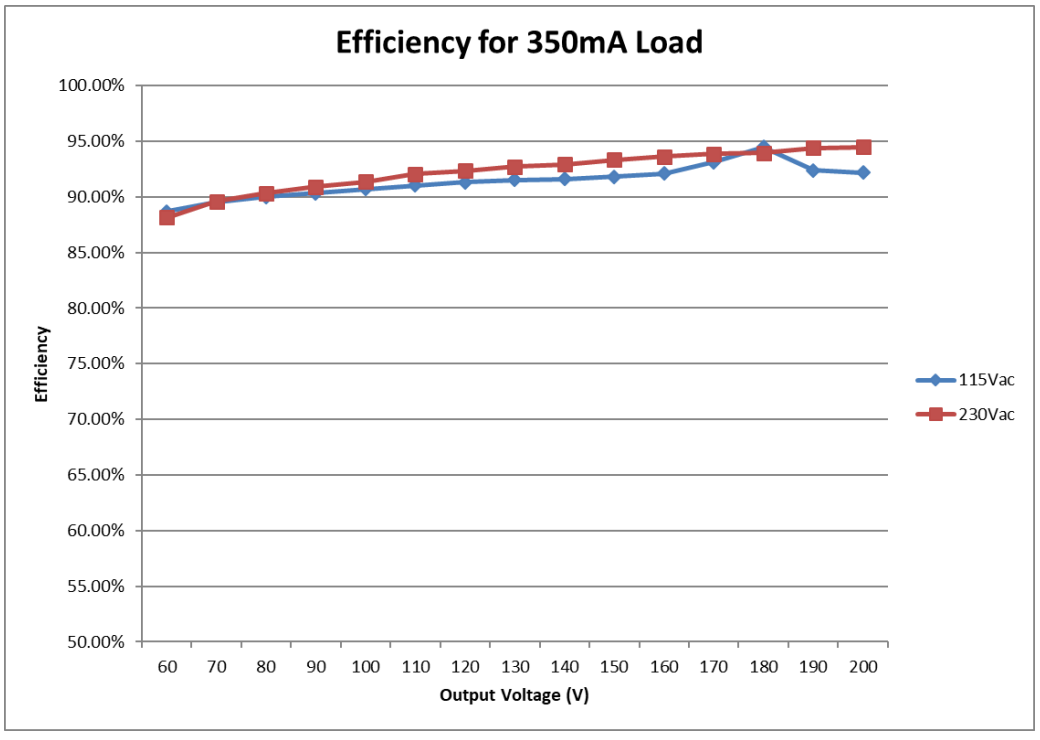


Figure 17 Efficiency at 350 mA output

10.2 Power factor and current harmonics (iTHD)

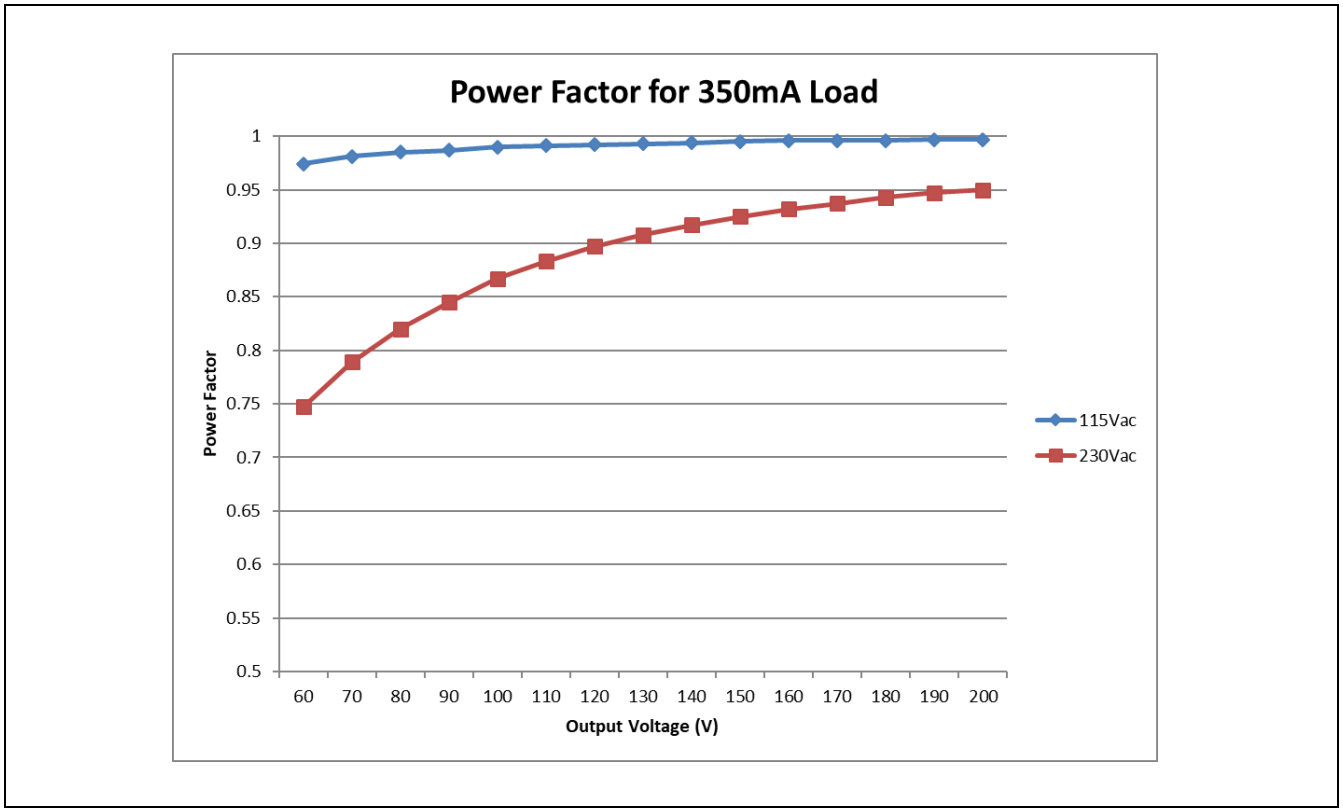


Figure 18 Power factor vs output voltage at 350 mA load

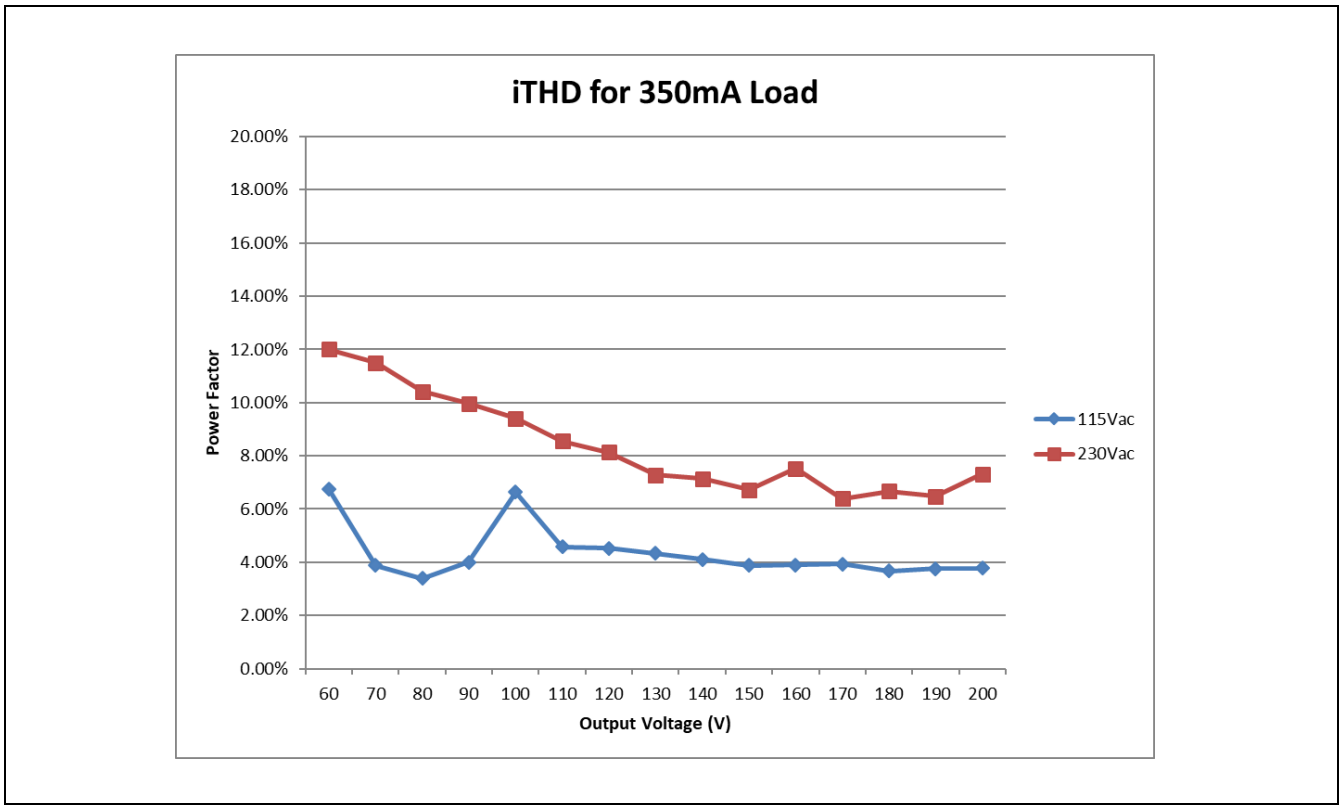


Figure 19 THDi vs output voltage at 350 mA load

Table 3 EN 61000-3-2 class C limits for system power greater than 25 W

	Harmonics limits class C according EN 61000-3-2 for system power >25 W	
	Harmonics order n	**Maximum value expressed as a percentage of the fundamental input current**
Requirements	2	<2%
	3	<30 λ %
	5	10%
	7	<7%
	9	<5%
	11 ≤ n ≤ 39	<3%
		λ = power factor

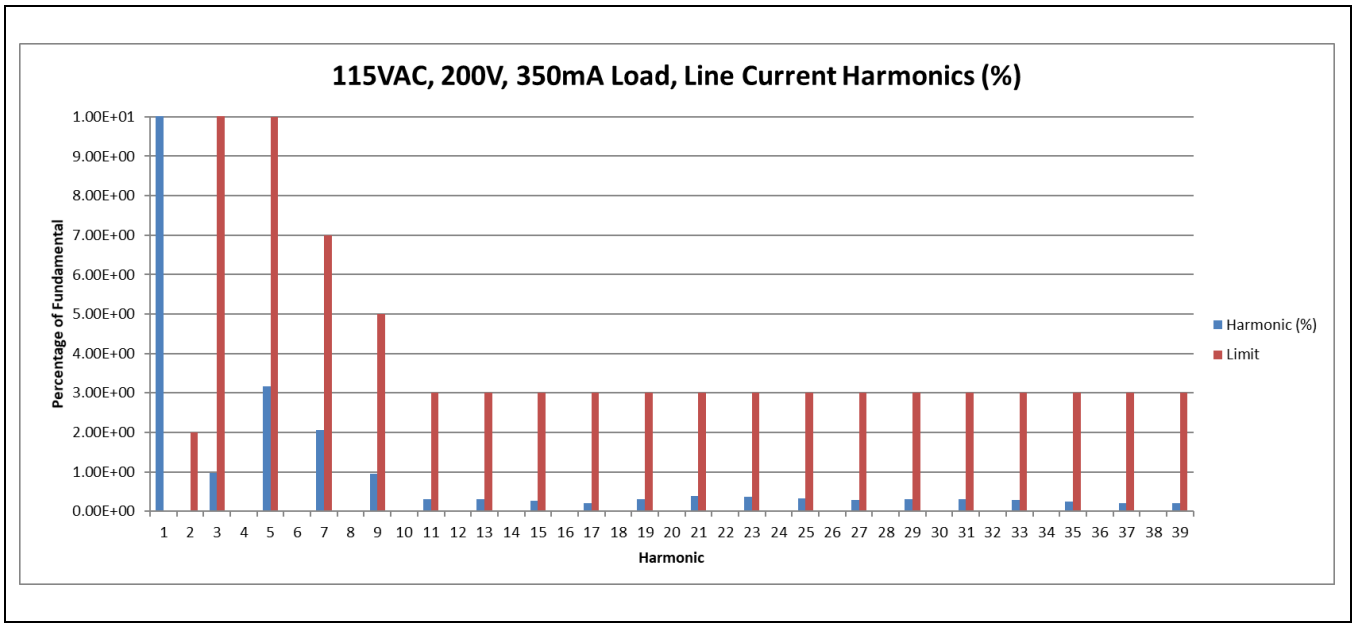


Figure 20 Harmonic test results at 115 V AC and 350 mA, 200 V load

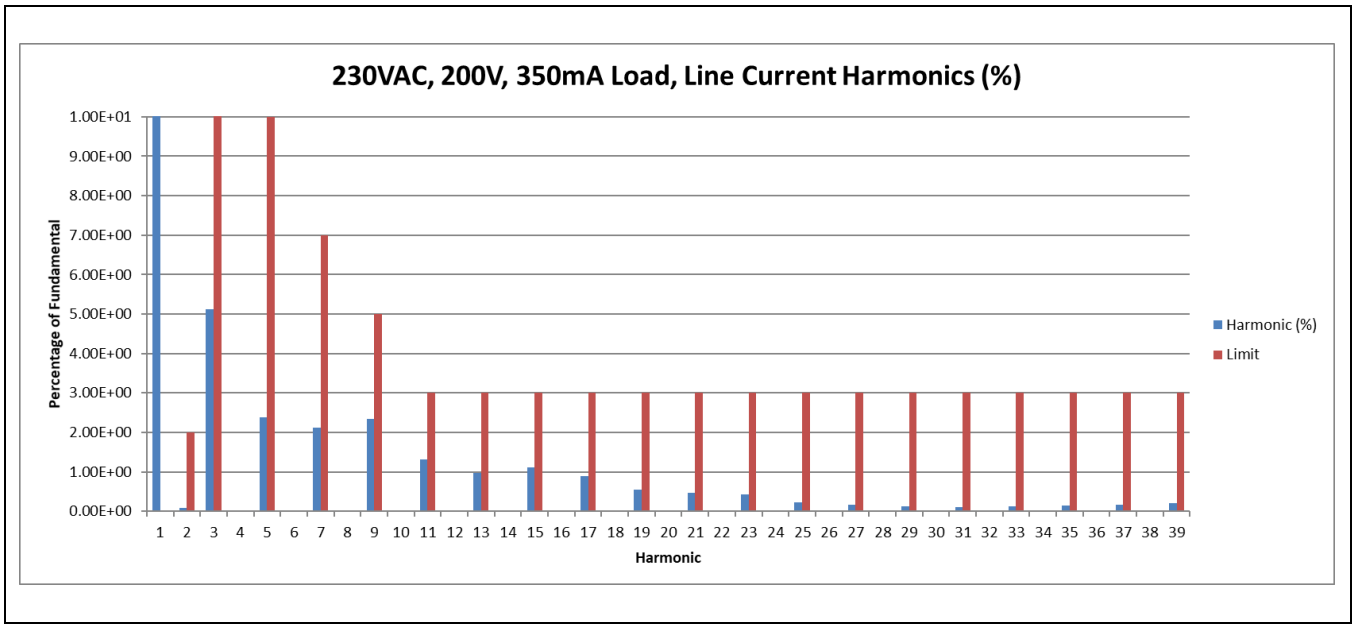


Figure 21 Harmonic test results at 230 V AC and 350 mA, 200 V load

Class C limits are met at 100 percent load.

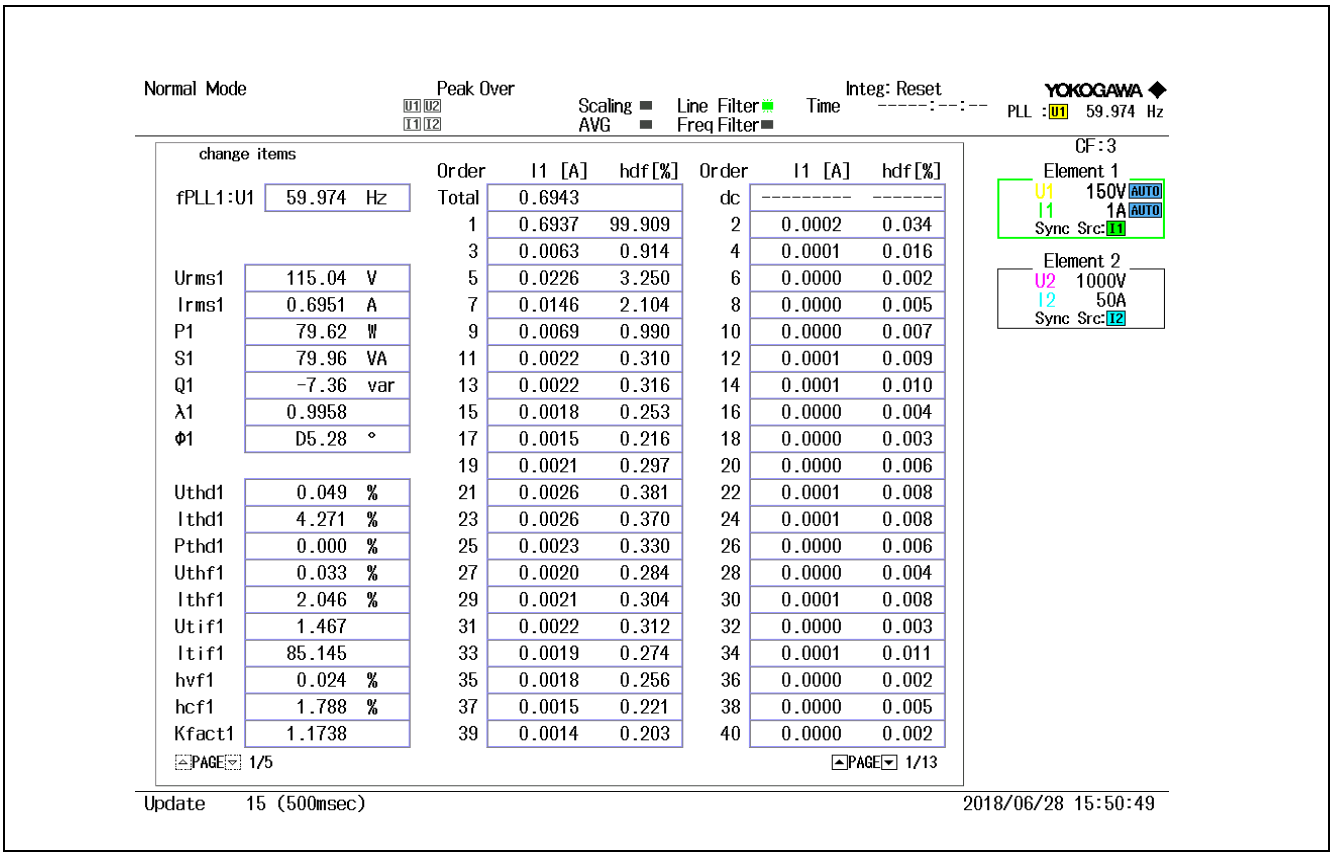


Figure 22 Harmonic test results at 115 V AC and 350 mA, 200 V load

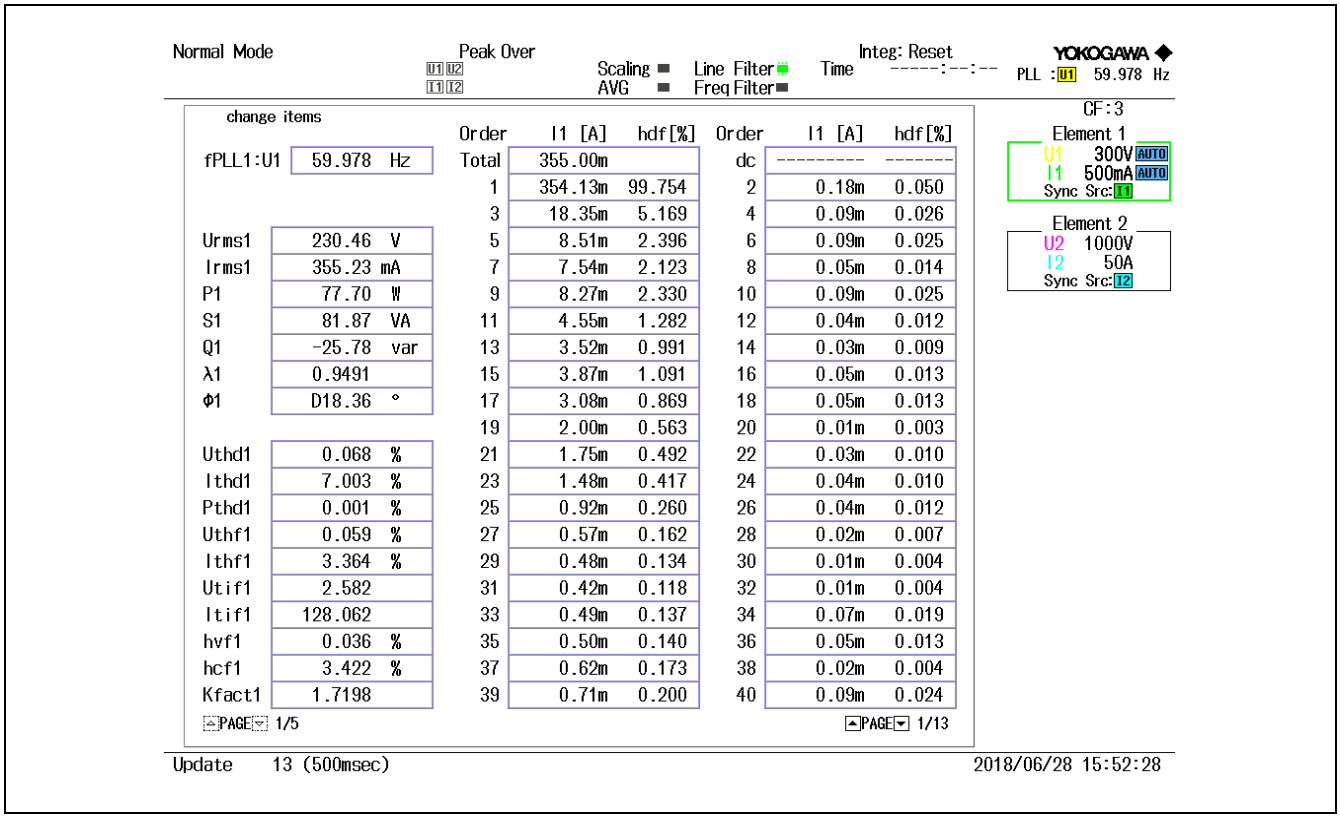


Figure 23 Harmonic test results at 230 V AC and 350 mA, 200 V load

As seen from the above figures, the class C limits are met at maximum load.

10.3 Operating waveforms

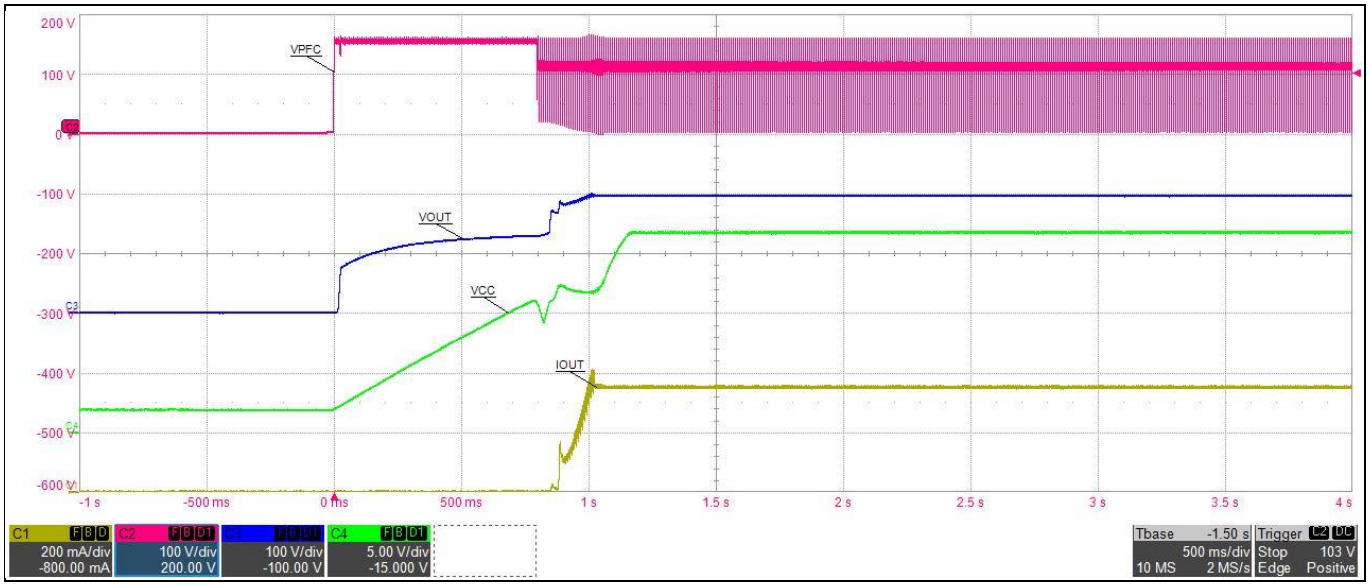


Figure 24 Start-up at 350 mA, 200 V LED load, 115 V AC input
PFC input bus (red), V_{CC} (green), output voltage (purple), output current (yellow)

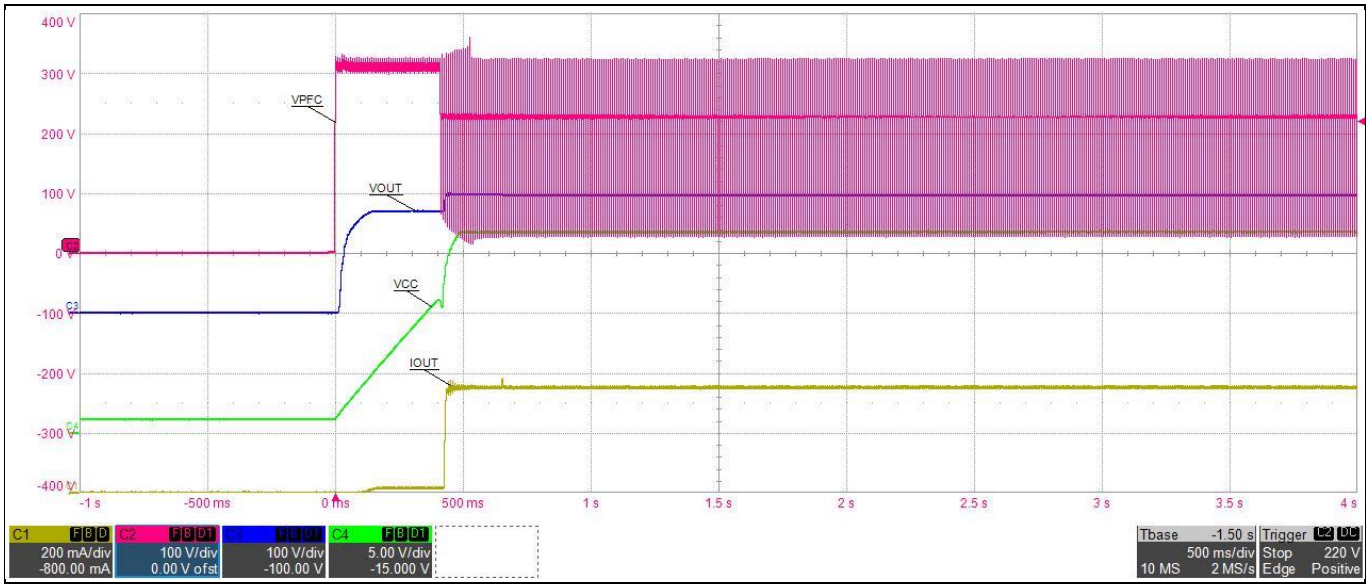


Figure 25 Start-up at 350 mA, 200 V LED load, 230 V AC input
PFC input bus (red), V_{CC} (green), output voltage (purple), output current (yellow)

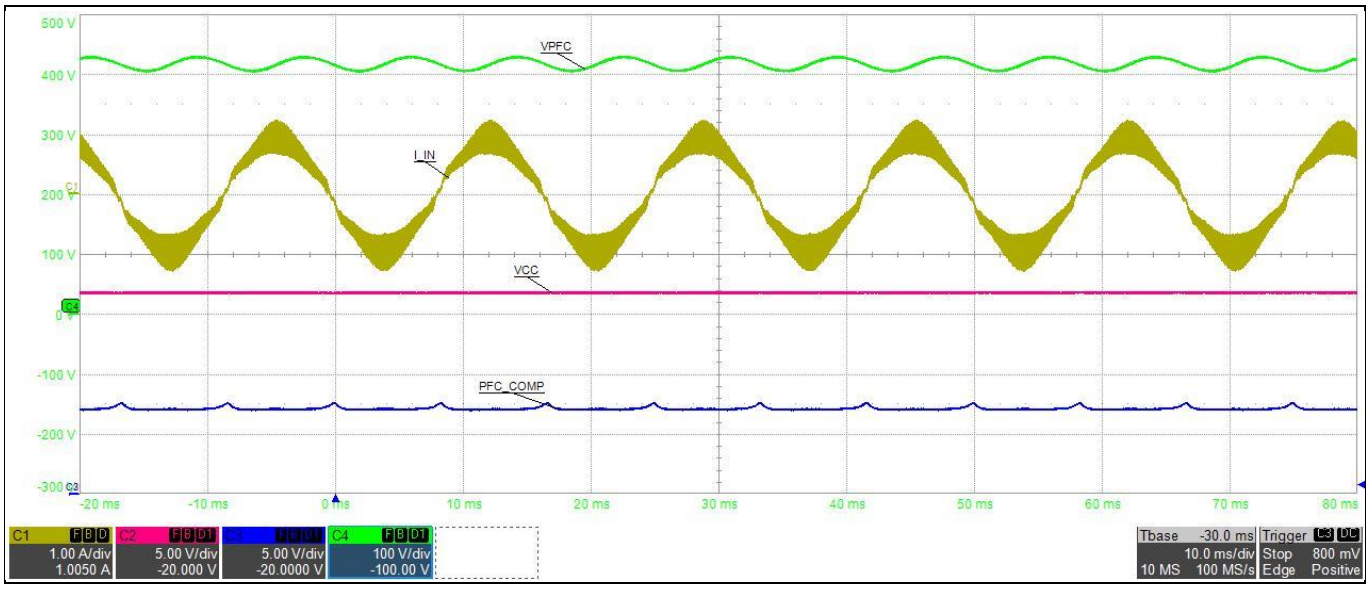


Figure 26 Steady-state operation of PFC at 350 mA, 200 V load, 115 V AC input
PFC output voltage (green), input AC current (yellow), V_{CC} (red), PFC COMP (purple)

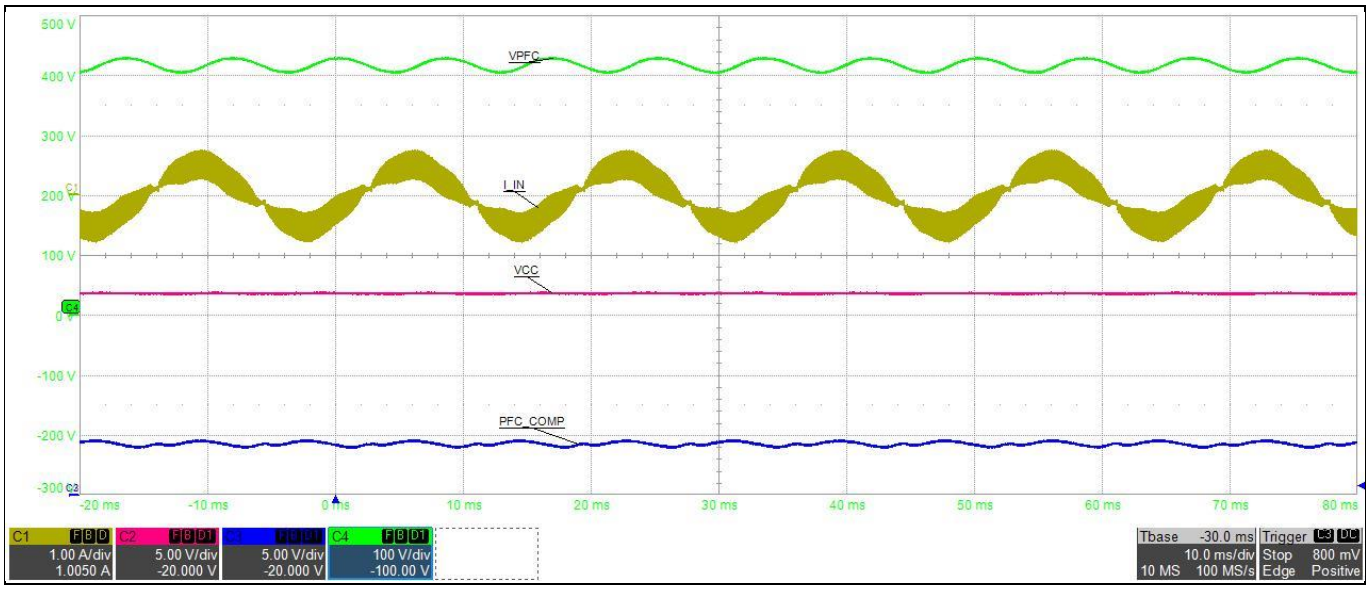


Figure 27 Steady-state operation of PFC at 350 mA, 200 V load, 230 V AC input
PFC output voltage (green), input AC current (yellow), V_{CC} (red), PFC COMP (purple)

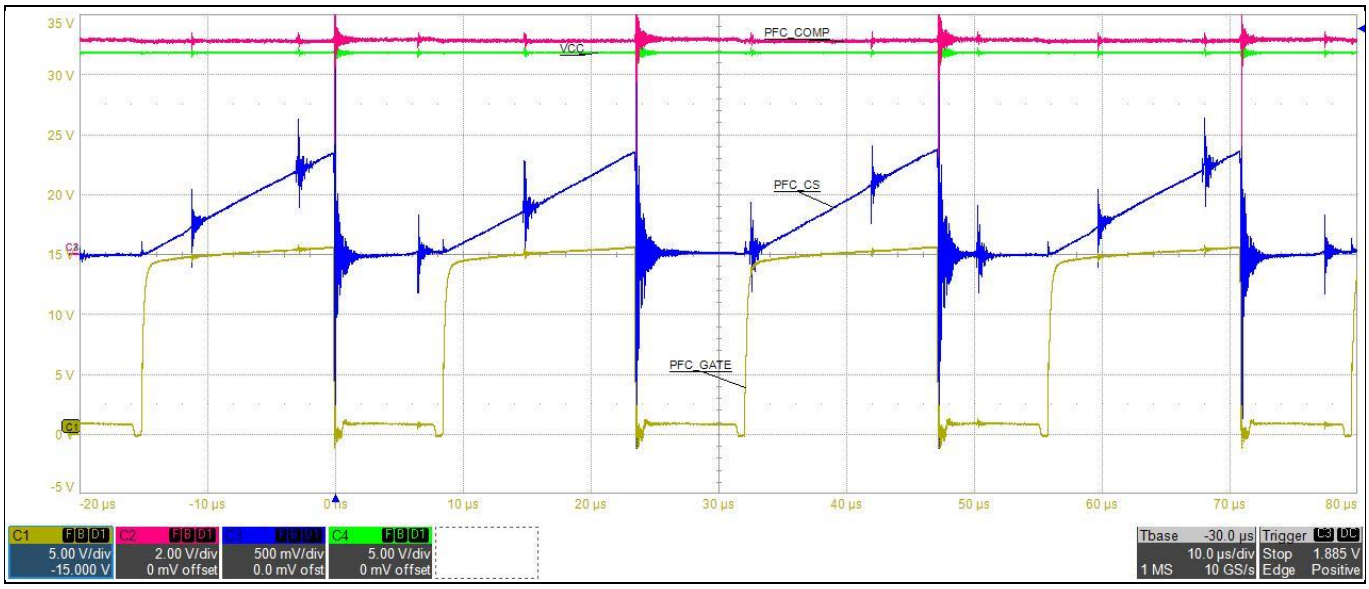


Figure 28 Steady-state operation of PFC at 350 mA, 200 V load, 115 V AC input V_{CC} (green), PFC gate Vgs (yellow), PFC CS (purple), PFC COMP (red)

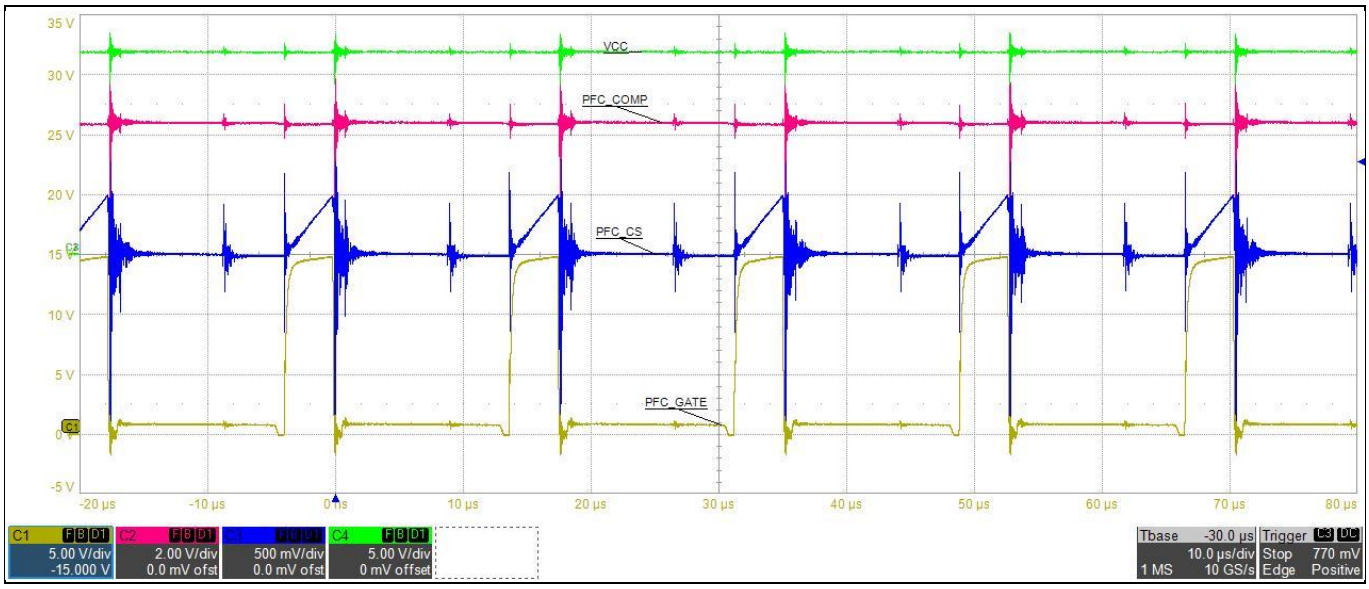


Figure 29 Steady state operation of PFC at 350 mA, 200 V load, 230 Vac input VCC (green), PFC Gate Vgs (yellow), PFC CS (purple), PFC COMP (red)

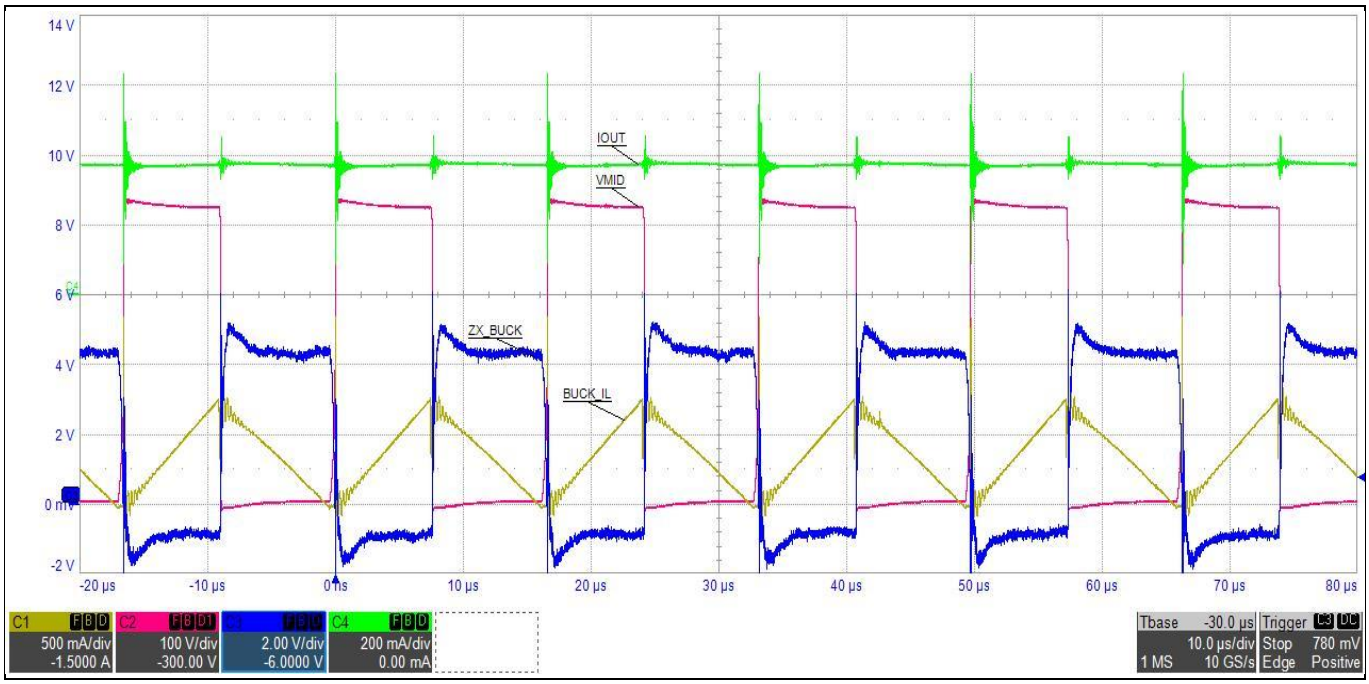


Figure 30 Steady-state operation of buck at 350 mA, 200 V LED load
Output current (green), buck inductor current (yellow), buck ZC (purple), wwitch node (purple)

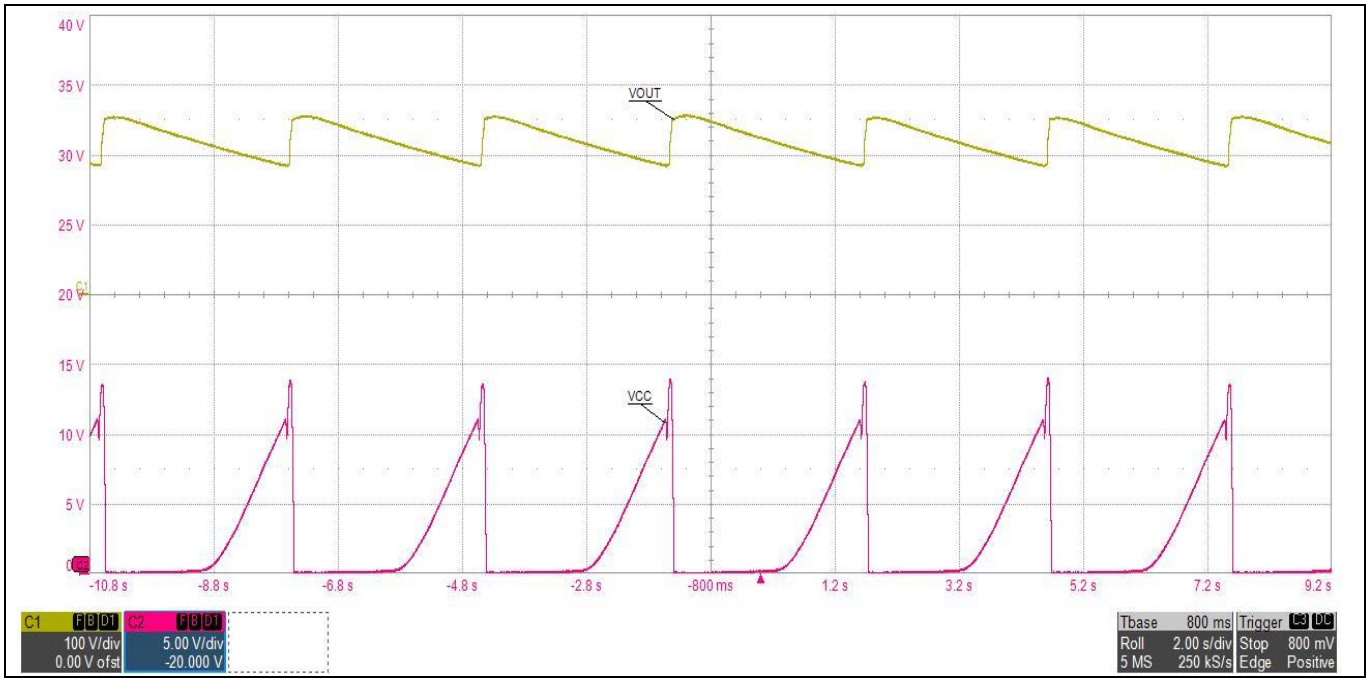


Figure 31 Open-circuit protection
Output voltage (yellow), V_{CC} (red)

10.4 Thermal performance under normal operating conditions

Thermal images captured under conditions of 120 V AC input, 200 V/350 mA load:

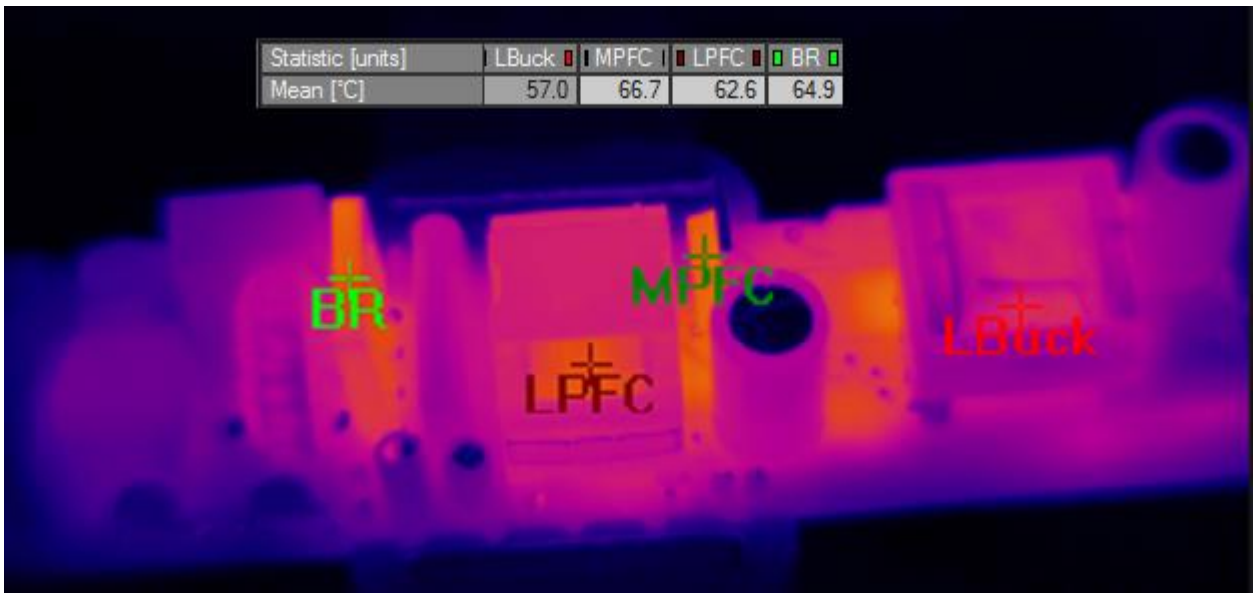


Figure 32 Top-side thermal image

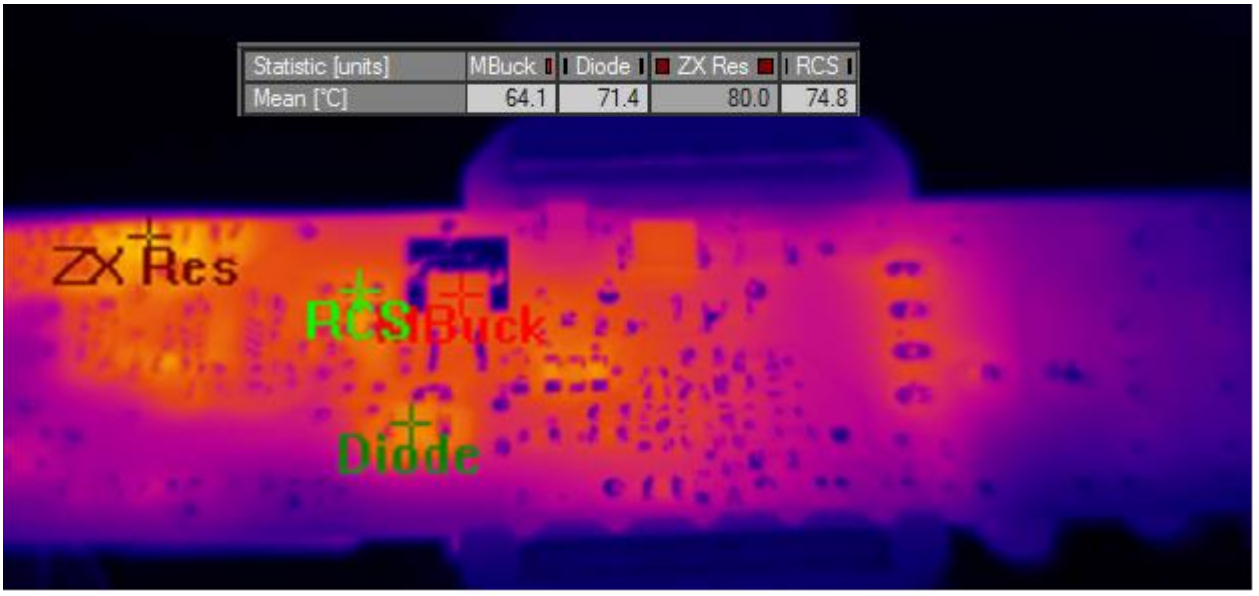


Figure 33 Bottom-side thermal image

Thermal images captured under conditions of 230 V AC input, 200 V/350 mA load:

Figure 34 Top-side thermal image

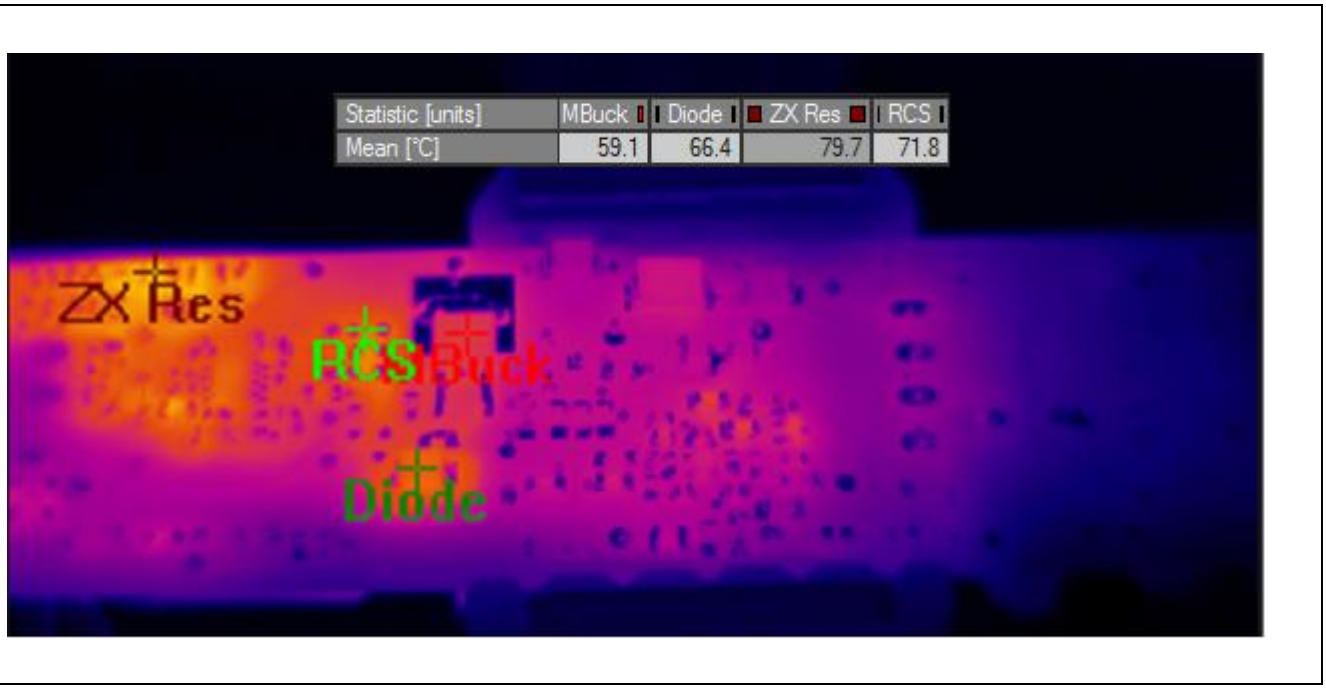


Figure 35 Bottom-side thermal image

10.5 Conducted EMI

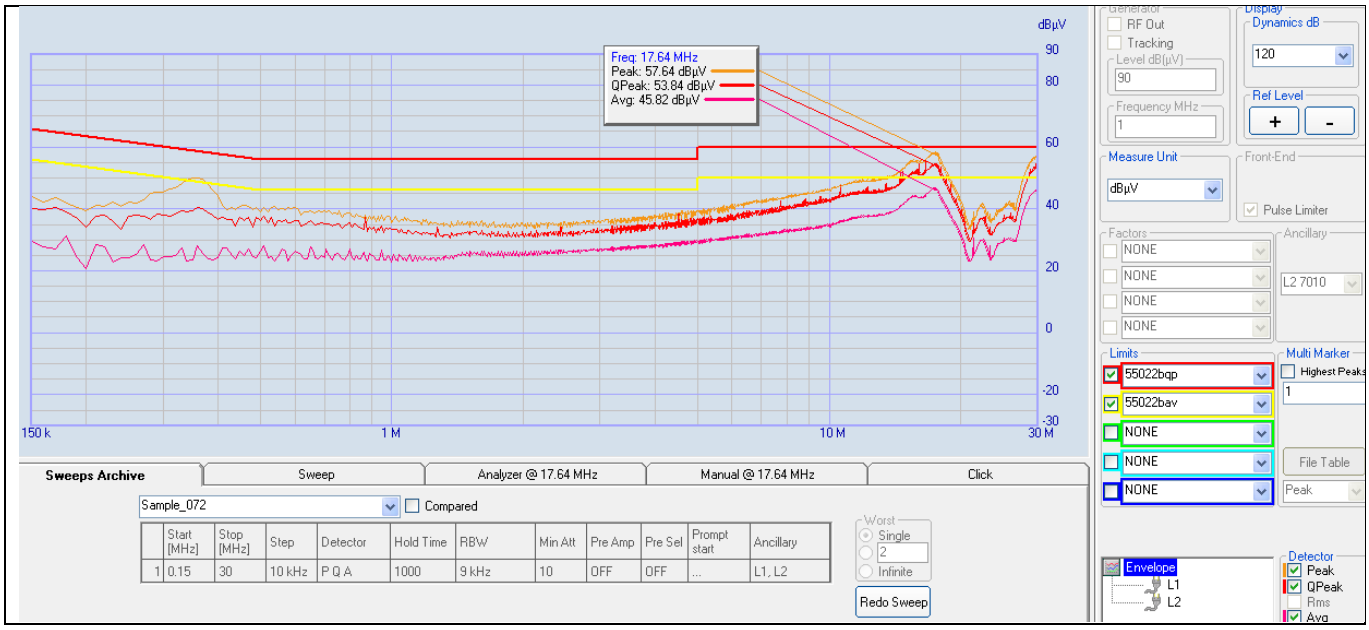


Figure 36 Conducted emissions at 120 V AC and 100 percent load

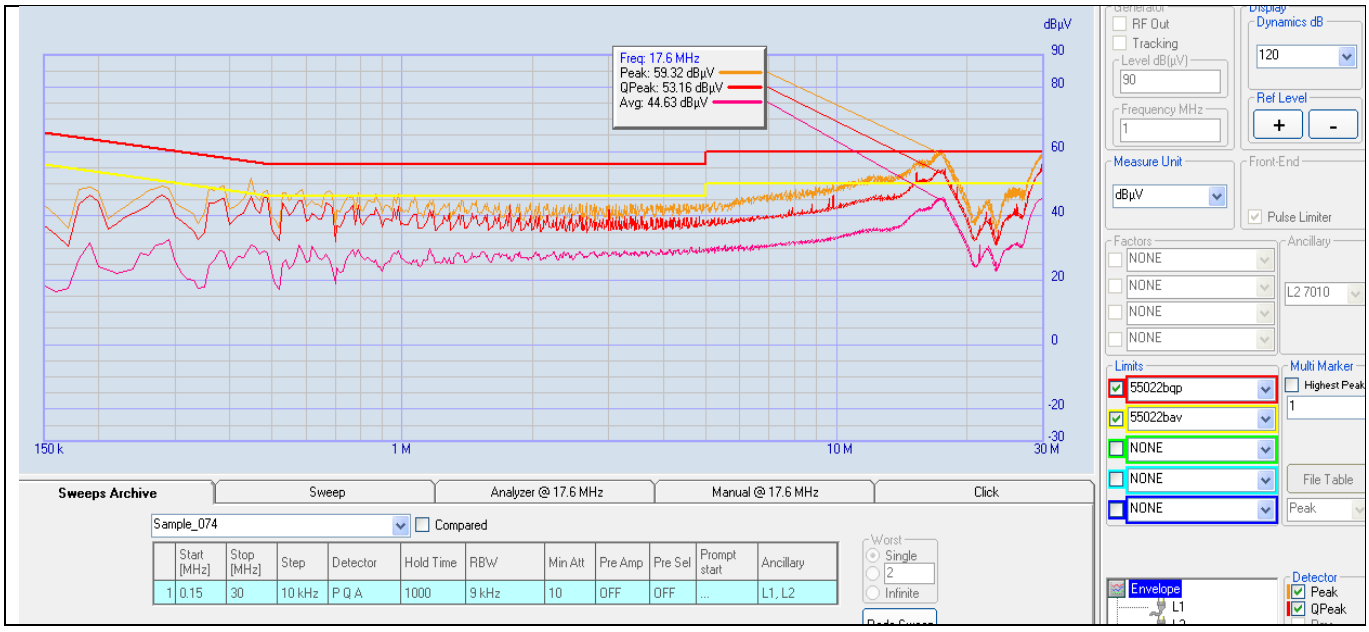


Figure 37 Conducted emissions at 230 V AC and 100 percent load

The limit lines in the above figures represent EN 55022 class B limits for the quasi-peak in red and average in yellow. Frequency sweep measurements are shown in red for quasi-peak and pink for average. The reults provided here are from pre-compliance tests only. These were not carried out at a certified test lab. For compliance with the standard the traces must remain below their respective limit lines for both quasi-peak and average measurements, as shown in the table below.

Tests were carried out using a 200 V LED load attached to a grounded heatsink.

EMI emissions are very dependent on the board layout; please refer to section 9.1.

Table 4 EN 55022 class B limits for conducted EMI

CISPR22 class B conducted EMI limits		
Frequency emission (MHz)	**Quasi-peak**	**Average**
0.15 – 0.50	66 to 56*	56 to 46*
0.50 – 5.00	56	46
5.00 – 30.0	60	50
FCC part 15 class B conducted EMI limit		
Frequency emission (MHz)	**Quasi-peak**	**Average**
0.15 – 0.50	66 to 56*	56 to 46*
0.50 – 5.00	56	46
5.00 – 30.0	60	50
*Decreases with logarithm of the frequency		

Note

Infineon Technologies does not guarantee compliance with any EMI standard

11 Conclusion

The IRXLED10 evaluation board demonstrates a cost-competitive two-stage PFC plus CC buck LED driver with the PFC stage controlled by the low-cost IRS2505L and the buck stage controlled by IRS2982. It is shown that the IRS2982 can be used in a ground-referenced buck converter where the controller is referenced to the switching node. It operates in CrCM by means of a floating ZC signal obtained from an RC network connected to the DC bus without the need for additional inductor winding. A very tight current regulation has been achieved over a wide line/load range. Accuracy of regulation over output voltage remains within +/-0.5 percent of the nominal output over a three-to-one voltage range.

The start-up time of the LED driver over the input range is 1.1 s at 115 V AC and less than 0.5 s at 230 V AC. The power factor is greater than 0.9 and the iTHD remains less than 12 percent over the full range of AC-line input. The thermal temperature of the board remains less than 90°C.

The output voltage range for the 350 mA is set from 60 V up to 200 V. This covers sufficient load range, below which it would not make economic sense to use this LED driver.

Test results show that the design specifications are met.

References

[1] IRS2505LPBF SMPS control IC datasheet, Infineon Technologies.

[2] IRS2982S SMPS control IC datasheet, Infineon Technologies.

[3] IRS2505L µPFC control IC design guide, Peter B. Green and Helen Ding, Infineon Technologies.

https://www.infineon.com/dgdl/an_201508_pl16_012.pdf?fileId=5546d462533600a4015364c508a02a2f

[4] 90 W PFC evaluation board for the IRS2505L, Peter B. Green, Infineon Technologies

https://www.infineon.com/dgdl/Infineon-aneval_201511_pl16_012-AN-v02_00-EN.pdf?fileId=5546d462533600a40153559ff7761263

Revision history

Major changes since the last revision

Page or reference	Description of change
	First release

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