Multi-output power factor flyback converter design using IRS2982S

Authors: Kali Naraharisetti
Peter B. Green

About this document

Scope and purpose

The purpose of this document is to provide a comprehensive functional description and guide to using the IRS2982S control IC for LED and general-purpose SMPS. The scope applies to all technical aspects that should be considered in the design process, including calculation of external component values, MOSFET selection and PCB layout optimization as well as additional circuitry that may be added if needed in certain cases.

Intended audience

Power supply design engineers, applications engineers, students.

Table of contents

1 Introduction

The IRS2982S is a versatile SMPS controller IC primarily intended for LED drivers in the 5 to 100 W power range suitable for buck, buck-boost and flyback converters operating in Critical Conduction Mode (CrCM) and Discontinuous Conduction Mode (DCM) at light loads. Flyback converters will be covered in this application note focusing on an isolated voltage-regulated design with Power Factor Correction (PFC).

All of the control and protection required for the converter is integrated in the IRS2982S as well as a HV start-up cell to enable rapid illumination at switch-on over a wide line input voltage range. The IRS2982S is also able to provide PFC in a single-stage flyback converter able to meet class C (lighting) line current harmonic limits of the EN 61000-3-2 standard.

A 36 W multiple-output isolated constant voltage-regulated PFC flyback evaluation board based on the IRS2982S controller is described in detail in this application note and detailed test results are presented.

Figure 1 IRXPSU1 36 W flyback evaluation board (top)

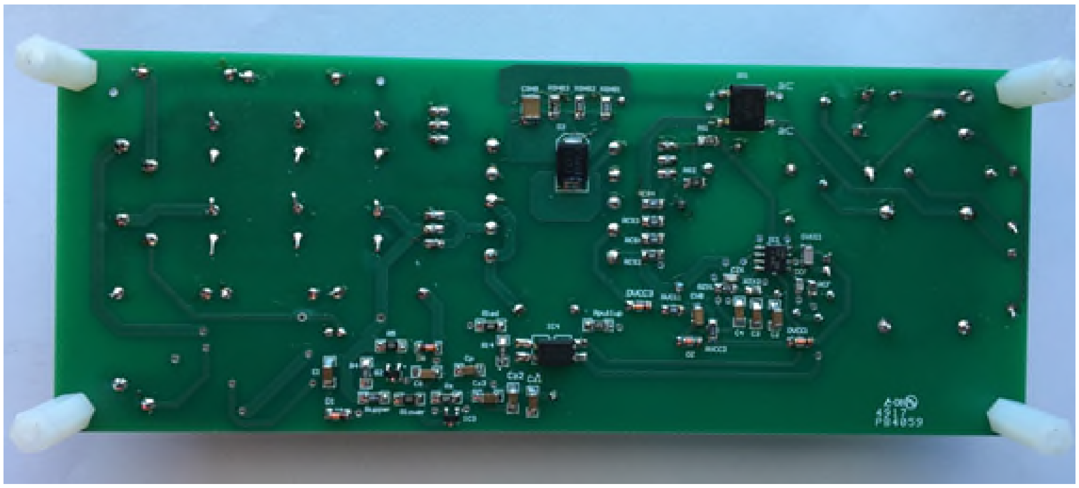


Figure 2 IRXPSU1 36 W flyback evaluation board (bottom)

2 IRS2982S functional overview

The IRS2982S is comprised of the following functional blocks:

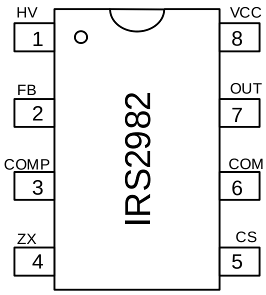
1. *HV start-up cell*
   The IC internal functional blocks remain disabled in low power mode until V_{CC} first rises above the V_{CCUV+} Under Voltage Lockout (UVLO) threshold, continuing to operate while V_{CC} remains above V_{CCUV-}. V_{CC} is initially supplied through the integrated HV start-up cell, which supplies a controlled current from the HV input provided a voltage greater than V_{HVSMIN} is present. The current supplied is limited to I_{HV_CHARGE}, reducing to less than I_{HVS_OFF} when V_{CC} reaches the cut-off threshold V_{HVS_OFF1}. The HV start-up cell switches over from start-up mode to support mode after the feedback (FB) input has exceeded V_{REG} for the first time. In this mode the cut-off threshold becomes V_{HVS_OFF2}. During steady-state operation under all line-load conditions V_{CC} is supplied through an auxiliary winding on the flyback transformer with V_{CC} high enough that the HV start-up does not supply current. If the auxiliary supply were unable to maintain V_{CC}, the HV start-up cell operating in support mode would supply current to assist.

2. *PWM controller*
   The SMPS control section operates in voltage mode where the gate drive output on-time is proportional to the error amplifier output voltage appearing at the compensation output COMP. An external capacitor C_{COMP} (shown in Figure 4) connected to 0 V (ground) acts with the trans-conductance characteristic of the error amplifier to provide loop compensation and stability. Minimum on-time is reached when V_{COMP} falls to $V_{COMPOFF}$, below which the gate drive is disabled. Under very light load conditions V_{COMP} transitions above and below $V_{COMPOFF}$ to produce burst mode operation. Off-time is determined by the demagnetization signal received at the ZX input, which is derived from the auxiliary transformer winding that supplies V_{CC} through a resistor divider. Internal logic limits the minimum off-time to t_{OFFMIN}, therefore the system transitions from CrCM to DCM at light loads. If the ZX input signal fails to provide triggering the next cycle will start automatically after a re-start period of t_{WD}.

3. *Protection*
   The IRS2982S includes cycle-by-cycle primary Over Current Protection (OCP), which causes the gate drive to switch off if the voltage detected at the CS exceeds the threshold V_{CSTH}. This prevents the possibility of transformer saturation at low-line under heavy load but does not protect against output over-load or short-circuit.

Over Voltage Protection (OVP) is also provided through the ZX input, which provides a voltage proportional to the output voltage. This disables the gate drive output and pulls the COMP voltage below the $V_{COMPOFF}$ threshold. The error amplifier then starts to charge C_{COMP} until the gate drive starts up again at minimum on-time. Under an open-circuit output condition the OVP causes the converter to operate in burst mode, preventing the output voltage from rising too high.

The IRS2982S uses an SO-8 package as shown below:



Pin	Name	Description
1	*HV*	High voltage start-up Input
2	*FB*	Feedback input
3	*COMP*	Compensation and averaging capacitor input
4	*ZX*	Zero crossing and over voltage detection input
5	*CS*	Current sensing Input
6	*COM*	IC power and signal ground
7	*OUT*	Gate driver output
8	V_{CC}	Logic and low-side gate driver supply

Figure 3 IRS2982S pin assignments

3 Flyback converter

3.1 Flyback converter types

There are several configurations of flyback converter that may be used with the IRS2982S, depending on the application. These can be classified according to isolation and regulation requirements as follows:

1. Isolated or non-isolated
2. Current or voltage regulation

In the case of voltage regulation current limiting is needed for protection against over-load or short-circuit and in the case of current regulation OVP is necessary for an open circuit.

The IRS2982S can operate in any of the four combinations of (1) and (2). Extremely accurate current or voltage regulation is achieved in non-isolated converters since direct feedback to the FB input is possible. Isolation is however required in the majority of flyback converters. For isolated constant current regulation an opto-isolator is necessary; for isolated constant voltage regulation FB may be taken from the auxiliary winding as shown in Figure 4 with a small loss of line and load regulation accuracy. An opto-isolator is also necessary for highly accurate voltage regulation.

The basic circuit in Figure 4 shows the main elements of the IRS2982S-based PFC flyback converter. This can be used as a stand-alone power supply or as a front-end stage with a current-regulating buck regulator as the back-end stage in a dimmable (or non-dimmable) off-line LED driver. This front-end stage is able to provide a regulated output voltage over a wide range of line and load with sufficient accuracy for the majority of applications.

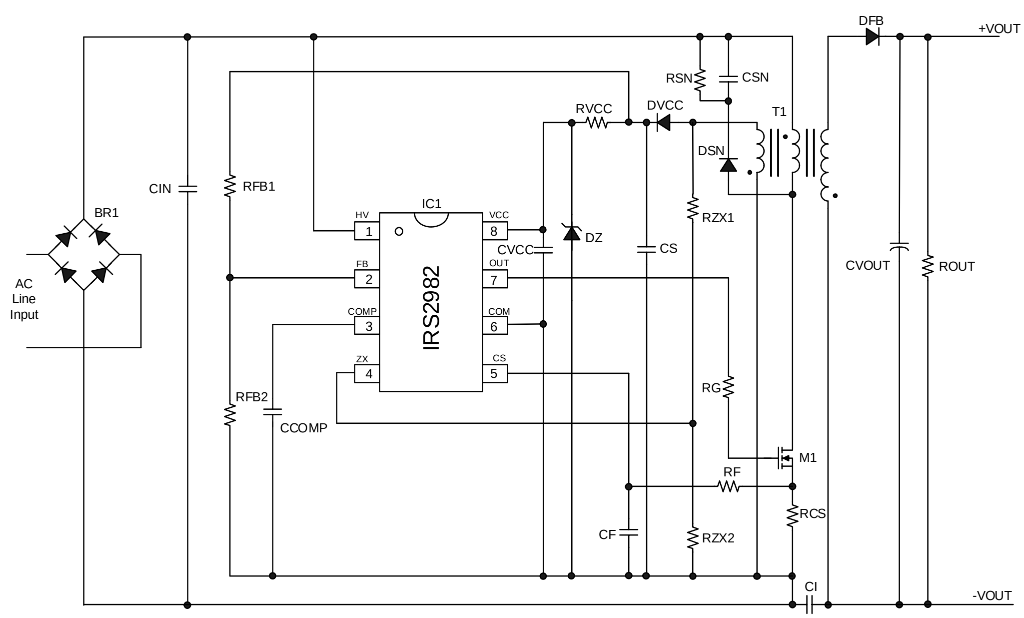


Figure 4 Isolated voltage-regulated flyback converter based on the IRS2982S

A 36 W PFC multiple-output flyback design as implemented in the IRXPSU1 evaluation board will be discussed in detail in the following sections.

3.2 Evaluation board specifications

Input and output at normal operation

- AC input voltage 90 V AC up to 265 V AC (45 to 65 Hz)
- Output voltages/output currents 3.3 V/0.15 A, 15 V/0.8 A, 30 V/0.8 A
- Maximum output voltage ripple on 3.3 V is +/-30 mV, 15 V is +/- 1 Vp-p, 30 V is +/- 1.5 Vp-p at full load
- Maximum output continuous power 36 W
- PF greater than 0.9, Total Harmonic Distortion (THD) less than 20 % for 40 % up to 100 % load over an AC-line of 115 V AC and 230 V AC
- Efficiency greater than 80 % for 50 % up to 100 % load over an AC-line of 115 V AC and 230 V AC
- Start-up time to reach the secondary nominal output voltages during full-load condition is less than 400 ms

Protection features

- Primary output OVP
- Cycle-by-cycle primary OCP

WARNING!
Output short-circuit and over-load protection are not provided on this evaluation board. This board can be damaged by sustained over-loading or short-circuiting the output!

Maximum component temperature

During worst-case scenario (ambient temperature 60°C) the maximum allowed component temperature is:

- Resistor less than 100°C
- Ceramic capacity, film capacity and electrolyte capacity less than 100°C
- Flyback transformer and chokes less than 100°C
- MOSFET, transistor and diodes less than 100°C
- IC less than 100°C

Dimensions of evaluation board

Maximum width 2.69 inches (68.4 mm), maximum length 6.98 inches (177.3 mm)

Safety requirements

The single-stage flyback converter should cover the safety requirements regarding EN 61347-2-13 and SELV maximum output voltage 60 V DC. This part of IEC 61347 specifies particular safety requirements for electronic control gear for use in DC supplies up to 250 V and AC supplies up to 1000 V at 50 Hz or 60 Hz and at an output frequency which can deviate from the supply frequency associated with LED modules.

4 Schematic

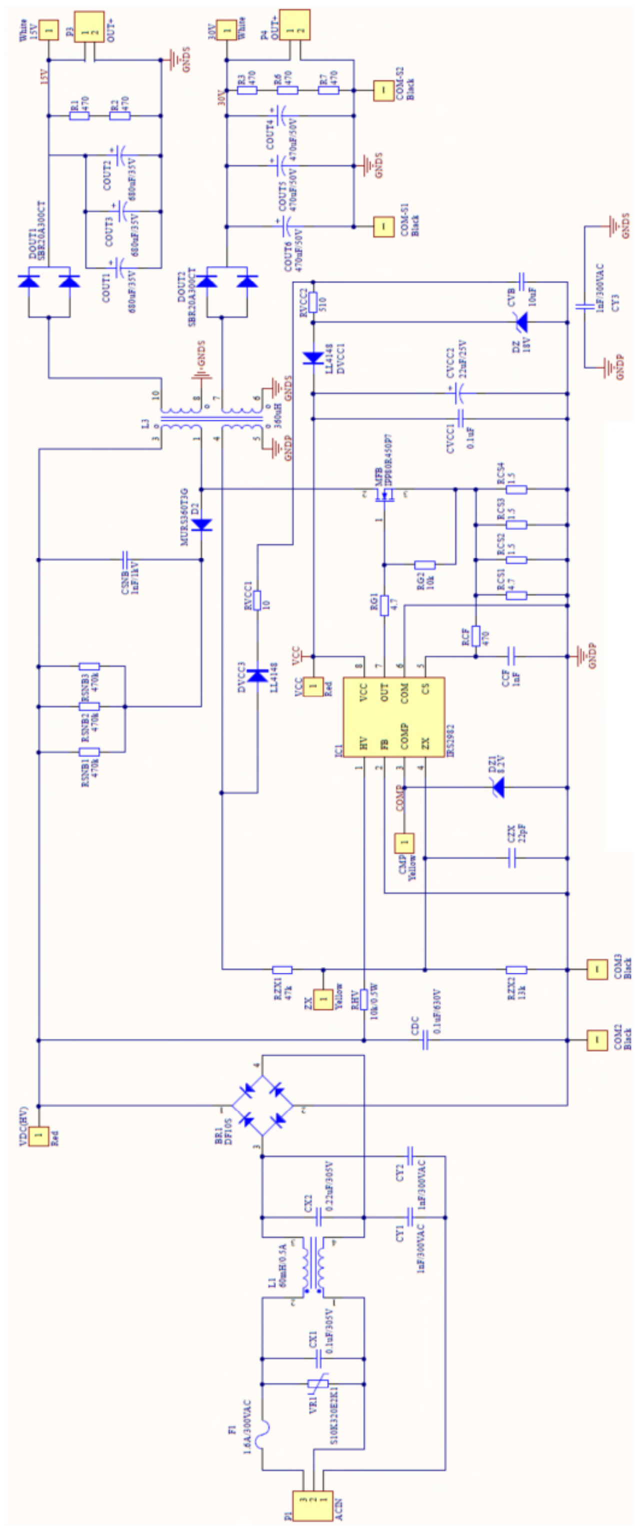


Figure 5.1 IRXPSU1 36 W PFC flyback schematic

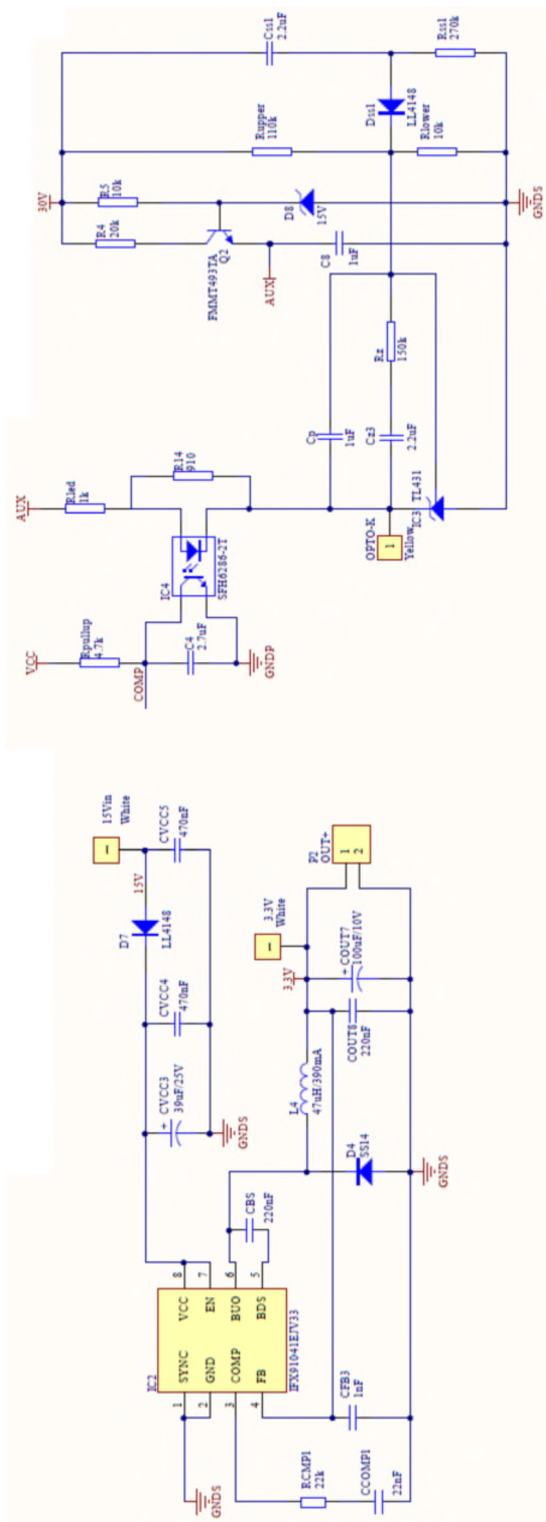


Figure 5.2 IRXPSU1 36 W PFC flyback schematic

5 Dimensioning

The principle of operation for the single-stage PFC flyback converter uses an unsmoothed DC bus voltage with only a small high-frequency capacitor to maintain a full wave-rectified voltage profile. The converter operates in CrCM under normal operating conditions with the on-time remaining effectively constant over the period of the AC-line cycle. This results in an approximately sinusoidal average input current with minimal phase shift and distortion. The output current or voltage is regulated by controlling the on-time using a FB loop that responds to line and load changes.

One of the principal advantages of operating a power supply in CrCM is that the power stage appears as a first order system which is easier to stabilize. Please see reference [5], which goes into detail about the modeling of the flyback power stage and compensating it using type-II error amplifier compensation. The second advantage of using CrCM is that there is no reverse recovery (t_{rr}) loss in the output diode, since the primary switch is turned on when the output diode current reaches zero. Therefore, selection of the output diode is quite easy and it need not have super-fast recovery time. The third advantage is that if the MOSFET is turned on in the drain voltage valley, the capacitive switching loss due to C_{oss} is reduced significantly. On the other hand, the drawbacks of CrCM are that the operating frequency varies in relation to the input and output conditions. The frequency increases during light-load conditions, which can increase switching losses. In order to limit switching frequency, the IRS2982 incorporates a minimum off-time of 3 µs, which limits the maximum switching frequency thereby limiting the switching losses. At full load, the frequency is at minimum. During this period, conduction losses are prominent over switching losses. CrCM operation involves high peak and RMS currents compared to CCM operation. During low-line and full-load condition, the switching frequency can decrease and enter an audible range, causing acoustic noise issues if the primary inductance is too high.

The advantages such as ease of design, simple compensation and low switching losses increase the overall efficiency of the converter. The advantages of CrCM operation outweigh the disadvantages.

The evaluation board is designed to provide multiple output voltages, as shown in Figure 4.
The flyback converter is designed for PFC with low AC-line input current Total Harmonic Distortion (iTHD). The MOSFET used is an IPP80R450P7 800 V rated CoolMOS™ device with 450 mΩ on-resistance, 24 nC gate charge and low parasitic capacitances in a TO-220. This device is able to withstand HV ringing at switch-off with minimal added snubber components and has low conduction and switching losses as well low gate drive current. The CoolMOS™ P7 series is the latest CoolMOS™ product family, which offers high performance though optimizing key parameters (C_{oss}, E_{oss}, Q_g, C_{iss} and $V_{GS(th)}$, etc.); integrating a zener diode for ESD protection and other measures, this product family fully addresses design needs, ease-of-use, and price/performance ratio, delivering best-in-class performance. The 700 V and 800 V CoolMOS™ P7 series have been designed for flyback converters and could also be used in PFC topologies. They are not recommended for soft-switching topologies where hard commutation could happen due to its body diode ruggedness. However, the 600 V CoolMOS™ P7 could be used in both soft- and hard-switching topologies including PFC, flyback, LLC and TTF. The output diode used on this board has less than 50 ns reverse recovery and a forward voltage drop less than 900 mV at maximum rated current of 10 A at 25°C temperature, reducing to 700 mV at 150 °C. The blocking voltage is 300 V, necessary to withstand the output voltage under open-circuit condition at high-line input added to the transformer secondary reflected voltage.
The parameters of the MOSFET and output diode contribute to the overall high efficiency of the converter.
The flyback transformer (more accurately described as a coupled inductor) consists of four windings; the primary for energy storage during the on-time, the secondary for energy transfer to the output during the off-time and the auxiliary, which supplies V_{CC} and provides the required de-magnetization and voltage FB signals.
The IRS2982S (IC1) V_{CC} supply is derived from the transformer auxiliary winding through DVCC3 initially charging CVB then CVCC1 and two through RVCC2 and DVCC1 with DZ to clamp the voltage to protect IC1.
Voltage FB is provided through a divider comprised of RFB1 and RFB2, which sets the output voltage.

Switching-cycle peak current limiting is set by parallel shunt resistors RCS1 to 4, which give a combined resistance of 450 mΩ, setting the peak current to 2.67 A according to the threshold VCSTH of 1.2 V. This limits the in-rush current during start-up and also protects against damage under over-load or short-circuit conditions. The evaluation board is not designed to withstand a sustained output over-load or short-circuit. The maximum peak current at low-line and full load, assuming DMAX is 0.5, is calculated as:

$$I_{PMAX} = \frac{\sqrt{2} \cdot V_{acmin} \cdot D_{max}}{L_{PRI} \cdot F_{SW}} = \frac{\sqrt{2} \cdot 90 \cdot 0.5}{346 \cdot 10^{-6} \cdot 65000} = 2.829$$ [A] [2]

The transformer turns-ratio is calculated as follows:

$$N\_15V = \frac{N_P}{N_{S\_15V}} = \frac{\sqrt{2} \cdot VAC_{MIN}}{V_{O15} + V_F} \cdot \frac{D_{MAX}}{1 - D_{MAX}} = \frac{\sqrt{2} \cdot 90}{15+1} \cdot \frac{0.5}{1-0.5} = 7.954$$ [3a]

$$N\_30V = \frac{N_P}{N_{S\_30V}} = \frac{\sqrt{2} \cdot VAC_{MIN}}{V_{O30} + V_F} \cdot \frac{D_{MAX}}{1 - D_{MAX}} = \frac{\sqrt{2} \cdot 90}{30+1} \cdot \frac{0.5}{1-0.5} = 4.105$$ [3b]

The primary to auxiliary winding turns-ratio is calculated to provide an auxiliary supply voltage of 20 V:

$$N_{AUX} = \frac{N_P}{N_A} = \frac{\sqrt{2} \cdot VAC_{MIN}}{V_{AUX} + V_{F(AUX)}} \cdot \frac{D_{MAX}}{1 - D_{MAX}} = \frac{\sqrt{2} \cdot 90}{20+1} \cdot \frac{0.5}{1-0.5} = 6.061$$ [4]

The transformer primary inductance is calculated according to the formula:

$$L_{PRI} = \frac{VAC_{MIN}^2 \cdot \eta \cdot D_{MAX}^2}{\sqrt{2} \cdot P_{OUT} \cdot f_{MIN}}$$ [H] [5]

$$\frac{90^2 \cdot 0.8 \cdot 0.5^2}{2 \cdot 36 \cdot 65000} = 346 \cdot 10^{-6} \text{ H} = 346$$ [µH]

Where η is the efficiency, assumed to be 0.9, and minimum frequency is set to 65 kHz to occur at the peak of the line input voltage at 90 Vrms.

The multi-output flyback has some known limitations such as poor cross-regulation and a minimum load requirement to limit the output voltage. On this board, good cross-regulation is achieved with a minimum load requirement on the main 30 V winding. As long as there is a minimum load at the 30 V output (at least 10 mA), the voltages on the 15 V and 3.3 V outputs remain well regulated. Please refer to Tables 1 and 2 to check the regulation on all the three windings. The cross-regulation issue can be minimized by good transformer design parctices.

In order to maintain a minimum load on the 15 V and 30 V outputs, two 470 Ω resistors in series are placed across the output of 15 V winding and three 470 Ω series resistors are placed across the 30 V winding. In doing so, the efficiency and standby power are reduced. In this evaluation board, the 30 V winding is the main winding and 15 V is quasi-regulated. 3.3 V is being supplied from the 15 V winding through the IFX91041 buck regulator.

For the multi-output transformer on this board, bifilar windings are used for the 15 V in order to achieve a good coupling with the regulating 30 V winding. The transformer winding stack-up is as follows: the first layer contains half the primary turns, the second layer is 15 V wound bifilar, the third layer is 30 V, the fourth layer is the auxiliary winding, and the fifth layer contains the remaining half of the primary turns.

In specific applications where the ICs always needs to stay active when there is no load on the main winding (30 V winding), the 15 V output needs to be regulated and the transformer winding stack-up would change, swapping the 15 V and 30 V windings as shown below:

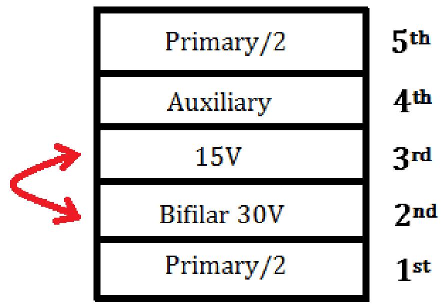


Figure 6 Transformer stack-up

IFX91041 buck controller IC is used on this board to step down the 15 V to 3.3 V. This converter operates with a fixed 370 kHz switching frequency. By applying a rectangular signal to the “Sync” pin the switching frequency may be adjusted to an external source between 200 and 500 kHz. Microcontrollers typically use a steady 3.3 V DC power supply. This is one of the main reasons for including the IFX91041 buck controller IC on this board, to step down the 15 V to a steady 3.3 V output with a very low output ripple.

The IFX91041 comes in three versions:
- A fixed 5 V output voltage version, named IFX91041EJV50
- A fixed 3.3 V output voltage version, named IFX91041EJV33
- A variable output voltage version, named IFX91041EJV

The output voltages are adjustable from 0.60 V up to 16 V. The values of the output voltages depend on the value of the input voltage – the input needs to be at least 0.70 V above the desired output voltage at full load to maintain the specified value at 100 % duty cycle and output load.The IFX91041 has an internal power stage, but requires an output filter consisting of the freewheeling (or catch) diode, the filter inductor and the filter capacitor.

The correct dimensioning of the output filter components is essential for proper functioning of the converter under each load and input voltage condition. The freewheeling diode needs to be a fast-switching diode capable of conducting the full load current, especially for starting under high input voltages. The use of a Schottky diode is recommended. The dimensioning of the filter inductor and its saturation inductance have to be considered. The inductor must not be driven in saturation under any start-up or load condition, especially at high input voltages. The filter capacitor shall be capable of handling the current ripple resulting from the choice of the filter inductor. The use of two filter capacitors in parallel is recommended. In this demo board IFX91041 is used to step down 15 V to 3.3 V. Please see reference [2] for more information on IFX91041.

6 Bill of Materials (BOM)

Quantity	Designator	Manufacturer	Part number	Value/rating
4	3.3 V, 15 V, 15 V_{in}, 30 V	Keystone	5002	0.04" diameter white
1	BR1	Diodes Inc.	DF10S	1000 V/1 A/SMD4P
1	C1	Murata	GRM31MR71E225KA93L	2.2 µF/25 V/ 10%/1206/X7R
4	C2, C3, C8, Cp	Yageo, TDK	C3216X7R1E105K085AA	1 µF/25 V/10%/1206/X7R
1	C4	KEMET	C1206C275K3PACTU	2.7 µF/25 V/ 5%/1206/NP0
2	CBS, COUT8	Yageo	CC1206KRX7R8BB224	220 nF/25 V/1206/10%
1	CCF	TDK	C2012X7R2E102K085AA	1 nF/250 V/0805/10%
1	CCOMP1	Samsung Electro-Mechanics America, Inc.	CL31B223KBCNNNC	22 nF/50 V/1206/10%
1	CDC	Epcos	B32922C3104M	0.1 µF/305 V AC/X2
1	CFB3	Samsung Electro-Mechanics America, Inc.	CL31C102JBCNNNC	1 nF/50 V/1206/10%
3	CMP, OPTO-K, ZX	Keystone	5004	0.04" diameter yellow
4	COM2, COM3, COM-S1, COM-S2	Keystone	5001	0.04" diameter black
3	COUT1, COUT2, COUT3	Rubycon	35ZLH680MEFC10X23	470 µF/35 V/20%
3	COUT4, COUT5, COUT6	Panasonic	EEU-FM1H471	470 µF/50 V/20%
1	COUT7	Würth Elektronik	865080243007	100 µF/10 V
1	CSNB	TDK	C4532X7R3A102M200KA	1 nF/1 kV/20%/1812/X7R
1	CVB	TDK	C3216X5R1H106K160AB	10 µF/50 V/1206/10%
1	CVCC1	TDK	C3216C0G1H104J160AA	0.1 µF/50 V/1206/5%
1	CVCC2	Panasonic	EEU-EB1H220S	22 µF/25 V
1	CVCC3	Panasonic	EEU-FC1E390	39 µF/25 V
2	CVCC4, CVCC5	Samsung Electro-Mechanics America, Inc.	CL31B474KAFNNNE	0.47 µF/25 V/10%/1206
1	CX1	Epcos	B32922C3104M	0.1 µF/305 V AC/X2
1	CX2	Epcos	B32922C3224M	0.22 µF/305 V AC/X2
3	CY1, CY2, CY3	Vishay	VY2102M29Y5US63V7, VY2102M29Y5UG63V7, VY2102M29Y5US63V7	1 nF/300 V AC/Y
3	Cz1, Cz2, Cz3	Yageo	CC1206ZRY5V8BB225	2.2 µF/25 V/5%/1206/NP0
1	CZX	KEMET	C0805C220J5GACTU	22 pF/50 V/0805/5%

4	D1, D7, DVCC1, DVCC3	Diodes Inc.	LL4148-13	75 V/0.15 A/MINIMELF
1	D2	ON Semi	MURS360T3G	600 V/3 A fast-recovery diode
1	D4	Vishay	SS14	40 V/1 A/0.5 Vf
1	D8	Nexperia USA Inc.	BZV55-C15,115	15 V
2	DOUT1, DOUT2	Diodes Inc.	SBR20A300CTFP	300 V/10 A/ITO-220AB
1	DZ	Micro Commercial Co.	BZV55C18-TP	18 V/0.5 W/MINIMELF
1	F1	Bussman	SS-5H-1.6A-APH	T1.6 A/300 V AC/4 to 8.5
1	IC1	Infineon	IRS2982S	SMPS controller
1	IC2	Infineon	IFX91041	Buck controller
1	IC3	Diodes Inc.	ZTL431	IC, voltage reference, SOT-23-3
1	IC4	Vishay	SFH6286-2T	5.3 kV
1	L1	KEMET	SS24H-R05600-CH	2 × 60 mH common mode
1	L3	Würth Elektronik	750317054	360 µH
1	L4	Würth Elektronik	74404042470	47 µH/390 mA
1	MFB	Infineon	IPA80R450P7	800 V/4.5 A/TO-220
1	P1	Phoenix Contact	1985205	Three-position 3.5 mm green
3	P2, P3, P4	Phoenix Contact	1985195	Two-position 3.5 mm green
1	Q2	ON Semi	FMMT493TA	100 V/1 A/NPN/SOT-23
5	R1, R2, R3, R6, R7	Yageo	FMP200JR-52-470R	470 Ω/2 W/5% AXIAL
1	R4	Yageo	RC1206JR-0720KL	20 k/0.25 W/5%/1206
2	R5, Rlower	Yageo, Panasonic	RC1206JR-0710KL, ERJ-8RQF103V	10 k/0.25 W/5 %/1206, 10 k/0.25 W/1206/1%
1	R14	Yageo	RC1206FR-07910RL	910 Ω/0.25 W/5%/1206
1	RCF	Panasonic	ERJ-6GEYJ471V	470/0.125 W/0805/5%
1	RCMP1	Stackpole Electronics Inc.	RMCF0805JT22K0	22 k/0.125 W/0805/5%
2	RCS1, RG1	Panasonic	ERJ-8GEYJ4R7V	4.7/0.25 W/1206/5%
3	RCS2, RCS3, RCS4	Panasonic	ERJ-8GEYJ1R5V	1.5/0.25 W/1206/5%
1	RG2	Panasonic	ERJ-8GEYJ103V	10 k/0.25 W/1206/5%
1	RHV	Yageo	CFR-50JB-52-10K	10 k/0.5 W/5%
1	Rled	Yageo	RC1206JR-072K2L	2.2 k/0.25 W/5%/1206
1	Rpullup	Yageo	RC1206JR-075K6L	5.6 k/0.25 W/5%/1206
3	RSNB1, RSNB2, RSNB3	Panasonic	ERJ-8GEYJ474V	470 k/0.25 W/1206/5%
1	Rupper	Panasonic	ERJ-8ENF1103V	110 k/0.125 W/1206/1%
1	RVCC1	Panasonic	ERJ-8GEYJ100V	10/0.25 W/1206/5%
1	RVCC2	Panasonic	ERJ-8GEYJ511V	510/0.25 W/1206/5%
1	Rz	Yageo	RC1206JR-07150KL	150 k/0.25 W/1206/1%
1	RZX1	Panasonic	ERJ-8GEYJ473V	47 k/0.25 W/1206/5%
1	RZX2	Panasonic	ERJ-6ENF1402V	14 k/0.125 W/0805/5%

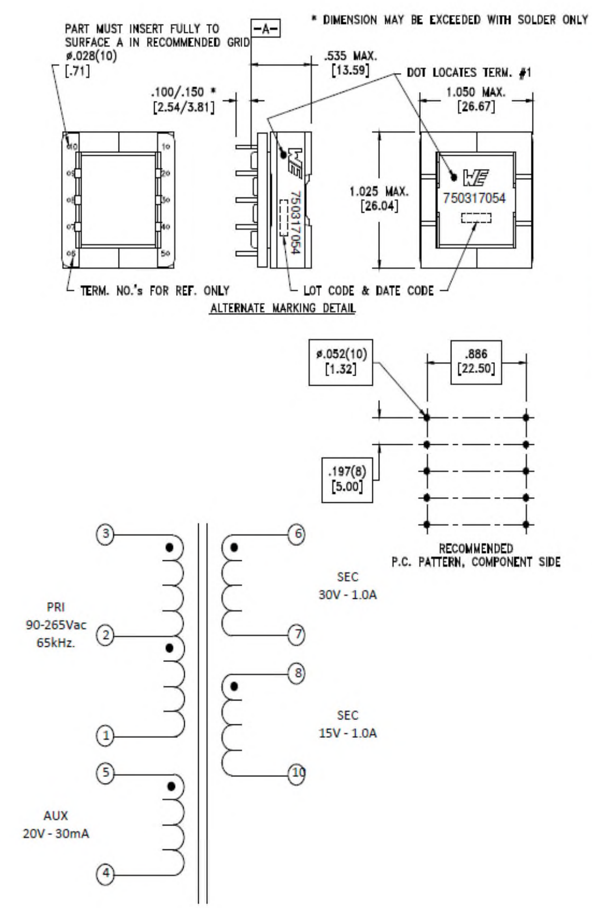
2	VCC, VDC(HV)	Keystone	5000	0.04" diameter red
1	VR1	Epcos	S10K320E2K1	510 V/3.5 kA/10 mm

7 Transformer specification

Würth 750317054 rev01

Primary inductance and leakage inductance:

Lp = 363 µH (±10 %), measured between pin 1 and pin 3, leakage inductance less than or equal to 4.5 µH



WÜRTH ELEKTRONIK

ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	3-2	@20°C	0.205 ohms ±10%
D.C. RESISTANCE	6-7	@20°C	0.120 ohms ±10%
D.C. RESISTANCE	5-4	@20°C	0.080 ohms ±10%
D.C. RESISTANCE	8-10	@20°C	0.030 ohms ±20%
D.C. RESISTANCE	2-1	@20°C	0.249 ohms ±10%
INDUCTANCE	3-1	10kHz, 100mV, Ls	363µH ±10%
SATURATION CURRENT	3-1	20% rolloff from initial	3.5A
LEAKAGE INDUCTANCE	3-1	tie(4+5, 6+7 8+10),100kHz, 100mV, Ls	3.2µH typ., 4.5µH max.
DIELECTRIC	1-10	tie(1+5, 6+10), 1500VAC, 1 second	
TURNS RATIO		(3-1):(6-7)	3.81:1, ±1%
TURNS RATIO		(3-1):(5-4)	6.1:1, ±1%
TURNS RATIO		(3-1):(8-10)	7.63:1, ±1%
TURNS RATIO		(3-2):(2-1)	0.97:1, ±1%

GENERAL SPECIFICATIONS:

OPERATING TEMPERATURE RANGE: -40°C to +125°C including temp rise.

Safety standard undefined

- Functional insulation only

Wire insulation & RoHS status not affected by wire color. Wire insulation color may vary depending on availability.

DFM		Packaging Specifications	CONVENTION PLACEMENT	Tolerances unless otherwise specified:	DRAWING TITLE	PART NO.
DATE		Method: Tray		Angles: ±1° Decimals: ±.005 [.13]	TRANSFORMER	750317054
ENG	JJB	PKG-0819		Fractions: ±1/64 Footprint: ± .001 [.03]		
REV.	01			This drawing is dual dimensioned. Dimensions in brackets are in millimeters.		
DATE	8/7/2017	www.we-online.com/midcom				SPECIFICATION SHEET 1 OF 1

Figure 7 Flyback transformer specification

8 PCB layout

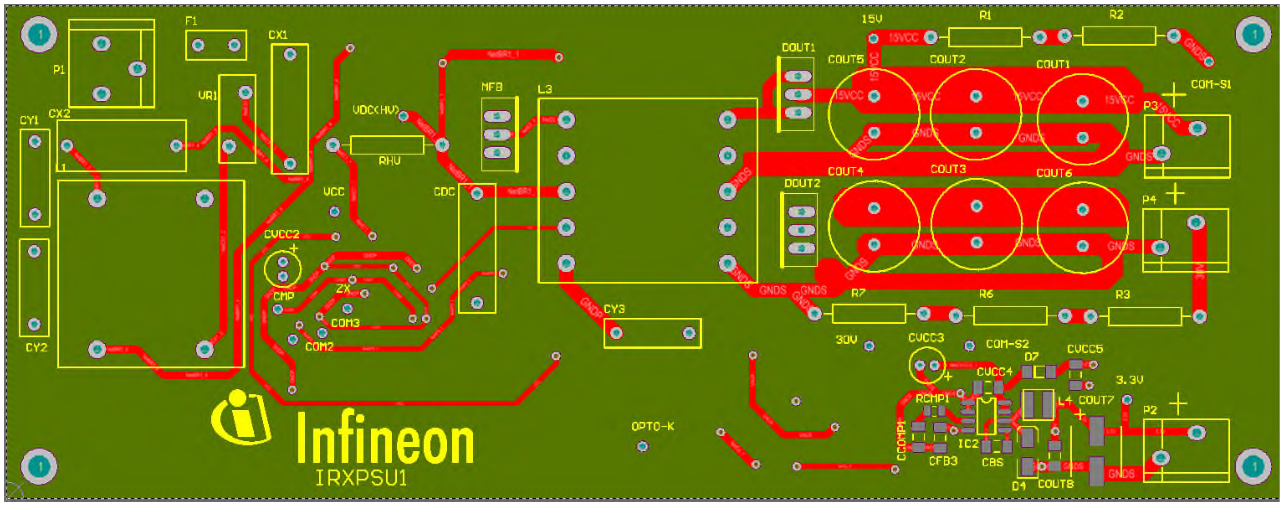


Figure 8.1 PCB top-side components and traces

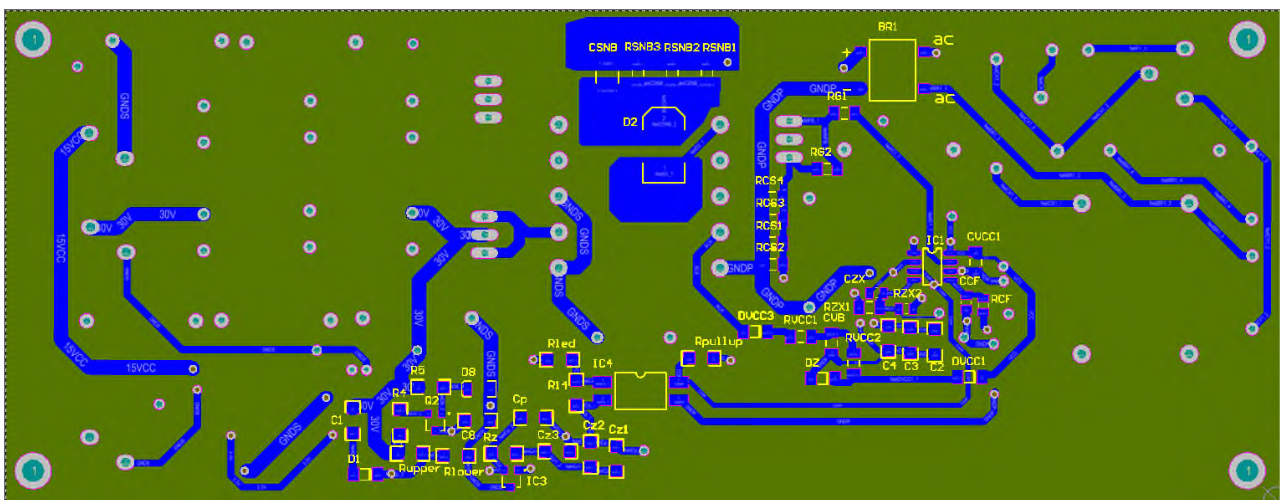


Figure 8.2 PCB bottom-side components and traces

9 Test results

9.1 Test measurements under different line and load conditions

Table 1 Input 115 V AC

Load	P_{out} (W)	P_{in} (W)	$V_{o\_3.3V}$	$I_{o\_3.3V}$	V_{o_15V}	I_{o_15V}	V_{o_30V}	I_{o_30V}	η	PF	THD
100 %	35.99	41.79	3.296	0.15	14.49	0.8	29.89	0.8	86.14	0.998	4.87
75 %	27.02	31.5	3.298	0.1125	14.52	0.6	29.9	0.6	85.79	0.996	7.22
50 %	18.02	21.52	3.298	0.075	14.54	0.4	29.9	0.4	83.75	0.993	8.33
25 %	9.01	11.869	3.298	0.0375	14.56	0.2	29.9	0.2	75.96	0.981	10.54

Table 1.1 Input 115 V AC (load only on 30 V winding, no load on 15 V, and 3.3 V windings)

Load only on 30 V main winding	V_{o_30V}	V_{o_15V} (no load)	$V_{o\_3.3}$ (no load)
100 % (0.8 A)	29.88	17.08	3.293
0.4 A	29.89	15.71	3.294
0.1 A	29.89	14.92	3.294
0.01 A	29.90	14.75	3.294

Table 1.1 shows the variation on all three windings when 15 V and 3.3 V are completely unloaded. Only the 30 V main winding has a load varying between 10 mA and 800 mA.

Table 1.2 Input 115 V AC (0.8 A load on 30 V winding, load on 15 V varying from 0 A to 0.8 A, no load on 3.3 V winding)

Load	V_{o_30V} (load = 0.8 A)	V_{o_15V} (varying load from 0 A to 0.8 A)	$V_{o\_3.3}$ (no load)
100 % (0.8 A)	29.85	14.68	3.293
0.4 A	29.86	14.92	3.294
0.2 A	29.87	15.17	3.294
0.1A	29.87	15.44	3.294
0.01A	29.87	16.57	3.294
0A (no load)	29.87	17.08	3.294

Table 2 Input 230 V AC

Load	P_{out} (W)	P_{in} (W)	$V_{o\_3.3V}$	$I_{o\_3.3V}$	V_{o_15V}	I_{o_15V}	V_{o_30V}	I_{o_30V}	η	PF	THD
100 %	36.03	41.36	3.298	0.15	14.52	0.8	29.9	0.8	87.11	0.976	14.89
75 %	27.02	31.7	3.298	0.1125	14.53	0.6	29.89	0.6	85.25	0.961	15
50 %	18.01	22.2	3.298	0.075	14.53	0.4	29.89	0.4	81.15	0.94	12.75
25 %	9.01	12.939	3.298	0.0375	14.54	0.2	29.89	0.2	69.63	0.862	13.98

Table 2.1 Input 230 V AC (load only on 30 V winding, no load on 15 V, and 3.3 V windings)

Load only on 30 V main winding	V_{o_30V}	V_{o_15V} (no load)	$V_{o\_3.3}$ (no load)
100 % (0.8 A)	29.88	16.45	3.293
0.4 A	29.89	15.41	3.294
0.1 A	29.89	15	3.294
0.01 A	29.90	14.81	3.294

Table 2.1 shows the variation on all three windings when 15 V and 3.3 V are completely unloaded. Only the 30 V main winding has a load varying between 10 mA and 800 mA.

Table 2.2 Input 230 V AC (0.8 A load on 30 V winding, load on 15 V varying from 0 A to 0.8 A, no load on 3.3 V winding)

Load	V_{o_30V} (load = 0.8 A)	V_{o_15V} (varying load from 0 A to 0.8 A)	$V_{o\_3.3}$ (no load)
100 % (0.8 A)	29.88	14.67	3.294
0.4 A	29.88	14.86	3.294
0.2 A	29.88	15.06	3.294
0.1 A	29.88	15.27	3.294
0.01 A	29.88	16.07	3.294
0 A (no load)	29.88	16.42	3.294

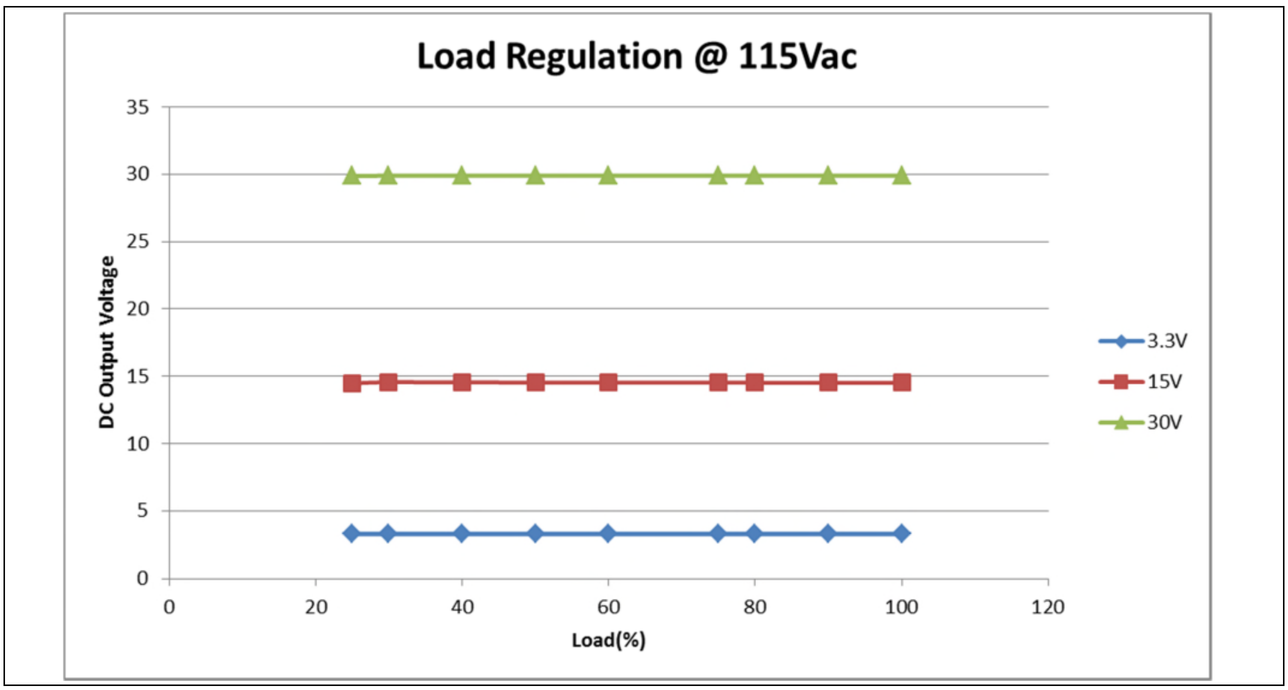


Figure 9 Load regulation at 115 V AC

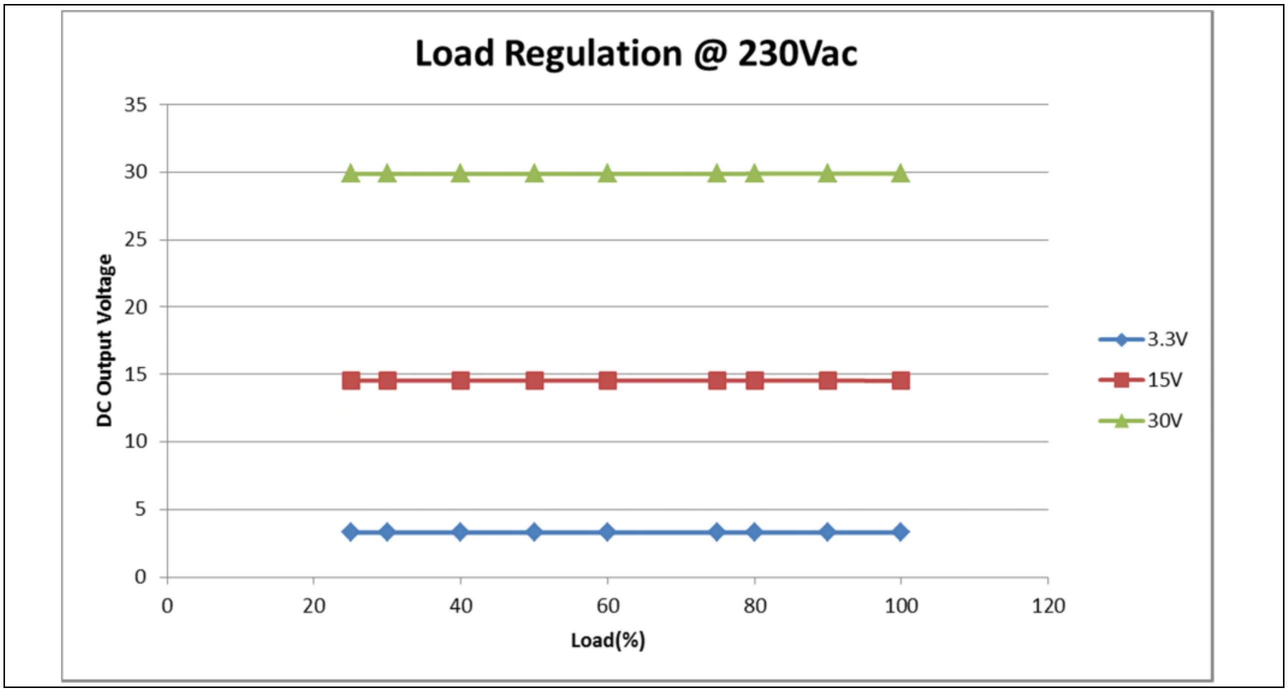


Figure 10 Load regulation at 230 V AC

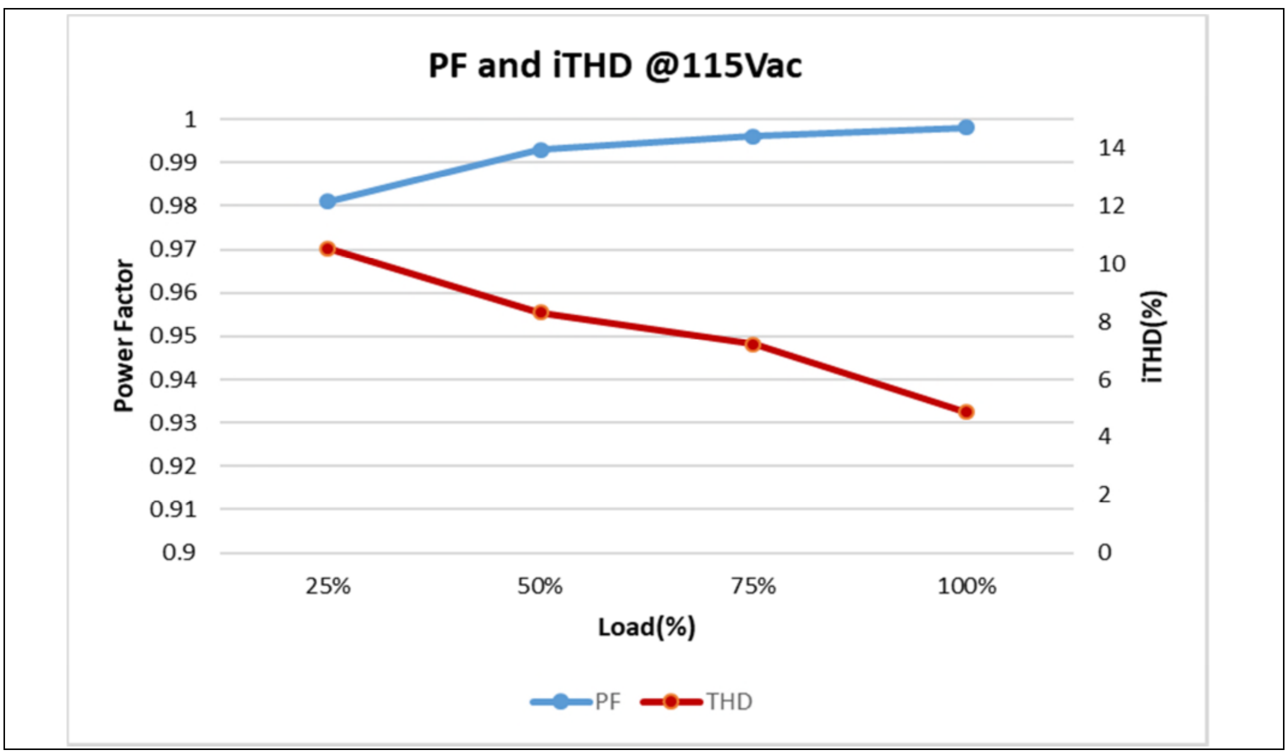


Figure 11 Power factor and iTHD vs load at 115 V AC

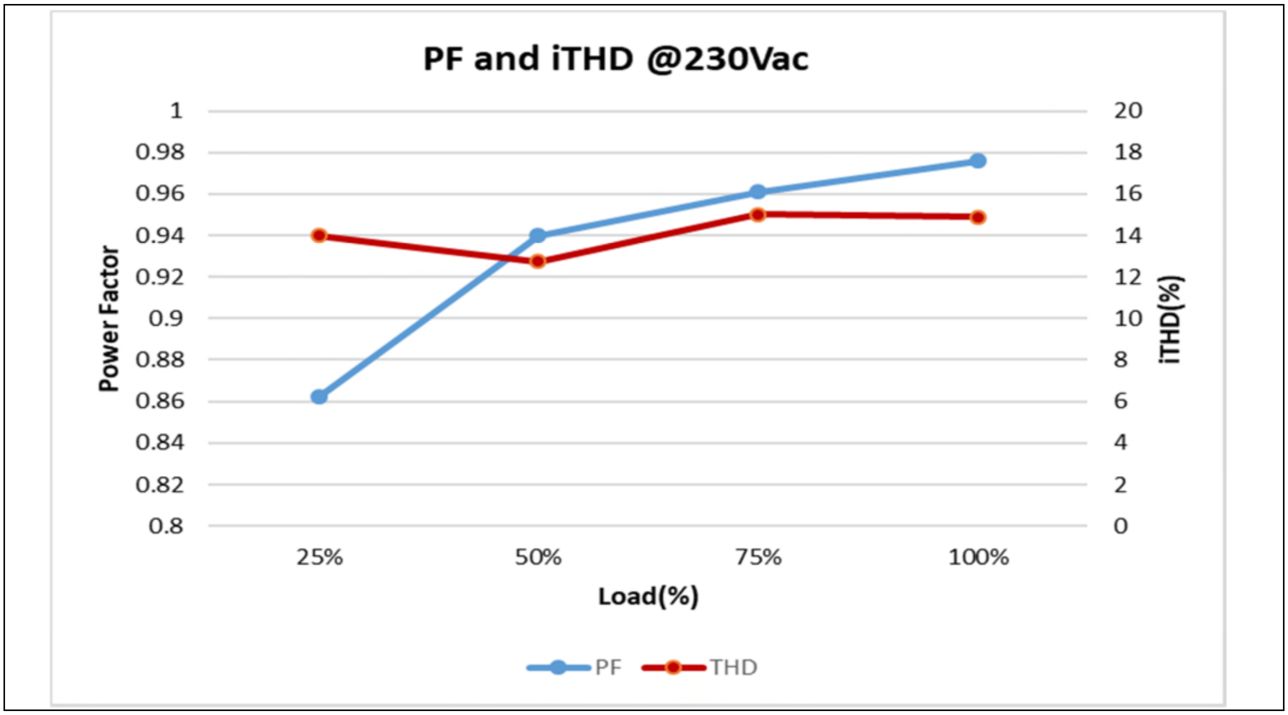


Figure 12 Power factor and iTHD vs load at 230 V AC

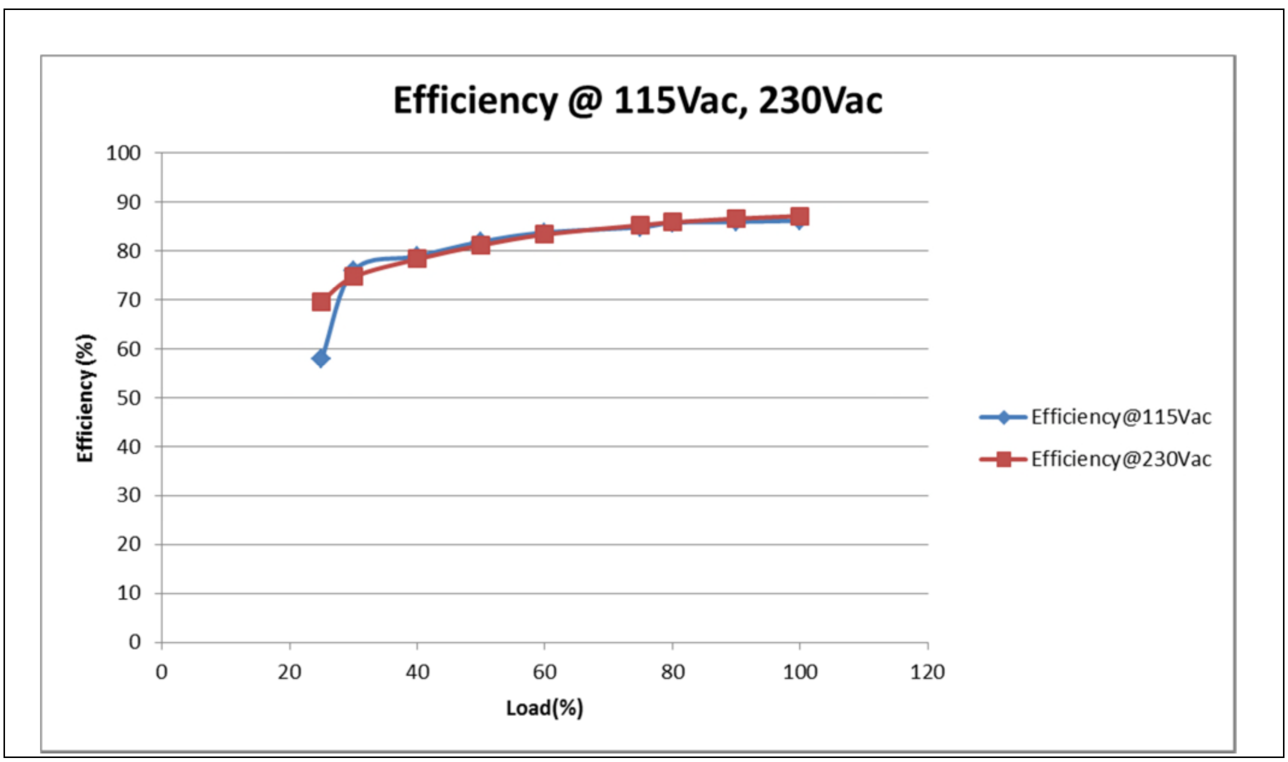


Figure 13 Efficiency vs load

9.2 Start and steady-state operation at maximum load

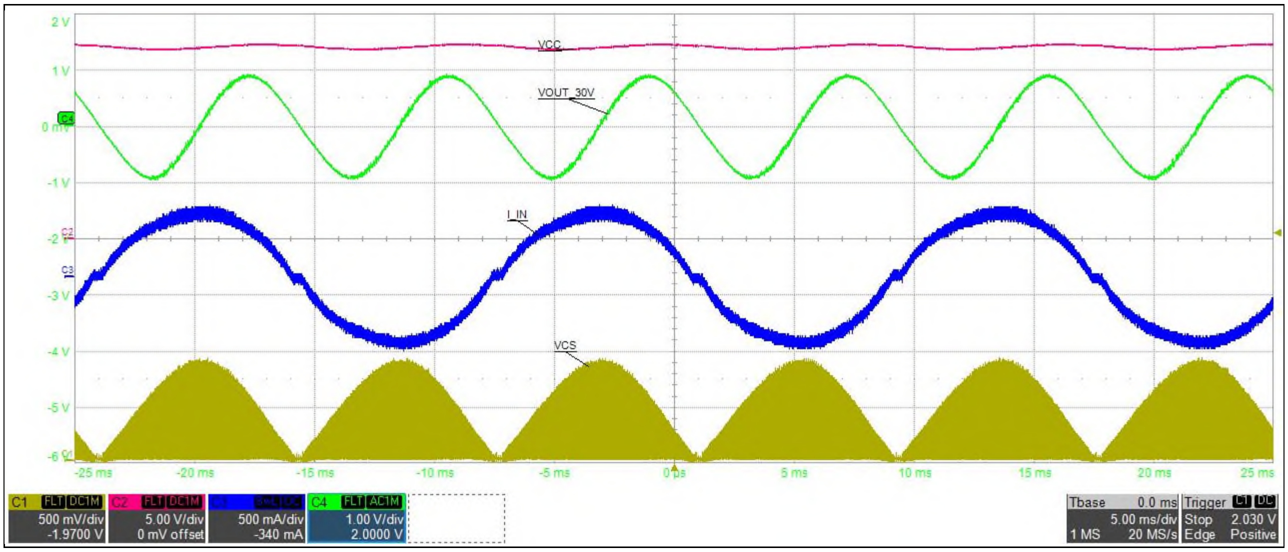


Figure 14 100 V AC steady-state operation at 100 % load
Input current (blue), CS (yellow), V_{CC} (red), V_{OUT} ripple (green)

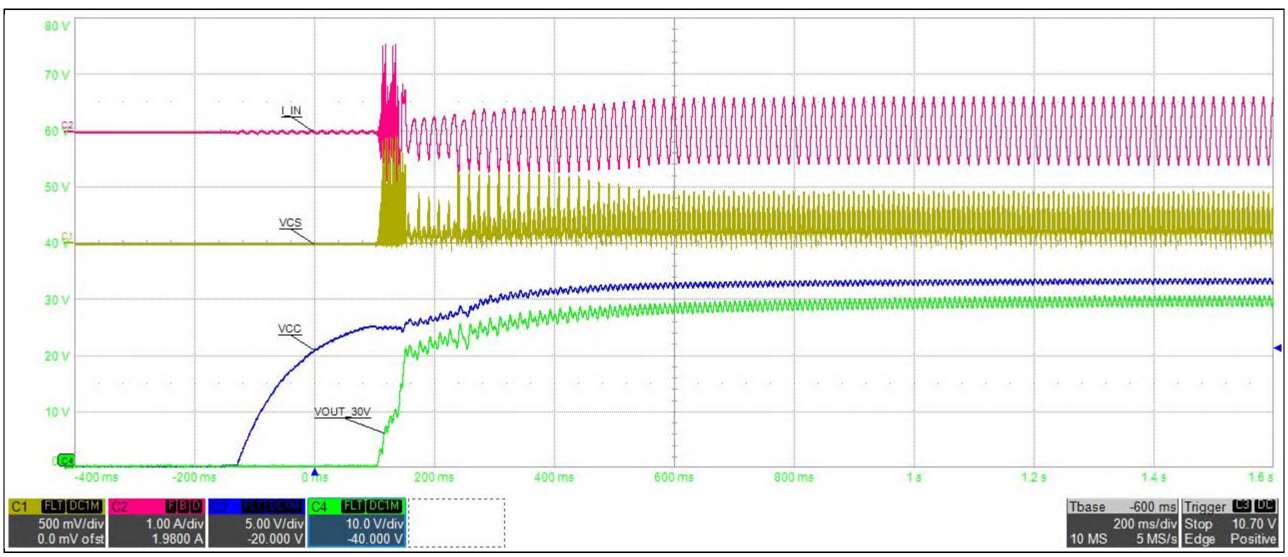


Figure 15 100 V AC start-up at 100 % load
Input current (blue), CS (yellow), V_{CC} (red), V_{OUT} (green)

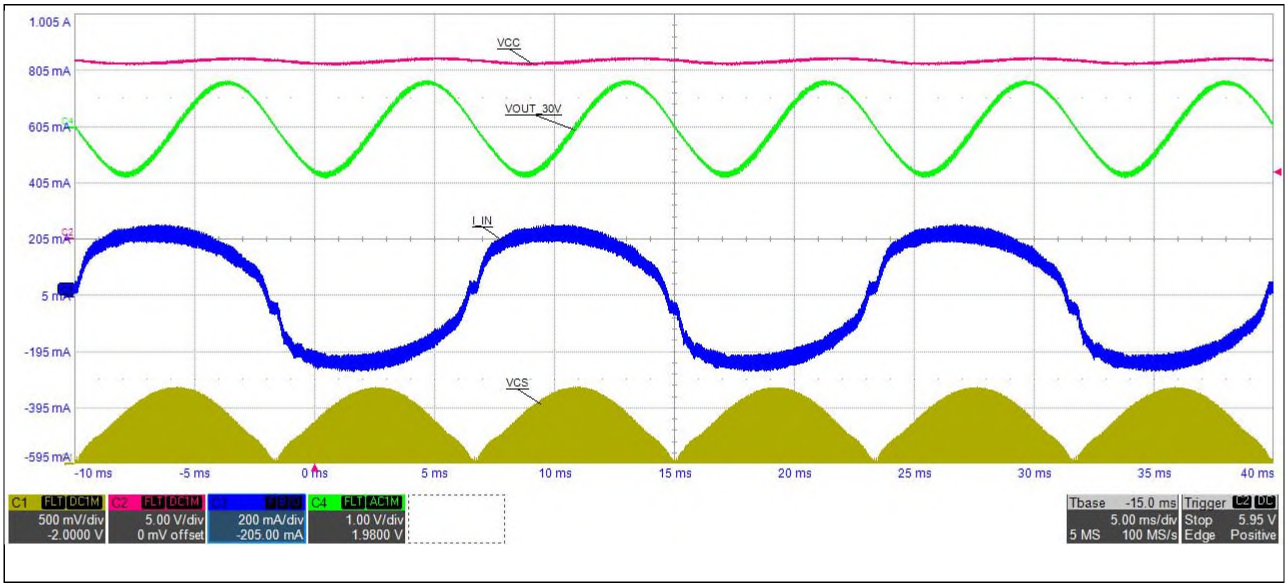


Figure 16 230 V AC steady-state operation at 100 % load
Input current (blue), CS (yellow), V_{CC} (red), V_{OUT} ripple (green)

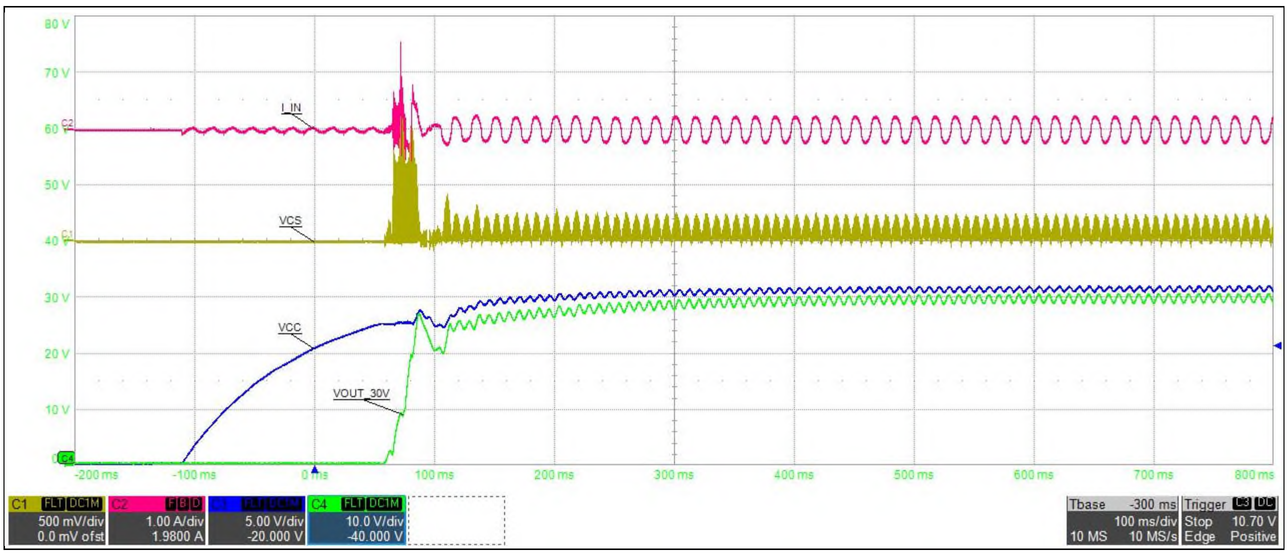


Figure 17 230 V AC start-up at 100 % load
Input current (red), CS (yellow), V_{CC} (blue), V_{OUT} (green)

9.3 Start-up under different line and load conditions

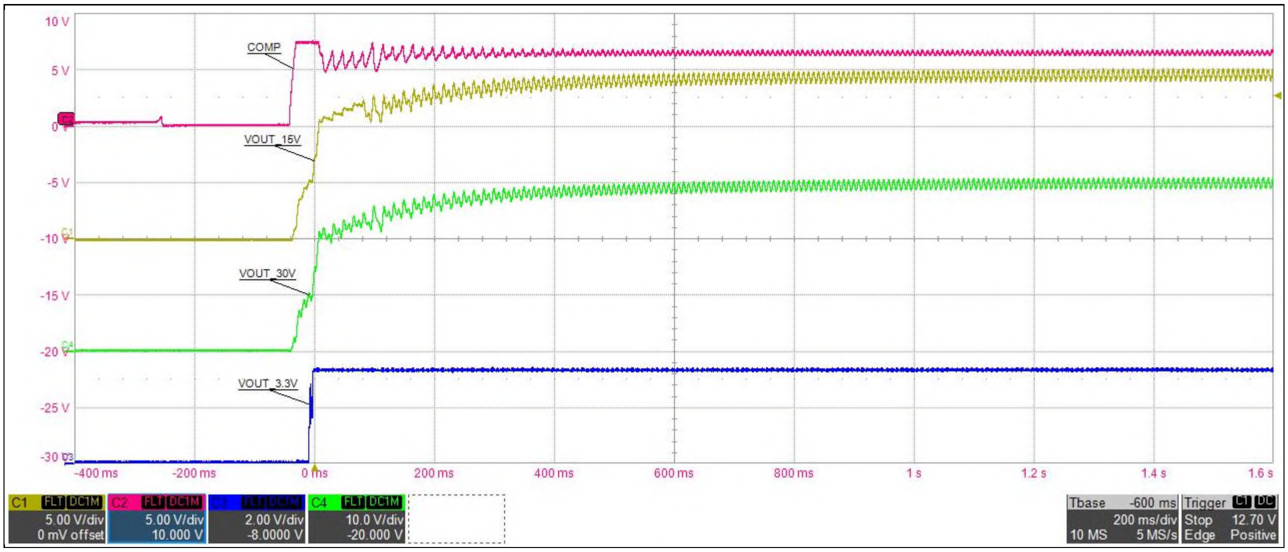


Figure 18 100 V AC start-up at 100 % load
30 V_{out} (green), V_{COMP} (red), 15 V_{out} (yellow), 3.3 V_{out} (blue)

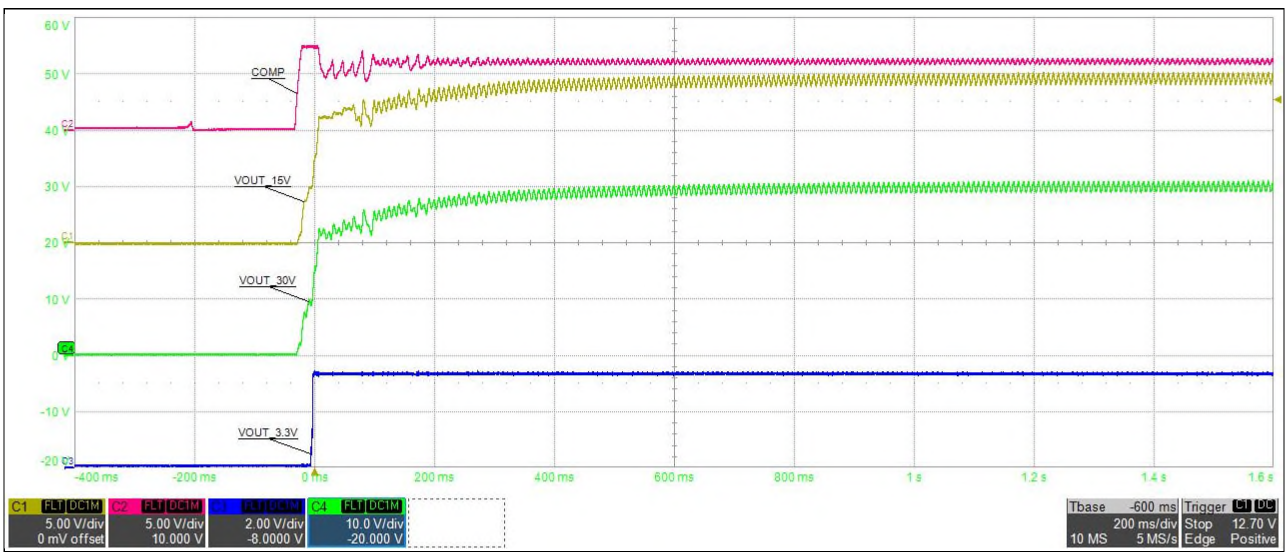


Figure 19 120 V AC start-up at 100 % load
30 V_{out} (green), V_{COMP} (red), 15 V_{out} (yellow), 3.3 V_{out} (blue)

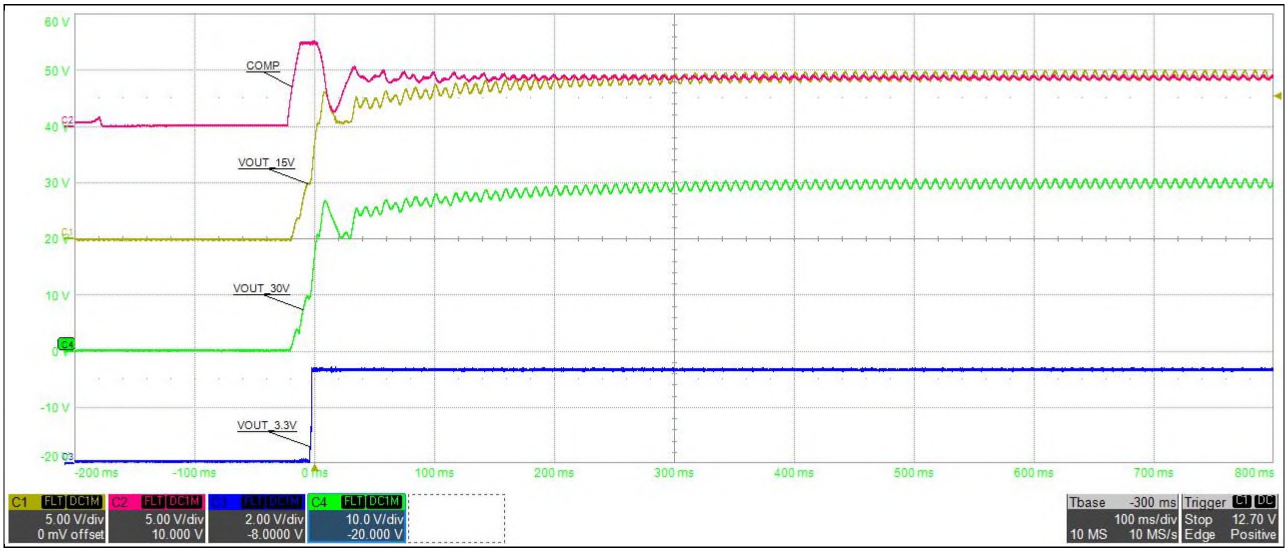


Figure 20 230 V AC start-up at 100 % load
30 V_{out} (green), V_{COMP} (red), 15 V_{out} (yellow), 3.3 V_{out} (blue)

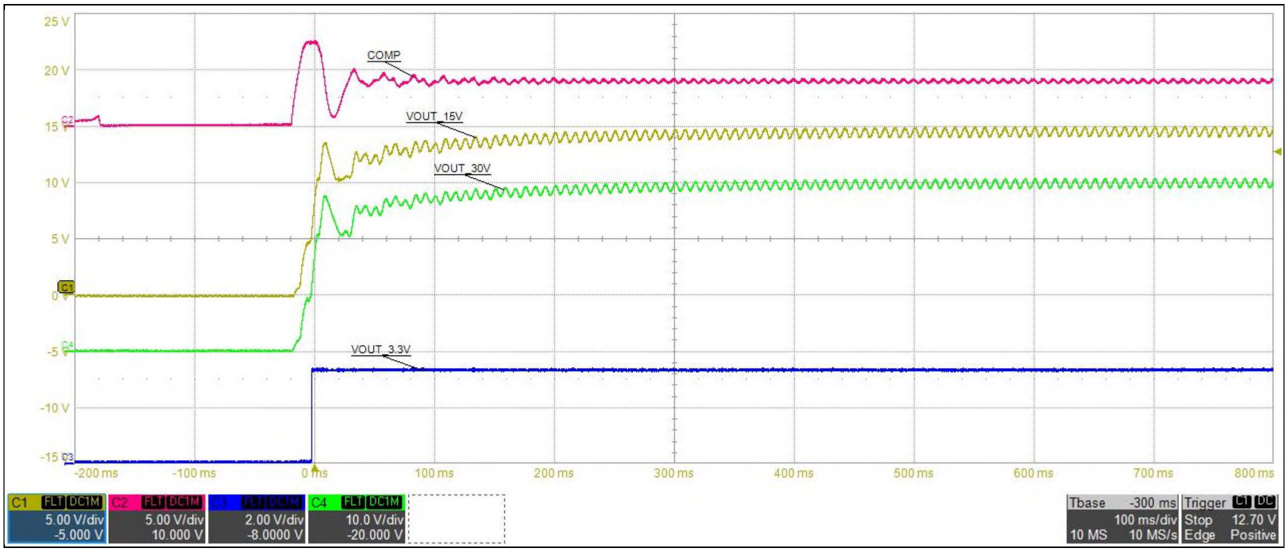


Figure 21 265 V AC start-up at 100 % load
30 V_{out} (green), V_{COMP} (red), 15 V_{out} (yellow), 3.3 V_{out} (blue)

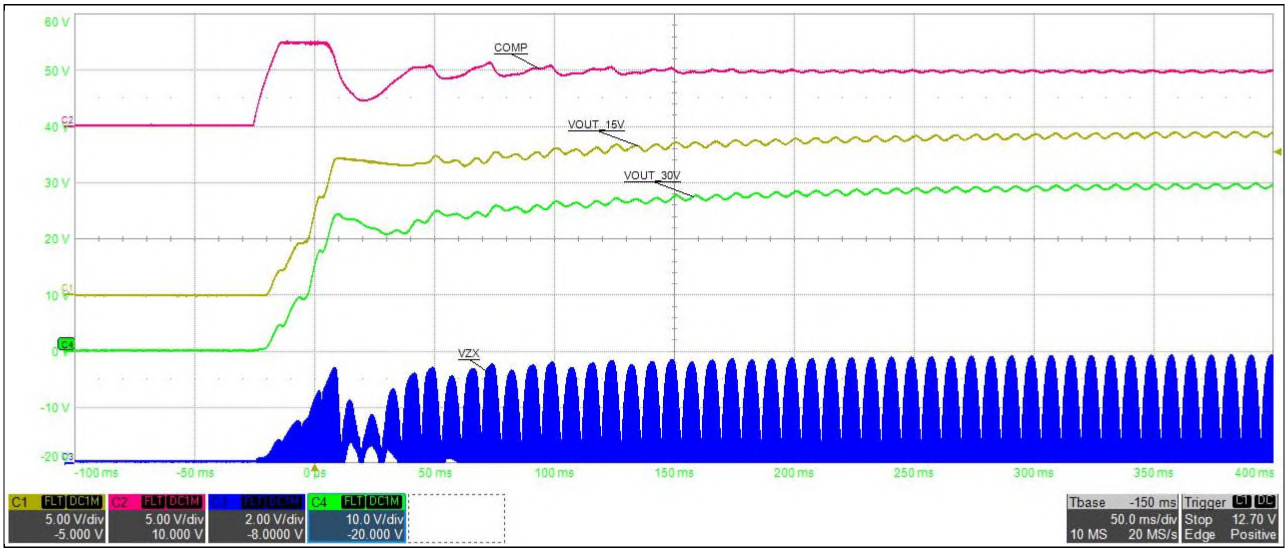


Figure 22 120 V AC start-up at 50 % load
30 V_{out} (green), V_{COMP} (red), 15 V_{out} (yellow), V_{ZX} (blue)

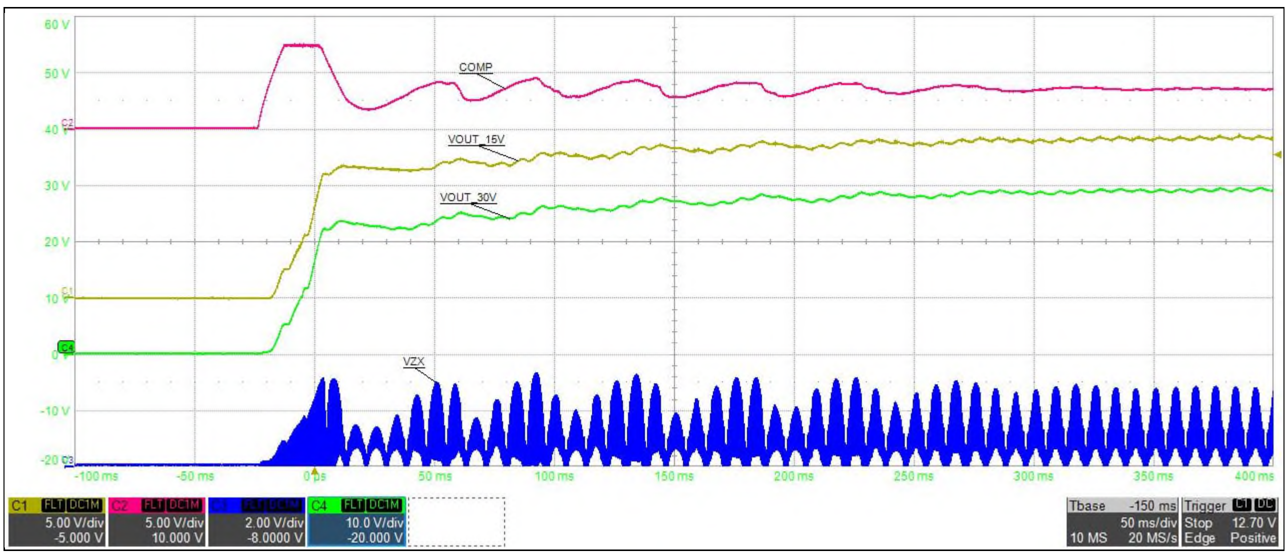


Figure 23 120 V AC start-up at 20 % load
30 V_{out} (green), V_{COMP} (red), 15 V_{out} (yellow), V_{ZX} (blue)

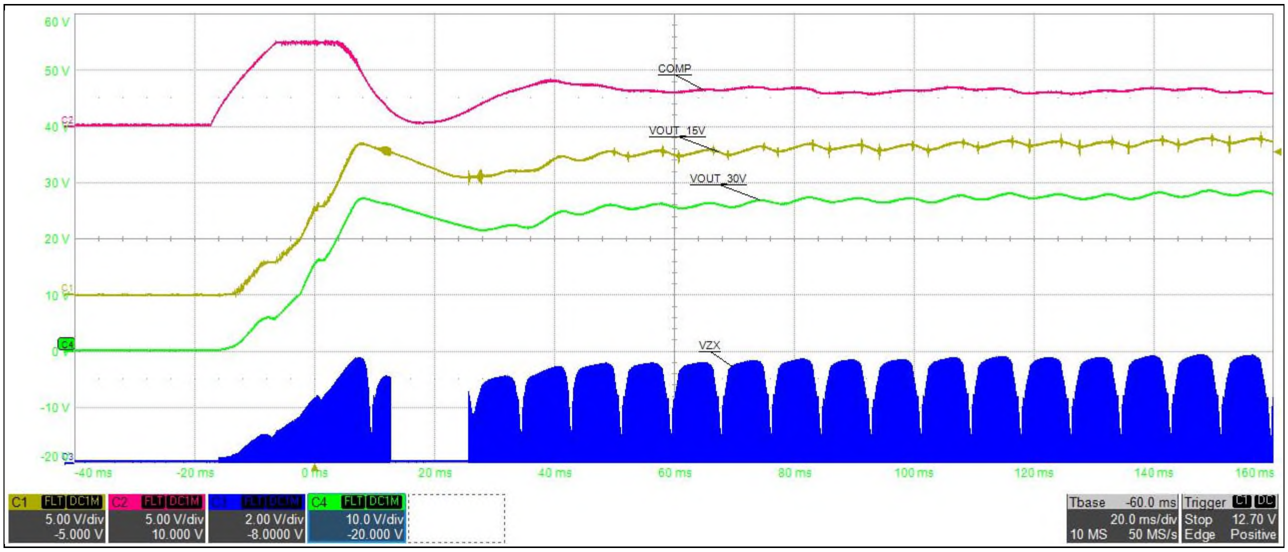


Figure 24 230 V AC start-up at 50 % load
30 V_{out} (green), V_{COMP} (red), 15 V_{out} (yellow), V_{ZX} (blue)

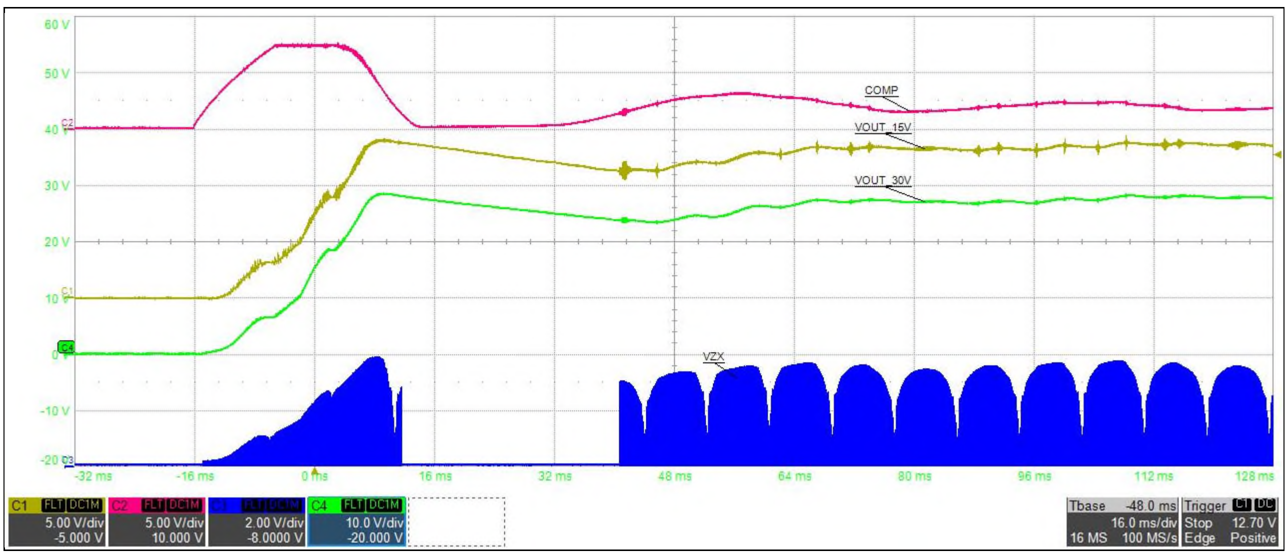


Figure 25 230 V AC start-up at 20 % load
30 V_{out} (green), V_{COMP} (red), 15 V_{out} (yellow), V_{ZX} (blue)

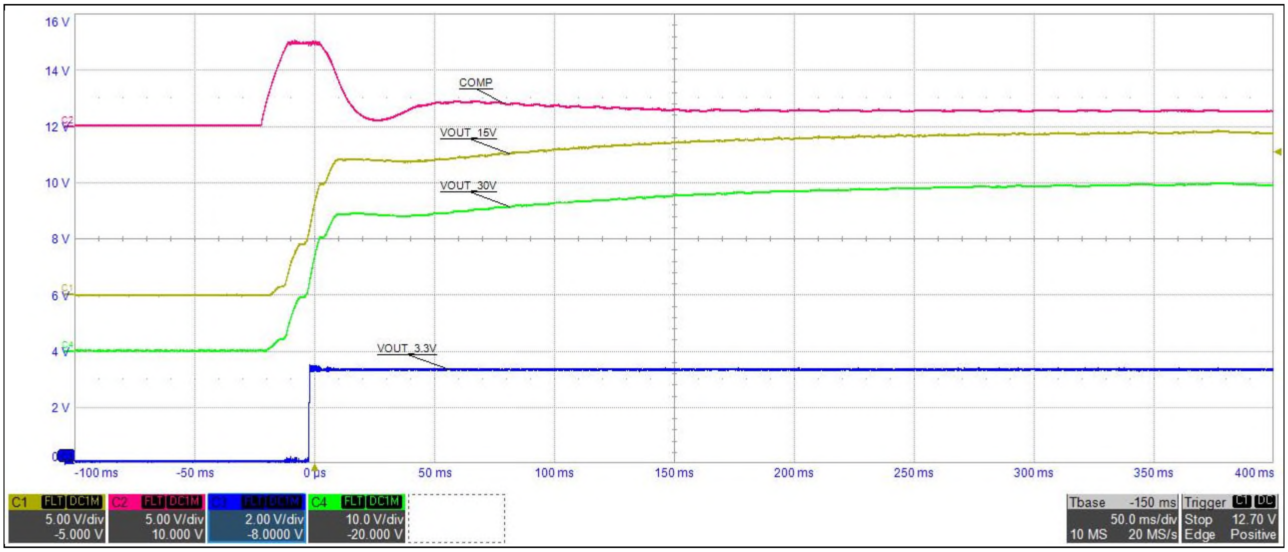


Figure 26 120 V AC start-up at 0 % load
30 V_{out} (green), V_{COMP} (red), 15 V_{out} (yellow), 3.3 V_{out} (blue)

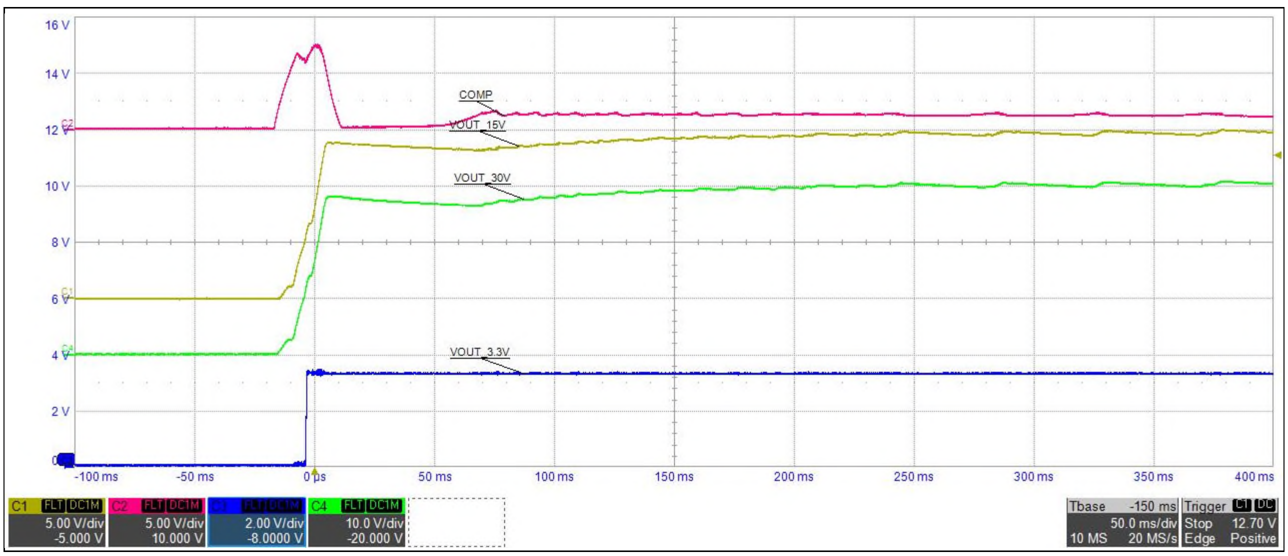


Figure 27 265 V AC start-up at 0 % load
30 V_{out} (green), V_{COMP} (red), 15 V_{out} (yellow), 3.3 V_{out} (blue)

9.4 Operation at line peak and zero crossing

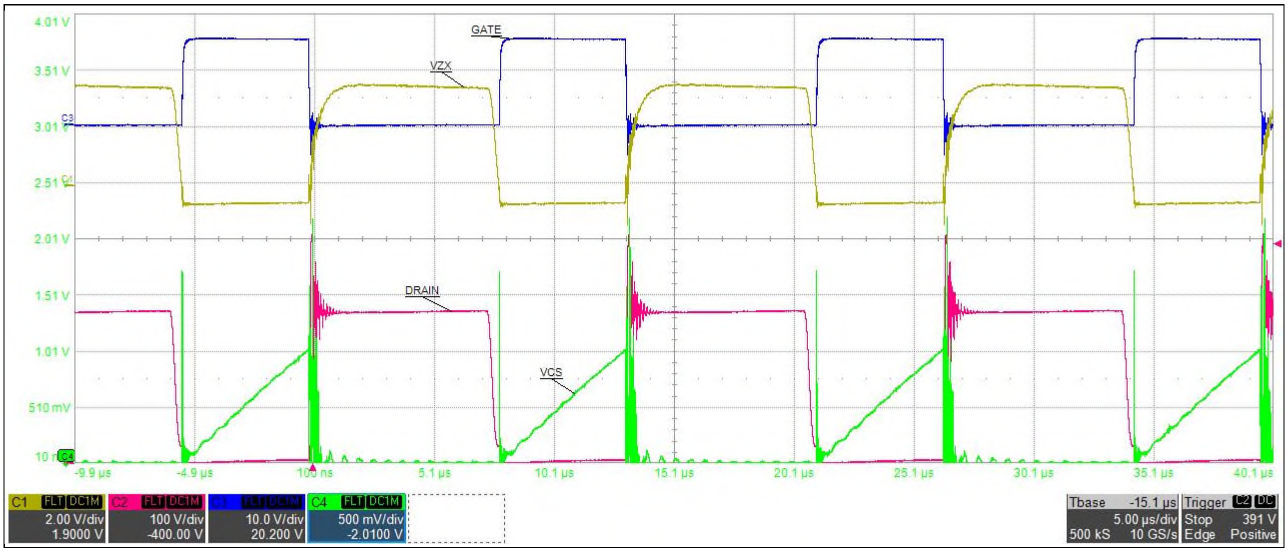


Figure 28 120 V AC at 100 % load, AC-line peak
Gate drive (blue), CS (green), V_{ZX} (yellow), V_{drain} (red)

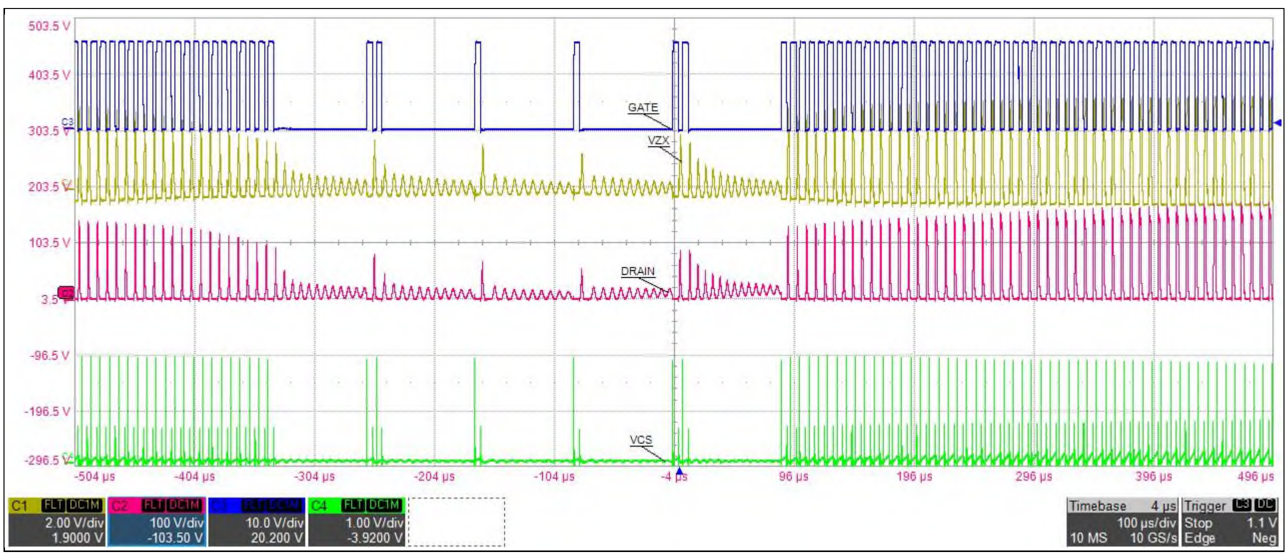


Figure 29 120 V AC at 100 % load line zero-crossing
Gate drive (blue), CS (green), V_{ZX} (yellow), V_{drain} (red)

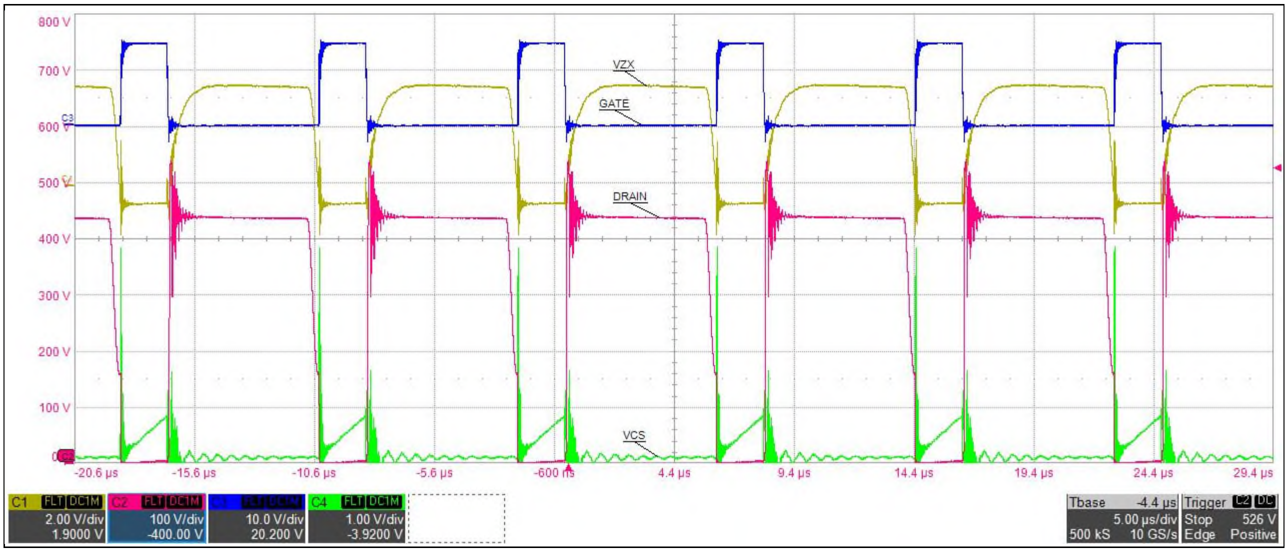


Figure 30 230 V AC at 100 % load line peak
Gate drive (blue), CS (green), V_{ZX} (yellow), V_{drain} (red)

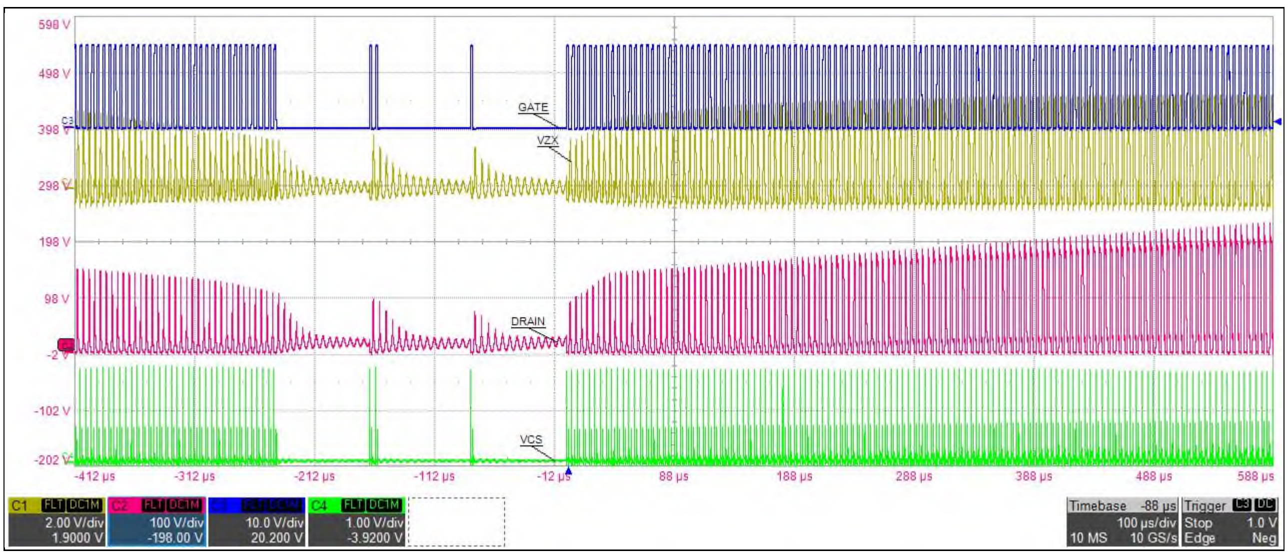


Figure 31 230 V AC at 100 % load line zero-crossing
Gate drive (blue), CS (green), V_{ZX} (yellow), V_{drain} (red)

Close to the line zero-crossing the amplitude of V_{ZX} is below the V_{ZX+} threshold of 1.54 V so the next switching cycle is not started until the re-start interval time-out period t_{WD}. This does not significantly impact PF and THD.

9.5 Burst mode operation at zero load

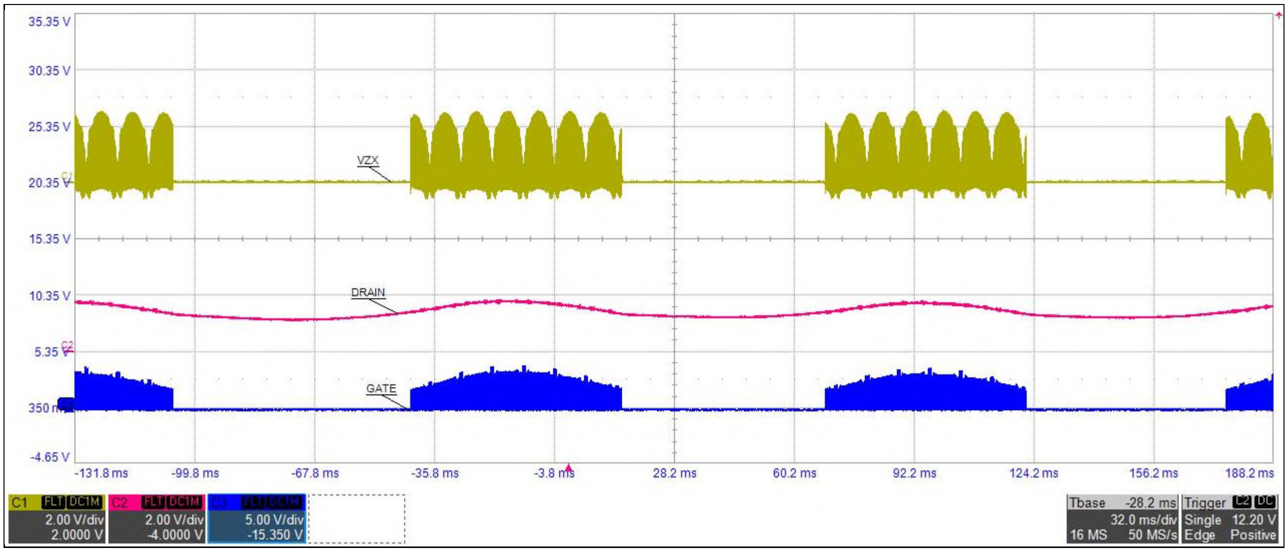


Figure 32 120 V AC start-up at 0 % load burst mode operation
Gate drive (blue), V_{ZX} (yellow), V_{OMP} (red)

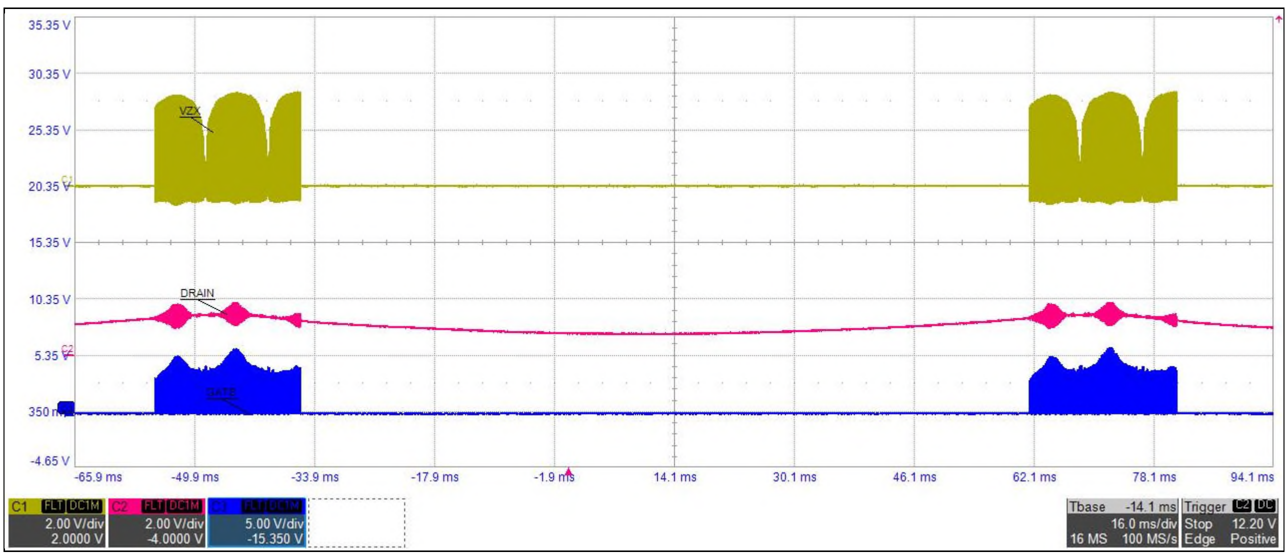


Figure 33 230 V AC start-up at 0 % load burst mode operation
Gate drive (blue), V_{ZX} (yellow), V_{COMP} (red)

9.6 Light-load DCM operation

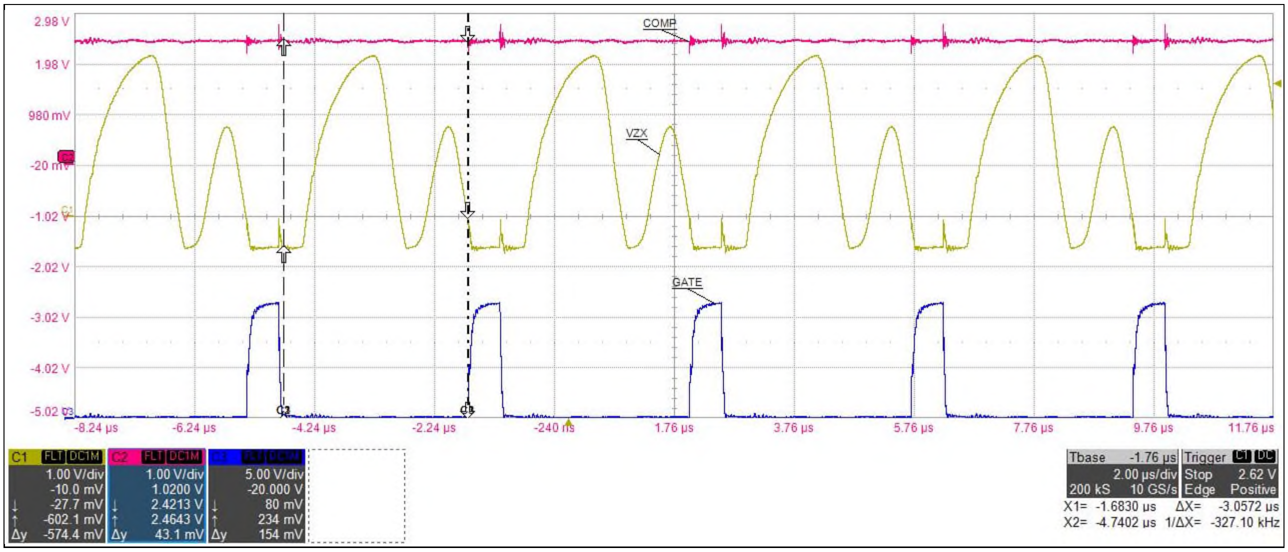


Figure 34 100 V AC start-up at zero load
Gate drive (blue), V_{ZX} (yellow), COMP (red)

9.7 HV start-up operation

The high-voltage start-up (HV pin) input current is measured with a 10 k resistor (RHV) connected from HV to the bus so that the oscilloscope traces in the following figures display approximately 1 mA/div:

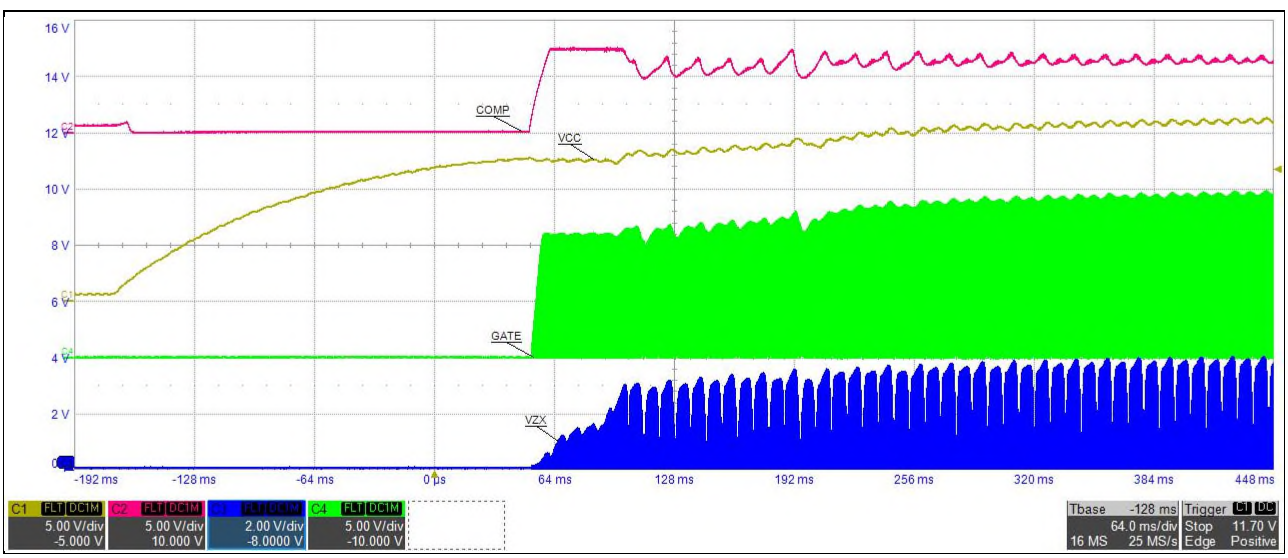


Figure 35 100 V AC start-up at 100 % load
COMP (red), ZX (blue), V_{CC} (yellow), gate drive (green)

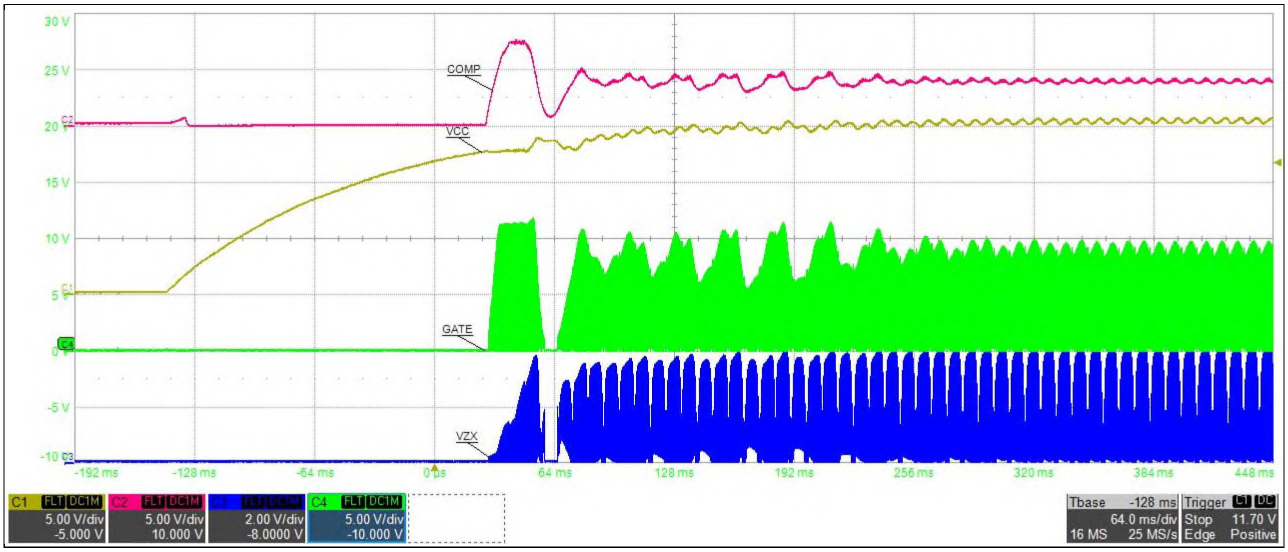


Figure 36 265 V AC start-up at 100 % load
COMP (red), ZX (blue), V_{CC} (yellow), gate drive (green)

9.8 HV start-up cell operation during zero-load burst mode

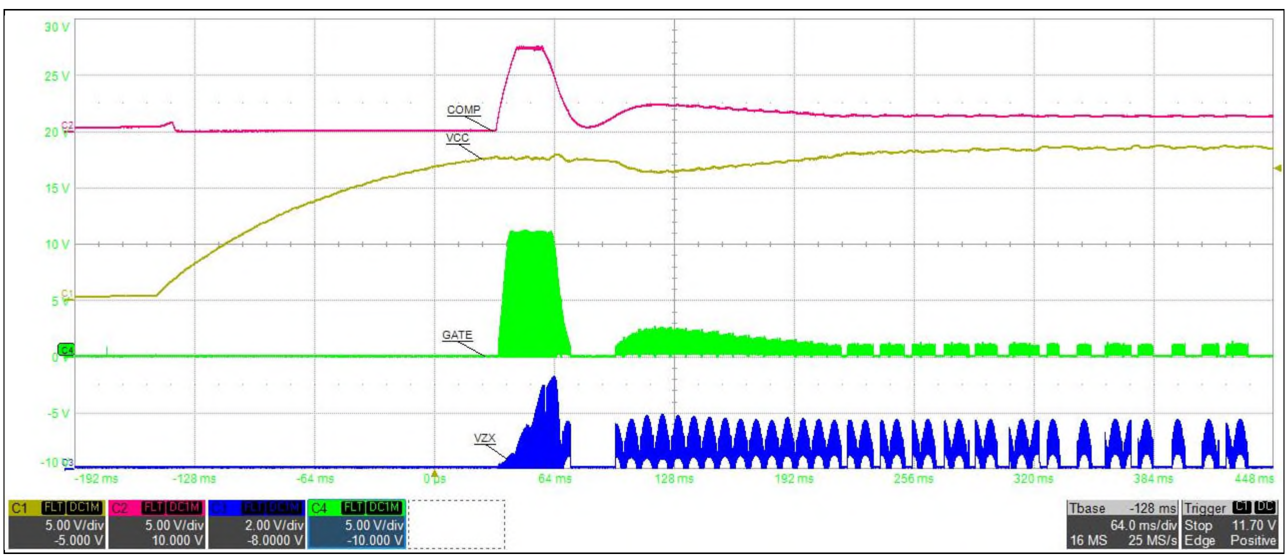


Figure 37 120 V AC start-up at 0 % load
COMP (red), ZX (blue), V_{CC} (yellow), gate drive (green)

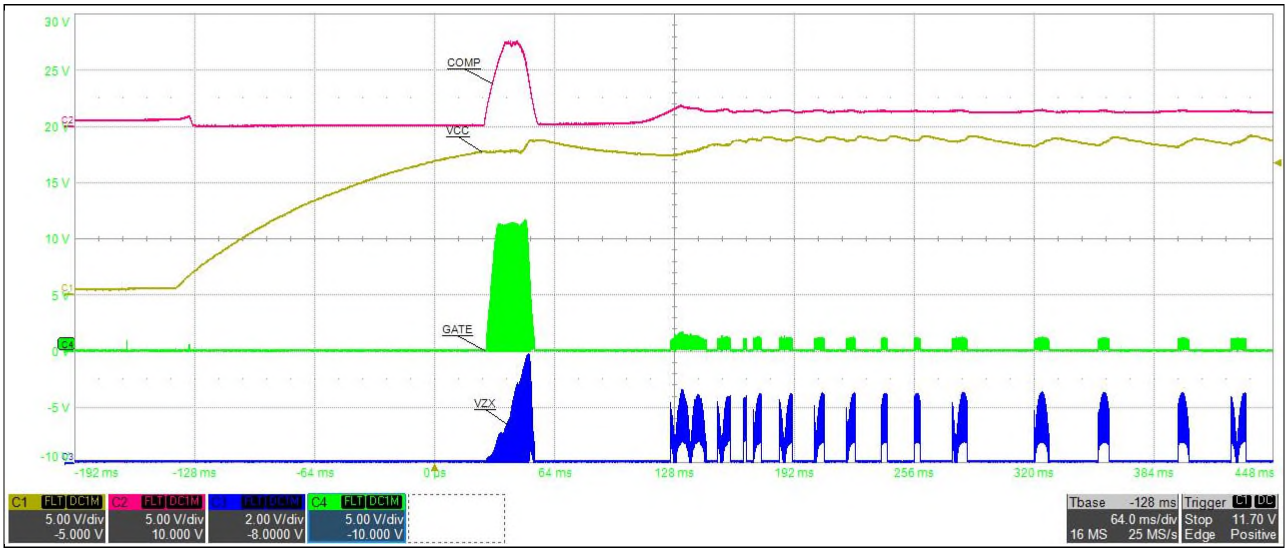


Figure 38 230 V AC start-up at 0 % load
COMP (red), ZX (blue), V_{CC} (yellow), gate drive (green)

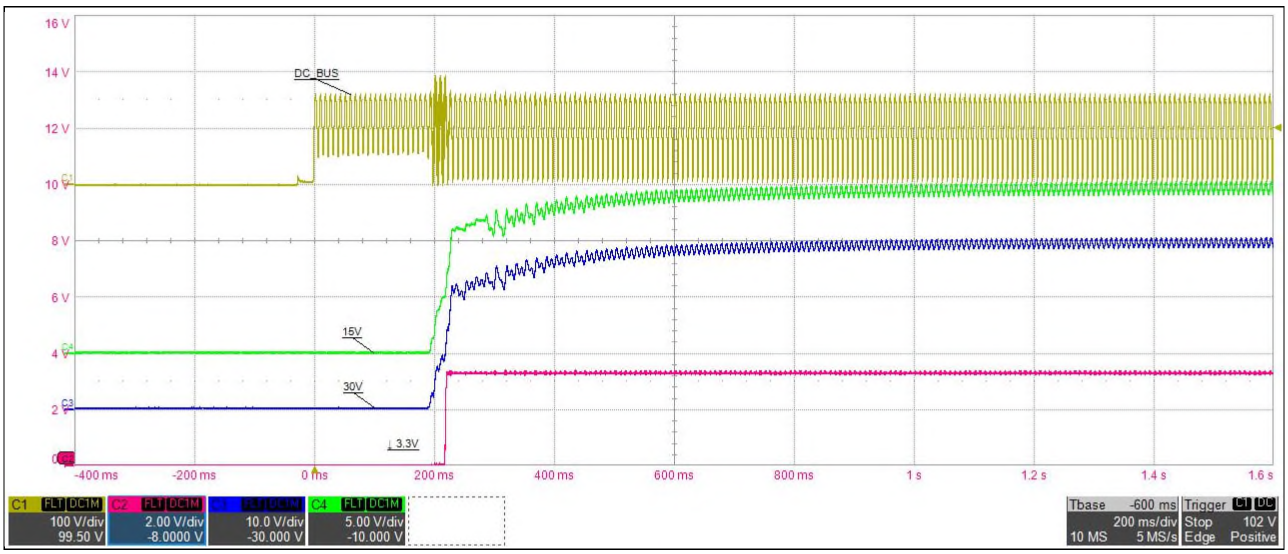


Figure 39 115 V AC start-up at 100 % load
DC bus (yellow), 3.3 V (red), 15 V (green), 30 V (blue)

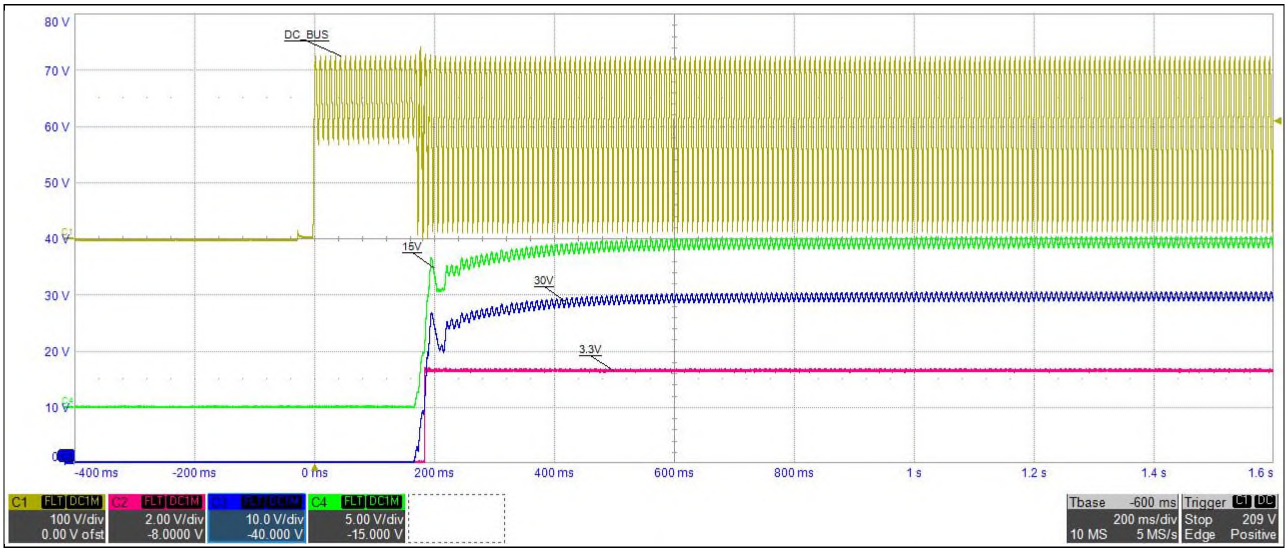


Figure 40 230 V AC start-up at 100 % load
DC bus (yellow), 3.3 V (red), 15 V (green), 30 V (blue)

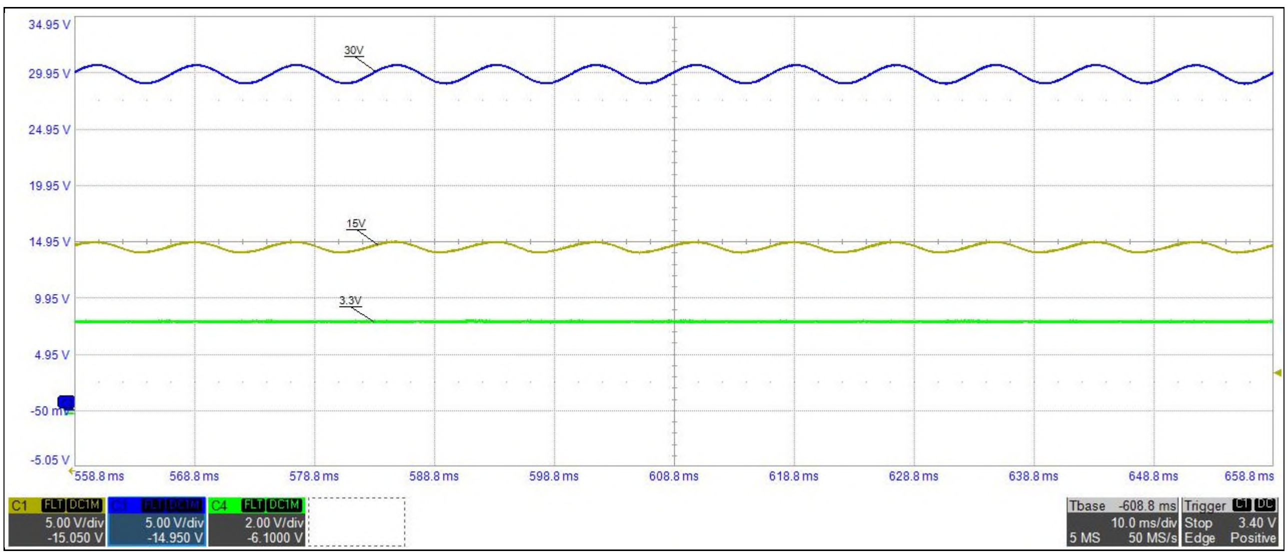


Figure 41 115 V AC steady-state at 100 % load
3.3 V (green), 15 V (yellow), 30 V (blue)

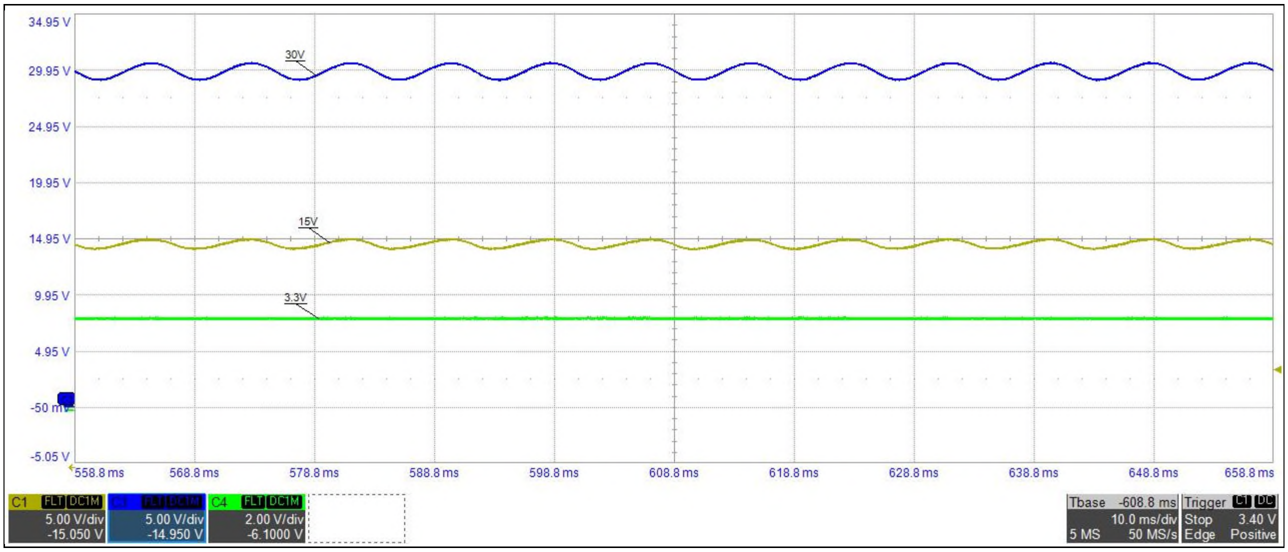


Figure 42 230 V AC start-up at 100 % load
3.3 V (green), 15 V (yellow), 30 V (blue)

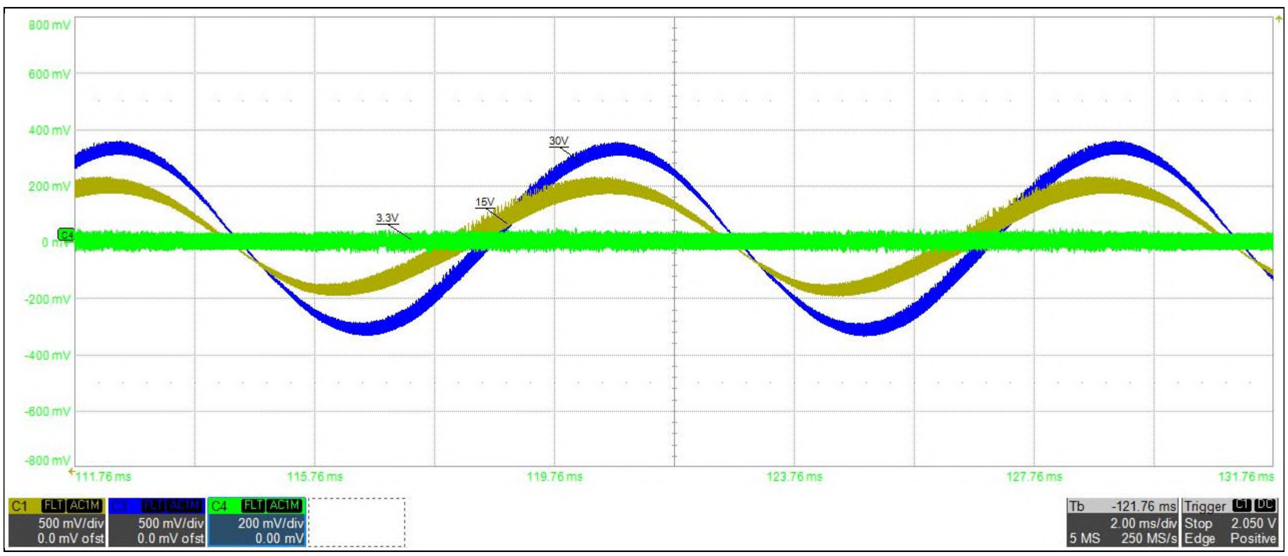


Figure 43 115 V AC ripple at 100 % load
3.3 V (green), 15 V (yellow), 30 V (blue)

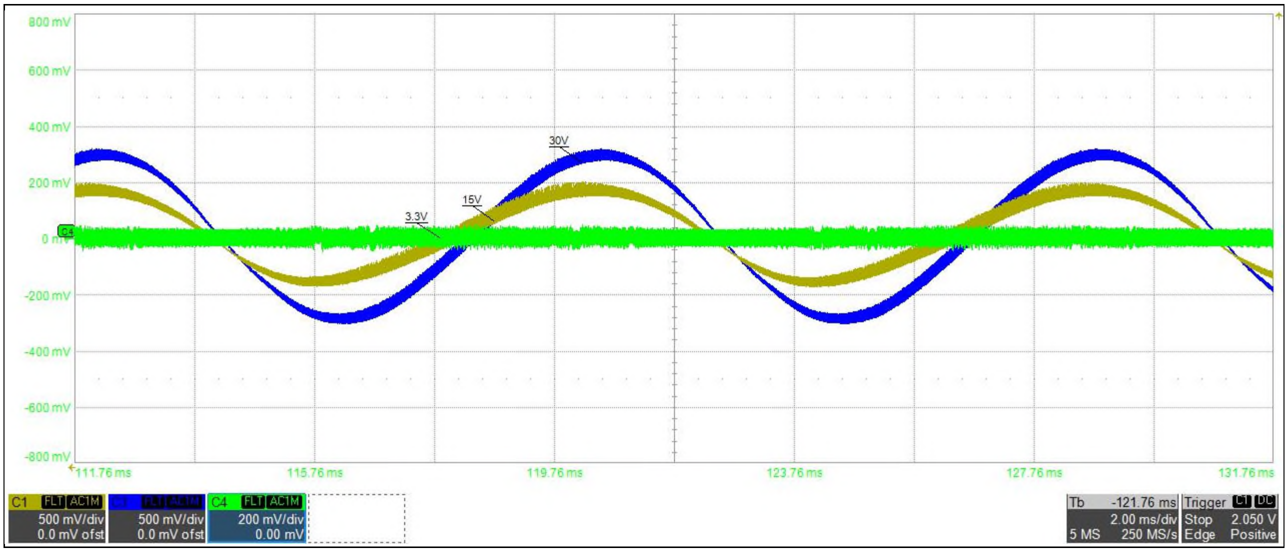


Figure 44 230 V AC ripple at 100 % load
3.3 V (green), 15 V (yellow), 30 V (blue)

9.9 Thermal performance under normal operating conditions

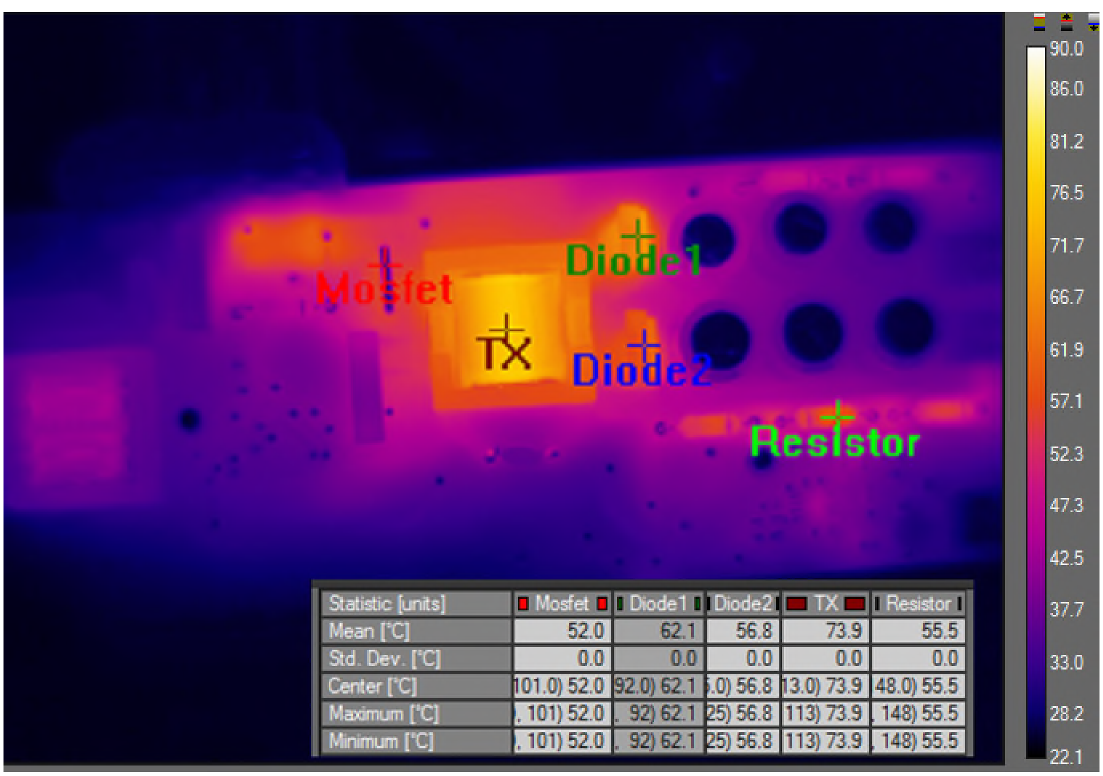


Figure 45 115 V AC at 100 % load (board top side)

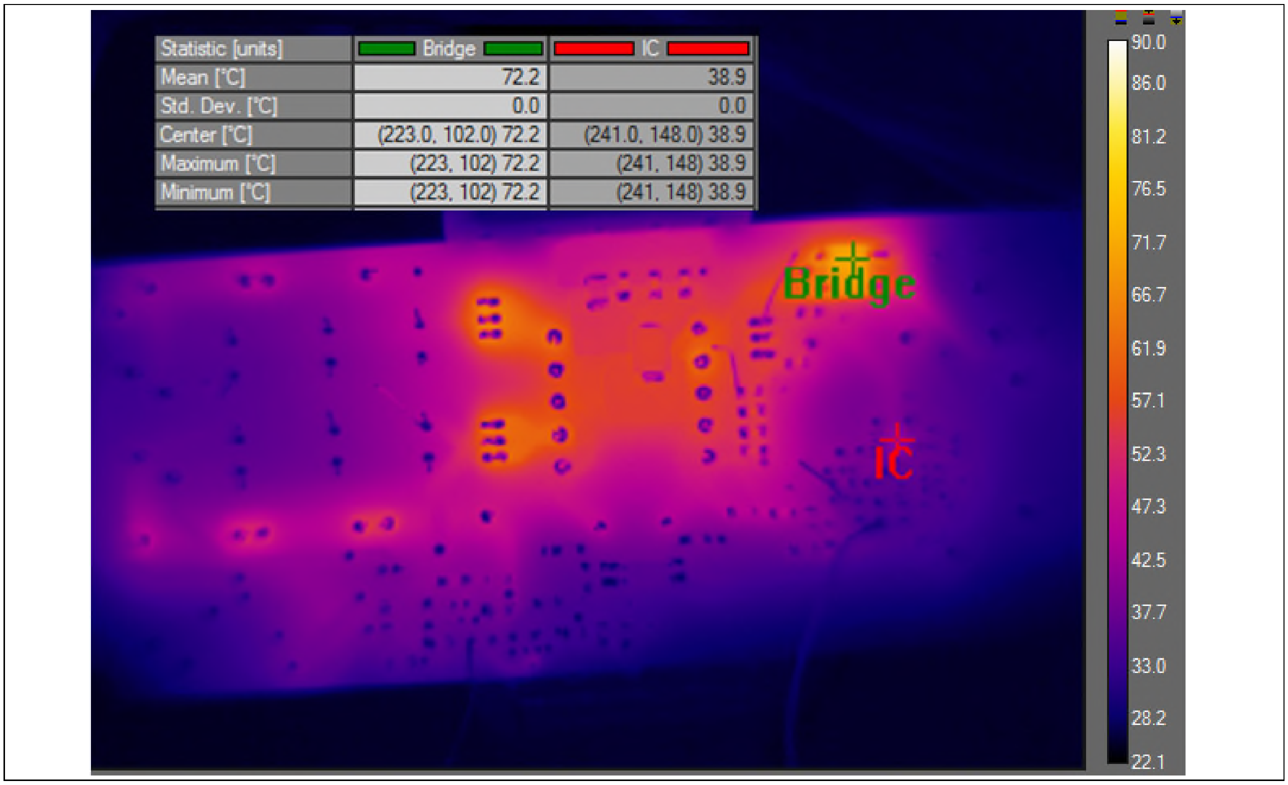


Figure 46 115 V AC at 100 % load (board bottom side)

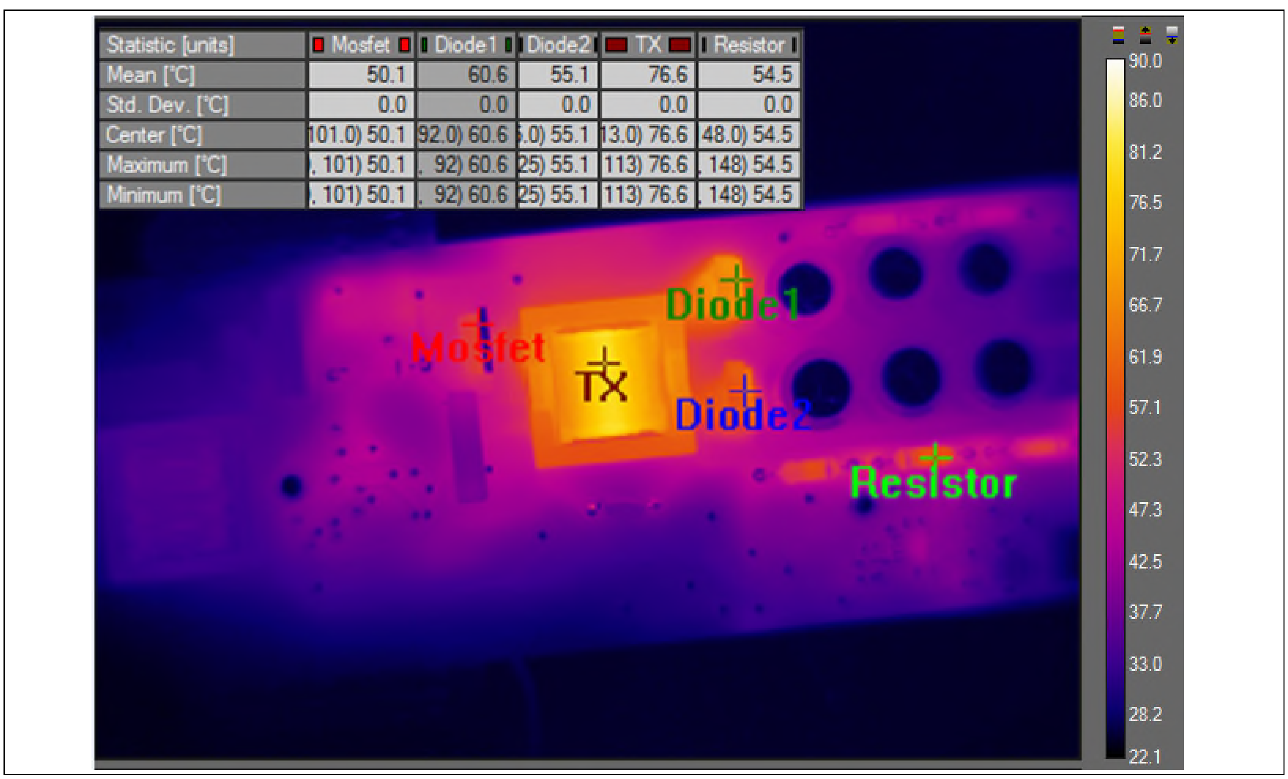


Figure 47 230 V AC at 100 % load (board top side)

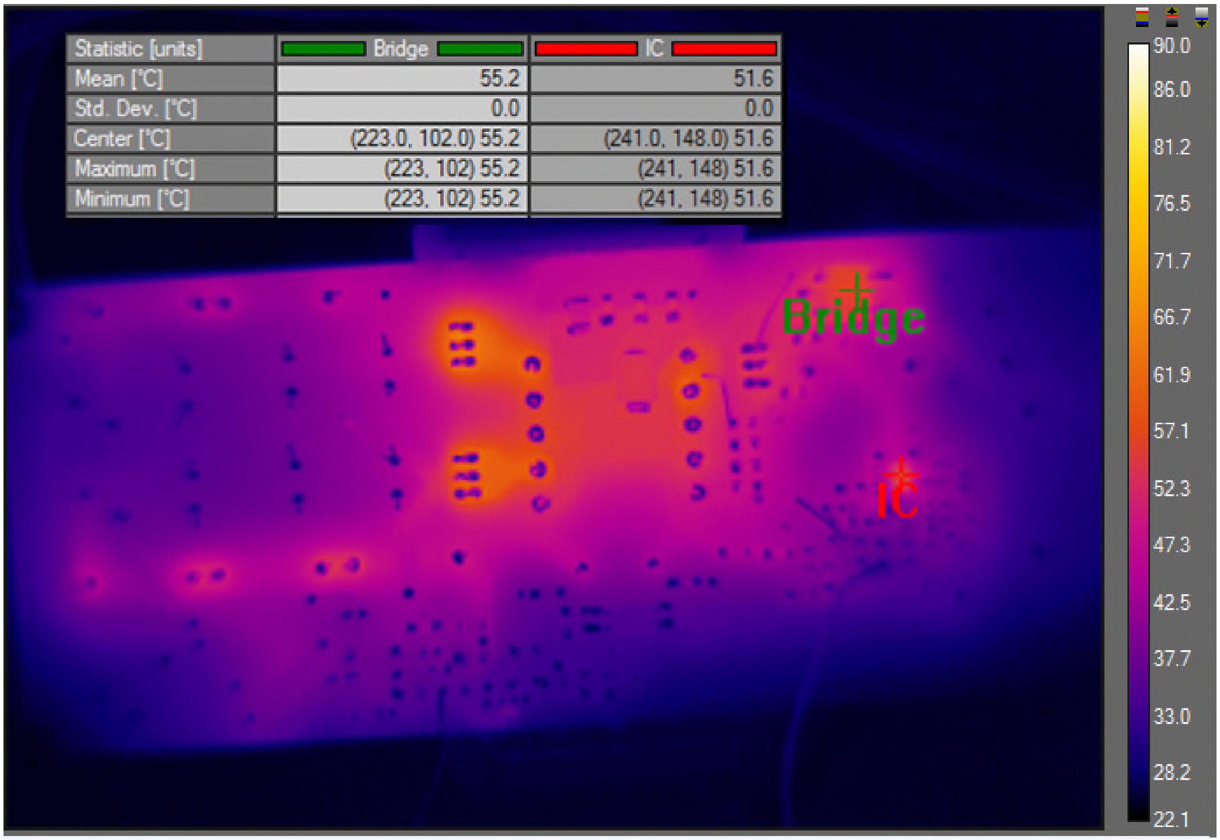


Figure 48 230 V AC at 100 % load (board bottom side)

9.10 Line current harmonics according to EN 61000-3-2

Table 3 EN61000-3-2 class C limits for system power greater than 25 W

Requirements	Harmonics Limits Class C according EN 61000-3-2 for System Power > 25W	
	Harmonics order n	Maximum value expressed as a percentage of the fundamental input current
	2 3 5 7 9 11 ≤ n ≤ 39	<2% <30 λ % 10% <7% <5% <3% λ = power factor

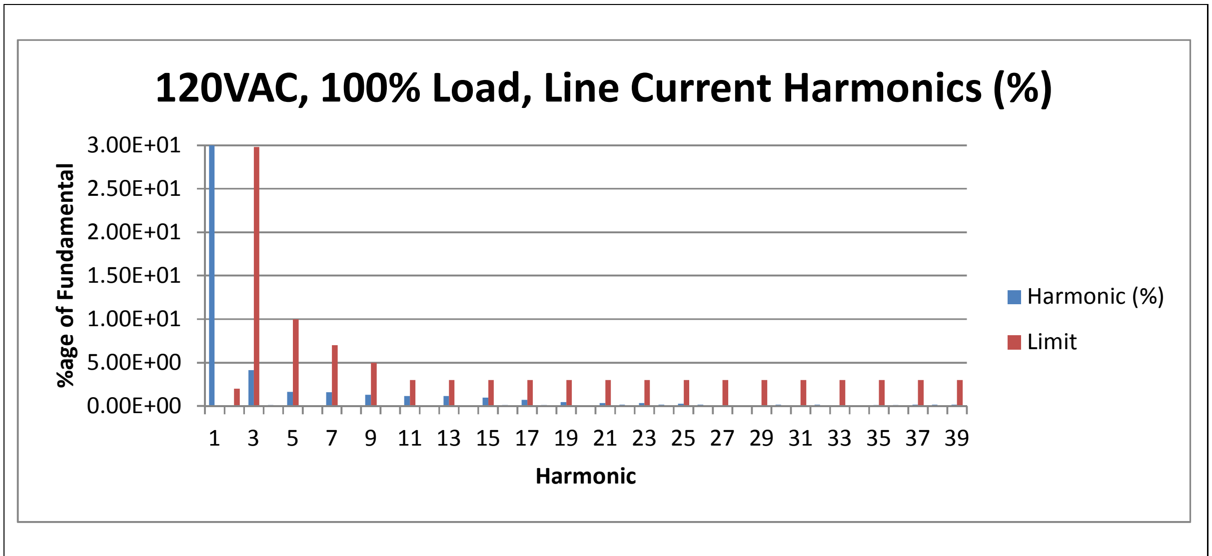


Figure 49 Harmonic test results at 120 V AC and 100 % load

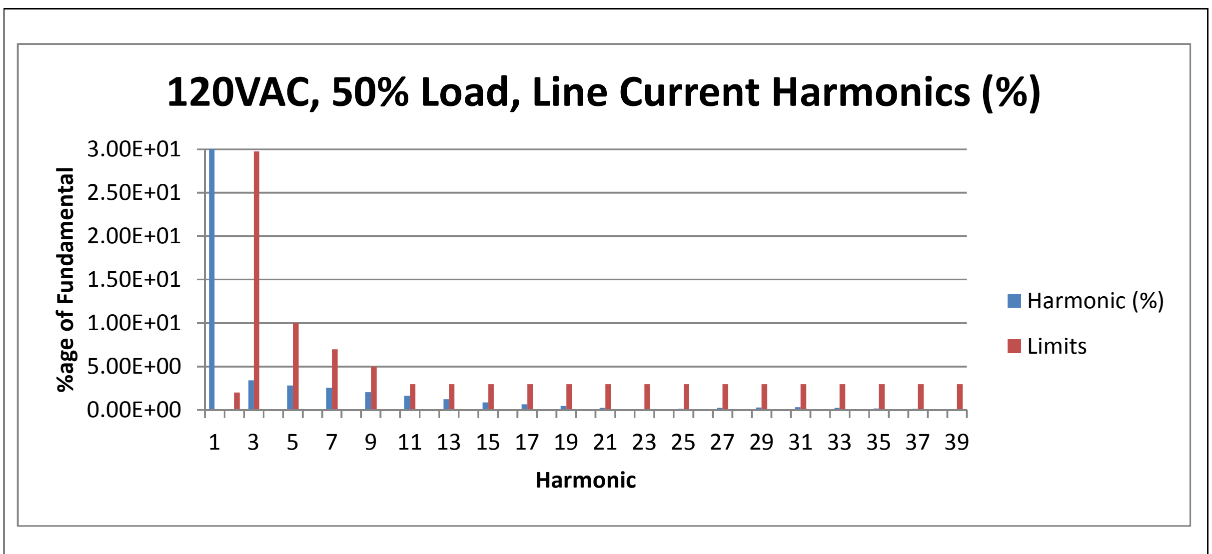


Figure 50 Harmonic test results at 120 V AC and 50 % load

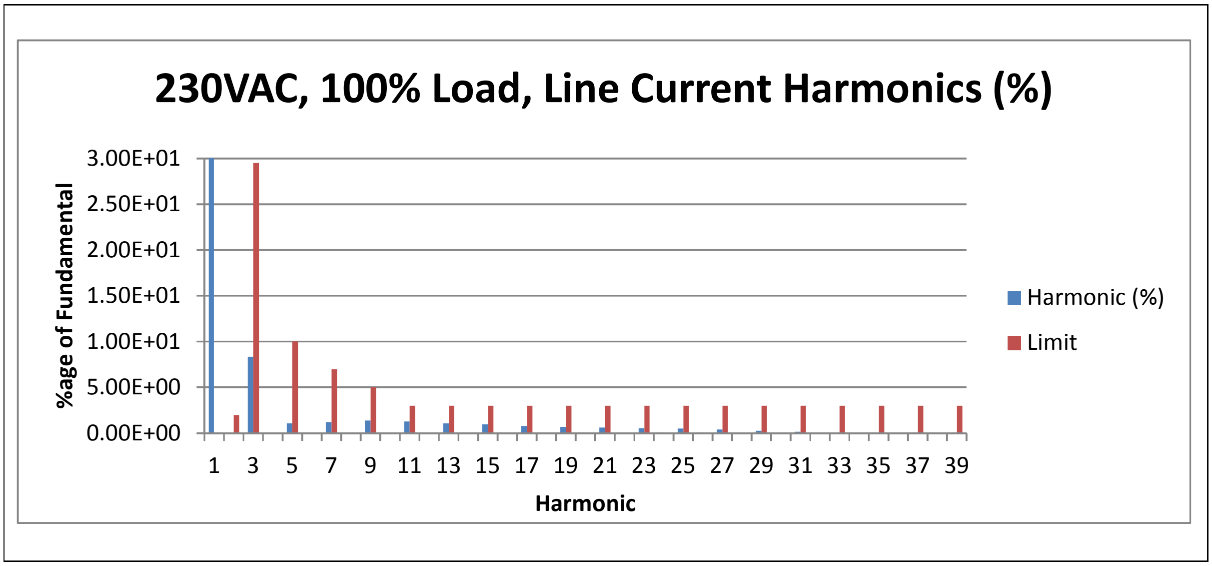


Figure 51 Harmonic test results at 230 V AC and 100 % load

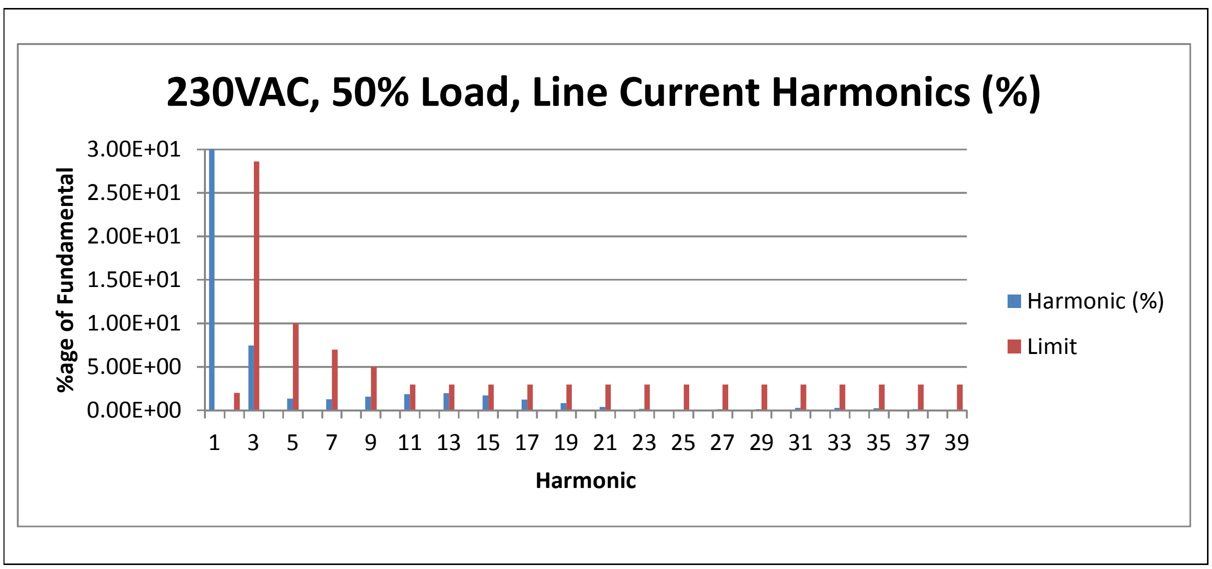


Figure 52 Harmonic test results at 230 V AC and 50 % load

Class C limits are met at 50 % and 100 % loads at 120 V AC and 230 V AC.

9.11 EMI conducted emissions (tested to CISPR22 limits)

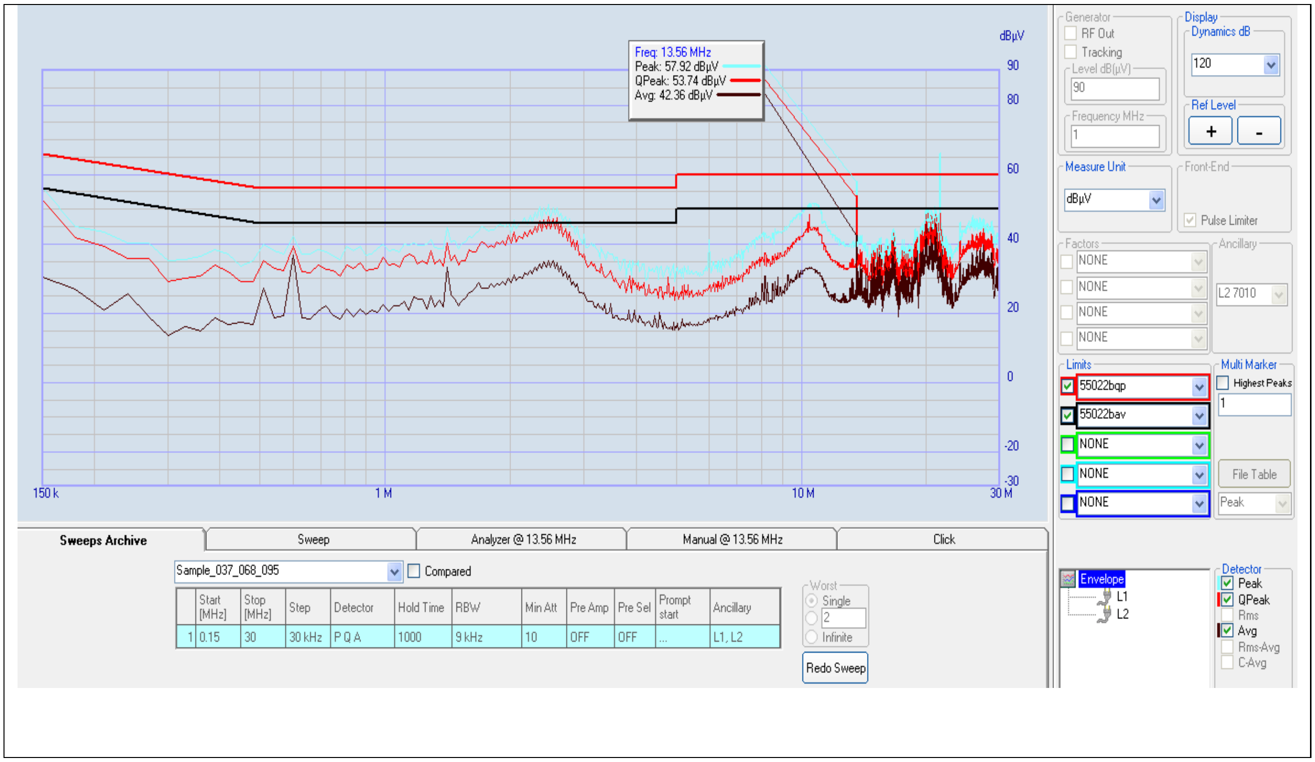


Figure 53 Conducted emissions at 115 V AC and 100 % load

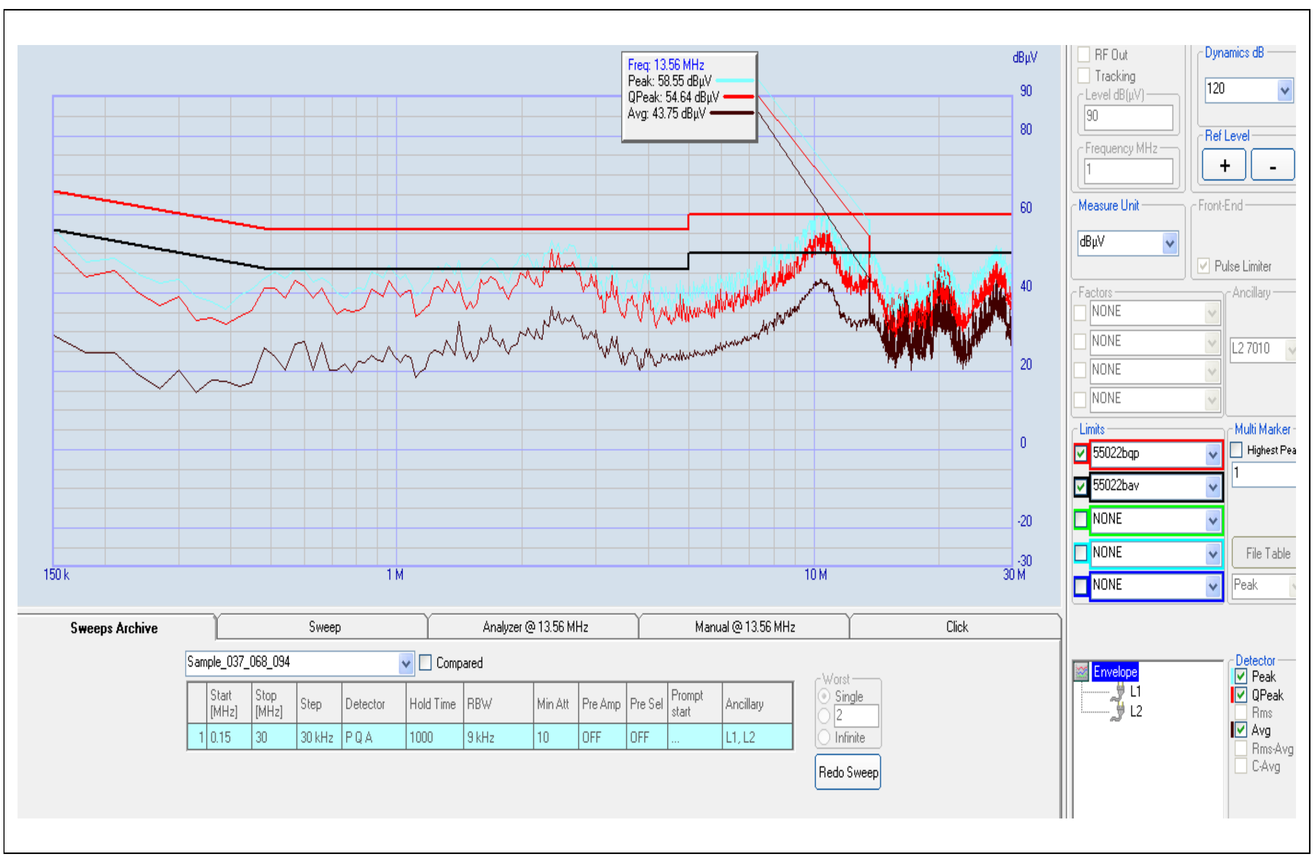


Figure 54 Conducted emissions at 230 V AC and 100 % load

The red limit line shows the limit for the quasi-peak measurement, for which the frequency sweep trace is also shown in red. To pass the red trace must remain below the red limit line and the black average measurement trace must remain below the black average limit line. The light blue trace may be disregarded.

EMI emissions are very dependent on the board layout.

Note

Infineon Technologies does not guarantee compliance with any EMI standard.

10 Conclusion

This application note explains the design and selection of components for a multiple-output flyback converter. The IRS2982 IC was used for primary control and PFC and the IFX91041 IC was used as a buck step-down regulator for the 3.3 V output. The 36 W multi-output flyback converter was designed using low-cost components to provide the functionality of a PFC flyback AC-DC power supply. PF remains above 0.9 at 115 V AC and 230 V AC nominal inputs from 40 % load to 100 %. The iTHD remains below 20 % from 40 % to 100 % load over the input AC-line range and meets IEC61000-3-2 class C individual harmonic limits.

Quasi-peak and average conducted emission sweeps fall within limits over the frequency spectrum from 150 kHz to 30 MHz. It should be noted that these measurements were not made by a certified test lab and are intended only as an indication of performance. Conducted EMI complies with CISPR22 quasi-peak and average iimits. The demo board has demonstrated that good cross-regulation can be achieved except at light-load conditions where it is necessary to add some pre-loading to prevent output voltages rising above the desired levels.

Thermal performance under normal operating conditions (measured in the open air at 25°C ambient temperature), as shown in section 9.9, indicates a temperature rise of 49°C at the transformer windings at low-line and 51°C at high-line. However the core remains at a lower temperature. The input bridge (BR1) operates at low-line with a rise of 47°C with a greatly reduced temperature rise at high-line of 30°C. The MOSFET has a 27°C rise at low-line and a 25°C rise at high-line due to higher primary peak current at low-line for the IPP80R450P7 measured with no heatsink attached.

Under all normal conditions the HV start-up cell is deactivated as the FB loop closes and it switches over from start-up mode to support mode. The HV cell allows the power supply to start up rapidly at any line input voltage, meeting the maximum specification of 400 ms from switch-on to reaching nominal output voltage.

In conclusion, the IRS2982S-based flyback converter design provides an excellent performance and robustness with tight control and reliable protection. This design is well suited to various applications such as set-top boxes, low voltage brushless DC controls, motor control drives, three-phase BLDC, etc.

Test results show that the design specifications are met.

11 References

[1] IRS2982SPBF SMPS control IC datasheet, Infineon Technologies

[2] IFX91041 Buck control IC, Infineon Technologies
https://www.infineon.com/dgdl/091130AppNote_IFX91041_Filter_Rev1.0.pdf?fileId=db3a30432a14dd54012a3d1cc78b59e6

[3] Peter. B. Green, 55 W flyback converter design using the IRS2982S controller

https://www.infineon.com/dgdl/Infineon-ApplicationNote_55WFlyback_ConverterDesign_IRS2982S_controller_IRXLED04-AN-v01_02-EN.pdf?fileId=5546d46253f6505701547c76f7d57264

[4] Peter. B. Green, Triac dimmable non-isolated flyback converter using the IRS2982S controller IRXLED06

https://www.infineon.com/dgdl/Infineon-UG_201607_PL16_035-AN-v01_00-EN.pdf?fileId=5546d4625a888733015aab2ec62045e8

[5] Peter. B. Green, Using the IRS2982S in a PFC flyback with opto-isolated feedback

https://www.infineon.com/dgdl/Infineon-AN_201610_PL16_01-AN-v01_00-EN.pdf?fileId=5546d4625a888733015a91a5e0fa622e

[6] Christophe Basso, Switch-Mode Power Supplies, Spice Simulations and Practical Designs, 2nd Edition

[7] Raymond Ridley, Power Supply Design, Vol 1 : Control

Revision history

Document version	Date of release	Description of changes
		First release
1.2		Changed schematic and few waveforms
1.3		Schematic was separated into 2 figures

Other Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2018-07-11

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

AN_1802_PL16_1803_202736