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Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Reference designs .xdc examples
Reference Designs & Application Notes	Reference design prepared for the logiHSSL-ZU starter kit
Additional Items	logiHSSL-ZU FPGA HSSL Starter Kit
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon	

Features

- Supports Xilinx® 7 Series, UltraScale™ and UltraScale+™ FPGAs, Zynq®-7000 SoC and UltraScale+ Zynq MPSoC device families
- Slave controller IP core compatible with the High Speed Serial Link (HSSL) native interface from Infineon Technologies AG
- Aimed at safety-critical automotive applications
- Enables easy interfacing between Infineon's AURIX™ TC2xx and TC3xx microcontrollers and Xilinx FPGA and SoC/MPSoC devices
- Low pin count (2 x 2 LVDS, 1 x clock)
- Supports baud rates of up to 320 Mbaud/s at a net payload data-rate of up to 84%
- Implements ARM® AMBA® AXI4–Lite Slave bus compliant interface and enables easy access to internal registers inside the logiHSSL IP
- Implements ARM AMBA AXI4 Master bus compliant interface that enables logiHSSL IP an easy access to 3 GB of local Xilinx device addressable space (from 0x00000000 to 0xBFFFFFFF). This enables AURIX microcontroller to access:
  - Registers and on-chip RAM in programmable logic (access to internal register spaces of other IPs)
  - Register space and On-Chip Memory (OCM) in the processing system through High priority ports.
  - On-board linearly addressable Flash memory
  - On-board DDR memory through local memory controllers
- logiHSSL-ZU FPGA HSSL Starter Kit is available from Xylon
- Prepared for the Xilinx Vivado® Design Suite

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz)	LUT	FF	IOB	CMT	BRAM	MULT/ DSP48/E	DCM / CMT	GTx	Design Tools
Zynq®-7000 (xc7z045ffg900)	80	7188	2002	0	0	2	0	0	0	Vivado 2018.1
Zynq® UltraScale+™ (xczu9eg-ffvb1156-2)	80	7067	2024	0	0	2	0	0	0	Vivado 2018.1

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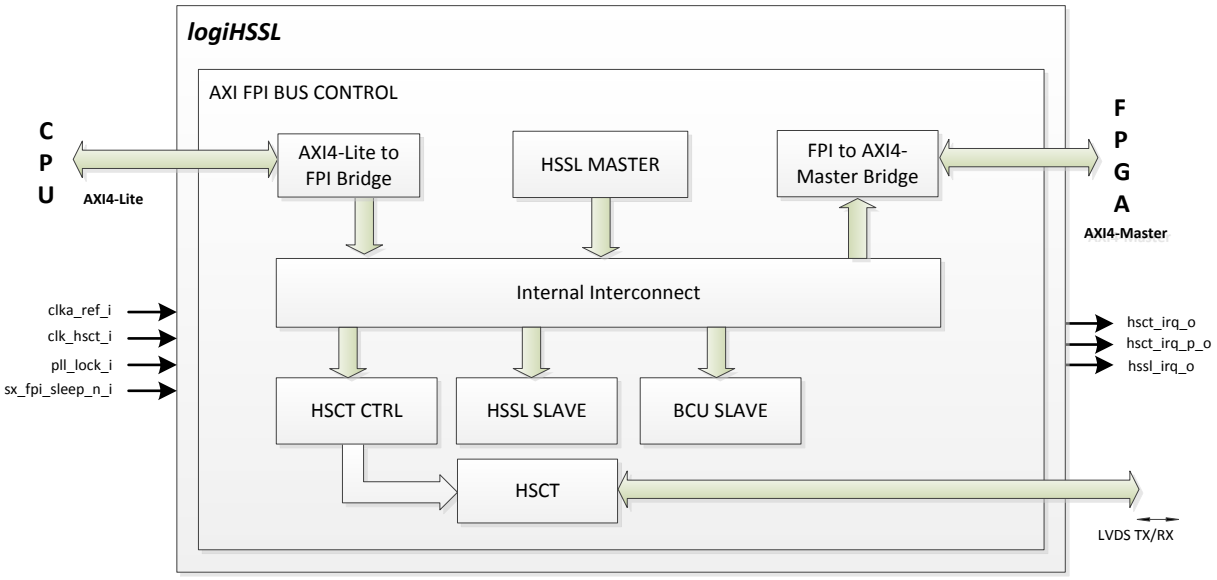

Figure 1: logiHSSL Architecture

Applications

Emerging automotive and industrial applications, such as the Advanced Driver Assistance (ADAS) and Automated Driving (AD), that are both performance-hungry and safety-critical. Typically the supporting system architectures use the Xilinx FPGA and SoC devices for data aggregation, pre-processing and data distribution tasks, and the Infineon AURIX microcontrollers to provide the ASIL D level functional safety.

General Description

The logiHSSL IP core enables high-speed communication between microcontrollers of Infineon's AURIX family (TC2xx and TC3xx) and Xilinx SoC (System-on-Chip), MPSoC (Multi-Processor SoC) and FPGA (Field Programmable Gate Arrays) devices via the Infineon High Speed Serial Link (HSSL). This serial link supports baudrates of up to 320 Mbaud at a net payload data-rate of up to 84%.

The new IP core allows system designers to combine functional safety and security provided by AURIX with the wide range of functional possibilities brought to the table by the Xilinx devices. Linked devices can access and control each other's internal and connected resources through the HSSL link. The logiHSSL IP is prepared for the Xilinx Vivado Design Suite to enable quick and efficient resource implementations in the latest Xilinx All Programmable devices for use in the embedded systems that meet the highest safety standards.

Functional Description

The logiHSSL IP core is an IP block for the Xilinx Vivado development flow. It includes the embedded Infineon High Speed Serial Interface (HSSL) and a control unit to connect an external Infineon AURIX automotive microcontroller with a Xilinx FPGA and/or ARM processing unit (SoC, MPSoC) for the purpose of the data exchange.

Following the architectural block diagram shown in Figure 1, five major modules can be identified.

HSCT Layer

The HSCT layer is the implementation of the HSCT link layer. It is the physical layer of the HSSL protocol.

HSSL Control Unit

The HSSL control unit is the IP core's main module that facilitates the control over the HSSL protocol, which includes the HSSL layer (upper layer) and HSCT layer (lower layer). The control is interfaced to the CPU by means of register set. There are separate register sets for HSSL and HSCT layers control.

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Internal Interconnect

Internal interconnect is a bus architecture that connects all units within the IP core.

AXI4–Lite Interface (Slave)

AXI4–Lite slave interface is used to access all IP core's registers within the HSSL control unit. It facilitates a bridge from the AXI4–Lite bus to the internal interconnect.

AXI4 Interface (Master)

IP core can access any AXI-addressable space in the FPGA/SoC/MPSoC through the AXI4 master interface. It facilitates a bridge from the internal interconnect to the AXI4 bus architecture, including the corresponding address remapping.

For more information on internal architecture of the HSSL protocol control (HSCT layer and HSSL control unit), as well as on the internal interconnect architecture, see AURIX TC27x C-Step 32-Bit Single-Chip Microcontroller documentation from Infineon.

Core I/O Signals

Table 2: Core I/O Signals

Signal	Signal Direction	Description
AXI4 - Master Interface	Bus	Refer to ARM AMBA AXI4 specification
AXI4 - Lite Interface	Bus	Refer to ARM AMBA AXI4 specification
clka_ref_i	Input	Input Reference Clock. It can be generated internally inside the Xilinx device, or generated from the Infineon microcontroller's (Master) side (preferred option).
clk_hsct_i	Input	A total of 5 high speed clocks for HSCT PHY module generated from the clka_ref_i clock.
hsct_irq_o	Output	HSCT interrupt signal
hsct_irq_p_o	Output	IRQ pulse widener Signal
hssl_irq_o	Output	HSSL interrupt signal
lvdsrx_data_ser_i lvdsrx_data_ser_o	Input Output	LVDS serial input and output that allows for bi-directional HSL communication.
pll_lock_i	Input	PLL Lock Signal Lock Detection. Indicates the state of the PLL within the clocking logic. Lock is asserted only when PLLs generating all the necessary clocks are locked – 5 clk_hsct_i clocks.
sx_fpi_sleep_n_i	Input	Turn Off Request from the processor. Going into the HSCT protocol sleep mode requires all transfer activities finished and no more frames queuing for transmission. The user enables or disables sleep mode during module initialization phase.

Verification Methods

The logiHSSL is fully supported by the Xilinx Vivado (IPI) Design Suits. This tight integration tremendously shortens IP integration and verification. A full logiHSSL implementation does not require any particular skills beyond general Xilinx tools knowledge. For more information, please contact Xylon Technical Support:

Email: support@logicbricks.com

Recommended Design Experience

The user should have experience in the following areas:

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- Xilinx design tools
- ModelSim

Available Support Products

To jump-start new designs that combine the Infineon's AURIX microcontrollers with the Xilinx All Programmable FPGA and SoC devices and solve the rising safety and performance requirements in emerging automotive and industrial designs, Xylon offers the complete logiHSSL-ZU FPGA HSSL Starter Kit. The kit includes the complete hardware platform built of the Xilinx UltraScale+ MPSoC based ZCU104 Evaluation Kit and the Infineon AURIX Evaluation board with the necessary cabling. Additionally, it comes with the fully functional reference hardware design. To learn more about this product, please contact Xylon or visit our web site:

Email: sales@logicbricks.com
URL: https://www.logicbricks.com/Products/logiHSSL-ZU.aspx

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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2100 Logic Drive
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Infineon AURIX/TriBoard and HSSL

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Revision History

Version	Date	Note
1.00.	08.05.2019.	Initial Xylon release.

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