Isolated multiple rail buck converter using TDA38825

20 A buck regulator

About this document

Scope and purpose

This document summarizes the application of designing an isolated multiple rail buck converter using TDA38825.

Intended audience

The intended audience for this document includes FAEs, customers, and application engineers who work on the design and development of power conversion circuits with fast constant on-time (COT) Point of Loads (POLs) products.

V 1.0
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1 Introduction

Among Infineon's POL product families, the proprietary Fast COT is the most popular loop control. It achieves fast load transient as conventional COT control does, at the same time, maintains high DC accuracy in Vout as voltage mode and current mode control do. See [1] for an introduction of the Fast COT control.

Power supply circuits come in the form of voltage step-up (boost) or the more common step-down (buck) DC-DC converter. Many of today's applications require multiple voltage rails to drive a variety of ICs. These rails can be inverting or non-inverting, with or without isolation. While designers typically use multiple buck converters with single filter inductors, they add cost, footprint, and height. A simpler alternative is to use a single buck converter with coupled inductors or transformers configured in isolated converter topologies. Designers can use the buck converter for inverting or non-inverting voltage rails and configure it for use as an inverting buck-boost converter. Coupled inductors or transformers can also be used with a buck-boost converter to generate multiple inverting or non-inverting outputs with voltage step up/down function.

This application note will discuss about the isolated DC-DC topology and demonstrate how they can be implemented using a synchronous buck converter TDA38825.

1.1 Typical applications:

Galvanic isolation and multiple output applications are common in various power electronics applications such as:

- Telecommunications, industrial programmable logic controllers (PLCs)
- Industrial factory automation, isolated communication interfaces (i.e., RS-485, RS-232)
- Bias supplies for gate drives, sensors, op amps, motor drive applications, and any application that requires positive and negative rails

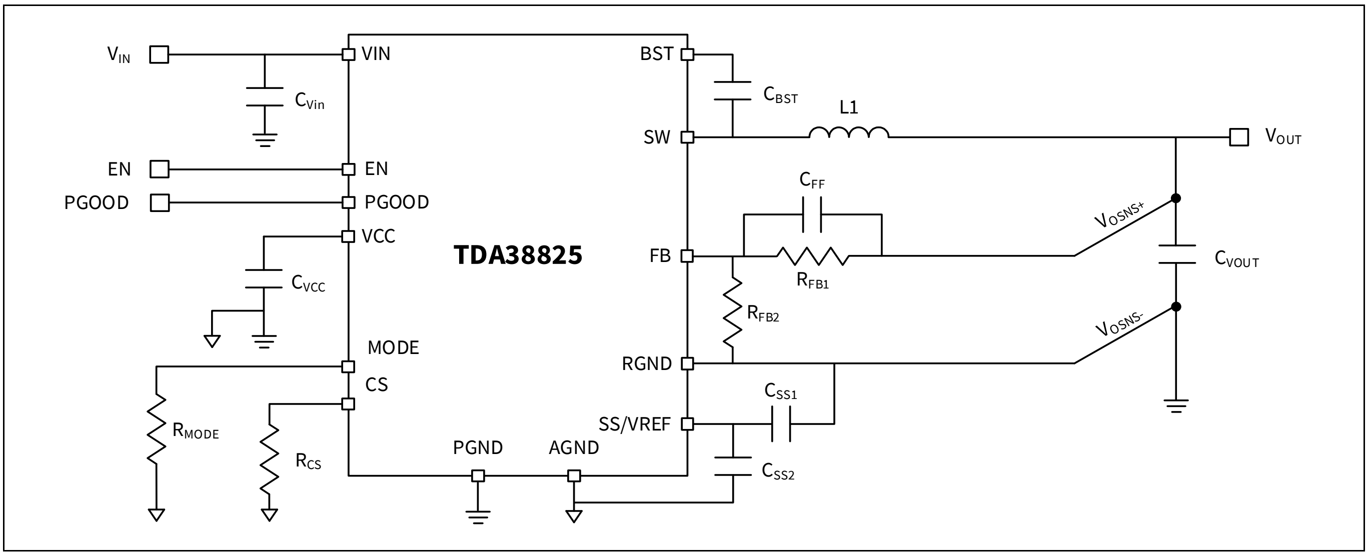


Figure 1 Application diagram of TDA38825

2 Overview

The TDA38825 [2] is a 20 A fully integrated and highly efficient DC-DC buck regulator. It uses a fast Constant On-Time (COT) control scheme, which simplifies the design efforts and achieves fast transient response while maintaining excellent line and load regulation. It can operate over a wide range of input voltages (2.7 V to 16 V) using an external bias supply.

TDA38825 is a versatile regulator, offering switching frequency selectable from 600 kHz, 800 kHz, and 1 MHz, programmable current limit, and soft-start time with a minimum of 1 ms, Forced Continuous Conduction Mode (FCCM) and Diode Emulation Mode (DEM) operation. The TDA38825 supports voltage tracking with an external reference input. It also features important protection functions such as pre-bias start-up, thermally compensated current limit, overvoltage and under voltage protection, and thermal shutdown to give a required system level security in the event of fault conditions. The TDA38825 is available in a standard QFN-21 (3 mm x 4 mm) package and can operate over a wide temperature range (-40°C < Tj < 125°C).

2.1 Specifications

These boards have been configured and optimized for the following operating conditions:

- VIN = 12 V
- VOUT_PRI = +3.3 V, IMAX_PRI = 2 A
- VOUT_SEC1 = +3.3 V, IMAX_SEC1 = 0.5 A
- VOUT_SEC2 = -3.3 V, IMAX_SEC2 = -0.5 A
- Fsw = 600 kHz

3 Schematic

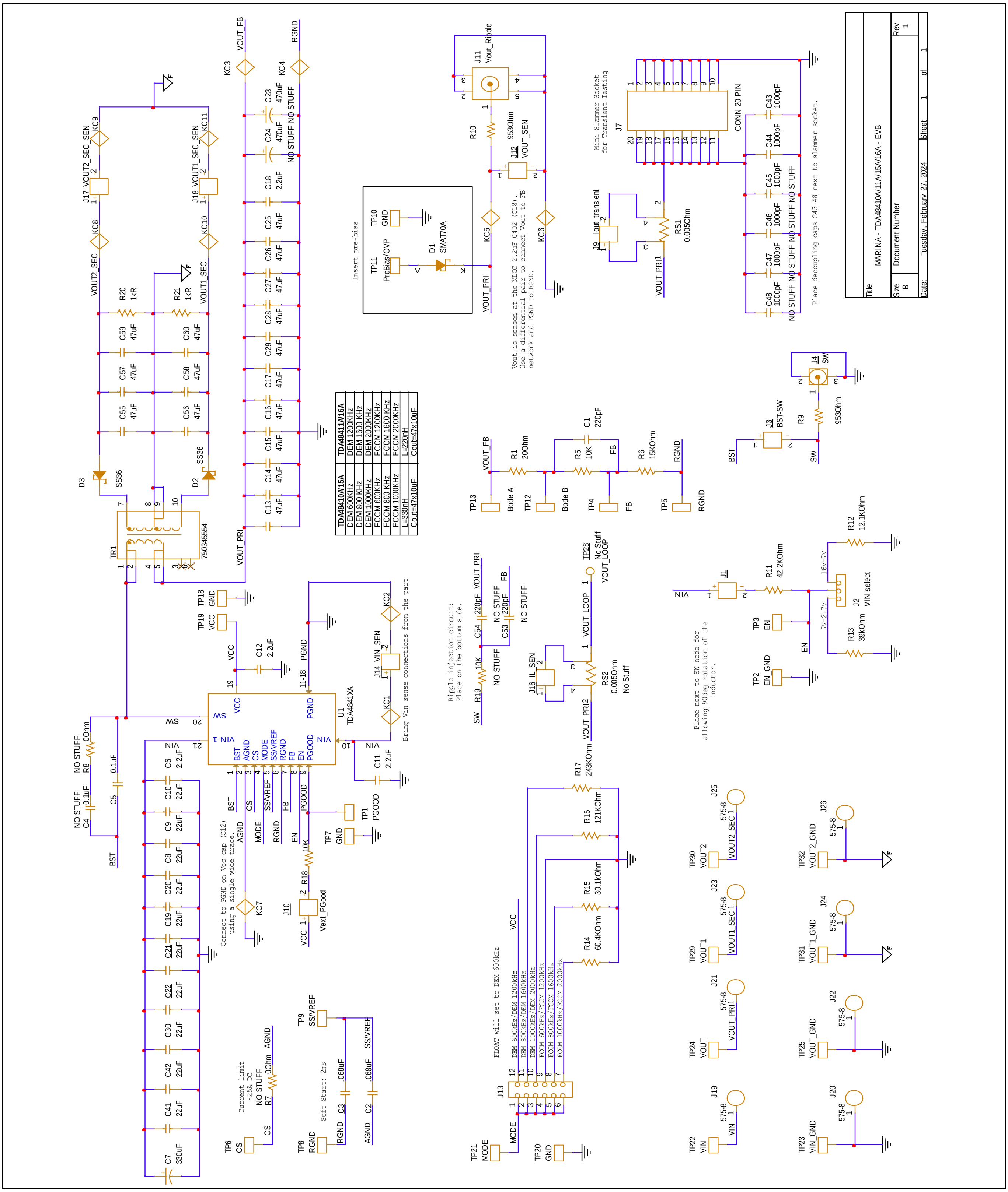


Figure 2 ISO buck schematic diagram

4 ISO buck operation principle

Figure 3 describes the operation principle of the ISO-buck converter. When the high-side MOSFET is turned on, the current flows through the primary winding of the transformer and charges the primary output capacitor. Considering the dot convention of the transformer, the voltage at the anode of the Schottky diode is negative, hence, the diode is reverse-biased and no current flows in the secondary winding. The load connected to the secondary output is supplied by Cout2. When the low-side MOSFET is turned on, the voltage applied at the transformer windings inverts its polarity. Therefore, the Schottky diode is now forward-biased and allows the current to flow from the secondary winding to Cout and the load. Under this condition the energy transfer from primary to secondary side occurs.

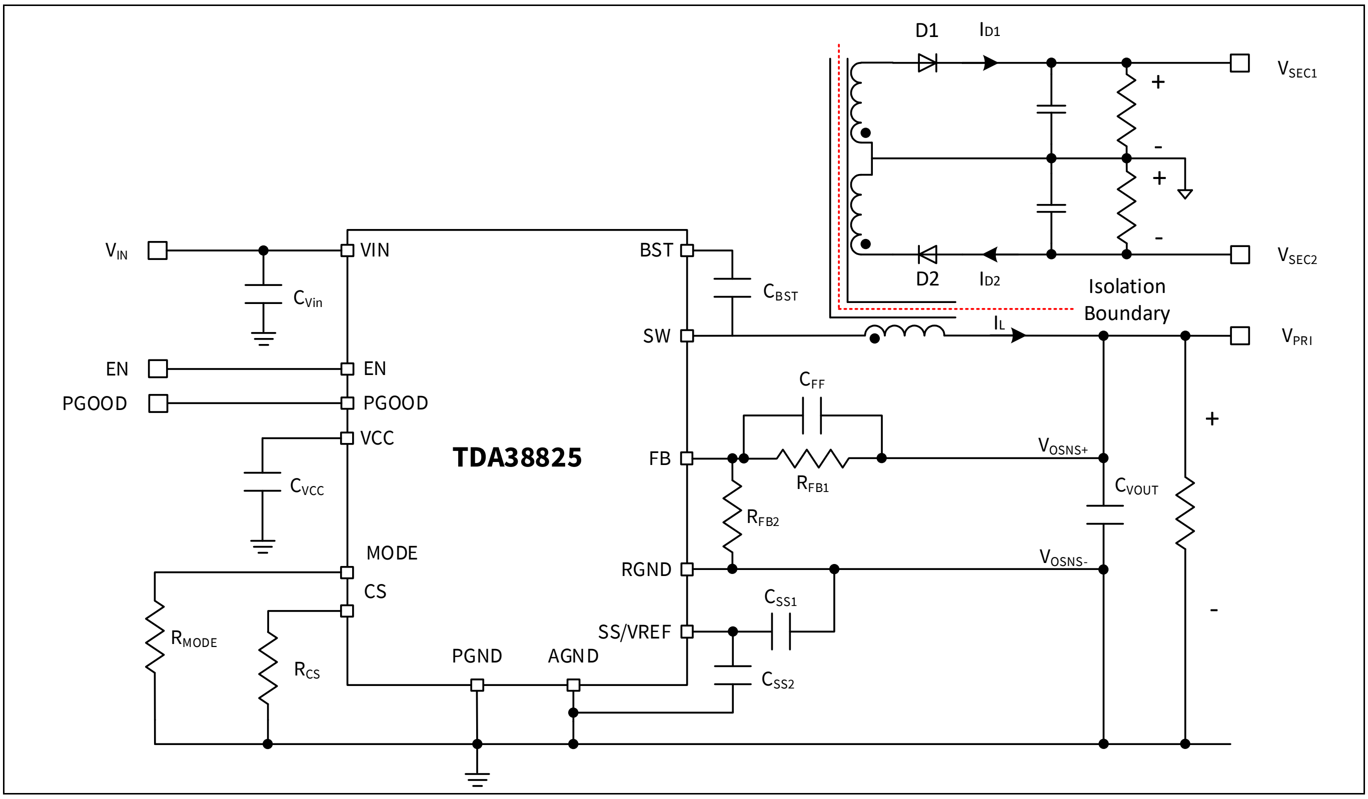


Figure 3 ISO buck application diagram

For a multiple output configuration, the total current of the various outputs reflected to the primary side must be accounted for to make sure the IC is able to handle the resultant current.

The equations for the above circuit are given as:

$$Vpri = D * Vin$$

Equation 1

$$Vsec_1 = N1 * Vpri - Vdiode$$

Equation 2

$$Vsec2 = -(N2 * Vpri - Vdiode)$$

Equation 3

$$\Delta i = (Vin - Vpri)\frac{D}{L*Fsw}$$

Equation 4

$$IDS\_pk = Iout_{pri} + \frac{\Delta i}{2} + \frac{Iout2}{N1} + \frac{Iout3}{N2}$$

Equation 5

Where Vpri is the primary output and Vsec1 and Vsec2 are the positive and negative secondary outputs, respectively, D is the duty cycle, N1 and N2 are the turn ratio of the transformer for Vsec1 and Vsec2, respectively. Vdiode is the forward voltage drop across the diode. IOUT1, IOUT2, and IOUT3 are the output current drawn from Vpri, Vsec1 and Vsec2, respectively, IDS_pk is the peak current through the top switch and Δi is the triangular portion of the primary inductor ripple current.

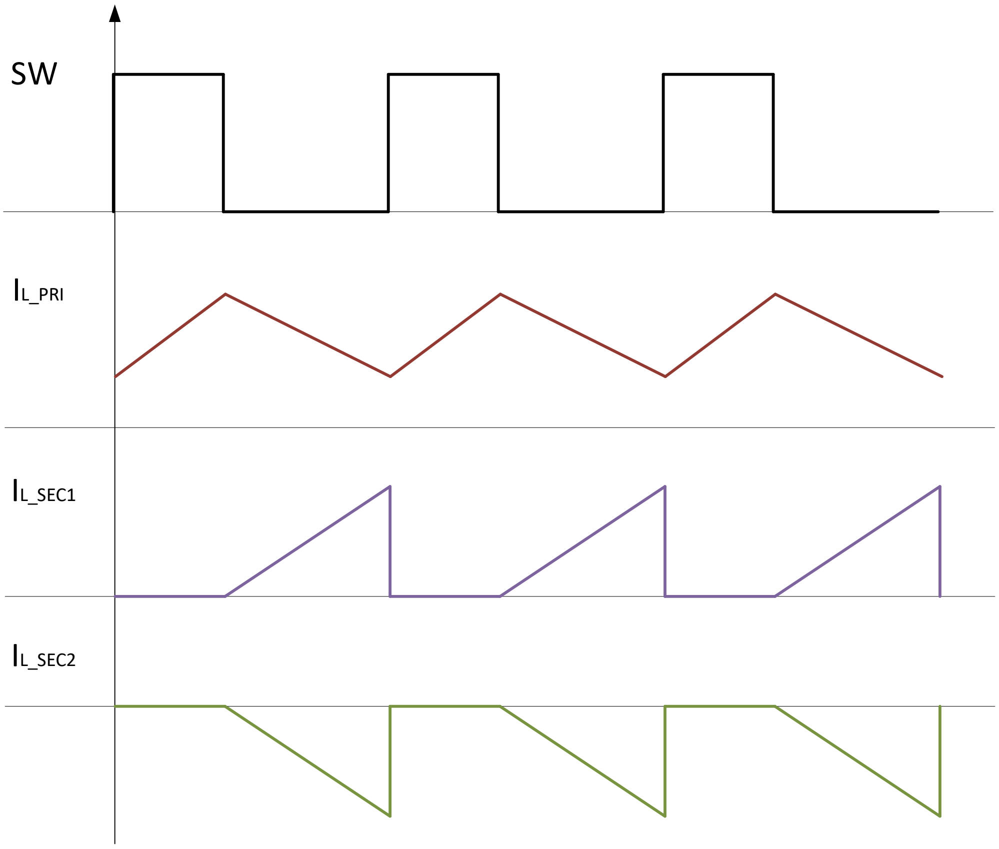


Figure 4 **Primary and secondary winding current**

5 Design of external components

5.1 Input capacitors

The input capacitor, just like in a standard buck, should limit the input voltage ripple. Key parameters of the input capacitor are, together with its value, the maximum operating voltage, and the RMS current capability. The input capacitor voltage rating must be higher than the maximum input operating voltage of the application. During the switching activity, a pulsed current flows into the input capacitor and so its RMS current capability must be selected according to the application conditions. Internal losses of the input filter depend on the ESR value so usually low ESR capacitors (like multilayer ceramic capacitors) have higher RMS current capability. On the other hand, given the RMS current value, a lower ESR input filter has lower losses and so contributes to higher conversion efficiency.

The maximum RMS input current flowing through the capacitor can be calculated as:

$$Irms = \left(Iout_{pri} + \frac{Iout2}{N1} + \frac{Iout3}{N2} \right) * \sqrt{\left(1 - \frac{D}{\eta}\right) * \frac{D}{\eta}}$$

Equation 6

Typically, CIN is dimensioned to keep the maximum peak-to-peak voltage across the input filter in the order of 5 percent of VINmax.

5.2 Transformer selection

The transformer has two essential tasks:

- Providing the isolation between primary and secondary sides in accordance with the application requirements
- Generating the necessary secondary output voltage from the regulated primary voltage with the most suitable turn ratio

The transformer selection implies defining the following parameters:

- Isolation voltage
- Turn ratio
- Primary inductance
- Peak and RMS currents
- Windings resistance
- Leakage inductance
- Parasitic capacitances

5.2.1 Selection of primary inductor

The inductor is selected based on output power, operating frequency, and efficiency requirements. A low inductor value results in a large ripple current, lower efficiency, and high output noise, but helps with size reduction and transient load response. Generally, the desired peak-to-peak ripple current in the inductor (Δi) is found between 20 percent and 50 percent of the output current.

The inductor saturation current must be higher than the maximum spec of the OCP limit plus the peak-to-peak inductor ripple current. For some core materials, inductor saturation current may decrease with increasing temperature. It is important to check the inductor saturation current at the maximum operating temperature.

The inductor value for the desired operating ripple current can be determined using the following relations:

$$L = (V_{in} - V_{out\_pri}) \times \frac{D_{min}}{\Delta i_{L(\max)} \times F_{sw}}$$

Equation 7

$$D_{min} = \frac{V_o}{V_{in(\max)}}$$

Equation 8

$$I_{sat} \geq OCP_{max} + \Delta i_{L(\max)}$$

Equation 9

Where: VIN = Maximum input voltage; ΔiLmax = Maximum peak-to-peak inductor ripple current; OCPmax = maximum spec of the OCP limit as defined in TDA38825; and Isat = inductor saturation current.

In this case, select the inductor to achieve ΔiLmax = 20 percent of maximum current of TDA38825, which is 20 A.

$$L = (12 - 3.3) \times \frac{0.275}{4 \times 600 * 10\hat{}3}$$

Equation 10

$$L = 1\ uH$$

Equation 11

Transformer parameters:

The transformer is obtained from Würth Elektronik after customizing it for 1 uH inductance value. Table 1 shows the parameters and Figure 5 shows the footprint and winding structure of the transformer.

Table 1 **Transformer parameters**

Transformer parameters	Test conditions	Values
DC Resistance (1-5)	Tie (1+2,4+5), at 20°C	15 mohms
DC Resistance (7-8)	Tie (8+9), @20°C	30 mohms
DC Resistance (8-10)	Tie (8+9), @20°C	30 mohms
Inductance (1-5)	Tie (1+2,4+5),10kHz, 100mV, Ls	1 uH +-20%
Saturation Current (1-5)	Tie (1+2,4+5), 30% rolloff from initial	25 A
Leakage Inductance (1-5)	Tie (1+2,4+5,7+8+9+10),100kHz, 100mV, Ls	0.5 uH
DIELECTRIC (1-10)	Tie (1+2,8+9), 1000VAC, 1 second	–
TURNS Ratio	(7-8):(1-5), tie(8+9,1+2,4+5)	1.13:1
TURNS Ratio	(7-8):(8-10), tie(8+9	1.00:1

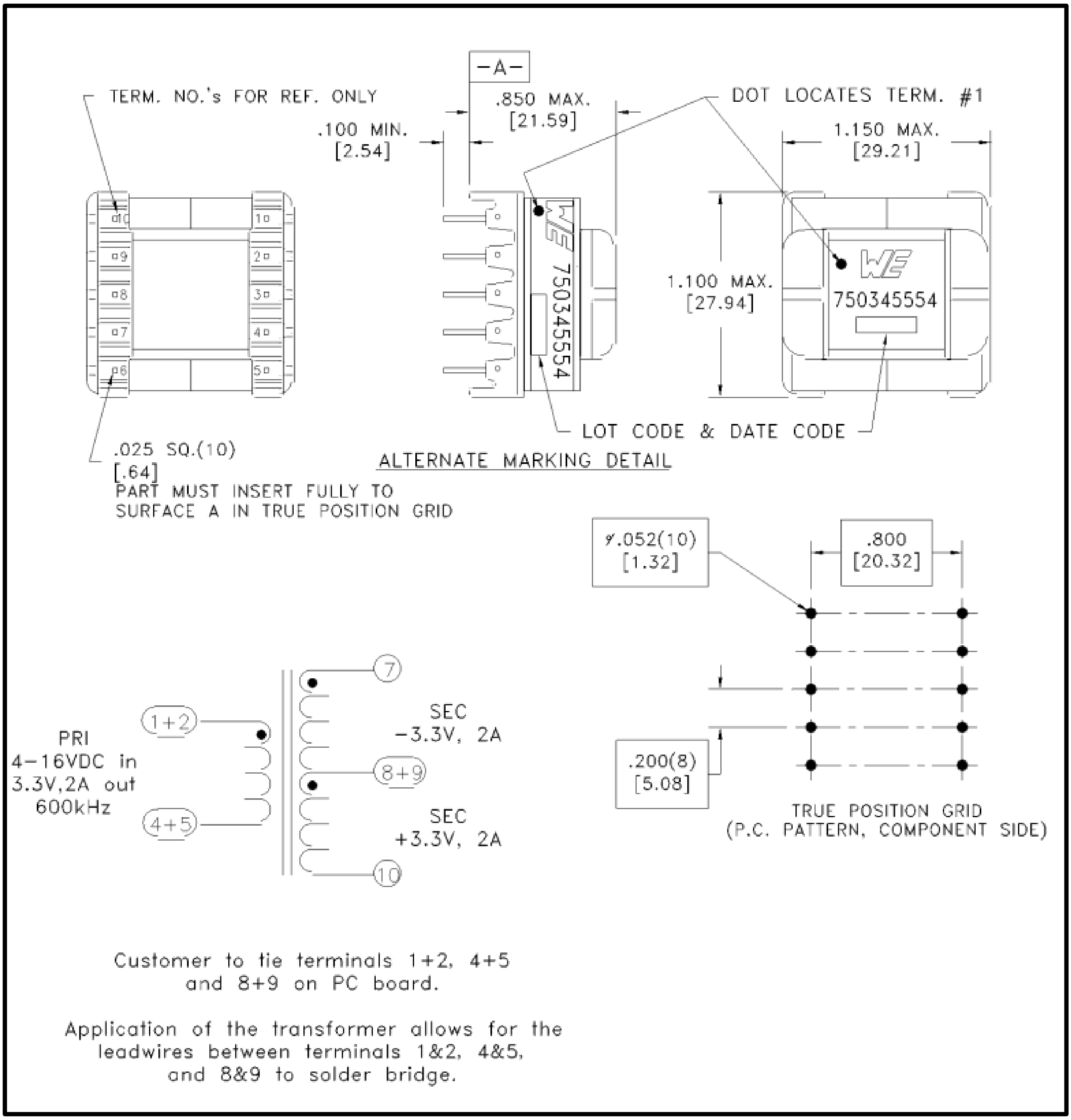


Figure 5 Transformer package and layout

5.3 Schottky diode selection

The selection of the Schottky diode should consider the following parameters:

- Maximum forward current, mainly defined by the secondary output current demand
- Forward voltage drop, which affects the secondary output voltage regulation
- Maximum peak reverse voltage. During the on-phase of the primary side, when in the secondary side no current flows, the diode is reverse biased and must withstand this voltage
- Junction capacitance, which should be as low as possible to reduce the ringing

5.4 Output capacitor selection

Primary output capacitor

As in a standard buck converter, the primary output capacitor is involved in:

- Determining the output voltage ripple
- Supporting load transient
- The loop stability, by setting one pole and one zero in the transfer function Considering the output voltage ripple requirement, the primary output capacitance should be selected according to the following equation

To satisfy the Vo ripple requirement, Co should satisfy the following criterion:

$$\boxed{C_o > \frac{\Delta i_{Lmax}}{8 \times \Delta V_{or} \times f_{sw}}}$$

Equation 12

Where ΔV_{or} is the desired peak-to-peak output ripple voltage. The ESR and ESL of the output capacitors, as well as the parasitic resistance or inductance due to PCB layout, can also contribute to the output voltage ripple. It is suggested to use multi-layer ceramic capacitor (MLCC) for their low ESR, ESL, and small size.

To meet the transient response requirements, the output capacitors should also meet the following criteria:

$$\boxed{C_o > \frac{L \times \Delta I_{o(\max)}^2}{2 \times \Delta V_{oL} \times V_o}}$$

Equation 13

Where ΔV_{OL} is the allowable Vo deviation during the load transient. $\Delta I_{o(max)}$ is the maximum step load current.

Secondary output capacitor:

The secondary output capacitor supplies the secondary output load current during the tON (when diode D1 is reverse biased) and its value defines the secondary output voltage ripple (ΔV_{OUT2}).

$$\boxed{C_{o\_sec} > \frac{Iout2 * D}{\Delta V_{out2} \times f_{sw}}}$$

Equation 14

5.5 Primary output voltage

The output voltage can be programmed with an external voltage divider. The FB voltage is compared to an internal reference voltage of 0.6 V. The divider ratio is set to provide 0.6 V at the FB pin when the output is at its desired value. The calculation of the feedback resistor divider is shown below.

$$V_o = V_{ref} \times (1 + \frac{R_{FB1}}{R_{FB2}})$$

Equation 15

Where R_{FB1} and R_{FB2} are the top and bottom feedback resistors, select R_{FB1} = 10 kΩ and R_{FB2} = 10 kΩ, to achieve V_o = 1.2 V. The same resistor divider can be used at the VSNS pin to achieve the same voltage scaling factor.

5.6 Secondary output voltage

The secondary output voltage is calculated as:

$$Vsec_1 = N1 * Vpri - Vdiode$$

Equation 16

$$Vsec2 = -(N2 * Vpri - Vdiode)$$

Equation 17

Where, N1 = N2 = 1.13, Vpri = 3.3 V, Vdiode = 0.4 V

$Vsec_1$ = (1.13*3.3)-0.4 = 3.33 V

Similarly, Vsec2 = -3.33 V

6 Typical operating waveforms

- Vin = 12 V, L = 1000 nH, Fsw = 600 kHz FCCM
- Vout_pri = 3.3 V, Iout_pri = 2 A
- Vout_sec1 = 3.3 V, Iout_sec1 = 0.5 A
- Vout_sec2 = -3.3 V, Iout_sec2 = 0.5 A

6.1 Efficiency

6.1.1 Efficiency for Vout_pri

- Vout_pri = 3.3 V, Iout_pri = 0-2 A
- Vout_sec1 = 3.3 V, No Load
- Vout_sec2 = -3.3 V, No Load

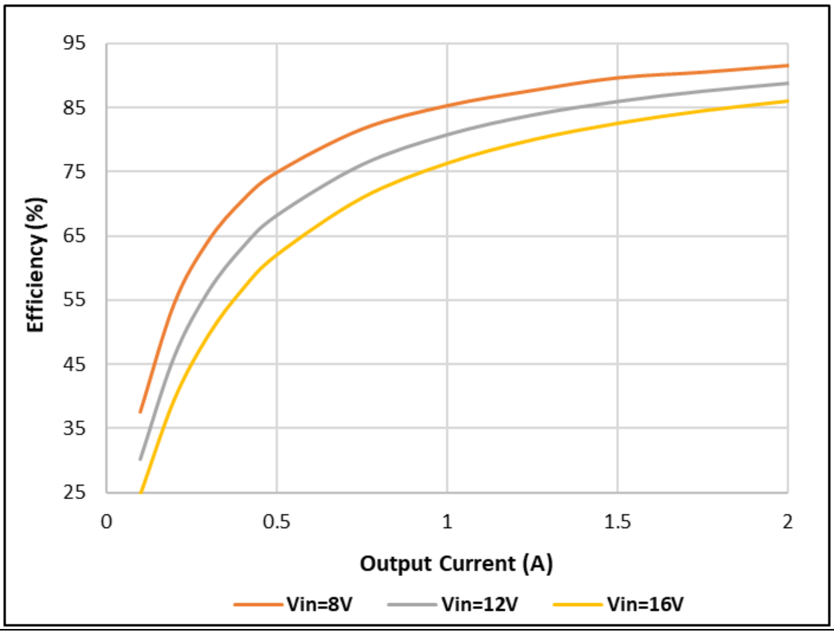


Figure 6 Efficiency for Vout_pri at different input voltage

6.1.2 Efficiency for Vout_sec1

Vout_sec1 = 3.3 V, Iout_sec2 = 0-0.5 A

Vout_pri = 3.3 V, No Load

Vout_sec2 = -3.3 V, No Load

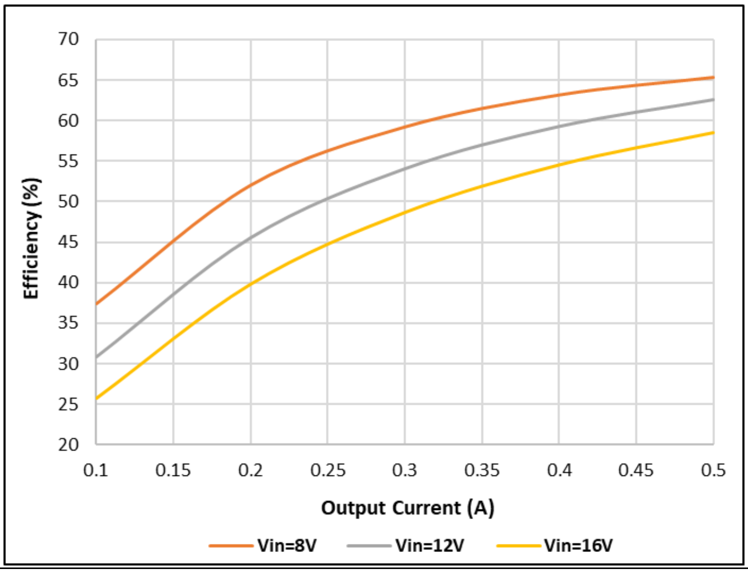


Figure 7 Efficiency for Vout_sec1 at different input voltage

6.1.3 Efficiency for Vout_sec2

- Vout_sec2 = -3.3 V, Iout_sec2 = 0-0.5 A
- Vout_pri = 3.3 V, No Load
- Vout_sec1 = 3.3 V, No Load

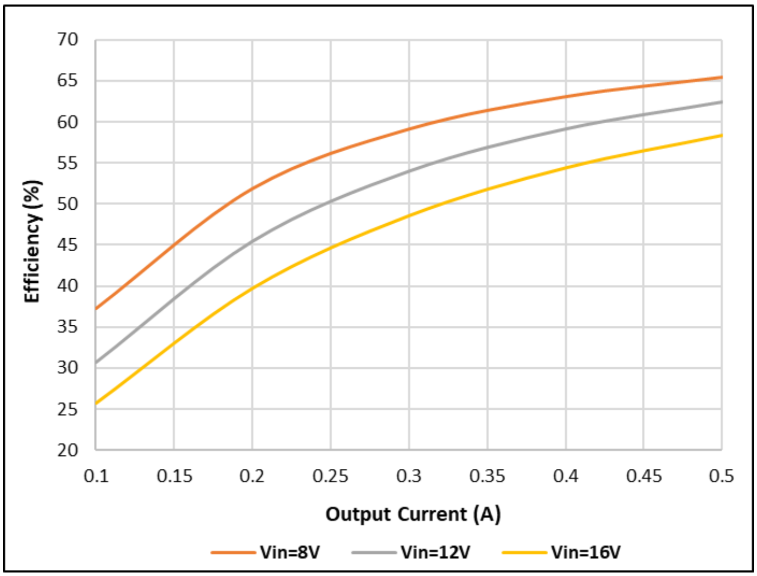


Figure 8 Efficiency for Vout_sec2 at different input voltage

6.2 Load regulation

6.2.1 Vout_pri regulation vs Iout_pri

- Vout_pri = 3.3 V, Iout_pri = 0-2 A
- Vout_sec1 = 3.3 V, No Load
- Vout_sec2 = -3.3 V, No Load

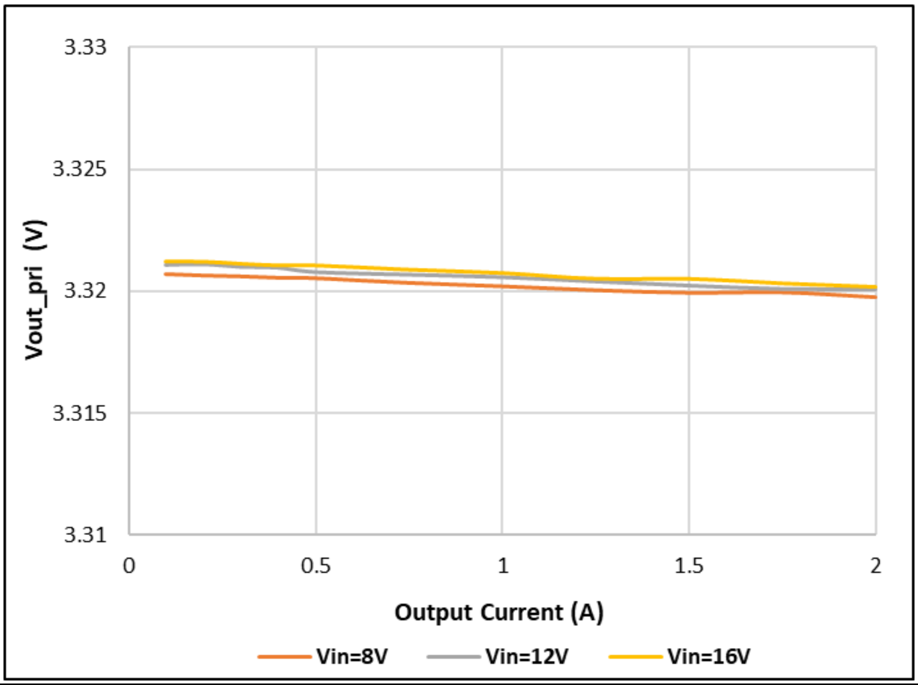


Figure 9 Vout_pri regulation vs Iout_pri

6.2.2 Vout_sec1 regulation vs Iout_sec1

- Vout_sec1 = 3.8 V, Iout_sec1 = 0-0.5 A
- Vout_pri = 3.3 V, No Load
- Vout_sec2 = -3.3 V, No Load

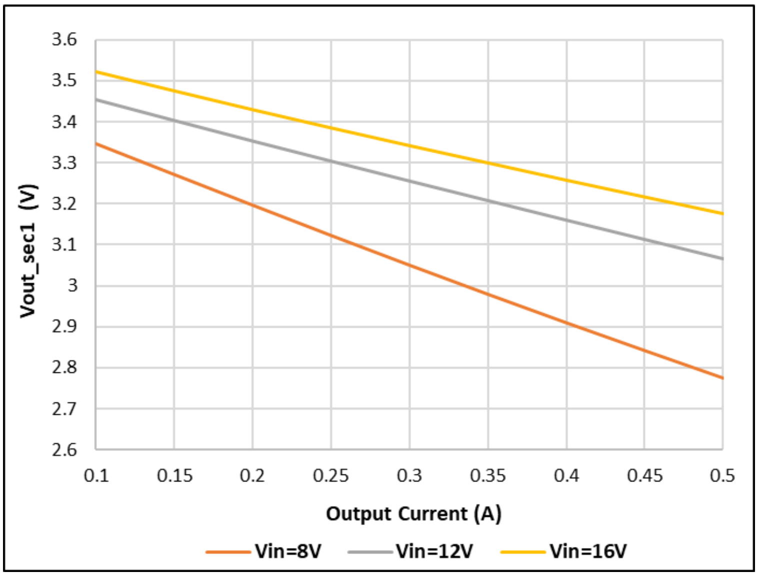


Figure 10 Vout_sec1 regulation vs Iout_sec1

6.2.3 Vout_sec2 regulation vs Iout_sec2

- Vout_sec2 = -3.3 V, Iout_sec2 = 0-0.5 A
- Vout_pri = 3.3 V, No Load
- Vout_sec2 = 3.3 V, No Load

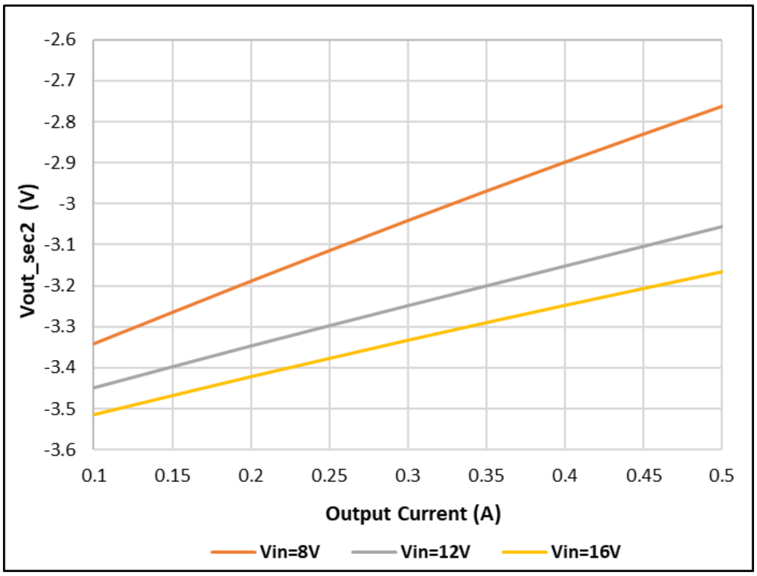


Figure 11 Vout_sec2 regulation vs Iout_sec2

6.2.4 Vout_sec1 regulation vs Vin

- Vout_sec1 = 3.3 V, Iout_sec1 = 0-0.5 A
- Vout_pri = 3.3 V, No Load
- Vout_sec2 = -3.3 V, No Load

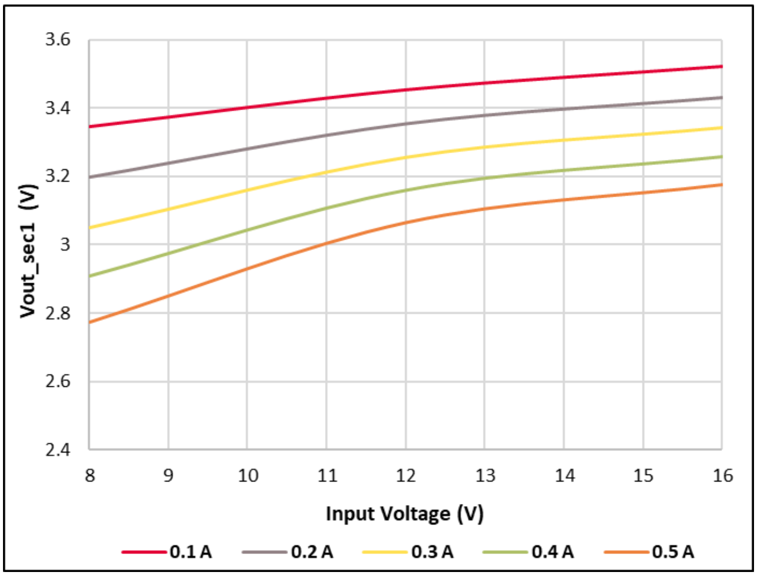


Figure 12 Vout_sec1 regulation vs Vin

6.2.5 Vout_sec2 regulation vs Vin

- Vout_sec2 = -3.3 V, Iout_sec2 = 0-0.5 A
- Vout_pri = 3.3 V, No Load
- Vout_sec2 = 3.3 V, No Load

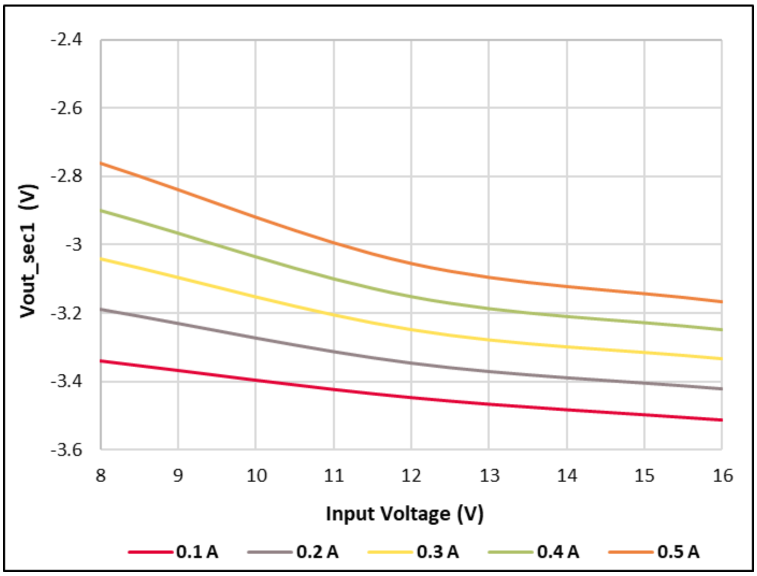


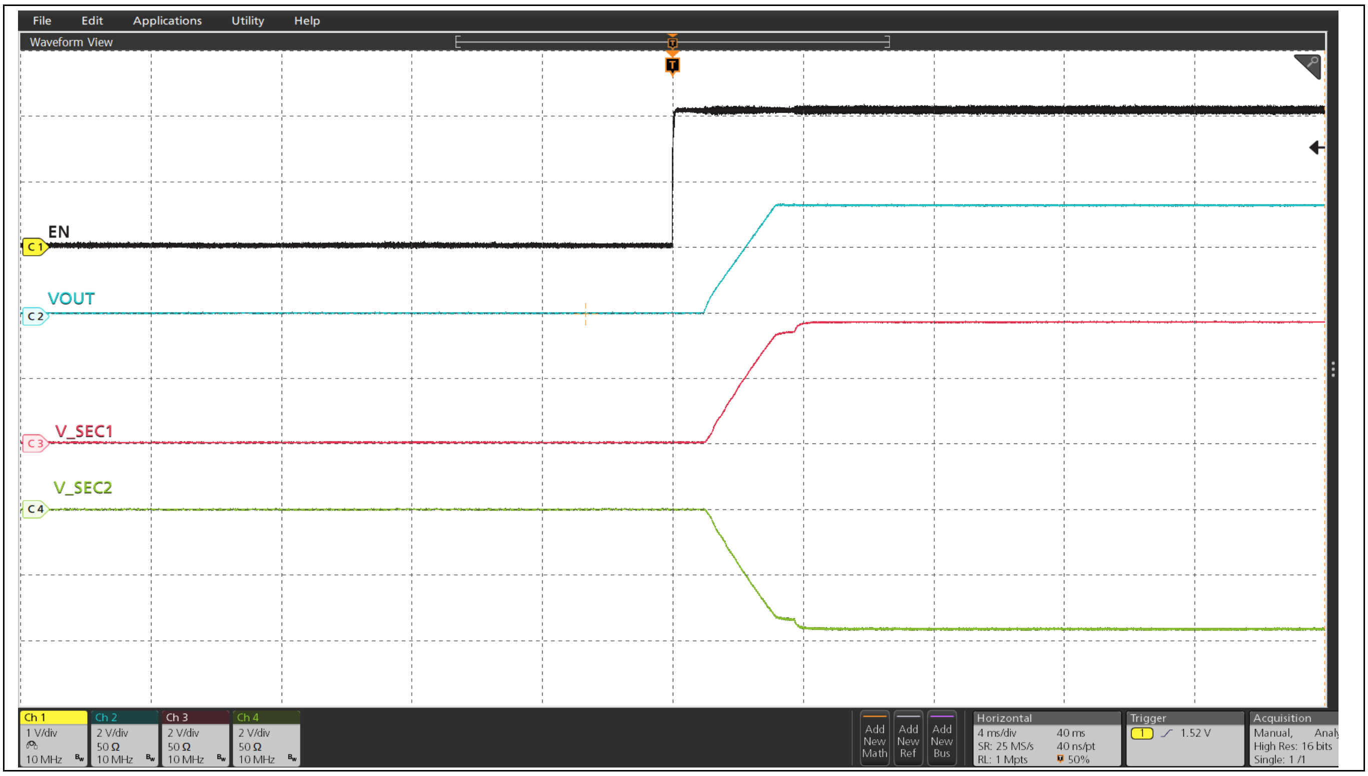
Figure 13 Vout_sec2 regulation vs Vin

6.3 Start-up

- Vout_pri = 3.3 V, No Load
- Vout_sec1 = 3.3 V, No Load
- Vout_sec2 = -3.3 V, No Load

Oscilloscope:

- Channel 1: Enable
- Channel 2: Vout_pri
- Channel 3: Vout_sec1
- Channel 4: Vout_sec2



Ch 1: 1 V/div, 10 MHz
Ch 2: 2 V/div, 50 Ω, 10 MHz
Ch 3: 2 V/div, 50 Ω, 10 MHz
Ch 4: 2 V/div, 50 Ω, 10 MHz
Horizontal: 4 ms/div, 40 ms, SR: 25 MS/s, 40 ns/pt, RL: 1 Mpts, 50%
Trigger: 1, 1.52 V
Acquisition: Manual, Analy, High Res: 16 bits, Single: 1 /1

Figure 14 Start-up by enable

6.4 Shutdown

- Vout_pri = 3.3 V, No Load
- Vout_sec1 = 3.3 V, No Load
- Vout_sec2 = -3.3 V, No Load

Oscilloscope:

- Channel 1: Enable
- Channel 2: Vout_pri
- Channel 3: Vout_sec1
- Channel 4: Vout_sec2

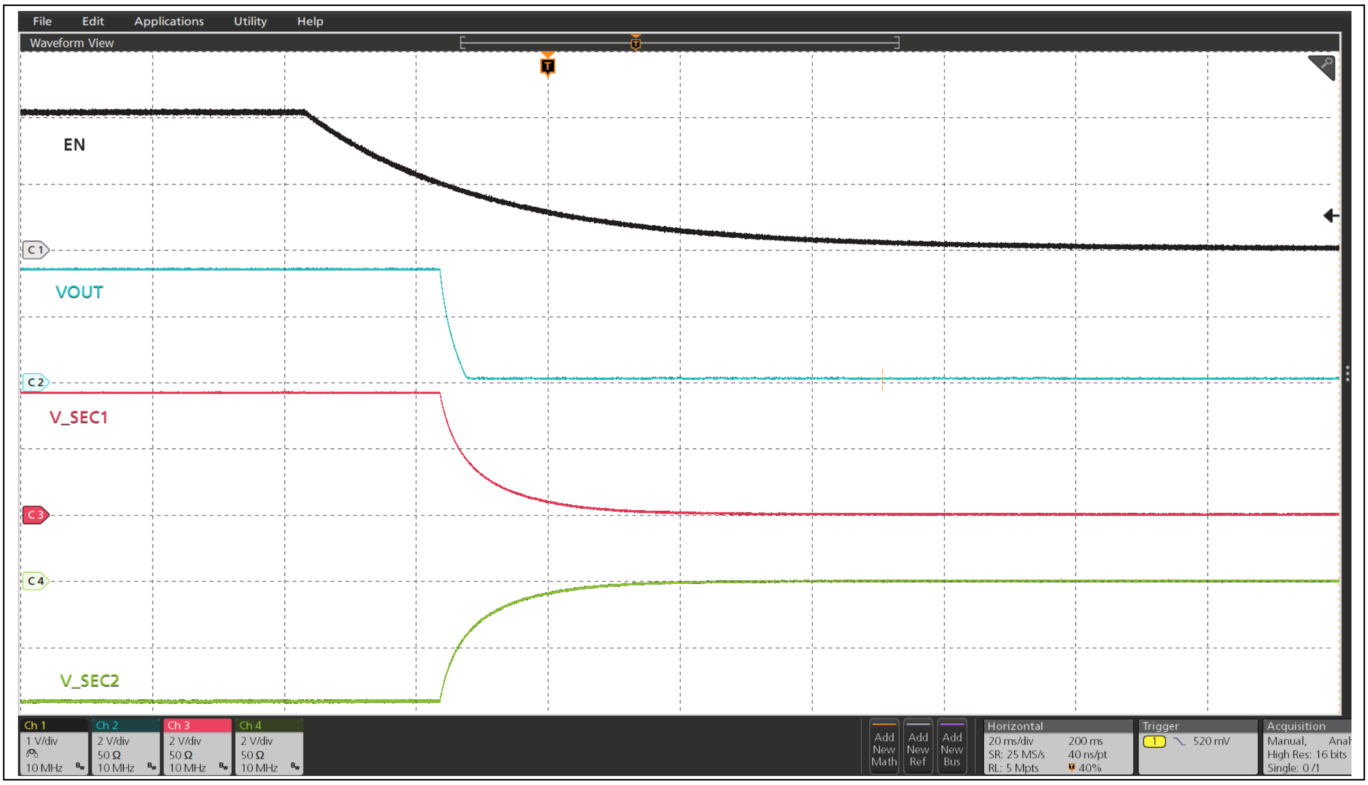


Figure 15 Shutdown by enable

6.5 Start-up with load

- Vout_pri = 3.3 V, 2 A
- Vout_sec1 = 3.3 V, 0.5 A
- Vout_sec2 = -3.3 V, 0.5 A

Oscilloscope:

- Channel 1: Enable
- Channel 2: Vout_pri
- Channel 3: Vout_sec1
- Channel 4: Vout_sec2

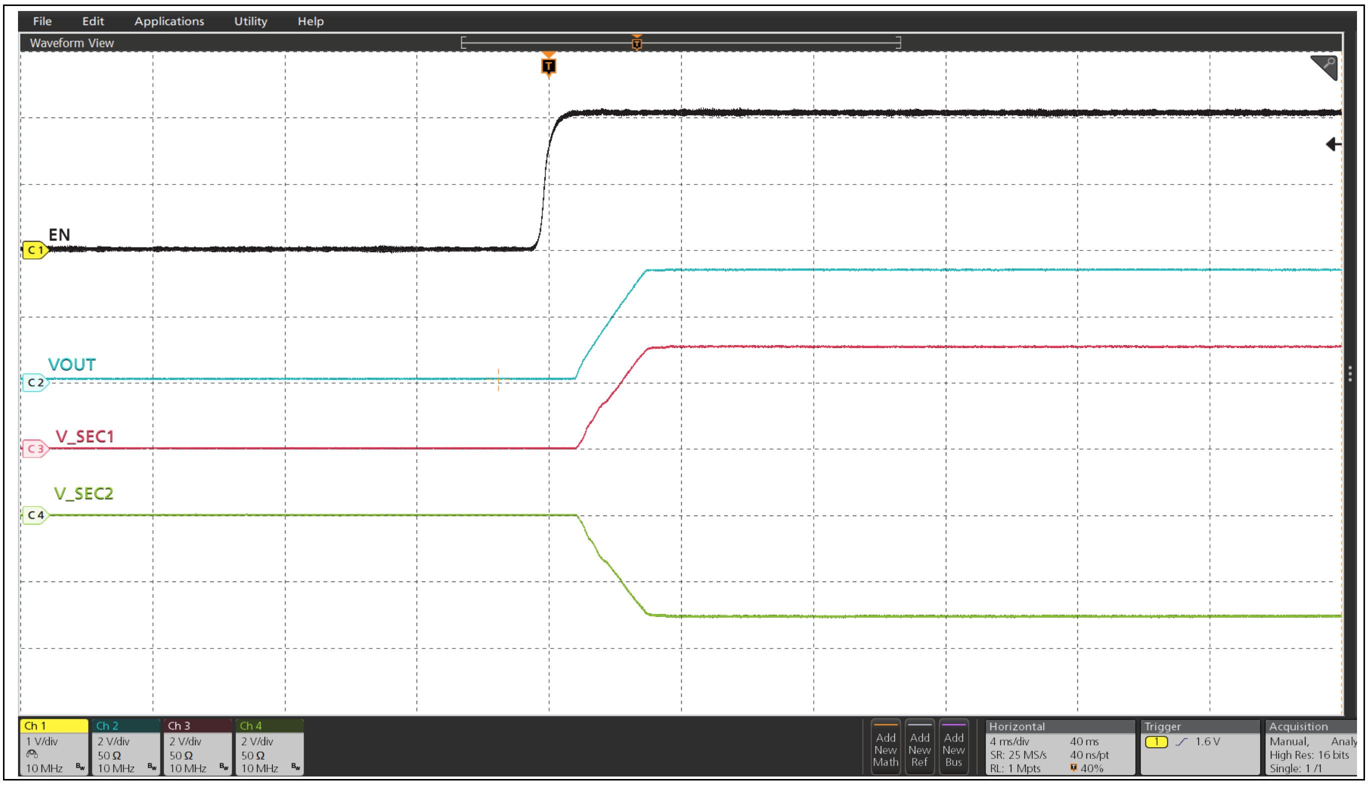


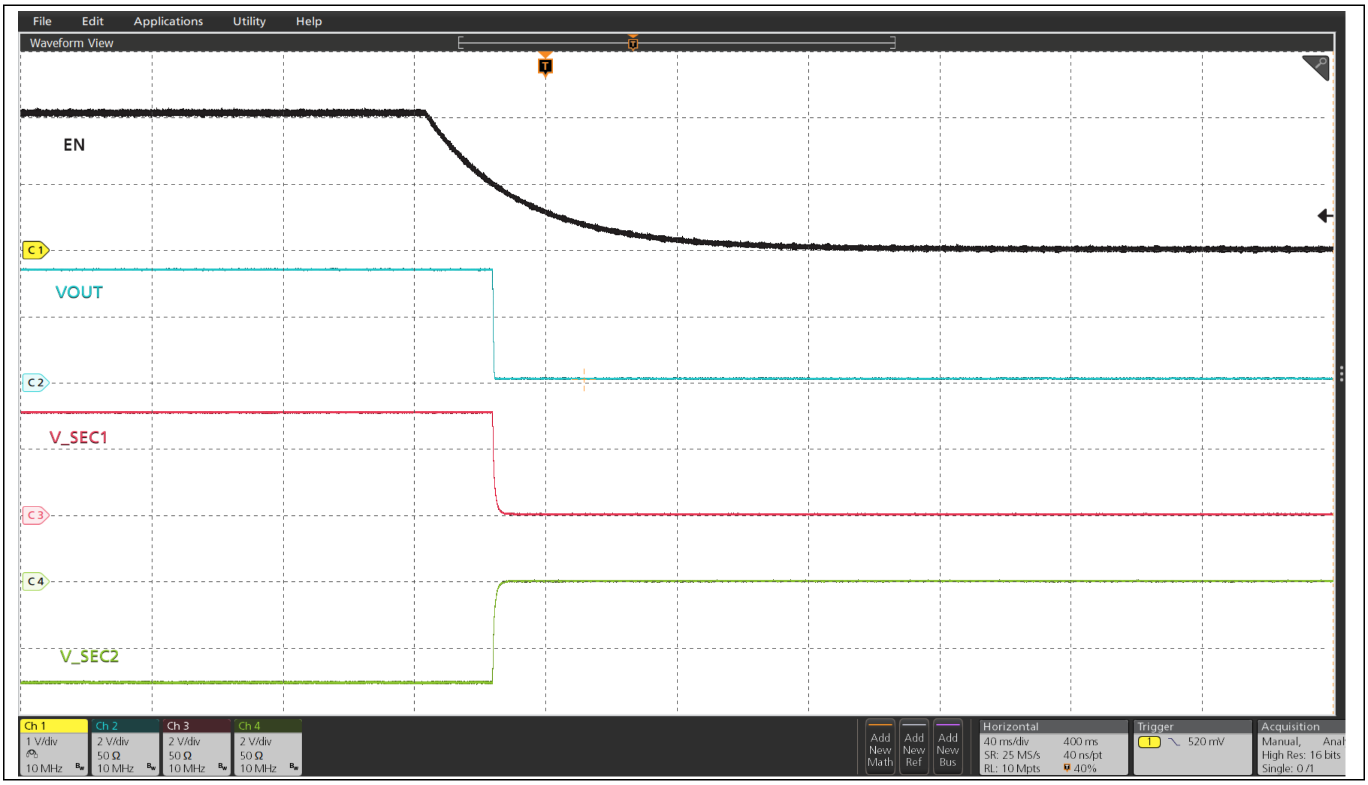
Figure 16 Start-up by enable

6.6 Shutdown with load

- Vout_pri = 3.3 V, 2 A
- Vout_sec1 = 3.3 V, 0.5 A
- Vout_sec2 = -3.3 V, 0.5 A

Oscilloscope:

- Channel 1: Enable
- Channel 2: Vout_pri
- Channel 3: Vout_sec1
- Channel 4: Vout_sec2



Ch 1: 1 V/div, 10 MHz
Ch 2: 2 V/div, 50 Ω, 10 MHz
Ch 3: 2 V/div, 50 Ω, 10 MHz
Ch 4: 2 V/div, 50 Ω, 10 MHz
Horizontal: 40 ms/div, 400 ms, SR: 25 MS/s, 40 ns/pt, RL: 10 Mpts, 40%
Trigger: 1, 520 mV
Acquisition: Manual, High Res: 16 bits, Single: 0/1

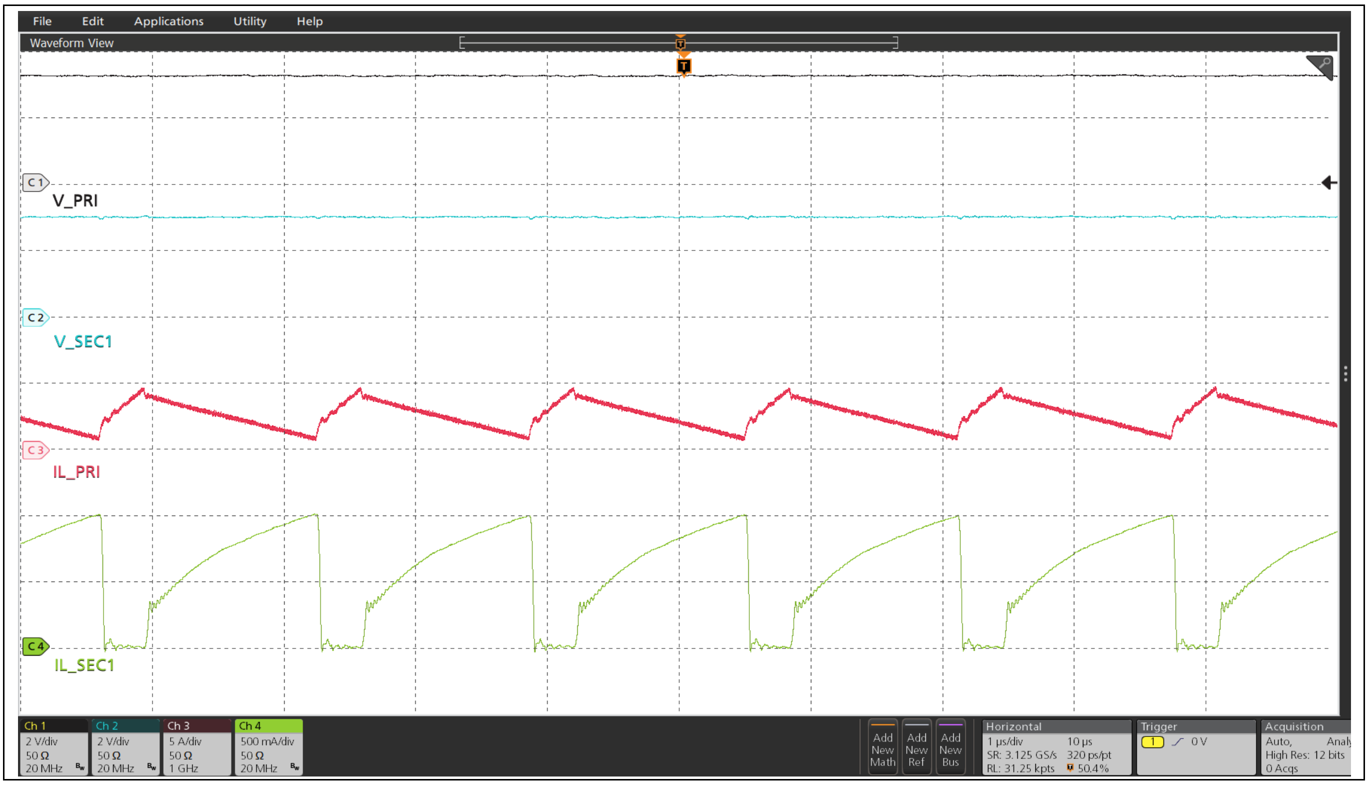
Figure 17 **Shutdown by enable**

6.7 Current waveform at steady state

- Vout_pri = 3.3 V, 2 A
- Vout_sec1 = 3.3 V, 0.5 A
- Vout_sec2 = -3.3 V, 0.5 A

Oscilloscope:

- Channel 1: Vout_pri
- Channel 2: Vout_sec1
- Channel 3: Primary inductor current
- Channel 4: Secondary1 inductor current



Ch 1: 2 V/div, 50 Ω, 20 MHz
Ch 2: 2 V/div, 50 Ω, 20 MHz
Ch 3: 5 A/div, 50 Ω, 1 GHz
Ch 4: 500 mA/div, 50 Ω, 20 MHz

Horizontal: 1 µs/div, 10 µs, SR: 3.125 GS/s, 320 ps/pt, RL: 31.25 kpts, 50.4%

Trigger: 1, 0 V

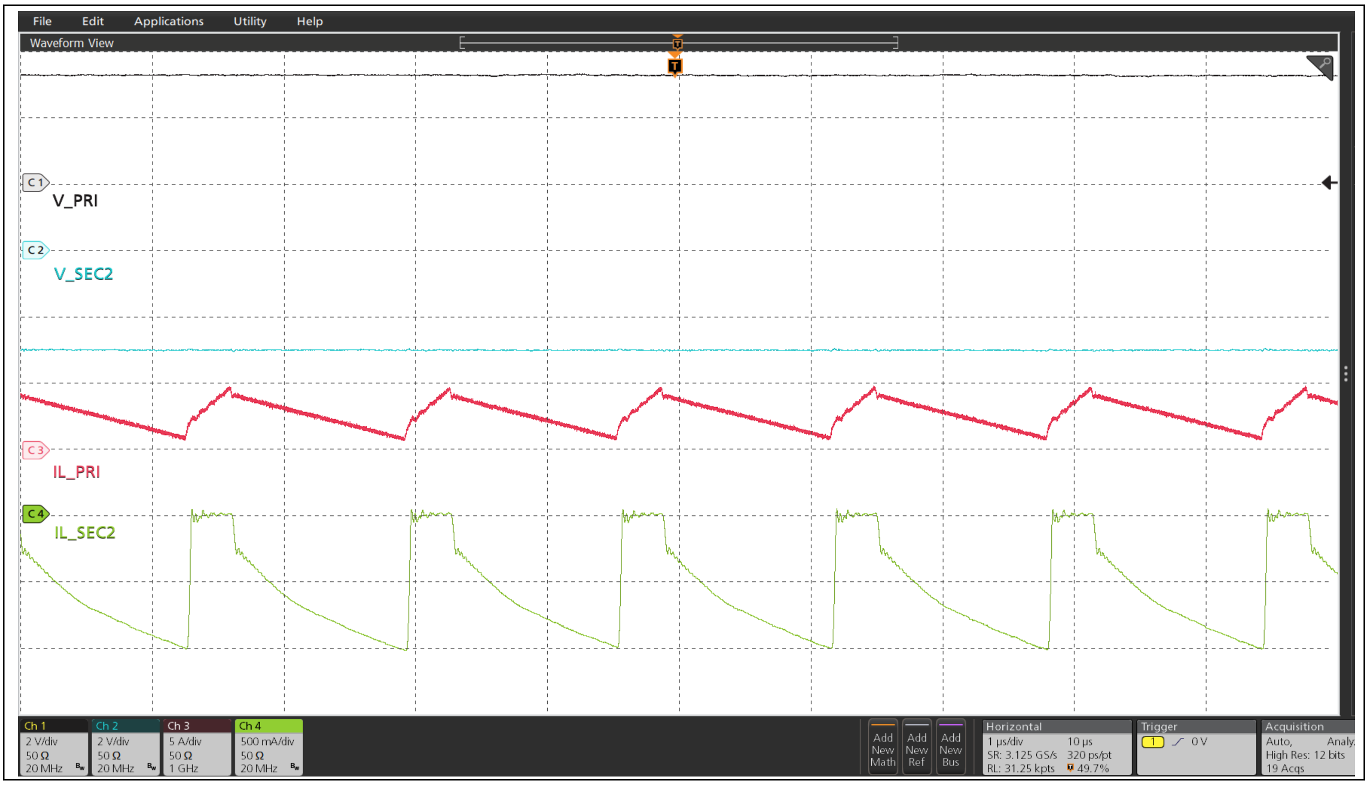
Acquisition: Auto, Anal, High Res: 12 bits, 0 Acqs

Figure 18 Primary and secondary1 inductor current and at steady state

- Vout_pri = 3.3 V, 2 A
- Vout_sec1 = 3.3 V, 0.5 A
- Vout_sec2 = -3.3 V, 0.5 A

Oscilloscope:

- Channel 1: Vout_pri
- Channel 2: Vout_sec2
- Channel 3: Primary inductor current
- Channel 4: Secondary2 inductor current



Ch 1
2 V/div
50 Ω
20 MHz

Ch 2
2 V/div
50 Ω
20 MHz

Ch 3
5 A/div
50 Ω
1 GHz

Ch 4
500 mA/div
50 Ω
20 MHz

Horizontal
1 µs/div 10 µs
SR: 3.125 GS/s 320 ps/pt
RL: 31.25 kpts 49.7%

Trigger
1 0 V

Acquisition
Auto, Analy
High Res: 12 bits
19 Acqs

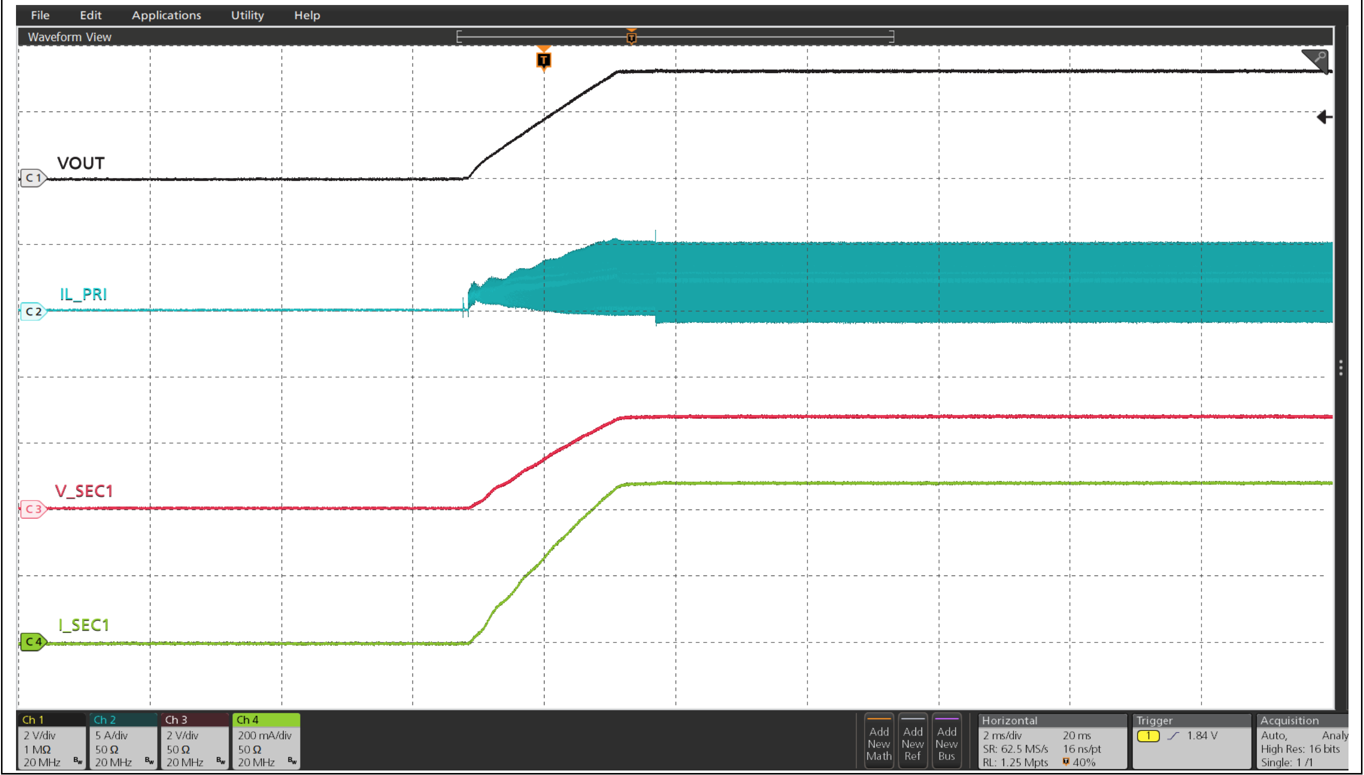
Figure 19 Primary and secondary2 inductor current at steady state

6.8 Current waveform at start-up

- Vout_pri = 3.3 V, 2 A
- Vout_sec1 = 3.3 V, 0.5 A
- Vout_sec2 = -3.3 V, 0.5 A

Oscilloscope:

- Channel 1: Vout_pri
- Channel 2: Primary inductor current
- Channel 3: Vout_sec1
- Channel 4: Iout_sec1



Ch 1
2 V/div
1 MΩ
20 MHz

Ch 2
5 A/div
50 Ω
20 MHz

Ch 3
2 V/div
50 Ω
20 MHz

Ch 4
200 mA/div
50 Ω
20 MHz

Horizontal
2 ms/div 20 ms
SR: 62.5 MS/s 16 ns/pt
RL: 1.25 Mpts 40%

Trigger
1 1.84 V

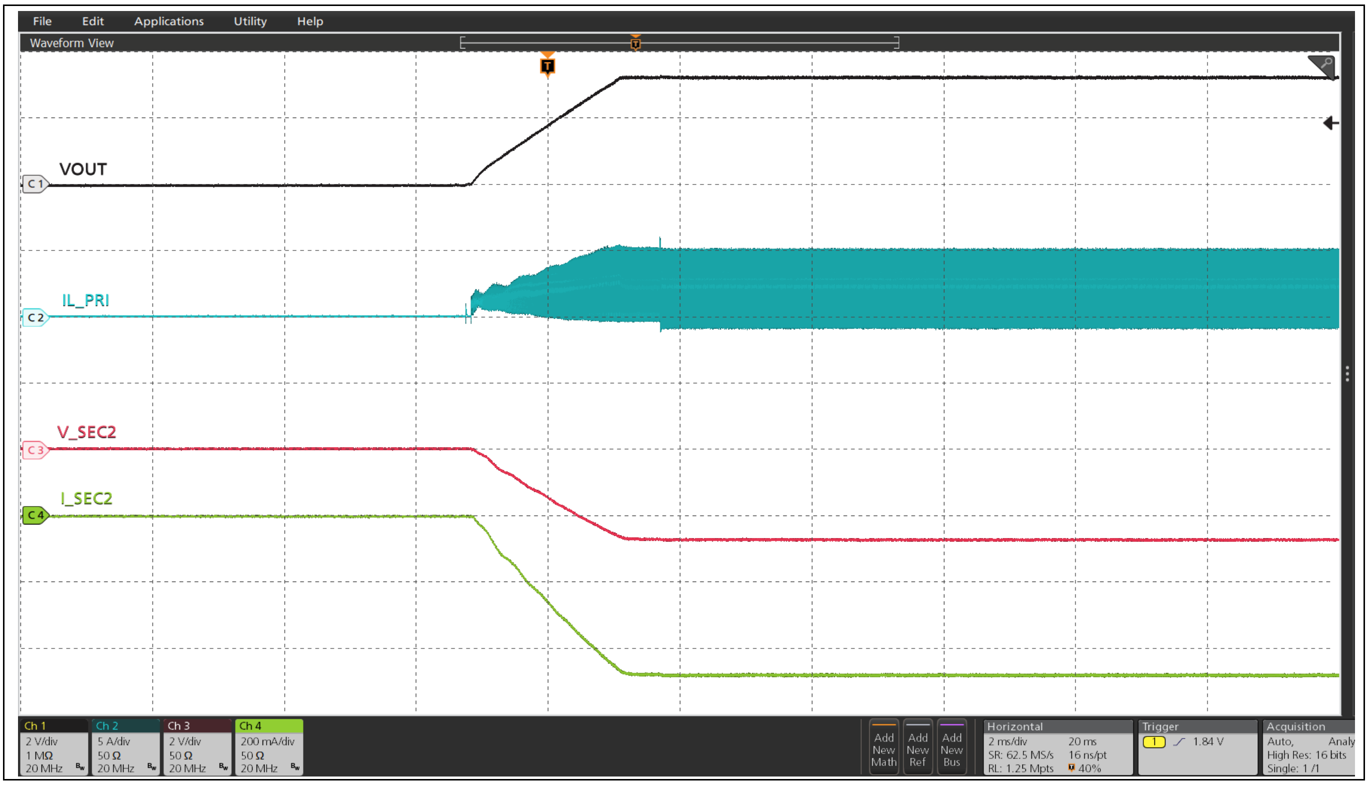
Acquisition
Auto, Analy
High Res: 16 bits
Single: 1 /1

Figure 20 Primary inductor current and Iout_sec1 waveform at start-up

- Vout_pri = 3.3 V, 2 A
- Vout_sec1 = 3.3 V, 0.5 A
- Vout_sec2 = -3.3 V, 0.5 A

Oscilloscope:

- Channel 1: Vout_pri
- Channel 2: Primary inductor current
- Channel 3: Vout_sec2
- Channel 4: Iout_sec2



Ch 1
2 V/div
1 MΩ
20 MHz

Ch 2
5 A/div
50 Ω
20 MHz

Ch 3
2 V/div
50 Ω
20 MHz

Ch 4
200 mA/div
50 Ω
20 MHz

Horizontal
2 ms/div 20 ms
SR: 62.5 MS/s 16 ns/pt
RL: 1.25 Mpts 40%

Trigger
1 1.84 V

Acquisition
Auto, Analy
High Res: 16 bits
Single: 1 /1

Figure 21 Primary inductor current and Iout_sec2 waveform at start-up

References

[1] Infineon Technologies AG: *Introduction of fast COT*; Available online

[2] Infineon Technologies AG: *TDA38825 Datasheet*; Available online

Revision history

Document revision	Date	Description of changes
1.0	2024-07-11	Initial release

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