Introduction to Simulation Model – Infineon Designer

MOTIX™ MCU embedded power TLE988x/9x

About this document

Scope and purpose

This document outlines the main features of MOTIX™ MCU embedded power IC TLE988x/9x by means of its digital twin. The digital twin is the simulation model. In typical application setups, the simulation model aims to be an easy, time-efficient, and cost-effective solution for exploring device capabilities and integration into complex applications.

Information covered in this document does not substitute datasheet content and shall be regarded as complementary to it. For more information on the device and its features, refer to the datasheet[1] and the user manual[2].

Intended audience

This application note, along with the simulation model itself, offers an interactive solution targeted at anybody who aims to explore the functionality and "what-if" scenarios for the TLE988x/9x device.

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1 MOTIX™ MCU embedded power TLE988x/9x

The products in this product family offer the following features to enable you to optimize your system with our MOTIX™ MCU:

- Bridge drivers with a current controlled output stage,
- Flexible charge- and discharge current settings
- Several diagnostic functions

The highly integrated products in the TLE988x/9x product family save space and energy, improve the overall system reliability through advanced diagnosis features and reduce the overall cost due to a minimum number of components. They perfectly fit with a range of motor control applications where a small package format and a minimum number of external components are essential. Such applications include window lift, sunroof, wiper, auxiliary pumps, HVAC fans, and engine cooling fan.

The available online circuits are listed below:

- 3-phase motor – 12 V Automotive motor control for auxiliary drives - MOTIX™ Embedded Power ICs TLE988x/9x

Click here to open the circuits.

2 Simulation model features

The simulation model enables you to:

- Perform transient simulations: observe and analyze the transient device response to different stimuli. The number of stimuli and probes is unlimited
- Measure the device's electrical parameters in typical conditions with increased precision at small resolution (for example 100 ns/1 µV/1 µA)
- Integrate the simulation model in a complex application and explore new possibilities
- Obtain results in the shortest time possible at zero error cost, without harm to physical components. The simulation can also be run by anyone, such as engineers and students without risk of damage
- Explore the main features of the real device:
    - Bridge driver including adaptive gate current control
    - Charge pump
    - Current sense amplifier

To keep the usability and simulation speed in a reasonable range, the simulation model does not cover all features of the real device:

- Current consumption of the IC is not considered (a realistic power efficiency calculation is not possible)
- There is no simulation capability for ESD, EMC, AC, DC, and no Monte Carlo analysis
- There are possible convergence issues for using DC sources, steep ramps, or high-frequency sources within the setup
- The simulation model has the following limitations:
    - Thermal network and self-heating are not available, and there is no overtemperature detection or protection
    - No fault management
    - No internal clock generation
    - No supply supervision

2.1 Details on the implementation

The 6 inputs INAx and INBx controlling each of the MOSFETs are controlled by ideal 0 V-5 V voltage sources. Due dead time between low-side and high-side switching is considered either externally from input stimuli or internally if the external time is less than specified value in the DRV_CCP_TIMESEL register. It is possible to test the fail safe mechanism via the FI input pin. A value of 1 V enables the driver while a value of 0 disables all gate drivers.

All internal communication registers have been emulated via the model parameters which are available for user control on the test bench. The value of each parameter must be specified directly in decimal value corresponding to the binary value of the corresponding register, from 0 to maximum bit size. Values outside this interval will be ignored. For a complete list of parameters, refer to Table 1 below. For more information, refer to the product datasheet [1] and user manual [2].

Important: To ensure the correct functioning of the bridge driver, you must set the simulation maximum time step to a maximum value depending on the register configuration. For middle range values of model parameters, a typical maximum time step can be set to 200 ns. The application included in the package takes approximatively 3.5 minutes for each ms of transient simulation, with all 3 phases active.

Table 1 Model parameter list

Parameter name	Description	Bit size and range
f_{CP_CLK}	f_{SYS} clock frequency	5 MHz to 40 MHz
$f_{CP\_DITH\_UPPER}$	low charge pump frequency dithering: 64 {10 00000} to 95 {10 11111}	7-bit (64 to 95)
$f_{CP\_DITH\_LOWER}$	high charge pump frequency dithering: 64 {10 00000} to 95 {10 11111}	7-bit (64 to 95)
R_{IN}	CSA input resistance	Typ. 1.3 kΩ
gain_sel	CSA differential gain	10, 20, 40, 60
offs_sel	CSA output offset	2-bit (0 to 3)
CP_STG_AUTO	single-stage or 2-stage mode: 0 -> 2-stage, 1 -> automatic	1-bit (0 or 1)
LS_I1ON	Low-side sequencer phase 1 and constant switch-on current	6-bit (0 to 63)
LS_I2ON	Low-side sequencer phase 2 and constant switch-on current	6-bit (0 to 63)
LS_I3ON	Low-side sequencer phase 3 and constant switch-on current	6-bit (0 to 63)
LS_I4ON	Low-side sequencer phase 4 and constant switch-on current	6-bit (0 to 63)
LS_T1ON	Low-side sequencer phase 1 and constant switch-on time	8-bit (0 to 255)
LS_T2ON	Low-side sequencer phase 2 and constant switch-on time	6-bit (0 to 63)
LS_T3ON	Low-side sequencer phase 3 and constant switch-on time	6-bit (0 to 63)
LS_T4ON	Low-side sequencer phase 4 and constant switch-on time	6-bit (0 to 63)
HS_I1ON	High-side sequencer phase 1 and constant switch-on current	6-bit (0 to 63)
HS_I2ON	High-side sequencer phase 3 and constant switch-on current	6-bit (0 to 63)
HS_I3ON	High-side sequencer phase 4 and constant switch-on current	6-bit (0 to 63)
HS_I4ON	High-side sequencer phase 4 and constant switch-on current	6-bit (0 to 63)
HS_T1ON	High-side sequencer phase 1 and constant switch-on time	8-bit (0 to 255)
HS_T2ON	High-side sequencer phase 2 and constant switch-on time	6-bit (0 to 63)
HS_T3ON	High-side sequencer phase 3 and constant switch-on time	6-bit (0 to 63)

Parameter name	Description	Bit size and range
HS_T4ON	High-side sequencer phase 4 and constant switch-on time	6-bit (0 to 63)
ICLMPON	Current clamping for on state current	6-bit (0 to 63)
LS_I1OFF	Low-side sequencer phase 1 and constant switch-off current	6-bit (0 to 63)
LS_I2OFF	Low-side sequencer phase 2 and constant switch-off current	6-bit (0 to 63)
LS_I3OFF	Low-side sequencer phase 3 and constant switch-off current	6-bit (0 to 63)
HS_I1OFF	High-side sequencer phase 1 and constant switch-off current	6-bit (0 to 63)
HS_I2OFF	High-side sequencer phase 2 and constant switch-off current	6-bit (0 to 63)
HS_I3OFF	High-side sequencer phase 3 and constant switch-off current	6-bit (0 to 63)
I_{4OFF}	Sequencer phase 4 switch-off current all half-bridges	6-bit (0 to 63)
LS_T1OFF	Low-side sequencer phase 1 and constant switch-off time	8-bit (0 to 255)
LS_T2OFF	Low-side sequencer phase 2 and constant switch-off time	6-bit (0 to 63)
LS_T3OFF	Low-side sequencer phase 3 and constant switch-off time	6-bit (0 to 63)
HS_T1OFF	High-side sequencer phase 1 and constant switch-off time	8-bit (0 to 255)
HS_T2OFF	High-side sequencer phase 2 and constant switch-off time	6-bit (0 to 63)
HS_T3OFF	High-side sequencer phase 3 and constant switch-off time	6-bit (0 to 63)
T4OFF	Sequencer phase 4 switch-off time all half-bridges	6-bit (0 to 63)
$I_{CLMPOFF}$	Current clamping for off state current	6-bit (0 to 63)
DRV_CCP_TIMESEL	Minimum cross-conduction protection time	3-bit (0 to 7)
LS_IAFOFF	Low-side active free-wheeling switch-off current	6-bit (0 to 63)
LS_IAFON	Low-side active free-wheeling switch-on current	6-bit (0 to 63)
LS_TAFOFF	Low-side active free-wheeling switch-off time	8-bit (0 to 255)
LS_TAFON	Low-side active free-wheeling switch-on time	8-bit (0 to 255)
HS_IAFOFF	High-side active free-wheeling switch-off current	6-bit (0 to 63)
HS_IAFON	High-side active free-wheeling switch-on current	6-bit (0 to 63)
HS_TAFOFF	High-side active free-wheeling switch-off time	8-bit (0 to 255)
HS_TAFON	High-side active free-wheeling switch-on time	8-bit (0 to 255)
HS_T1OFFADDDLY	High-side adaptive sequencer additional delay	4-bit (0 to 15)
LS_T1OFFADDDLY	Low-side adaptive sequencer additional delay	4-bit (0 to 15)

Parameter name	Description	Bit size and range
HB1_SEQCNF	Half bridge 1 sequencer switch-on and off configuration	1-bit (0 constant, 1 SEQ)
HB2_SEQCNF	Half bridge 2 sequencer switch-on and off configuration	1-bit (0 constant, 1 SEQ)
HB3_SEQCNF	Half bridge 3 sequencer switch-on and off configuration	1-bit (0 constant, 1 SEQ)
HB1ASM_EN	Half bridge 1 adaptive sequencer switch-on and off	1-bit (0 disable, 1enable)
HB2ASM_EN	Half bridge 2 adaptive sequencer switch-on and off	1-bit (0 disable, 1enable)
HB3ASM_EN	Half bridge 3 adaptive sequencer switch-on and off	1-bit (0 disable, 1enable)

3 Model performance

3.1 3-phase motor – transient

This test bench shows a proposal for 3-phase motor bridge driver. All half-bridges are connected in a star configuration and drive a motor emulated with a resistor-inductor equivalent circuit. Each MOSFET is switched on and off at a frequency of 20 kHz and a duty cycle of 40%. Each phase of one complete PWM pulse takes 3 ms. During this time, each half bridge is switched 20 pulses one after the other in a complete rotation.

All half-bridges are configured to operate in sequencer mode with adaptive control enabled.

The sources programmed to produce this pattern is depicted in Figure 1. Load emulation is visible in Figure 2. Simulation results including input stimuli, gate currents, and inductor current are visible in Figure 3.

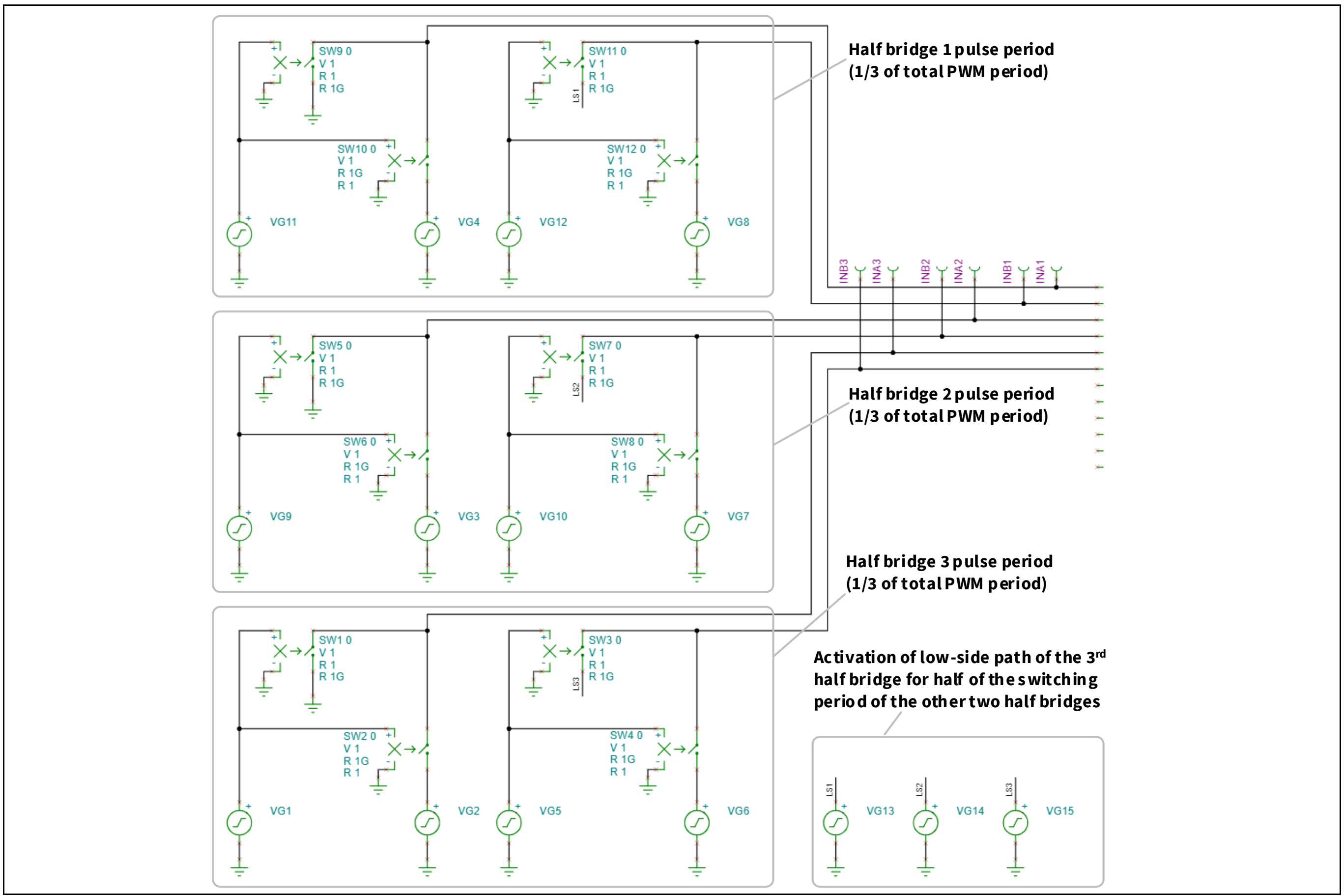

Figure 1 Input stimuli

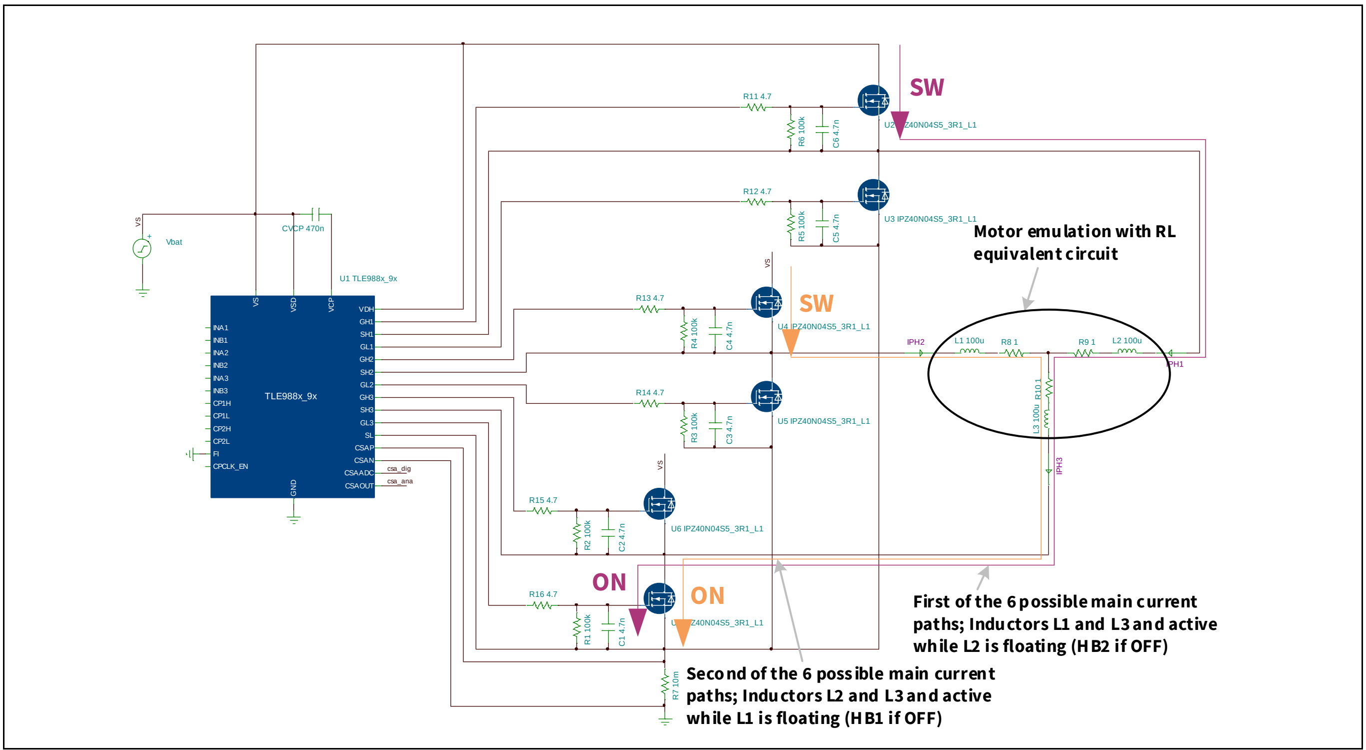

Figure 2 Test setup 3-phase load configuration [click to open]

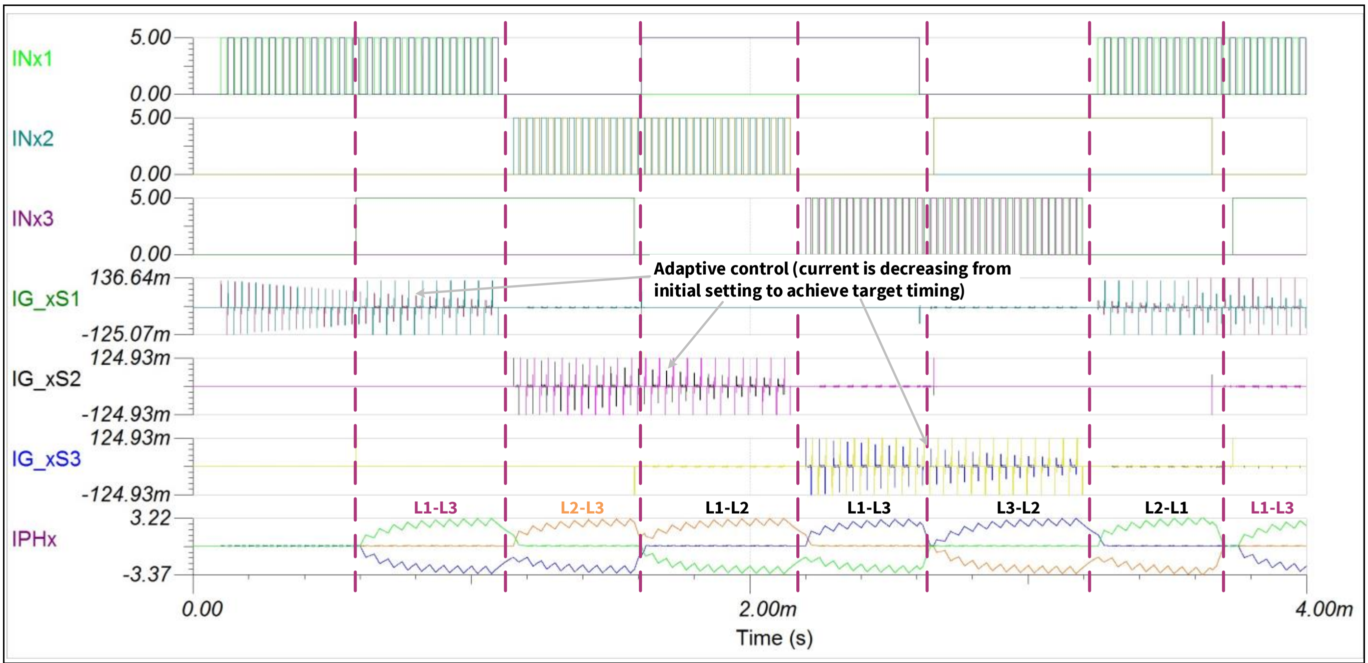

Figure 3 Simulation results 3-phase motor

4 List of references

[1] Datasheet: https://www.infineon.com/dgdl/Infineon-TLE988x_9x_DataSheet-DataSheet-v01_10-EN.pdf?fileId=8ac78c8c8823155701882e60aa3a4f50

[2] Product User Manual: https://www.infineon.com/dgdl/Infineon-TLE988x_9x_Firmware_User_Manual-UserManual-v01_00-EN.pdf?fileId=8ac78c8c8823155701884e06350d1e9d

5 Revision history

Document version	Date of release	Description of changes
Rev.1.00	2023-11-16	Initial version

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