1200 V CoolSiC™ MOSFET: Trench technology essentials

About this document

Scope and purpose

The benefits of wide bandgap silicon carbide (SiC) semiconductors arise from their higher breakthrough electric field, larger thermal conductivity, higher electron-saturation velocity, and lower intrinsic carrier concentration compared to silicon (Si). Based on these advantages of the SiC material, SiC MOSFETs are becoming an attractive switching transistor for high-power applications, such as solar inverters and electric vehicles (EV) chargers. This application note introduces the CoolSiC™ trench MOSFET, describing the SiC MOSFET's products, characteristics, gate-oxide reliability, and application designs. The general features of the CoolSiC™ MOSFET and applications that can help design power systems effectively using a novel transistor are also described.

For more information on the latest chip generations, please read the respective application notes.

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems who would like to get an introduction to CoolSiC™ 1200 V SiC MOSFET.

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1 Infineon 1200 V SiC Trench CoolSiC™ MOSFET

Silicon carbide (SiC) as a compound semiconductor material is formed by silicon (Si) and carbon (C). Currently, 4H–SiC is preferred for power devices, primarily because of its high carrier mobility, particularly in the vertical c-axis direction.

Table 1 summarizes the differences between the physical properties of Si and SiC [1]. As a rule of thumb, SiC has ten times the electric breakthrough field, allowing for thinner epitaxial layers to support high-blocking voltage in power devices. For example, a 4500 V power device would require only a 40 µm to 50 µm drift layer, as opposed to almost 500 µm in the case of silicon. The thinner and more highly doped drift layer leads to much lower drift resistance and thus, to low forward voltage and low conduction loss, while maintaining the high blocking voltage. Secondly, SiC thermal conductivity amounts to 3.7 W/cm/K allowing for more efficient thermal management. With a high electric breakthrough field, SiC can be used especially for high-voltage unipolar devices such as MOSFETs and Schottky diodes, achieving low switching loss.

In today's power transistors, with the push towards high power and high voltage, ordinary Si-based MOSFETs as a unipolar device are becoming less popular due to the high on-state losses. Consequently, the Si IGBT as a bipolar device was typically the preferred choice for voltages exceeding 1000 V. The Si IGBT as a bipolar device also has lower on-state losses than a high-voltage Si MOSFET. However, a major drawback is that high-speed operation is not possible with Si IGBTs due to the restricted dynamics of injected holes that result in significant switching loss, for example, by tail currents. Alternatively, the larger critical electric field for breakdown of SiC allows a greatly reduced drift-region resistance for the same breakdown voltage compared to a silicon-based part. SiC MOSFETs also have the benefit of being unipolar devices, and thus enable faster switching than a Si IGBT, and better controllability of switching behavior. These features make the SiC MOSFET a very attractive device.

Table 1 Physical properties' comparison of basic semiconductor material [1]

Physical properties	4H-SiC	Si
Band gap [eV]	3.23	1.124
Breakthrough field [MV/cm]	2.5	0.25
Thermal conductivity [W/cm/K]	3.7	1.5
Ideal bulk mobility [cm^2/Vs]	1000	1420
Electron saturation vel. [cm/s]	$2x10^7$	$1.05x10^7$

Infineon has developed a truly "normally off" SiC MOSFET using the trench technology with the trade mark name CoolSiC™ MOSFET. The following chapters introduce this CoolSiC™ MOSFET and describe its basic performance, benefits, and application design guidelines.

2 Characteristics of the CoolSiC™ MOSFET

This chapter introduces the static and dynamic characteristics of the 1200 V CoolSiC™ MOSFET. Products that use the 1200 V CoolSiC™ MOSFET include chips, discrete units, and modules, as shown in Figure 1. More information is available in the respective product datasheets.

Figure 1 **Solutions using 1200 V CoolSiC™ MOSFET**

2.1 Static characterization

Static characterization includes:

- Blocking capability
- Output characteristics
- $R_{ds(on)}$ versus T_j
- Threshold voltage $V_{GS(th)}$
- Transfer characteristics
- Junction capacitance
- Body diode I-V characteristics

2.1.1 Blocking capability

The leakage current, I_{DSS}, of the CoolSiC™ MOSFET was measured with increasing temperature at a blocking voltage of 1200 V. This was done by shorting the gate and source terminals (V_{GS} = 0 V), and thus turning the device off.

2.1.2 Output characteristics

The I-V curves, or output characteristics, of each MOSFET were measured in the pulse mode at junction temperatures of 25°C and 175°C. Figure 2 (left graph) shows the drain current as a function of the drain-source voltage, V_{DS}, with different gate-source voltages, V_{GS}. The solid black curves are the typical results at 25°C and the red dashed curves are those at the maximum junction temperature of 175°C.

As the SiC MOSFET is a voltage-controlled device, it turns on step by step with increasing gate-source voltage. If the higher gate voltage is above the threshold level, the higher drain current is at the specified drain voltage. For higher drain currents or lower gate-source voltages, a significant curve steadily lowers the current slope with increasing V_{DS}. This behavior is a consequence of the built-in junction field effect transistor (JFET), which is formed by the deep p+ wells. As the p+ wells are linked to source, the junction channel of the JFET is controlled by a drain-source voltage drop. The JFET channel thus narrows down with rising V_{DS}. This feature improves the short-circuit ruggedness by limiting the saturation current when the drain voltage, V_{DS}, is very high.

The temperature behavior of the I-V characteristic also depends on temperature. At higher gate voltages, the drain current decreases with temperature. This results in better performance when multiple devices are paralleled. At lower gate voltages, the drain current increases with temperature. Thus, a low V_{GS} for the on-state is not recommended. For the recommended gate-source voltages, refer to the respective datasheet. Each generation has a slightly different trade-off between the on-state behavior and gate-oxide reliability, thus FIT rate.

2.1.3 On-state resistance versus the junction temperature

Figure 2 (b) shows an example of the on-state resistance, $R_{DS(on)}$, as a function of the junction temperature, T_j, with drain-to-source current, I_{DS}, as a parameter.

The $R_{DS(on)}$ of the CoolSiC™ MOSFET is mainly determined by the following factors: the MOSFET's channel, the JFET, and the drift region in the device. These all depend on temperature. The MOSFET's channel has a negative temperature characteristic due to the behavior of the interface states, while the drift region and JFET have positive temperature characteristics. The total $R_{DS(on)}$ of CoolSiC™ MOSFET is not dominated by the MOSFET's channel resistance because of the advantageous channel orientation along the preferred crystal plane with a low density of interface defects. Thus, the total $R_{DS(on)}$ exhibits a positive temperature coefficient in the complete temperature range. This behavior is beneficial for balancing the current distribution of parallel devices.

Moreover, with high temperature, the $R_{DS(on)}$ rises to limit the highest saturation current, thus improving the short circuit ruggedness of the device.

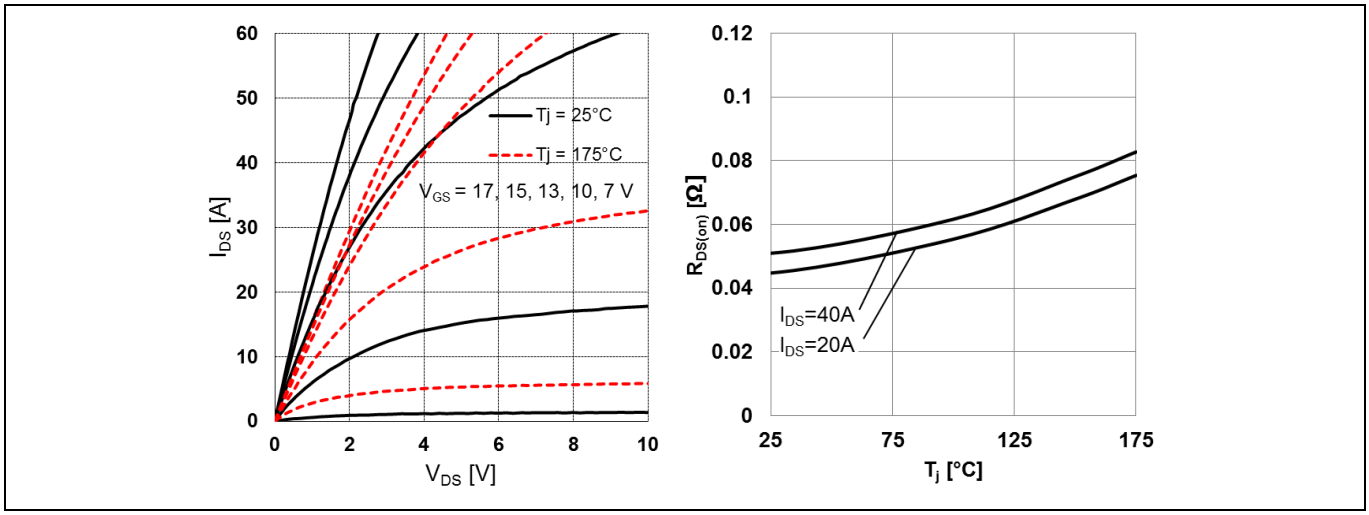


Figure 2 **(a) Typical output characteristics, V_{GS}, as a parameter, with T_j = 25°C and T_j = 175°C**
(b) Typical on-resistance vs. junction temperature, I_{DS} as parameter (V_{GS} = 15 V)

2.1.4 The threshold voltage

The threshold voltage, $V_{GS(th)}$, is the gate-source voltage required to start the current flow through the device channel at a specific drain-to-source current. Figure 3 (a) shows the threshold voltage versus temperature at I_{DS} = 10 mA**.** This threshold voltage $V_{GS(th)}$ was measured by first applying a 1 milisecond pulse-gate voltage at a V_{GS} = +20 V as a precondition [10]. $V_{GS(th)}$ was then read at V_{GS} = V_{DS} by forcing the current I_{DS} = 10 mA. The typical value for $V_{GS(th)}$ provides good noise immunity against parasitic turn-on, making it easier to use the device.

Characteristics of the CoolSiC™ MOSFET

Typically, SiC MOSFETs have a short-channel effect that reduces the threshold voltage at higher drain voltages. This effect is called drain-induced barrier lowering (DIBL), already identified in low-voltage Si power MOSFETs. In the CoolSiC™ MOSFET, the $V_{GS(th)}$ reduces when the blocking voltage, V_{DS}, increases, as shown in Figure 3 (b) where the drain current I_{DS} = 10 mA.

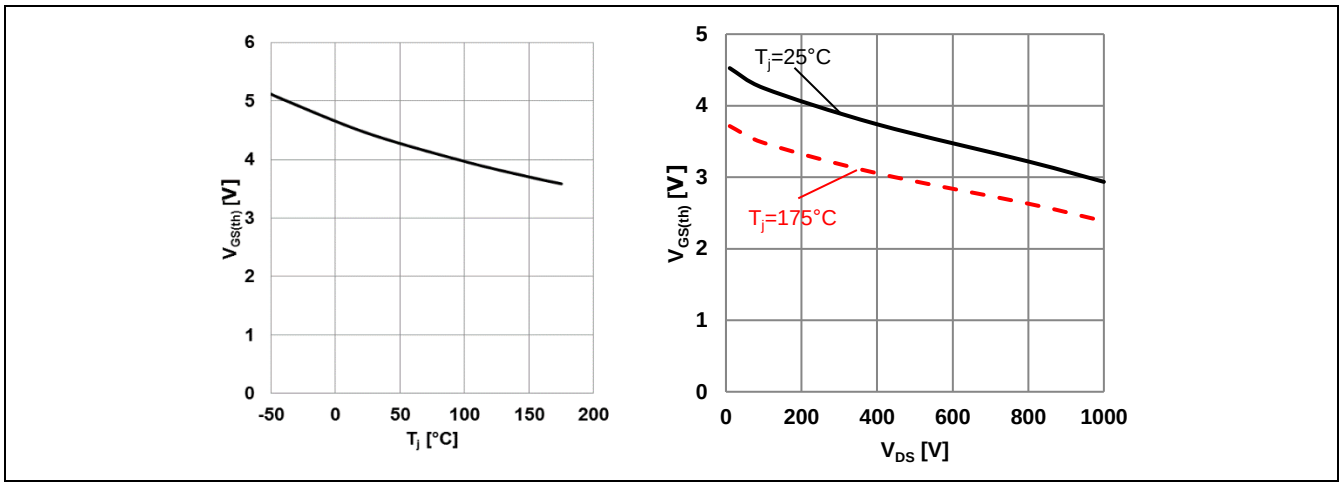


Figure 3 **(a) The typical gate-source threshold voltage as a function of junction temperature (I_{DS} = 10 mA, V_{GS} = V_{DS}); (b) The typical gate-source threshold voltage as a function of the drain-source voltage (I_{DS} = 10 mA)**

2.1.5 Transfer characteristics and small signal capacitance

The transfer characteristics of the CoolSiC™ MOSFET were obtained by measuring the drain current as the gate-source voltage increases from 0 V to V_{gsmax} for a fixed drain-source voltage (V_{DS} = 20 V), as shown in Figure 4 (a). The slope of the transfer curve is known as the transconductance g_{fs} of the MOSFET. It indicates that there is a crossing point at V_{GS} = 15 V. The temperature dependence decreases with increasing gate-source voltage, and the current decreases with temperature. This helps limit the saturation current in the event of a short circuit.

The low-signal capacitance of the CoolSiC™ MOSFET was measured at room temperature while the drain-source voltage was increased (up to 1000 V), as shown in Figure 4 (b). The device design is optimized to a favorably small ratio of the Miller capacitor, C_{rss}, related to the gate-source capacitor, $C_{iss.}$ It helps avoid issues related to bridge topology and parasitic turn-on from the Miller capacitor. Here, the capacitor C_{iss} is the input capacitance with C_{gs} + C_{gd}, the output capacitor C_{oss} is equal to C_{gd} + C_{ds}, and C_{rss} is the Miller capacitance, also called the reverse capacitance.

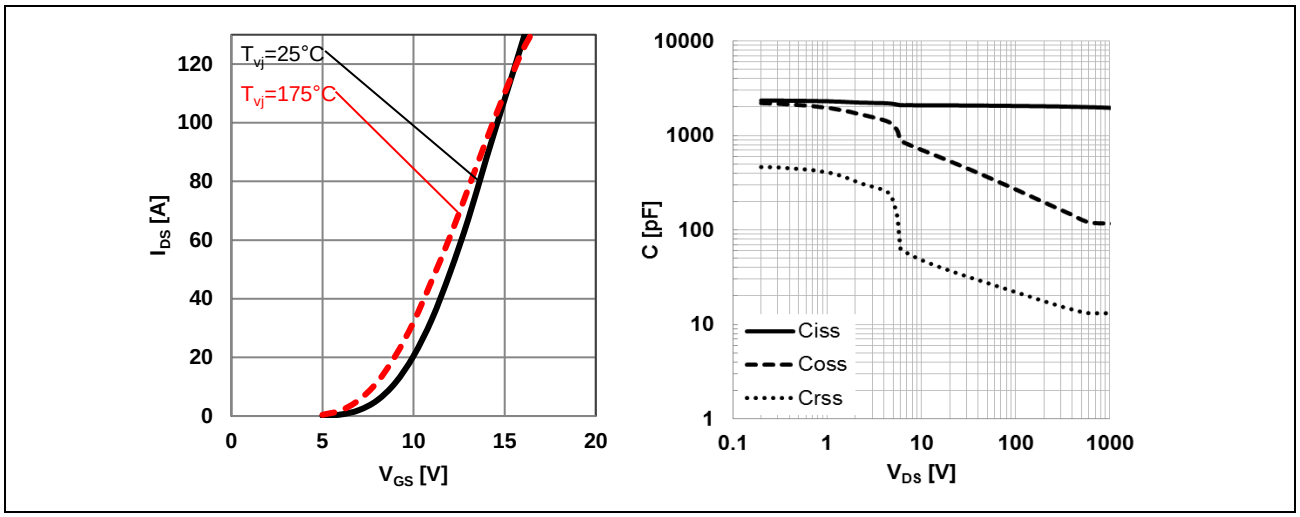


Figure 4 **(a) Typical transfer characteristics (V_{DS} = 20 V). (b) Typical capacitance as a function of the drain-source voltage**

2.1.6 Third quadrant operating mode

Like other MOSFETs, the CoolSiC™ MOSFET also integrates an intrinsic body diode with p-n junction behavior. As shown in Figure 5, the intrinsic bipolar body diode has a relatively high forward voltage, V_{SD}, compared to silicon parts. This is due to the wide bandgap characteristics of the silicon carbide material. The forward voltage, V_{SD}, has a negative temperature coefficient as well as a standard Si p-n junction diode. Therefore, it is not effective to use the body diode to conduct currents for long periods of time. Fortunately, unlike IGBTs, the SiC MOSFETs can conduct reverse current from source to drain through the channel if a positive bias is applied to the gate. This mode of operation is called synchronous rectification (or third quadrant operation) and achieved with a positive voltage on the gate. Figure 5 highlights that the synchronous rectification mode is highly recommended to limit conduction losses. Applying synchronous rectification also has an additional benefit, which is that the positive temperature coefficient of R_{dson} supports current sharing.

However, the body diode has to operate during dead time when both the high-side and low-side MOSFETs are turned off in bridge topologies. Therefore, it is necessary to design the dead time period as short as possible (synchronous rectification mode). The value of dead time depends on the topology and the design circuit. For example, hard or soft switching, PCB layout, gate drive IC selection, and so on. The time interval can range from a 100 nanoseconds to several hundred nanoseconds.

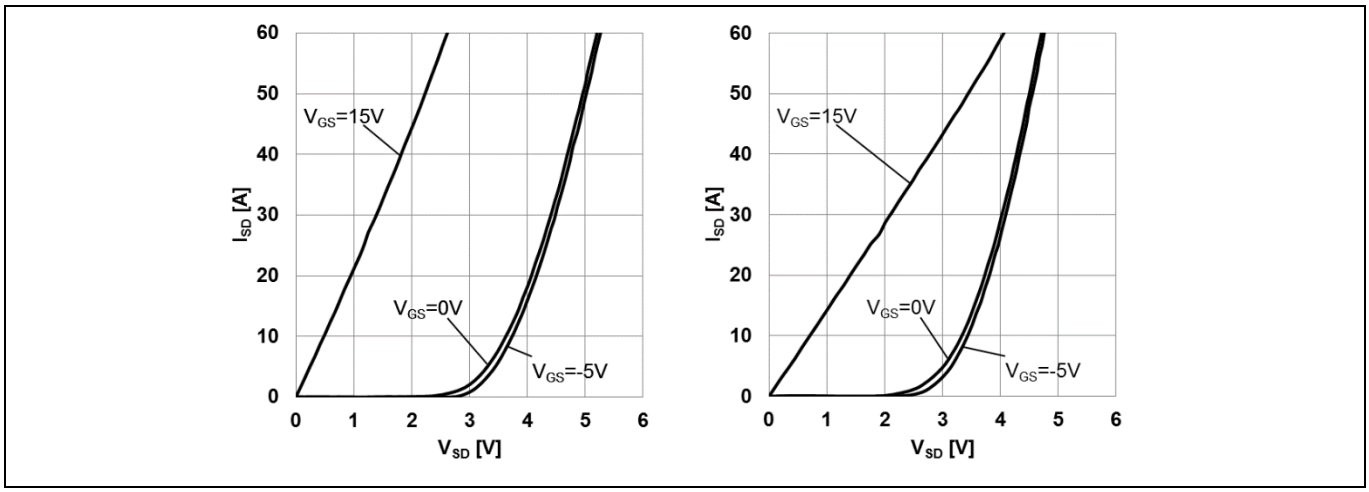


Figure 5 **Reverse current I_{SD} as a function of the voltage at different gate voltages and temperature. (a) T_j = 25°C, (b) T_j = 175°C**

2.2 Dynamic characterization

Dynamic characterization includes switching characteristics, body diode reverse-recovery charges, and short circuit and gate charges.

2.2.1 Switching characteristics

A clamped double-pulse testing circuit was used to measure the switching losses for TO-247 3-pin and TO-247 4-pin packages at 175°C, as shown in Figure 6. The 20 A 1200 V G5 SiC Schottky diode was used as a high-side freewheeling diode. The external gate resistor, R_G, was at 2 Ω and the V_{GS} was at +15 V for turn-on and -5 V for turn-off. Both the TO-247 3-pin and TO-247 4-pin packages showed much lower switching losses compared to their Si counterpart. As the TO-247 4-pin package can separate the gate-source pin and the power-source pin (Kelvin connection), the TO-247 4-pin can reduce E_{on} by 40% and E_{off} by around 10% at a drain current of 40 A in a 45 mΩ rated device. The higher the current to be switched, the bigger the benefit of the TO-247 4-pin package will be. For a hard-switching topology, using the TO-247 4-pin package is recommended for reducing switching losses and ringing.

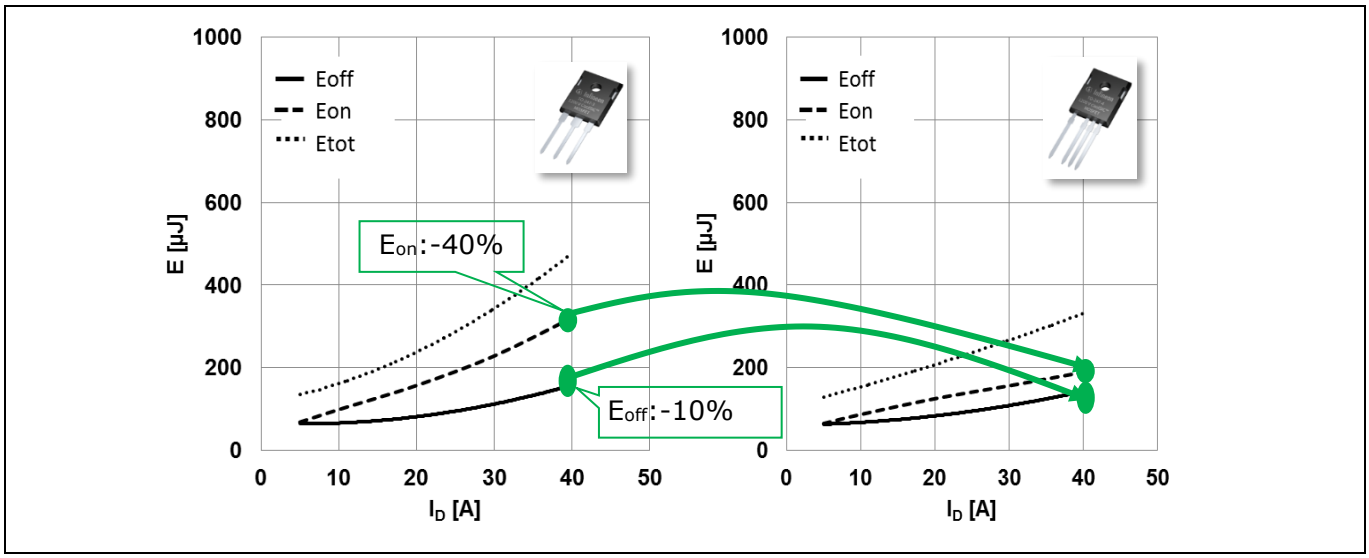


Figure 6 **Typical switching energy losses as a function of the drain-source current with T_j = 175°C. (a) TO-247 3-pin, (b) TO-247 4-pin**

Characteristics of the CoolSiC™ MOSFET

Figure 7 shows the typical turn-on and turn-off waveforms of the TO-247 3-pin CoolSiC™ MOSFET at 800 V_{DC} and 175°C. The test was a double-pulse test using its own body diode as a freewheeling diode. The test showed that the SiC MOSFET has implemented the feature of tuning the drain-source slew rate dv/dt and di/dt, which helps mitigate spikes or ringing. It also showed that the CoolSiC™ MOSFET provides good control for switching transients through the gate resistor value. At higher external gate resistor values, the drain-source slew rate, dv/dt, decreases, however at the cost of increased switching loss. When increasing the external gate resistor, the ringing voltage on the drain source can be suppressed. The ringing of the gate-to-source voltage, V_{GS}, is further reduced during turn-on and turn-off transients.

The slew rate dv/dt and switching losses can be fully controlled by changing the external gate resistor, R_G, as shown in Figure 8. This proves that the device can clearly be controlled through R_G for a trade-off between the slew rate dv/dt and switching losses. A higher R_G leads to fewer EMI problems and low R_G can reduce switching losses. Also, the gate-to-source V_{GS} waveform is smooth during turn-on and turn-off with different gate resistors due to a favorable Miller capacitance, C_{rss}, and gate-to-source capacitance, C_{gs} ratio.

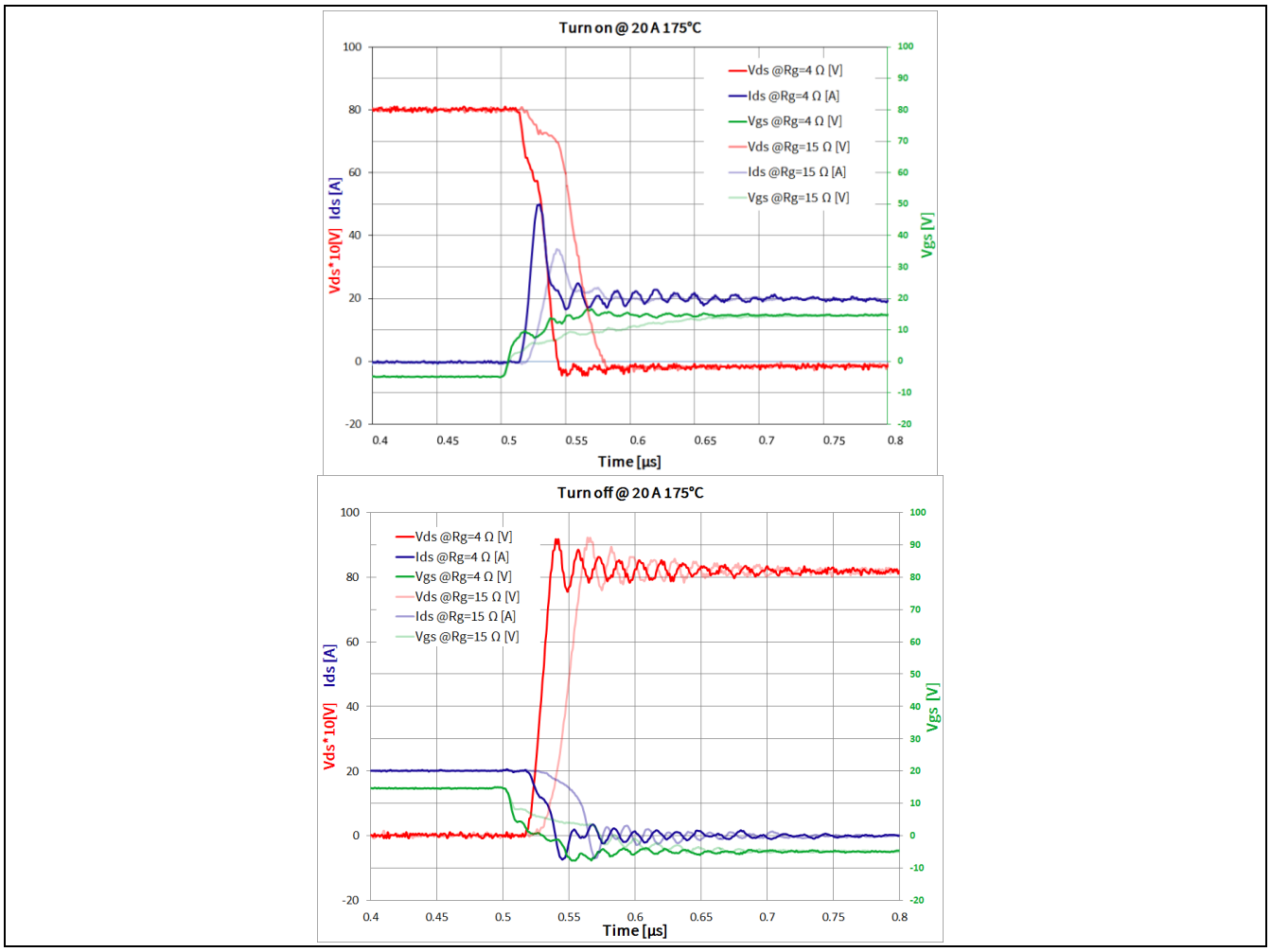


Figure 7 **Typical switching turn-on and turn-off waveforms (TO-247 3-pin)**

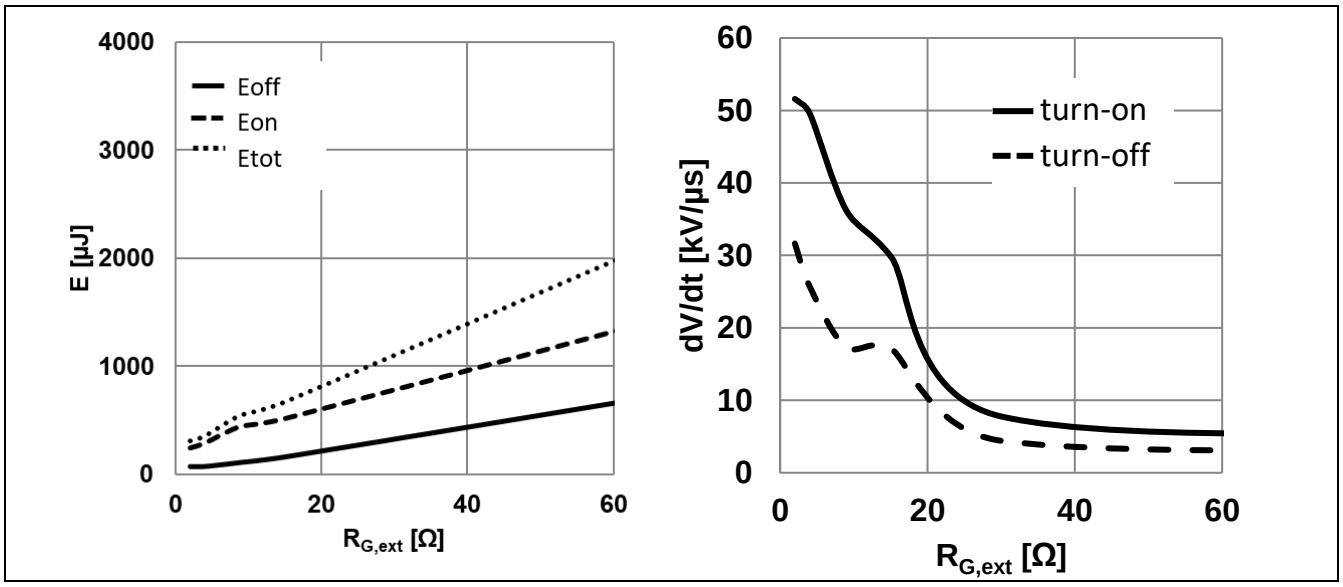


Figure 8 **(a) Typical switching energy losses and (b) maximum dv/dt values versus external gate resistor R_G at V_{DS} = 800 V, 40 A, V_{GS} = +15/-5 V, 175°C, in a half-bridge configuration**

2.2.2 Body diode reverse-recovery

The switching performance of the intrinsic body diode is measured with Q_{rr} and I_{rrm} at V_{DS} = 800 V, $V_{GS,nom}$, and $I_{SD,nom}$. As shown in Figure 9, the reverse-recovery charge is dependent on temperature, unlike in a SiC Schottky diode. The higher the temperature, the higher the reverse-recovery charge. This effect is evidently caused by minority carriers injected by the forward-biased intrinsic pn-junction that generates a reverse-recovery charge. Fortunately, the absolute values at the rated current are still fairly low, i.e., the CoolSiC™ MOSFET has significantly lower, almost negligible, reverse-recovery losses.

The body diode, Q_{rr}, is an important parameter for a bridge topology with hard commutation. During the dead time period in a bridge topology, the body diode is freewheeling current before the corresponding transistor is turned on. When the transistor is turned on, the body diode reverse-recovery current goes through the corresponding transistor for a short period. With the low Q_{rr} of the CoolSiC™ MOSFET, switching loss can be minimized. It also enables an increase in the switching frequency.

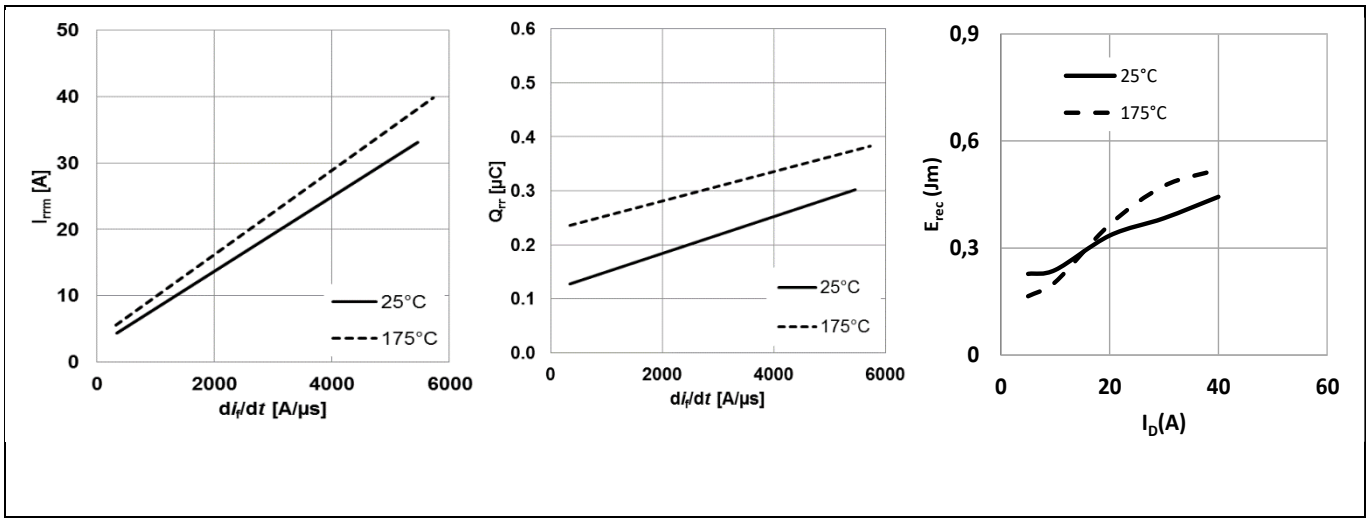


Figure 9 **Typical (a) reverse-recovery charge, (b) reverse-recovery current, and (c) reverse-recovery energy as a function of the diode's current slope**

2.2.3 Short circuit capability

Figure 10 shows the short circuit waveforms of the TO-247 4-pin and TO-247 3-pin packages with V_{GS} = -5 V/+15 V and DC voltage V_{DD} = 800 V. Initially, the drain current increases rapidly and reaches the peak current level. Due to the fast turn-on with a Kelvin-source design, the TO-247 4-pin current rises faster, and has less self-heating at the beginning of the short circuit event with high peak current exceeding 300 A. The TO-247 3-pin package, on the other hand, has a smaller peak current. A major reason is the negative feedback induced via the di/dt against the applied V_{GS} in the case of the 3-pin device. This effect is eliminated in the solution with a Kelvin connection that enables faster switching. Thus, the current can rise to higher values in a 4-pin device before the saturation effect takes place.

After peak current, the drain current reduces significantly to about 150 A. This is due to the reduction in carrier mobility and the JFET effect with rise in temperature and self-heating. The test waveform in Figure 10 shows a clean, robust behavior. This proves a 2 µs the short circuit capability specified in the datasheet (10x) for both packaged TO-247 first-generation CoolSiC™ MOSFETs (3 µs) and power modules (2 µs).

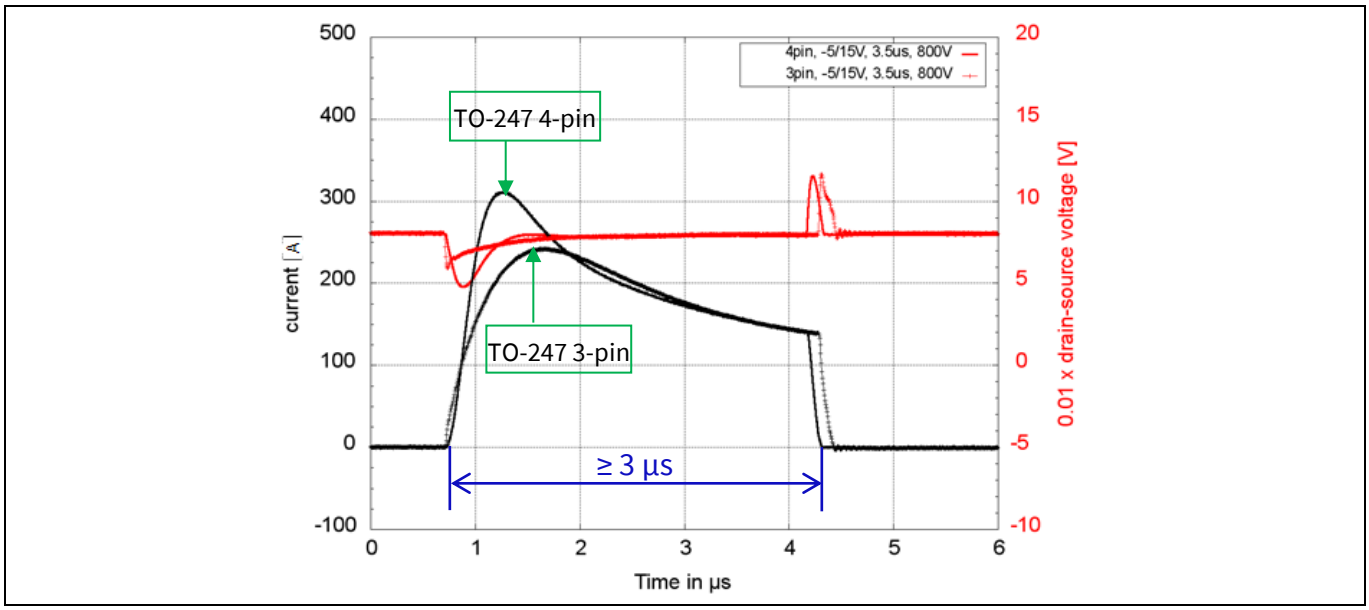


Figure 10 **A typical short circuit as a function of time at 25°C**

2.2.4 Gate charge

Figure 11 provides the gate-charge waveform at $I_{DS,nom}$ and V_{DS} = 800 V with a declining V_{DS} as reference. The CoolSiC™ MOSFET's Miller plateau is non-flat with a "Miller ramp". This means that the gate-source voltage of the MOSFET changes during the drain-source voltage fall and rise transitions instead of remaining constant. As there is no "typical" flat Miller plateau, the Q_{GD} cannot simply be extracted by using the length of the plateau/ramp phase. During the ramp phase, the C_{gs} is also charged (V_{GS} rises) for the CoolSiC™ MOSFET. Therefore, to estimate a more practical Q_{GD}, the V_{DS} waveform was overlaid on the Q_G waveform, and Q_{GD} was extracted when V_{DS} was between 97% to 10%. This also fits nicely to the integral of C_{rss}. $Q_{GS,pl}$ is defined as the charge from the origin (V_{GS} = -5 V) to the start of the ramp. The total gate charge, Q_G, is still defined as the charge from the origin (V_{GS} = -5 V) to the point on the curve where the driving voltage equals the actual gate-to-source voltage of the device.

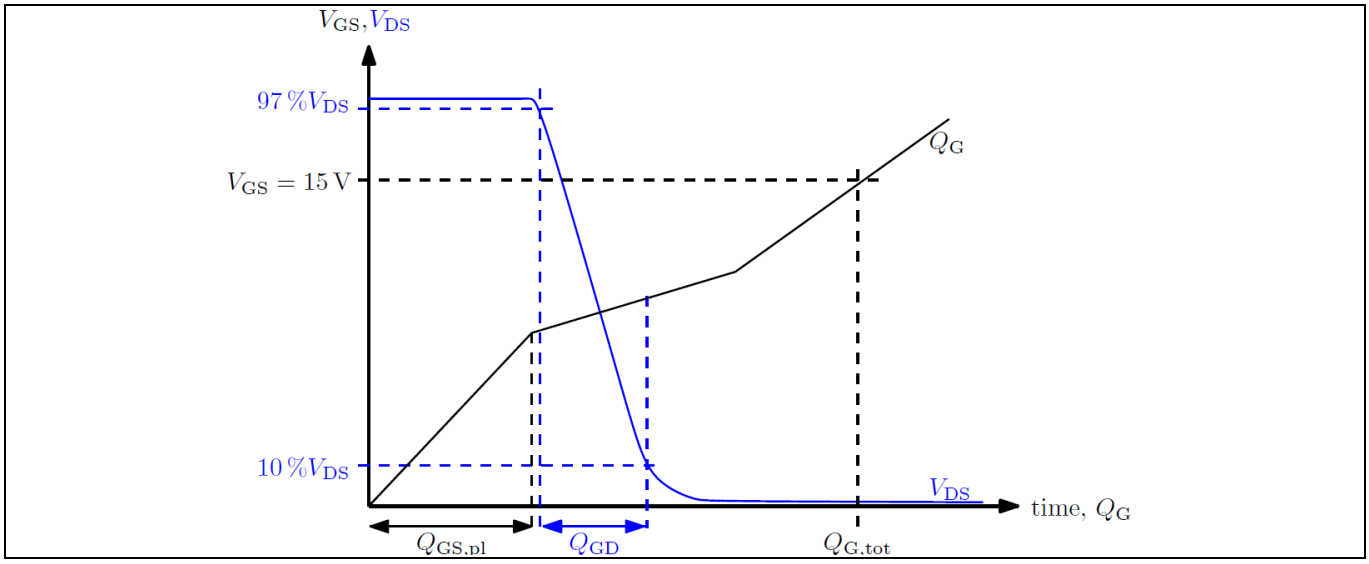


Figure 11 **Typical gate charge, $V_{GS} = f(Q_G)$, $I_{DS,nom}$,V_{DS} = 800 V, turn-on pulse**

3 Driver design guideline

This chapter provides the points to consider while designing a gate driver and some design tips for paralleling the discrete TO-247 4-pin CoolSiC™ MOSFETs.

3.1 Design considerations

When designing a gate driver for CoolSiC™ MOSFETs, it is essential to consider the on-state and off-state of the gate-to-source V_{GS} voltage. The recommended value for the turn-on V_{GS} can be found in the product datasheet. The CoolSiC™ MOSFET's technology enables a high and temperature stable threshold voltage, $V_{GS(th)}$, that allows for the 0 V turn-off V_{GS} in many applications. This translates into a simplified gate driver circuit, including its power supply. However, CoolSiC™ MOSFETs can switch at very high speeds, with voltage slew rates ranging from tens to hundreds of volts per nanosecond. To improve the noise margin and ensure reliable operation at very high switching speeds, a negative gate-to-source turn-off voltage is often recommended. This is even more advisable for hard-switching topologies, where the turn-off switching losses can be reduced by using a negative V_{GS} for turn-off. When defining the turn-off V_{GS} considering the parameter stability over time is recommended, as discussed in AN2018-09 [14].

Using a gate driver with a Miller clamp function can also help ensure that the CoolSiC™ MOSFETs are kept off. It also enhances the robustness of the CoolSiC™ MOSFETs against parasitic turn-on due to high dV/dt induced Miller currents.

A gate-driver reference circuit for a discrete CoolSiC™ MOSFET TO-247 package is shown in Figure 12. The circuit generally includes an isolated DC-DC power supply and an isolated gate driver IC. Depending on the selected isolated gate driver IC, if no GND2 pin is present, a virtual GND2 can be created and referenced to the source of the CoolSiC™ MOSFET. The output section of the gate driver is supplied via the isolated DC-DC power supply. The rectified output of the isolated DC-DC is split into two rails: +15 V connected to the *VCC2* pin and -5 V connected to the VEE2 pin. The middle point of the power supply is connected to the source terminal, creating the aforementioned virtual ground GND2. Therefore, the 15 V is used for turning on and the -5 V is used for turning off the CoolSiC™ MOSFET.

When selecting the gate driver IC, the following characteristics should be considered:

- **Maximum supply voltage capability**: The maximum driving voltage V_{GS} of the CoolSiC™ MOSFET should be considered, including a safety margin to allow for voltage overshoots during fast transients. When targeting high dv/dt switching of CoolSiC™ MOSFETs, small gate resistors are selected. These can lead to undesired larger voltage spikes due to inductances in the gate path. Due to this a higher design should be considered for the absolute maximum supply voltage rating of the gate driver IC, compared to Si MOSFETs. Generally, a gate driver IC with maximum voltage rating of 28 V or above is recommended, which might not be fulfilled by Si-targeted gate driver ICs
- **CMTI rating**: With high dv/dt slew rates of the CoolSiC™ MOSETs, a high common mode transient immunity (CMTI) rating of the gate driver IC is highly recommended. Otherwise, the gate signal might not be registered correctly and even a false turn-on signal might appear. These could result in the destruction of the application. As a rule of thumb, allow for a safety margin and select a gate driver IC with a CMTI rating higher that the expected slew rates in the application to allow for imperfect layouts and cross coupling in the application
- **Design of the output stage**: To achieve switching (turn-on and turn-off) of the CoolSiC™ MOSFETs, apart from the peak current of the gate driver IC, a gate driver IC with a pure PMOS turn-on transistor should be selected. This will ensure strong turn-on currents all the way to the *VCC2* rail, minimizing the switching losses. It will also enable the CoolSiC™ MOSFET's fast switching performance with a high dv/dt slew rate
- **Propagation delay skew**: To enable high switching frequencies and improve efficiency, the dead time for bridge topologies should be minimized as much as possible. While propagation delay might seem relevant,

this has no impact on the dead time. It only influences the delays in the control loop. The important parameter to look for is the skew, which defines the part-to-part propagation delay matching between the gate driver ICs. The shorter the skew is, the shorter the dead time can be. As the skew defines the mismatch between the gate drivers for the same edge (turn-on or turn-off), Infineon has recently introduced the SKEW+ parameter. This parameter defines the maximum mismatch that can be expected for two gate driver ICs for opposite edges (one gate driver turns-off while the other turns-off or vice versa)

There are several gate driver ICs from Infineon that are recommended for driving the CoolSiC™ power MOSFETs. They offer a broad variety of features tailored for specific applications. Advanced options for SiC MOSFETs using the EiceDRIVER™ gate driver ICs are presented in the application note AN2017-04 [12].

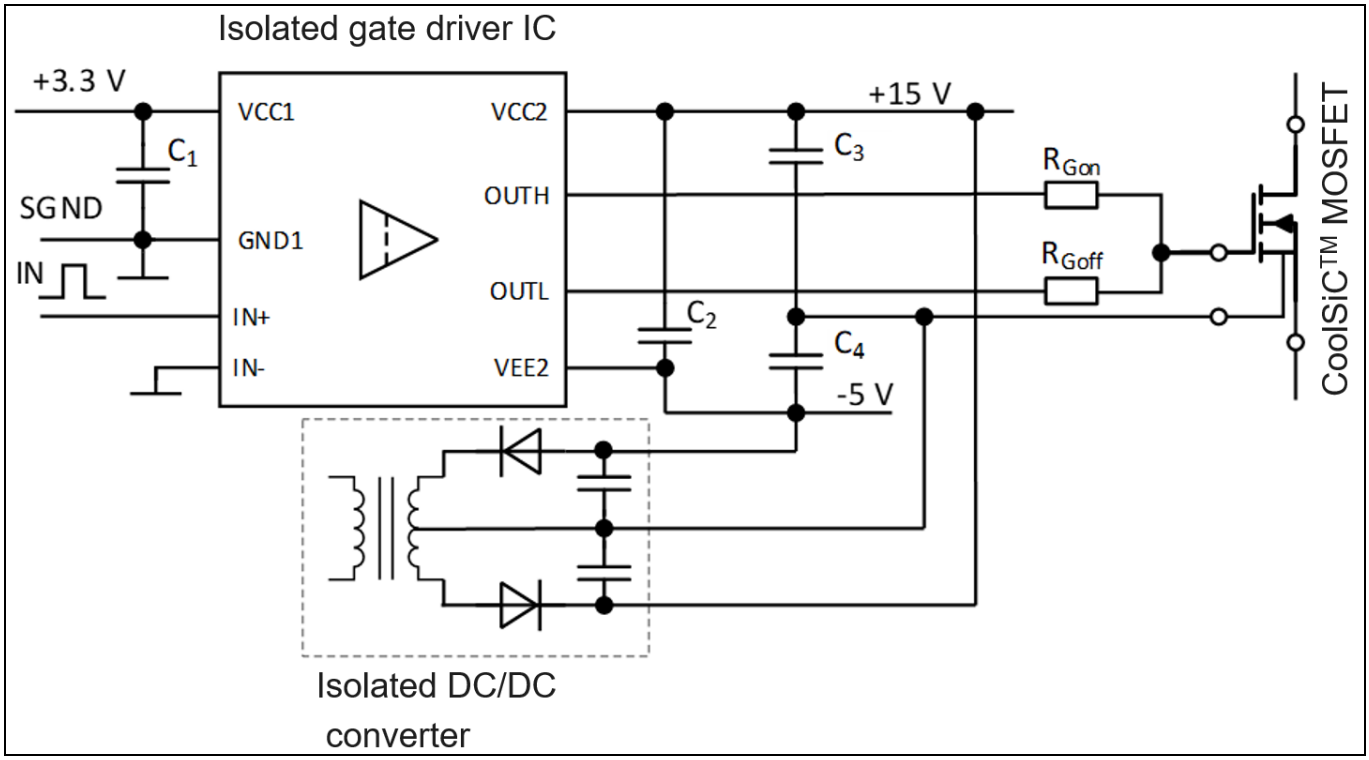


Figure 12 **A gate-driver design reference for the discrete CoolSiC™ MOSFET**

3.2 Design tips

Following are some design tips for the CoolSiC™ MOSFET TO-247 package:

- Separate gate resistors (R_G) for turn-on and turn-off (R_{Gon} and R_{Goff}) allow for better control of the slew rate for turn-on and turn-off. This can prevent any unnecessary rise in switching losses. Normally, a lower value can be selected for the turn-off resistor, R_{Goff}, than for the turn-on resistor, R_{Gon}, to obtain a fast fall-time and to reduce the risk of a parasitic turn-on
- For multiple discrete MOSFETs in parallel, make sure that there is equal current sharing during conduction and switching. As a rule of thumb, split the gate resistor. Have one common resistor on the output of the gate driver IC, but also place individual gate resistors between the gates of the CoolSiC™ MOSFETs and the common resistor. Avoid power circuit current across the Kelvin sources when connecting the Kelvin sources of the discrete MOSFETs
- The bulk driving energy for turning the CoolSiC™ MOSFETs on and off is mainly provided by the decoupling capacitors C_3 and C_4. C_3 provides the energy for charging the gate capacitance, while C_4 is responsible for the energy needed to discharge the gate capacitance. Dimension these based on the acceptable voltage drop

on the power supply, considering the gate charge of the MOSFETs and the switching frequency. A good starting value for the capacitors would be 4.7 µF.

- Capacitor C_2 is connected directly across the supply terminals on the output side. This capacitor decouples and filters the high frequency noise that could be present on the supply rail and couples them into the gate driver. A good starting value for this capacitor is 100 nF
- The input side of the gate driver also requires decoupling of the power supply rail, especially in the case of longer traces or wires, or fast switching. This is done through capacitor C_1. A good starting value for which would be 100 nF

Generally, the capacitors should be low ESR, low ESL, and placed as close as possible to the pins of the gate driver IC. Usually Multilayer Ceramic Capacitors (MLLC) with class II dieelectic (X7R, X8R, Z5U, Y5V) are selected. Keep in mind the reduction of capacitance with DC bias.

3.3 Gate drive circuit and PCB layout

Figure 13 shows the gate-driver reference circuit and PCB layout for two TO-247 4-pin devices in parallel. In the circuit, an EiceDRIVER™ isolated gate driver IC U1 1EDI60N12AF is used. One isolated DC-DC converter U2 is used for converting the +12 V input on the primary side to a +18 V output on the secondary side. To generate a negative rail, a 3 V Zener diode, ZD2, is used to split the +18 V into +15 V for turn-on and -3 V for turn-off.

For the PCB layout, the gate source and power source tracks must be separated to prevent the gate signal from noise interference. This rule should be applied for both TO-247 3-pin and 4-pin packages. Normally, gate source tracks use a narrow width to handle the gate signal, and the power source tracks use a much wider width to handle high-current and high-power conduction. This enables a Kelvin connection on the PCB board.

To reduce the commutation loop inductance, the power source and drain tracks are designed as short as possible. The gate resistors and gate driver IC should be placed close to their corresponding MOSFETs to reduce the gate-loop parasitic inductance. When paralleling TO-247 4-pin packages, splitting part of the gate resistance to the Kelvin source (see R_3 and R_7 in the circuit diagram in Figure 13) is recommended. This limits the circulating current [9] that could form between the power source to the Kelvin source in each device.

Driver design guideline

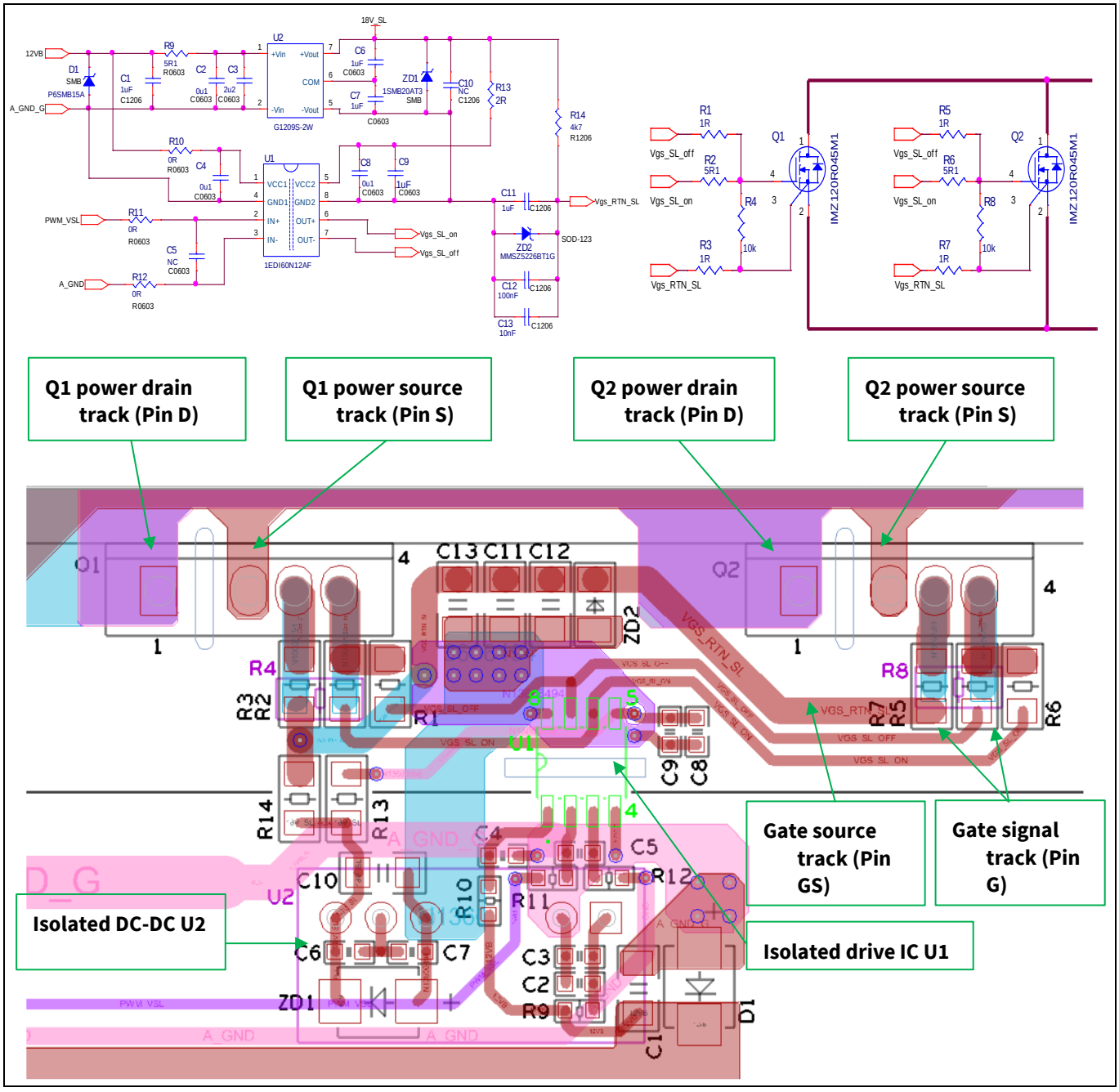


Figure 13 **Example of a drive circuit and PCB layout for two TO-247 4-pin units**

The result of the high slew rate dv/dt is that it may generate high currents, I_{GD}, that flow in the Miller capacitance (C_{gd}). If the gate driving circuit is not properly designed, this effect may cause the device to turn on by mistake when it is intended to be off, the so-called parasitic turn-on. In a conventional hard-switching, half-bridge topology application, this induced turn-on increases the risk of shoot-through current. This is a potential reason for unwanted losses and may even damage or destroy the device by exceeding its safe operation ratings. Therefore, it is important to select a gate driver IC that not only meets the drive and speed requirements but can also handle the Miller currents during fast switching.

Driver design guideline

Infineon's CoolSiC™ MOSFET has a high $V_{GS(th)}$, and a small Miller capacitance, C_{rss}, to gate-source capacitance, C_{gs}, ratio (C_{rss}/C_{gs}). This provides a high robustness against parasitic turn-on. Besides this, there are additional practical approaches that can help minimize the chances of a parasitic turn-on:

- Reduce the gate loop inductance by placing the driver as close to the gate and source sense pads as possible
- If the turn-off gate resistor used for adjusting the turn-off slew rate is on the large side, then combined with the negative voltage it is not sufficient to mitigate the possibility of having Miller current-induced parasitic turn-ons. Therefore, selecting a gate driver IC with a Miller clamp or a Miller clamp driver is highly recommended to provide a low impedance path for the current to flow [12]
- If the gate driver has a low pull-down output impedance, the low impedance will help bypass I_{GD} to the ground. If the gate resistor is used for slew rate control, consider using a separate turn-off gate resistor to minimize the impedance during turn-off. The smaller the turn-off resistor, the smaller the pull-down impedance will be to directly bypass the I_{GD} to the ground
- When using a gate driver with a single output for both sourcing and sinking the gate currents, if separate control of the turn-on and off through dedicated gate resistors is desired, the gate resistors can be placed in parallel and a low voltage drop diode, such a Schottky diode, can be added in series to the turn-off resistor to separate the current direction between the two resistors

4 Advantages of the CoolSiC™ MOSFET

This chapter outlines the advantages of the CoolSiC™ MOSFET as compared to alternative Si or SiC switching devices.

4.1 Comparison of switching losses with a 1200 V Si IGBT

Figure 14 shows the switching comparison between a 40 A 1200 V H3 IGBT and a 45 mΩ M1 CoolSiC™ MOSFET, using the same double-pulse test circuit at 800 V DC, R_G = 2.2 Ω and V_{GS} = +15 V/-5 V. The test setup used the same freewheeling diode with a 1200 V/20 A G5 SiC Schottky diode on the high side. The CoolSiC™ MOSFET has a significantly lower temperature dependency than the Si IGBT from room temperature to high temperature. Especially for turn-off losses, the Si IGBT has a bipolar nature with approximately ten times higher turn-off losses at 175°C, and five times higher turn-off losses at 25°C. The CoolSiC™ MOSFET also has lower turn-on losses than the Si IGBT by a factor of 25% to 50% depending on the drain current, I_D.

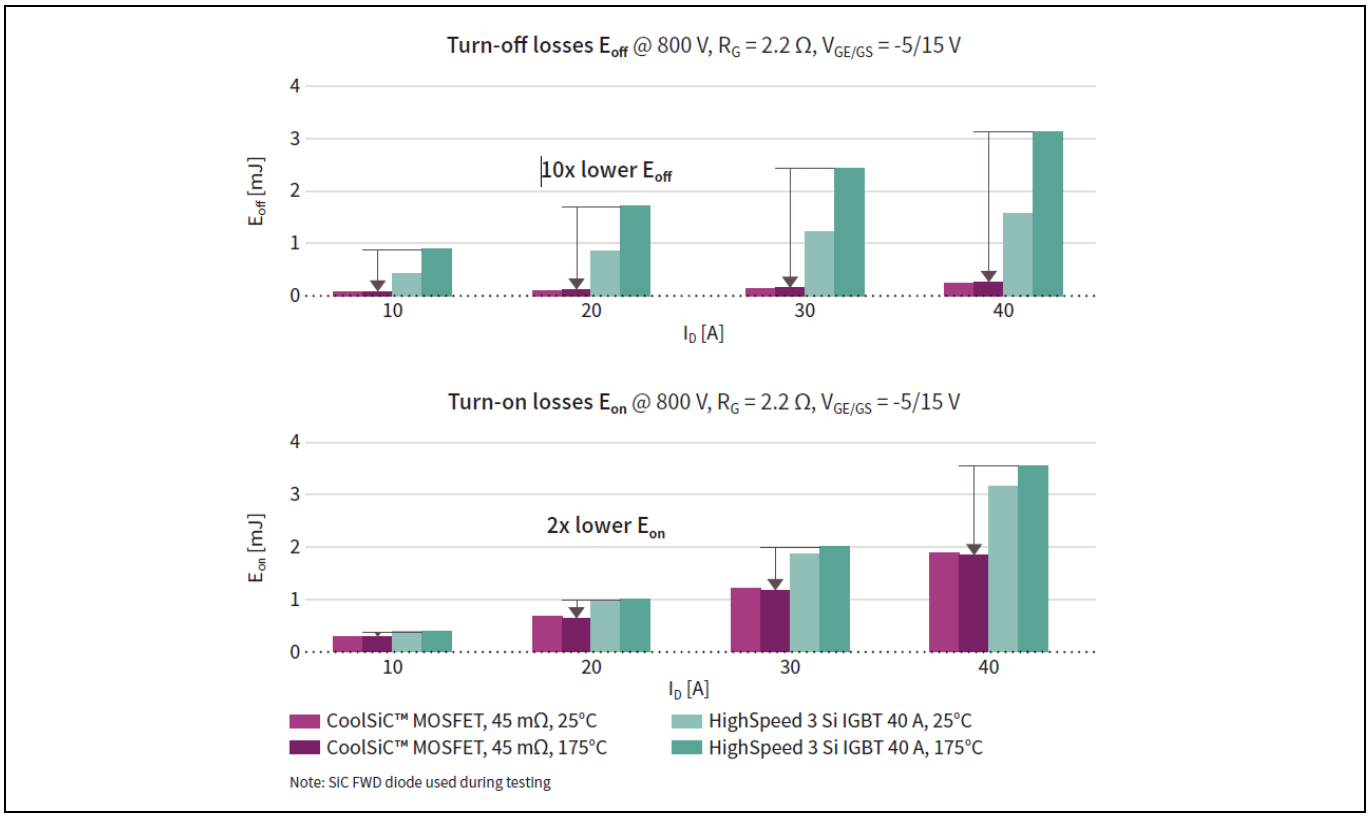


Figure 14 **Comparison between E_{off} and E_{on} switching of a 1200 V H3 IGBT and the M1 CoolSiC™ MOSFET**

4.2 Comparison of conduction losses with a 1200 V Si IGBT

Figure 15 shows the output characteristics of a 40 A 1200 V H3 IGBT and a 45 mΩ M1 CoolSiC™ MOSFET. The forward voltage of both the devices is the same at a rated current of 40 A at 25°C. However, the CoolSiC™ MOSFET has a nearly resistive output characteristic when the current is below the rated current. In contrast, the Si IGBT has a diode-like knee voltage drop, typically in the order of 1 V to 2 V, increasing only with the log of the current, as shown by the solid green line. In real-life applications, the actual current through the device is normally lower than the nominal rated current of the device. For example, assuming an operating RMS current of 15 A, at room temperature the forward voltage of the CoolSiC™ MOSFET is half that of the Si IGBT. At a high temperature of 175°C, the forward voltage of the CoolSiC™ MOSFET is around 80% of the Si IGBT. This proves that the CoolSiC™ MOSFET has lower conduction losses than the same rated Si IGBT in real-life conditions.

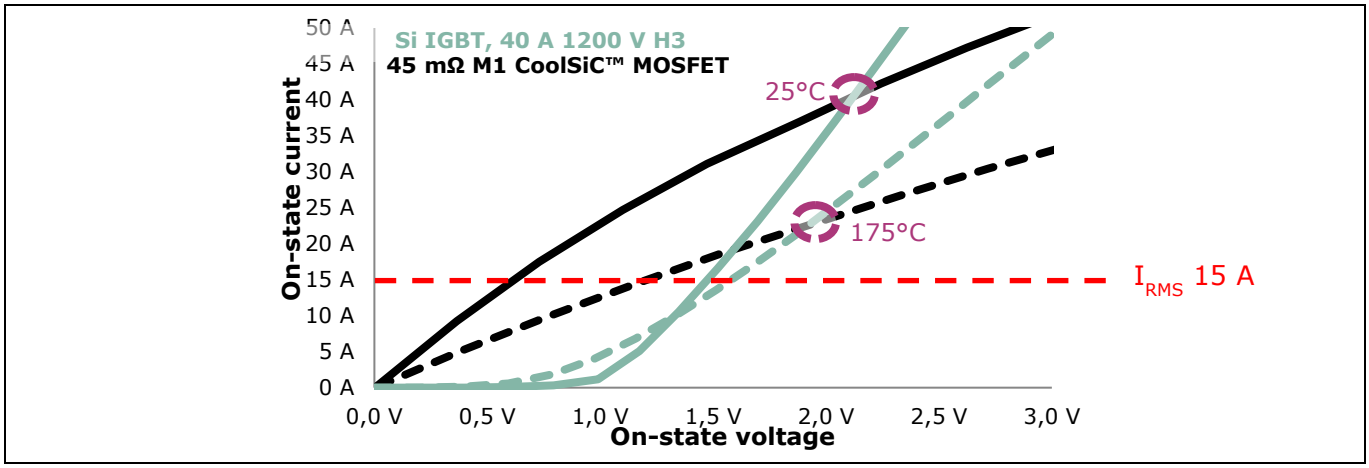


Figure 15 **Comparison between output characteristics of 1200 V H3 IGBT and CoolSiC™ MOSFET**

4.3 Comparison of body diode commutation

The intrinsic body diode of the CoolSiC™ MOSFET performs similar to a SiC Schottky diode with low reverse-recovery charge, Q_{rr}. At 25°C, it has almost the same Q_{rr} as the 1200 V G5 SiC Schottky diode for the same rated current. However, the Q_{rr} increases with the rise in junction temperature due to the intrinsic pn-junction structure with reverse-recovery time. As shown in Figure 16 (a), the body diode of the CoolSiC™ MOSFET has a slightly higher Q_{rr} than a 1200 V 20 A SiC G5 Schottky diode at 175°C. It has a very small influence on the overall performance, even at maximum junction temperatures.

Figure 16 (b) shows a comparison of the Q_{rr} with the 650 V 41 mΩ Si MOSFET that integrates a fast recovery body diode and the CoolSiC™ MOSFET. It proves that the 1200 V CoolSiC™ MOSFET's body diode has less than 10% Q_{rr} of the 650 V Si MOSFET both at room temperature and high temperature.

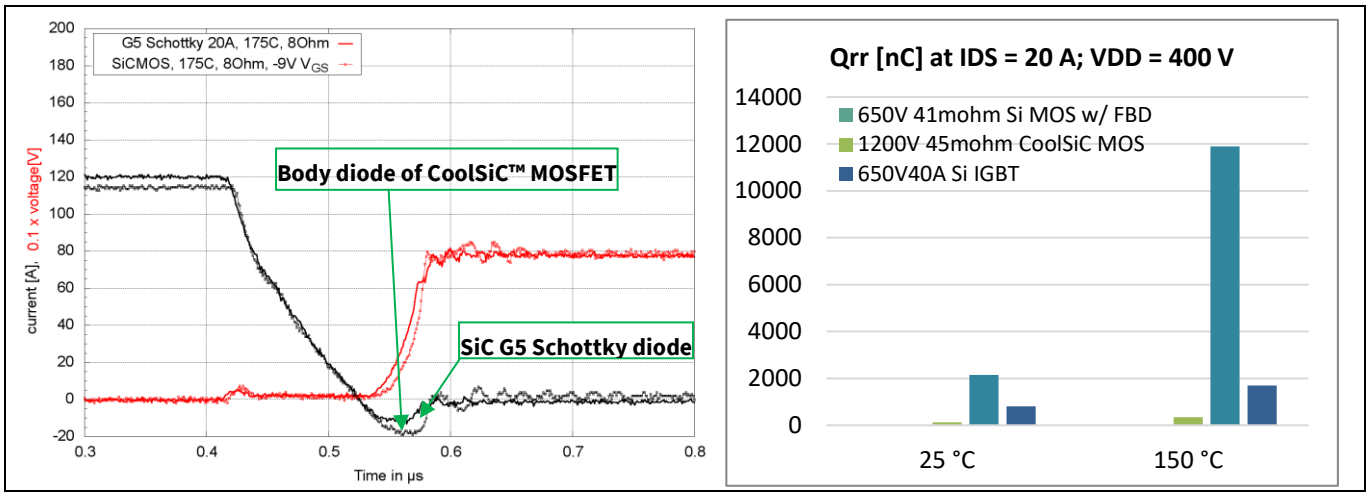


Figure 16 **a) Comparison of the body diode commutation and b) body diode Q_{rr} with a 650 V Si MOSFET with fast body diode**

4.4 Comparison of a CoolSiC™ MOSFET with alternative SiC switches

Given the benefits of the SiC material mentioned in Chapter 1, there have been extensive investments in research and development of the SiC MOSFET as a normally switched-off transistor. The initial fabrication of the SiC MOSFET was stifled mainly due to the quality of the SiC/SiO2 interface. The poor quality of the boundary between the SiC surface and oxide resulted in low mobility in the inversion layer, while the high electric field generated within the SiC in blocking mode could degrade the gate oxide, thus influencing the lifetime and reliability of SiC MOSFETs. Although these issues have improved in recent years, there are still many concerns about increasing channel mobility while keeping the same gate-oxide reliability as that in a traditional Si transistor.

Unlike the standard planar SiC MOSFET, the SiC trench MOSFET uses a crystal lattice plane for the inversion channel, which enables high channel mobility. Thus, allowing the SiC MOSFET's gate oxide to be thicker, which in turn leads to higher robustness. However, as SiC devices operate in blocking mode with high drain-induced electric fields, the challenge is to limit the electric gate-oxide field at the corners of the trenches. The CoolSiC™ 1200 V trench MOSFET uses a favorable trench structure to increase channel mobility. In addition, the device is specifically realized by deep buried p-type regions that adjoin a part of the trench structure and reach well below the depth of the actual trench to reduce the off-state induced electric field. The CoolSiC™ MOSFET contains a trench structure in which the MOS channel is aligned to the a-plane to optimize channel mobility and to reduce the V_{th} spread. Finally, the abovementioned deep p-regions are effectively connected by an ohmic contact to the source and thus, act as a powerful body diode.

With the same high performance as other SiC MOSFETs, the CoolSiC™ MOSFET has the following unique advantages:

- The CoolSiC™ MOSFET has a very reliable gate oxide with critical electric field, well-suited to guarantee full gate-oxide reliability
- Its V_{GS} operating window enables the best trade-off between performance and reliability
- The CoolSiC™ MOSFET structure has a favorable ratio of the Miller capacitance, C_{rss}, and the gate-to-source capacitance, C_{gs}. This provides an excellent trade-off between controllable switching speeds and immunity against parasitic turn-on
- The large area of the p-emitter enables the device to be used as a rapid freewheeling diode with high commutation robustness and low reverse-recovery charge, Q_{rr}.

Advantages of the CoolSiC™ MOSFET

- The CoolSiC™ MOSFET technology offers chips, discretes, and modules, in different packages, voltage classes, and current ratings. This wide portfolio covers a wide range of applications and power ratings

With these advantages, the CoolSiC™ MOSFET brings many benefits to the system design including high reliability and improved efficiency. It enables high switching frequency and high power density, and reduces system complexity and total system costs.

4.5 Gate-oxide reliability of the CoolSiC™ MOSFET

The CoolSiC™ MOSFET normally targets high-power applications with high frequency and high voltage, which typically require the highest reliability. Besides the standard reliability topics, gate oxide is one of the most important concerns for the SiC MOSFET [6] [7].

The commercially available SiC MOSFETs have a relatively thin gate oxide to reduce the channel resistance. Therefore, the reliability of the gate oxide under high gate voltage scenarios must be investigated. For SiC MOSFETs, the main focus so far has been stability under reverse-bias stress due to the differing fields applied. In actual applications, however, the on-state stress on the oxide is much more severe in existing MOSFETs due to the thin oxide layers. Tests on commercial MOSFET products reveal that this issue is still a serious concern for applications in industrial systems.

Thanks to their specific trench structure, CoolSiC™ MOSFETs can increase the channel mobility and improve the gate-oxide reliability. The challenge of gate-oxide reliability of SiC MOSFET devices is to ensure a sufficiently low failure rate, including extrinsic defects, throughout the desired lifetime under a given operating conditions. Long-term tests were performed with a large number of CoolSiC™ MOSFETs to investigate the extrinsic gate-oxide failure rates referring to [2]. This experiment was done using two groups of 1000 discrete devices at 150°C, under constant gate-bias stress for three 100-day durations. The gate-source voltage was increased by +5 V after each 100-day period. The failure statistics fit well to the linear E-model. By extrapolating these results to an operating lifetime of 20 years for the device, the model predicts a failure rate of 0.2 ppm with the on-state operation of V_{GS} being +15 V. The experiment proved that the gate-oxide reliability of the CoolSiC™ MOSFET is similar to that of IGBTs. This matches well with typical industrial requirements.

5 Basics of the CoolSiC™ MOSFET power modules

Semiconductor power modules offer several advantages in terms of power density, thermal management, manufacturability, and reliability. Figure 17 shows the construction of a semiconductor power module.

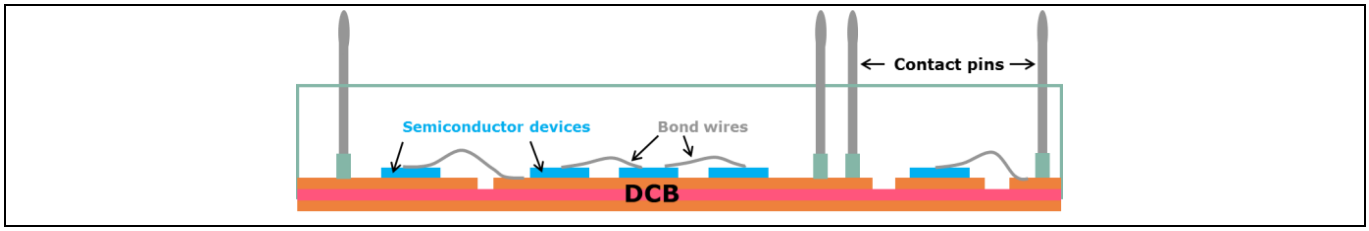


Figure 17 **The construction of a semiconductor power module**

The semiconductor power device is assembled on a substrate. The substrate of a power module has several functions:

- To isolate the power device from the heatsink/baseplate
- To transfer heat from the power device to the heatsink
- To connect several power devices in a circuit or parallel assembly

The power module's semiconductor chips are connected to the system via terminals at the top of the power module. Infineon power modules use solder or PressFIT pins as well as screw contact terminals. The connection of the devices with the terminals and the internal circuitry not ensured by the Direct Copper Bonded (DCB) is performed with bond wires. In contrast to the well-known standard packages with baseplates, the Easy module platform enables a highly symmetric, low-inductive design. The flexible pin grid of Easy modules simplifies the PCB layout and offers a stray inductance below 10 nH. The 62 mm package offers the possibility of a low-inductance connection of systems in the medium power range.

For assembly and mounting Instructions, please refer to Infineon's application note AN2023-07 for Easy PressFIT modules, and AN2012-05 for 62 mm modules.

5.1.1 Stray inductance

Probably the most important parasitic that has to be taken into account for developing a power electronic application is stray inductance. Stray inductances are a consequence of internal and external connections between the semiconductor devices and the power electronic system.

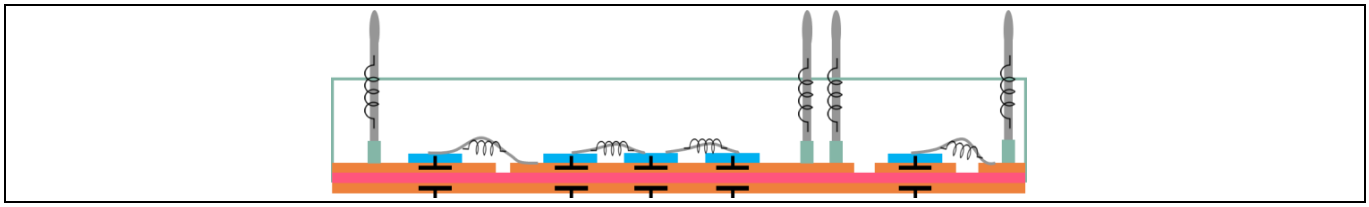


Figure 18 **The construction of a semiconductor power module with equivalent parasitic parameters**

During a switching event, the voltage drops along an inductor according to the following equation:

$$\Delta V = L \times di/dt.$$

This voltage drop has an influence on the turn-on and turn-off behavior of a power device. Figure 19 shows the turn-on and turn-off waveforms of a CoolSiC™ Easy power module.

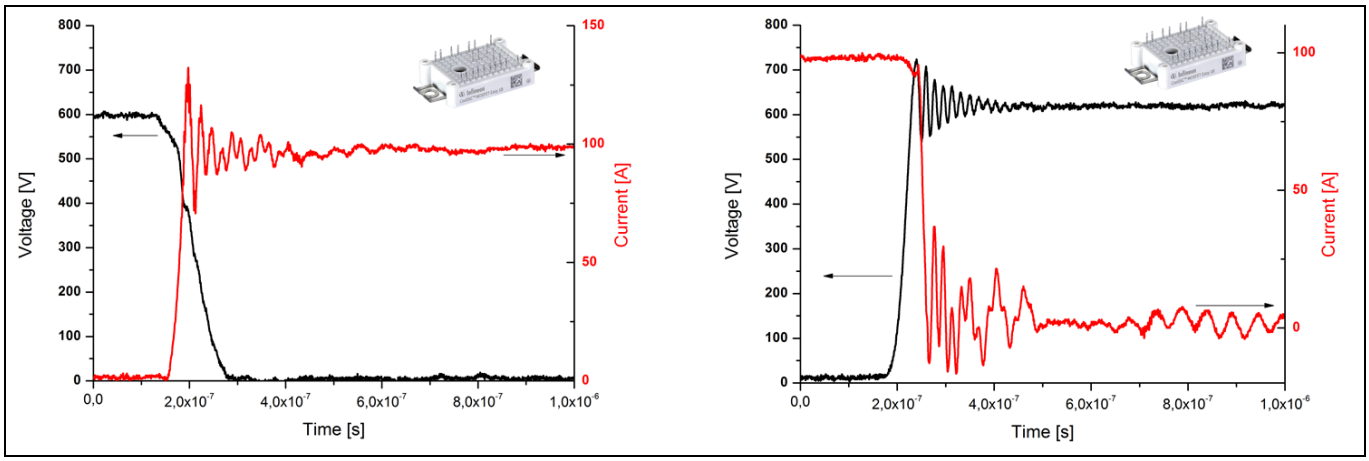


Figure 19 **Switching waveforms of a CoolSiC™ MOSFET Easy1B module**

The voltage drop during turn-on leads to a drop of V_{DS}, which drastically reduces the turn-on energy. During device turn-off, the voltage experiences a spike. If this voltage spike is larger than the device's breakdown voltage, the device will fail, and the power module will be destroyed. Therefore, device turn-off is a critical event to consider with respect to the stray inductance of power modules.

As the CoolSiC™ MOSFET is much faster than IGBTs in the same voltage class, power modules with large stray inductances (> 20 nH) limit the use of CoolSiC™ MOSFET power modules with respect to the maximum allowed switching speed and/or applied voltages. This is why CoolSiC™ MOSFET modules have to reduce the stray inductance as much as possible.

Infineon has a long experience in the development of low-inductive power modules. One example of low inductive modules is the EasyPACK™, shown in Figure 20.

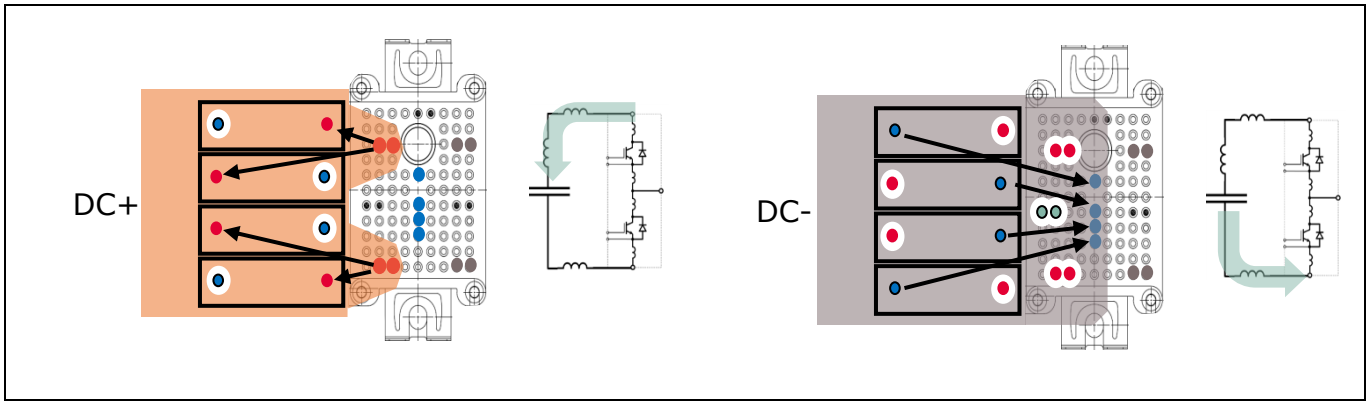


Figure 20 **CoolSiC™ MOSFET EasyPACK™ module**

The EasyPACK™ module uses a strip-line approach in a thin package leading to low stray inductances. This approach along with a smart module design were used to develop the CoolSiC™ MOSFET power modules with half-bridge, six-pack, or booster topologies, which lead to a stray inductance of only 9 nH. This low stray inductance allows for fast switching at high voltage. These modules can be configured for different inverter or rectifier topologies that target solar, EV charger, UPS, and other high-switching frequency converters.

6 Conclusion

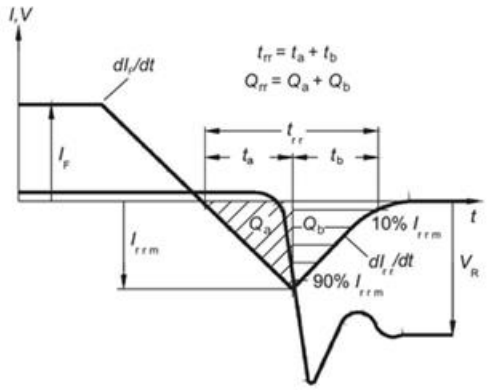
This application note presented the CoolSiC™ 1200 V SiC MOSFET including its features and the results of a performance characterization. Some general, practical design guidelines were highlighted for designing the CoolSiC™ MOSFET in a power system.

The tests discussed were performed with the CoolSiC™ 1200 V M1 SiC MOSFET. Although most of the information in this document holds true for newer trench generations also, please consult the respective datasheets and application notes for more details on the latest chip generations.

7 Glossary

$R_{ds(on)}$	The resistance at the actual junction temperature, given at the datasheet current I_{DS}
T_j	The temperature on the top of the chip where the power dissipation takes place (junction → pn-junction)
$V_{GS(th)}$	Voltage between the gate and the source at which current starts to flow, defined for $V_{GS} = V_{DS}$ and I_{DS} = 10 mA. This threshold voltage must always be measured after the device is brought to a defined state. Here, after V_{GS} = + 20 V, e.g., an IGSS at 20 V. Otherwise, due to the effects of hysteresis, this value differs
I_{DSS}	I_{DSS} (DSS = drain-source at shorted gate-source voltage = 0 V) is the leakage current whenever the switch is off at V_{GS} = 0 V and V_{DSS} = 1200 V
V_{GS}	The bias between the drain and source, corresponds to V_{ge} in an IGBT
I_{DS}	The load current flowing between drain and source. The value given in the datasheet is calculated by: $$I_{D,max} = \sqrt{\frac{T_{vj,max} - T_C}{R_{th(vj-c),max}} \frac{1}{R_{DS,on}}}$$
V_{DS}	The bias between the drain and source. Corresponds to V_{ce} in an IGBT
C_{rss}	The effective capacitance between the gate and drain. It is measured at 800 V which is the typical DC link voltage in an application. It equals the gate-drain capacitance
C_{gs}	The effective capacitance between source and gate
C_{iss}	The effective capacitance between the gate and source. It is measured at 800 V, which is the typical DC link voltage in an application. It equals the sum of gate-source capacitance and gate-drain capacitance
C_{gd}	The effective capacitance between the drain and gate
C_{oss}	The effective capacitance between the source and drain. It is measured at 800 V which is the typical DC link voltage in an application. It equals the sum of gate-drain capacitance and gate-source capacitance
C_{ds}	The effective capacitance between the source and drain
R_{G_int}	The effective internal gate resistance. It comprises the sum of the resistance of the distributed gate network and additional resistors added to the gate pad
E_{on}	The turn-on loss energy. It is measured according to the guidelines available for IGBTs
E_{off}	The turn-off loss energy. It is measured according to the guidelines available for IGBTs
E_{tot}	The total loss energy, i.e., the sum of E_{on} and E_{off}
Q_{rr}	The reverse-recovery charge. It is measured according to the guidelines known from the silicon pin diodes
I_{rrm}	The reverse-recovery current. See the following image:

Glossary

	
Q_{GD}	Typically the gate charge needed to pass the Miller plateau
Q_G	The total gate charge
$Q_{GS,pl}$	The gate charge required to reach the Miller from the off-state V_{GS}
R_G	The gate resistor applied externally. Adds to R_{G_int}
R_{G_on}	The externally applied gate resistor for turn-on in the case of separated sink and source outputs of a driver circuit/IC. Adds to R_{G_int}
R_{G_off}	The externally applied gate resistor for turn-off in the case of separated sink and source outputs of a driver circuit/IC. Adds to R_{G_int}

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Revision history

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Revision 1.0	2018-01-05	First release
Revision 1.1	2018-07-01	Various minor changes and additional information implemented in all paragraphs, Figure 8 revised
Revision 1.2	2024-06-05	Adjusted title and text with universal statements covering different SiC trench generations.

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