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Interfacing Cypress MoBL® Asynchronous Dual-Port to TI OMAP2420 Multimedia Processor

AN5056

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Associated Project: MoBL® Dual-Port SRAM

Associated Part Family: CYDM256B16/CYDM128B16/CYDM064B16/CYDM256A16/CYDM128A/CYDM064A16

Software Version: N/A

Associated Application Notes: N/A

Introduction

The Texas Instruments OMAP2420 is a low-power, high-performance multimedia application processor that supports all cellular standards, and complements any modem or chipset and any air interface. The OMAP2420 includes the benefits of the OMAP 2 architecture's parallel processing, giving users the ability to instantly run applications and operate multiple functions simultaneously without quality of service compromises. The OMAP2420 includes an integrated ARM1136 processor (330 MHz), a TI TMS320C55x™ DSP (220 MHz), 2D/3D graphics accelerator, imaging and video accelerator, high-performance system interconnects and industry-standard peripherals.

The OMAP2420 is targeted at streaming video, 2D/3D electronic gaming, video conferencing, video recording, audio, and high-resolution still-image capture that is used in 2.5G and 3G wireless terminals and high-performance PDAs.

The OMAP™ platform enables OEMs and ODMs to quickly bring to market devices featuring rich user interfaces, high processing performance, and long battery life through the maximum flexibility of a fully-integrated mixed-processor solution.

The OMAP2420 multimedia processor supports a General-purpose memory controller (GPMC) that readily connects to Cypress asynchronous Dual-Ports. This application note describes the wiring, GPMC register settings, and other design considerations for connecting the OMAP2420 multimedia processor to the 1/4-Mb Cypress MoBL® Dual-Port (CYDM256A16-55/CYDM256B16-55). The same design can be used in interfacing the OMAP2420 multimedia processor to other Cypress MoBL Dual-Ports in the x16 configuration, such as the CYDM128A16/CYDM128B16 and CYDM064A16/CYDM064B16.

General-Purpose Memory Controller (GPMC)

The Texas Instruments OMAP2420 multimedia processor supports two types of external memory interfaces: SDRC and GPMC. SDRC is primarily used to gluelessly interface the processor with SDRAMs, while the GPMC is used to interface to asynchronous and synchronous burst memories, such as NAND/NOR flashes and asynchronous SRAM. The GPMC is a 16-bit memory interface, and it can be configured to gluelessly interface to Cypress's low-power MoBL Dual-Ports.

The Cypress MoBL Dual-Port CYDM256A16/CYDM256B16 has a standard asynchronous SRAM interface. Table 1 lists the signal connections between the OMAP2420's GPMC and Cypress MoBL Dual-Port CYDM256A16/CYDM256B16. This is a 1.8V LVCMOS interface.

Table 1. GPMC & MoBL Dual-Port Signal Equivalents

OMAP2420 GPMC Signal (I/O)		MoBL Dual-Port Signal (I/O)		Function
GPMC.CSx	O	CE	I	Chip Select
GPMC.WE	O	R/W	I	Write Enable
GPMC.OE	O	OE	I	Output Enable
SDRC.D[3:0]	O	A[13:10]	I	Address
GPMC.A[10:1]	O	A[9:0]	I	Address
GPMC.D[15:0]	I/O	I/O[15:0]	I/O	Data
GPMC.BE[1]	O	UB	I	Upper Byte Enable
GPMC.BE[0]	O	LB	I	Lower Byte Enable

Layout Guidelines

Figure 1 below shows the physical wiring between the OMAP2420 multimedia processor and the MoBL Dual-Port CYDM256A16/CYDM256B16. Either port of the Dual-Port may be used.

Figure 1. Wiring Diagram of OMAP2420 to CYDM256A16/CYDM256B16

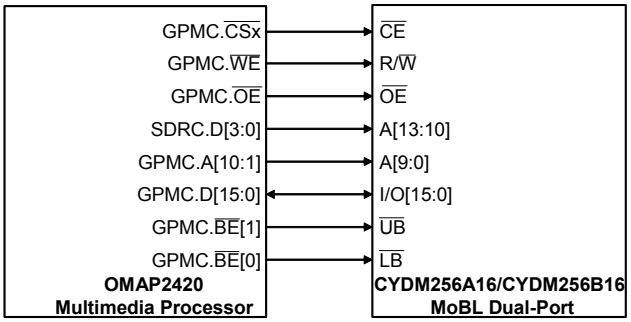

Table 2 shows the list of GPMC pins that are not required for the memory interface (optional).

Table 2. TI OMAP2420 GPMC Default Signal Connections

OMAP2420 GPMC Signal	Default
SDRC.D[15:4]	NC
GPMC.CLK	NC
GPMC.ADV	NC
GPMC.WP	NC
GPMC.IO_DIR	NC
GPMC.WAIT[3:0]	V_{SS}

Table 3 shows the list of MoBL Dual-Port pins that are not required for the memory interface (optional).

Table 3. Cypress MoBL DP Default Signal Connections

CYDM256A16/CYDM256B16 Signal	Default
SEM	V_{DD}
SFEN	V_{DD}
M/$\overline{S}$	V_{DD}
INT	NC
BUSY	NC
ODR[4:0]	NC

GPMC Register Settings

In order for the GPMC to properly interface to the Cypress MoBL Dual-Port, Table 4 shows the GPMC registers that need to be configured, while the rest of the registers can be left in their default states.

Table 4. GPMC Register Settings

Field	Value	Description
GPMC_CONFIG: GPMC Configuration Register		
LIMITED ADDRESS	0b	Limited address device support
GPMC_CONFIG1_x: Signal Control Configuration Register		
READMULTIPLE	0b	Selects the read single or multiple access
READTYPE	0b	Selects the read mode operation
WRITETYPE	0b	Selects the write mode operation
WAITREAD MONITORING	0b	Selects the WAIT monitoring configuration for read accesses
WAITWRITE MONITORING	0b	Selects the WAIT monitoring configuration for write accesses
DEVICESIZE	01b	Selects the device size attached
DEVICETYPE	00b	Selects the attached device type
MUXADDDATA	0b	Enables the address and data multiplexed protocol
TIMEPARAGRANULARITY	0b	Signals timing latencies scalar factor
GPMC_CONFIG2_x: $\overline{CSx}$ Timing Configuration Register		
CSWROFFTIME	00111b	$\overline{CSx}$ deassertion time from start-cycle time for write accesses
CSRDOFFTIME	01000b	$\overline{CSx}$ deassertion time from start-cycle time for read accesses
CSEXTRADELAY	0b	$\overline{CSx}$ adds half GPMC_FCLK cycle
CSONTIME	0000b	$\overline{CSx}$ assertion time from start-cycle time

Table 4. GPMC Register Settings (Continued)

Field	Value	Description
GPMC_CONFIG4_x: $\overline{WE}$/$\overline{OE}$ Timing Configuration Register		
WEOFFTIME	00111b	$\overline{WE}$ deassertion time from start-cycle time
WEEXTRADELAY	0b	$\overline{WE}$ adds half GPMC_FCLK cycle
WEONTIME	0000b	$\overline{WE}$ assertion time from start-cycle time
OEOFFTIME	01000b	$\overline{OE}$ deassertion time from start-cycle time
OEEXTRADELAY	0b	$\overline{OE}$ adds half GPMC_FCLK cycle
OEONTIME	0000b	$\overline{OE}$ assertion time from start-cycle time
GPMC_CONFIG5_x: Access/Cycle Time Configuration Register		
ACCESSTIME	00111b	Delay between start-cycle time and first data valid
WRCYCLETIME	00111b	Total write cycle time
RDCYCLETIME	01000b	Total read cycle time
GPMC_CONFIG6_x: Cycle2Cycle and BusTurnAround Configuration Register		
CYCLE2CYCLEDELAY	0001b	Chip-select high pulse delay between two successive accesses
CYCLE2CYCLESAMECSEN	1b	Adds Cycle2CycleDelay between two successive accesses to the same chip-select
GPMC_CONFIG7_x: Chip-Select Address Mapping Configuration Register		
CSVALID	1b	Chip-select x enable

In order to arrive at the register settings shown above, assume the system clock GPMC_FCLK runs at its maximum frequency of 100 MHz. Please note that this setting may vary depending on the speed of the desired memory interface as well as the speed of the system clock. Given most timing parameters of the OMAP processor are specified with a range of guaranteed values, the timing analysis below uses the worst-case values, and the register settings takes into account the timing margin required for successful operations. The following section provides a brief explanation for each of the register settings.

GPMC_CONFIG - GPMC Configuration Register

LIMITED ADDRESS - No limit is placed on the maximum address size of the memory device (0b).

GPMC_CONFIG1_x - Signal Control Configuration Register

READMULTIPLE - The MoBL Dual-Port does not support burst read operation; thus, all reads are single (0b).

READTYPE - The MoBL Dual-Port is an asynchronous device that supports asynchronous read operation only (0b).

WRITETYPE - The MoBL Dual-Port is an asynchronous device that supports asynchronous write operation only (0b).

WAITREADMONITORING - The wait pins are not used for read operation (0b).

WAITWRITEMONITORING - The wait pins are not used for write operation (0b).

DEVICESIZE - The MoBL Dual-Port CYDM256A16 and CYDM256B16 have a 16-bit data bus (01b).

DEVICETYPE - The MoBL Dual-Port is an asynchronous SRAM, which has a NOR flash-like interface (0b).

MUXADDDATA - The MoBL Dual-Port does not support multiplexed address and data bus operation (0b).

TIMEPARAGRANULARITY - The MoBL Dual-Port can operate with regular timing parameters without having to use a latency scalar (0b).

GPMC_CONFIG2_x - $\overline{CSx}$ Timing Configuration Register

CSWROFFTIME - This is the number of GPMC_FCLK cycles from start-cycle time to $\overline{CSx}$ deassertion for write operation. The value of this register needs to satisfy the minimum write cycle time of the MoBL Dual-Port (00111b). Please refer to the write timing example in the next section of this application note.

CSRDOFFTIME - This is the number of GPMC_FCLK cycles from start-cycle time to $\overline{CSx}$ deassertion for read operation. The value of this register needs to satisfy the minimum read cycle time of the MoBL Dual-Port (01000b). Please refer to the read timing example in the next section of this application note.

CSEXTRADELAY - Adding a half-cycle delay to the $\overline{CSx}$ signal is not required for the MoBL Dual-Port interface (0b).

CSONTIME - This is the number of GPMC_FCLK cycles from start-cycle time to $\overline{CSx}$ assertion. This is at the beginning of the read or write cycle (0000b).

GPMC_CONFIG4_x - $\overline{WE}$/$\overline{OE}$ Timing Configuration Register

WEOFFTIME - This is the number of GPMC_FCLK cycles from start-cycle time to $\overline{WE}$ deassertion for write operation. The value of this register needs to satisfy the minimum write cycle time of the MoBL Dual-Port (00111b). Please refer to the write timing example in the next section of this application note.

WEEXTRADELAY - Adding a half-cycle delay to the $\overline{WE}$ signal is not required for the MoBL Dual-Port interface (0b).

WEONTIME - This is the number of GPMC_FCLK cycles from start-cycle time to $\overline{WE}$ assertion. This is at the beginning of the write cycle (0000b).

OEOFFTIME - This is the number of GPMC_FCLK cycles from start-cycle time to $\overline{OE}$ deassertion for read operation. The value of this register needs to satisfy the minimum read cycle time of the MoBL Dual-Port (01000b). Please refer to the read timing example in the next section of this application note.

OEEXTRADELAY - Adding a half-cycle delay to the $\overline{OE}$ signal is not required for the MoBL Dual-Port interface (0b).

OEONTIME - This is the number of GPMC_FCLK cycles from start-cycle time to $\overline{OE}$ assertion. This is at the beginning of the read cycle (0000b).

GPMC_CONFIG5_x - Access/Cycle Time Configuration Register

ACCESSTIME - This is the number of cycles from the beginning of a read cycle to first valid data on the data bus (00111b).

WRCYCLETIME - This is the number of GPMC_FCLK cycles of a single write operation (00111b). Please refer to the write timing example in the next section of this application note.

RDCYCLETIME - This is the number of GPMC_FCLK cycles of a single read operation (01000b). Please refer to the read timing example in the next section of this application note.

GPMC_CONFIG6_x - Cycle2Cycle and BusTurnAround Configuration Register

CYCLE2CYCLEDELAY - This is the number of GPMC_FCLK cycles inserted between two successive accesses (0001b).

CYCLE2CYCLESAMCSEN - CYCLE2CYCLEDELAY is added for successive accesses from the same chip-select (1b).

GPMC_CONFIG7_x - Cycle2Cycle and BusTurnAround Configuration Register

CSVALID - This enables this chip-select for the MoBL Dual-Port interface (1b).

GPMC control and configurations can be done dynamically. GPMC ensures that a new CS configuration takes effect only when no access is requested (CS idle). To prevent inconsistency and critical behavior, the GPMC configuration must be done by MPU software while other masters are inactive.

For more information about GPMC register settings, please see OMAP2410 and OMAP2420 *Multimedia Processors Technical Reference Manual*, TI literature number SWPU064A, December 2004.

Timing Considerations

This section of the application note provides a sample timing analysis of read and write operations with the TI OMAP2420 multimedia processor and Cypress MoBL Dual-Port CYDM256A16-55/CYDM256B16-55.

Read Operation

With a GPMC reference clock (GPMC_FCLK) of 100 MHz (10-ns period), the register setting required to initiate proper read operation is shown in Table 4. RdCycleTime, which defines the length of a read cycle, needs to be set to 01000b GPMC_FCLK. Thus, a single read cycle is 80 ns. Figure 2 shows the timing details of a read operation between the OMAP2420 and MoBL Dual-Port.

The signal names for the OMAP processor and the MoBL Dual-Port are shown on the left. Timing parameters for the OMAP2420 are shown with an uppercase T, while parameters for the MoBL Dual-Port are shown with a lowercase t. Please refer to Table 5 for timing parameter definitions.

Figure 2. Read Timing

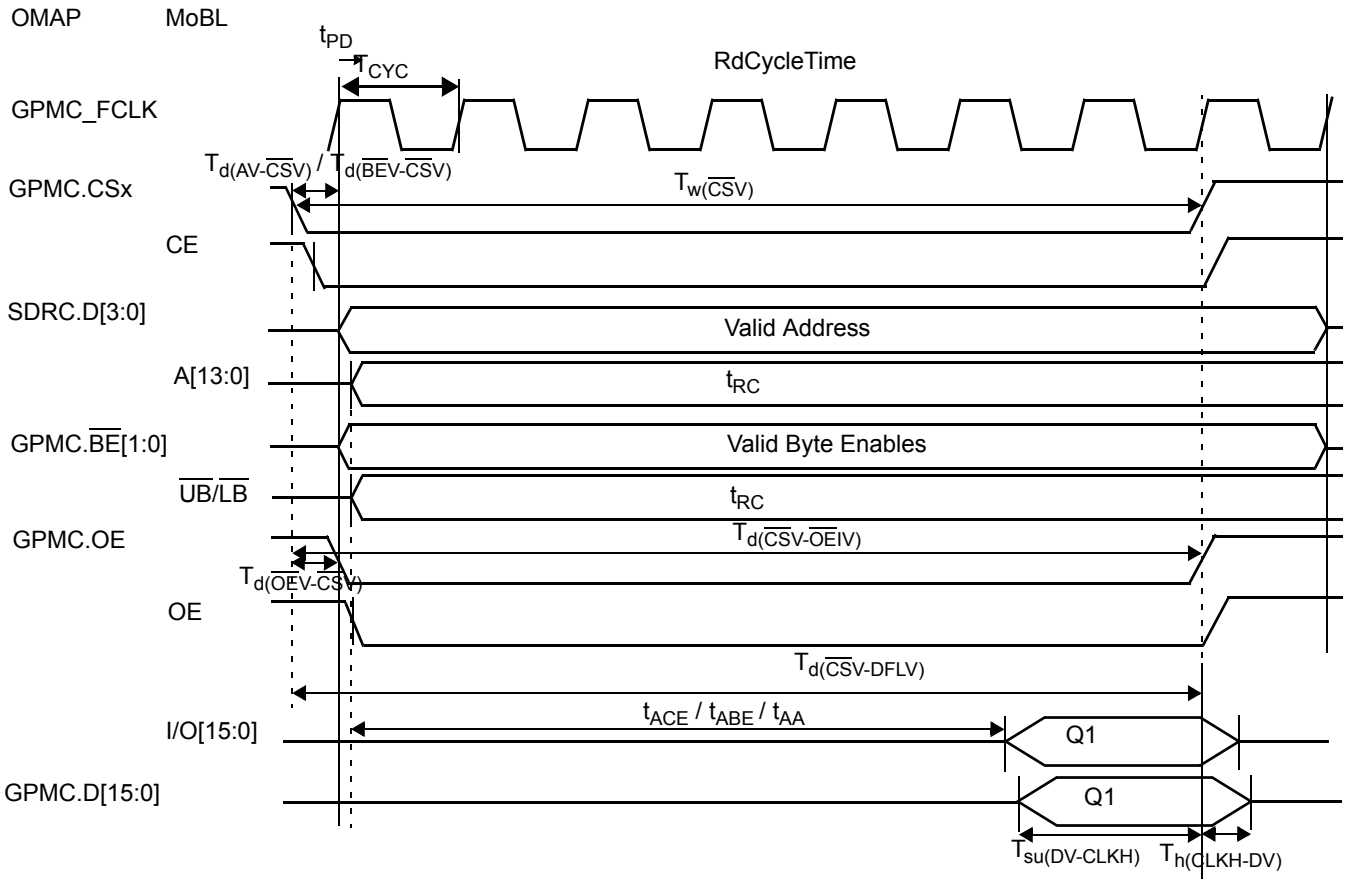

Table 5. Read Timing Parameters

Symbol	Part	Description	Min. (ns)	Max. (ns)
t_{PD}	PCB	Board propagation delay	1	
T_{CYC}	OMAP	GPMC_FCLK period	10	
$T_{W(\overline{CSV})}$	OMAP	GPMC.$\overline{CSx}$ low duration	75	80
$T_{d(AV\text{-}\overline{CSV})}$	OMAP	Delay, Address valid to GPMC.$\overline{CSx}$ low	–5	0
$T_{d(\overline{BEV}\text{-}\overline{CSV})}$	OMAP	Delay, GPMC.$\overline{BEx}$ valid to GPMC.$\overline{CSx}$ low	–5	0
$T_{d(\overline{OEV}\text{-}\overline{CSV})}$	OMAP	Delay, GPMC.$\overline{OE}$ low to GPMC.$\overline{CSx}$ low	–5	0
$T_{d(\overline{CSV}\text{-}\overline{OEIV})}$	OMAP	Delay, GPMC.$\overline{CSx}$ low to GPMC.$\overline{OE}$ high	75	80
$T_{d(\overline{CSV}\text{-}DFLV)}$	OMAP	Access time, from GPMC.$\overline{CSx}$ low to data latching clock edge	65	70
$T_{su(DV\text{-}CLKH)}$	OMAP	Set-up, read data valid before input data latching edge	2	–
$T_{h(CLKH\text{-}DV)}$	OMAP	Hold, read data valid after input data latching edge	1	–
t_{RC}	DP	Read cycle time	55	–
t_{ABE}	DP	Bye enable access time	–	55
t_{ACE}	DP	$\overline{CE}$ low to data valid	–	55
t_{AA}	DP	Address to data value	–	55

The following timing analysis is based on the OMAP2420 GPMC running at 100 MHz with a Cypress MoBL Dual-Port CYDM256A16-55/CYDM256B16-55.

Propagation Delay

Propagation delay (t_{PD}) is the board flight time between the OMAP2420 multimedia processor and the MoBL Dual-Port. This delay is important to take into account. A 3-inch FR-4

strip-line generates 0.528 ns delay (176 ps/inch delay) between the OMAP processor and the Dual-Port. The board propagation delay will vary for different board designs, and as a conservative assumption, 1 ns is used for this application note. Assume all signals going from OMAP2420 to the MoBL Dual-Port to have the same trace length and thus the same propagation delay. The only propagation delay that will be added is for the data coming back from the Dual-Port to the OMAP processor during a read operation.

Worst-Case Analysis

Since most timing parameters are specified with a range of guaranteed values, it is possible to perform a worst-case timing analysis using the tightest timing budget provided by the data sheets of the two devices. Referring to Figure 2, the worst-case parameters are shown in Table 6.

Table 6. Worst Case Timing Parameters for Read

Symbol	Worst-Case (ns)	Explanation
$T_{W(\overline{CS}V)}$	75	Shortest $\overline{CE}$ period
$T_{d(AV\text{-}\overline{CS}V)}$	–5	Earliest $\overline{CE}$ assertion
$T_{d(\overline{BE}V\text{-}\overline{CS}V)}$	–5	Earliest $\overline{CE}$ assertion
$T_{d(\overline{OE}V\text{-}\overline{CS}V)}$	–5	Slowest $\overline{OE}$ assertion
$T_{d(\overline{CS}V\text{-}\overline{OE}IV)}$	75	Shortest $\overline{OE}$ assertion
$T_{d(\overline{CS}V\text{-}DFLV)}$	65/70	Minimum setup/hold time
$T_{su(DV\text{-}CLKH)}$	2	Minimum set-up
$T_{h(CLKH\text{-}DV)}$	1	Minimum hold
t_{RC}	55	Minimum read cycle
t_{ABE}	55	Slowest access time
t_{ACE}	55	Slowest access time
t_{AA}	55	Slowest access time

Address and Byte Enables

The read cycle timing window needs to be at least t_{RC} as required by the MoBL Dual-Port. This means the address, byte enables, chip-select and other control signals need to be valid for at least 55 ns for a successful read. With the OMAP2420, both the address and byte enables remain valid for the entire read cycle defined by the RDCYCLETIME field in the GPMC_CONFIG5_x register (80 ns). Thus, the t_{RC} requirement is satisfied by both the valid address and byte enable signals.

Chip-Select and Output Enable

In the worst-case scenario, GPMC.$\overline{CS}$x is asserted 5 ns prior to the start of the read cycle and holds valid for a shortest period of 75 ns. Essentially, this means the “effective read cycle” is only 70 ns. This still satisfies the MoBL Dual-Port’s t_{RC} minimum requirement of 55 ns. The output enable signal (GPMC.$\overline{OE}$) is defined with reference to the assertion of the GPMC.$\overline{CS}$x signal. The worst-case scenario happens when the output enable signals are asserted $T_{d(\overline{OE}V\text{-}\overline{CS}V)}$ (5 ns) after the assertion of GPMC.$\overline{CS}$x, and they are deasserted $T_{d(\overline{CS}V\text{-}\overline{OE}IV)}$ (75 ns) after the initial GPMC.$\overline{CS}$x assertion. That is, the GPMC.$\overline{CS}$x and GPMC.$\overline{OE}$ are deasserted at the same time. Please refer to Figure 2 for details.

Data

The data is read from the MoBL Dual-Port with a certain access time after the address (t_{AA}), output enable (t_{DOE}), and chip or byte enables (t_{ACE} or t_{ABE}) become valid. In this case, all control signals (address, output enable, chip-select, byte enables) are valid at the beginning of the read cycle (time zero). With MoBL Dual-Port’s maximum access time requirement of $t_{AA} = t_{ABE} = t_{ACE} = 55$ ns, the MoBL Dual-Port will provide the data 55 ns after the beginning of a read cycle. The data will propagate back to the OMAP2420 processor and this incurs another 2 ns of propagation delay to the overall timing. That is, the data will arrive at the OMAP2420 processor $t_{DATAVALIDSTART}$ (57 ns) after the beginning of the read cycle ($t_{PD} \times 2 = 2$ ns, as the data needs to propagate back to the OMAP2420). Since all control signals will be valid for the first 70 ns in the read cycle, the data, for the worst case, will also hold at the OMAP2420 processor for least $t_{DATAVALIDEND}$ (72 ns).

For the OMAP2420 processor, its minimum read data set-up and hold time requirements are $T_{su(DV\text{-}CLKH)}$ (2 ns) and $T_{h(CLKH\text{-}DV)}$ (1 ns), respectively. The data becomes valid 57 ns after the beginning of a read cycle, and it remains valid until the end of the “effective read cycle” time of 70 ns (when chip-select and output enable are de-asserted). At the instant that data is latched into the OMAP2420 multimedia processor, the data setup and hold time needs to be satisfied.

$T_{d(\overline{CS}V\text{-}DFLV)}$ defines the time that data gets latched into the OMAP2420 processor with respect to the assertion of the chip-select signal. In this case, by setting ACCESSTIME field in the GPMC_CONFIG5_x register to 00111b (70 ns), the value of $T_{d(\overline{CS}V\text{-}DFLV)}$ ranges from 65 ns to 70 ns.

To find the worst-case for set-up time:

$T_{su(DV\text{-}CLKH)} \leq (T_{d(\overline{CS}V\text{-}DFLV)min} + T_{d(AV\text{-}\overline{CS}V)}) - t_{DATAVALIDSTART}$

$2 \text{ ns} \leq (65 \text{ ns} + (-5 \text{ ns})) - 57 \text{ ns}$

$2 \text{ ns} \leq 3 \text{ ns}$ (True)

To find the worst-case for hold time:

$T_{h(CLKH\text{-}DV)} \leq t_{DATAVALIDEND} - (T_{d(\overline{CS}V\text{-}DFLV)max} + T_{d(AV\text{-}\overline{CS}V)})$

$1 \text{ ns} \leq 72 \text{ ns} - (70 \text{ ns} + (-5 \text{ ns}))$

$1 \text{ ns} \leq 7 \text{ ns}$ (True)

Write Operation

Similar to the read operation, the write operation runs on the same internal GPMC_FCLK reference clock of 100 MHz. The register setting required to initiate proper write operation is shown in Table 4. WrCycleTime, which defines the length of a write cycle, needs to be set to 00111b GPMC_FCLK. Thus, a single write cycle is 70 ns. Figure 3 shows the timing details of a write operation between the OMAP2420 and MoBL Dual-Port.

The timing diagram in Figure 3 demonstrates a write operation between the OMAP2420 multimedia processor and the MoBL Dual-Port. The following analysis is based on the timing parameters for the Cypress CYDM256A16-55/CYDM256B16-55. Table 7 lists the parameters as specified by the data sheets of the two devices.

Figure 3. Write Timing

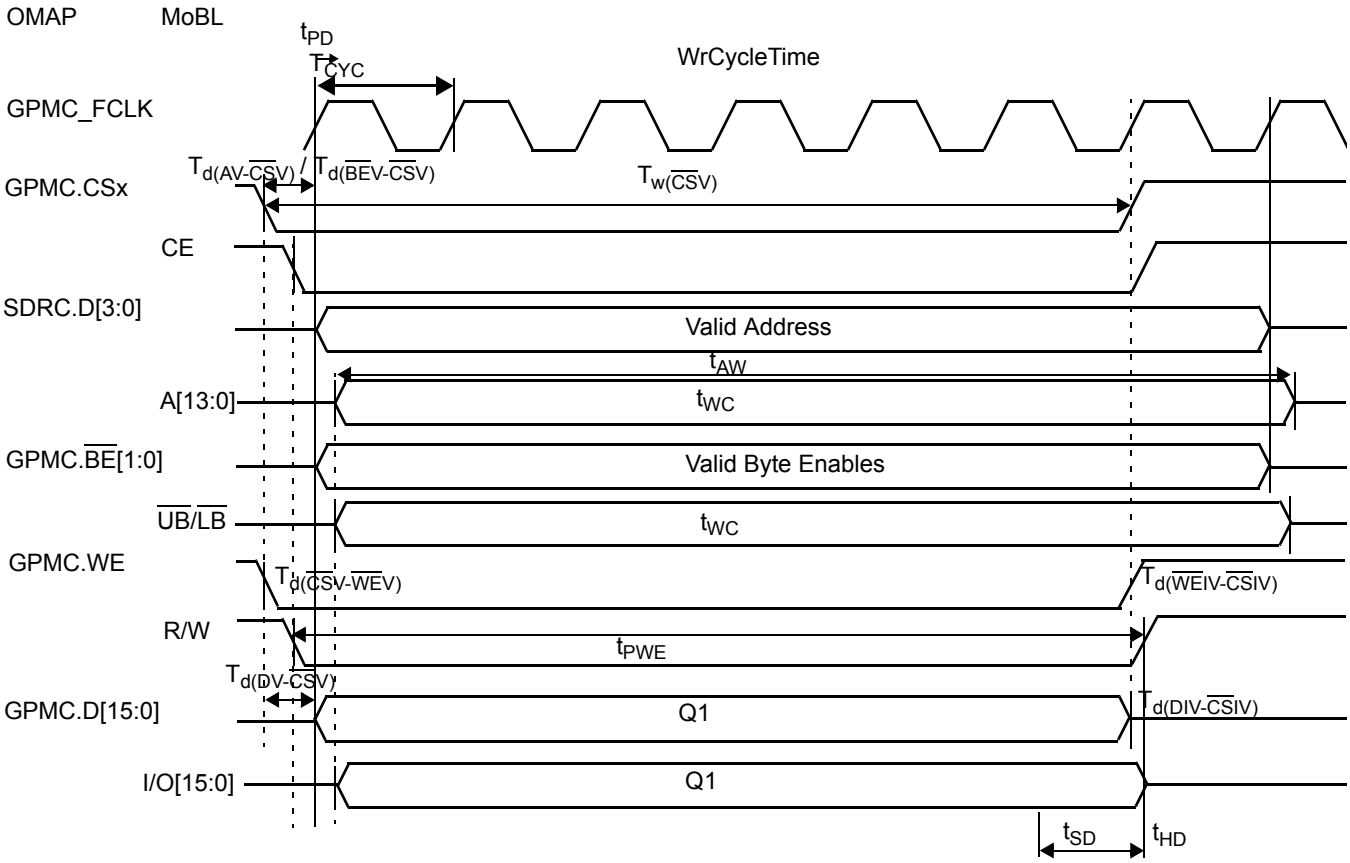

Table 7. Write Timing Parameters

Symbol	Part	Description	Min (ns)	Max (ns)
t_{PD}	PCB	Board propagation delay	1	
T_{CYC}	OMAP	REF_CLK period	10	
$T_{W(\overline{CSV})}$	OMAP	GPMC.$\overline{CSx}$ low duration	65	70
$T_{d(AV\text{-}\overline{CSV})}$	OMAP	Delay, Address valid to GPMC.$\overline{CSx}$ low	–5	0
$T_{d(\overline{BEV}\text{-}\overline{CSV})}$	OMAP	Delay, GPMC.$\overline{BEx}$ valid to GPMC.$\overline{CSx}$ low	–5	0
$T_{d(\overline{CSV}\text{-}\overline{WEV})}$	OMAP	Delay, GPMC.$\overline{CSx}$ low to GPMC.$\overline{WE}$ low	–5	0
$T_{d(\overline{WEIV}\text{-}\overline{CSIV})}$	OMAP	Delay, GPMC.$\overline{WE}$ high to GPMC.$\overline{CSx}$ high	–5	0
$T_{d(DV\text{-}\overline{CSV})}$	OMAP	Delay, data bus valid to GPMC.$\overline{CSx}$ low	–5	0
$T_{d(DIV\text{-}\overline{CSIV})}$	OMAP	Delay, data bus invalid to GPMC.$\overline{CSx}$ high	–5	0

Table 7. Write Timing Parameters (Continued)

Symbol	Part	Description	Min (ns)	Max (ns)
t_{WC}	DP	Write cycle time	55	-
t_{AW}	DP	Address valid to write end	45	-
t_{PWE}	DP	Write pulse width	40	-
t_{SD}	DP	Data set-up to write end	30	-
t_{HD}	DP	Data hold from write end	0	-

The following timing analysis is based on the OMAP2420 GPMC running at 100 MHz with a Cypress MoBL Dual-Port CYDM256A16-55/CYDM256B16-55.

Worst Case Analysis

The single write timing analysis is similar to the one done for the read operation. Referring to Figure 3, the worst case parameters are shown in Table 8.

Table 8. Worst Case Timing Parameters for Write

Symbol	Worst Case (ns)	Explanation
$T_{W(\overline{CSV})}$	65	Shortest $\overline{CE}$ period
$T_{d(AV\text{-}\overline{CSV})}$	–5	Earliest $\overline{CE}$ assertion
$T_{d(\overline{BE}V\text{-}\overline{CSV})}$	–5	Earliest $\overline{CE}$ assertion
$T_{d(\overline{CSV}\text{-}\overline{WEV})}$	0	Slowest WE assertion
$T_{d(\overline{WE}IV\text{-}\overline{CSI}V)}$	0	Shortest WE period
$T_{d(DV\text{-}\overline{CSV})}$	-5	Slowest data valid
$T_{d(DIV\text{-}\overline{CSI}V)}$	0	Shortest data valid period
t_{WC}	55	Minimum write cycle
t_{AW}	45	Minimum address enable to write end
t_{PWE}	40	Minimum write pulse width
t_{SD}	30	Minimum data set-up time
t_{HD}	0	Minimum data hold time

Address and Byte Enables

The write cycle timing window needs to be at least t_{WC} as required by the MoBL Dual-Port. This means the address, byte enables, chip-select and other control signals need to be valid for at least 55 ns for a successful write operation. With the OMAP2420 processor, both the address and byte enables remain valid for the entire write cycle defined by the WRCYCLETIME field in the GPMC_CONFIG5_x register (70 ns). Thus, this requirement is satisfied by both the valid address and byte enable signals.

Chip-Select

In the worst-case scenario, GPMC.$\overline{CSx}$ is asserted 5 ns prior to the start of the write cycle and holds valid for a shortest period of 65 ns. Essentially, this means the “effective write cycle” is only 60 ns (with valid control signals). This still satisfies the MoBL Dual-Port’s minimum requirement of 55 ns. Please refer to Figure 3 for details.

Data

The data is written into the MoBL Dual-Port on the rising edge of the R/$\overline{W}$ signal, and this needs to satisfy both the minimum address valid to R/$\overline{W}$ deassertion time (t_{AW}) and the minimum write pulse width (t_{PWE}) requirements. The minimum t_{AW} required from the Dual-Port is 45 ns and the GPMC supplies 70 ns (address valid for entire write cycle), which satisfies the requirement. On the other hand, the minimum write pulse width is satisfied, because $T_{W(\overline{CSV})} - T_{d(\overline{WE}IV\text{-}\overline{CSI}V)} - T_{d(\overline{CSV}\text{-}\overline{WEV})}$ = 65 ns – 0 ns – 0 ns = 65 ns.

The minimum write set-up and hold time required by the MoBL Dual-Port is defined by t_{SD} and t_{HD}, respectively. These parameters are in reference to the time before and after the deassertion of the R/$\overline{W}$ signal. According to the worst case parameters, the data will be valid $T_{d(DV\text{-}\overline{CSV})}$ with reference to the assertion of GPMC.$\overline{CSx}$ and becomes invalid $T_{d(DIV\text{-}\overline{CSI}V)}$ with reference to the deassertion of GPMC.$\overline{CSx}$. This satisfies the t_{SD} set-up time, as the available set-up time is $T_{W(\overline{CSV})} - T_{d(WEIV\text{-}\overline{CSI}V)}$ = 65 ns – 0 ns = 65 ns $\geq$ 30 ns, and the available hold time is $T_{d(\overline{WE}IV\text{-}\overline{CSI}V)}$ = 0 ns $\geq$ 0 ns (worst-case).

Conclusion

Systems using a TI OMAP2420 multimedia processor can easily benefit from the performance and flexibility of a Cypress Dual-Port. As one of the industry’s lowest power consuming Dual-Ports, designing in the Cypress MoBL Dual-Port allows the customer to interconnect multiple processors in a system, where power is of the most concern, and without having to compromise in performance. In addition, as this application note has shown, the interface between the TI OMAP2420 and Cypress MoBL Dual-Ports does not require any glue logic, which will save valuable board spaces.

For further information, please visit the Cypress web site at www.cypress.com. The web site also provides the latest data sheets, models, and any related documentation.

References

1. Cypress Semiconductor, CYDM256A16, CYDM128A16, CYDM064A16, CYDM128A08, CYDM064A08 1.8 V 4K/8K/16K x16 and 8K/16K x8 MoBL® Dual-Port Static RAM Data sheet, May 2005.
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Document History Page

Document Title: Interfacing Cypress MoBL® Asynchronous Dual-Port to TI OMAP2420 Multimedia Processor
Document Number: 001-16632

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1200303	HKH	01/27/2008	New Application Note
*A	3130712	HKH	01/07/2011	No technical updates. Updated as per new application note template.
*B	4285347	HKH	02/18/2014	Obsolete spec.

n March of 2007, Cypress recataloged all of its Application Notes using a new documentation number and revision code. This new documentation number and revision code (001-xxxxx, beginning with rev. **), located in the footer of the document, will be used in all subsequent revisions

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