32-bit Security Controller – V15 / 32-bit Security Controller – V02

SLx16 / SLx17

Integration Guide

Key features

- Up to 240 KB (32-bit Security Controller – V15) / 800 KB (32-bit Security Controller – V02) SOLID FLASH™ NVM
- Up to 12 KB (32-bit Security Controller – V15) / 20 KB (32-bit Security Controller – V02) user RAM
- 32-bit architecture based on the Arm® SecurCore® SC300 enhanced by Infineon Technologies' security technology
- Supported interfaces: UART, GPIO

About this document

Scope and purpose

This document provides the information on the SMD packages, connectivity and technical data required for integration of the product(s) listed. Further functionalities and interfaces supported by the product(s) but not related to integration are not fully described. Each Infineon Technologies customer is permitted to incorporate information concerning packages and electrical characteristics contained herein into its data books. When doing so, the customer is also requested to identify those features of the Infineon hardware used in its solution products (i.e., Infineon Technologies hardware + third-party firmware/operating system) and concretize this information where possible. Examples of OS-dependent values are **operational** and **standby currents** of the solution product.

Intended audience

This document is intended for device integrators and board manufacturers.

Table of contents

1 Introduction

This document describes the interfaces of the security controller to provide device integrators and board manufacturers useful information regarding its connectivity and technical data.

2 Connectivity

This chapter explains the schematics of the product and gives some recommendations as to how the controller can be externally connected.

2.1 Power supply schematic

The following figure illustrates how the security controller is to be supplied.

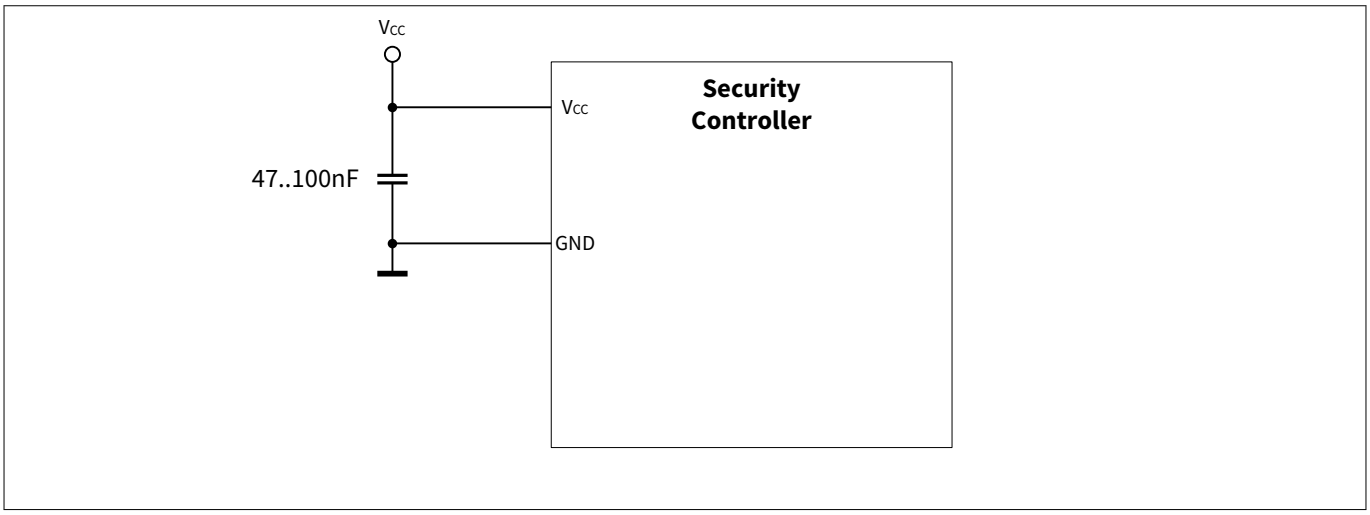

Figure 1 Power supply diagram

Contrary to other areas of application in which different types of capacitors are switched in parallel to stabilize the power supply, here normally only one capacitor is required. This is due to the wide variation limits of the supply voltage and the additional internal measures to handle sudden changes in load. For this decoupling capacitor, use a ceramic type with a low equivalent series resistance.

2.2 Initial delivery state: Flash Loader operation

The product is delivered in its first life cycle to operate the Flash Loader, which becomes active after powering up the device.

The Flash Loader supports the following interface(s):

- ISO/IEC 7816-3 card interface

The Flash Loader configuration defines the following features:

- A fixed pin-out
- A fixed protocol for the associated interface (based on an Infineon Technologies proprietary protocol):
  - ISO/IEC 7816-3 card
- A fixed command set (Flash Loader commands)

Flash Loader ISO/IEC 7816-3 card operation mode

The following communication parameters apply to the data transfer:

- Direct convention
- 8 data bits
- Even parity
- 2 stop bits
- Character repetition enabled
- Block guard time disabled
- Frame checking disabled

When the Flash Loader is active and a reset occurs, the protocol driver transmits the Flash Loader Answer To Reset (ATR) selected by the customer when ordering the chip:

1. ’3B 10 96’ (Standard ATR) indicates
   - ’Negotiable Protocol Mode’
   - Communication via T=0 with the minimum UART clock division factor ’16’. For a terminal clock of 10 MHz, the division factor ’16’ effects a maximum data rate of 625 kbaud (3.5712 MHz and clock division factor ’16’: 223.2 kbaud).

     Note: For compatibility reasons, a PPS negotiation with clock division factor ’8’ will be accepted by the protocol driver.

   - ’No Clock Stop’
   - ’Class A’ chip

2. ’3B 10 97’ offers the same operation parameters, but accepts the minimum UART clock division factor ’8’. That allows a maximum data rate of 1250 kbaud in the case of a 10-MHz terminal clock frequency.

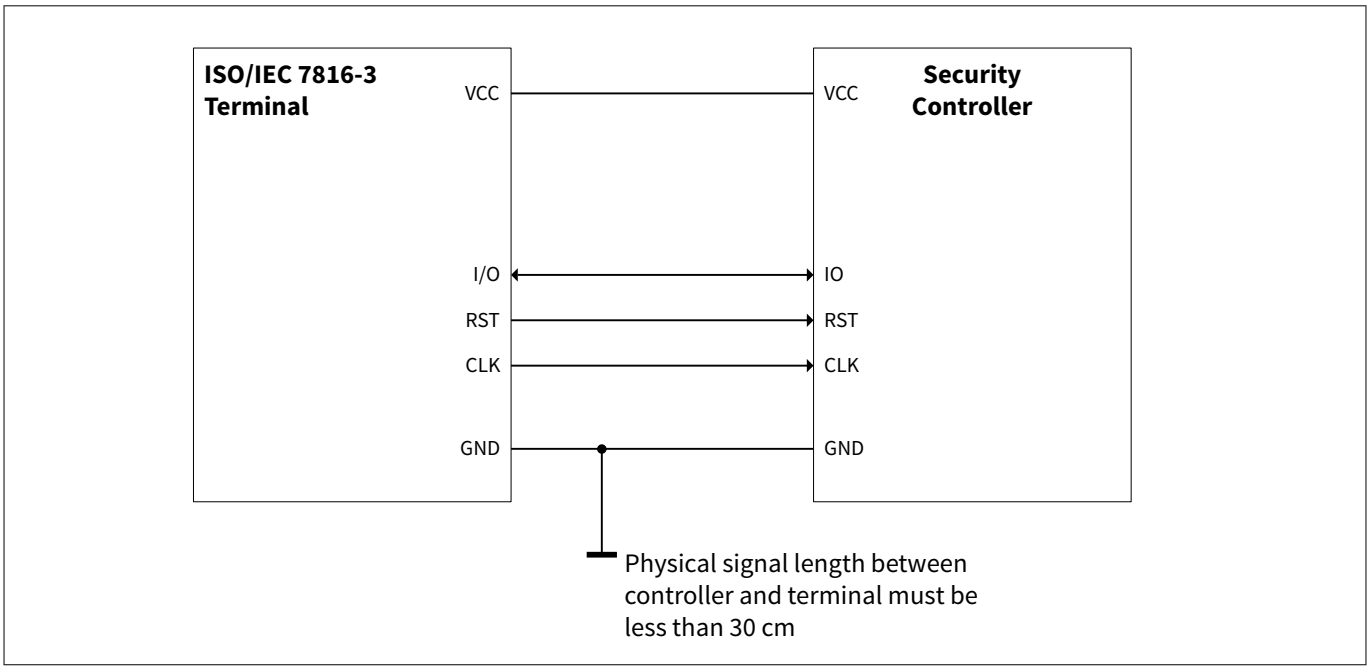

Figure 2 ISO/IEC 7816-3 card interface schematic diagram

The figure illustrates how the ISO/IEC 7816-3 terminal is to be connected to the security controller.

Table 1 UART: Flash Loader signal to symbol reference

Symbol	Flash Loader signal name	Signal function / remarks
GPIO0.2	UART_RST	UART chip reset signal (active low)
GPIO0.0	UART_CLK	UART clock signal
GPIO0.1	UART_IO	UART bi-directional data signal
VCC	VDD	Chip power and pad supply
GND	GND	Common ground reference

2.3 Final product configuration: pinout, signal and interface characteristics defined by OS

The OS loaded via the Flash Loader can configure a variety of product characteristics. This also includes which interfaces are connected to which pins. In this regard, the following sections give general guidelines on how power pins and interface signals should be connected in the system.

2.3.1 Interfaces

This section shows how the interfaces are to be connected.

2.3.1.1 ISO/IEC 7816-3 card

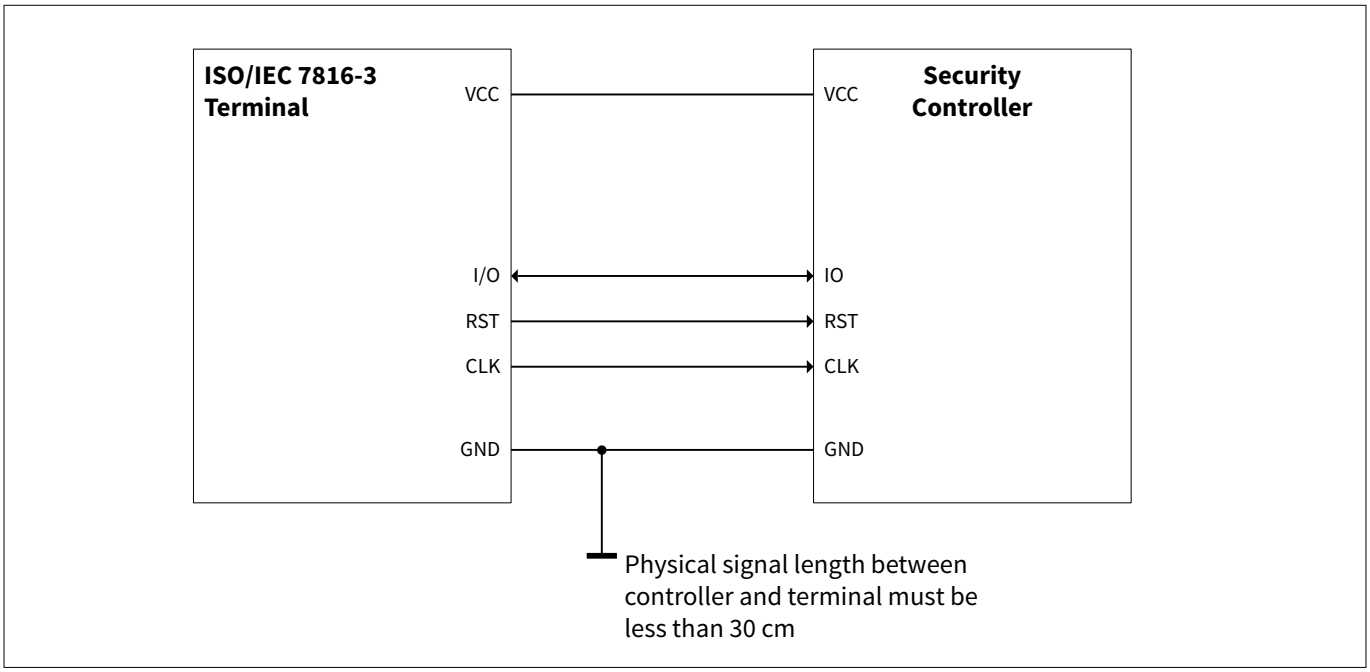

Figure 3 ISO/IEC 7816-3 card interface schematic diagram

The figure illustrates how the ISO/IEC 7816-3 terminal is to be connected to the security controller.

2.3.1.2 GPIO

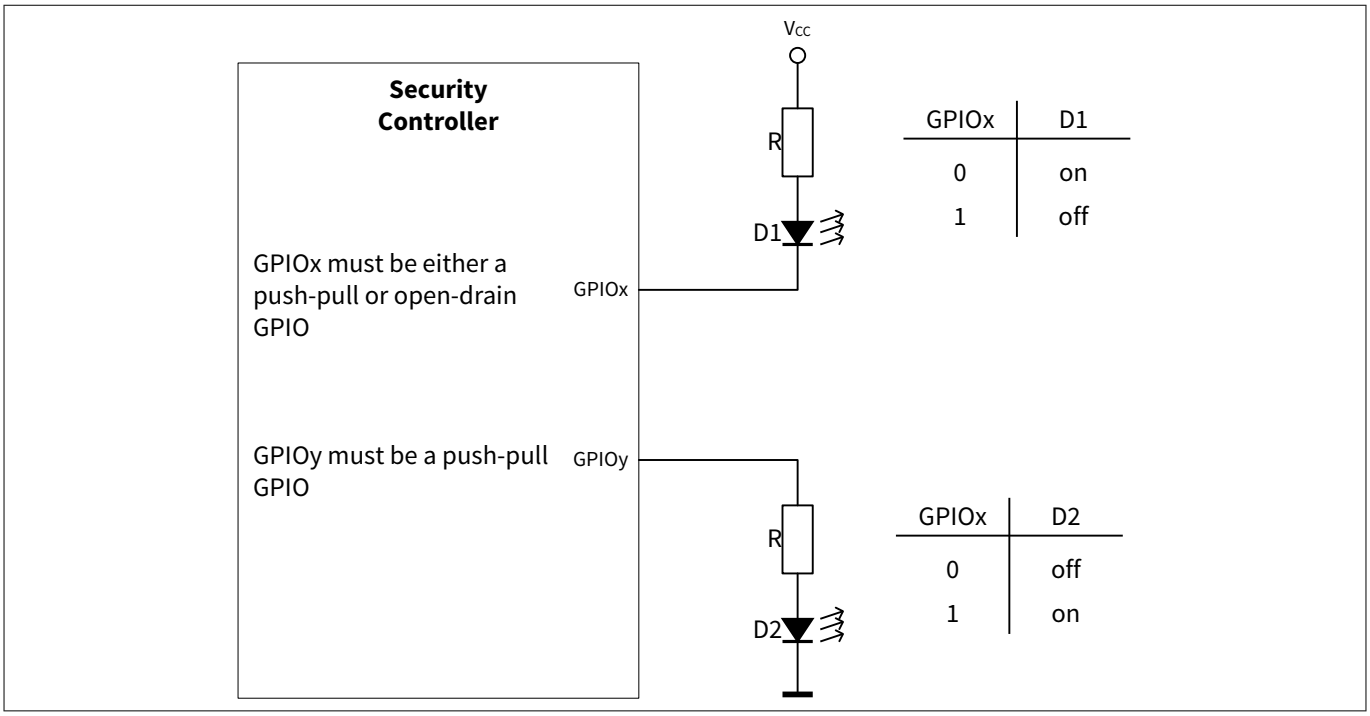

Figure 4 GPIO connectivity

The figure illustrates how GPIO is to be connected to the security controller. Refer to ***GPIO interface characteristics*** for electrical characteristics of the interface.

3 Description of delivery forms

This chapter provides information about available delivery forms and how the product's interfaces are assigned to the package pins.

For further information on compliance of the packages with European Parliament Directives, see ***RoHS compliance***.

For details and recommendations on the assembly of packages on PCBs, please see:

http://www.infineon.com/cms/en/product/technology/packages

3.1 External connectivity

Package pins are usually connected to a product pad and are used as inputs, outputs, or bi-directionally, depending on the available input and output stages. However in some products pins are not connected internally for example. The abbreviations listed here are used in the package description to classify each pin.

Table 2 Abbreviations for pin type

Abbreviation	Description
I	Input. Digital levels
O	Output. Digital levels
I/O	I/O is a bi-directional signal
PWR	Power
GND	Ground
NC	Not connected (JEDEC Standard). May be connected externally

Table 3 Abbreviations for buffer type

Abbreviation	Description
GPIO_I	GPIO input pad
GPIO_IO	GPIO input / output pad Open-drain/push-pull for output configurable Pull-up/pull-down configurable

3.2 SMD packages

The following packages are available:

- PG-USON-6-2 (for V02 controller only)
- PG-USON-8-5 (for V15 controller only)
- PG-USON-8-6 (for V02 controller only)
- PG-USON-10-2
- PG-VQFN-8-4 (for V02 controller only)

Note: It is recommended to connect the exposed die pad to the common ground reference (GND) for heat distribution.

The figures in the sections below show the following aspects of the package:

- Package outline: shows the package dimensions of the controller in the individual packages
- Package footprint: shows footprint recommendations
- Tape and reel packing
- Sample marking pattern: describes the productive sample marking pattern on the package
- Package layout: shows a simple layout with the pin numbers described in the pad-to-signal reference section

Note: Unless specified otherwise, all figure dimensions are given in mm.

Note: The drawings are for information only and not drawn to scale. More detailed information about package characteristics and assembly instructions is available on request.

3.2.1 PG-USON-6-2

Package outline

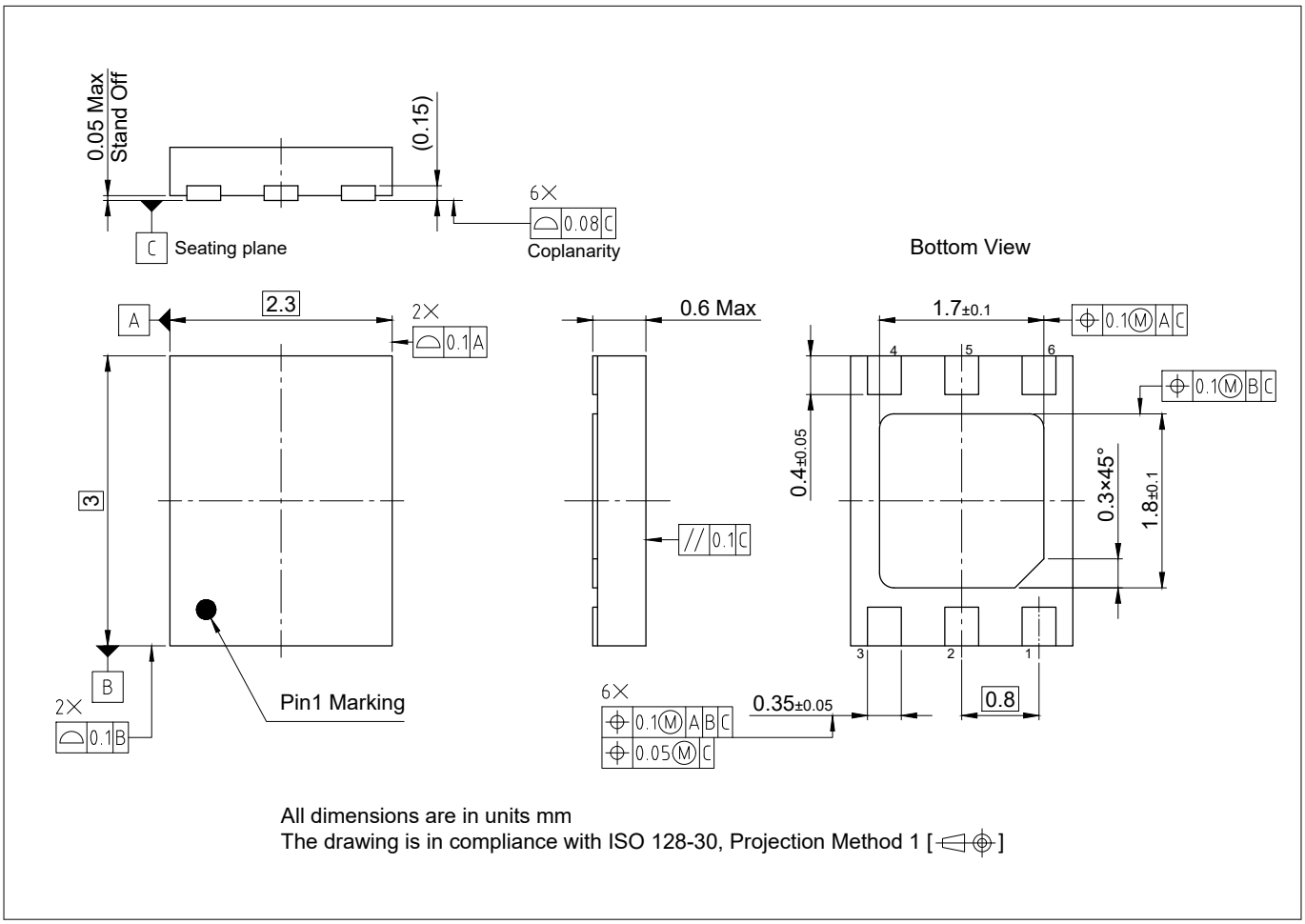

Figure 5 PG-USON-6-2 package outline

3 Description of delivery forms

Package footprint

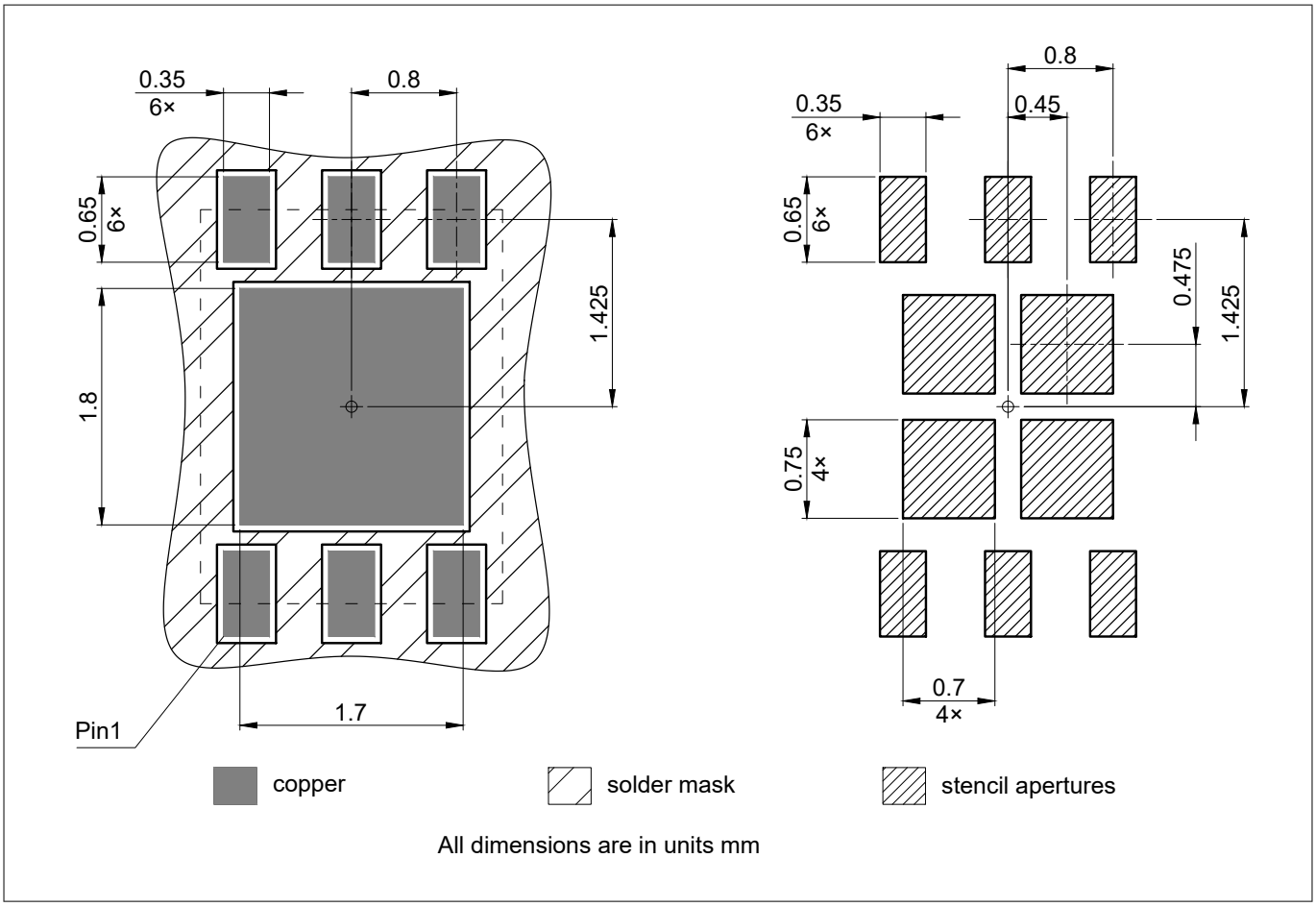

Figure 6 PG-USON-6-2 package footprint

Tape & reel packing

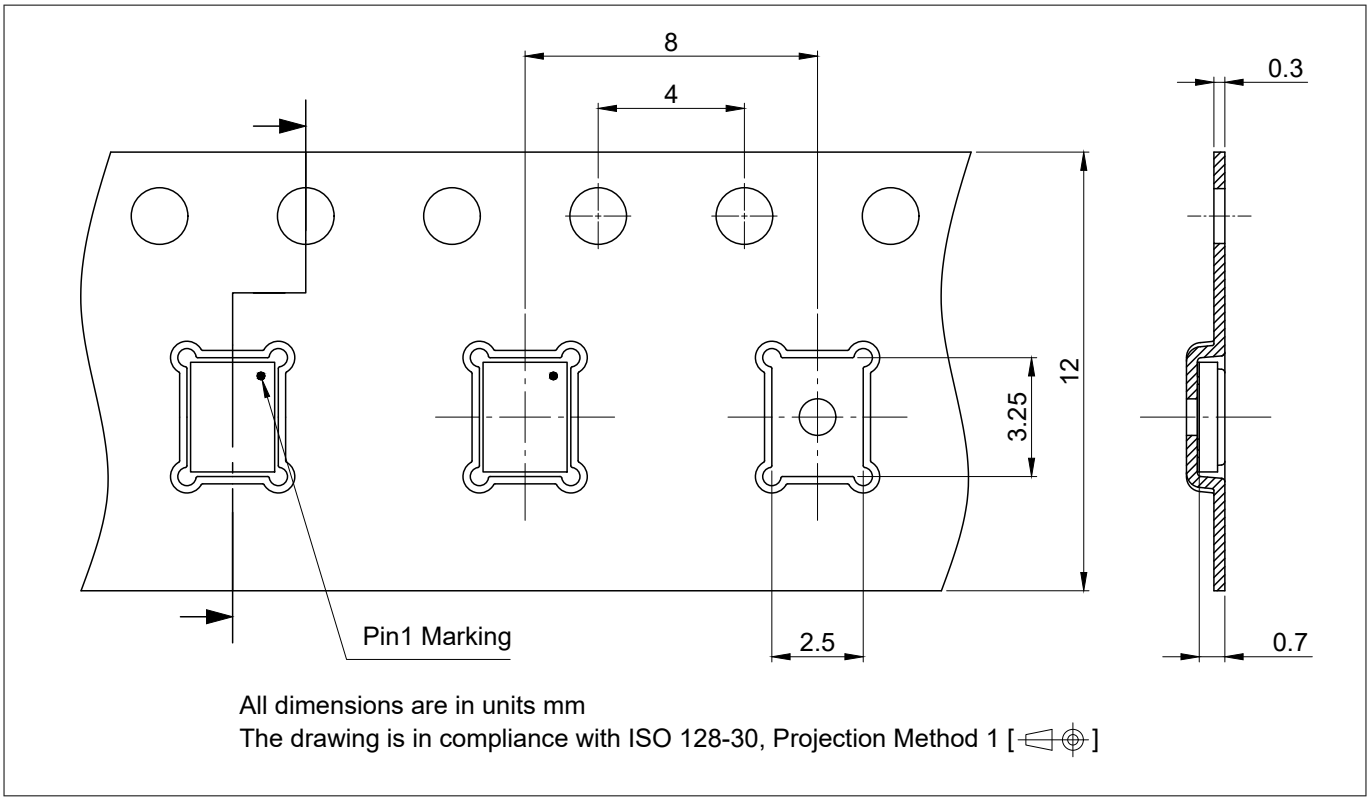

Figure 7 PG-USON-6-2 tape & reel packing

Production sample marking pattern

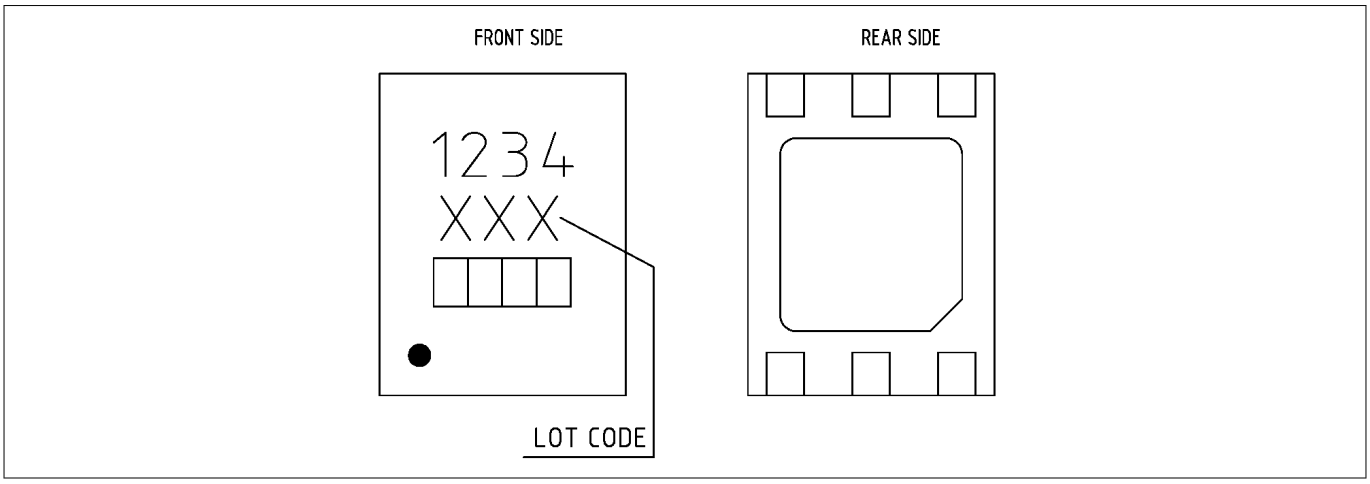

Figure 8 PG-USON-6-2 sample marking pattern

The dot indicates pin 01 for the chip. The following table describes the sample marking pattern:

Table 4 Marking table for PG-USON-6-2 packages

Indicator	Description
XXX	Lot code, defined and inserted during fabrication, issued by the packaging site

Table 4 Marking table for PG-USON-6-2 packages (continued)

Indicator	Description
1234	Type code: "123<N> • <N>: hardware derivative number
□□□□	Engineering samples: “E<YWW>”: • Engineering Sample • <Y>: 2nd digit of production year • <WW>: production week Qualified production parts: “<YYWW>”: • <YY>: production year • <WW>: production week

Package layout

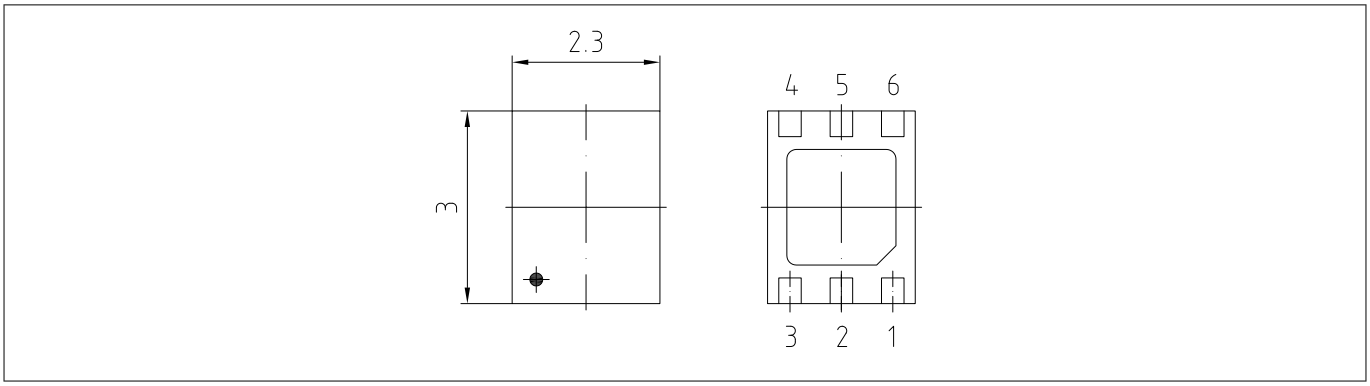

Figure 9 PG-USON-6-2 package layout

Pad-to-signal reference

Table 5 Pad-to-signal reference for PG-USON-6-2

Pad	Symbol	Pin type	Buffer type	Signal function / remarks
01	GND	GND	–	**Power supply:** Common ground reference (V_{SS})
02	NC	–	–	No internal connection / do not connect externally
03	GPIO0.1	I/O	GPIO_IO	**GPIO0.1:** SWIO usage **UART_IO:** ISO/IEC 7816-3 card usage
04	GPIO0.0	I	GPIO_I	**GPIO0.0:** SWIO usage **UART_CLK:** ISO/IEC 7816-3 card usage
05	GPIO0.2	I	GPIO_I	**GPIO0.2:** SWIO usage **UART_RST:** ISO/IEC 7816-3 card usage
06	VCC	PWR	–	**Power supply:** Chip power and pad supply (V_{CC})

3.2.2 PG-USON-8-5

Package outline

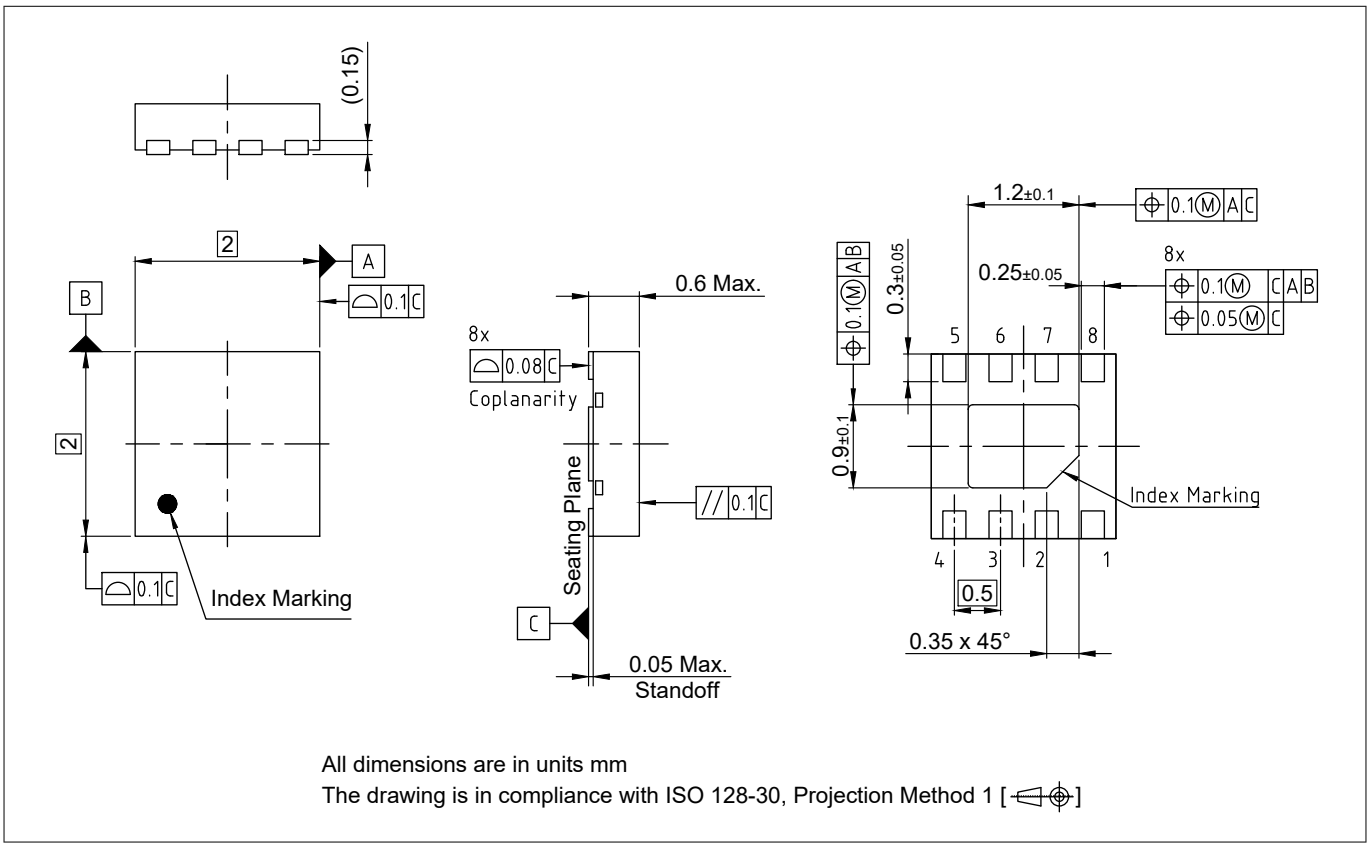

Figure 10 PG-USON-8-5 package outline

Package footprint

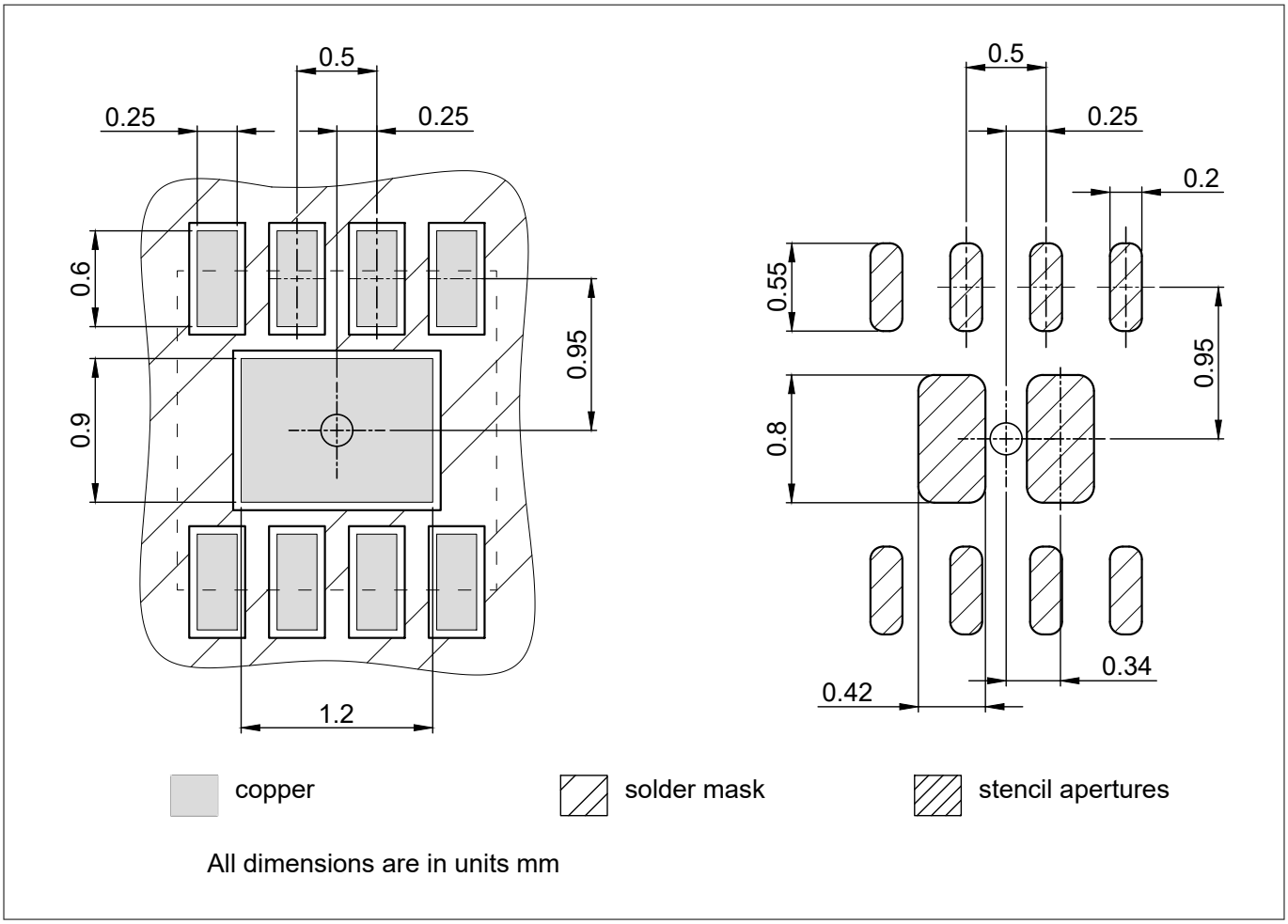

Figure 11 PG-USON-8-5 package footprint

Tape & reel packing

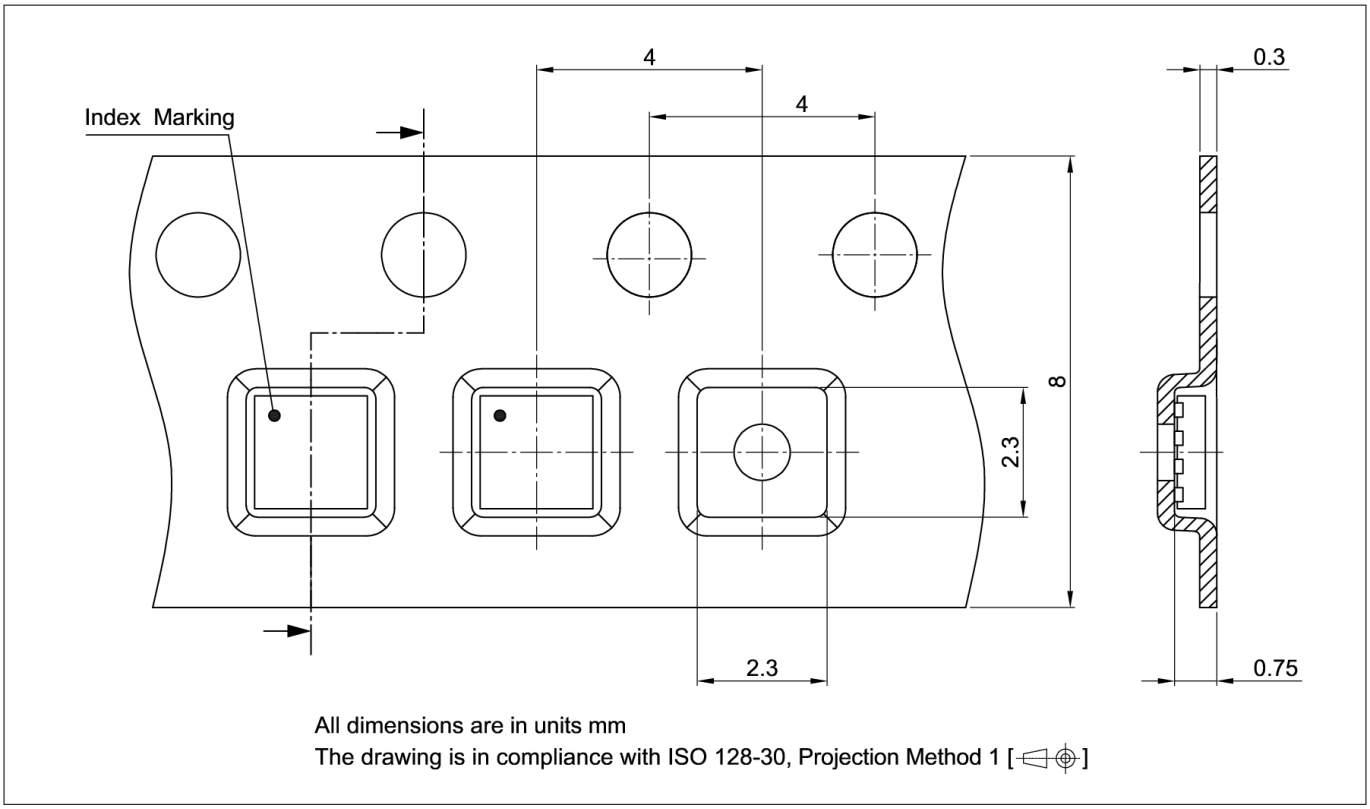

Figure 12 PG-USON-8-5 tape & reel packing

Production sample marking pattern

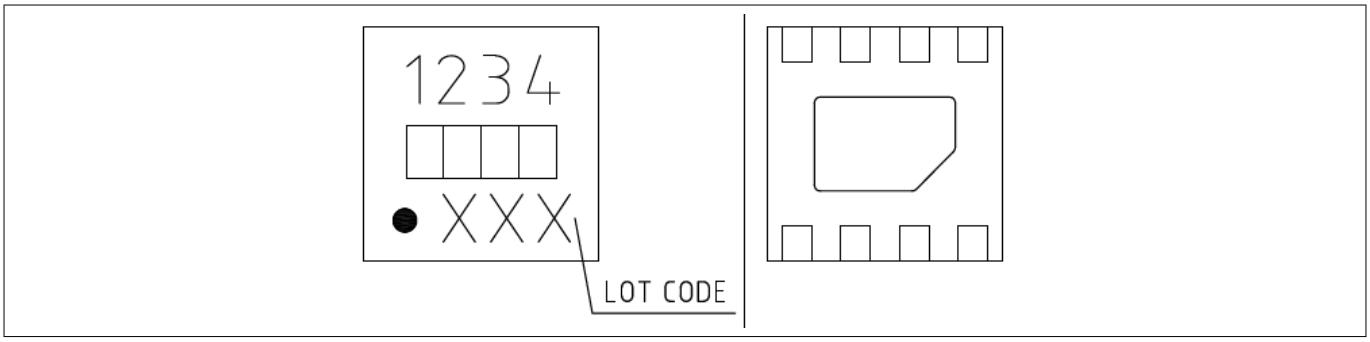

Figure 13 PG-USON-8-5 sample marking pattern

The dot indicates pin 01 for the chip. The following table describes the sample marking pattern:

Table 6 Marking table for PG-USON-8-5 packages

Indicator	Description
XXX	Lot code, defined and inserted during fabrication, issued by the packaging site
1234	Type code: "123<N>" • <N>: hardware derivative number
□□□□	• Engineering Sample

Table 6 Marking table for PG-USON-8-5 packages (continued)

Indicator	Description
	• <Y>: 2nd digit of production year • <WW>: production week Qualified production parts: “<YYWW>”: • <YY>: production year • <WW>: production week

Package layout

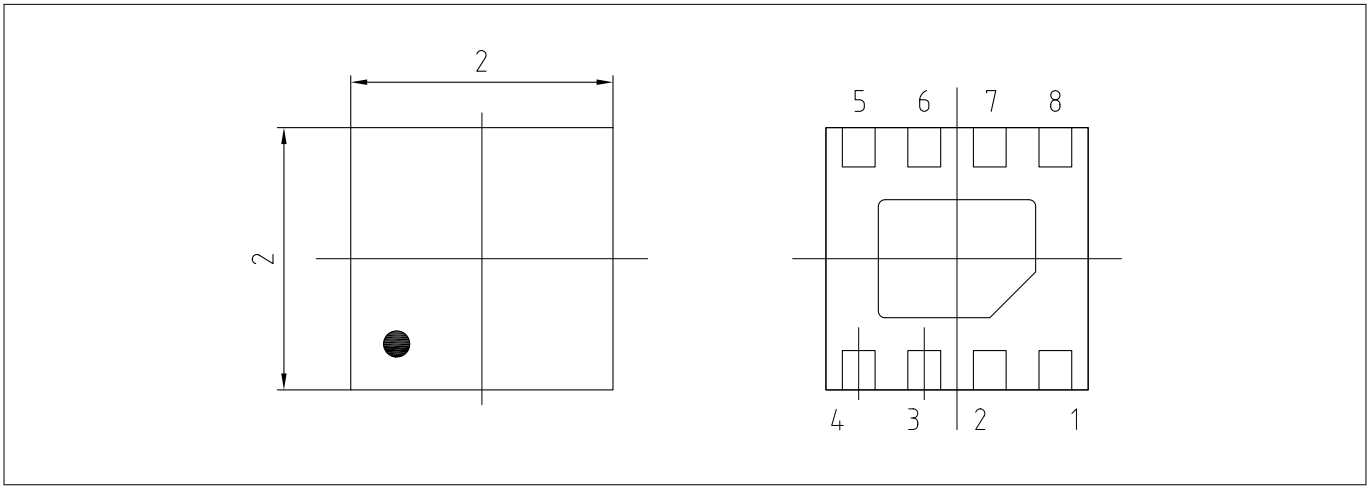

Figure 14 PG-USON-8-5 package layout

Pad-to-signal reference

Table 7 Pad-to-signal reference for PG-USON-8-5

Pad	Symbol	Pin type	Buffer type	Signal function / remarks
01	GND	GND	–	**Power supply:** Common ground reference (V_{SS})
02	NC	–	–	No internal connection / do not connect externally
03	GPIO0.1	I/O	GPIO_IO	**GPIO0.1:** SWIO usage **UART_IO:** ISO/IEC 7816-3 card usage
04	NC	–	–	No internal connection / do not connect externally
05	NC	–	–	No internal connection / do not connect externally
06	GPIO0.0	I	GPIO_I	**GPIO0.0:** SWIO usage **UART_CLK:** ISO/IEC 7816-3 card usage
07	GPIO0.2	I	GPIO_I	**GPIO0.2:** SWIO usage **UART_RST:** ISO/IEC 7816-3 card usage
08	VCC	PWR	–	**Power supply:** Chip power and pad supply (V_{CC})

3.2.3 PG-USON-8-6

Package outline

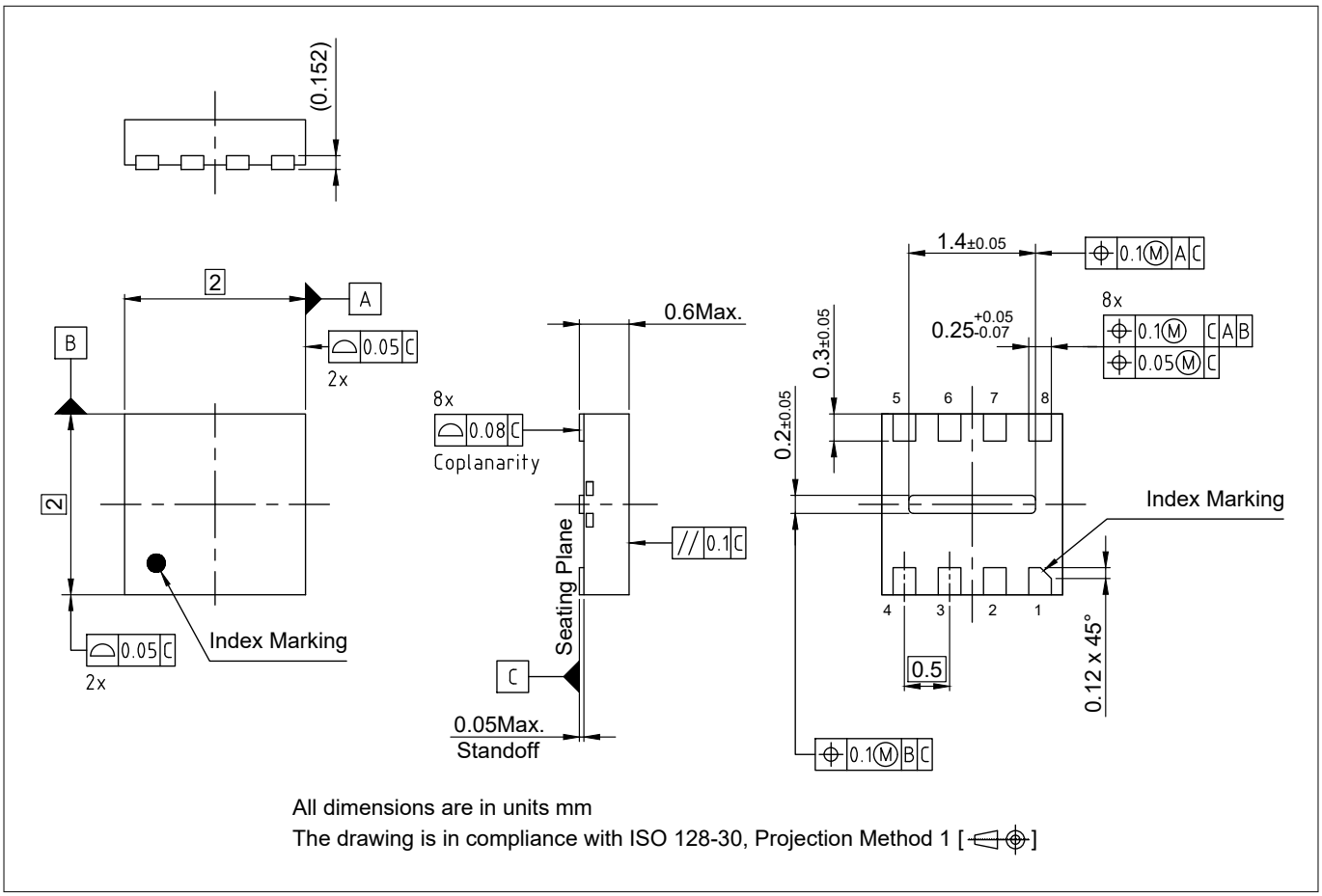

Figure 15 PG-USON-8-6 package outline

3 Description of delivery forms

Package footprint

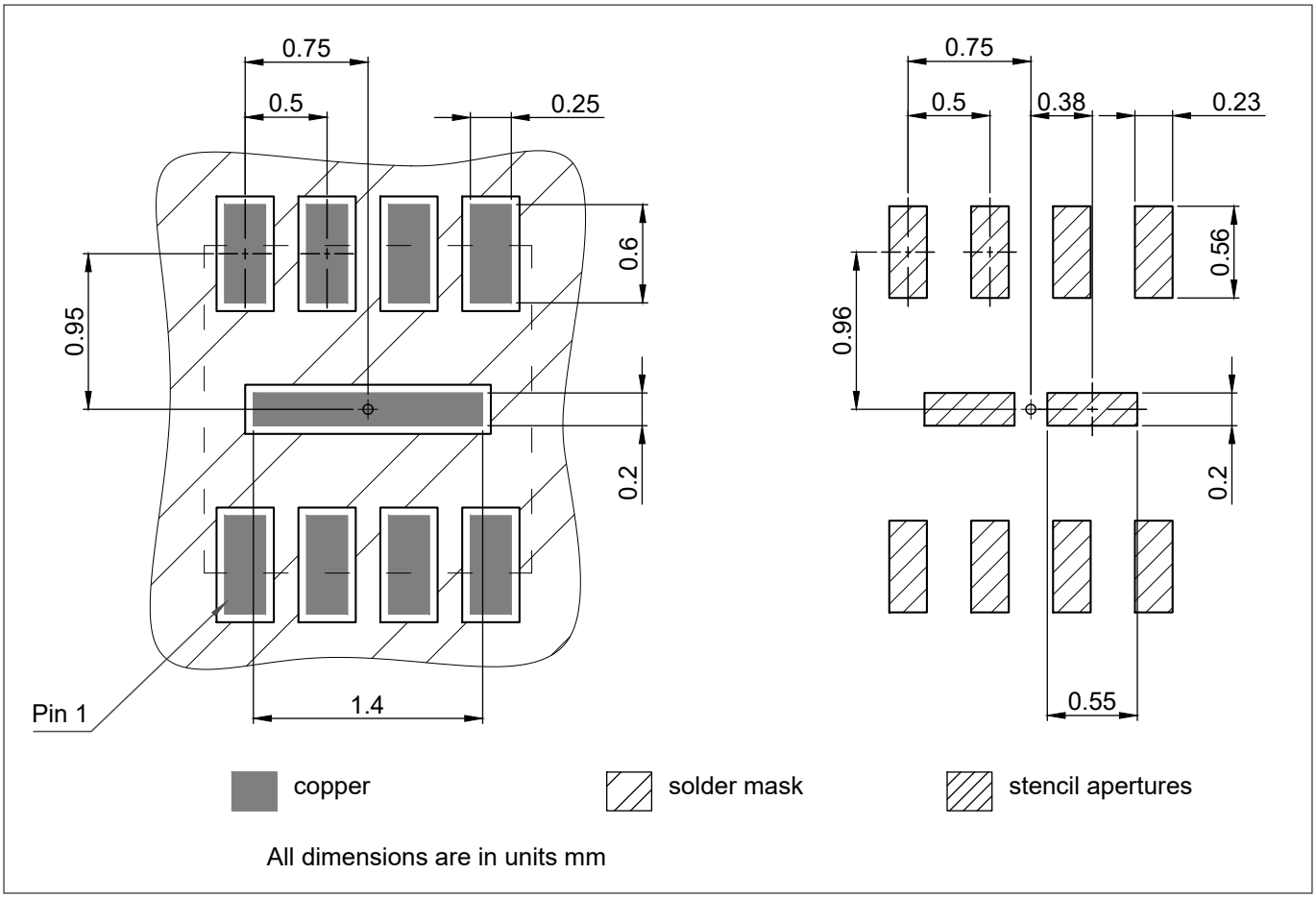

Figure 16 PG-USON-8-6 package footprint

Tape & reel packing

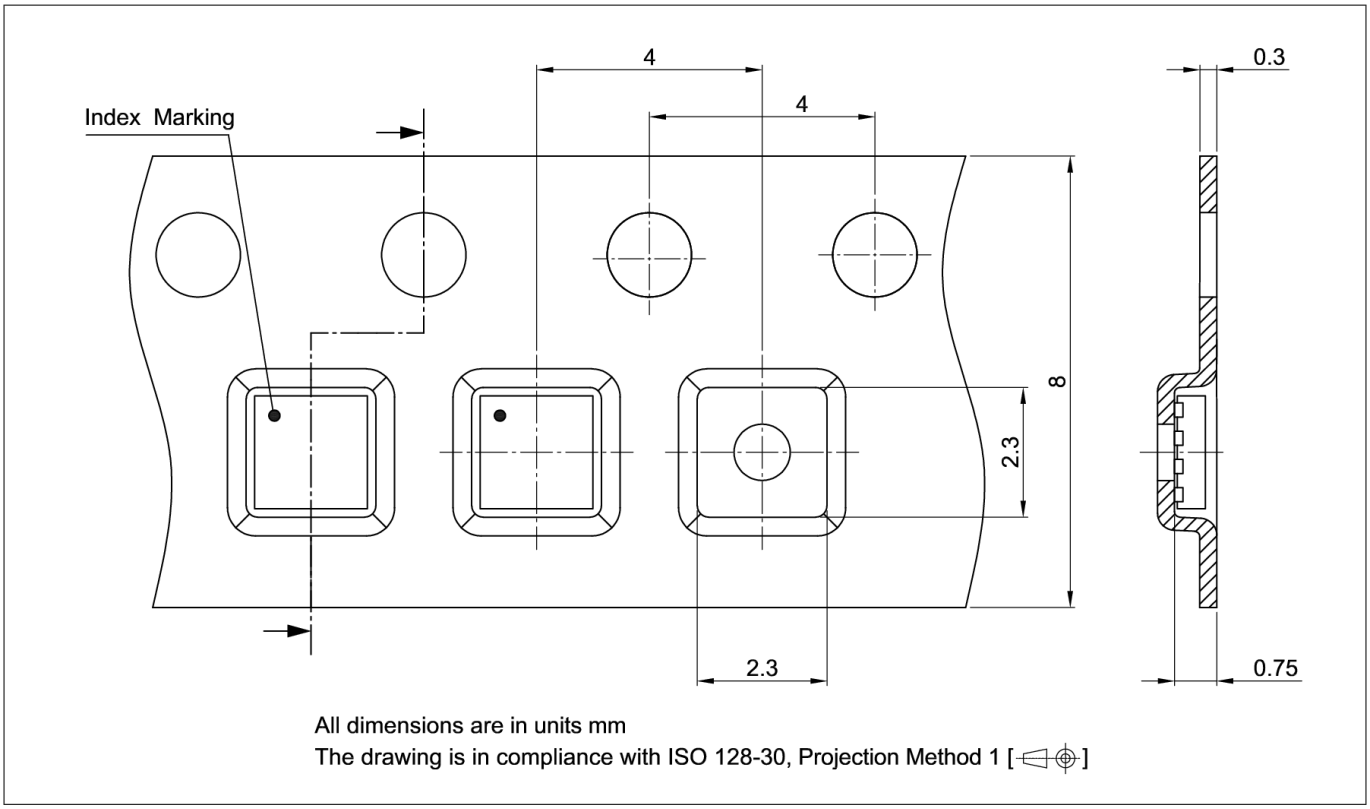

Figure 17 PG-USON-8-6 tape & reel packing

Production sample marking pattern

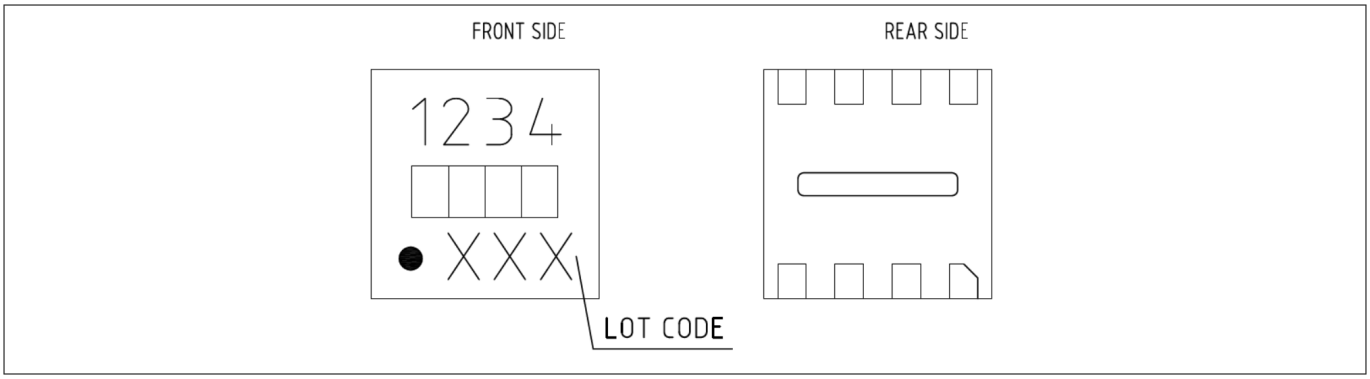

Figure 18 PG-USON-8-6 sample marking pattern

The dot indicates pin 01 for the chip. The following table describes the sample marking pattern:

Table 8 Marking table for PG-USON-8-6 packages

Indicator	Description
1234	Type code: "1234<N> • <N>: hardware derivative number
□□□□	Qualified production parts: “<YYWW>”: • <YY>: production year • <WW>: production week

Table 8 Marking table for PG-USON-8-6 packages (continued)

Indicator	Description
XXX	Lot code, defined and inserted during fabrication, issued by the packaging site

Package layout

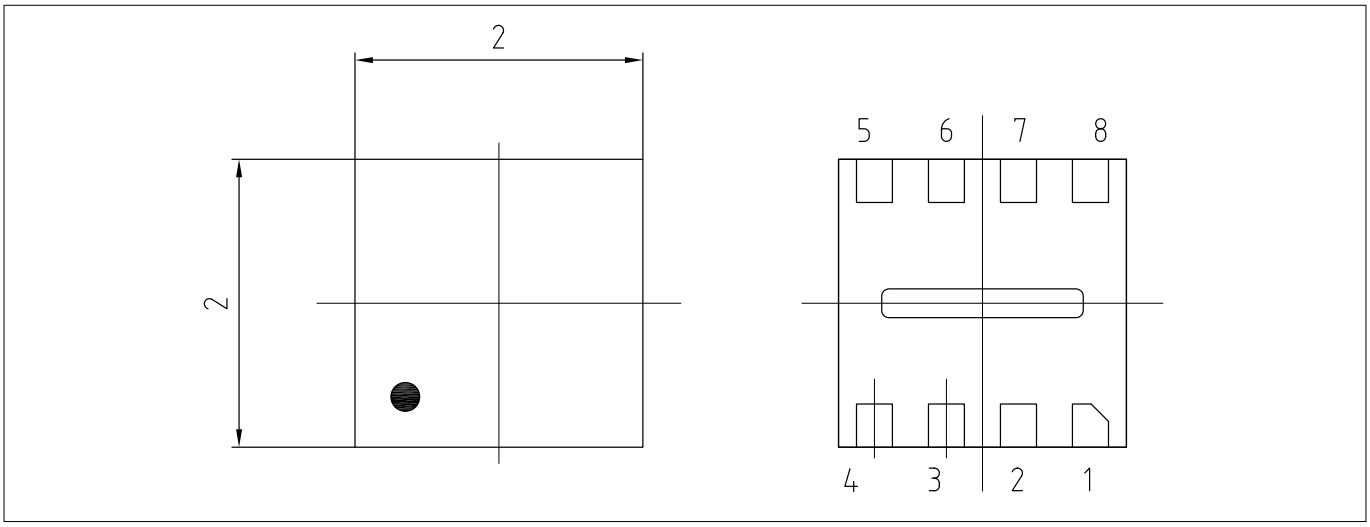

Figure 19 PG-USON-8-6 package layout

Pad-to-signal reference

Table 9 Pad-to-signal reference for PG-USON-8-6

Pad	Symbol	Pin type	Buffer type	Signal function / remarks
01	GND	GND	–	**Power supply:** Common ground reference (V_{SS})
02	NC	–	–	No internal connection / do not connect externally
03	GPIO0.1	I/O	GPIO_IO	**GPIO0.1:** SWIO usage **UART_IO:** ISO/IEC 7816-3 card usage
04	NC	–	–	No internal connection / do not connect externally
05	NC	–	–	No internal connection / do not connect externally
06	GPIO0.0	I	GPIO_I	**GPIO0.0:** SWIO usage **UART_CLK:** ISO/IEC 7816-3 card usage
07	GPIO0.2	I	GPIO_I	**GPIO0.2:** SWIO usage **UART_RST:** ISO/IEC 7816-3 card usage
08	VCC	PWR	–	**Power supply:** Chip power and pad supply (V_{CC})

3.2.4 PG-USON-10-2

Package outline

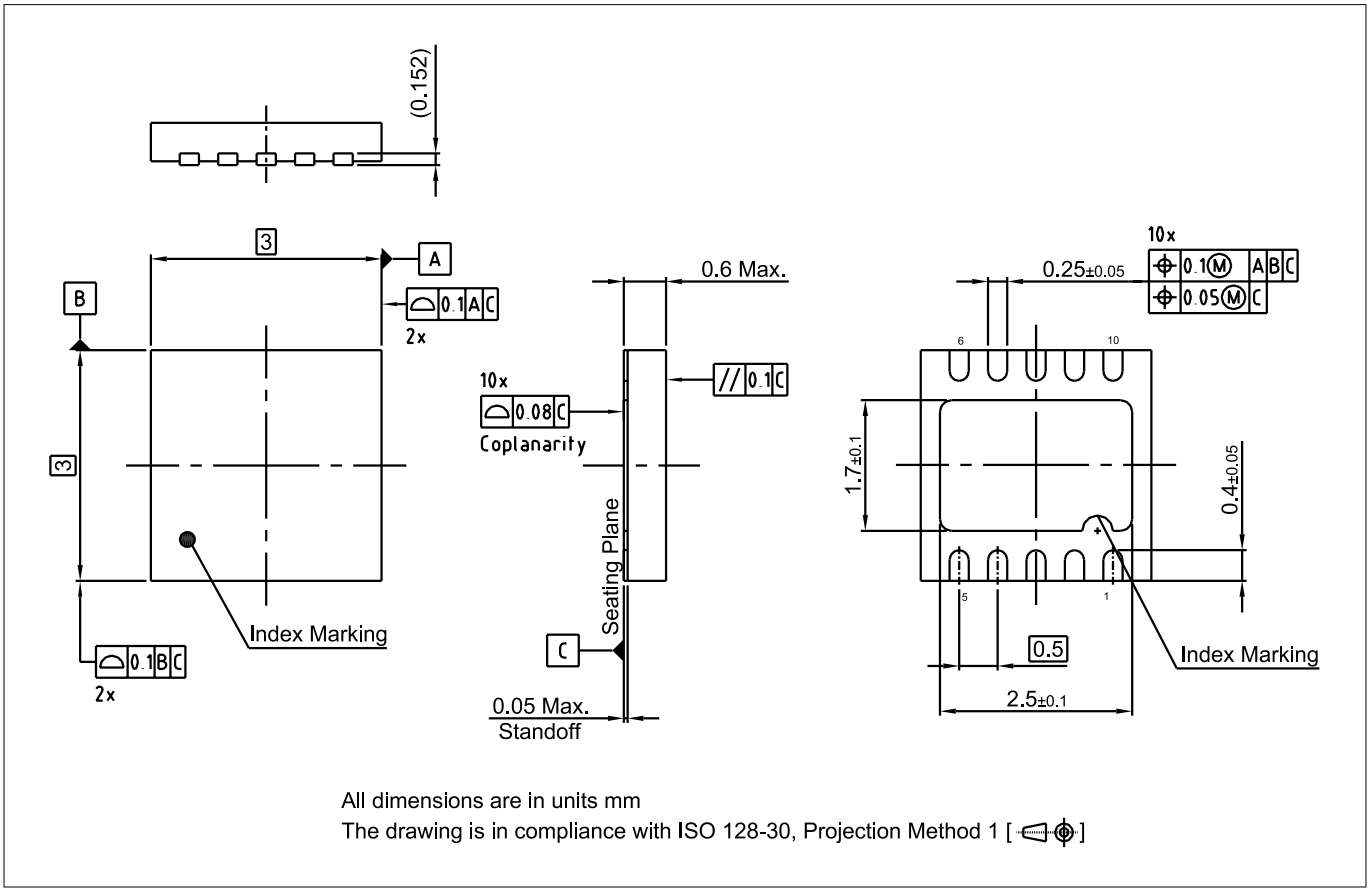

Figure 20 PG-USON-10-2 package outline

Package footprint

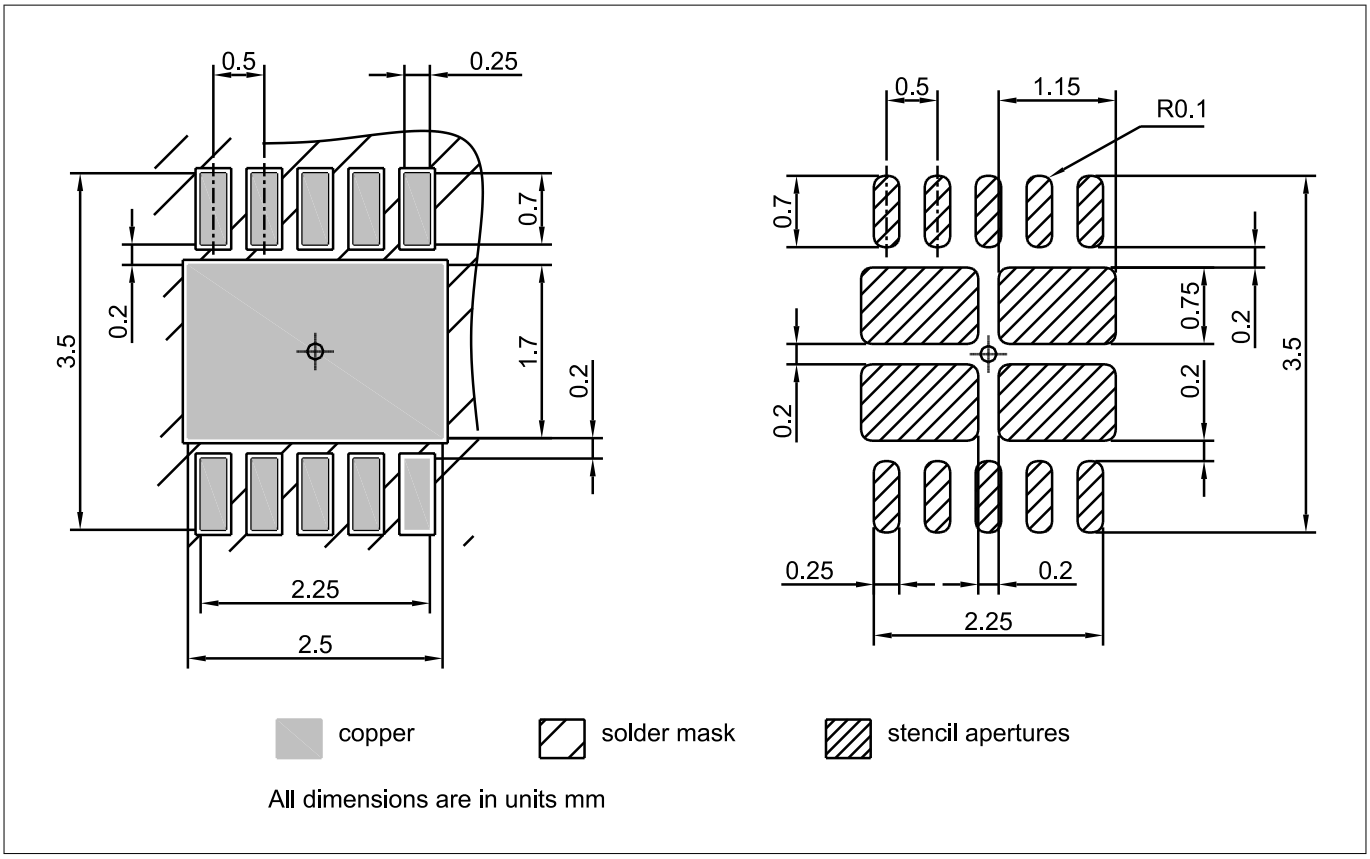

Figure 21 PG-USON-10-2 package footprint

Tape & reel packing

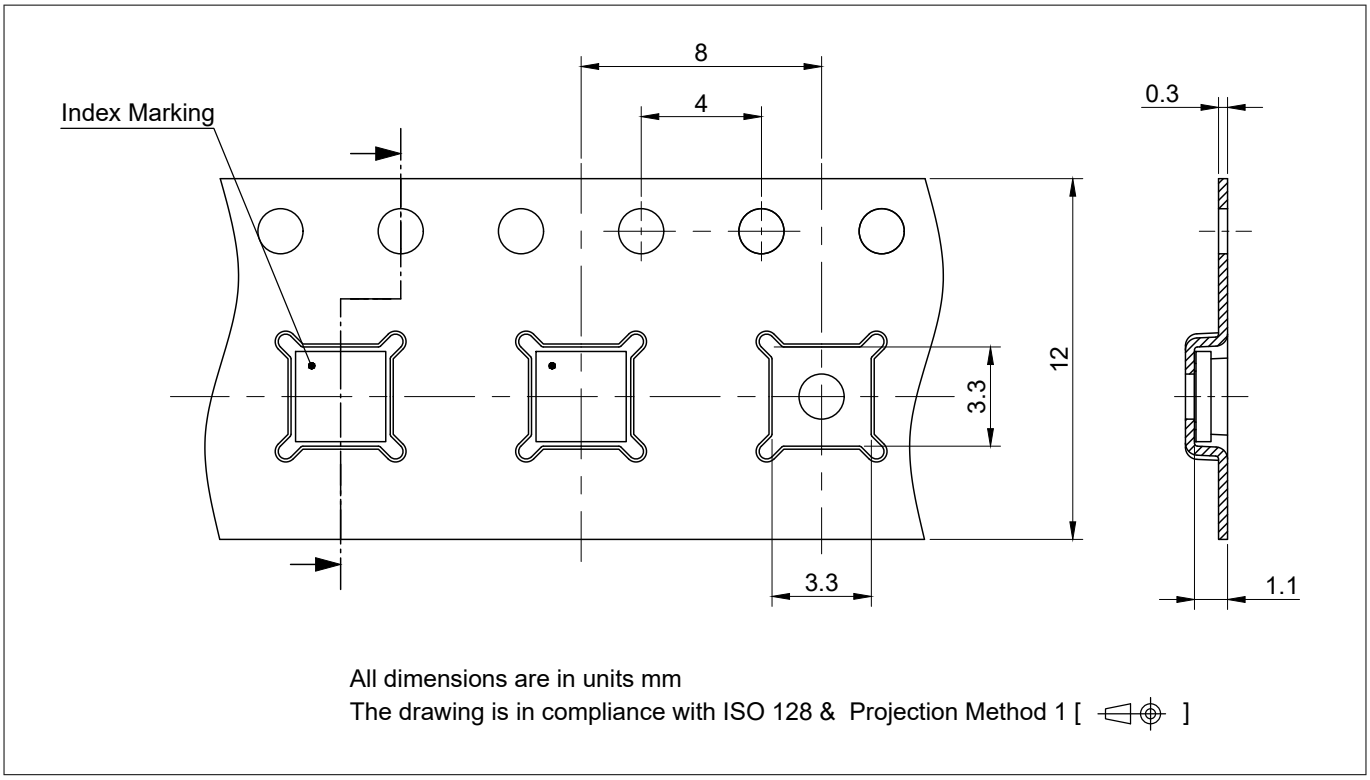

Figure 22 PG-USON-10-2 tape & reel packing

Production sample marking pattern

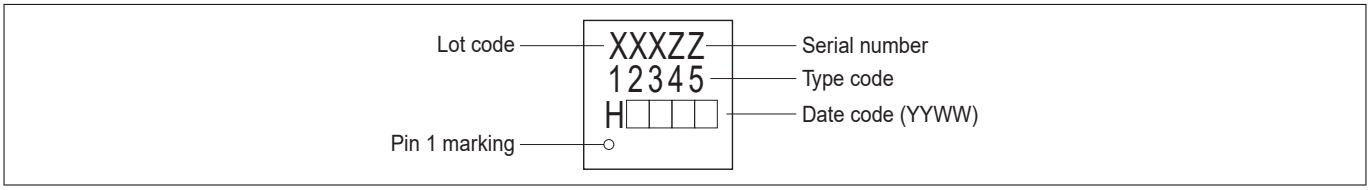

Figure 23 PG-USON-10-2 sample marking pattern

The dot indicates pin 01 for the chip. The following table describes the sample marking pattern:

Table 10 Marking table for PG-USON-10-2 packages

Indicator	Description
XXX	Lot code, defined and inserted during fabrication, issued by the packaging site
ZZ	Serial number, defined and inserted during fabrication, issued by the packaging site
12345	Type code: "XXXX<N>
H□□□□	Engineering samples: “HE<YWW>”: • Halogen-free • Engineering Sample • <Y>: 2nd digit of production year • <WW>: production week Qualified production parts: “H<YYWW>”:

Table 10 Marking table for PG-USON-10-2 packages (continued)

Indicator	Description
	• Halogen-free • <YY>: production year • <WW>: production week

Package layout

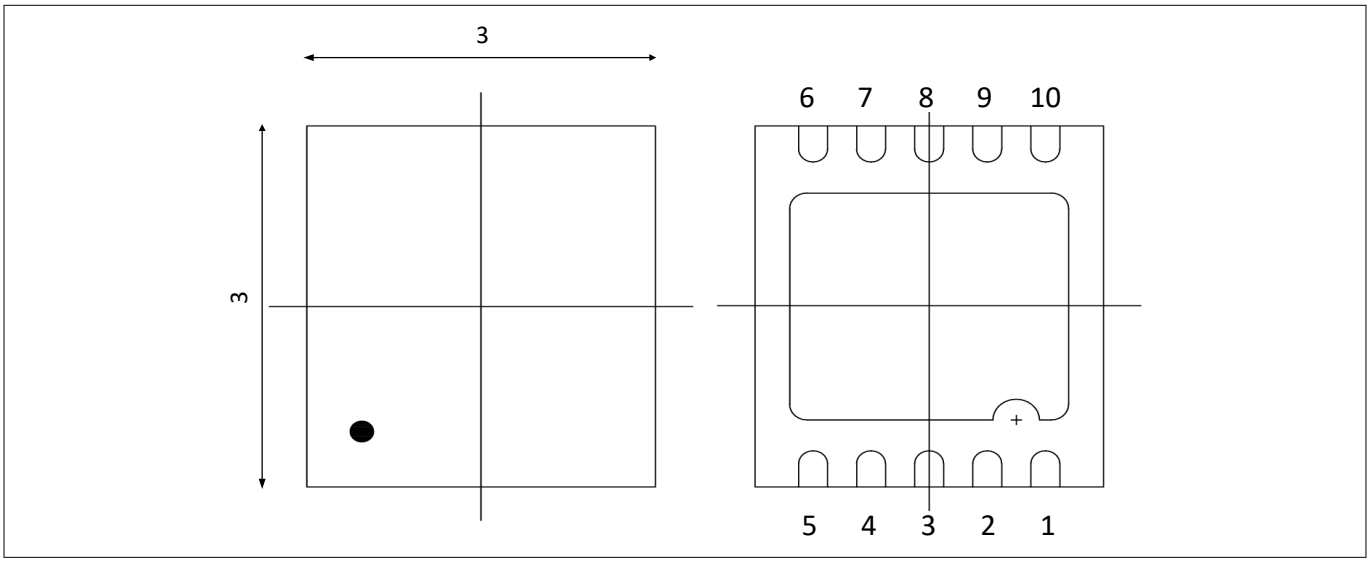

Figure 24 PG-USON-10-2 package layout

Pad-to-signal reference

Table 11 Pad-to-signal reference for PG-USON-10-2

Pad	Symbol	Pin type	Buffer type	Signal function / remarks
01	GND	GND	–	**Power supply:** Common ground reference (V_{SS})
02	NC	–	–	No internal connection / do not connect externally
03	GPIO0.1	I/O	GPIO_IO	**GPIO0.1:** SWIO usage **UART_IO:** ISO/IEC 7816-3 card usage
04	NC	–	–	No internal connection / do not connect externally
05	NC	–	–	No internal connection / do not connect externally
06	NC	–	–	No internal connection / do not connect externally
07	NC	–	–	No internal connection / do not connect externally
08	GPIO0.0	I	GPIO_I	**GPIO0.0:** SWIO usage **UART_CLK:** ISO/IEC 7816-3 card usage
09	GPIO0.2	I	GPIO_I	**GPIO0.2:** SWIO usage **UART_RST:** ISO/IEC 7816-3 card usage
10	VCC	PWR	–	**Power supply:** Chip power and pad supply (V_{CC})

3.2.5 PG-VQFN-8-4

Package outline

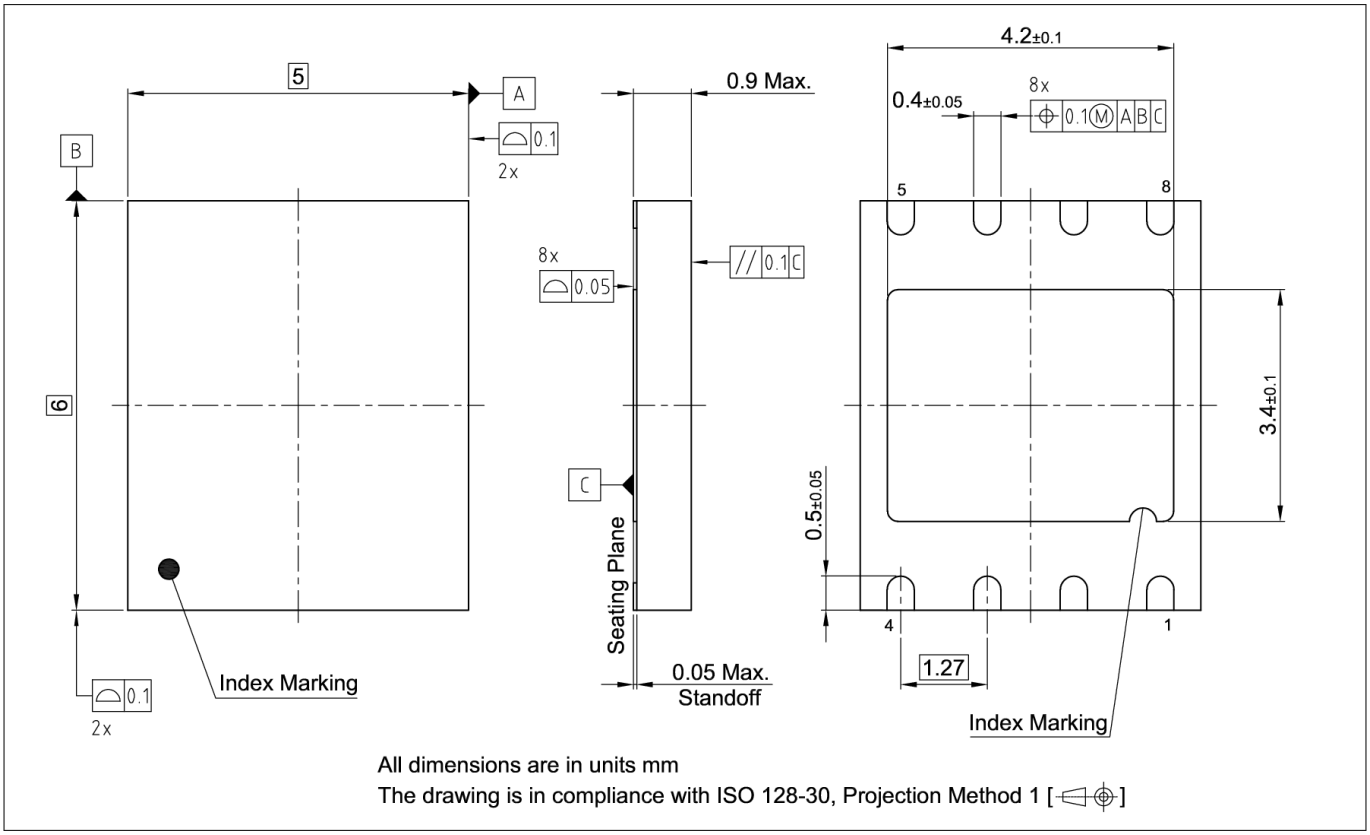

Figure 25 PG-VQFN-8-4 package outline

Package footprint

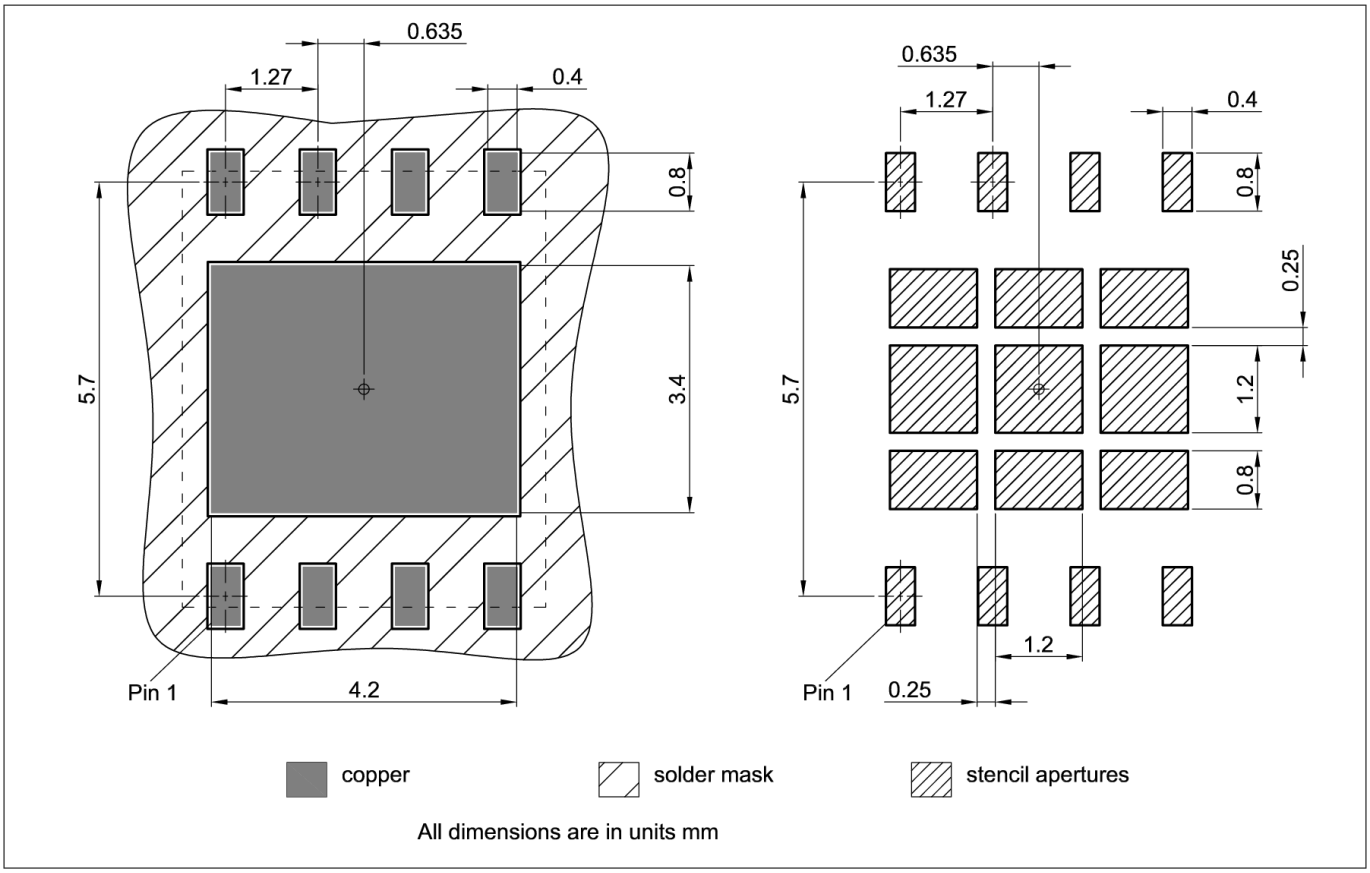

Figure 26 PG-VQFN-8-4 package footprint

Tape & reel packing

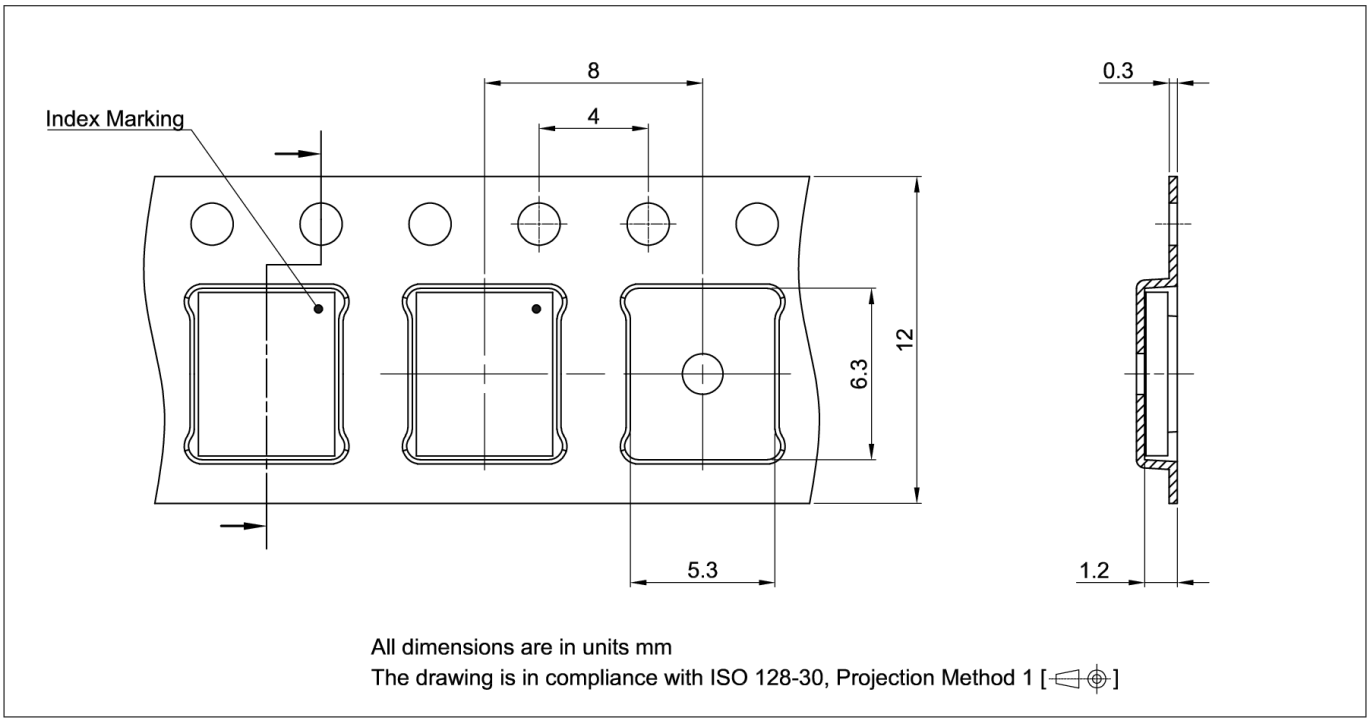

Figure 27 PG-VQFN-8-4 tape & reel packing

Production sample marking pattern

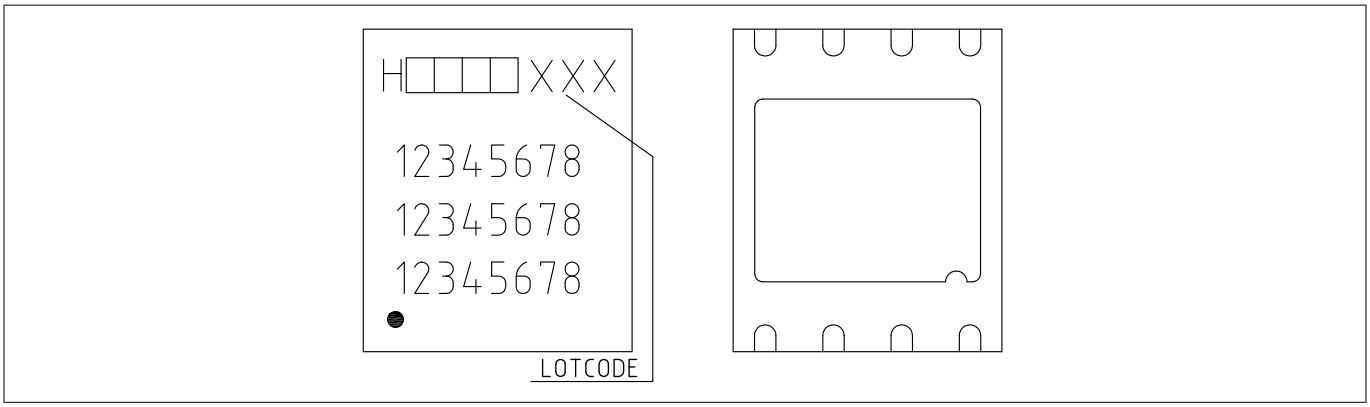

Figure 28 PG-VQFN-8-4 sample marking pattern

The dot indicates pin 01 for the chip. The “lot code” and “serial number” are defined and inserted during fabrication.

The following table describes the sample marking pattern:

Table 12 Marking table for PG-VQFN-8-4 packages

Indicator	Description
H□□□□	Engineering samples: “HE<YWW>”: • Halogen-free • Engineering Sample • <Y>: 2nd digit of production year • <WW>: production week (calendar week) Qualified production parts: “H<YYWW>”: • Halogen-free • <YY>: production year • <WW>: production week (calendar week)
XXX	Lot code, defined and inserted during fabrication, issued by the packaging site

Package layout

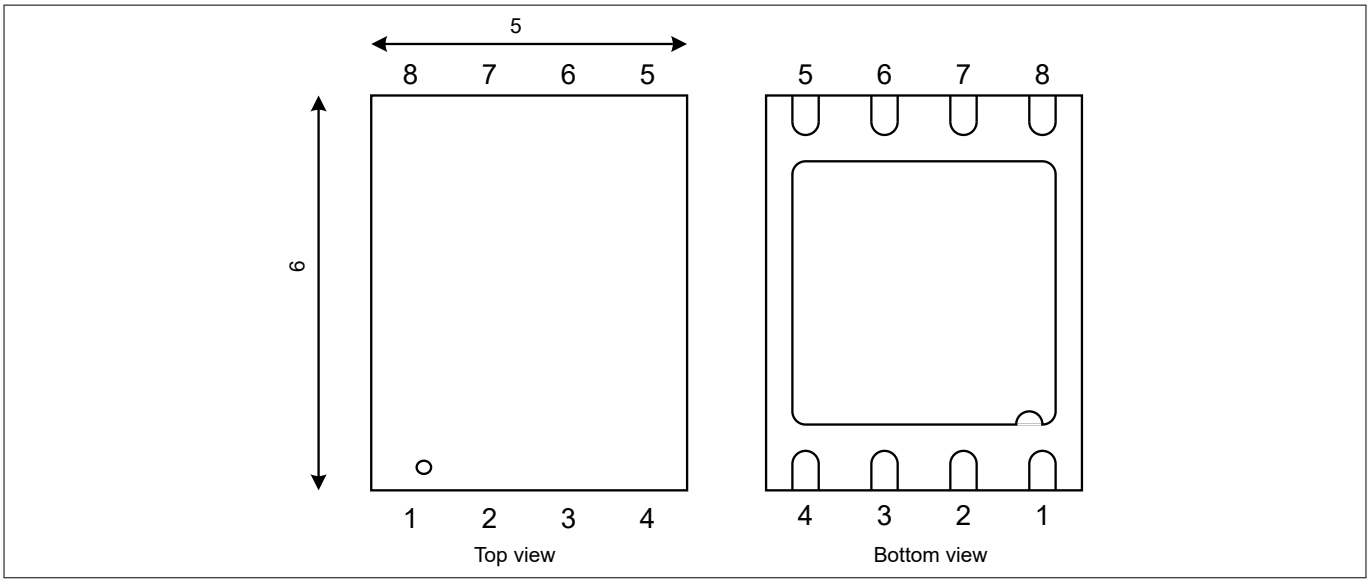

Figure 29 PG-VQFN-8-4 package layout

Pad-to-signal reference

Table 13 Pad-to-signal reference for PG-VQFN-8-4

Pad	Symbol	Pin type	Buffer type	Signal function / remarks
01	GND	GND	–	**Power supply:** Common ground reference (V_{SS})
02	NC	–	–	No internal connection / do not connect externally
03	GPIO0.1	I/O	GPIO_IO	**GPIO0.1:** SWIO usage **UART_IO:** ISO/IEC 7816-3 card usage
04	NC	–	–	No internal connection / do not connect externally
05	NC	–	–	No internal connection / do not connect externally
06	GPIO0.0	I	GPIO_I	**GPIO0.0:** SWIO usage **UART_CLK:** ISO/IEC 7816-3 card usage
07	GPIO0.2	I	GPIO_I	**GPIO0.2:** SWIO usage **UART_RST:** ISO/IEC 7816-3 card usage
08	VCC	PWR	–	**Power supply:** Chip power and pad supply (V_{CC})

3.3 Chip scale packages

The following packages are available:

- SG-XFWLB-6-2 (for V02 controller only)
- SG-XFWLB-6-3 (for V15 controller only)

Note: Due to the lack of mechanical protection, chips delivered in this package are sensitive to mechanical damage. Therefore increased production fall-off rate compared to mold packages is to be expected. To reduce escape of chips with mechanical damage to the field, the customer OS should activate the Crack Detection Circuitry after chip assembly (please refer to the Hardware Reference Manual and Application Notes for details).

*For further information and specialties of this package please see "**Recommendations for Board Assembly of Infineon xWLy Packages**" [1] on the Infineon Homepage.*

The figures in the sections below show the following aspects of the package:

- Package outline: shows the package dimensions of the controller in the individual packages
- Package footprint: shows footprint recommendations
- Tape and reel packing
- Sample marking pattern: describes the productive sample marking pattern on the package
- Package layout: shows a simple layout with the pin numbers described in the pad-to-signal reference section

Note: Unless specified otherwise, all figure dimensions are given in mm.

Note: The drawings are for information only and not drawn to scale. More detailed information about package characteristics and assembly instructions is available on request.

1 Link might not provide the latest released version of the document. Please check the package catalog available on the Infineon Web page

3.3.1 SG-XFWLB-6-2

Package outline

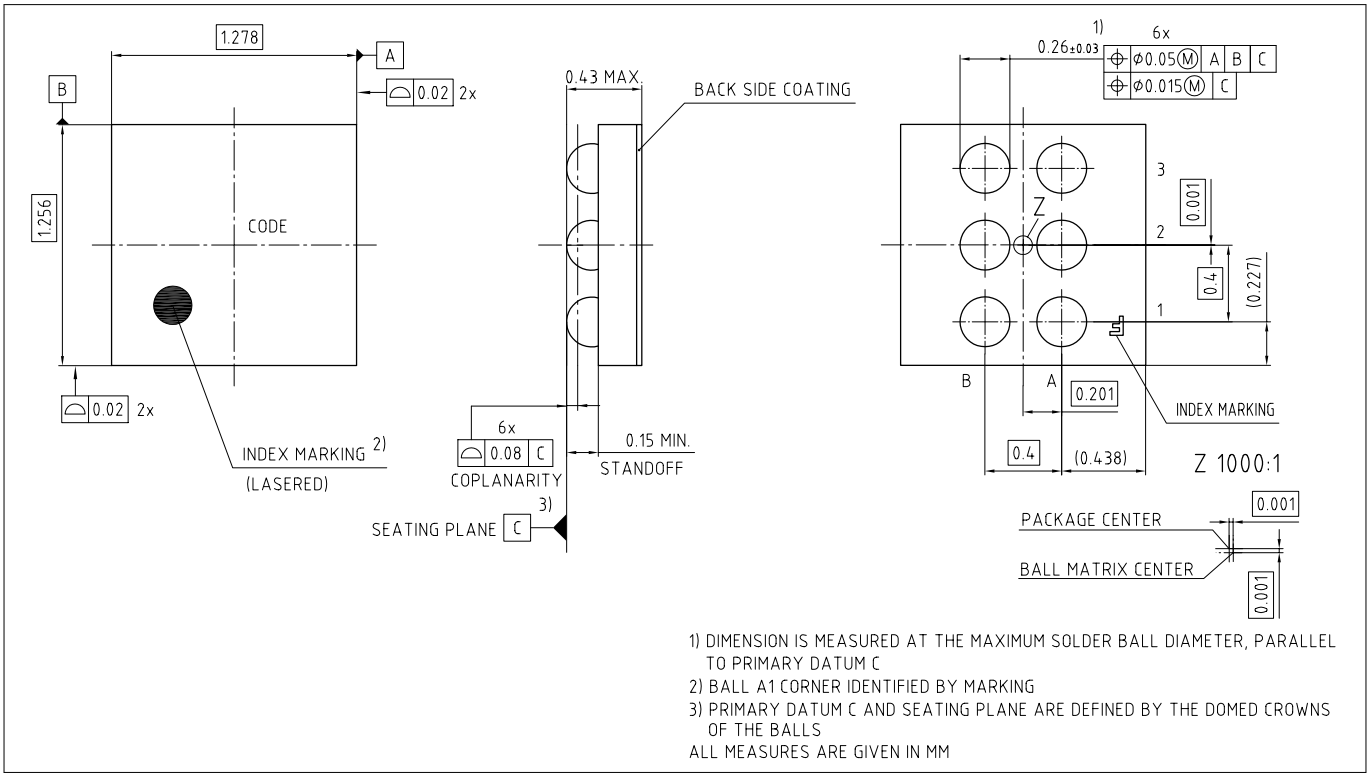

Figure 30 SG-XFWLB-6-2 package outline

Package footprint

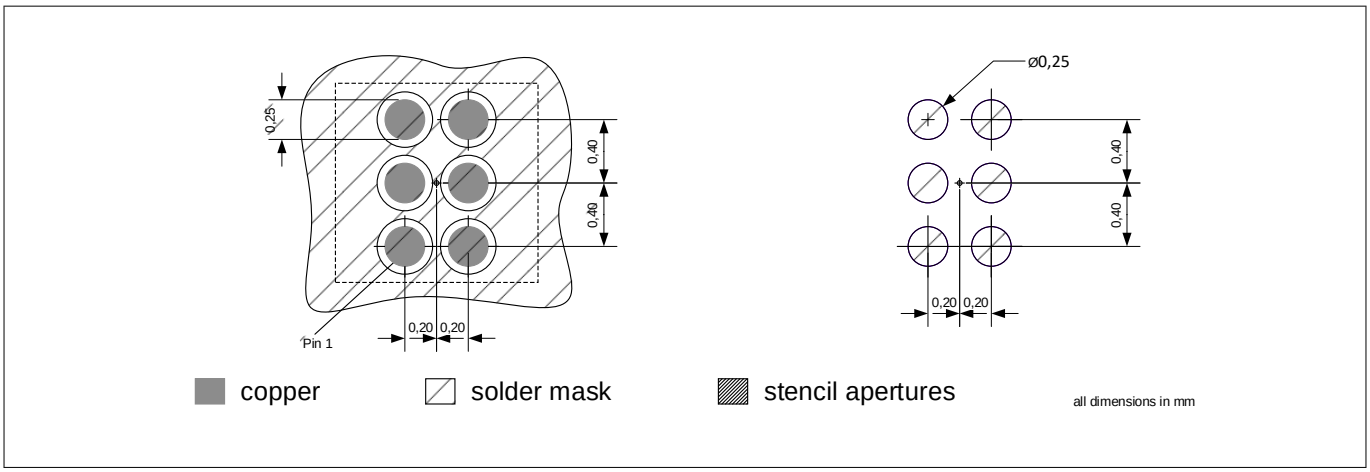

Figure 31 SG-XFWLB-6-2 package footprint

3 Description of delivery forms

Tape & reel packing

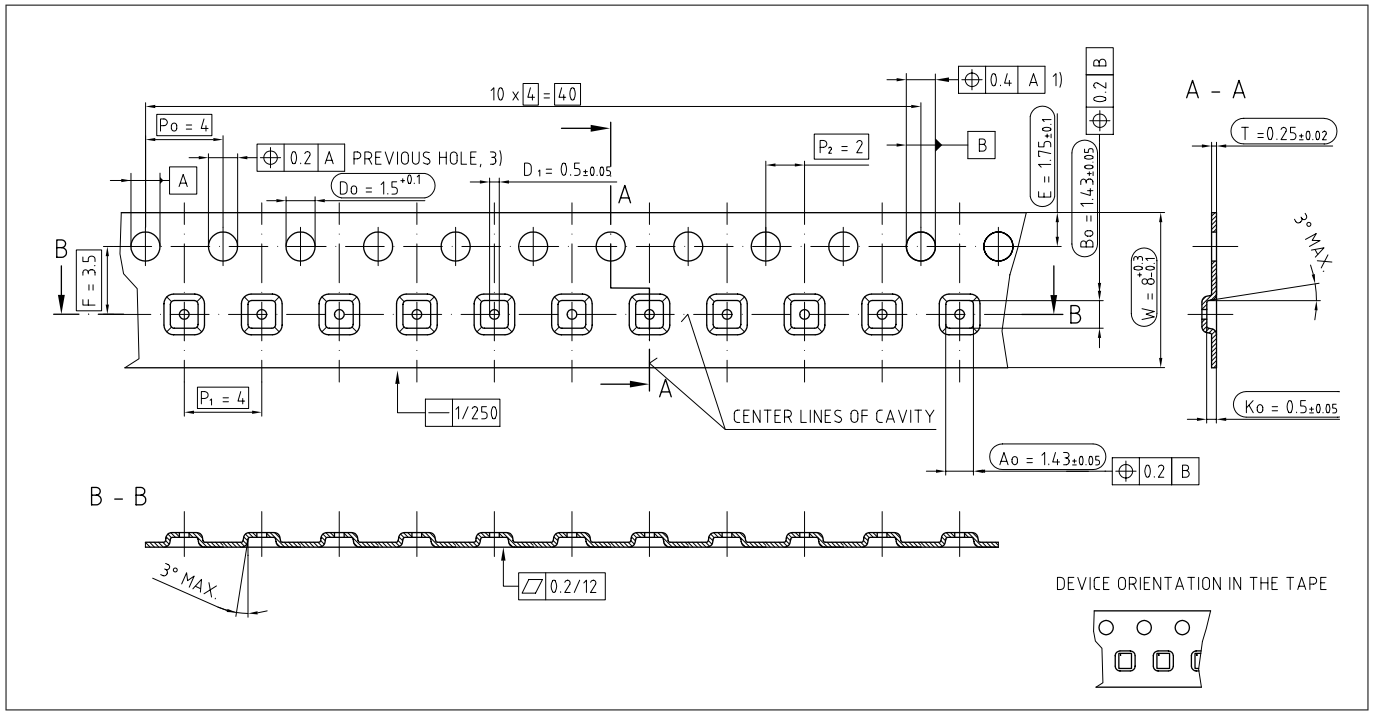

Figure 32 SG-XFWLB-6-2 tape & reel packing

Production sample marking pattern

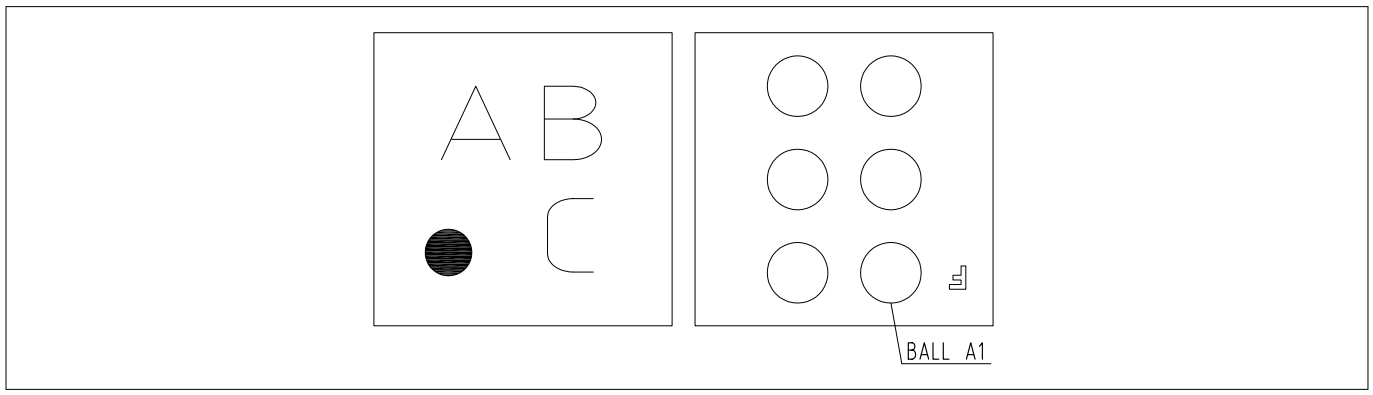

Figure 33 SG-XFWLB-6-2 sample marking pattern

The dot indicates ball 01 for the chip.

A

1-digit year-month code (ces-code)

B

1-digit day-of-the-month code according to the table below.

C

Product specific text.

Table 14 Day of the month code

Date	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Code	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	G

Table 14 Day of the month code (continued)

Date	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
Code	H	J	K	L	M	N	P	Q	R	T	U	V	W	X	Y	

Package layout

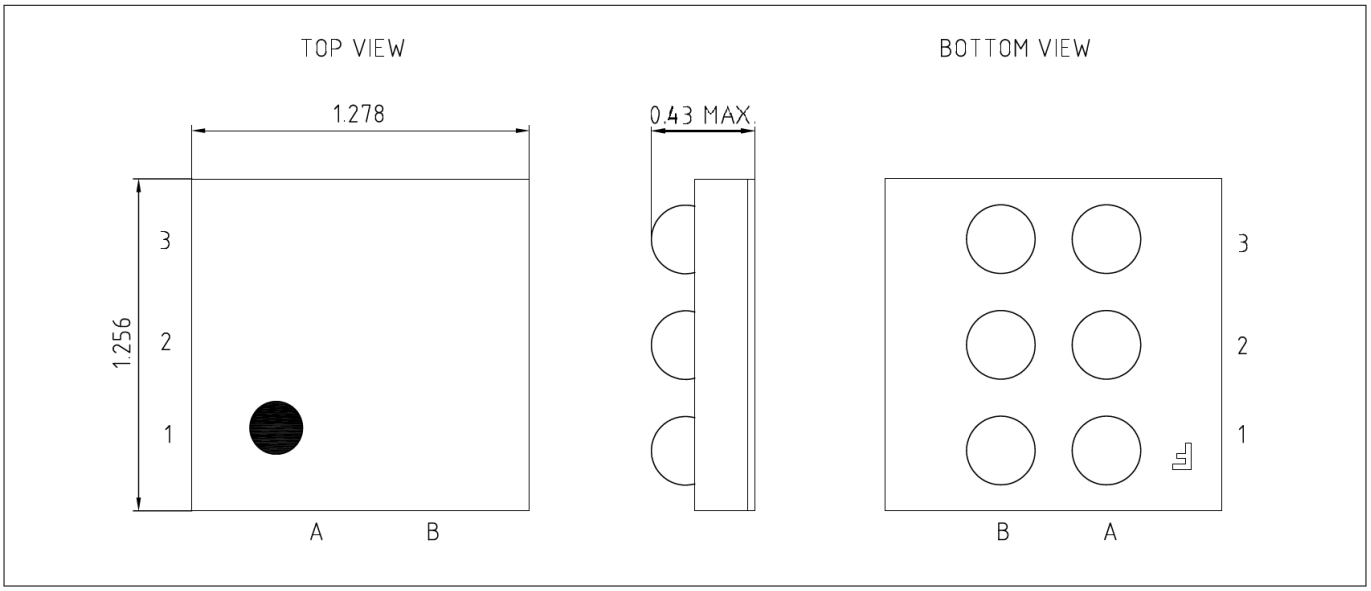

Figure 34 SG-XFWLB-6-2 package layout

Pad-to-signal reference

Table 15 Pad-to-signal reference for SG-XFWLB-6-2

Pad	Symbol	Pin type	Buffer type	Signal function / remarks
A1	GPIO0.0	I	GPIO_I	**GPIO0.0:** SWIO usage **UART_CLK:** ISO/IEC 7816-3 card usage
A2	GPIO0.2	I	GPIO_I	**GPIO0.2:** SWIO usage **UART_RST:** ISO/IEC 7816-3 card usage
A3	VCC	PWR	–	**Power supply:** Chip power and pad supply (V_{CC})
B1	NC	–	–	No internal connection / do not connect externally
B2	GPIO0.1	I/O	GPIO_IO	**GPIO0.1:** SWIO usage **UART_IO:** ISO/IEC 7816-3 card usage
B3	GND	GND	–	**Power supply:** Common ground reference (V_{SS})

3.3.2 SG-XFWLB-6-3

Package outline

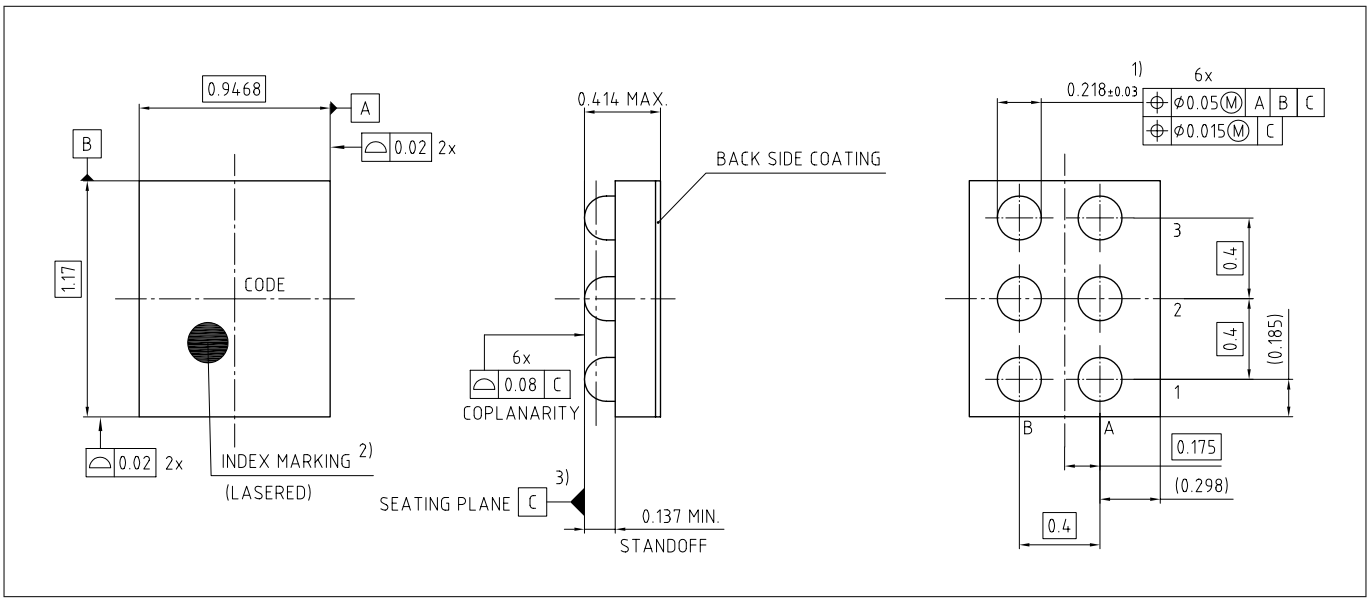

Figure 35 SG-XFWLB-6-3 package outline

Production sample marking pattern

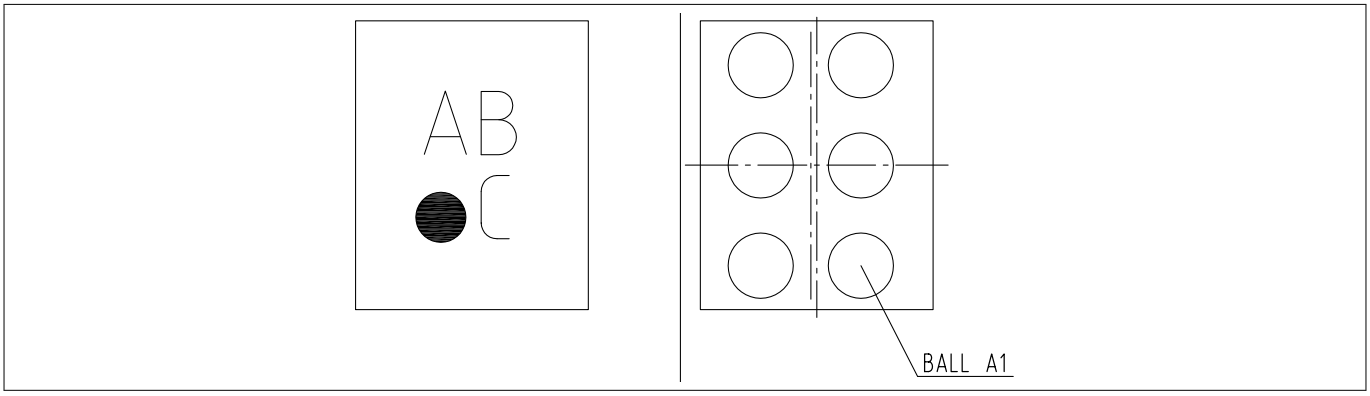

Figure 36 SG-XFWLB-6-3 sample marking pattern

A

1-digit year-month code (ces-code)

B

1-digit day-of-the-month code according to the table below.

C

Product specific text.

Table 16 Day of the month code

Date	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Code	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	G
Date	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	

Table 16 Day of the month code (continued)

Code	H	J	K	L	M	N	P	Q	R	T	U	V	W	X	Y	

Package layout

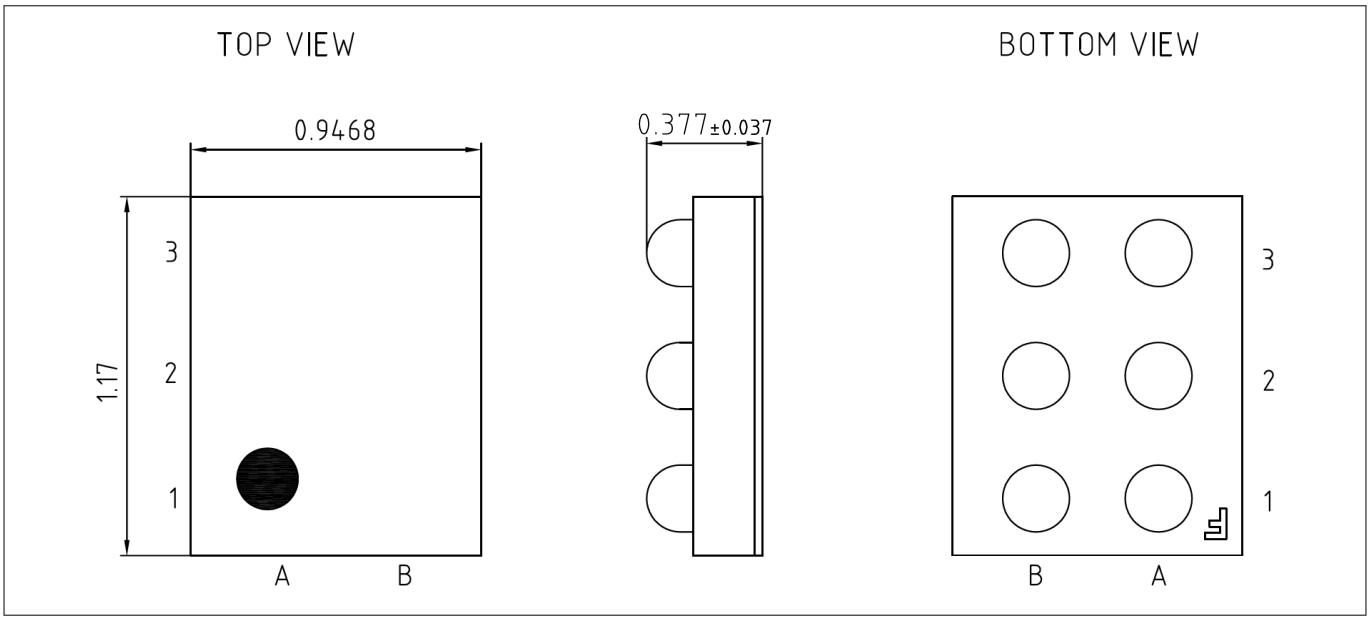

Figure 37 SG-XFWLB-6-3 package layout

Pad-to-signal reference

Table 17 Pad-to-signal reference for SG-XFWLB-6-3

Pad	Symbol	Pin type	Buffer type	Signal function / remarks
A1	GPIO0.0	I	GPIO_I	**GPIO0.0:** SWIO usage **UART_CLK:** ISO/IEC 7816-3 card usage
A2	GPIO0.2	I	GPIO_I	**GPIO0.2:** SWIO usage **UART_RST:** ISO/IEC 7816-3 card usage
A3	VCC	PWR	–	**Power supply:** Chip power and pad supply (V_{CC})
B1	NC	–	–	No internal connection / do not connect externally
B2	GPIO0.1	I/O	GPIO_IO	**GPIO0.1:** SWIO usage **UART_IO:** ISO/IEC 7816-3 card usage
B3	GND	GND	–	**Power supply:** Common ground reference (V_{SS})

4 Electrical characteristics

This section summarizes certain electrical characteristics of the controllers. It provides operational characteristics as well as electrical DC and AC characteristics and particular interface characteristics.

Notes:

1. *T_A as given for the operating temperature range of the controller unless otherwise stated.*
2. *All currents flowing into the controller are considered positive.*

4.1 Absolute maximum ratings

Table 18 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Operating temperature, ambient	T_A	−25	–	+85	°C	T_J must be kept, (for SLC application)
Operating temperature, ambient	T_A	−40	–	+105	°C	T_J must be kept, (for SLM application)
Junction temperature	T_J	–	–	+110	°C	–
Supply voltage	V_{CC}	−0.3	–	7.0	V	–
Input voltage, signal group “GPIO”	V_{IN_GPIO}	−0.3	–	7.0	V	GPIO with ISA[2)] feature

Notes:

1. *The values stated in the table may be further restricted for particular products (i.e. sales codes).*
2. *All voltages are referenced to the power supply ground in the corresponding package, unless otherwise specified.*
3. *Stresses exceeding the values listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions whose values exceed those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability, including NVM data retention and write/erase endurance.*

2 Indirect Supply Avoidance. Pins provided with the "Indirect Supply Avoidance" feature (ISA) allow the supply voltage of the security controller to be switched off regardless of the input voltage at these pins and without drawing a significant pad input current. The input level of all other pins or interfaces that are not provided with this feature must remain unconnected or at low level (to prevent brownout effects).

4.2 Operational characteristics

This section specifies the AC and DC characteristics of the controller, along with details relating to the specific interfaces provided by the controller.

4.2.1 DC electrical characteristics

Table 19 DC characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	1.62	–	5.5	V	Overall functional range
Supply voltage	$V_{CC\_ISO\_A}$	4.5	5.0	5.5	V	Supply voltage range for operation of ISO/IEC 7816-3 Class A
Supply voltage	$V_{CC\_ISO\_B}$	2.7	3.0	3.3	V	Supply voltage range for operation of ISO/IEC 7816-3 Class B
Supply voltage	$V_{CC\_ISO\_C}$	1.62	1.80	1.98	V	Supply voltage range for operation of ISO/IEC 7816-3 Class C
Supply voltage	V_{CC_GPIO}	1.62	–	5.5	V	Supply voltage range for operation of GPIO
Supply current, 4mA current operating mode	I_{CCAVG}	–	–	4.0	mA	Frequency adjusted via ICKLSCAL
Supply current	I_{CCAVG}	–	3.8	–	mA	While running a Dhrystone test T_A = +25°C; V_{CC} = 3.3 V; f_{sys} = 33 MHz
Supply current spikes[3]	I_{CCD_A}	–	–	100	mA	$Q \leq 20$ nAs; V_{CC} in ISO/IEC 7816-3 Class A supply voltage range
Supply current spikes[3]	I_{CCD_B}	–	–	50	mA	$Q \leq 10$ nAs; V_{CC} in ISO/IEC 7816-3 Class B supply voltage range
Supply current spikes[3]	I_{CCD_C}	–	–	30	mA	$Q \leq 6$ nAs; V_{CC} in ISO/IEC 7816-3 Class C supply voltage range
Supply current, deep sleep state	I_{CCS1}	–	–	200	µA	T_A = +25°C, f_{UART_CLK} = 1 MHz all other GPIO inputs at V_{CC}, no other interface activity
Supply current, deep sleep state	I_{CCS2A}	–	–	200	µA	T_A = +25°C, V_{CC} in ISO/IEC 7816-3 Class A supply voltage range, f_{UART_CLK} stopped, all other GPIO inputs at V_{CC}, no other interface activity
Supply current, deep sleep state	I_{CCS2B}	–	–	100	µA	T_A = +25°C, V_{CC} in ISO/IEC 7816-3 Class B supply voltage range, f_{UART_CLK} stopped, all other GPIO inputs at V_{CC}, no other interface activity

3 The maximum spike amplitude and spike charge defined by ETSI TS 102 221 are kept within the specified range. The maximum spike length which is technically irrelevant for terminal regulator and voltage stability is typically kept within the specified range.

Table 19 DC characteristics (continued)

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Supply current, deep sleep state	I_{CCS2C}	–	–	100	µA	T_A = +25°C, V_{CC} in ISO/IEC 7816-3 Class C supply voltage range, f_{UART_CLK} stopped, all other GPIO inputs at V_{CC}, no other interface activity

4.2.2 AC electrical characteristics

Table 20 AC characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
V_{CC} rampup time	t_{VCCR}	1	–	–	µs	0 to 100% of V_{CC} target voltage ramp[4]
BOS startup time until entry into user mode	t_{WA}	–	–	–		Refer to corresponding Product List
NVM power-up time	t_{EEPU}	–	32	–	µs	T_A = 25°C
NVM power-down time	t_{EEPD}	–	8	–	µs	T_A = 25°C
NVM wake-up time[5]	t_{EEREC}	–	22		µs	T_A = 25°C
Wake-up from sleep mode to initial CPU activity	t_{WUPS}	–	–	40	µs	
System oscillator frequency	f_{OSC}	-	33	-	MHz	Average system frequency for nominally adjusted oscillator at T_j = +25°C and zero lifetime (without silicon aging). The actual oscillator frequency may vary due to dynamic on-chip power management functions (e.g. voltage drop monitor, current limitation) and environmental conditions.
System oscillator frequency temperature drift	f_{OSC_T}	-	-23	-	kHz/°C	Average system oscillator frequency drift as function of junction temperature).
1 MHz clock frequency range	$f_{CLK1MHZ}$	0.90	1	1.10	MHz	After NVM osc. calibration. For T_J = −25°C ... +85°C
System clock frequency	f_{SYSCLK}	f_{OSC} / 32		f_{OSC}	MHz	

4.2.2.1 Power-up considerations

The rampup times given in ***AC characteristics*** apply under the assumption of a linear rise in voltage from 0% to 100% of the target voltage level. However, owing to possible current spike effects, it is recommended to follow the voltage characteristics shown in the figure below.

4 Please refer to ***Power-up considerations***

5 The NVM needs a time t_{EEPD} for power down; if sleep mode is requested and a wake-up condition is pending, the total time the NVM is not available is t_{EEPD} + t_{EEREC}

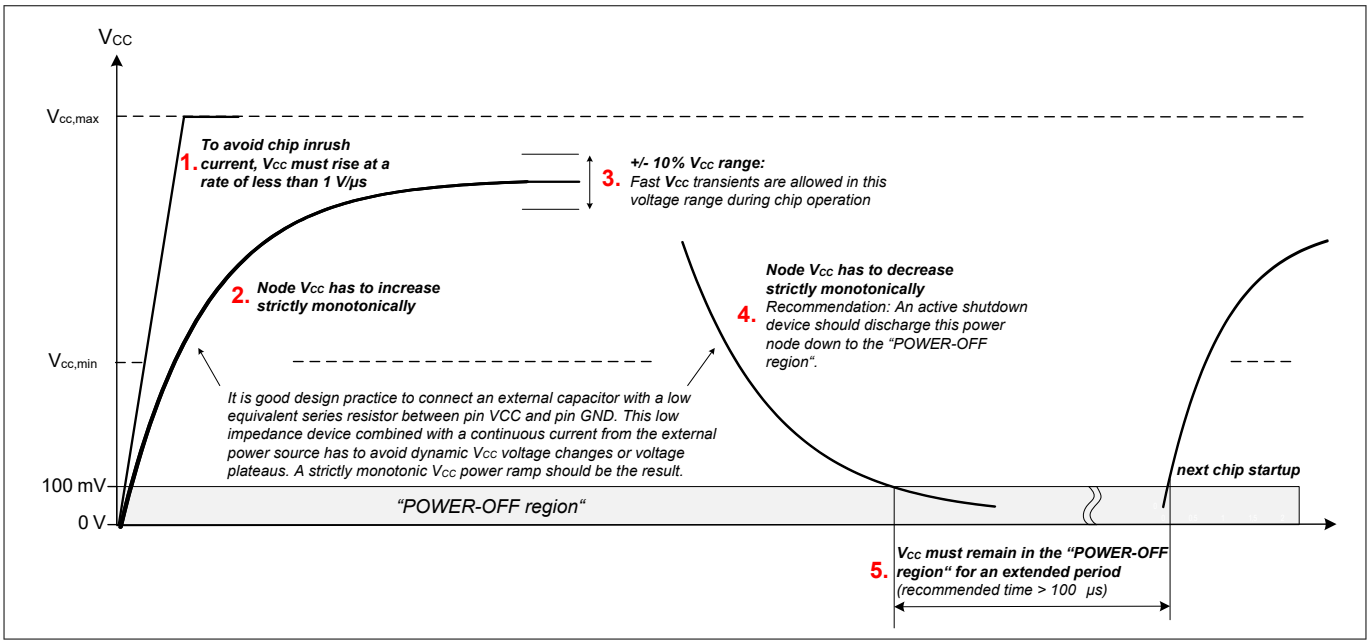

Figure 38 Recommended power-up behavior

4.3 Particular interface characteristics

This chapter provides electrical characteristics with respect to operation of particular interfaces of the controller.

Note: Unless otherwise stated, all values in this section are measured at the pins of the used package, i.e., the resistance, capacitance and inductance, for example, of the package and the bond wires are already included in these values!

4.3.1 ISO/IEC 7816-3 card interface characteristics

The electrical characteristics of the pads described below comply with the standards ISO/IEC 7816-3 ***[3]***, GSM 11.11 ***[6]***, GSM 11.12 ***[7]***, GSM 11.18 ***[8]***, ETSI TS 102.221 ***[5]***.

Notes:

1. *All currents flowing out of the pad are considered to be positive.*

2. *Symbol T_A describes the ambient temperature range.*

Table 21 ISO/IEC 7816-3 card maximum ratings

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Pad input voltage	V_I	−0.3		V_{CC_ISO} + 0.3	V	

Table 22 ISO/IEC 7816-3 card DC electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC_ISO}				V	Note: V_{CC_ISO} includes: $V_{CC\_ISO\_A}$ $V_{CC\_ISO\_B}$ $V_{CC\_ISO\_C}$
Voltage Class A	$V_{CC\_ISO\_A}$	4.5		5.5	V	
Voltage Class B	$V_{CC\_ISO\_B}$	2.7		3.3	V	
Voltage Class C	$V_{CC\_ISO\_C}$	1.62		1.98	V	
UART_RST						
Input high voltage						
	V_{IH}	0.8 * V_{CC_ISO}		V_{CC_ISO}	V	Voltage Class A, B, C, −150 µA < I_{IH} < +20 µA, T_A = 0°C to +50°C
	V_{IH}	0.7 * V_{CC_ISO}		V_{CC_ISO}	V	Voltage Class A, B, C, T_A = 0°C to +50°C

Table 22 ISO/IEC 7816-3 card DC electrical characteristics (continued)

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
	V_{IH}	$V_{CC\_ISO\_A}$ – 0.7 V		$V_{CC\_ISO\_A}$	V	Voltage Class A, −20 µA ≤ I_{IH}, T_A = −25°C to +85°C
	V_{IH}	0.8 * $V_{CC\_ISO\_B}$		$V_{CC\_ISO\_B}$	V	Voltage Class B, −20 µA ≤ I_{IH}, T_A = −25°C to +85°C
	V_{IH}	0.8 * $V_{CC\_ISO\_C}$		$V_{CC\_ISO\_C}$	V	Voltage Class C, −20 µA ≤ I_{IH}, T_A = −25°C to +85°C
Input low voltage						
	V_{IL}	0		0.12 * V_{CC_ISO}	V	Voltage Class A, B, C, −20 µA < I_{IL} < 200 µA, T_A = 0°C to +50°C
	V_{IL}	0		0.2 * V_{CC_ISO}	V	Voltage Class A, B, C, T_A = 0°C to +50°C
	V_{IL}	0		0.6	V	Voltage Class A, I_{IL} ≤ 200 µA, T_A = −25°C to +85°C
	V_{IL}	0		0.2 * $V_{CC\_ISO\_B}$	V	Voltage Class B, I_{IL} ≤ 200 µA, T_A = −25°C to +85°C
	V_{IL}	0		0.2 * $V_{CC\_ISO\_C}$	V	Voltage Class C, I_{IL} ≤ 200 µA, T_A = −25°C to +85°C
UART_CLK						
Input high voltage						
	V_{IH}	0.7 * V_{CC_ISO}		V_{CC_ISO}	V	Voltage Class A, B, C, −100 µA < I_{IH} < +20 µA, T_A = 0°C to +50°C
	V_{IH}	0.7 * V_{CC_ISO}		V_{CC_ISO}	V	Voltage Class A, B, C, T_A = 0°C to +50°C
	V_{IH}	0.7 * V_{CC_ISO}		V_{CC_ISO}	V	Voltage Class A, B, C, −20 µA ≤ I_{IH}, T_A = −25°C to +85°C
Input low voltage						

Table 22 ISO/IEC 7816-3 card DC electrical characteristics (continued)

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
	V_{IL}	0		0.5	V	Voltage Class A, B, $-20\ \mu A < I_{IL} < 100\ \mu A$, $T_A = 0°C$ to $+50°C$
	V_{IL}	0		$0.2 * V_{CC\_ISO\_C}$	V	Voltage Class C, $-20\ \mu A < I_{IL} < 100\ \mu A$, $T_A = 0°C$ to $+50°C$
	V_{IL}	0		$0.2 * V_{CC\_ISO}$	V	Voltage Class A, B, C, $T_A = 0°C$ to $+50°C$
	V_{IL}	0		0.5	V	Voltage Class A, $I_{IL} \le 200\ \mu A$, $T_A = -25°C$ to $+85°C$
	V_{IL}	0		$0.2 * V_{CC\_ISO\_B}$	V	Voltage Class B, $I_{IL} \le 20\ \mu A$, $T_A = -25°C$ to $+85°C$
	V_{IL}	0		$0.2 * V_{CC\_ISO\_C}$	V	Voltage Class C, $I_{IL} \le 20\ \mu A$, $T_A = -25°C$ to $+85°C$
UART_IO						
Input high voltage						
	V_{IH}	$0.7 * V_{CC\_ISO}$		V_{CC_ISO}	V	Voltage Class A, B, C, $-20\ \mu A < I_{IH} < 300\ \mu A$, $T_A = 0°C$ to $+50°C$
	V_{IH}	$0.7 * V_{CC\_ISO}$		V_{CC_ISO}	V	Voltage Class A, B, C, $T_A = 0°C$ to $+50°C$
	V_{IH}	$0.7 * V_{CC\_ISO}$		$V_{CC\_ISO} + 0.3$	V	Voltage Class A, B, C, $-20\ \mu A < I_{IH} < 20\ \mu A$, $T_A = -25°C$ to $+85°C$
Input low voltage						
	V_{IL}	0		$0.15 * V_{CC\_ISO}$	V	Voltage Class A, B, C, $-20\ \mu A < I_{IL} < 1000\ \mu A$, $T_A = 0°C$ to $+50°C$
	V_{IL}	0		$0.2 * V_{CC\_ISO}$	V	Voltage Class A, B, C, $T_A = 0°C$ to $+50°C$
	V_{IL}	−0.3		0.8	V	Voltage Class A, $I_{IL} < 1000\ \mu A$, $T_A = -25°C$ to $+85°C$

Table 22 ISO/IEC 7816-3 card DC electrical characteristics (continued)

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
	V_{IL}	−0.3		0.15 * $V_{CC\_ISO\_A}$	V	Voltage Class A, I_{IL} < 1000 µA, T_A = −25°C to +85°C
	V_{IL}	−0.3		0.2 * $V_{CC\_ISO\_B}$	V	Voltage Class B, I_{IL} < 1000 µA, T_A= −25°C to +85°C
	V_{IL}	−0.3		0.2 * $V_{CC\_ISO\_C}$	V	Voltage Class C, I_{IL} < 1000 µA, T_A = −25°C to +85°C
Output high voltage						
	V_{OH}	0.7 * V_{CC_ISO}		V_{CC_ISO}	V	Voltage Class A, B, C, −20 µA < I_{OH}, 20 kΩ to V_{CC_ISO}, T_A = 0°C to +50°C
	V_{OH}	0.7 * V_{CC_ISO}		V_{CC_ISO}	V	Voltage Class A, B, C, 0 µA < I_{OH} < 20 µA, 20 kΩ to V_{CC_ISO}, T_A = 0°C to +50°C
	V_{OH}	3.8		$V_{CC\_ISO\_A}$	V	Voltage Class A, I_{OH} = 20 µA, 20 kΩ to V_{CC_ISO}, T_A = −25°C to +85°C
	V_{OH}	0.7 * $V_{CC\_ISO\_B}$		$V_{CC\_ISO\_B}$	V	Voltage Class B, I_{OH}= 20 µA, 20 kΩ to V_{CC_ISO}, T_A= −25°C to +85°C
	V_{OH}	0.7 * $V_{CC\_ISO\_C}$		$V_{CC\_ISO\_C}$	V	Voltage Class C, I_{OH} = 20 µA, 20 kΩ to V_{CC_ISO}, T_A = −25°C to +85°C
Output low voltage						
	V_{OL}	0		0.15 * $V_{CC\_ISO\_A}$	V	Voltage Class A, −1 mA = I_{OL}, T_A = 0°C to +50°C

Table 22 ISO/IEC 7816-3 card DC electrical characteristics (continued)

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
	V_{OL}	0		0.15 * $V_{CC\_ISO\_B}$	V	Voltage Class B, −1 mA = I_{OL}, T_A = 0°C to +50°C
	V_{OL}	0		0.15 * $V_{CC\_ISO\_C}$	V	Voltage Class C, −500 µA = I_{OL}, T_A = 0°C to +50°C
	V_{OL}	0		0.4	V	Voltage Class A, −1000 µA < I_{OL} < 0 µA, T_A = 0°C to +50°C
	V_{OL}	0		0.08 * $V_{CC\_ISO\_A}$	V	Voltage Class A, −1000 µA < I_{OL} < 0 µA, T_A = 0°C to +50°C
	V_{OL}	0		0.15 * $V_{CC\_ISO\_B}$	V	Voltage Class B, −500 µA < I_{OL} < 0 µA, T_A = 0°C to +50°C
	V_{OL}	0		0.15 * $V_{CC\_ISO\_C}$	V	Voltage Class C, −500 µA < I_{OL} < 0 µA, T_A = 0°C to +50°C
	V_{OL}	0		0.4	V	Voltage Class A, B, −1 mA = I_{OL}, T_A = −25°C to +85°C
	V_{OL}	0		0.3	V	Voltage Class C, −1 mA = I_{OL}, T_A = −25°C to +85°C

Table 23 ISO/IEC 7816-3 card AC electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
UART_RST						
Rise/fall time						
	t_R, t_F			1	µs	Voltage Class A, B, C, T_A = 0°C to 50°C
	t_R, t_F			400	µs	Voltage Class A, B, C, T_A = −25°C to +85°C
Input load capacitance	C_{LOAD}			30	pF	

Table 23 ISO/IEC 7816-3 card AC electrical characteristics (continued)

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
UART_CLK						
External frequency	f_{UART_CLK}	1		10	MHz	@ duty cycle 40% to 60%
Rise/fall time						
	t_R, t_F			0.09 *1/ f_{UART_CLK}	µs	Voltage Class A, B, C, T_A = 0°C to +50°C, measured between 10% and 90% of signal amplitude
	t_R, t_F			0.09 *1/ f_{UART_CLK}	µs	Voltage Class A T_A = −25°C to +85°C, measured between 10% and 90% of signal amplitude
	t_R, t_F			50	ns	Voltage Class B, C, T_A = −25°C to +85°C, measured between 10% and 90% of signal amplitude
Input load capacitance	C_{LOAD}			30	pF	
UART_IO						
Rise/fall time						
	t_R, t_F			1	µs	Voltage Class A, B, C, T_A = 0°C to +50°C
	t_R, t_F			1	µs	Voltage Class A, B, C, T_A = −25°C to +85°C
Input load capacitance	C_{LOAD}			30	pF	
Output load capacitance	C_{LOAD}			30	pF	

4.3.2 GPIO interface characteristics

The electrical characteristics of the GPIOs including restrictions with respect to the maximum sink/source currents for all GPIOs of the controller are given below.

Table 24 GPIO operation supply and input voltages

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC_GPIO}	1.62	–	5.50	V	
GPIO pad input voltage	V_{IN_GPIO}	−0.3	–	V_{CC_GPIO} + 0.3	V	V_{CC_GPIO} is in the operational supply range.

Table 25 GPIO DC electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Input current, pull-up (weak) enabled	I_{PUW}	−3	–	−20	µA	$0\ V \le V_{IN\_GPIO} \le V_{CC\_GPIO} - 0.5\ V$
Input current, pull-down (weak) enabled	I_{PDW}	3	–	20	µA	$0.5\ V \le V_{IN\_GPIO} \le V_{CC\_GPIO}$
Input leakage current	I_{LI}	−2	–	2	µA	Pull-up/down off, output stage off; $0\ V \le V_{IN\_GPIO} \le V_{CC\_GPIO}$
Input low voltage	V_{IL}	−0.3	–	$0.3 * V_{CC\_GPIO}$	V	
Input high voltage	V_{IH}	$0.7 * V_{CC\_GPIO}$	–	V_{CC_GPIO} + 0.3	V	
Output low voltage	V_{OL}	–	–	0.3	V	I_{OL} = 1 mA
Output high voltage	V_{OH}	V_{CC_GPIO} − 0.3	–	–	V	I_{OH} = −1 mA
Input capacitance[6)]	C_{IN}	–	–	10	pF	

Table 26 GPIO AC electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Output signal rise time	t_r	–	3.5	15.0	ns	10% V_{CC_GPIO} to 90% V_{CC_GPIO}; C_{LOAD} = 15 pF, pull-up/down off, no DC load.
Output signal fall time	t_f	–	–	15.0	ns	90% V_{CC_GPIO} to 10% V_{CC_GPIO}; C_{LOAD} = 15 pF, pull-up/down off, no DC load.
Output signal fall time	t_f	–	3.5	15.0	ns	90% V_{CC_GPIO} to 10% V_{CC_GPIO}; C_{LOAD} = 15 pF, pull-up/down off, no DC load; Slew Rate

6 Bare die + typical package, e.g. VQFN or chipcard module. Package details are available on request.

Table 26 GPIO AC electrical characteristics (continued)

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
						Control OFF (default operation mode).
Maximum GPIO input frequency	f_{GPIO_in}	20		40	MHz	With active input filter. The max. input frequency is depending on input signal shape. Test condition: V_{cc_GPIO} = 3.3 V, $t_r = t_f$ = 2 ns (20%-80%), 100% signal swing.

5 RoHS compliance

On January 27, 2003 the European Parliament and the council adopted the directives:

- 2002/95/EC on the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment ("RoHS")
- 2002/96/EC on Waste Electrical and Electrical and Electronic Equipment ("WEEE")

Some of these restricted (lead) or recycling-relevant (brominated flame retardants) substances are currently found in the terminations (e.g. lead finish, bumps, balls) and substrate materials or mold compounds.

The European Union has finalized the Directives. It is the member states' task to convert these Directives into national laws. Most national laws are available, some member states have extended timelines for implementation. The laws arising from these Directives have come into force in 2006 or 2007.

The electro and electronic industry has to eliminate lead and other hazardous materials from their products. In addition, discussions are on-going with regard to the separate recycling of certain materials, e.g. plastic containing brominated flame retardants.

Infineon is fully committed to giving its customers maximum support in their efforts to convert to lead-free and halogen-free[7)] products. For this reason, Infineon's "Green Products" are ROHS-compliant.

Since all hazardous substances have been removed, Infineon calls its lead-free and halogen-free semiconductor packages "green." Details on Infineon's definition and upper limits for the restricted materials can be found here.

The assembly process of our high-technology semiconductor chips is an integral part of our quality strategy. Accordingly, we will accurately evaluate and test alternative materials in order to replace lead and halogen so that we end up with the same or higher quality standards for our products.

The use of lead-free solders for board assembly results in higher process temperatures and increased requirements for the heat resistivity of semiconductor packages. This issue is addressed by Infineon by a new classification of the Moisture Sensitivity Level (MSL). In a first step the existing products have been classified according to the new requirements.

7 Any material used by Infineon is PBB and PBDE-free. Plastic containing brominated flame retardants, as mentioned in the WEEE directive, will be replaced if technically/economically beneficial.

References

The following documents set out or describe specifications and/or standards referenced in the text of this document.

Contact-based smart cards

[1] International Standardization Organization/International Electrotechnical Commission: *ISO/IEC 7816-1: Identification Cards – Integrated Circuit(s) Cards with Contacts Part 1: Physical Characteristics (1998-10-15) Amendment 1 - Maximum height of the IC contact surface*, 2003-11-15

[2] International Standardization Organization/International Electrotechnical Commission: *ISO/IEC 7816-2: Information Technology – Identification Cards – Integrated Circuit(s) Cards with Contacts Part 2: Dimension and location of the contacts (Second edition)*, 2007-10-15

[3] International Standardization Organization/International Electrotechnical Commission: *ISO/IEC 7816-3: Identification Cards - Integrated Circuit Cards - Part 3: Cards with contacts - Electrical interface and transmission protocol (Third Edition)*, 2006-11-01

[4] International Standardization Organization/International Electrotechnical Commission: *ISO/IEC 7816-4: Identification cards - Integrated circuit cards - Part 4: Organization, security and commands for interchange (Second edition)*, 2005-01-15

[5] European Telecommunications Standards Institute: *ETSI TS 102 221 – Smart cards; UICC-Terminal interface; Physical and logical characteristics (Release-11)*, 2012-06

[6] European Telecommunications Standards Institute: *ETSI TS 100 977 (V8.13.0) - Digital cellular telecommunications system (Phase 2+); Specification of the Subscriber Identity Module - Mobile Equipment (SIM-ME) Interface (3GPP TS 11.11 version 8.13.0 Release 1999)*, 2005-06

[7] European Telecommunications Standards Institute: *ETSI TS 300 641 (Third Edition) - Digital cellular telecommunications system (Phase 2); Specification of the 3 Volt Subscriber Identity Module - Mobile Equipment (SIM-ME) interface (GSM 11.12 version 4.3.1)*, 1998-03

[8] European Telecommunications Standards Institute: *ETSI TS 101 116 (V7.0.1) - Digital cellular telecommunications system (Phase 2+); Specification of the 1.8 Volt Subscriber Identity Module - Mobile Equipment (SIM - ME) interface (GSM 11.18 version 7.0.1 Release 1998)*, 1999-07

Revision history

Reference	Description
Revision 2.1, 2020-08-03	
SG-XFWLB-6-2	'Product specific text according to deal tmac.' changed to 'Product specific text'.
SG-XFWLB-6-3	'Product specific text according to deal tmac.' changed to 'Product specific text'.
Revision 2.0, 2020-07-16	
PG-USON-6-2	Added footprint and packing figures
PG-USON-8-5	Added packing figure
PG-USON-8-6	Replaced incorrect package layout figure, replaced package outline figure by updated figure
PG-VQFN-8-4	Replaced package outline figure by updated figure
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