32-bit Security Controller SLE/SLI/SLM 97

Integration Guide

Key features

Common features

- Up to 1016 KB SOLID FLASH™ NVM
- Up to 32 KB user RAM
- 32-bit architecture based on the ARM SecurCore SC300 enhanced by Infineon Technologies' cache and security technology
- Supported interfaces: UART, NRG interface, I2C, GPIO, SWP, SPI, USB

Note: Memory size and interface configuration depend on the individual sales code, see corresponding Product List.

Special features

- M9900 - standard grade (SLE97)
  - Temperature range -25 to 85°C
  - Data retention 17 years
- M9905 - automotive grade (SLI97)
  - Temperature range -40 to 105°C
  - Data retention 17 years
- M9906 - industrial grade (SLM97)
  - Temperature range -40 to 105°C
  - Data retention 10 years

About this document

Scope and purpose

This document provides the information on the SMD packages, connectivity and technical data required for integration of the product(s) listed. Further functionalities and interfaces supported by the product(s) but not related to integration are not fully described. Each Infineon Technologies customer is permitted to incorporate information concerning packages and electrical characteristics contained herein into its data books. When doing so, the customer is also requested to identify those features of the Infineon hardware used in its solution products (i.e., Infineon Technologies hardware + third-party firmware/operating system) and concretize this information where possible. Examples of OS-dependent values are **operational** and **standby currents** of the solution product.

Intended audience

This document is intended for device integrators and board manufacturers.

Table of contents

Table of contents

1 Introduction

This document describes the interfaces of the 32-bit Security Controller SLE/SLI/SLM 97 to provide device integrators and board manufacturers useful information regarding its connectivity and technical data.

2 Connectivity

This chapter explains the schematics of the product and gives some recommendations as to how the controller can be externally connected.

For diagrams showing the different connectivity options for the controllers, see ***Appendix A***.

2.1 Power supply schematic

The following figure illustrates how the security controller is to be supplied.

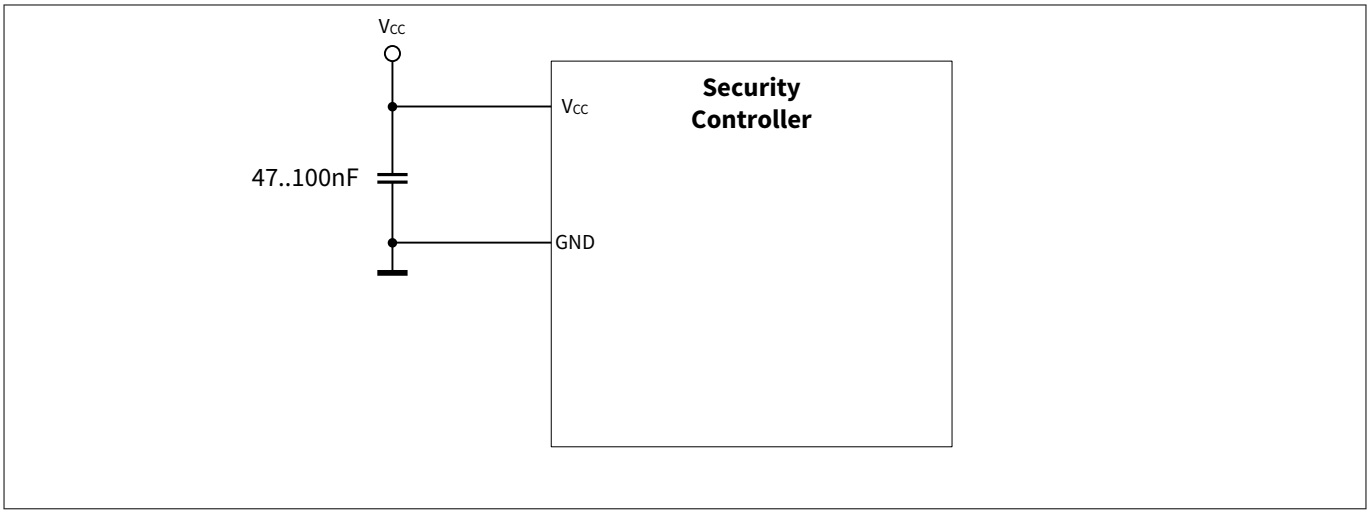

Figure 1 Power supply diagram

Contrary to other areas of application in which different types of capacitors are switched in parallel to stabilize the power supply, here normally only one capacitor is required. This is due to the wide variation limits of the supply voltage and the additional internal measures to handle sudden changes in load. For this decoupling capacitor, use a ceramic type with a low equivalent series resistance.

2.2 Initial delivery state: Flash Loader operation

The product is delivered in its first life cycle to operate the Flash Loader, which becomes active after powering up the device.

The Flash Loader supports the following interface(s):

- ISO/IEC 7816-3 card interface

The Flash Loader configuration defines the following features:

- A fixed pin-out
- A fixed protocol for the associated interface (based on an Infineon Technologies proprietary protocol):
  - ISO/IEC 7816-3 card
- A fixed command set (Flash Loader commands)

Flash Loader ISO/IEC 7816-3 card operation mode

The following communication parameters apply to the data transfer:

- Direct convention
- 8 data bits
- Even parity
- 2 stop bits
- Character repetition enabled
- Block guard time disabled
- Frame checking disabled

When the Flash Loader is active and a reset occurs, the protocol driver transmits the Flash Loader Answer To Reset (ATR) selected by the customer when ordering the chip:

1. ’3B 10 96’ (Standard ATR) indicates
   - ’Negotiable Protocol Mode’
   - Communication via T=0 with the minimum UART clock division factor ’16’. For a terminal clock of 10 MHz, the division factor ’16’ effects a maximum data rate of 625 kbaud (3.5712 MHz and clock division factor ’16’: 223.2 kbaud).

     Note: For compatibility reasons, a PPS negotiation with clock division factor ’8’ will be accepted by the protocol driver.

   - ’No Clock Stop’
   - ’Class A’ chip

2. ’3B 10 97’ offers the same operation parameters, but accepts the minimum UART clock division factor ’8’. That allows a maximum data rate of 1250 kbaud in the case of a 10-MHz terminal clock frequency.

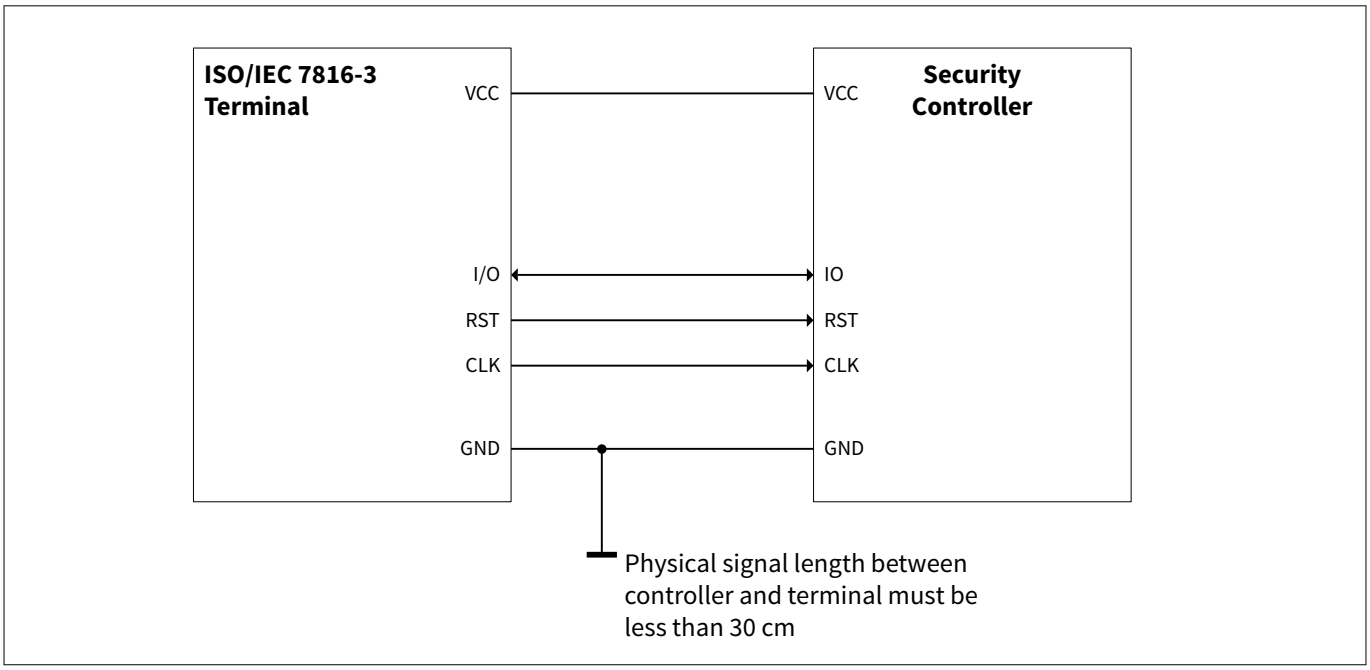

Figure 2 ISO/IEC 7816-3 card interface schematic diagram

The figure illustrates how the ISO/IEC 7816-3 terminal is to be connected to the SLx97 security controller.

Connectivity

Table 1 UART: Flash Loader signal to symbol reference

Symbol	Flash Loader signal name	Signal function / remarks
GPIO0.2	UART_RST	UART chip reset signal (active low)
GPIO0.0	UART_CLK	UART clock signal
GPIO0.1	UART_IO	UART bi-directional data signal
VCC	VDD	Chip power and pad supply
GND	GND	Common ground reference

2.3 Final product configuration: pinout, signal and interface characteristics defined by OS

The OS loaded via the Flash Loader can configure a variety of product characteristics. This also includes which interfaces are connected to which pins. In this regard, the following sections give general guidelines on how power pins and interface signals should be connected in the system.

2.3.1 Interfaces

This section shows how the interfaces are to be connected.

2.3.1.1 ISO/IEC 7816-3 card

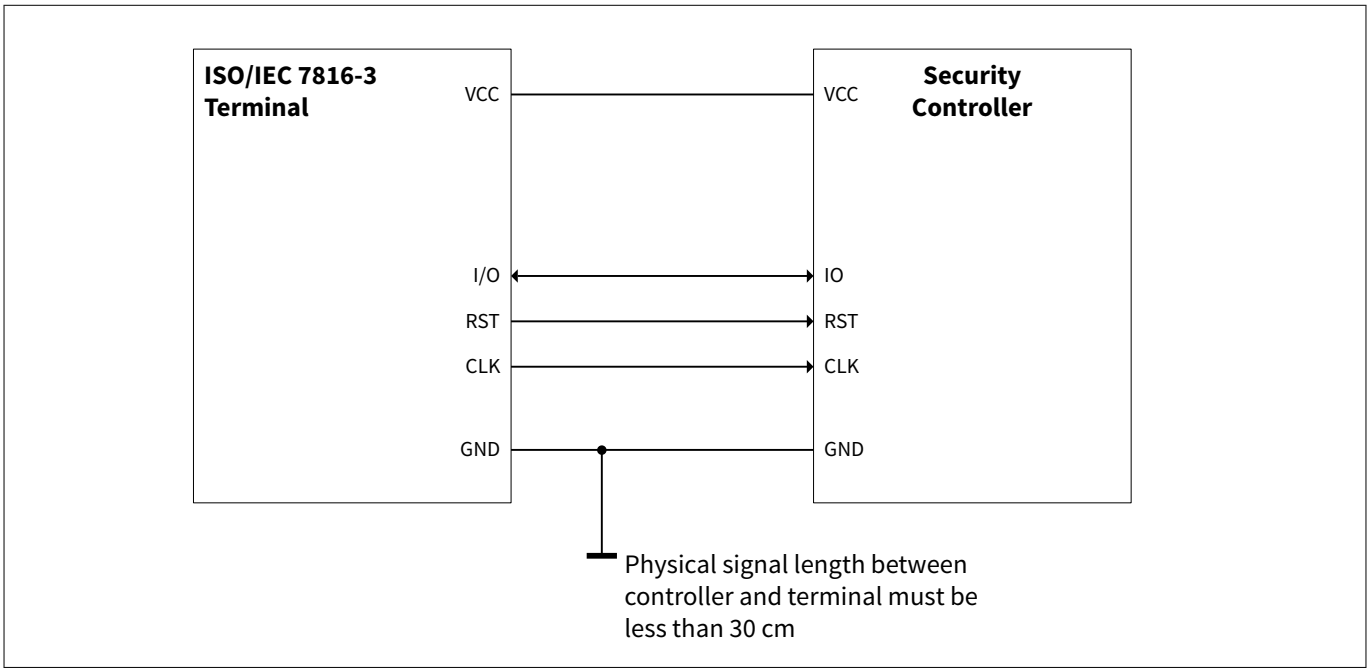

Figure 3 ISO/IEC 7816-3 card interface schematic diagram

The figure illustrates how the ISO/IEC 7816-3 terminal is to be connected to the SLx97 security controller.

2.3.1.2 I2C

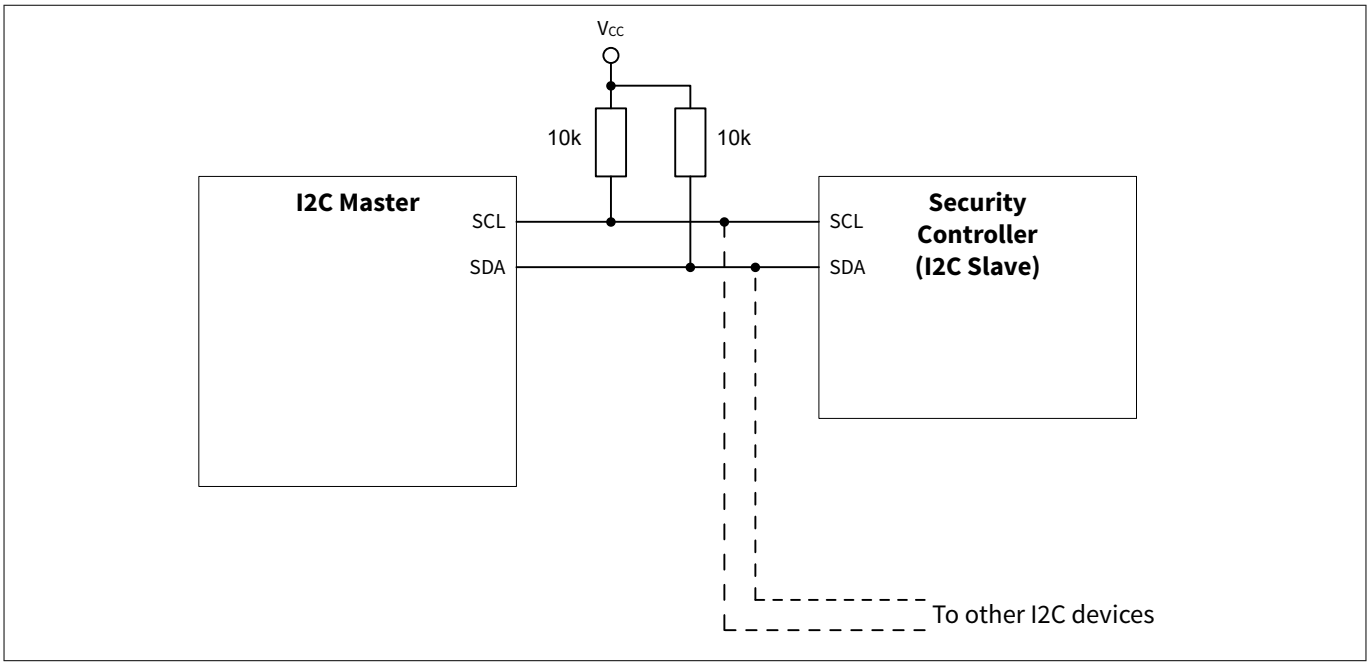

Figure 4 I2C connectivity

The figure illustrates how the I2C bus is to be connected to the SLx97 security controller (I2C slave). The necessary power lines are not highlighted in the figure.

*Note: Depending on the chosen interface configuration different pins may be used, please refer to the pin list of the applicable package in the **Description of delivery forms** chapter.*

2.3.1.3 GPIO

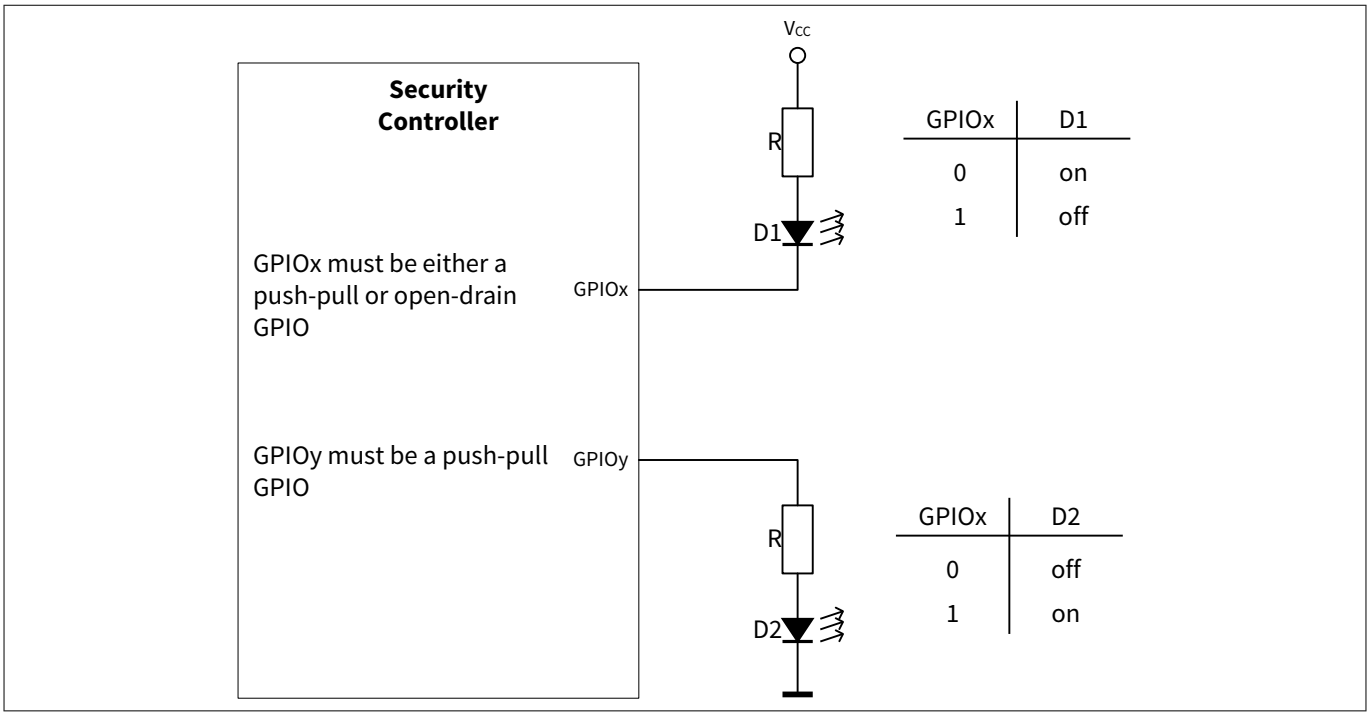

Figure 5 GPIO connectivity

The figure illustrates how GPIO is to be connected to the SLx97 security controller. Refer to ***SPI / GPIO interface*** for electrical characteristics of the interface.

2.3.1.4 SWP

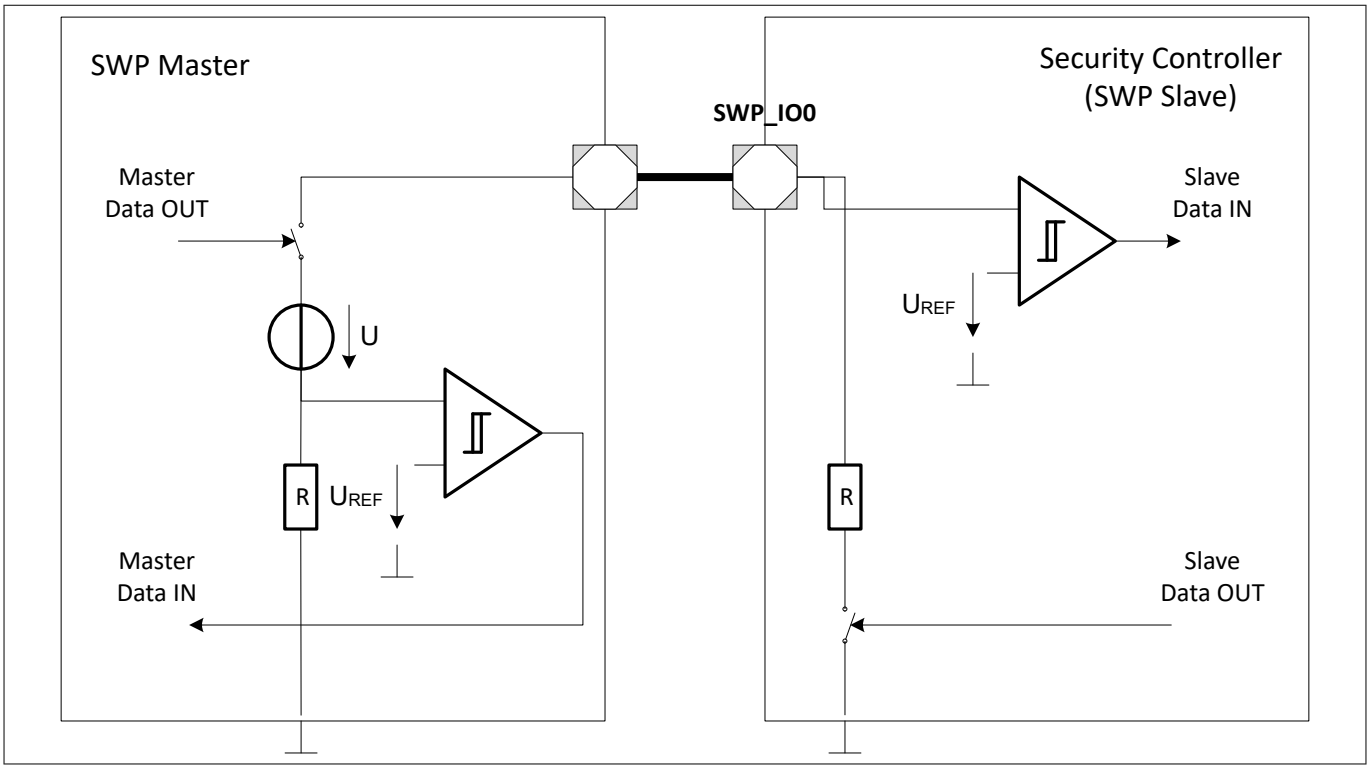

Figure 6 SWP connectivity

The figure illustrates how the SWP master is to be connected to the SLx97 security controller (SWP slave).

The following lengths of the line between the SWP master and SWP slave must not be exceeded:

- 10 cm for 1.7 Mbit/s SWP
- 5 cm for 3.4 Mbit/s SWP

2.3.1.5 SPI

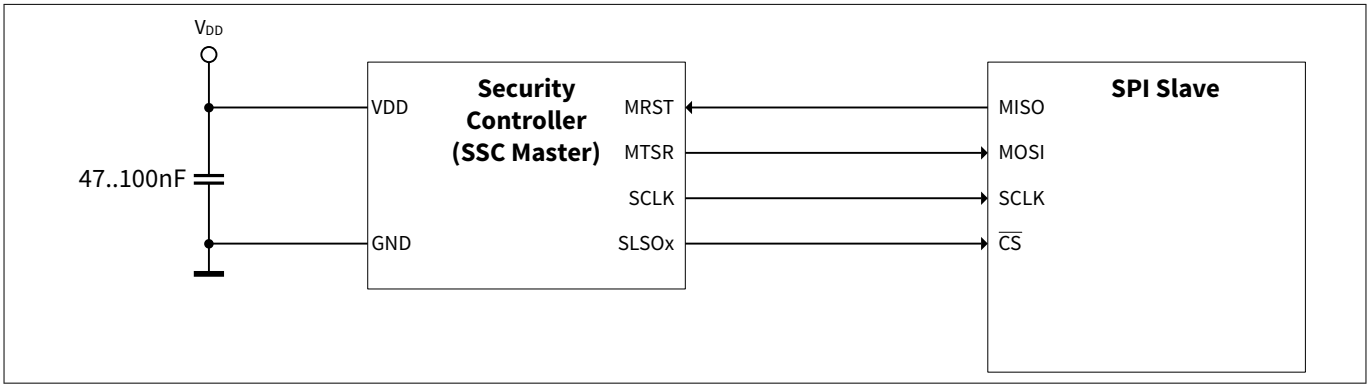

Figure 7 Connectivity as SPI master

The figure illustrates how to connect a security controller as SSC master to an SPI slave. Power connections are not shown.

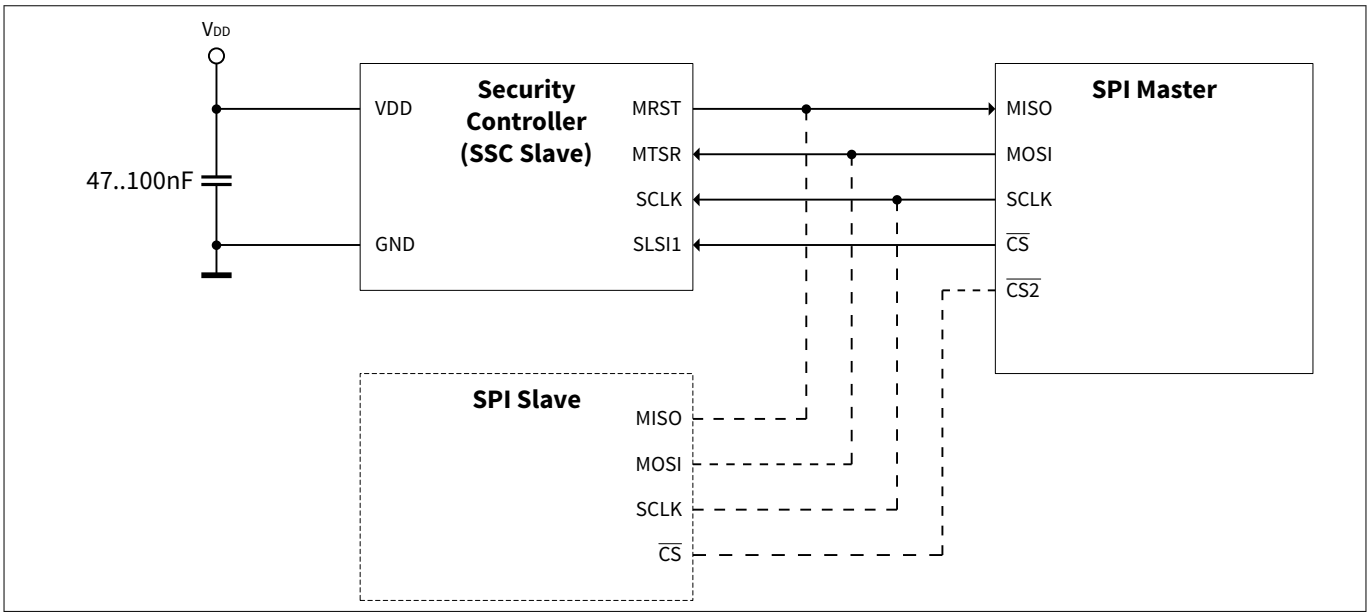

Figure 8 Connectivity as SPI slave

The figure illustrates how to connect a security controller as SSC slave to an SPI master. Power connections are not shown.

2.3.1.6 USB

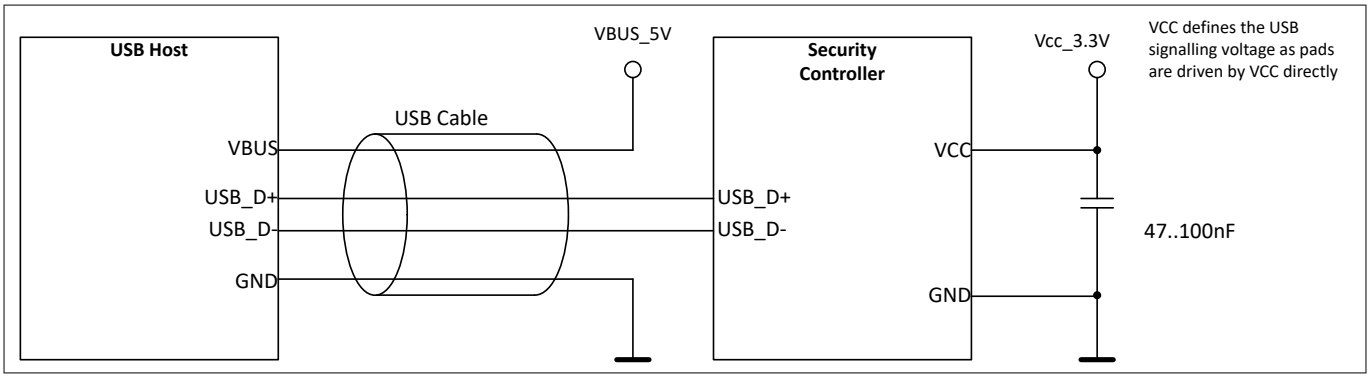

Figure 9 USB connectivity

The figure illustrates how to connect a USB host to the SLx97 security controller.

3 Description of delivery forms

This chapter provides information about available delivery forms and how the product's interfaces are assigned to the package pins.

For further information on compliance of the packages with European Parliament Directives, see ***RoHS compliance***.

For details and recommendations on the assembly of packages on PCBs, please see:

http://www.infineon.com/cms/en/product/technology/packages

3.1 External connectivity

Package pins are usually connected to a product pad and are used as inputs, outputs, or bi-directionally, depending on the available input and output stages. However in some products pins are not connected internally for example. The abbreviations listed here are used in the package description to classify each pin.

Table 2 Abbreviations for pin type

Abbreviation	Description
I	Input. Digital levels
O	Output. Digital levels
I/O	I/O is a bi-directional signal
PWR	Power
GND	Ground
NC	Not connected (JEDEC Standard). May be connected externally

Table 3 Abbreviations for buffer type

Abbreviation	Description
GPIO_I	GPIO input pad
GPIO_IO	GPIO input / output pad Open-drain/push-pull for output configurable Pull-up/pull-down configurable
SWP_IO	Input/output pad. Pull-down configurable
ISO_I_CLK	Input pad
ISO_I	Input pad
ISO_IO	Input/output pad

3.2 SMD packages

The following packages are available:

- PG-USON-8-3 (for SLE97 only)
- PG-VQFN-8-4, -6[1)]
- PG-VQFN-32-13, -20[2)]

The figures in the sections below show the following aspects of the package:

- Package outline: shows the package dimensions of the controller in the individual packages
- Package footprint: shows footprint recommendations
- Tape and reel packing
- Sample marking pattern: describes the productive sample marking pattern on the package
- Package layout: shows a simple layout with the pin numbers described in the pad-to-signal reference section

Note: Unless specified otherwise, all figure dimensions are given in mm.

Note: The drawings are for information only and not drawn to scale. More detailed information about package characteristics and assembly instructions is available on request.

3.2.1 PG-USON-8-3

Package outline

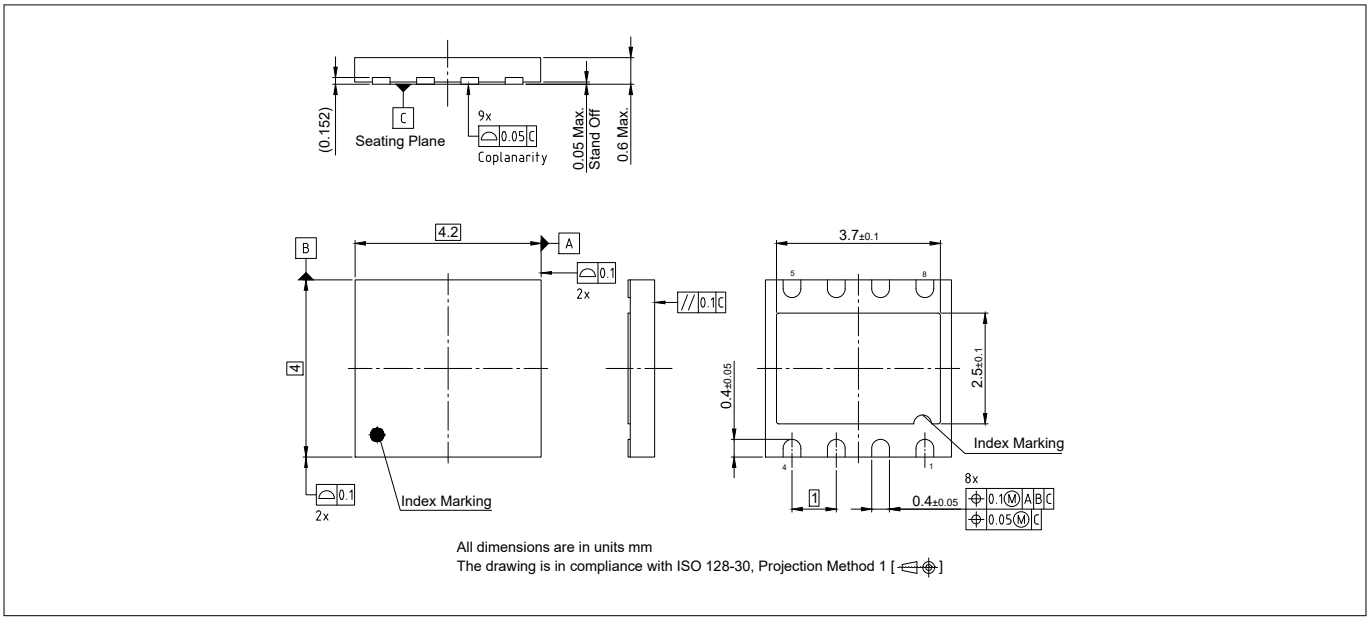

Figure 10 PG-USON-8-3 package outline

1 PG-VQFN-8-4 and PG-VQFN-8-6 are identical packages produced at different fabrication sites. For details, see the corresponding package specifications

2 PG-VQFN-32-13 and PG-VQFN--32-20 are identical packages produced at different fabrication sites. For details, see the corresponding package specifications

Description of delivery forms

Package footprint

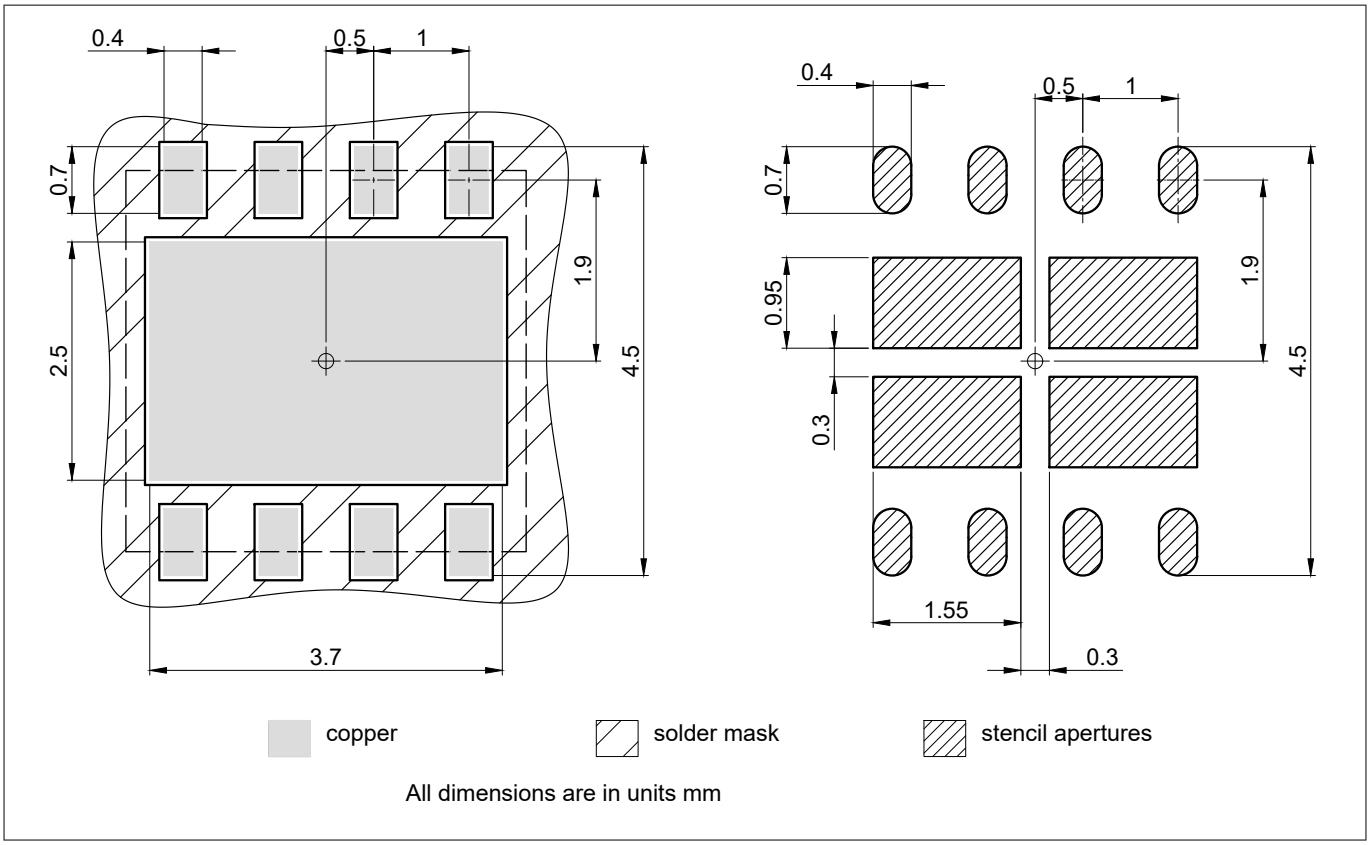

Figure 11 PG-USON-8-3 package footprint

Tape & reel packing

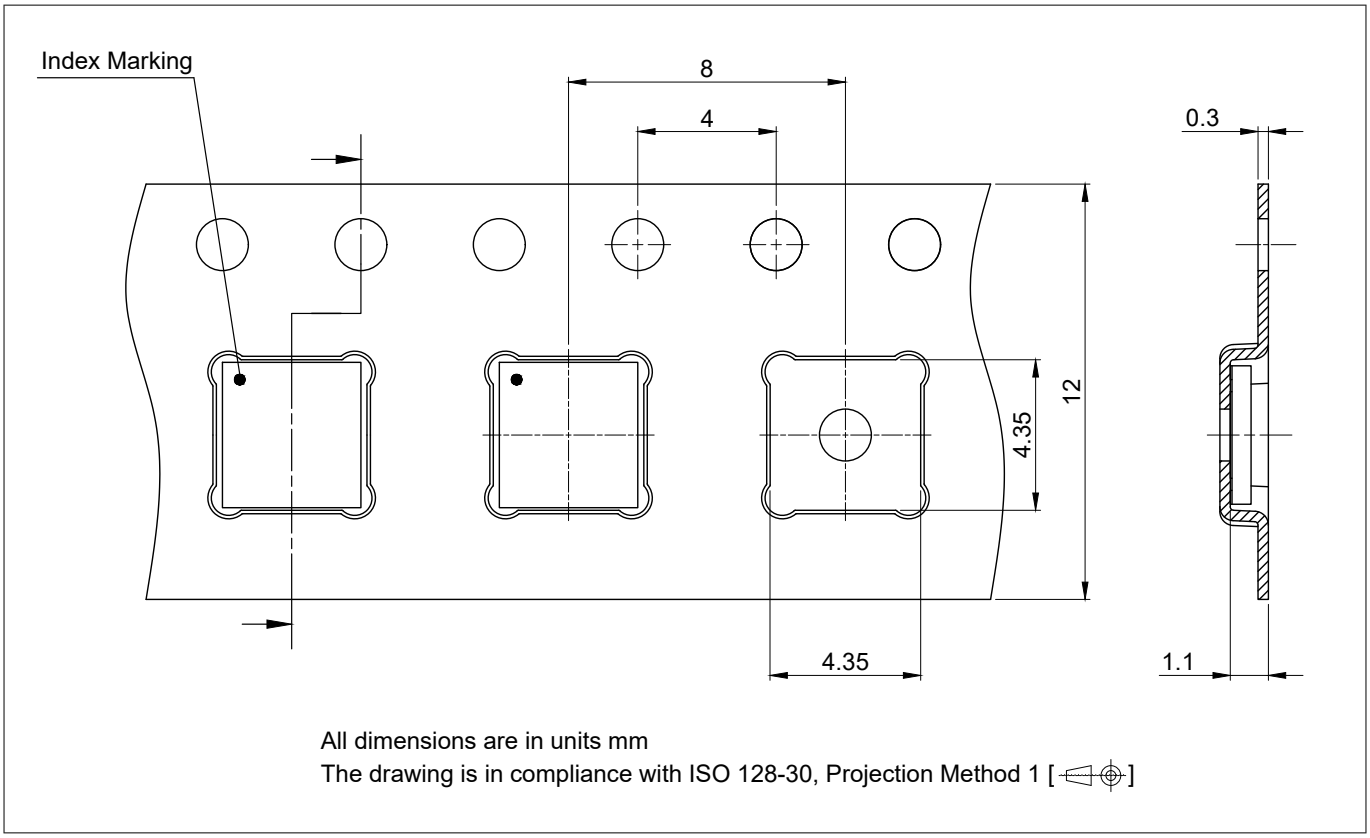

Figure 12 PG-USON-8-3 tape & reel packing

Production sample marking pattern

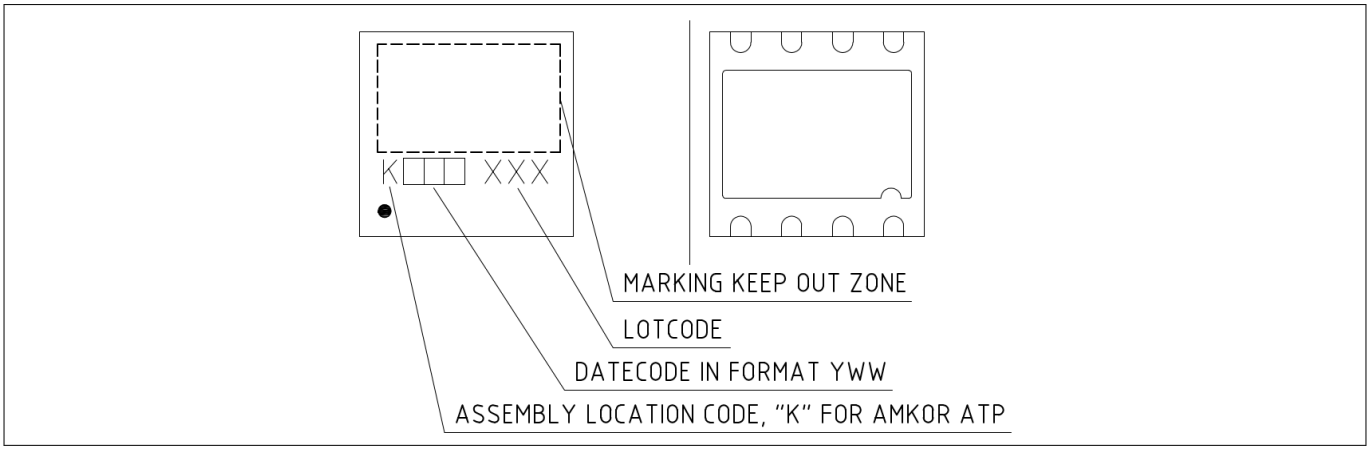

Figure 13 PG-USON-8-3 sample marking pattern

The dot indicates pin 01 for the chip. The following table describes the sample marking pattern:

Table 4 Marking table for PG-USON-8-3 packages

Indicator	Description
XXX	Lot code, defined and inserted during fabrication, issued by the packaging site
K□□□	Assembly location code:

Table 4 Marking table for PG-USON-8-3 packages (continued)

Indicator	Description
	• "K" for AMKOR ATP • <Y>: 2nd digit of production year • <WW>: production week

Package layout

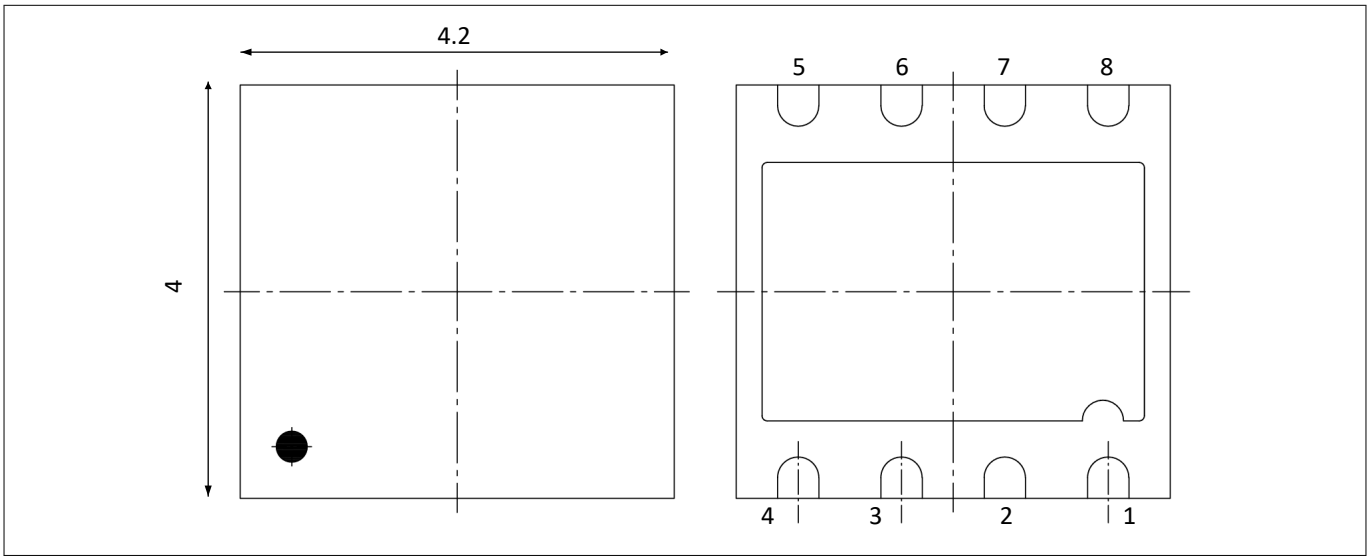

Figure 14 PG-USON-8-3 package layout

Pad-to-signal reference

The contacts and their functionality are given in the table below.

Table 5 Pad-to-signal reference for PG-USON-8-3

Pad	Symbol	Pin type	Buffer type	Signal function / remarks
1	GND	(n.a.)	–	Common ground reference. All GND pins must be tied together externally
2	SWP_IO0	I/O	SWP_IO	**SWP usage:** SWP_IO0
3	NC	–	–	No internal connection / do not connect externally
4	ISO_0	I/O	ISO_IO	**ISO/IEC 7816-3 card usage:** UART_IO **I2C usage:** SDA **IMM/SWIO usage:** IO
5	ISO_1	I	ISO_I_CLK	**ISO/IEC 7816-3 card usage:** UART_CLK **I2C usage:** SCL **IMM/SWIO usage:** CLK
6	ISO_2	I	ISO_I	**ISO/IEC 7816-3 card usage:** UART_RST **IMM/SWIO usage:** RST
7	NC	–	–	No internal connection / do not connect externally
8	V_{CC}	(n.a.)	–	Power and pad supply (V_{CC})

3.2.2 PG-VQFN-8-4, -6

Package outline

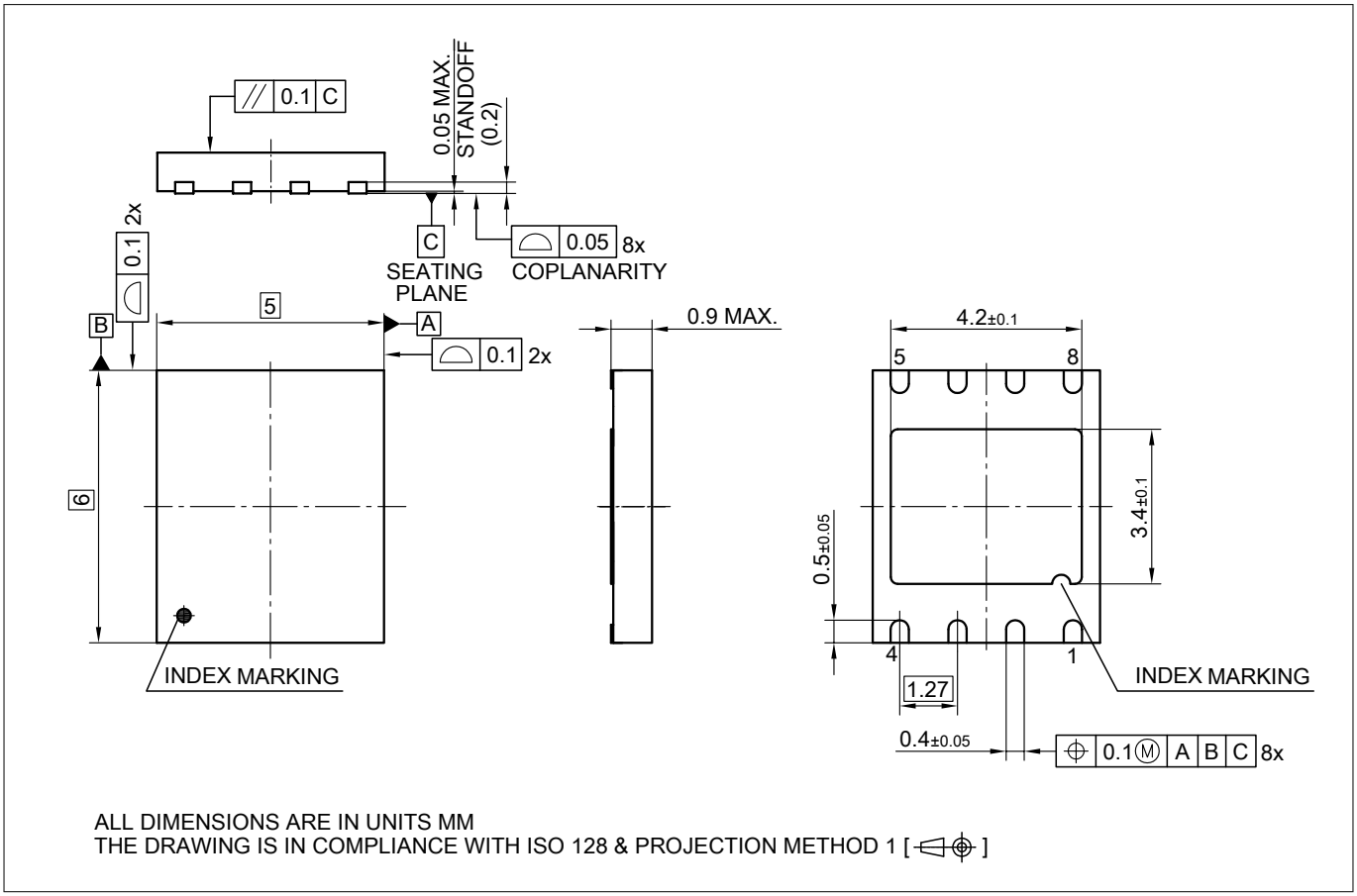

Figure 15 PG-VQFN-8-4, -6 package outline

Package footprint

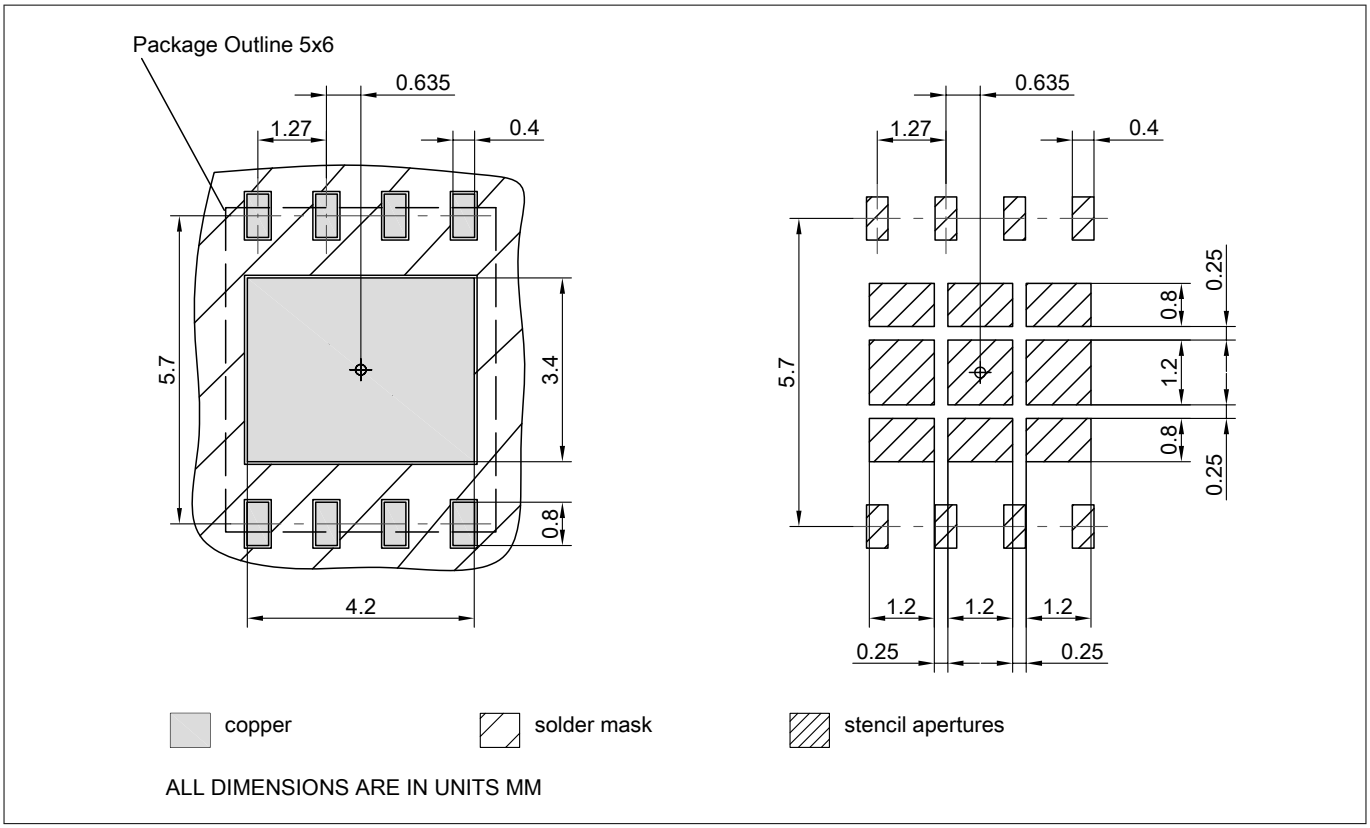

Figure 16 PG-VQFN-8-4, -6 package footprint

Tape & reel packing

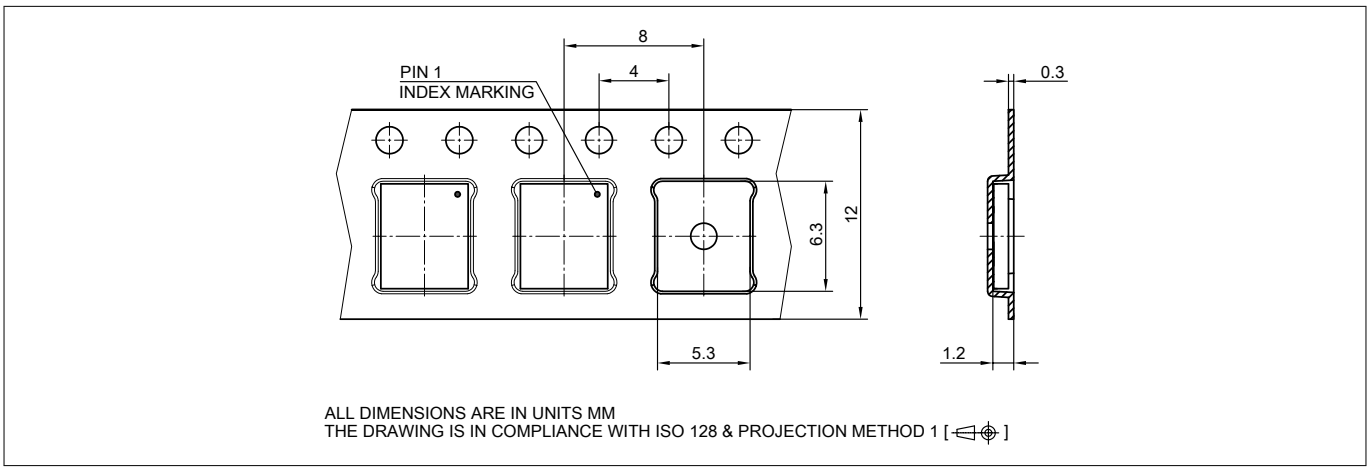

Figure 17 PG-VQFN-8-4, -6 tape & reel packing

Description of delivery forms

Production sample marking pattern

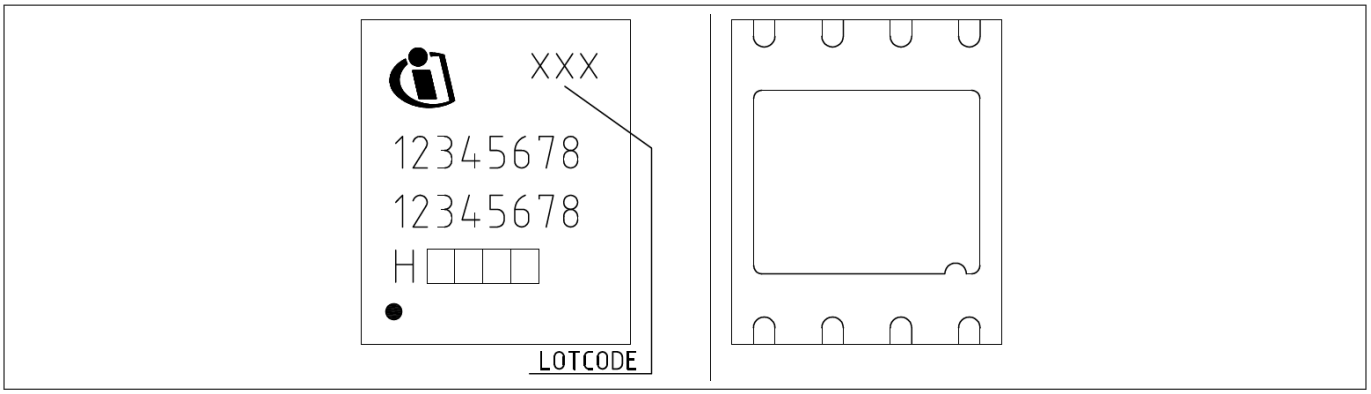

Figure 18 PG-VQFN-8-4, -6 sample marking pattern

The dot indicates pin 01 for the chip. The “lot code” and “serial number” are defined and inserted during fabrication.

The following table describes the sample marking pattern:

Table 6 Marking table for PG-VQFN-8-4, -6 packages

Indicator	Description
H□□□□	Engineering samples: “HE<YWW>”: • Halogen-free • Engineering Sample • <Y>: 2nd digit of production year • <WW>: production week (calendar week) Qualified production parts: “H<YYWW>”: • Halogen-free • <YY>: production year • <WW>: production week (calendar week)
XXX	Lot code, defined and inserted during fabrication, issued by the packaging site

Package layout

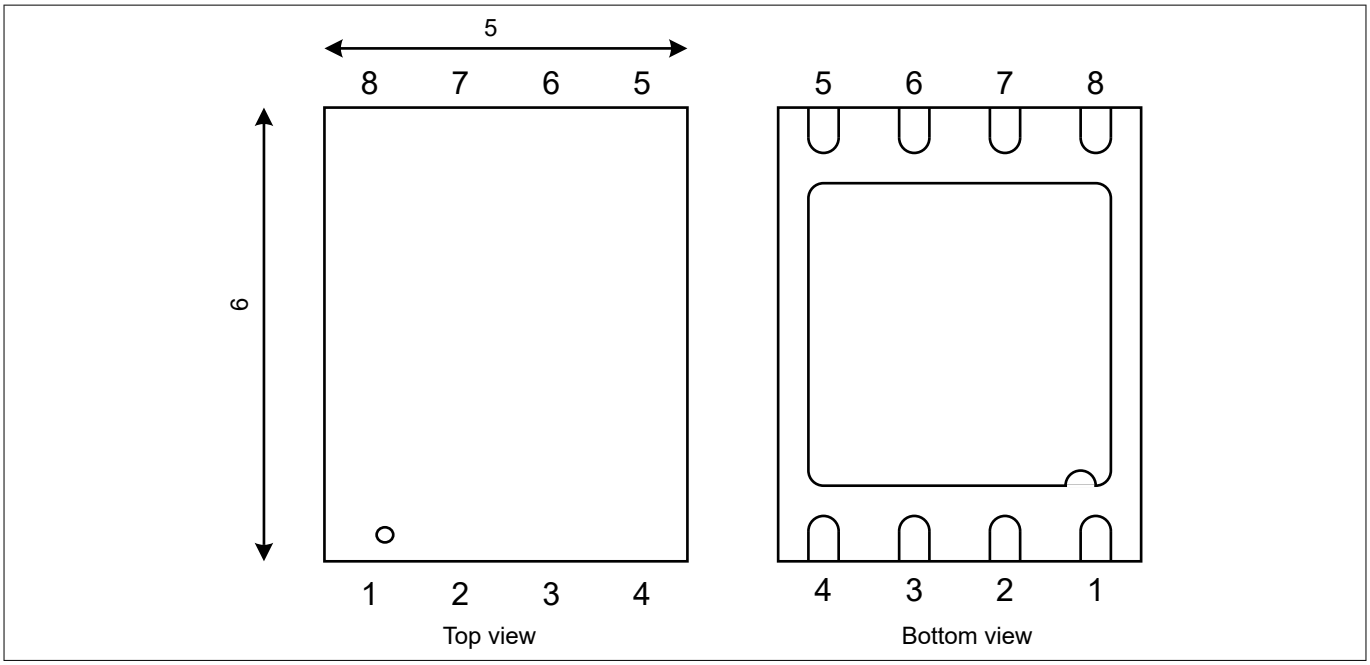

Figure 19 PG-VQFN-8-4, -6 package layout

Pad-to-signal reference

The contacts and their functionality are given in the table below.

Table 7 Pad-to-signal reference for PG-VQFN-8-4, -6 (USB)

Pad	Symbol	Pin type	Buffer type	Signal function / remarks
1	GND	(n.a.)	–	Common ground reference. All GND pins must be tied together externally
2	SWP_IO0	I/O	SWP_IO	**SWP usage:** SWP_IO0
3	ISO_0	I/O	ISO_IO	**ISO/IEC 7816-3 card usage:** UART_IO **I2C usage:** SDA **IMM/SWIO usage:** IO
4	D-	I/O	–	**USB usage:** D-/ Dm
5	D+	I/O	–	**USB usage:** D+/ Dp
6	ISO_1	I	ISO_I_CLK	**ISO/IEC 7816-3 card usage:** UART_CLK **I2C usage:** SCL **IMM/SWIO usage:** CLK
7	ISO_2	I	ISO_I	**ISO/IEC 7816-3 card usage:** UART_RST **IMM/SWIO usage:** RST
8	V_{CC}	(n.a.)	–	Power and pad supply (V_{CC})

Description of delivery forms

Table 8 Pad-to-signal reference for PG-VQFN-8-4, -6 (I2C)[3)]

Pad	Symbol	Pin type	Buffer type	Signal function / remarks
1	GND	(n.a.)	–	Common ground reference. All GND pins must be tied together externally
2	SWP_IO0	I/O	SWP_IO	**SWP usage:** SWP_IO0
3	ISO_0	I/O	ISO_IO	**ISO/IEC 7816-3 card usage:** UART_IO **IMM/SWIO usage:** IO
4	GPIO0.3	I/O	GPIO_IO	**GPIO function:** General purpose I/O **I2C usage:** SCL
5	GPIO0.2	I	GPIO_I	**GPIO function:** General purpose I/O **I2C usage:** SDA
6	ISO_1	I	ISO_I_CLK	**ISO/IEC 7816-3 card usage:** UART_CLK **IMM/SWIO usage:** CLK
7	ISO_2	I	ISO_I	**ISO/IEC 7816-3 card usage:** UART_RST **IMM/SWIO usage:** RST
8	V_{CC}	(n.a.)	–	Power and pad supply (V_{CC})

3 SLI/SLM products only. The I2C bond option is identified by an “I” in the marking pattern on the package. The availability of GPIO signals depends on the individual product. If the GPIO signal is not available, the pin must be treated as reserved, without any external connection

3.2.3 PG-VQFN-32-13, -20

Package outline

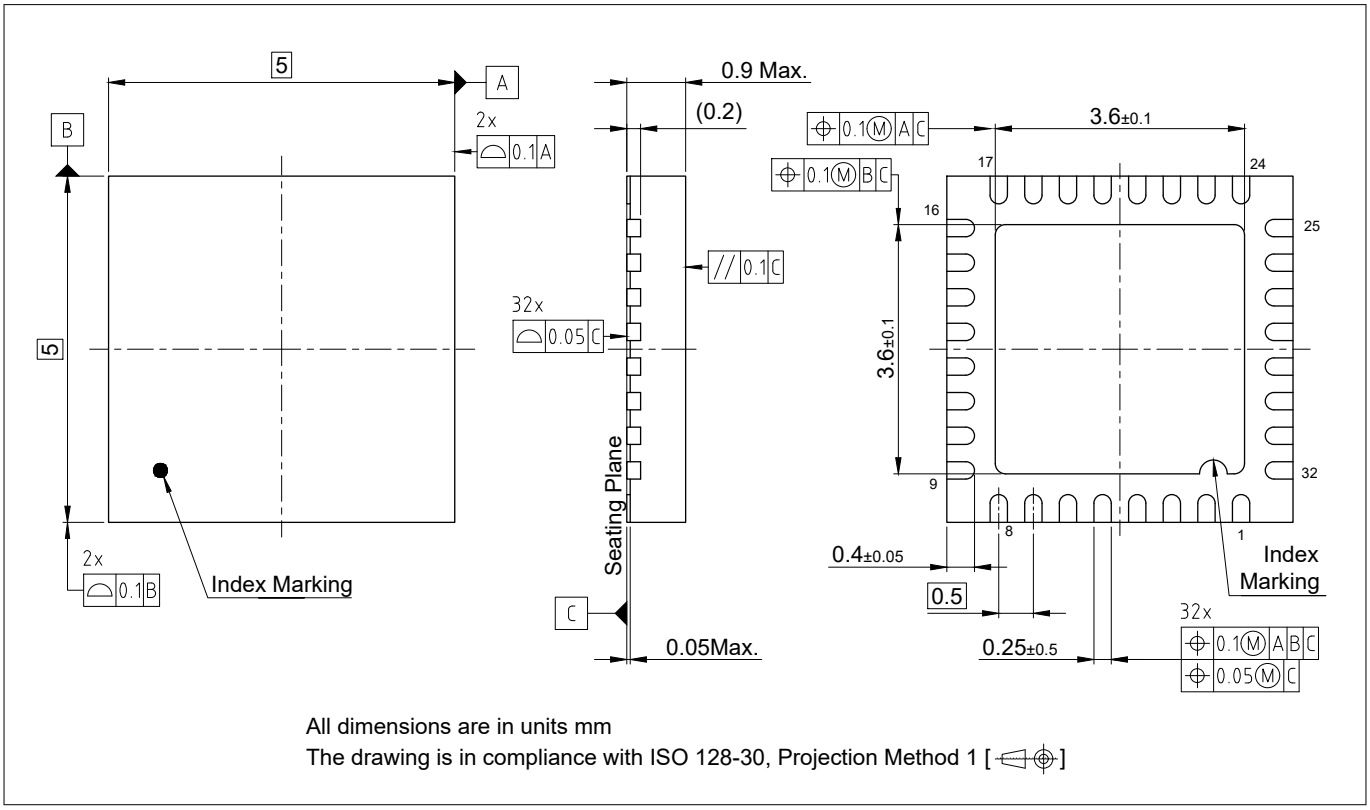

Figure 20 PG-VQFN-32-13, -20 package outline

Description of delivery forms

Package footprint

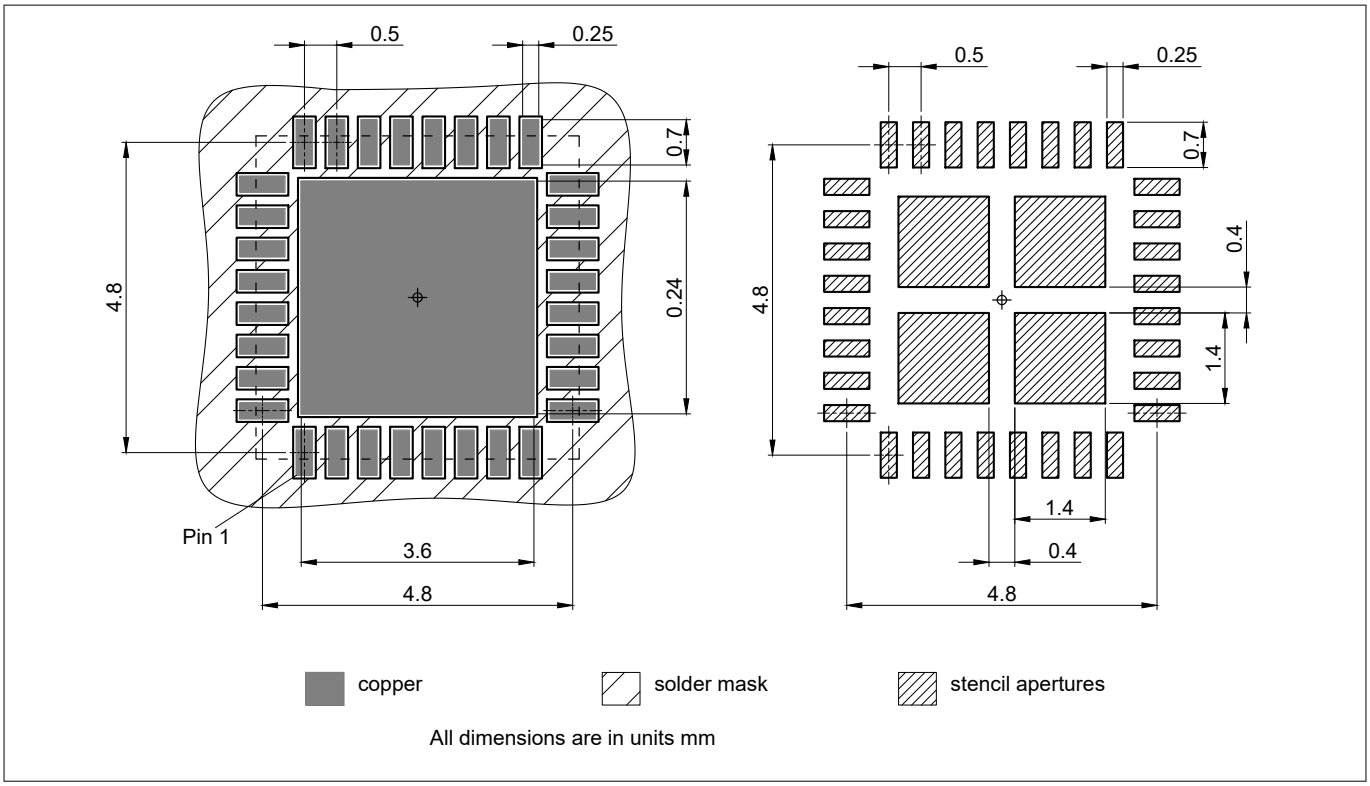

Figure 21 PG-VQFN-32-13, -20 package footprint

Tape & reel packing

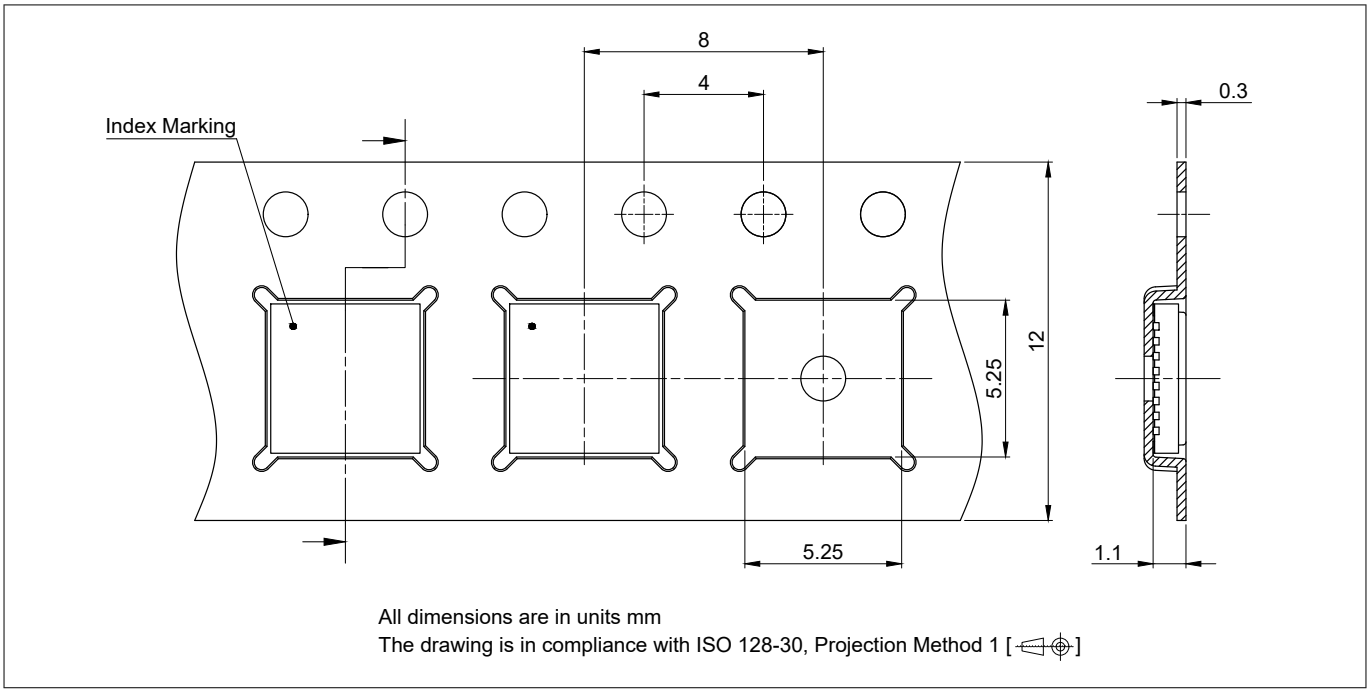

Figure 22 PG-VQFN-32-13, -20 tape & reel packing

Description of delivery forms

Production sample marking pattern

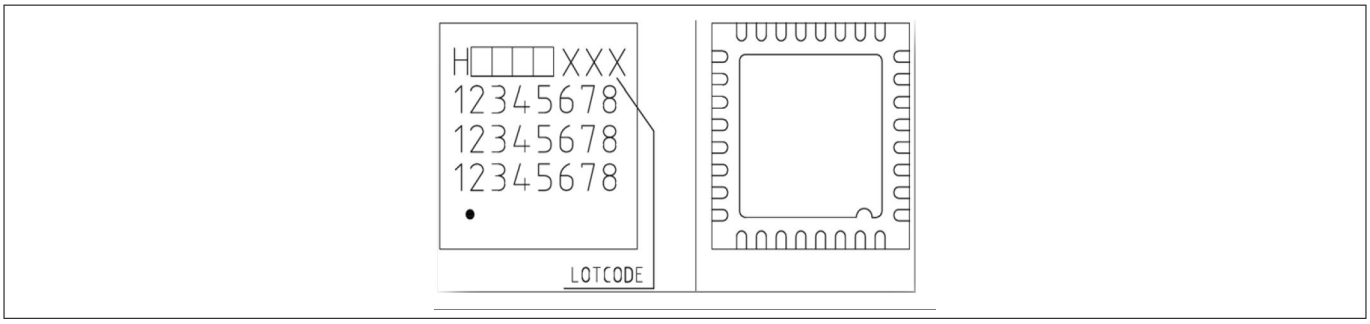

Figure 23 PG-VQFN-32-13, -20 sample marking pattern

The black dot indicates pin 01 for the chip. The following table describes the sample marking pattern:

Table 9 Marking table for PG-VQFN-32-13, -20 packages

Indicator	Description
H□□□□	Engineering samples: “HE<YWW>”: • Halogen-free • Engineering Sample • <Y>: 2nd digit of production year • <WW>: production week (calendar week) Qualified production parts: “H<YYWW>”: • Halogen-free • <YY>: production year • <WW>: production week (calendar week)
XXX	Lot code, defined and inserted during fabrication, issued by the packaging site
12345 (line 1)	Type code: "XXXX<N> • <N>: hardware derivative number
12345 (line 2)	1st Z: ‘T’ for test keys, ‘P’ for productive keys 2nd Z: ‘1’, ‘2’, ... for perso revision (revision of SW image/ certificate)
12345 (line 3)	For initial engineering samples only: ‘A’ for first assembly lot, ‘B’ for second assembly lot, ‘C’ for third assembly lot

Description of delivery forms

Package layout

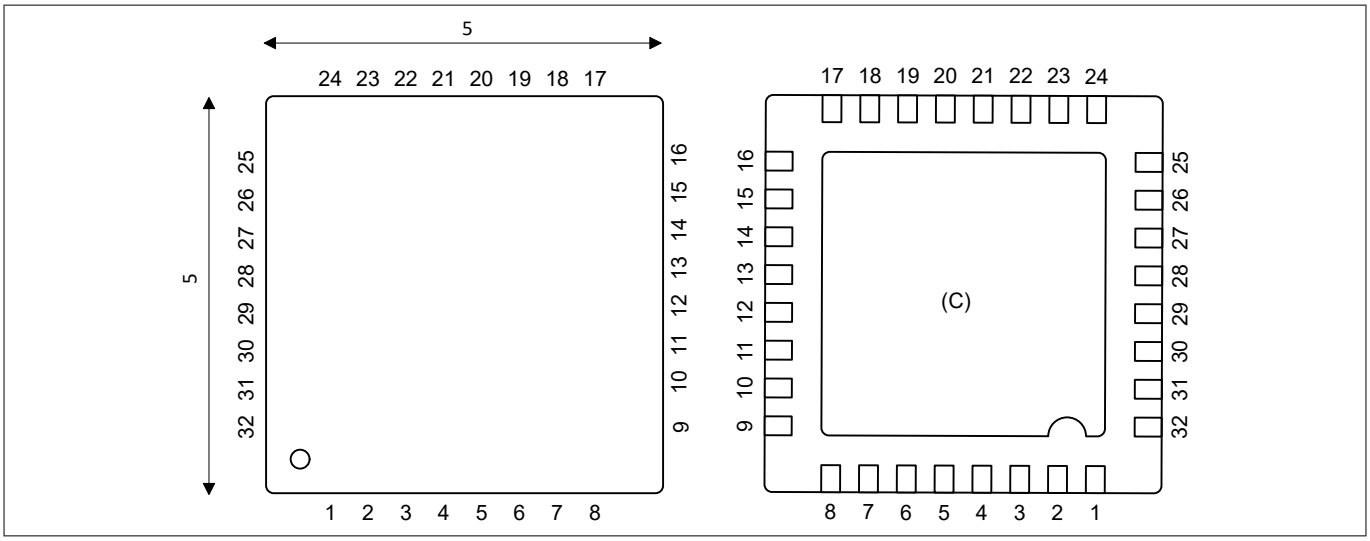

Figure 24 PG-VQFN-32-13, -20 package layout

Pad-to-signal reference

The contacts and their functionality are given in the table below. Pads not listed in the following table are not connected.

Table 10 Pad-to-signal reference for PG-VQFN-32-13, -20

Pad	Symbol	Pin type	Buffer type	Signal function / remarks
5	D+	I/O	–	**USB usage:** D+/ Dp
6	ISO_1	I	ISO_I_CLK	**ISO/IEC 7816-3 card usage:** UART_CLK **I2C usage:** SCL **IMM/SWIO usage:** CLK
7	ISO_2	I	ISO_I	**ISO/IEC 7816-3 card usage:** UART_RST **IMM/SWIO usage:** RST
8	V_{CC}	(n.a.)	–	Power and pad supply (V_{CC})
10	GPIO0.0	I	GPIO_I	**GPIO function:** General purpose I/O **SPI/SSC function:** MT, MR, SR, ST
11	GPIO0.1	I	GPIO_IO	**GPIO function:** General purpose I/O **SPI/SSC function:** MR, ST, SLSO
12	GPIO0.2	I	GPIO_I	**GPIO function:** General purpose I/O **I2C usage:** SDA **SPI/SSC function:** SCLK
13	GPIO0.3	I/O	GPIO_IO	**GPIO function:** General purpose I/O **I2C usage:** SCL **SPI/SSC function:** SLSO, SLSI
17	GND	(n.a.)	–	Common ground reference. All GND pins must be tied together externally
18	SWP_IO0	I/O	SWP_IO	**SWP usage:** SWP_IO0

Table 10 Pad-to-signal reference for PG-VQFN-32-13, -20 (continued)

Pad	Symbol	Pin type	Buffer type	Signal function / remarks
19	ISO_0	I/O	ISO_IO	**ISO/IEC 7816-3 card usage:** UART_IO **I2C usage:** SDA **IMM/SWIO usage:** IO
20	D-	I/O	–	**USB usage:** D-/ Dm

*Note: The exposed die pad referenced as (C) in **Figure 24** must be connected to the common ground reference (GND) for heat distribution.*

3.3 Chip scale packages

The following packages are available:

- SG-WFWLB-16-2,-3[4)]
- SG-WFWLB-16-5[5)]

Note: Chip scale packages are only available for SLE 97 and SLM 97 products.

*Note: Due to the lack of mechanical protection chips delivered in this package are sensitive to mechanical damage. Therefore a higher risk of increased production fall-off rate compared to mold packages should be considered. For further information and specialties of this package please see "**Recommendations for board Assembly of Infineon xWLy Packages**" on the Infineon Homepage.*

The figures in the sections below show the following aspects of the package:

- Package outline: shows the package dimensions of the controller in the individual packages
- Package footprint: shows footprint recommendations
- Tape and reel packing
- Sample marking pattern: describes the productive sample marking pattern on the package
- Package layout: shows a simple layout with the pin numbers described in the pad-to-signal reference section

Note: Unless specified otherwise, all figure dimensions are given in mm.

Note: The drawings are for information only and not drawn to scale. More detailed information about package characteristics and assembly instructions is available on request.

4 SG-WFWLB-16-2 produced in Dresden, SG-WFWLB-16-3 produced at TSMC

5 SG-WFWLB-16-5 produced for industrial applications

3.3.1 SG-WFWLB-16-2, -3, -5

Package outline

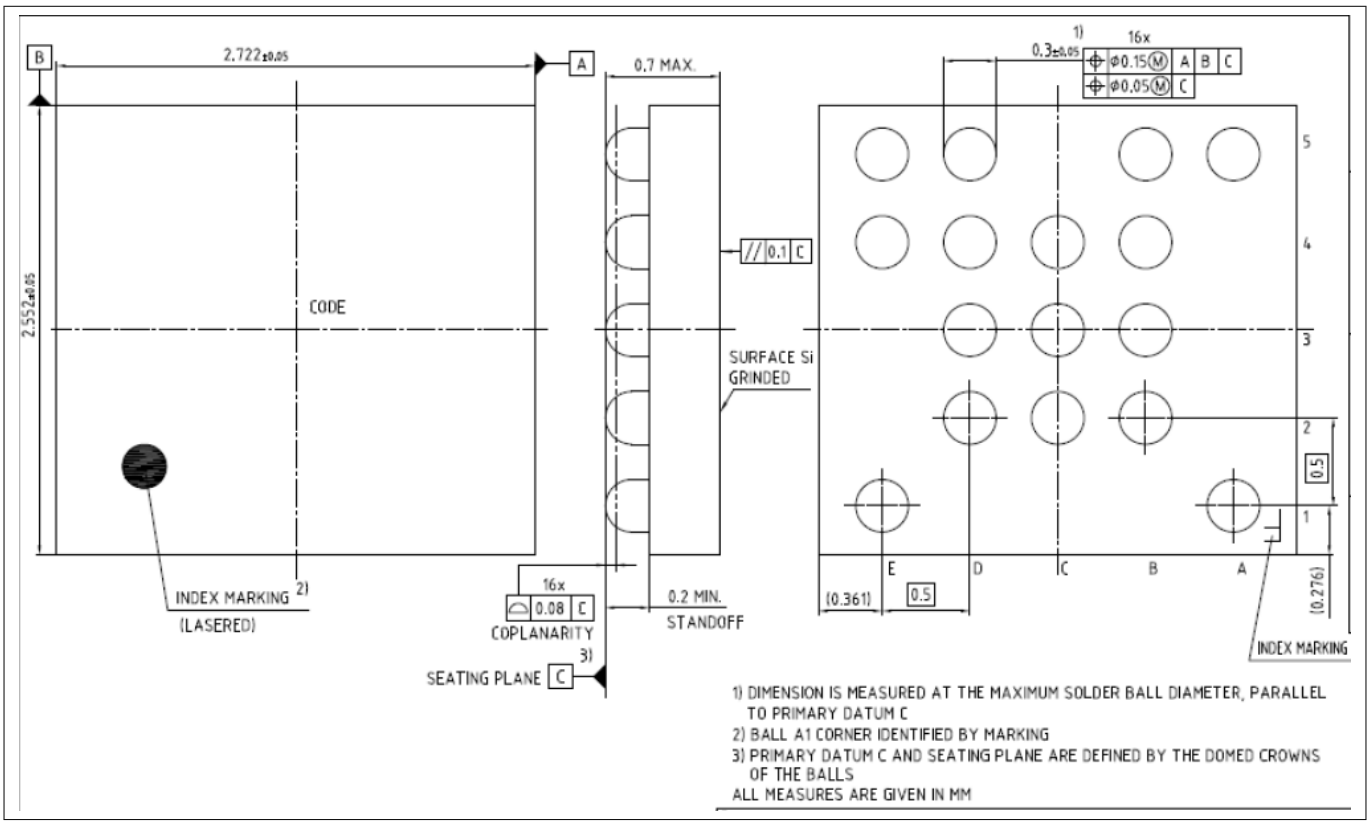

Figure 25 SG-WFWLB-16 package outline

Package footprint

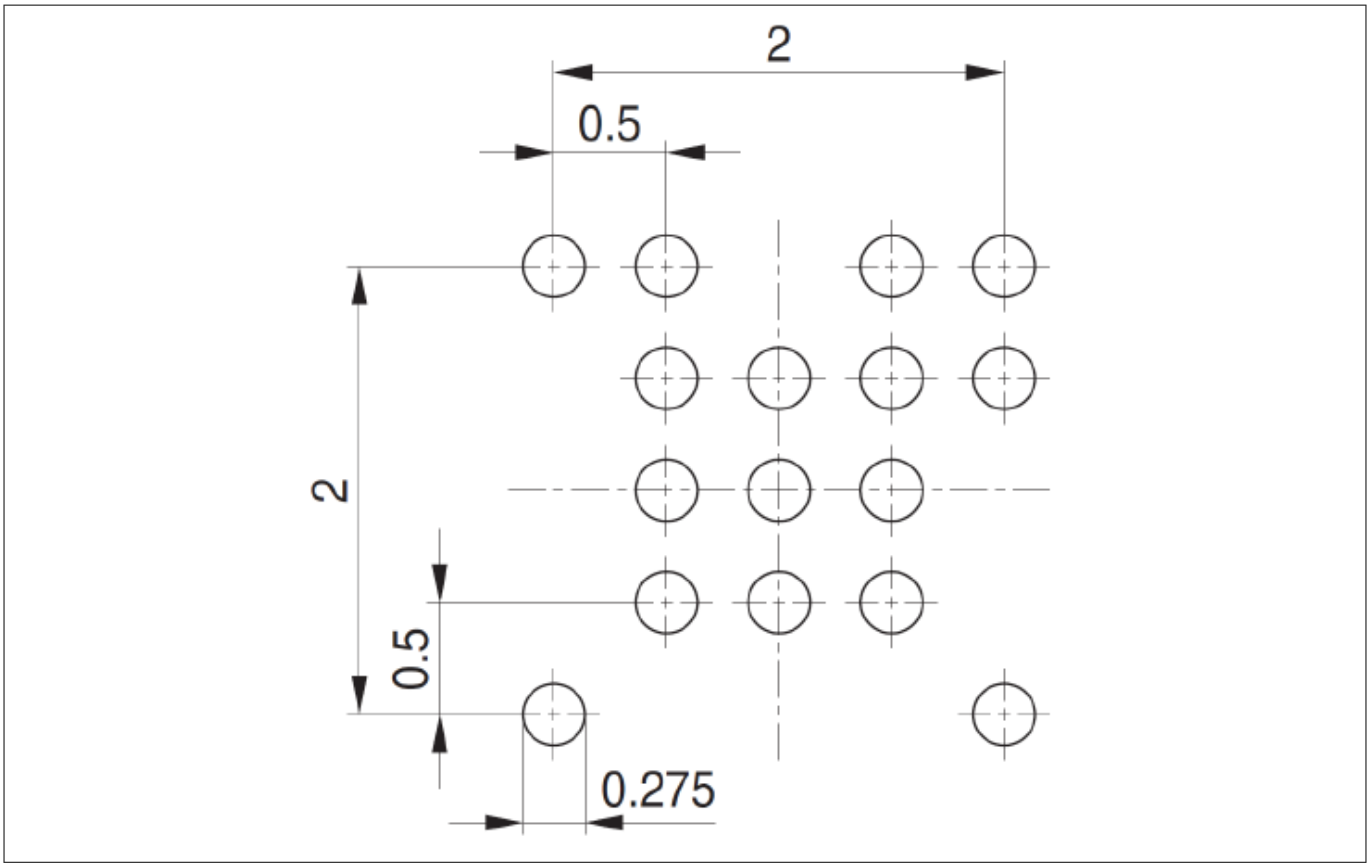

Figure 26 SG-WFWLB-16 package footprint

Tape & reel packing

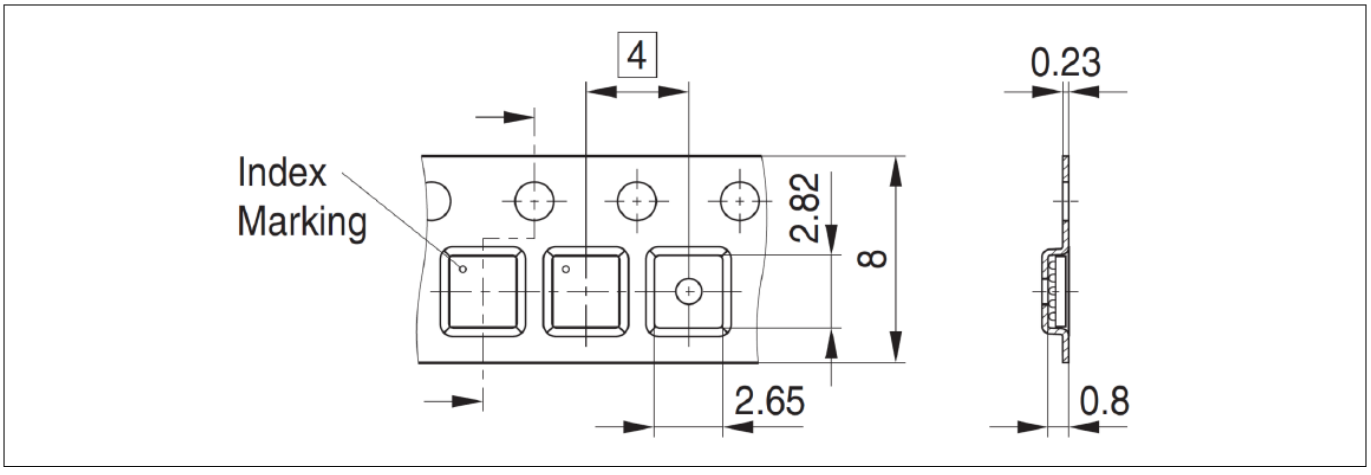

Figure 27 SG-WFWLB-16 tape & reel packing

Production sample marking pattern

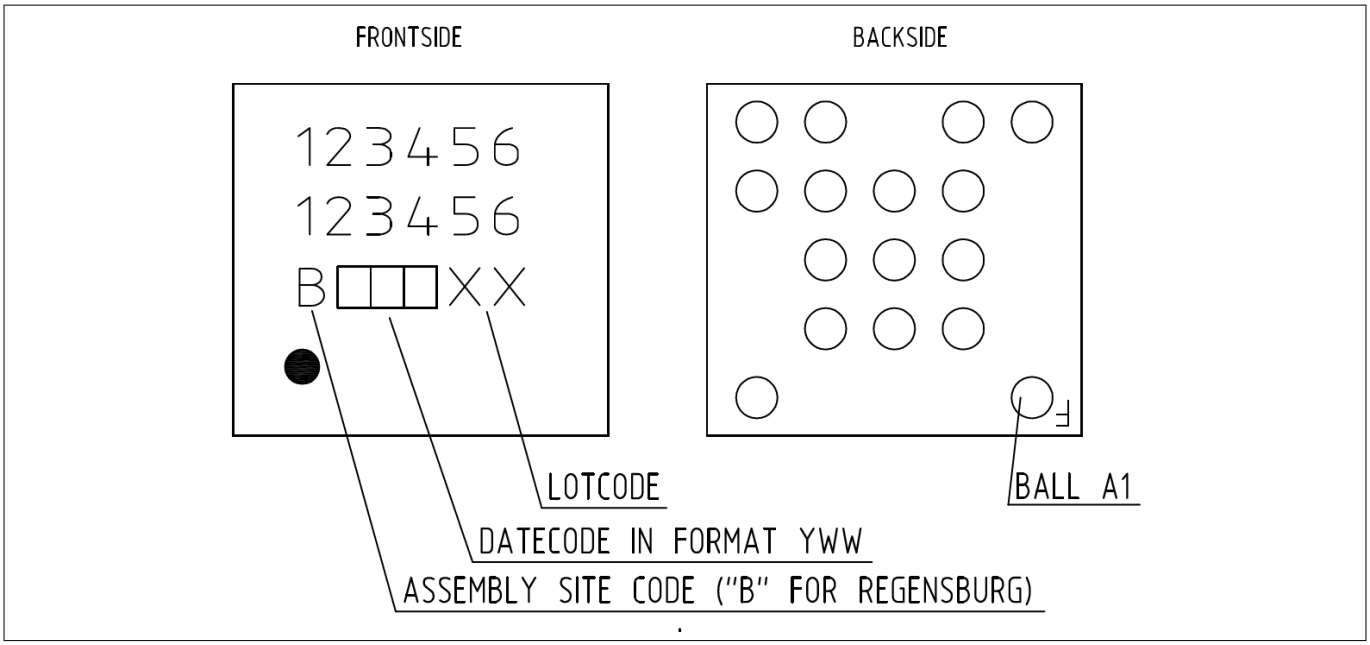

Figure 28 SG-WFWLB-16 sample marking pattern

The dot indicates pin 01 for the chip. The following table describes the sample marking pattern:

Table 11 Marking table for SG-WFWLB-16 packages

Indicator	Description
XX	Lot code, defined and inserted during fabrication, issued by the packaging site
123456	Type code: "XXXX<N> • <N>: hardware derivative number
B□□□	Qualified production parts: “B<YWW>”: • Assembly site code, e.g. B for Regensburg • <Y>: 2nd digit of the production year • <WW>: production week Engineering samples are additionally marked with 'ES'

Package layout

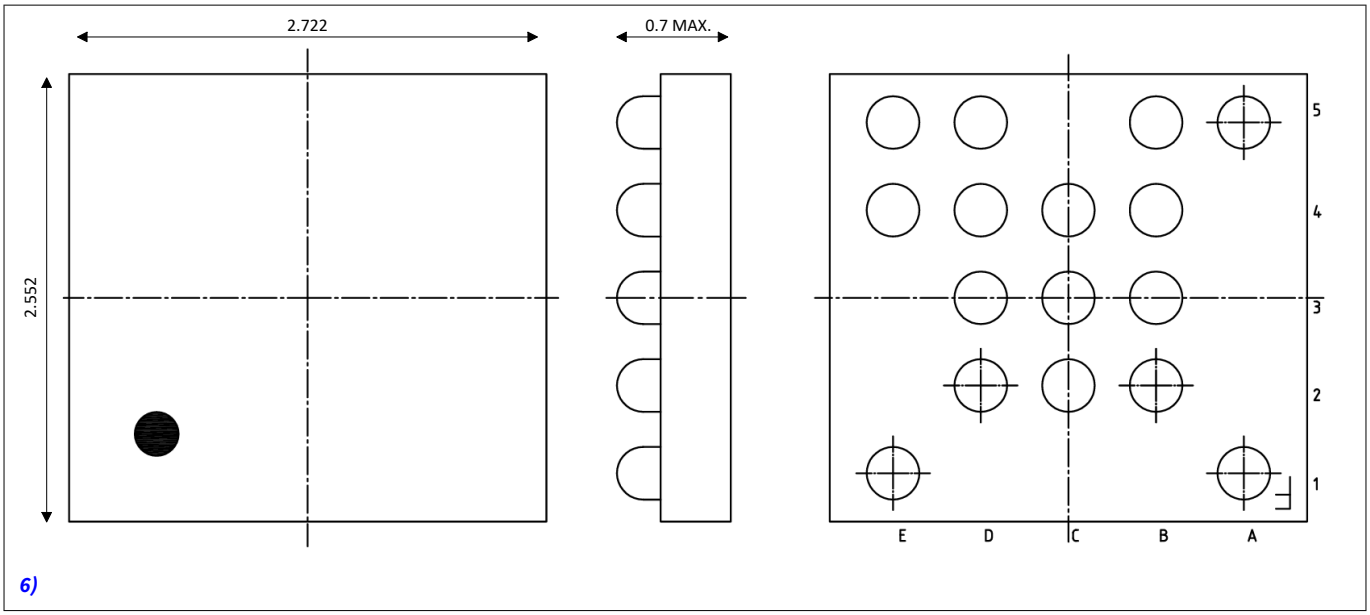

Figure 29 SG-WFWLB-16 package layout

Pad-to-signal reference

The contacts and their functionality are given in the table below.

Table 12 Pad-to-signal reference for SG-WFWLB-16

Pad	Symbol	Pin type	Buffer type	Signal function / remarks
A1, B2, D2, E1	NC	–	–	No internal connection / do not connect externally
A5, C3	V_{CC}	(n.a.)	–	Power and pad supply (V_{CC})
B3	ISO_2	I	ISO_I	**ISO/IEC 7816-3 card usage:** UART_RST **IMM/SWIO usage:** RST
B4	ISO_1	I	ISO_I_CLK	**ISO/IEC 7816-3 card usage:** UART_CLK **I2C usage:** SCL **IMM/SWIO usage:** CLK
B5	GPIO0.0	I	GPIO_I	**GPIO function:** General purpose I/O **SPI/SSC function:** MT, MR, SR, ST
C2, E5	GND	(n.a.)	–	Common ground reference. All GND pins must be tied together externally
C4	GPIO0.2	I	GPIO_I	**GPIO function:** General purpose I/O **I2C usage:** SDA **SPI/SSC function:** SCLK
D3	ISO_0	I/O	ISO_IO	**ISO/IEC 7816-3 card usage:** UART_IO

6 All dimensions in mm

Table 12 Pad-to-signal reference for SG-WFWLB-16 (continued)

Pad	Symbol	Pin type	Buffer type	Signal function / remarks
				I2C usage: SDA **IMM/SWIO usage:** IO
D4	GPIO0.3	I/O	GPIO_IO	**GPIO function:** General purpose I/O **I2C usage:** SCL **SPI/SSC function:** SLSO, SLSI
D5	GPIO0.1	I	GPIO_IO	**GPIO function:** General purpose I/O **SPI/SSC function:** MR, ST, SLSO
E4	SWP_IO0	I/O	SWP_IO	**SWP usage:** SWP_IO0

4 Electrical characteristics

This section summarizes certain electrical characteristics of the controllers. It provides operational characteristics as well as electrical DC and AC characteristics and particular interface characteristics.

4.1 Absolute maximum ratings

Table 13 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	- 0.3	–	7.0	V	–
Input voltage	V_{IN}	- 0.3	–	V_{CC} + 0.3	V	–
Operating temperature (ambient)	T_A	- 25	–	85	°C	T_J must be kept. For standard grade SLE97
		- 40	–	105	°C	T_J must be kept. For automotive grade SLI97 and industrial grade SLM97
Junction temperature	T_J	- 25	–	110	°C	For standard grade SLE97
		- 40	–	110	°C	For automotive grade SLI97 and industrial grade SLM97
Storage temperature	T_S	- 40	–	125	°C	–
Pulse voltage ESD protection of ISO pad group ISO, I^2C	V_{ESD}	4000	–	–	V	ISO 7816-1 *[4]*
Pulse voltage ESD protection of SWP, USB pads	V_{ESD}	4000	–	–	V	
Pulse voltage ESD protection GPIO pad group, SPI, I^2C	V_{ESD}	2000	–	–	V	

Notes:

1. *The values stated in the table may be further restricted for particular products (i.e. sales codes).*
2. *All voltages are referenced to the power supply ground in the corresponding package, unless otherwise specified.*
3. *Stresses exceeding the values listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions whose values exceed those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability, including NVM data retention and write/erase endurance.*

4.2 Operational characteristics

This section specifies the AC and DC characteristics of the controller, along with details relating to the specific interfaces provided by the controller.

Notes:

1. *T_A as given for the operating temperature range of the controller unless otherwise stated.*
2. *All currents flowing into the controller are considered positive.*

4.2.1 DC electrical characteristics

Table 14 DC characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	1.62	–	5.5	V	Overall functional voltage range[7]
		4.5	5.0	5.5	V	ISO/IEC 7816-3 Class A
		2.7	3.0	3.3	V	ISO/IEC 7816-3 Class B
		3.0	3.3	3.6	V	STD USB 2.0
		2.7	3.3	3.6	V	IC USB 3.0
		1.62	1.8	1.98	V	ISO/IEC 7816-3 Class C ETSI TS 102613
		1.65	1.8	1.95	V	ISO Class *C**, IC USB 1.8[8]
Supply current	I_{CC}	–	–	21	mA	f_{SYS} = 44 MHz
Supply current spikes[9]	I_{CCD}					
		–	–	100	mA	Q ≤ 20 nAs ISO Class A
		–	–	50	mA	Q ≤ 10 nAs ISO Class B
		–	–	30	mA	Q ≤ 6 nAs ISO Class C
Supply current in current limitation mode	I_{MAX}	–	–	10	mA	V_{CC} < 5.0 V
		–	–	6	mA	V_{CC} < 3.3 V
		–	–	5	mA	V_{CC} in ETSI TS 102613 low power mode range
		–	–	4	mA	V_{CC} < 1.98 V

7 The SWP pad and the GPIO pad group are 5 V tolerant but operate only up to 3.6 V.

8 Product specific restrictions apply.

9 The maximum spike amplitude and spike charge defined by ETSI 102 221 and ETSI 102 613 are kept within the specified range. The maximum spike length which is technically irrelevant for terminal regulator and voltage stability is typically kept within the specified range.

Table 14 DC characteristics (continued)

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Supply current in sleep mode	I_{CCS1}	–	–	200	µA	T_A = 25°C, f_{UART_CLK} = 1 MHz; All inputs at V_{CC}, No peripheral active
	I_{CCS2}	–	–	100	µA	Class B / Class C T_A = 25°C, CLK off RNG oscillators and DCO off RST and IO at V_{CC}
	I_{CCS3}	–	–	200	µA	T_A = 25°C, RNG oscillators and DCO off All inputs at V_{CC} After I^2C mode start-up

4.2.2 AC electrical characteristics

Table 15 AC characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
External supply VCC						
Supply ramp-up time	t_{VCCR}	1[10]	-	10^7	µs	0 to 100% of target supply voltage
Wait until start of application program	t_{WUC}	400	-	16,000[11]	clk pulses	
Security Sensor Threshold						
Analog high frequency filter	f_{HFA}	-	16	-	MHz	
Digital low frequency sensor		-	-	1	MHz	
NVM						
Erase + Write time	t_{WR}	-	-	2.5	ms	For standard grade SLE97
		-	2.5	-	ms	For automotive grade SLI97 and industrial grade SLM97
Erase Page	t_{ER}	-	1.5	-	ms	
Fast Write Page	t_{WRP}	-	1.0	-	ms	Pre-erased, no verify included, no software times included
Power Down time[12]	t_{EEPD}	-	-	10	µs	
Recovery time	t_{REC}	-	-	54	µs	
System						
Internal frequency	f_{SYS}	-	-	44 (typical)	MHz	Programmable down to 1/32. Maximum frequency is product specific
1 MHz frequency	f_{1MHZ}	-	1.0	-	MHz	f_{SYS} = 44 MHz
TRNG						
Generate 8 random bits[13]	t_{TRNG-8}	1584	2072	27200	cycles	f_{SYS} = 44 MHz; RNG_PRESCAL = 5, min./max compression 8/128

10 At faster supply ramp times chip internal ESD elements temporary causing a cross current between VCC and GND larger than allowed (I_{CC}).

11 Max. value specified by ISO 7816 is 40,000 clock pulses until 1st ATR byte is sent

12 The EEPROM needs a time t_{EEPd} for power down; if sleep mode is requested and a wake-up condition is pending, e.g. timer full flag = 1_B, the total time the EEPROM is not available is $t_{EEPd} + t_{Rec}$.

13 The generation time for 16 bits is simply twice the value given in this table

4.2.2.1 Operating restrictions

In order to maintain proper operation of the chip the following restrictions have to be considered:

- Crypto@2304T and SCP must not operate at the same time. The time between both operations must be at least 100 clocks.
- Crypto@2304T must not operate during erasing or writing of the NVM. The time between both operations must be at least 100 clocks.
- Changing of fSYS is not allowed during:
  - NVM erasing or writing.
  - Crypto@2304T operation.
  - DES operation.
- In current limitation mode ABFS and AFFS power management functions must be enabled.
- Controllers with stacked flash must avoid over heating. A corresponding application note describes how to operate such devices.

4.2.2.2 Power-up considerations

The rampup times given in ***AC characteristics*** apply under the assumption of a linear rise in voltage from 0% to 100% of the target voltage level. However, owing to possible current spike effects, it is recommended to follow the voltage characteristics shown in the figure below.

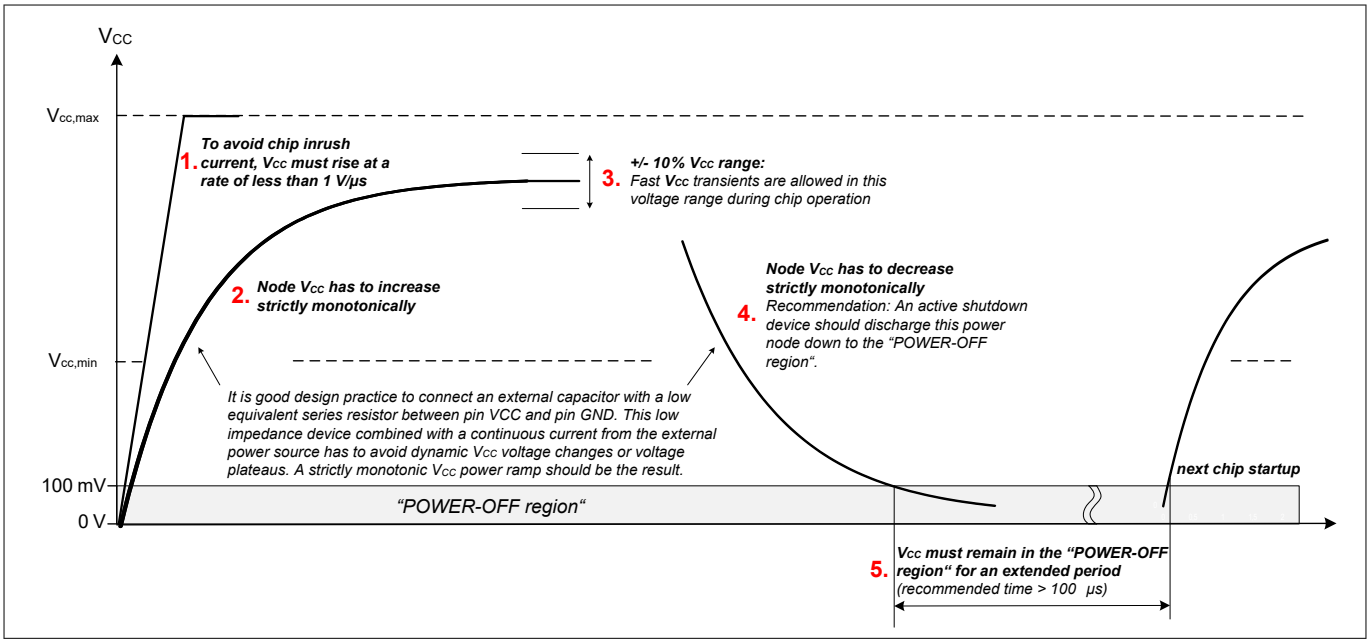

Figure 30 Recommended power-up behavior

4.3 Particular interface characteristics

This chapter provides electrical characteristics with respect to operation of particular interfaces of the controller.

Note: Unless otherwise stated, all values in this section are measured at the pins of the used package, i.e., the resistance, capacitance and inductance, for example, of the package and the bond wires are already included in these values!

4.3.1 ISO/IEC 7816-3 card interface characteristics

The electrical characteristics of the pads described below comply with the standards ISO/IEC 7816-3 *[6]*, GSM 11.11 *[9]*, GSM 11.12 *[10]*, GSM 11.18 *[11]*, ETSI TS 102.221 *[8]* and EMVCo standards *[1]*.

Notes:

1. *All currents flowing out of the pad are considered to be positive.*

2. *Symbol T_A describes the ambient temperature range.*

Table 16 ISO/IEC 7816-3 card maximum ratings

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Pad input voltage	V_I	−0.3		V_{CC_ISO} + 0.3	V	

Table 17 ISO/IEC 7816-3 card DC electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
UART_IO, bidirectional port	V_{IH}	0.7 * V_{CC}	–	V_{CC} + 0.3	V	I_{IH} = - 20 µA ... + 20 µA
	V_{IL}	- 0.3	–	0.2 x V_{CC}	V	I_{IL} = - 1 mA ... + 20 µA
	V_{OH}	0.7 * V_{CC}	–	V_{CC} + 0.3	V	I_{OH} = - 20 µA ... + 20 µA
ISO/IEC 7816-3 *[6]*						
UART_IO, bidirectional port	V_{OL}	0	–	0.4	V	I_{OL} = 1 mA Class A
		–	–	0.15 * V_{CC}	V	I_{OL} = 1 mA Class B
		–	–	0.15 * V_{CC}	V	I_{OL} = 0.5 mA Class C
GSM 11.11 *[9]*, GSM 11.12 *[10]*, GSM 11.18 *[11]*, ETSI TS 102.221 *[8]*						
UART_IO, bidirectional port	V_{OL}	–	–	0.4	V	I_{OL} = -1 mA Class A & B
		–	–	0.3	V	I_{OL} = -1 mA Class C
EMVCo standards *[1]*						
UART_IO, bidirectional port	V_{OL}	–	–	0.08 * V_{CC}	V	I_{OL} = 1.0 mA Class A
		–	–	0.15 * V_{CC}	V	I_{OL} = 0.5 mA Class B
		–	–	0.15 * V_{CC}	V	I_{OL} = 0.5 mA Class C
UART_RST	V_{IH}	0.8 * V_{CC}	–	V_{CC} + 0.3	V	I_{IH} = - 20 µA ... + 20 µA

Table 17 ISO/IEC 7816-3 card DC electrical characteristics (continued)

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
	V_{IL}	- 0.3	–	0.2 * V_{CC}	V	I_{IL} = - 50 µA ... + 20 µA
UART_CLK	V_{IH}	0.7 * V_{CC}	–	V_{CC} + 0.3	V	I_{IH} = - 20 µA ... + 20 µA
	V_{IL}	- 0.3	–	0.2 * V_{CC}	V	I_{IL} = - 20 µA ... + 20 µA

Table 18 ISO/IEC 7816-3 card AC electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
ISO_0, UART_IO						
Rise/fall time	t_R, t_F	–	–	1	µs	30 pF external
Pad input capacitance	C_{IN}			5	pF	Bare die (no package considered)
ISO_2, UART_RST						
Rise/fall time	t_R, t_F	–	–	1	µs	30 pF external
Hold time low	t_{HR}	80	–	–	µs	Both conditions have to be kept. External clock pulses
		400	–	–	clk	
Pad input capacitance	C_{IN}			2	pF	Bare die (no package considered)
ISO_1, UART_CLK						
External frequency	f_{UART_CLK}	1	–	10	MHz	@ specified duty cycle
Rise/fall time	t_R, t_F	–	–	0.1*1/ f_{UART_CLK}	ns	0.1 V_{CC} to 0.9 V_{CC} = V_T 0.5 V_{CC}
Duty cycle		40	–	60	%	
Pad input capacitance	C_{IN}			2	pF	Bare die (no package considered)

4.3.2 I2C interface characteristics

The electrical characteristics of the I2C interface are given below.

Table ***Table 19*** describes the requirements for devices connected to the standard and fast mode I^2C interface. The SCL and SDA lines of the I^2C module can be either configured to connect to ISO_1 and ISO_0 pad or to GPIO0.3 and GPIO0.2 pads.

Notes:

1. *The I^2C over ISO configuration is compliant with the I^2C- bus specification but cannot support the clock stretching feature.*
2. *The I^2C over GPIO configuration is compliant with the I^2C-bus specification up to Vcc < 3.6 V. This configuration supports clock stretching.*

Table 19 I2C interface characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Input low-level	V_{IL}	- 0.3[14]	–	0.2 V_{CC}	V	ISO Pads
		- 0.3	–	0.3 V_{CC}	V	GPIO Pads
Input high level	V_{IH}	0.7 V_{CC}	–	V_{CC} + 0.3	V	
Hysteresis of input stage	V_{hys}	0.05	–	–	V	
Output low-level	V_{OL}	0	–	0.4	V	1 mA; V_{CC} > 2 V
		0	–	0.3	V	1 mA; $V_{CC} \leq$ 2 V
Output fall time from V_{IHmin} to V_{ILmax}	t_{OF}[15]	23	–	120	ns	ISO Pad @ Cb = 30 pF
		–	–	250	ns	ISO Pad @ Cb = 100 pF
		0.3	–	–	ns	GPIO Pad @ Cb = 10 pF
Spikes suppressed by input filter	t_{SP}	–	–	–	ns	ISO Pad - no input filter available
		5	–	20	ns	GPIO Pad
SCL clock frequency	f_{SCL}	0	–	400	kHz	
Input current	I_i[16]	- 10	–	10	µA	Pull up/down disabled
Pad input capacitance	C_i	–	–	2	pF	ISO CLK Pad
		–	–	5	pF	ISO I/O Pad
		–	–	5	pF	GPIO Pad
External bus pull up on SDA	R_p	1.2[17]	–	–	kΩ	ISO Pads
SDA data hold time	$t_{HD;DAT}$	0[18]	–	–	ns	
SDA data setup time	$t_{SU;DAT}$	100	–	–	ns	Standard mode requires min. 250 ns.
Fall time of SCL signal	t_f	–	–	25	ns	Standard requires max. 300 ns.
Bus capacitance on SDA and SCLK	C_b[19]	30	–	100	pF	ISO Pads

14 This parameter is not conform with the requirements in the I^2C-bus specification.
15 ISO and GPIO pad output stages do not have an output slope control which is necessary for full compliant I^2C pads.
16 At I^2C bus specification levels the ESD protection circuit could cause an input leakage higher than I_i.
17 Restriction to achieve SDA output low-levels V_{OL} on ISO pads.
18 The I^2C bus system must guard this hold time (with respect to the V_{IH}(min.) of the SCL signal) all over the bus.
19 Restriction to fulfill the I^2C-bus specification output fall time requirement on ISO pads. On GPIO pads the output fall time specified in I^2C bus specification can not be achieved.

4.3.3 USB interface characteristics

The USB interface supports transmit and receive mode for Standard USB (STD USB) and Interchip USB (IC USB) for the 1.8 V and 3.0 V voltage classes. The USB interface is compliant to the Universal Serial Bus Specification Revision 2.0 ***[14]*** and Inter-Chip USB Supplement to the USB 2.0 Specification ***[15]*** except for deviations explicitly stated below. Terminals should provide a maximum current of at least 64 *mA* measured with a capacitor in the range of 50 to 200 *nF* connected between Vcc and GND close to the contacting elements.

Table 20 USB electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Supply voltage	V_{DDP}	3.00	–	3.60	V	STD USB
		1.65	1.80	1.95	V	IC USB 1.8 V
		2.70	3.00	3.60	V	IC USB 3.0 V
	V_{DDPext}	3.60	–	5.50	V	STD USB Restricted[20]
Output high voltage	V_{OH}	2.8	–	3.6	V	STD USB (R_L = 14.25 kΩ to GND)
		V_{DD} - 0.45	–	–	V	IC USB (I_{OH} = - 2 mA)
Output low voltage	V_{OL}	0	–	0.3	V	STD USB (R_L = 14.25 kΩ to 3.6 V)
		–	–	0.45	V	IC USB (I_{OL} = 2 mA)
Signal crossover voltage	V_{CRS}	1.3	–	2.0	V	
Input high voltage	V_{IH}	2.0	–	–	V	STD USB
		0.65*V_{DD}	–	V_{DD} + 0.3	V	IC USB 1.8 V (V_{OH} >= V_{OH}min.)
		2.0	–	V_{DD} + 0.3	V	IC USB 3.0 V (V_{OH} >= V_{OH}min.)
Input low voltage	V_{IL}	- 0.3	–	0.8	V	STD USB
		- 0.3	–	0.35*V_{DD}	V	IC USB 1.8 V
		- 0.3	–	0.8	V	IC USB 3.0 V
Differential Input Sensitivity	V_{DI}	0.2	–	–	V	|(D+) - (D-)|
Common Mode Range	V_{CM}	0.8	–	2.5	V	STD USB
Load Capacitance[21]	C_{LOAD}	–	–	50	pF	STD USB Capacitance on D+ / D-
		–	–	18	pF	IC USB Capacitance on D+ / D-
Input capacitive load	C_{INPUT}	–	–	9.5	pF	
Input impedance	Z_{IN}	300	–	–	kΩ	STD USB[22]

20 In the voltage range above 3.6 V the current and timing requirement targets may not be achieved.

21 Maximum difference between capacitance on D+ and D- allowed is 10%. For Interchip USB the load mismatch (C_{LOAD} D+ - C_{LOAD} D-) must be in between -2 pF and +2 pf at the package terminal.

22 The output impedance should be in this range for Standard USB. This impedance range includes all parasitic of the wiring, bonding and package.

4.3.4 SPI / GPIO interface

In *Table 21* the electrical characteristics of the SPI / GPIO are given.

Table 21 SPI electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
DC characteristics						
SPI / GPIO supply	VDDP[23)]	1.62	–	3.6	V	
Input leakage current	I_{LI}	- 4	–	4	µA	Pull-up off Output stage off - 0.3 < V_{PAD} < VDDP+ 0.3 V T = 25°C
		- 15	–	15	µA	Pull-up off Output stage off - 0.3 < V_{PAD} < VDDP+ 0.3 V T_J = - 40 – 125°C
Pull up impedance	R_{PU}	8.5	–	13.5	kΩ	Internal pull-up resistor
Input Low Voltage	V_{IL}	- 0.3	–	0.3*VDDP	V	
Input High Voltage	V_{IH}	0.7*VDDP	–	VDDP+0.3	V	
Low-level input current per group of GPIO pads	I_{IL_SUM}	–	–	4	mA	Group assignment: GPIO0.(0, 1, 2, 3)
Output low voltage	V_{OL}	–	–	0.3	V	I_{OL} = 1 mA, SRx=0 (fast mode)
		–	–	0.3	V	I_{OL} = 0.5 mA, SRx=1 (slow mode)
		–	–	0.1	V	I_{OL} = 50 µA, SRx=0 (fast mode)
Output high voltage	V_{OH}	VDDP - 0.3	–	–	V	I_{OH} = - 1 mA, SRx=0 (fast mode)
		VDDP - 0.3	–	–	V	I_{OH} = - 0.5 mA, SRx=1 (slow mode)
High-level output current per group of GPIO pads	I_{OH_SUM}	–	–	4	mA	Group assignment: GPIO0.(0, 1, 2, 3)
Input pad capacitance	C_{IN}	–	–	5	pF	
AC characteristics						
SPI clock rate	f_{SPI}	–	–	50	MHz	SPI slave, 50/50 duty cycle
				22	MHz	SPI master, $f_{OSC}/2$
Pad output signal rise / fall time	t_R, t_F	0.3	–	2.5	ns	0.3*VDDP to 0.7*VDDP, fast mode C_{LOAD} = 10 pF
		0.6	–	5.3	ns	0.3*VDDP to 0.7*VDDP, slow mode C_{LOAD} = 10 pF
Pad input low pass filter	f_{cutoff}[24)]	50	100	200	MHz	50/50 duty cycle
	t_{cutoff}	2.5	5	10	ns	high or low pulse width

23 These pads will operate with higher supply voltages, but switching levels and the SPI timing requirements may not be achieved.

24 Spikes faster than max. are filtered, spikes slower than min. are not filtered.

4.3.5 SWP interface characteristics

The AC and DC electrical characteristics of the SWP interface are compliant with ETSI TS 102 613 *[16]* (UICC related characteristics).

4.3.5.1 SWP characteristics

Table 22 SWP operation supply voltage

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Class B full power mode	$V_{CC\_SWP\_B}$	2.7	–	3.3	V	
Class C full power mode and low power mode	$V_{CC\_SWP\_C}$	1.62	–	1.98	V	

Table 23 SWP electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
DC characteristics[25]						
Input voltage high-level	V_{IH}	1.13	–	2.28	V	Class B; @ $I_{Lmin} \le I \le I_{Hmax}$
		0.7 * $V_{CC\_SWP\_C}$	–	$V_{CC\_SWP\_C}$ + 0.3	V	Class C; @ $I_{Lmin} \le I \le I_{Hmax}$
Input voltage low-level	V_{IL}	−0.3	–	0.48	V	Class B; @ $I_{Lmin} \le I \le I_{Hmax}$
		−0.3	–	0.25 * $V_{CC\_SWP\_C}$	V	Class C; @ $I_{Lmin} \le I \le I_{Hmax}$
Output current high-level	I_H	600	–	1000	µA	Class B, C; @ V_{IH}; pull-down resistor disabled
Output current low-level	I_L		–	20	µA	Class B, C; @ V_{IH}; pull-down resistor disabled
Input pull-down resistor	R_{PD}	200	–	340	kΩ	
AC characteristics						
Bit duration	T	590	–	10000	ns	
Logical 1 time	T_{H-1}	70	–	80	% of T	Measured from 50% of rising edge to 50% of next falling edge of signal amplitude
Logical 0 time	T_{H-0}	20	–	30	% of T	Measured from 50% of rising edge to 50% of next falling edge of signal amplitude
Input fall time	t_F	5	–	0.05 * T	ns	@ T < 5 µs, measured from 90% to 10% of signal amplitude

25 The SWP signal from the master must remain between −0.3 V and V_{CC} + 0.3 V during dynamic operation.

Table 23 SWP electrical characteristics (continued)

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
		–	–	250	ns	@ T ≥ 5 µs, measured from 90% to 10% of signal amplitude
Input rise time	t_R	5	–	0.05 * T	ns	@ T < 5 µs, measured from 10% to 90% of signal amplitude
		–	–	250	ns	@ T ≥ 5µs, measured from 10% to 90% of signal amplitude
Input capacitance[26)]	C_{IN}	–	–	10	pF	

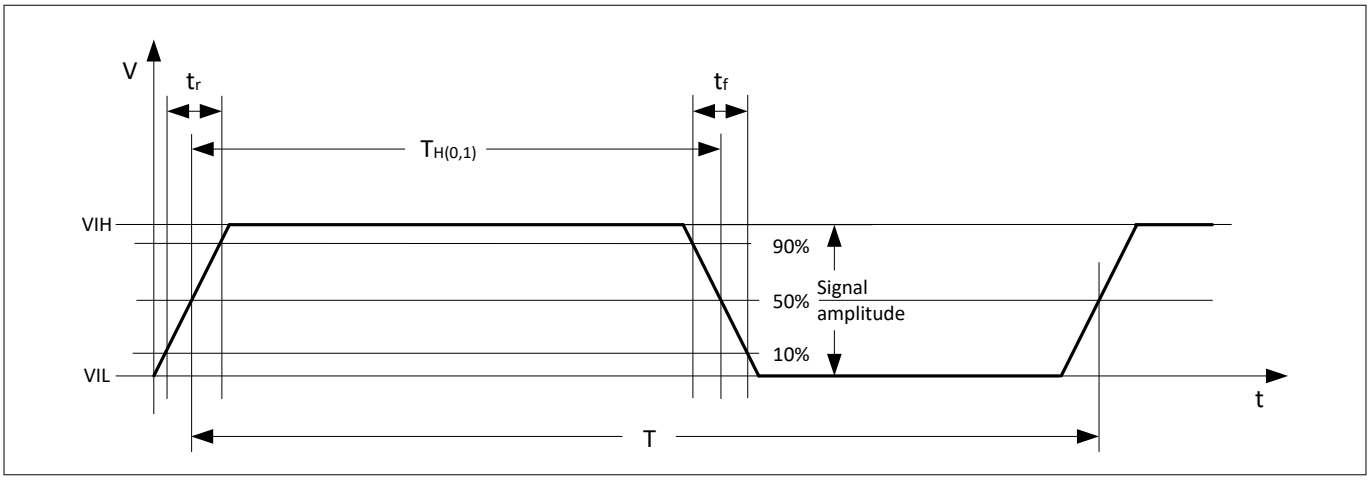

Figure 31 Input voltage signal timing relations

26 Bare die + typical package, e.g. chipcard module. Package details are available on request.

5 RoHS compliance

On January 27, 2003 the European Parliament and the council adopted the directives:

- 2002/95/EC on the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment ("RoHS")
- 2002/96/EC on Waste Electrical and Electrical and Electronic Equipment ("WEEE")

Some of these restricted (lead) or recycling-relevant (brominated flame retardants) substances are currently found in the terminations (e.g. lead finish, bumps, balls) and substrate materials or mold compounds.

The European Union has finalized the Directives. It is the member states' task to convert these Directives into national laws. Most national laws are available, some member states have extended timelines for implementation. The laws arising from these Directives have come into force in 2006 or 2007.

The electro and electronic industry has to eliminate lead and other hazardous materials from their products. In addition, discussions are on-going with regard to the separate recycling of certain materials, e.g. plastic containing brominated flame retardants.

Infineon is fully committed to giving its customers maximum support in their efforts to convert to lead-free and halogen-free[27)] products. For this reason, Infineon's "Green Products" are ROHS-compliant.

Since all hazardous substances have been removed, Infineon calls its lead-free and halogen-free semiconductor packages "green." Details on Infineon's definition and upper limits for the restricted materials can be found here.

The assembly process of our high-technology semiconductor chips is an integral part of our quality strategy. Accordingly, we will accurately evaluate and test alternative materials in order to replace lead and halogen so that we end up with the same or higher quality standards for our products.

The use of lead-free solders for board assembly results in higher process temperatures and increased requirements for the heat resistivity of semiconductor packages. This issue is addressed by Infineon by a new classification of the Moisture Sensitivity Level (MSL). In a first step the existing products have been classified according to the new requirements.

27 Any material used by Infineon is PBB and PBDE-free. Plastic containing brominated flame retardants, as mentioned in the WEEE directive, will be replaced if technically/economically beneficial.

A Use-case specific schematics

The following sections show examples of the different connectivity options of the SLx97 controller. These examples are shown for specific packages, please see the pad-to-signal reference tables in the ***Description of delivery forms*** chapter for the pins that apply to other packages.

Example: I2C

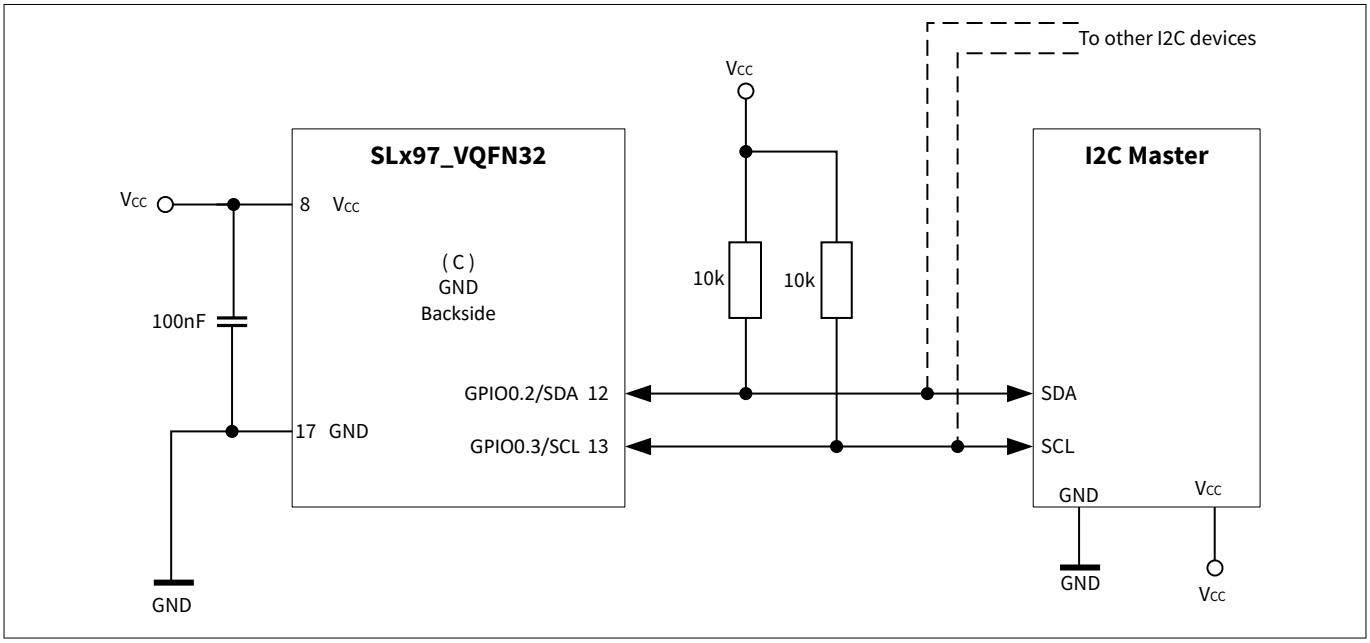

Figure 32 Connecting the security controller with I2C (PG-VQFN-32 package)

Example: SPI

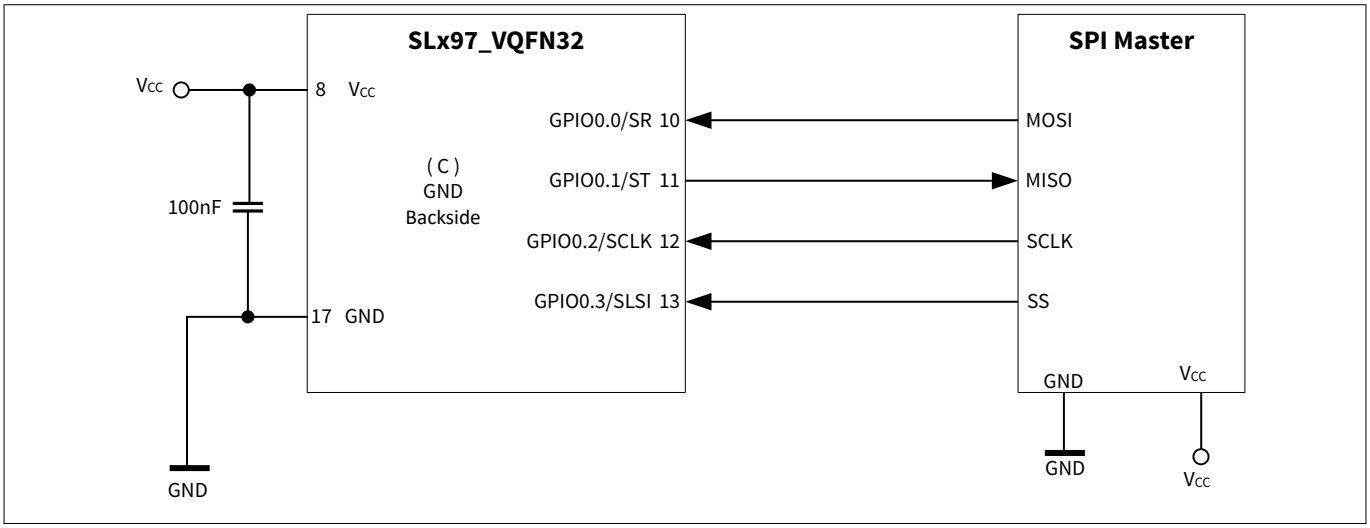

Figure 33 Connecting the security controller with SPI (PG-VQFN-32 package)

A Use-case specific schematics

Example: ISO/IEC 7816, SPI and SWP

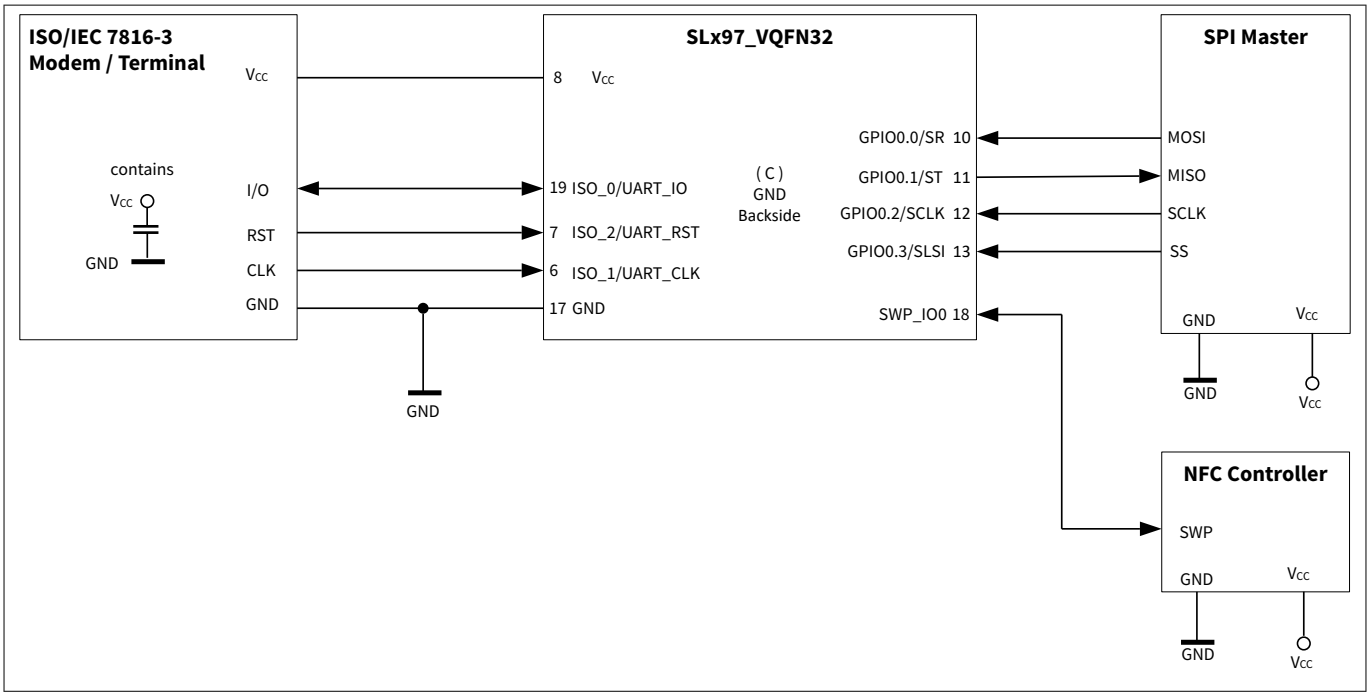

Figure 34 Connecting the security controller with ISO/IEC 7816, SPI and SWP (PG-VQFN-32 package)

Example: ISO/IEC 7816, I2C and SWP

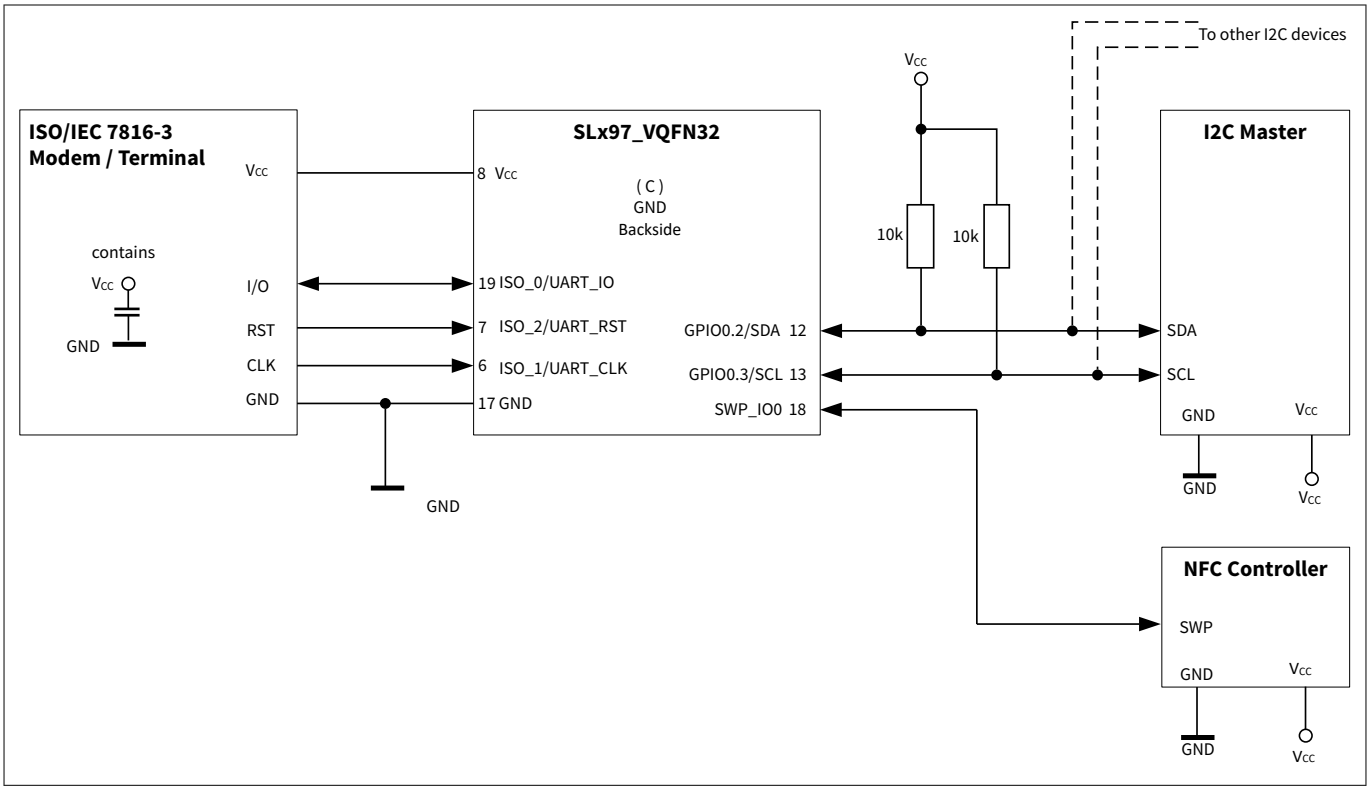

Figure 35 Connecting the security controller with ISO/IEC 7816, I2C and SWP (PG-VQFN-32 package)

A Use-case specific schematics

Example: ISO/IEC 7816 and SWP

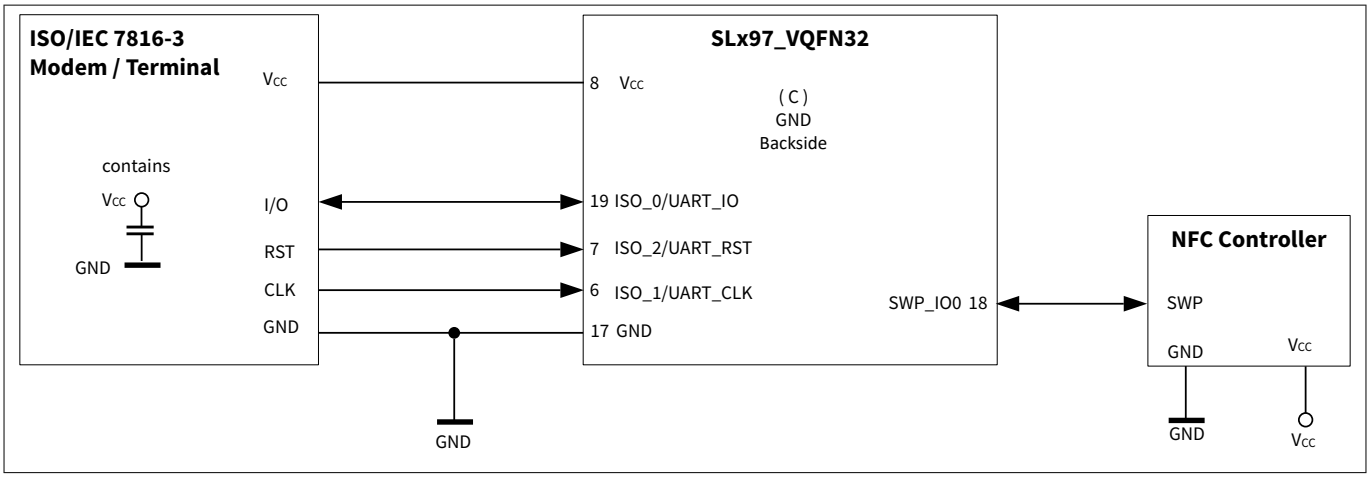

Figure 36 Connecting the security controller with ISO/IEC 7816 and SWP (PG-VQFN-32 package)

References

The following documents set out or describe specifications and/or standards referenced in the text of this document.

Payment-related standards

[1] EMVCo: EMV Integrated Circuit Card Specifications for Payment Systems; Book 1: Application Independent ICC to Terminal Interface Requirements, Version 4.3, November 2011

[2] EMVCo: EMV Integrated Circuit Card Specifications for Payment Systems; Book 2: Security and Key Management, Version 4.3, November 2011

[3] EMVCo: EMV Integrated Circuit Card Specifications for Payment Systems; Book 3: Application Specification, Version 4.3, November 2011

Contact-based smart cards

[4] ISO/IEC 7816: Information Technology – Identification Cards – Integrated Circuit(s) Cards with Contacts Part 1: Physical Characteristics (1998-10-15) Amendment 1 - Maximum height of the IC contact surface (2003-11-15)

[5] ISO/IEC 7816: Information Technology – Identification Cards – Integrated Circuit(s) Cards with Contacts Part 2: Dimension and location of the contacts, Second edition (2007-10-15)

[6] ISO/IEC 7816: Information Technology – Identification Cards – Integrated Circuit(s) Cards with Contacts Part 3: Electrical interface and transmission protocols, Third edition (2006-11-01)

[7] ISO/IEC 7816: Information Technology – Identification Cards – Integrated Circuit(s) Cards with Contacts Part 4: Organization, security and commands for interchange, Second edition (2005-01-15)

[8] ETSI TS 102 221 – Smart cards; UICC-Terminal interface; Physical and logical characteristics - (Release 11)

[9] ETSI TS 100 977, V8.13.0 (2005-06) Digital cellular telecommunications system (Phase 2+); Specification of the Subscriber Identity Module - Mobile Equipment (SIM-ME) Interface (GSM – 3GPP TS 11.11 version 8.13.0 Release 1999)

[10] ETSI TS 300 641, March 1998, Third Edition Digital cellular telecommunications system (Phase 2); Specification of the 3 Volt Subscriber Identity Module - Mobile Equipment (SIM-ME) interface (GSM 11.12 version 4.3.1)

[11] ETSI TS 101 116, V7.0.1 (1999-07) Digital cellular telecommunications system (Phase 2+); Specification of the 1.8 Volt Subscriber Identity Module - Mobile Equipment (SIM - ME) interface (GSM 11.18 version 7.0.1 Release 1998)

Inter-integrated circuit

[12] I^2C-bus specification and user manual, Rev. 6 – 4 April 2014

[13] IFX I2C Protocol Specification 1.50, Infineon Technologies AG, 2015-01-19

USB interface

[14] USB 2.0 Specification, April 2000

[15] Inter-Chip USB Supplement to USB 2.0

SWP interface

[16] ETSI TS 102 613 - Smart Cards; UICC - Contactless Front-end (CLF) Interface; Part 1: Physical and data link layer characteristics (Release 11)

Revision history

Reference	Description
Revision 1.3, 2019-09-18	
	First edition

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Edition 2019-09-18

Published by

Infineon Technologies AG

81726 Munich, Germany

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Email:
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Document reference
IFX-csb1548773856094

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