

MA12040/P and MA12070/P

Errata Sheet

About this document

Scope and purpose

Documentation of errata items for the MA12040/P and MA12070/P.

Intended audience

Designers and FAEs working with the MA12040/P and MA12070/P.

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1 Issue or limitation of operation or performance

1.1 Reverse output polarity on BTL and PBTL modes

Applicable for device version:

- MA12040P
- MA12070P

Silicon version:

All

Customer identification:

All

Description of the issue/limitation:

Reversed output polarity can be observed on both output Channel A and Channel B on BTL and PBTL output configurations compared to its input polarity.

The MA12040P in BTL and PBTL configurations produces positive signal on output Channel B and negative output signal on Channel A as opposed to the expected positive signal on output Channel A and negative output signal on Channel B.

Affected output channels in which the reversed polarity can be observed are on OUT0A, OUT0B, OUT1A and OUT1B in BTL and PBTL configurations.

Application information:

Application examples where this bug becomes an issue include:

- 2.1 Configuration of one MA12040P device. The BTL configured channel will have reversed polarity compared to the two SE configured channels. This leads to out of phase problems with audio playback.
- MA12040P BTL or PBTL configured channels used in combination with a MA12040 (analog input) or a third-party amplifier in one system. This can for example happen when MA12040P is used to drive two mid-range or tweeter speakers in BTL and one MA12040 (analog input) or a third part amplifier is used to drive a subwoofer. The two mid-range or speakers will have reversed polarity compared to the subwoofer. This leads to out of phase problems with audio playback.

Workaround:

Reverse the output polarity of a BTL or PBTL configured channel.

1.2 /CLIP Pin always active in PBTL configuration

Applicable for device version:

- MA12040 and MA12040P
- MA12070 and MA12070P

Silicon version:

All

Customer identification:

All

Description of the issue/limitation:

The /CLIP Pin that indicates the clipping level of the device is always active (pulled low) in PBTL configuration.

Workaround:

Alternatively, the monitor registers for Channel 0 and Channel 1 can be polled for modulation index. The modulation index will give a measure of how close the output signal is to clipping.

1.3 PVDD hot plugging

Applicable for device version:

- MA12040 and MA12040P

Silicon version:

All

Customer identification:

All

Description of the issue/limitation:

Hot plugging the PVDD pins can cause damage to the amplifier. Hot plugging can trigger the ESD-cells that are designed for ESD (Electro static discharge) and not the power/energy level of a fast voltage ramp up from power supply.

Workaround:

Make sure that the ramp up voltage stays below $0.25\text{V}/\mu\text{s}$. This can be controlled by using the soft start function of the power supply or by using a load switch with a controlled ramp up voltage.

1.4 Limiter false active

Applicable for device version:

- MA12070P

Silicon version:

All

Customer identification:

All

Description of the issue/limitation:

The Limiter is false active for a short period when the input signal is close to silence and the total gain of the channel is equal to -64.25 dBFS or below. The cycle time of this event is linked to the attack and release time of the limiter.

Workaround:

Do not turn on the limiter when the total gain is -64.25 dBFS or below.

1.5 Device failure due to in-rush current

Applicable for device version:

- MA12040 and MA12040P
- MA12070 and MA12070P

Silicon version:

All

Customer identification:

All

Description of the issue/limitation:

It is known that large output in-rush current cannot be handled well by the substrate of the IC. This might result in device breakdown. Large in-rush currents can occur when for example a double / simultaneous short is created at the output in combination with long (> 1m) speaker cables.

Workaround:

If this is a likely scenario for the application, it is recommended to apply a schottky diode at each output node. This way large in-rush currents are diverted to PCB ground instead of IC substrate.



Revision history

Document version	Date of release	Description of changes
V 1.0	July 2018	Initial release

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