Input capacitor (DCLINK) calculation

For single phase motor bridge

About this document

Scope and purpose

This application note provides information how to calculate and dimension the input capacitor (DCLINK capacitor) for single phase motor bridge to drive brushed DC motors.

Intended audience

Hardware engineers who develop single phase motor drivers.

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1 Single phase half-bridge to drive a brushed DC motor

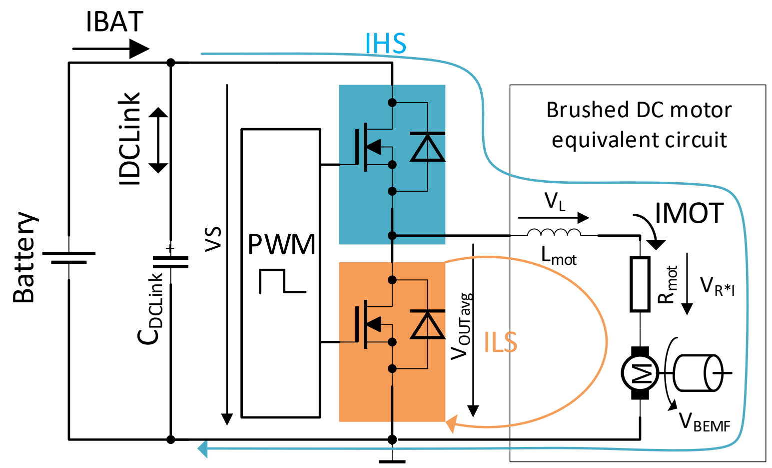

Figure 1 Half-bridge with high-side and low-side switches driving a brushed DC motor in PWM mode

The input capacitor, also known as DCLINK capacitor, stabilizes the supply voltage and provides instantaneous current to the PWM operated half-bridge.

Figure 1 shows a half bridge driving a brushed DC motor in PWM mode operation. During the on phase of the high-side switch (blue), current flows from the battery and out of the input capacitor (DCLINK capacitor) into the motor to spin it.

During the off phase, the low-side switch (orange) is active and provides a freewheeling path for the motor current stored in the motor inductance.

2 Assumptions for the analysis and calculations

For the analysis and calculations provided in this document, following assumptions are made:

- The motor inductance is large enough to ensure that the motor current IMOT is continuous
- The PWM frequency is high enough to ensure that the motor current IMOT is continuous
- The battery current IBAT is a constant current with no AC components. All the AC current flowing into the power stage during PWM operation is provided by the DCLINK capacitor
- Equivalent series inductance (ESL) of the DC link capacitor is neglected

3 Waveform analysis of PWM operated half-bridge

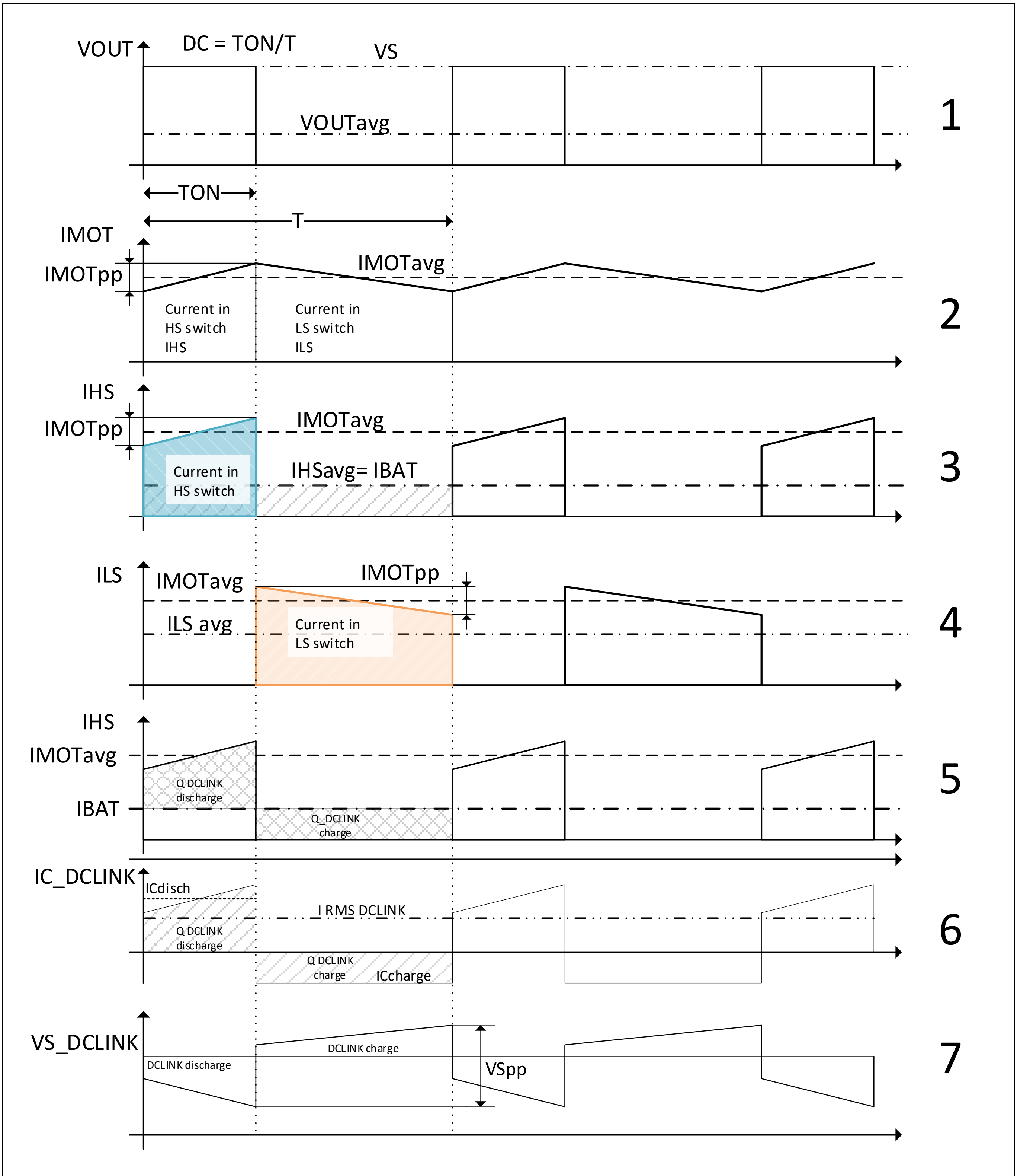

Figure 2 Idealized waveform analysis of a PWM operated motor half bridge

Waveform 1:
Output voltage VOUT, PWM operated with duty cycle DC

- The duty cycle DC is defined as:

$$DC = \frac{TON}{T}$$

Equation 1

- The average output voltage generated by the PWM'ed supply voltage VS (which is the battery voltage) is defined as:

$$VOUTavg = DC \times VS$$

Equation 2

Waveform 2:
Motor current IMOT with average motor current IMOTavg and peak to peak ripple current IMOTpp

- The motor current IMOT consists of the current through the high-side and low-side switches

$$IMOT = IHS + ILS$$

Equation 3

Note: During the start-up of the DC motor, the motor current can be multiple times higher than the current under normal load condition, when the motor is spinning. The same applies when the motor is blocked.

- The peak to peak motor ripple current IMOTpp is considered in this analysis as constant and should be measured for verification. IMOTpp depends on the motor operating condition, for example:
  - The motor does not turn during start-up or stall condition where no V_{BEMF} is generated
  - Mechanical load is applied causing a voltage drop over the winding resistance of the motor

Waveform 3:
Current in high-side switch IHS with high-side average current IHSavg and average motor current IMOTavg

The blue area shows the current through the high-side switch IHS during TON. This area reflects the charge IMOTavg*TON. This charge must be provided in the end by the battery. The average current through the high-side switch IHSavg over the period T is the constant average current provided by the battery (power supply) IBAT. The hatched area shows the charge provided by the battery IBAT (=IHSavg) * T (period). Both areas need to be equal and therefore:

$$IBAT \times T = IMOTavg * TON = IMOTavg * DC * T$$

Equation 4

The battery current IBAT and the average current through the high-side switch IHSavg can be calculated by:

$$IHSavg = IBAT = \mathrm{DC} \times IMOT\mathrm{avg}$$

Equation 5

Waveform 4:
Current in low-side switch ILS with low-side average current ILSavg and IMOTavg

The orange area shows the current through the low-side switch ILS. This is the freewheeling path for the motor current.

Waveform 5 + 6:
Current in high-side switch with discharge (Q DCLINK discharge) and charge (Q DCLINK charge) of DCLINK capacitor, discharge current of DCLINK capacitor ICdisch, RMS current through the DCLINK capacitor I RMS DCLINK

During the on phase of the high-side switch TON, the current through the high-side switch consists of two components:

- The constant battery current IBAT
- The discharge current of the DCLINK capacitor ICdisch

During the off phase of the high-side switch, the DCLINK capacitor is recharged by the battery current IBAT.

The DCLINK capacitor's discharge current can be calculated by:

$$ICdisch = IMOTavg - IBAT = IMOTavg \times (1 - DC)$$

Equation 6

In steady state condition, the DCLINK capacitor's charge and discharge during one period must be equal and therefore:

$$Qdischarge = Qcharge$$

Equation 7

The DCLINK's discharge during TON can be calculated by:

$$Qdischarge = (ICdisch) \times TON$$

Equation 8

Using Equation 1 and Equation 6 results in:

$$Qdischarge = IMOTavg \times (1 - DC) \times DC \times T$$

Equation 9

The charge and discharge of the DCLINK capacitor results in an RMS current IRMSDCLINK. The calculation is explained in Chapter 7.

Waveform7:
Idealized supply voltage ripple VSpp at DCLINK capacitor

The charge and discharge of the DCLINK capacitor leads to a voltage ripple at the supply voltage VS_DCLINK. The calculation of the voltage ripple VSpp is handled in Chapter 4.

4 Calculation of the DCLINK voltage ripple VSpp

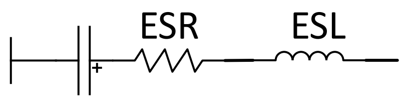

Figure 3 Equivalent circuit diagram of an (aluminum) electrolyte capacitor

ESR: equivalent series resistance

ESL: equivalent series inductance

Note: The calculation of VSpp does not consider the ESL. The impact of the ESL on VSpp is compensated by an additional ceramic capacitor, see Chapter 6.

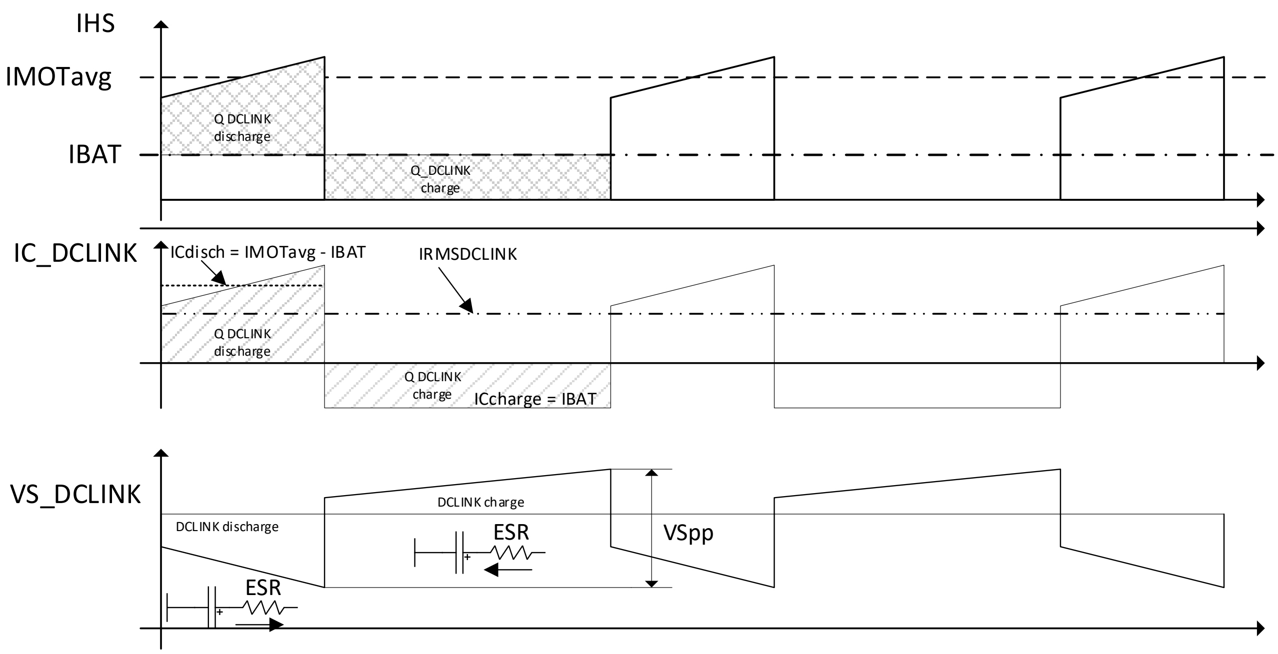

Figure 4 Idealized waveforms for supply voltage ripple VSpp calculation

Figure 4 shows the idealized waveforms for the supply voltage ripple VSpp caused by discharging and charging the DCLINK capacitor. Equation 10 calculates the supply voltage ripple VSpp. It includes three components:

- Voltage ripple caused by discharging and charging the capacitance of the DCLINK capacitor over one period
- Voltage step caused by the ESR of the capacitor and the discharge current
- Voltage step caused by the ESR of the capacitor and the charge current

Figure 5 shows a scope plot with real waveforms of VSpp, IMOT, VOUT, and IBAT. For the measurement, the setup in Figure 6 was used.

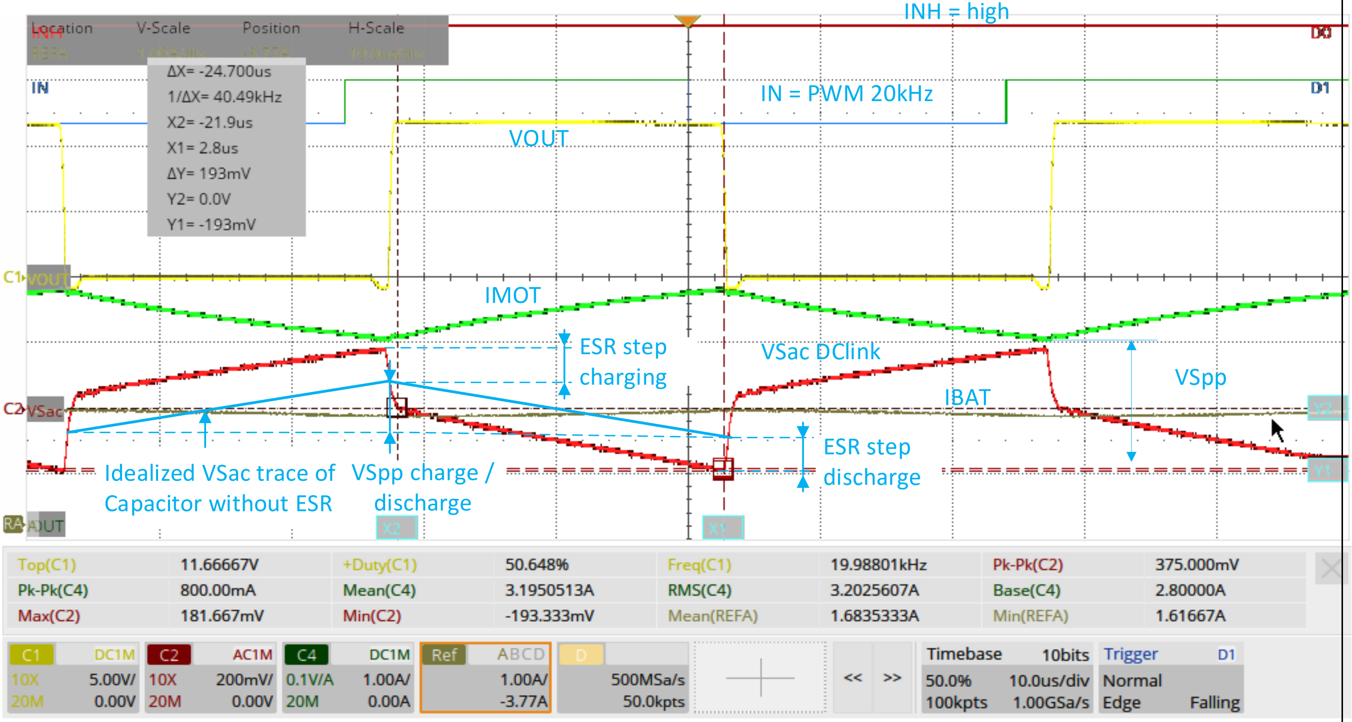

Figure 5 Scope plot of VSpp, VOUT, IMOT, VSpp, IBAT

$$\mathrm{VSpp} = \overbrace{(\mathrm{ICdisch} + 0{,}5 \times IMOTpp) \times ESR}^{\text{ESR step by discharge current}} + \overbrace{\frac{Qdischarge}{CDCLINK}}^{\text{dVS by charge / discharge of capacitance}} + \overbrace{IBAT * ESR}^{\text{ESR step by charge current}}$$

$$\mathrm{VSpp} = (IMOTavg \times (1 - DC) + 0{,}5 \times IMOTpp) \times ESR + \frac{Qdischarge}{CDCLINK} + (\mathrm{DC} \times IMOT\mathrm{avg} * ESR)$$

$$\mathrm{VSpp} = (IMOTavg + 0{,}5 \times IMOTpp) \times ESR + \frac{Qdischarge}{CDCLINK}$$

$$\mathrm{VSpp} = (IMOTavg + 0{,}5 \times IMOTpp) \times ESR + \frac{IMOTavg \times (1 - DC) \times DC \times T}{CDCLINK}$$

with: $T = \frac{1}{fPWM}$

$$\mathrm{VSpp} = (IMOTavg + 0{,}5 \times IMOTpp) \times ESR + \frac{IMOTavg \times (1 - DC) \times DC}{CDCLINK \times fPWM}$$

Equation 10: VSpp and its derivation

5 Calculating the DCLINK capacitor size

Solving Equation 10 for CDCLINK results in:

$$\mathrm{VSpp} = (IMOTavg + 0{,}5 \times IMOTpp) \times ESR + \frac{IMOTavg \times (1-DC) \times DC}{CDCLINK \times fPWM}$$

$$CDCLINK \times fPWM = \frac{IMOTavg \times (1-DC) \times DC}{\mathrm{VSpp} - (IMOTavg + 0{,}5 \times IMOTpp) \times ESR}$$

$$CDCLINK = \frac{1}{fPWM} \times \left(\frac{IMOTavg \times (1-DC) \times DC}{\mathrm{VSpp} - (IMOTavg + 0{,}5 \times IMOTpp) \times ESR}\right)$$

Equation 11 Calculation of DCLINK capacitance

Note: For an operating condition with given DC, IMOTavg, IMOTpp, ESR, and VSpp, the DCLINK capacitance increases with lower PWM frequency and decreases with higher PWM frequency.

Practical usage of Equation 11 to calculate an appropriate DCLINK capacitor size:

- VSpp voltage ripple ~ 1Vpp (or defined by application requirements)
- Duty cycle DC: max voltage ripple occurs @ ~ 70% - 80% DC, see also Figure 8
- IMOT/IMOTpp: to be measured or derived from motor specification
- ESR: to be derived from DCLINK capacitor datasheet

6 Compensate VSpp voltage spike with ceramic bulk capacitor

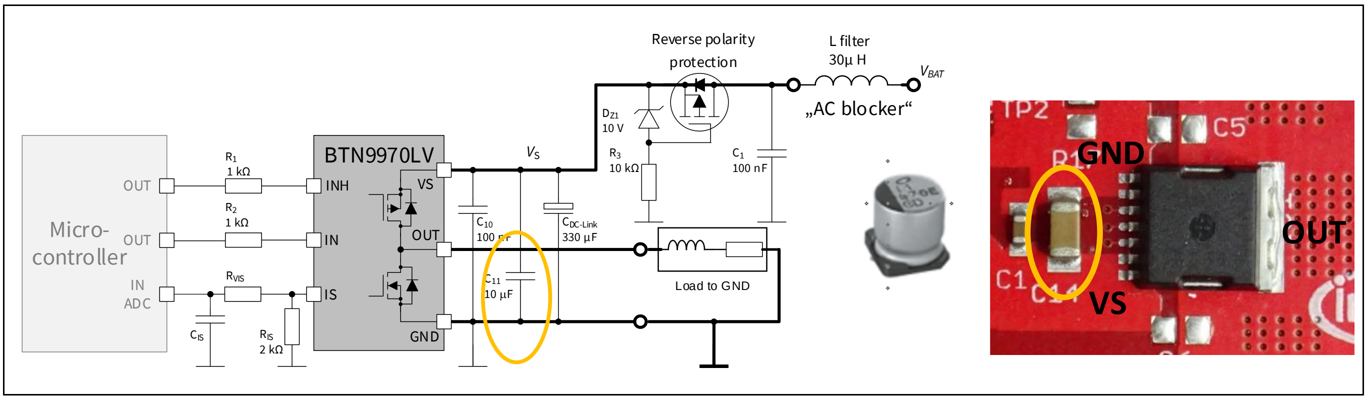

Figure 6 Measurement setup using BTN9970 high current half-bridge

Measurement setup, evaluation board DC-Shield_BTN9970LV:

- BTN9970 half-bridge
- Load circuitry: instead of a motor, a load of 250 µH inductance + 1,86 Ω was used
- CDCLINK: 330 µF SMD aluminum electrolyte capacitor with 65 mΩ ESR (measured)
- Lfilter: 33 µH inductor to block AC currents from battery
- C11: 10 µF X7R ceramic bulk capacitor
- C110: 100nF ceramic capacitor

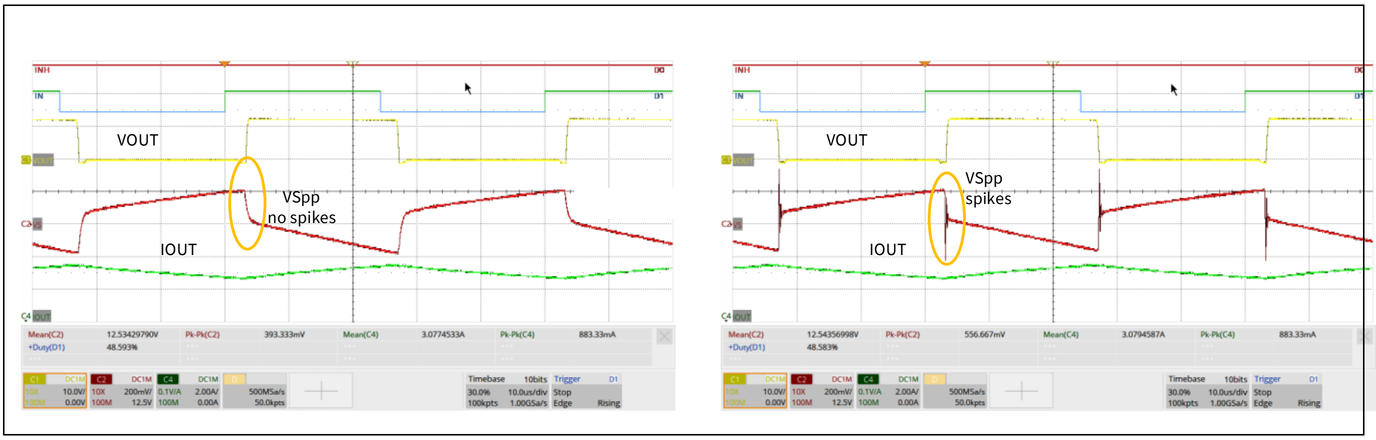

Figure 7 VSpp voltage ripple with (left) and without (right) ceramic bulk capacitor

The ceramic capacitor C11 is a low impedance current source during the switching event when the high-side switch turns on and takes over the motor current. The current through the switch rises immediately from 0 to the value of IMOTavg- 0.5 x IMOTpp, see Figure 2, waveform 3.

The capacitor C11 reduces the emission into the VS supply line.

7 Calculating the DCLINK RMS current

To select an appropriate DCLINK capacitor the RMS current through the capacitor needs to be estimated.

The RMS current is in general defined by:

$$IRMSDCLINK = \sqrt{\left(\frac{1}{T} \times \int_0^T IDCLINK(t)^2 \times dt\right)}$$

Equation 12

Solving the integral for piecewise liner waveforms results in:

$$IRMSDCLINK = \sqrt{\left(DC \times \left(IMOT\text{avg}^2 \times (1 - DC) + \frac{1}{12} \times IMOTpp^2\right)\right)}$$

Equation 13

8 Practical validation of VSpp / measurement versus calculation

The equations were validated in practice with the measurement setup in Figure 6.

A PWM frequency of 20 kHz was used. The duty cycle varied from 10% to 90%.

The ESR of 65 mΩ for the DCLINK capacitor was determined by measurement in the lab. The capacitance of 330 µF is specified in the datasheet.

Comments to the curve traces shown in Figure 8 :

- *IMOTavg measured*: In the used setup, the average motor current increases linearly with the duty cycle DC
- *IMOTpp measured*: The motor peak to peak ripple current reaches its maximum at 50% DC
- The course of the traces *VSPP calculated* and *VSPP measured* show a reasonably good match. Differences are most likely caused by measurement inaccuracy. The maximum peaks at ~ 70% to 80% DC
- The DCLINK RMS current *ICRMS calculated* has the peak around 70% to 80% DC.

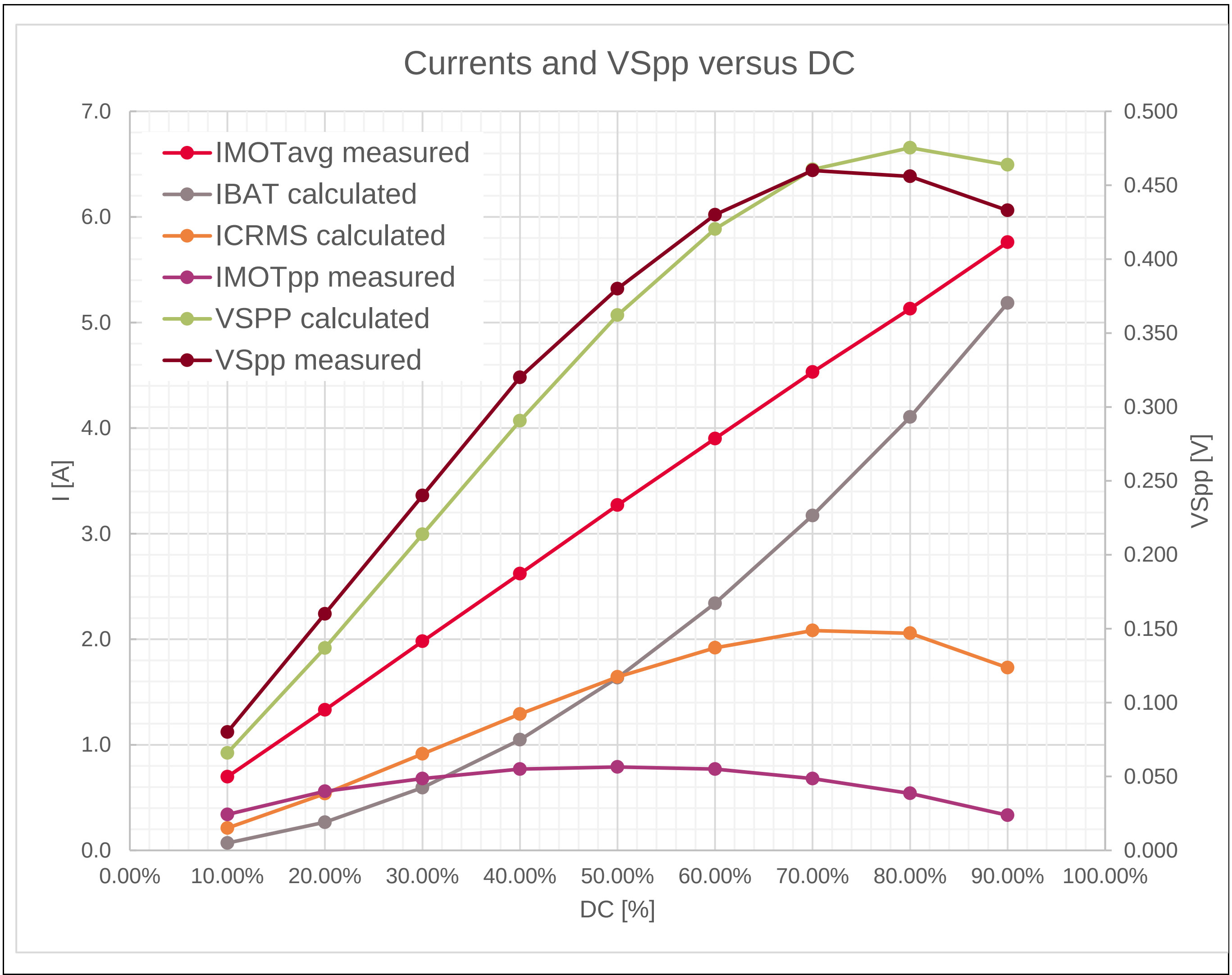

Figure 8 **Currents and VSpp supply voltage ripple versus duty cycle DC**

9 The impact of cold temperatures on DCLINK performance

When selecting a DCLINK capacitor, the ESR behavior versus temperature, in particular for cold temperatures, should be considered. In the example shown in Figure 9 the VSpp voltage almost doubles at cold temperatures from 450mVpp to 800mVpp due to the increase of ESR at cold temperature.

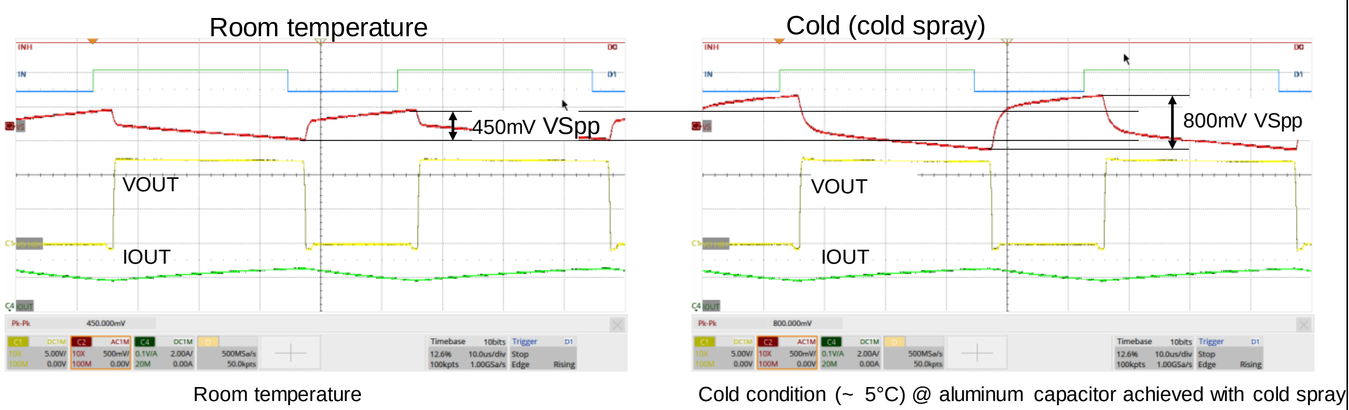

Figure 9 Impact of cold temperature to the DCLINK aluminum electrolyte capacitor

10 Other things worth to look at

In this document the steady state operating condition for a DC motor was considered.

In the real application other operating conditions need to be considered, such as:

- Inrush current during motor start-up and stall current condition, when the rotor is locked. This leads to much higher motor currents
- Operation of the motor bridge in overcurrent detection (for example, when the motor is defect or has a short to GND or VBAT)

References

[1] DC-Shield_BTN9970LV documentation: https://www.infineon.com/cms/en/product/evaluation-boards/dc-shield_btn9970lv/

Revision history

Document revision	Date	Description of changes
1.00	2023-08-01	Initial version

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