MOTIX™ TLE987x Verified Chipset application note

MOTIX™ TLE987x/OptiMOS™ IAUC100N04S6N022

About this document

Purpose

The purpose of this document is to provide a limited number of verified driver/MOSFET combinations with a best fit driver configuration that can be used to achieve good system performance.

Following the guidance provided in this report, you will see a proposal for the schematics in the B6 bridge of your motor control unit. For this schematics proposal, you can select one of four OptiMOS™ 6 MOSFETs, ranging from 1.0mΩ to 2.8mΩ, depending on your application needs. For each possible MOSFET selection, a dedicated gate driver configuration is provided, which was tested for a wide range of conditions.

For these specific combinations and configurations, you will then get detailed information on the switching characteristics.

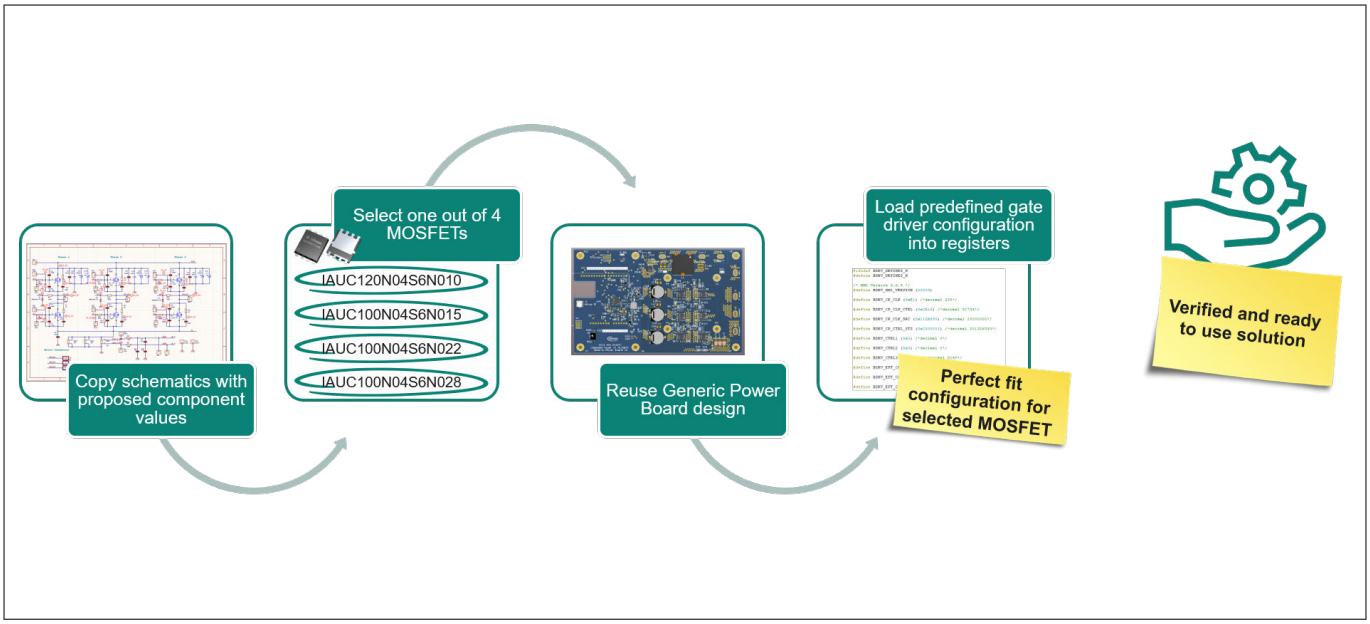

Figure 1 Getting ready to use your solution with few easy steps

Scope

This Verified Chipset application note gives information about the system behavior of the MOTIX™ MCU TLE987x gate driver and theOptiMOS™6 IAUC100N04S6N022 MOSFET. It gives information about the expected switching timings of the combined driver/MOSFET system. The information includes a wide range of conditions, including voltage-, load current- and temperature variations that are expected in automotive applications. Additionally, some information about the deviation between the selected driver and MOSFET lots will be provided.

In addition to the switching behavior, the effects of the behavior on EMC behavior and power dissipation are shown on a reference PCB. This information can give a first insight into how different settings and application conditions can change EMC and power dissipation.

Intended audience

Development engineers of low-voltage motor drive electronic control units.

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1 Motivation and collaterals

Motivation

Designing and configuring a motor control unit for automotive purposes can be a complex task. There is a huge range of MOSFETs and drivers available on the market that can be combined. Additionally, each driver must be configured specifically for the selected MOSFET and external components.

This means that there is an almost infinite number of combinations of drivers, MOSFETs, and configurations possible and each of these has its unique switching characteristics. Furthermore, these switching characteristics can vary between individual samples or operational conditions such as voltage, current, or temperature.

The objective of these switching characteristics is always to safely operate the motor within thermal and EMC boundary conditions, and this must be qualified together with the data available in datasheets and user manuals.

So finding and qualifying a good solution can be a difficult task. The task risks having to include multiple design steps to meet every objective, which delays the time to market.

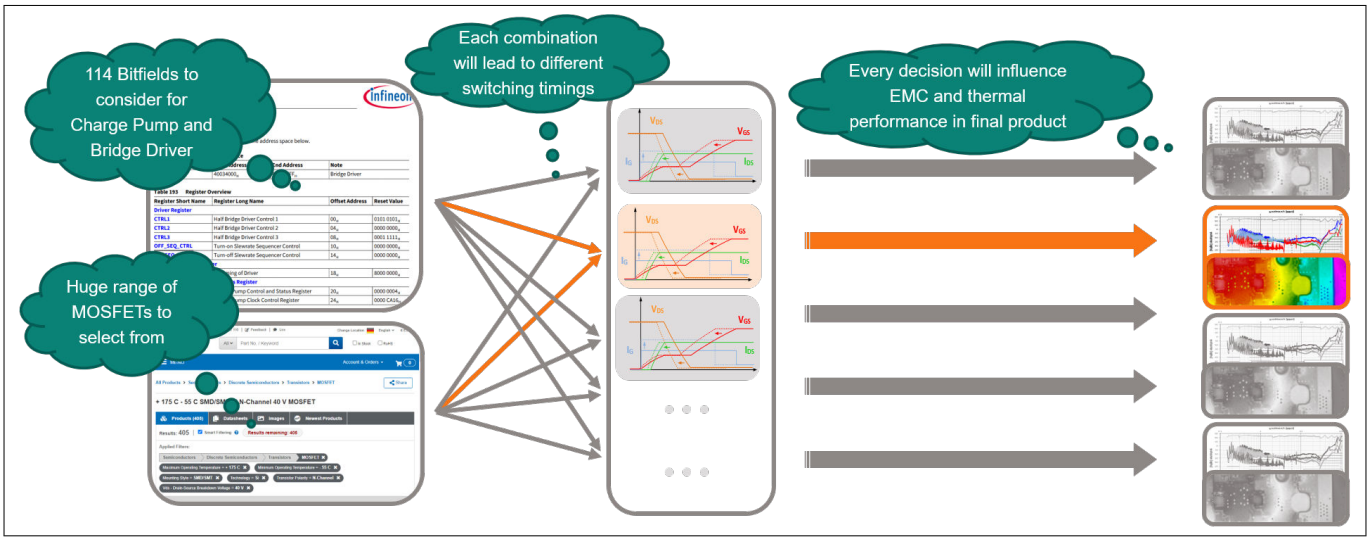

Figure 2 Going from product selection and configuration to switching characteristics to EMC performance and thermal performance

Purpose

The purpose of this document is to provide a limited number of verified driver/MOSFET combinations with a best fit driver configuration that can be used to achieve good system performance.

Following the guidance provided in this report, you will see a proposal for the schematics in the B6 bridge of your motor control unit. For this schematics proposal, you can select one of four OptiMOS™ 6 MOSFETs, ranging from 1.0mΩ to 2.8mΩ, depending on your application needs. For each possible MOSFET selection, a dedicated gate driver configuration is provided, which was tested for a wide range of conditions.

For these specific combinations and configurations, you will then get detailed information on the switching characteristics.

Collaterals to help you reach your goal

To provide the best overview possible on the system's behavior, various collaterals are available to you. These include:

- Report describing all characteristics for a specific driver/MOSFET combination
- EMC measurements to show the effects of various configurations (included in report)
- Thermal simulation to show the effect of power dissipation generated from various configurations (included in report)

1 Motivation and collaterals

- Reference PCB (called the Generic Power Board) available on the Infineon homepage to replicate the behavior described in the report
- FOC software example including configuration wizard to select a predefined gate driver configuration
- Simulation Program with Integrated Circuit Emphasis (SPICE) model of the system described in the report

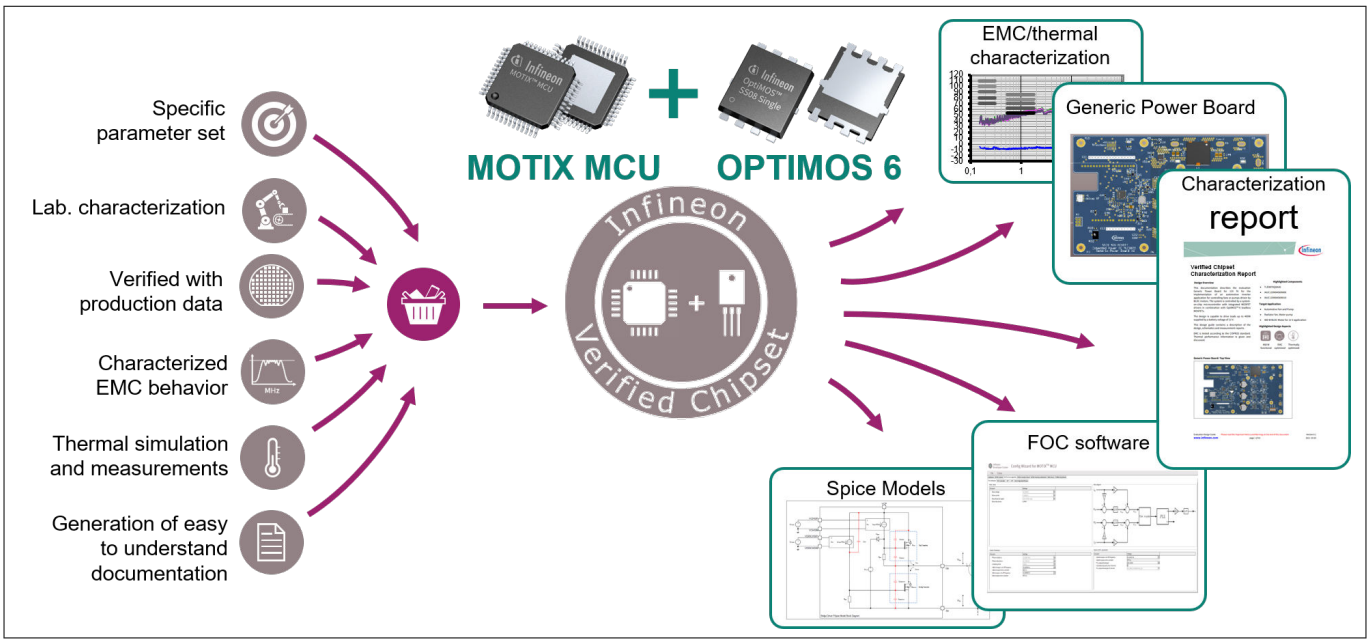

Figure 3 Collaterals

These collaterals will help you to better understand the characteristics you can expect from your own design.

2 Overview

This gate driver register configuration for TLE987x given in this document can be used to drive the Infineon IAUC100N04S6N022 MOSFET. This MOSFET can be selected from the list of OptiMOS ™6 MOSFETs below. There are separate application notes for each MOSFET.

- IAUC120N04S6N010
- IAUC100N04S6N015
- **IAUC100N04S6N022**
- IAUC100N04S6N028

There are three different gate driver register configurations given that are optimized as follows:

- Optimized for electromagnetic compatibility (EMC), (slow-switching)
- Optimized for power dissipation, (fast-switching)
- Sweet-spot, (medium-switching)

This application note refers to these configurations as slow, fast, and medium switching. When following the schematics guidance in Schematics, these configurations can be used and will result in a reasonable switching performance.

This application note consists of two parts. Configuration-dependent switching behavior describes switching characteristics that are determined by the characterization of multiple devices from different production lots. The example of the Generic Power Board shows how these characteristics influence the EMC and thermal behavior on an example PCB. The characteristics of part one are mainly influenced by the selection of components and the configuration of the driver and therefore are mostly independent from the PCB design. The presented results of part two are very PCB-specific and therefore only serve as an example and show how different driver configurations can change these characteristics. Description of characterized samples and boundary conditions describes how data was generated and where there are limits and boundary conditions.

In Configuration-dependent switching behavior the switching characteristics were generated for the following variation of conditions:

- Load current variation
- DC-Link voltage variation
- Temperature variation
- MOSFET front end lots: 30 devices from 2 front end lots from the years 2018 to 2022
- TLE987x gate driver front end Lots: 3 devices from 3 Front End lots and 2 production sites from years 2018 to 2022

The switching times were identified under these conditions and using these specified samples. The aim of providing the data is to present information about realistic switching behavior for different MOSFETs and driver samples, also taking into consideration the distribution across production . The switching times only consider these samples, and may not apply to other samples from past or to future lots.

Step-by-step guide on making use of the Verified Chipset

There are two approaches to working with this document.

- Approach 1: You do not yet have a PCB and want to identify the best MOSFET/driver combination that best meets your needs
- Approach 2: You have already selected your MOSFET/driver combination and want to design it into your application

The figure below shows the differences between these two approaches.

2 Overview

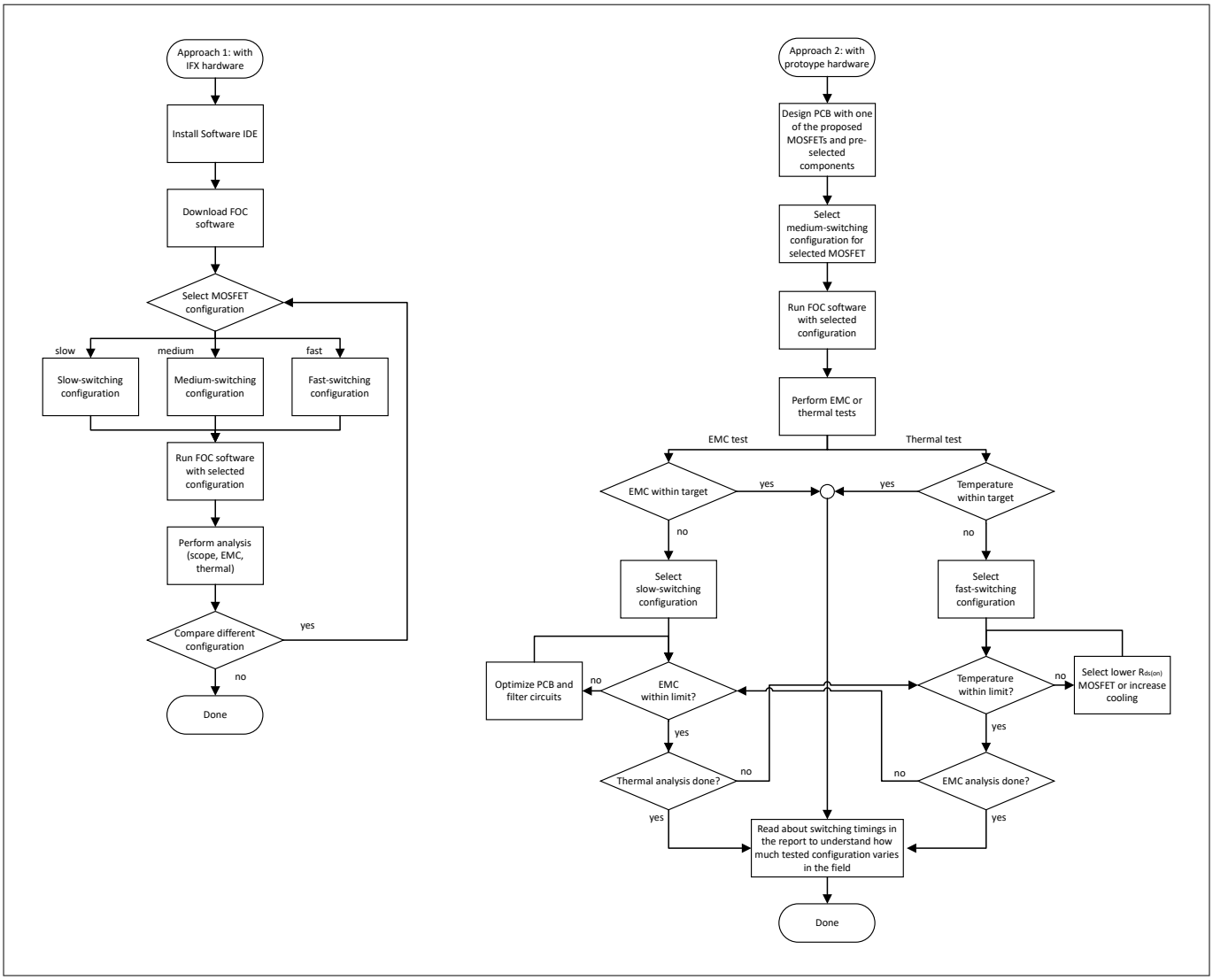

Figure 4 Decision tree

Approach 1: If you are currently considering which MOSFET/driver combination might be right for your application, read the chapter The example of the Generic Power Board. This chapter explains how the configuration of the driver and the selection of the MOSFET can change your EMC and power dissipation. This enables you to make a preliminary selection and already know how much you can still influence the performance of the system by programming only, or by exchanging the MOSFETs. You can also order the PCB and the Nanotec DB42S03 Motor and run some tests. Once you have the hardware, to set up your development environment, follow the following steps:

1. To obtain a working development environment, follow the first steps mentioned in the Generic power evaluation board user guide
2. Download the provided field-oriented control (FOC) example software (link) from the Infineon Development Center and open the Config Wizard. You can select the MOSFET that is present on the board and apply one of the three proposed MOSFET configurations (slow-, medium-, or fast-switching)
3. Run the FOC software with the Nanotec DB42S03 Motor
4. Now you can run various tests, such as switching time measurements, EMC analysis, or thermal analysis to confirm the behavior that is described in the report. You can also try out any of the three different driver configurations to see their effects

Approach 2: If you decide that the proposed Infineon OptiMOS ™ 6 MOSFET and Motix™MCU gate driver is a good fit for your application, you can design your own prototype PCB and test the proposed configuration for your specific solution. To make best use of the information provided in this document for your own PCB design, it is recommended that you follow the steps below.

1. Select a MOSFET from the provided list and design your PCB. Follow the external circuitry proposed in Schematics. For all other aspects, follow the Hardware design guideline. When your PCB is available, continue with step 2
2. Configure the driver with one of the three proposed settings for the selected MOSFET. To maintain some margin to optimize the switching for either EMC or thermal performance, it is recommended that you start with the medium-switching time setting
3. You can now do an EMC analysis and thermal analysis to get a first impression of the performance of your PCB. Based on your results, you can follow the steps below
   - If your EMC emission exceeds your limits: You can program the EMC-optimized gate driver configuration (slow-switching) and test again. If it is still too high, you must optimize the PCB by changing the filter components or changing the layout. If you are now within your EMC limits, you can take this switching time as your configuration, regardless of which OptiMOS ™ 6 MOSFET you use
   - If your power dissipation is too high: You can program the power-dissipation-optimized gate driver configuration (fast-switching) and test again, provided your EMC allows this. If you are already using the power-dissipation-optimized gate driver configuration and need further optimization, or this configuration causes your EMC limits to be exceeded again, you can select a smaller $R_{DS(on)}$ MOSFET and repeat the test with the same gate driver configuration. In this way, you can improve your power dissipation while maintaining your EMC performance. Alternatively, you can either introduce an additional cooling measure or optimize your layout so that the heat can be dissipated more efficiently
4. When you have found a MOSFET/driver configuration combination that meets your needs, you can refer to Configuration-dependent switching behavior. This shows you how much the switching behavior changes for each configuration, either during runtime via different application conditions, or between samples from different lots. In this way, you can estimate if the solution you have selected meets your objectives for the conditions of your tests only, or also for other conditions

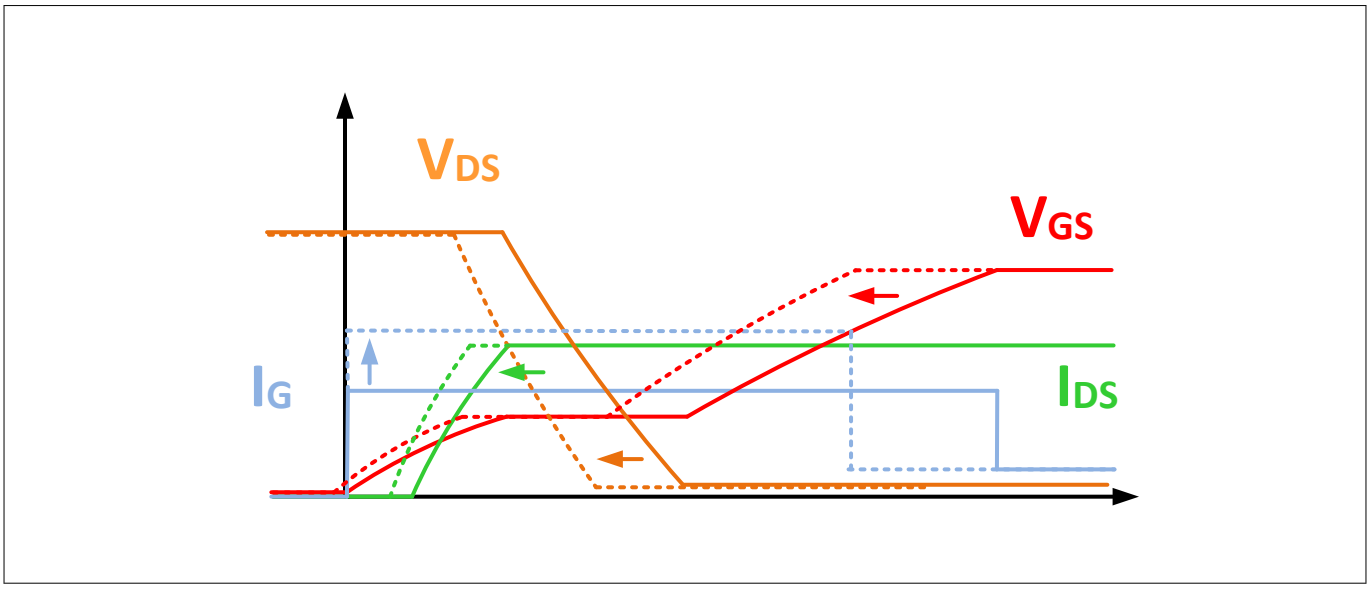

Figure 5 MOSFET switching with two different constant gate currents

The figure above illustrates the switching of a MOSFET and how changing the gate current applied by the driver influences it. The dotted lines represent one configuration with higher gate current and the non-dotted lines represent one configuration with lower gate current. The higher gate current speeds up the total switching time, which can be seen by the gate-source voltage (V_{GS}) reaching its maximum value earlier. The same happens to the drain current (I_{DS}) and the drain-source voltage (V_{DS}). So the turn-on delay is also decreasing. In addition to the delays, the slopes of both V_{GS} and I_{DS} also become steeper. This illustrates how changing the gate driver current configuration alone changes many aspects of the switching behavior.

3 Configuration-dependent switching behavior

This chapter describes all configurations and how they differ for better EMC (slow-switching), better power dissipation (fast-switching), or the ideal "sweet spot" (medium-switching). This chapter focuses on the impact of the individual gate driver or MOSFET and the impact of the operational conditions, such as temperature, supply voltage, and load current. The descriptions of the configurations are described in more detail in the chapter Characterization.

Gate driver configurations

The following list specifies the gate current register settings used for the three different configuration possibilities. Each current configuration is to be used with half-range configuration (DRV_CTRL3.ICHARGEDIV2_N = 0x00 & DRV_CTRL3.IDISCHARGEDIV2_N = 0x00).

- EMC-optimized (slow switching) configuration: DRV_CTRL3.ICHARGE_TRIM and DRV_CTRL3.IDISCHARGE_TRIM = 0x03
- Sweet-spot-optimized (medium switching) configuration: DRV_CTRL3.ICHARGE_TRIM and DRV_CTRL3.IDISCHARGE_TRIM = 0x07
- Power-dissipation-optimized (fast switching) configuration: DRV_CTRL3.ICHARGE_TRIM and DRV_CTRL3.IDISCHARGE_TRIM = 0x0B

The following table describes the register configuration of the TLE987x gate driver module for each configuration option.

Table 1 Gate driver module configurations

Register	Slow-switching	Medium-switching	Fast-switching
CTRL1	03030303_H	03030303_H	03030303_H
CTRL2	$0000\ 0303_H$	$0000\ 0303_H$	$0000\ 0303_H$
CTRL3	$0000\ 0303_H$	$0000\ 0707_H$	$0000\ 0B0B_H$
OFF_SEQ_CTRL T	$0000\ 0000_H$	$0000\ 0000_H$	$0000\ 0000_H$
ON_SEQ_CTRL T	$0000\ 0000_H$	$0000\ 0000_H$	$0000\ 0000_H$
TRIM_DRVx	$801F1F00_H$	$801F1F00_H$	$801F1F00_H$
CP_CTRL_STS	$0000\ 0005_H$	$0000\ 0005_H$	$0000\ 0005_H$
CP_CLK_CTRL	$0000\ CA16_H$	$0000\ CA16_H$	$0000\ CA16_H$

Schematics

The following figure and table show the schematics and specific component values used during the characterization. Selecting different components can change the behavior of the gate driver and therefore possibly results in different characteristics to those described in this report.

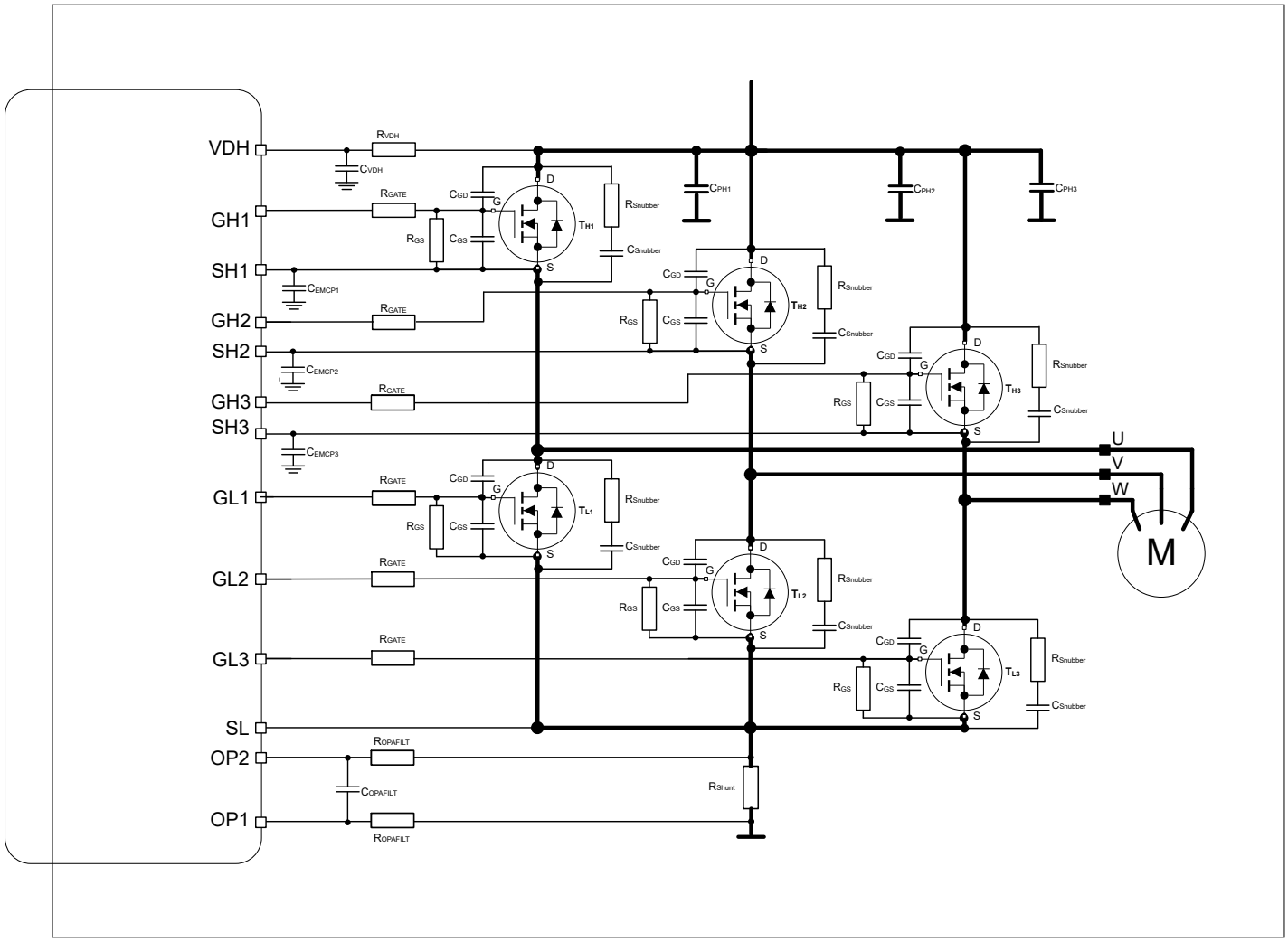

Figure 6 **B6-bridge schematic example for TLE987x**

Table 2 **Passive components inside B6 bridge used during characterization**

Symbol	Function	Value
C_{GS}	FET gate-source resistor	Not placed
R_{GS}	FET gate-source resistor	100kΩ
C_{GD}	FET gate-drain resistor	Not placed
$R_{Snubber}$	Snubber resistor	1Ω
$C_{Snubber}$	Snubber capacitor	18nF

3.1 The influence of the gate driver, MOSFET, and operational conditions on switching timings

The information in this chapter is designed to help you take the right decisions for your application. It highlights the most important factors that influence different switching timings. These factors are: gate driver, MOSFET, supply voltage, load current, and temperature. Before discussing the individual influencing factors, we outline the test conditions applied to our tests and the results on the key switching timings.

There are many factors to consider when designing hardware for motor control. One of the main challenges is to find the right gate driver and MOSFET for the target application. However, an even bigger challenge is to understand how operational and environmental conditions affect the behavior of the gate driver and the

MOSFET. Acquiring all this knowledge requires a lot of time and effort. And even then, it is still possible to overlook something that might result in unexpected application behavior in the field.

Therefore, this application note helps you to understand the Motix TLE9879x smart gate driver and IAUC100N04S6N022 MOSFETs. The aim is to reduce development effort and provide the necessary information to take the right decision. This application note discusses the characterization results of a number of Motix TLE9879QXA40 gate drivers tested with IAUC100N04S6N022 MOSFETs under different operational and environmental conditions. The following are the test conditions applied:

Test conditions

- Supply voltage
  - 9 V, 13.5 V, 16 V, and 18 V
- Temperature
  - -40°C, 25°C, 80°C, and 150°C
- Load current
  - 8 A, 18 A, and 30 A
- Gate charge & discharge current setting
  - 3, 7, and 11
- Gate drivers
  - 3 Motix™ TLE9879QXA40 gate driver samples
- MOSFETs
  - 30 OptiMOS™6 IAUC100N04S6N022 MOSFETs

Key switching timings

The following are the key switching timings for the combination of gate drivers and MOSFETs:

- Turn ON delay
- Turn OFF delay
- VDS fall time
- VDS rise time

The following gives a brief explanation of how the influencing factors affect the switching characteristics. For more information, refer to Characterization.

Gate drivers

Based on characterization results, the gate driver is the main contributor to the variations in turn ON, turn OFF, VDS rise time, and VDS fall time. The measured VDS rise time, VDS fall time, turn ON delay and turn OFF on each of the 3 gate driver samples differ significantly, especially at lower gate charge current settings. For example, Figure 7 shows measured VDS fall time on three different gate driver samples at three gate charge current settings when tested at operational conditions. The plot is divided into three sections, one for each gate charge current setting. The spread and measured VDS fall times are different for each gate driver sample.

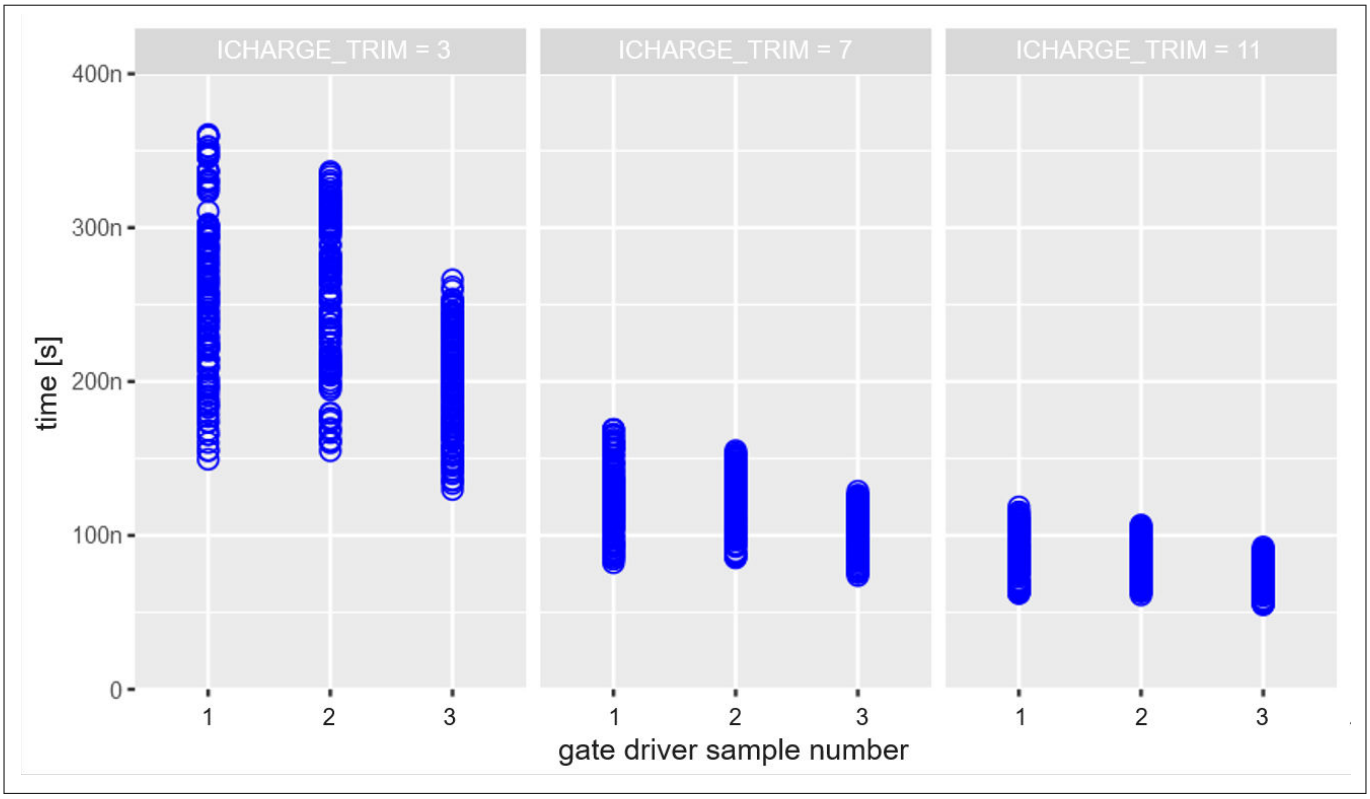

Figure 7 **The plot shows the comparison between measured VDS fall time of three gate driver samples when tested with a MOSFET at all test conditions.**

MOSFETs

The MOSFET does not have a significant effect on turn ON delay, turn OFF delay, VDS rise time, and VDS fall time when compared to the gate driver. The figure below shows VDS fall time of all high-side MOSFETs mounted on 7 PCBs in a 3-phase bridge configuration. Each PCB contains 3 high-side MOSFETs. The spread of the VDS fall time values is similar for various high-side MOSFETs at each gate charge current setting.

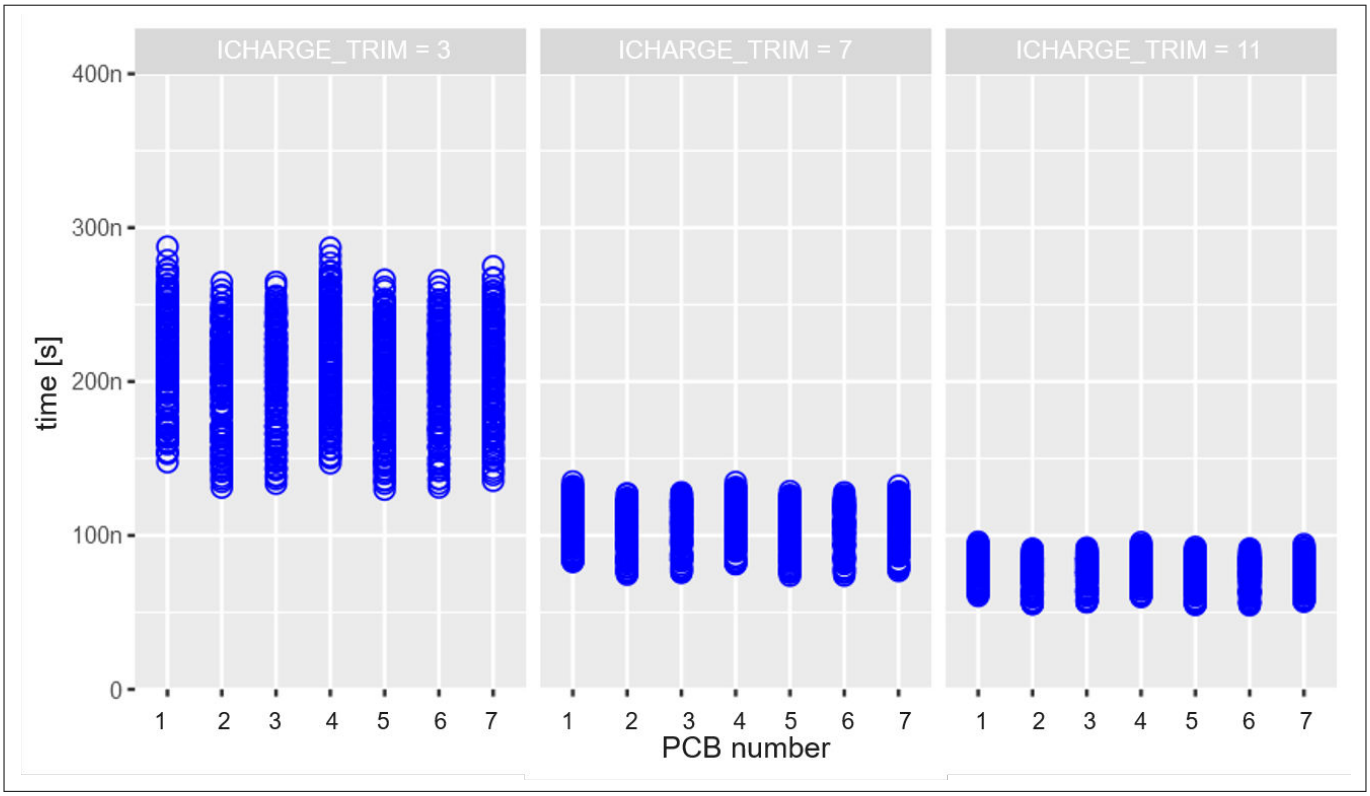

Figure 8 **The plots shows the comparison between measured VDS fall time when a gate driver sample is tested with all high-side MOSFETs at the full range of test conditions. The MOSFETs are mounted on each PCB in 3 phase bridge configuration.**

Supply voltage

The supply voltage influences VDS fall and VDS rise times, however, it does not have any noticeable influence on turn ON and turn OFF delay times. The plots in Figure 9 and Figure 10 show measured VDS fall times and VDS rise times at various supply voltages. The VDS rise and fall times are significantly influenced by supply voltages, especially at lower gate charge current settings. On the contrary, the change in turn ON and turn OFF delays with supply voltage is negligible at medium and higher gate charge current settings. There is a slight change in turn ON and turn OFF delays with different supply voltage at lower gate charge current settings, but it is insignificant.

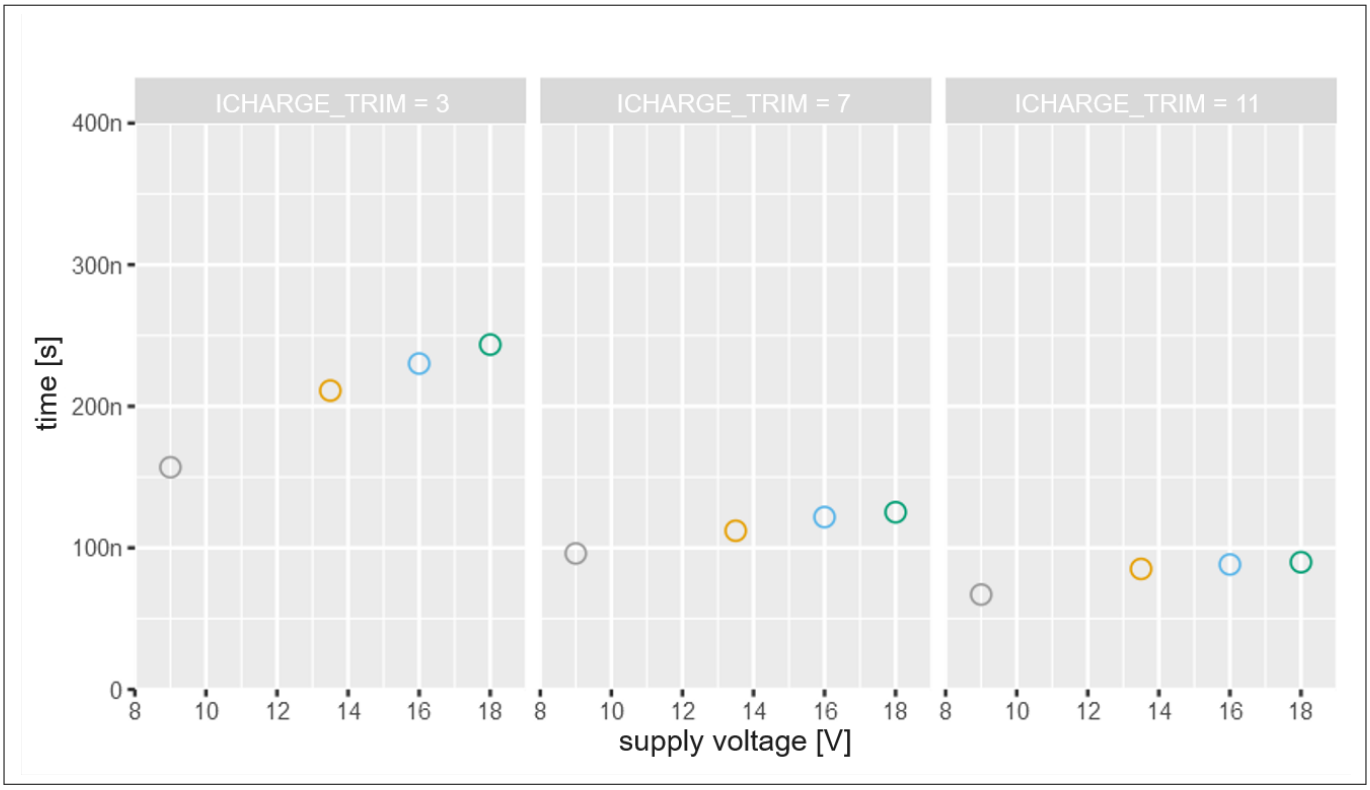

Figure 9 **The plot shows the dependency of VDS fall time for high-side MOSFETs on supply voltage at different gate charge current settings**

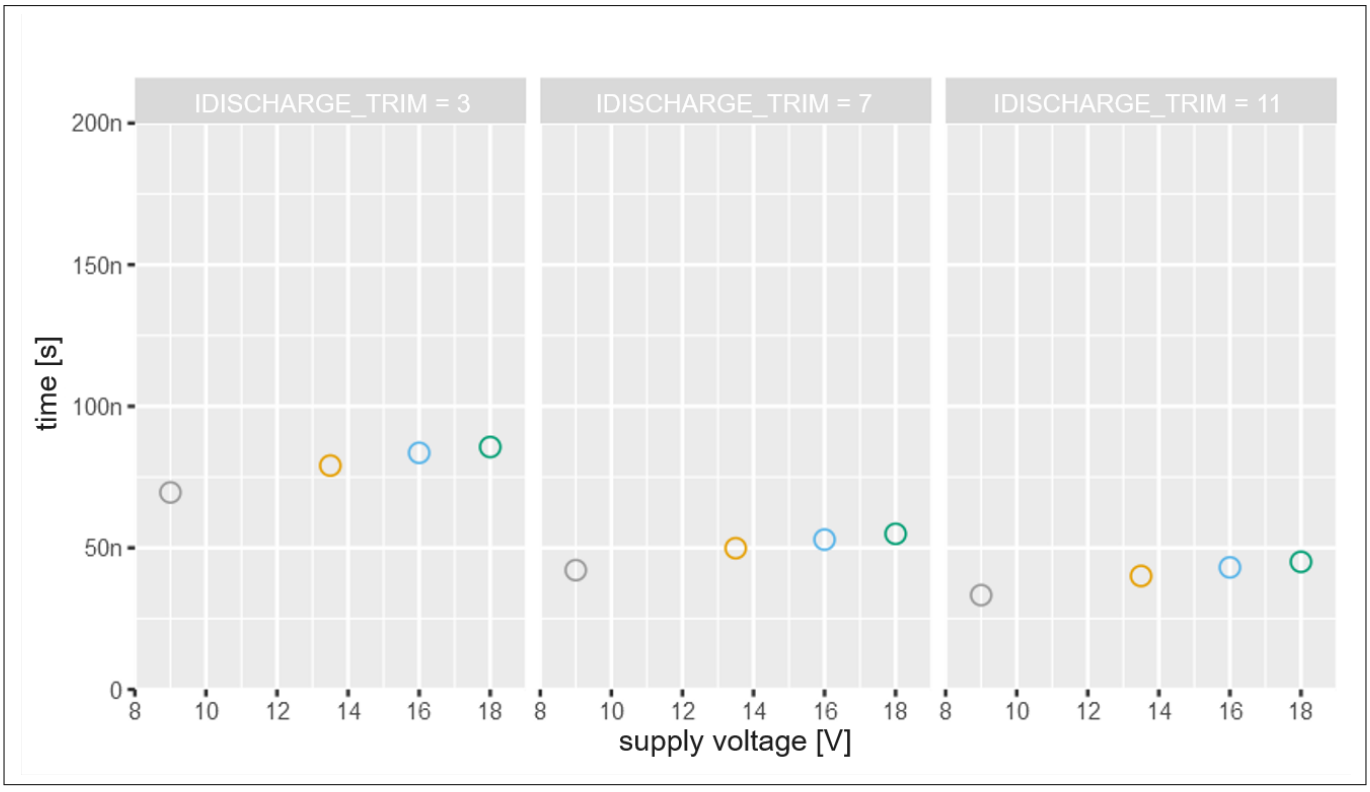

Figure 10 **The plot shows the dependency of VDS rise time for high-side MOSFETs on supply voltage at different gate discharge current settings.**

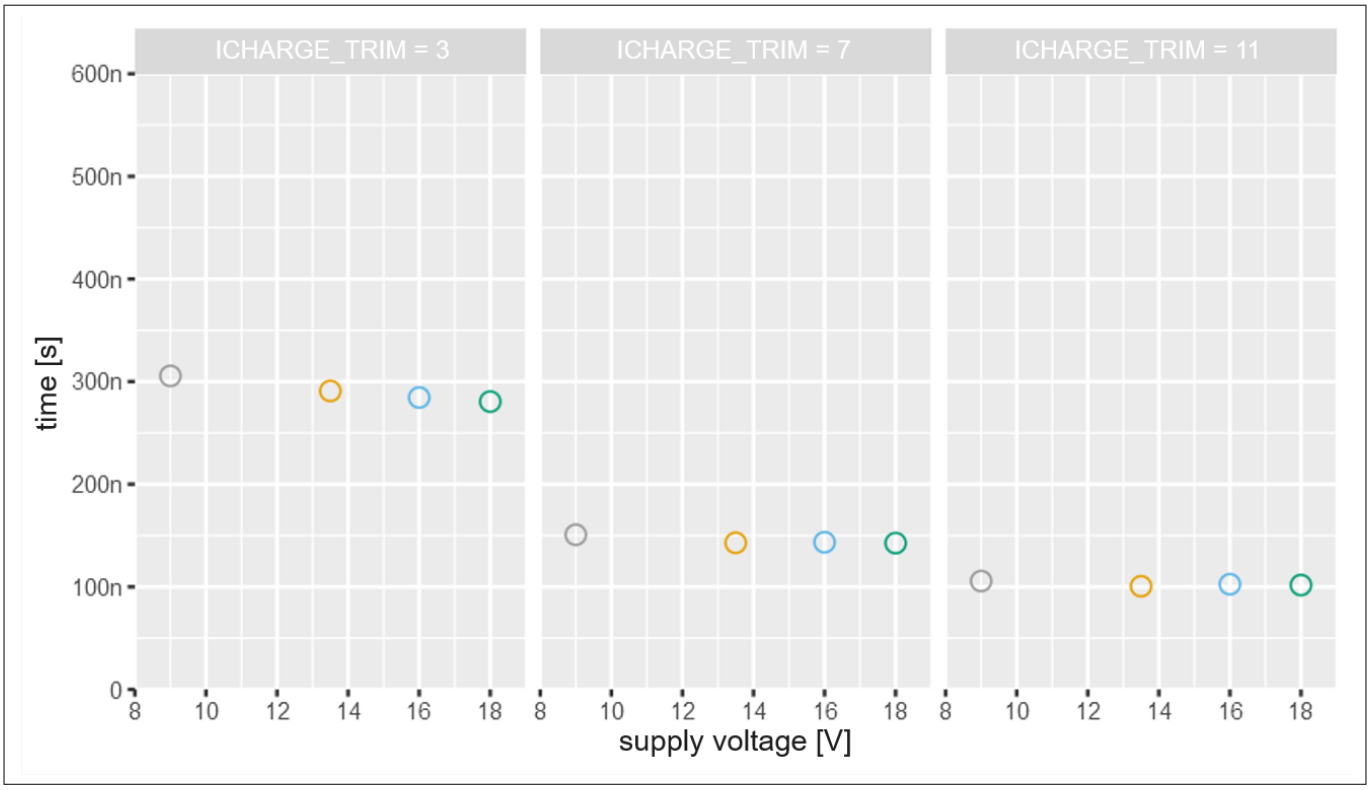

Figure 11 **The plot shows the dependency of turn ON delay for high-side MOSFETs on supply voltage at different gate charge current settings.**

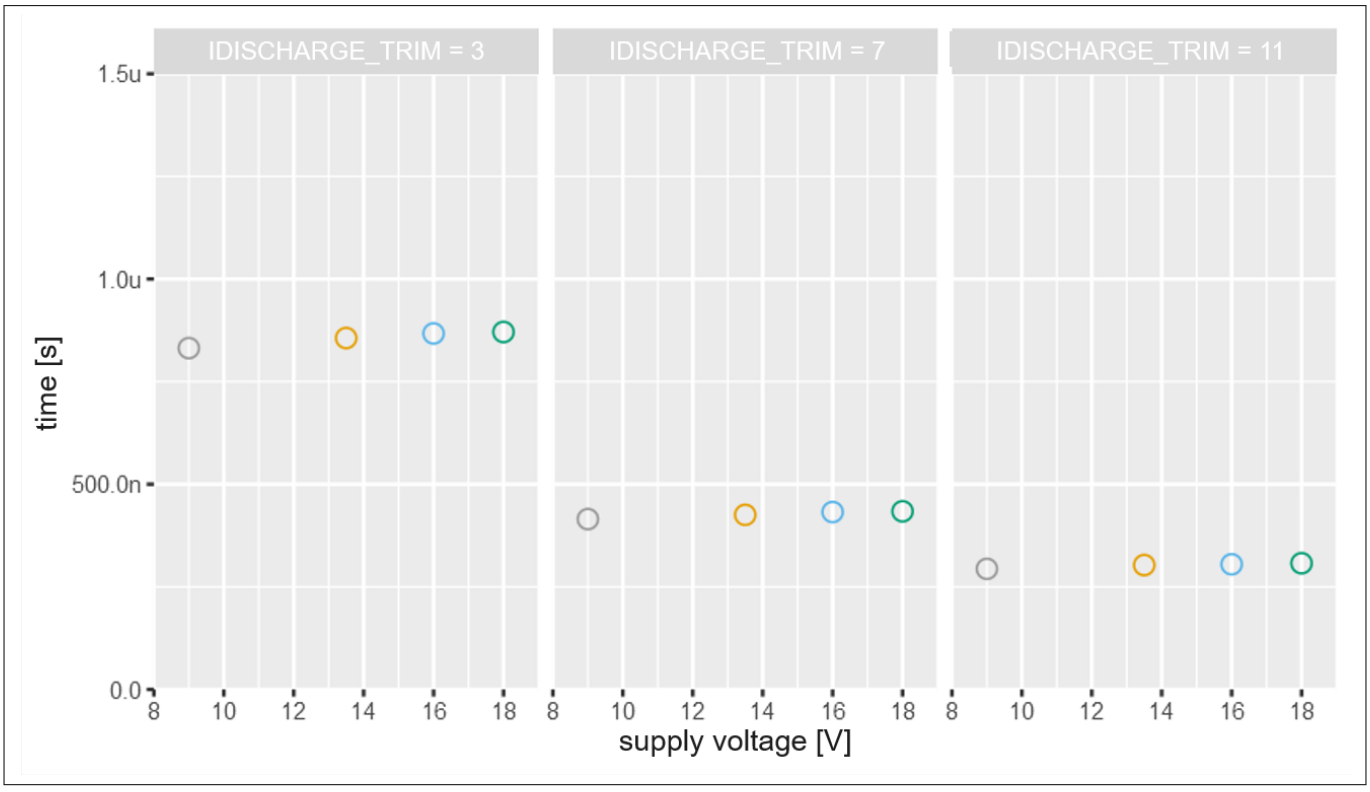

Figure 12 **The plot shows the dependency of turn OFF delay for high-side MOSFETs on supply voltage at different gate discharge current settings.**

Temperature

The change in temperature directly influences the VDS rise time, VDS fall time, turn ON delay, and turn OFF delay. The variation of VDS rise and fall times with temperature is prominent at lower gate charge current settings than at medium and higher gate charge current settings. The plots in Figure 13 and Figure 14 show measured VDS fall time and VDS rise time of high-side MOSFET at various temperatures. As it can be seen from the plots, the temperature has a very small influence on the turn ON delay. It decreases marginally with rising temperatures at all gate charge current settings as it can be seen in Figure 15. Figure 16 shows measured turn OFF delays at different gate discharge current settings. The turn OFF delay increases with rising temperatures, especially at lower gate discharge current settings.

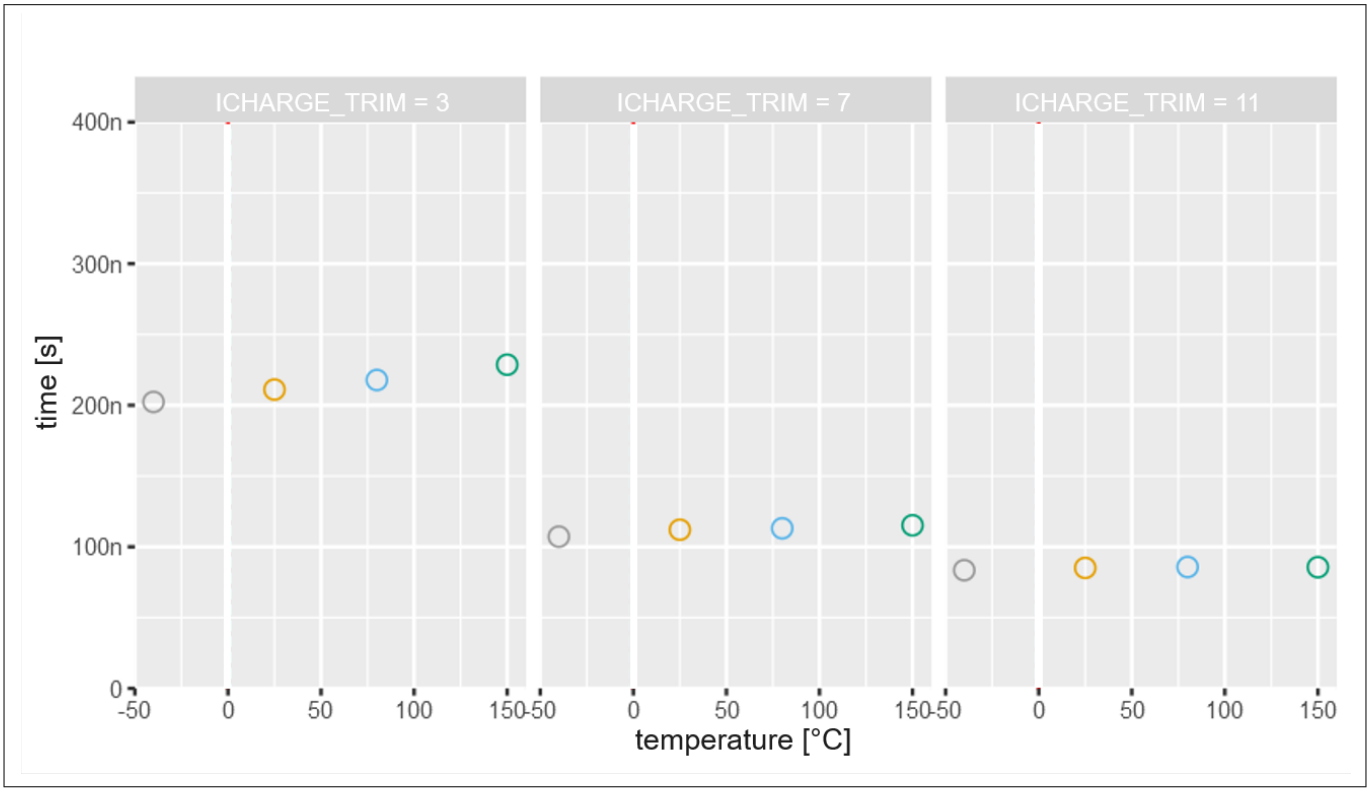

Figure 13 **The plot shows the dependency of VDS fall time for high-side MOSFETs on temperature at different gate charge current settings.**

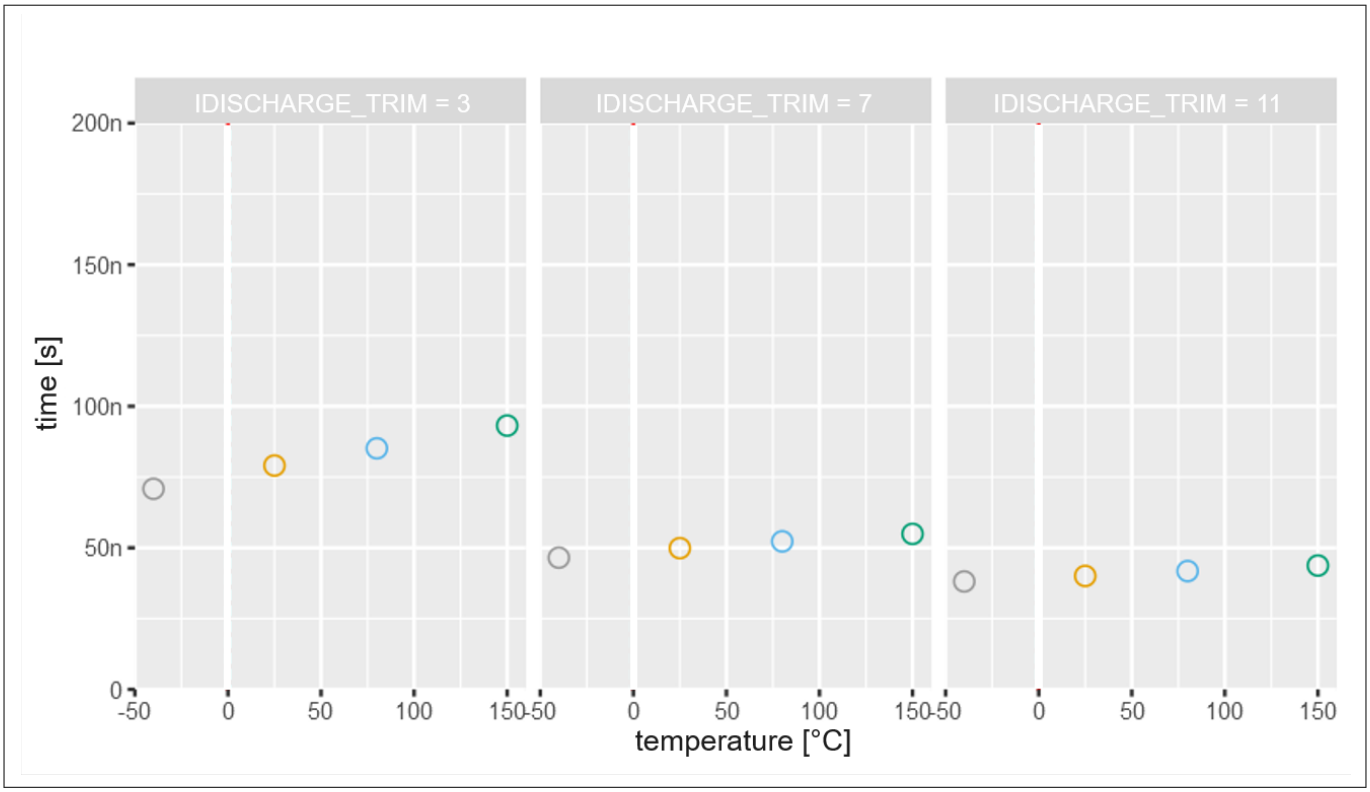

Figure 14 **The plot shows the dependency of VDS rise time for high-side MOSFETs on temperature at different gate discharge current settings.**

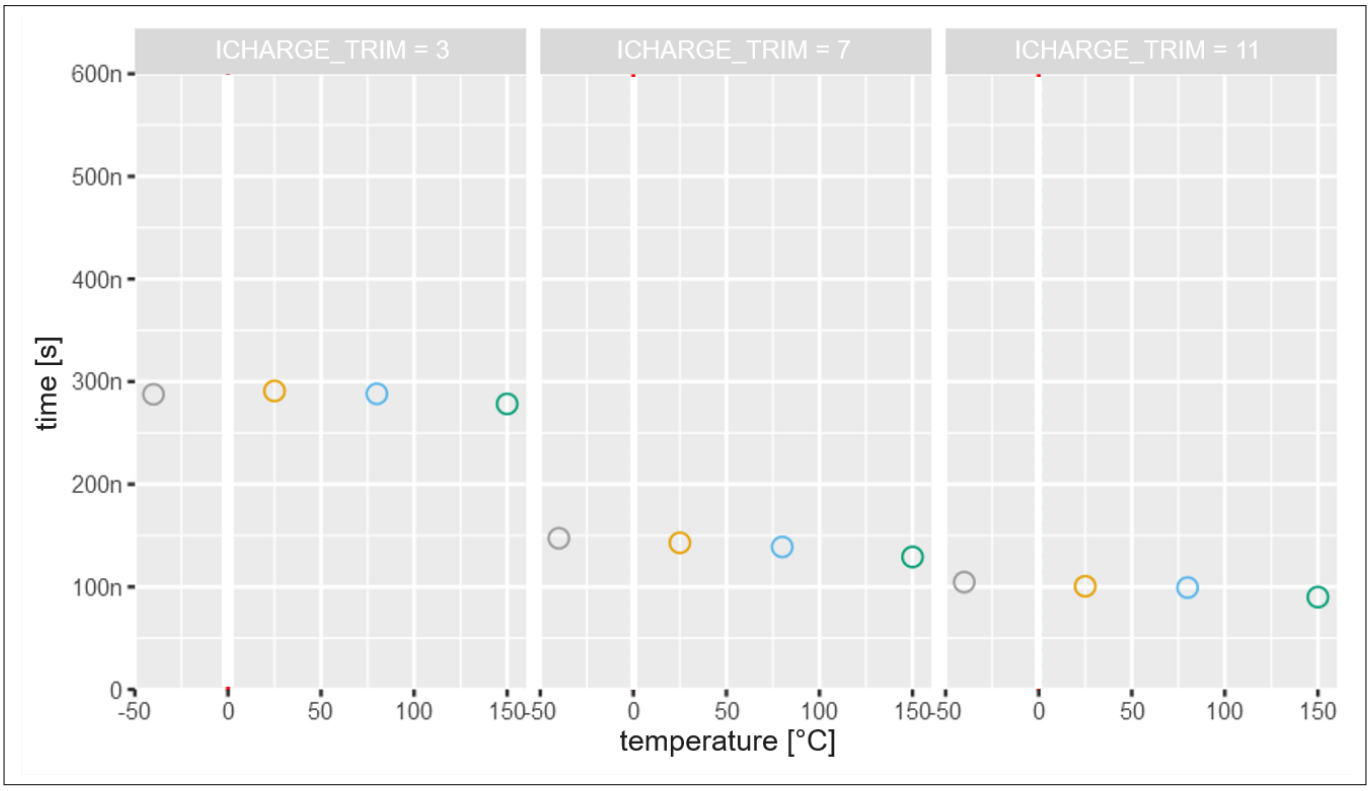

Figure 15 **The plots shows the dependency of turn ON delay for high-side MOSFETs on temperature at different gate charge current settings.**

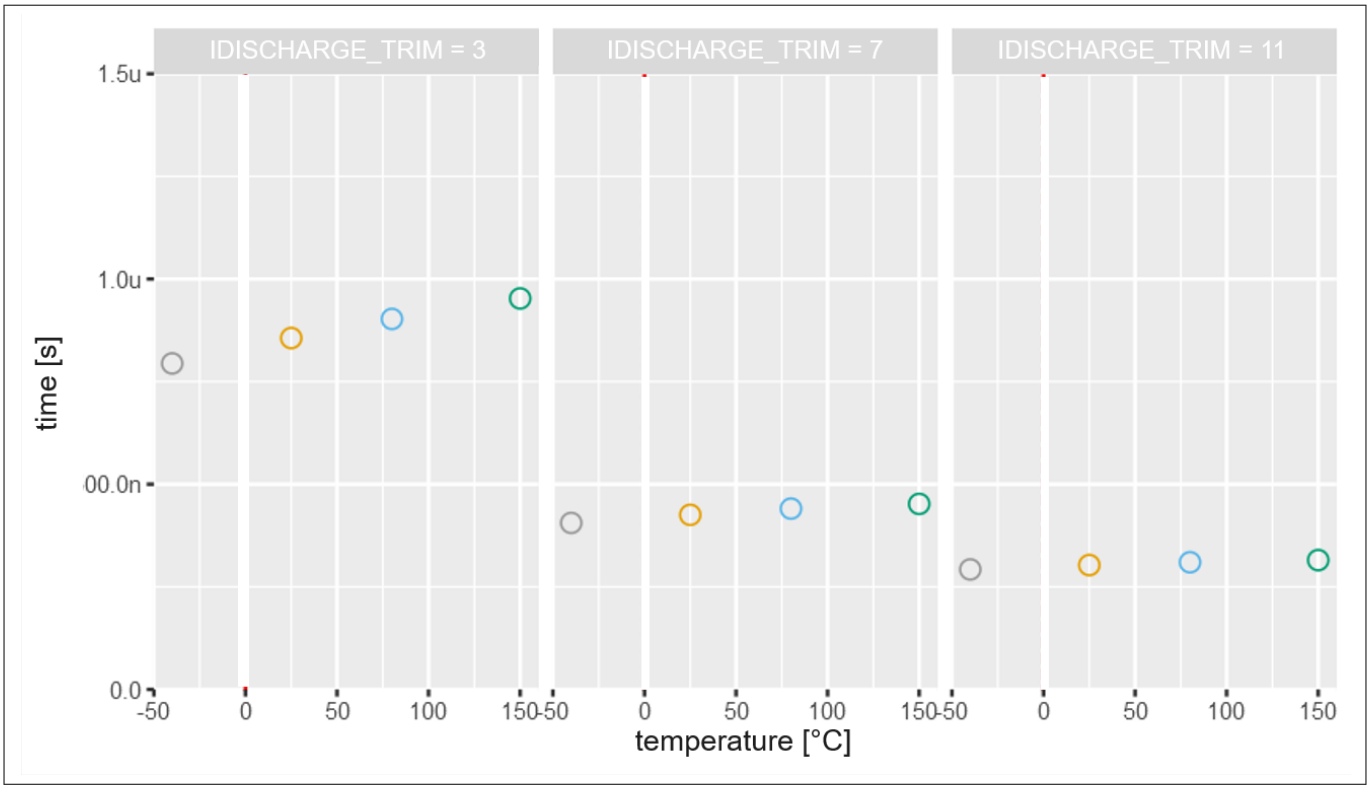

Figure 16 **The plot shows the dependency of turn OFF delay for high-side MOSFETs on temperature at different gate discharge current settings.**

Load current

Based on the characterization data, the influence of load current on VDS rise and fall times is negligible. Figure 17 and Figure 18 show measured VDS fall and rise times for high-side MOSFET at different load currents. It can be seen from these plots that the measured time does not vary significantly with load current. There is a slight variation in measured VDS fall and rise time with load current but it can be ignored. Figure 19 shows measured turn ON delay for high side MOSFETs at different load currents. The turn ON delay increases with increasing load current at lower gate charge current settings. However, turn ON delay looks almost identical for all load currents at medium and high gate charge current settings. This unexpected behavior is a result of voltage transient at source pin of the MOSFET due to inductance during the turn ON phase. It is explained in detail in section [reference]. The turn OFF delay decreases slightly with increasing load current at all gate charge current settings as can be seen in Figure 20.

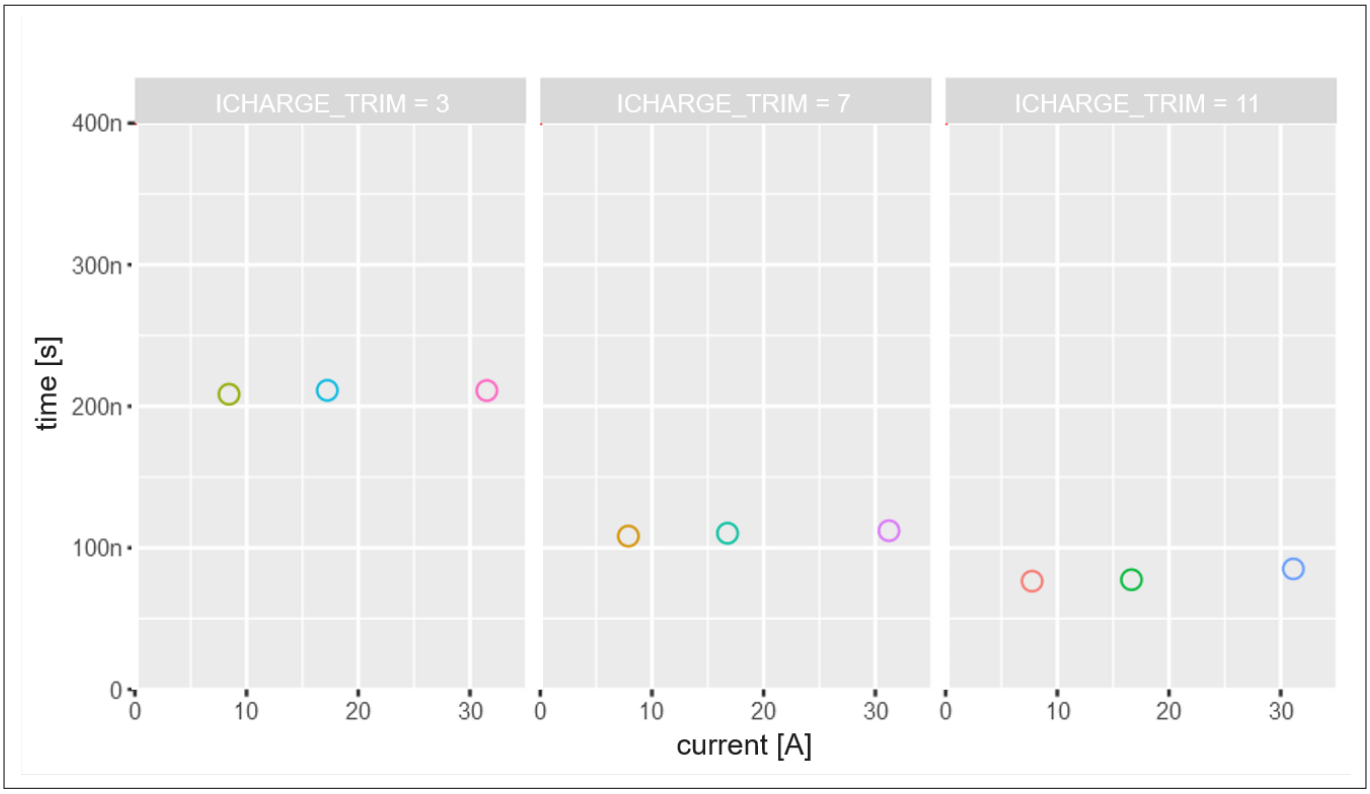

Figure 17 **The plot shows the dependency of VDS fall time for high-side MOSFETs on load current at different gate charge current settings.**

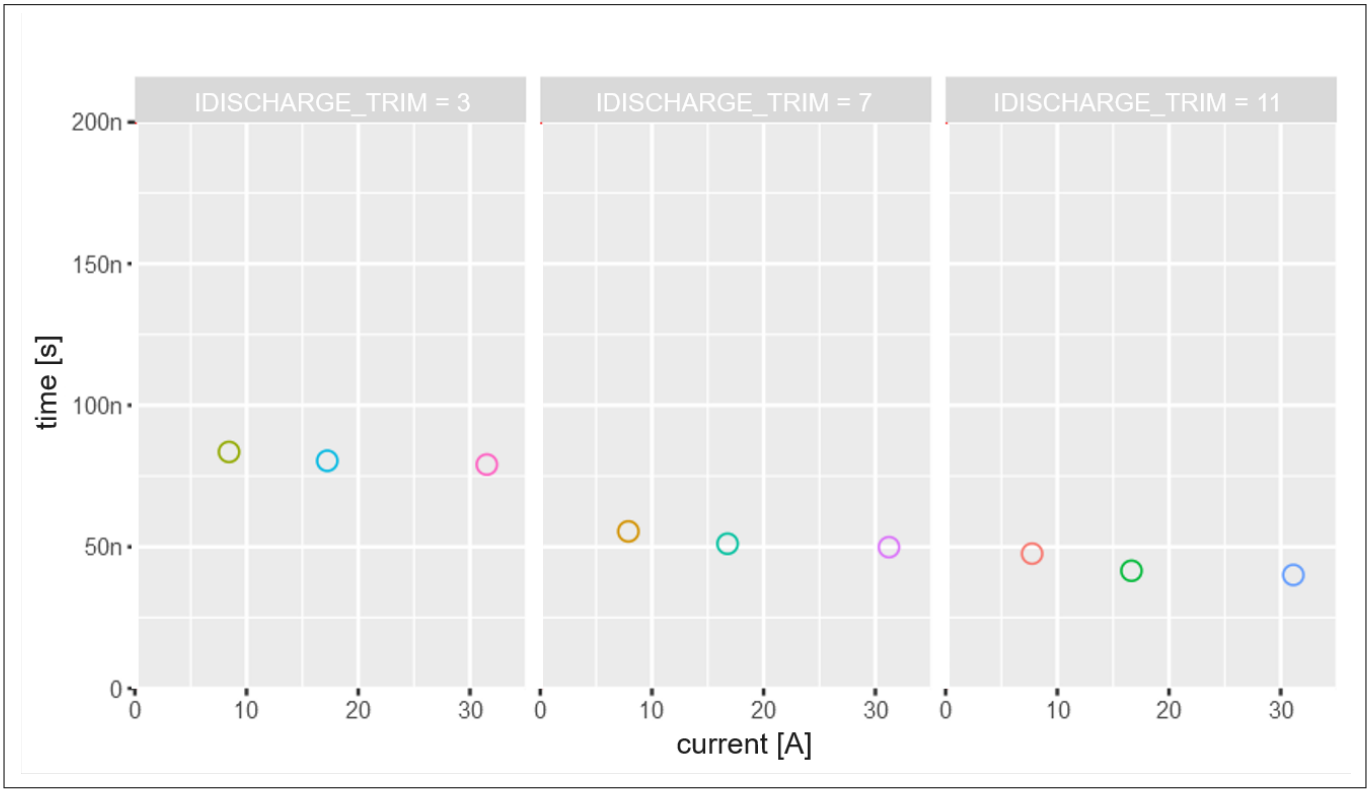

Figure 18 **The plot shows the dependency of VDS rise time for high-side MOSFETs on load current at different gate discharge current settings.**

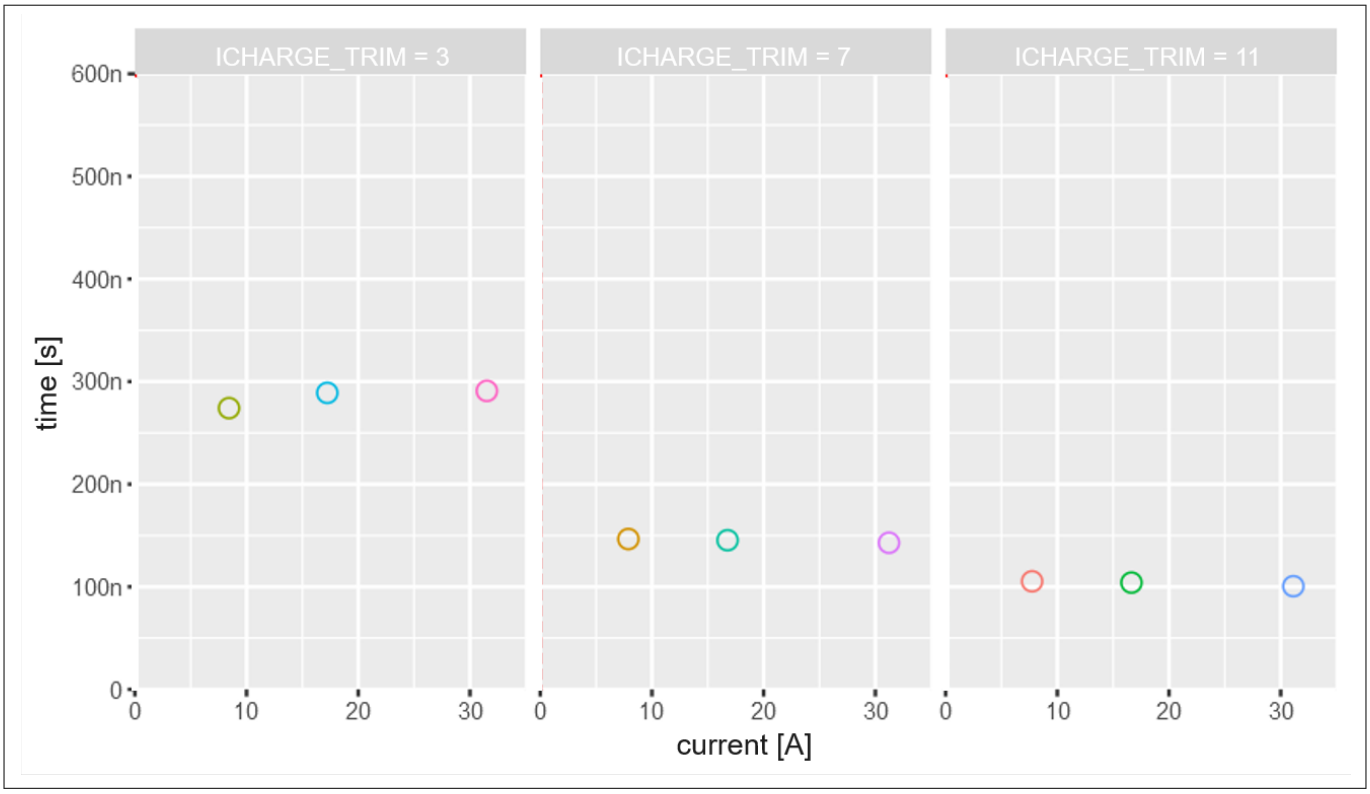

Figure 19 **The plot shows the dependency of turn ON delay for high side MOSFETs on load current at different gate charge current settings.**

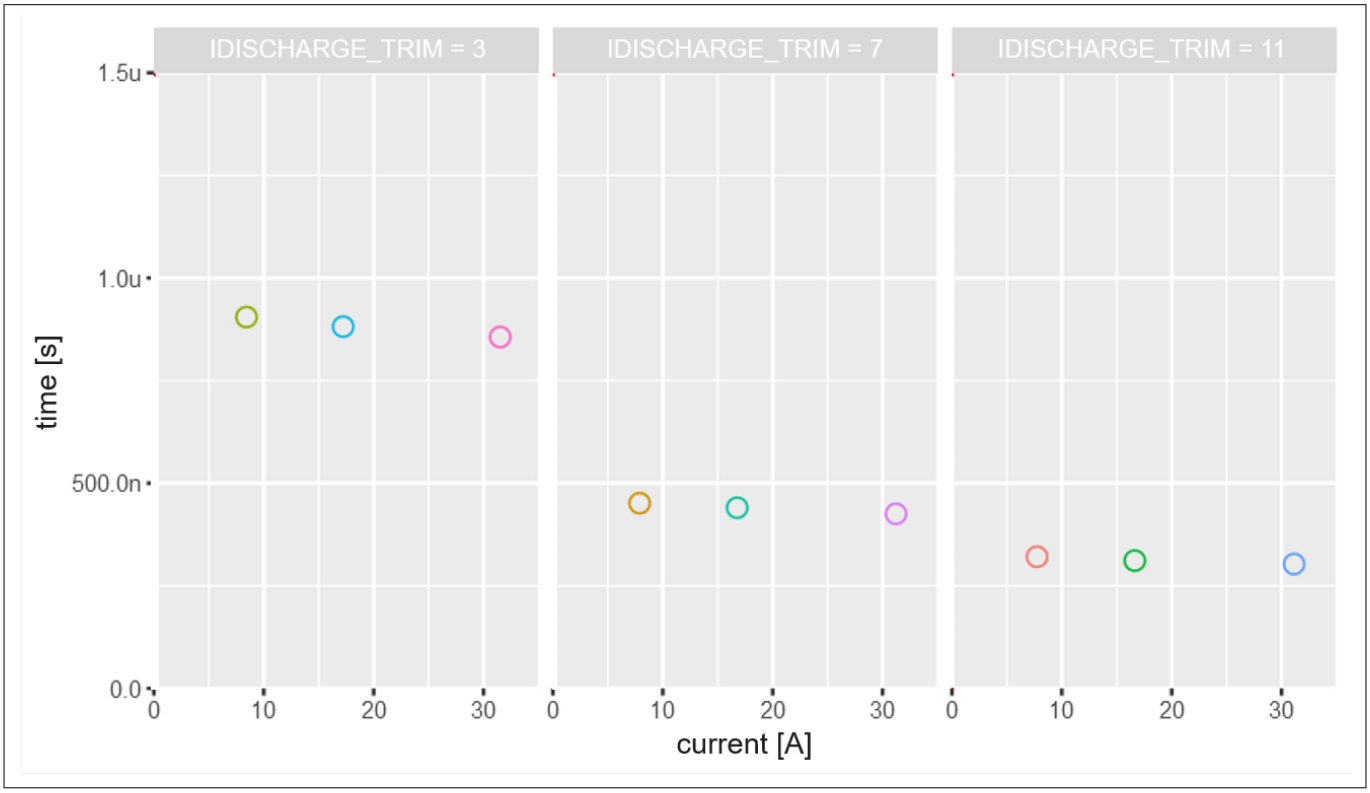

Figure 20 **The plot shows the dependency of turn OFF delay for high side MOSFETs on load currents at different gate charge current settings.**

Difference in high-side and low-side MOSFET switching times

The measured VDS fall time and turn ON delay of high-side and low-side MOSFETs are significantly different as can be seen in Figure 21 and Figure 22.

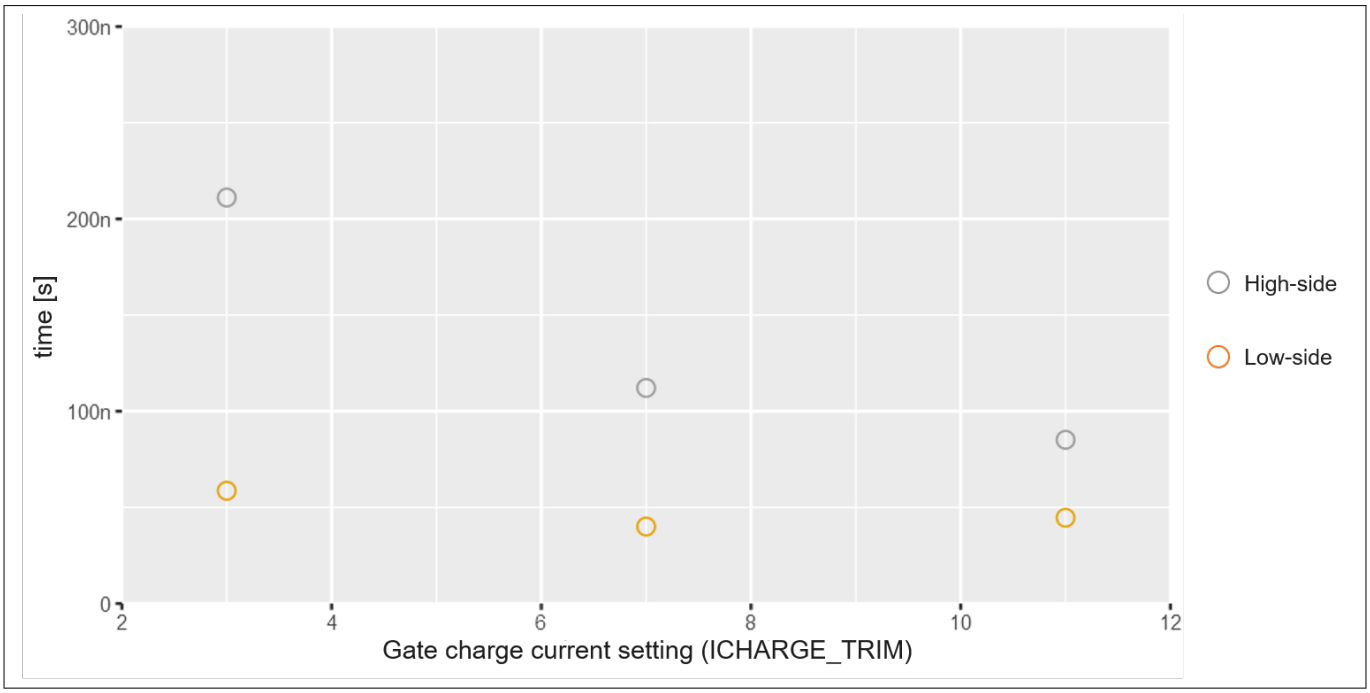

Figure 21 **The plot shows the comparison between measured VDS fall times for high-side and low-side MOSFETs**

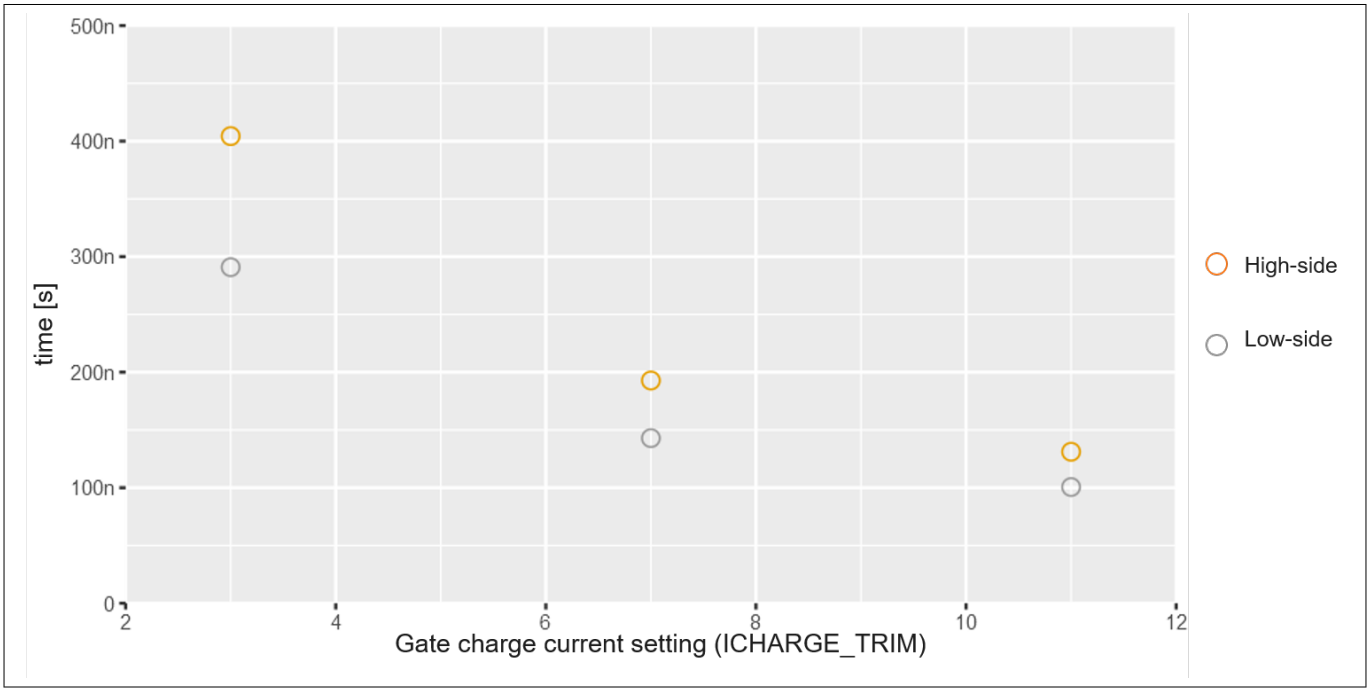

Figure 22 **The plot shows the comparison between measured turn ON delay for high-side and low-side MOSFETs**

The reason for different VDS fall time and turn ON delay for high-side from low-side MOSFETs is parasitic inductance of the PCB. Due to parasitic inductance, the gate charge current of low-side MOSFET increases during the turn ON phase. The figure below shows the gate charge current of a high-side MOSFET on the left

and a low-side MOSFET on the right at gate charge current setting of 3. The gate current of the low-side MOSFET is higher compared to the high-side MOSFET and as a result, the gate capacitor of the low-side MOSFET charges faster when compared to the high-side MOSFET and consequently the faster switching of the MOSFET takes place.

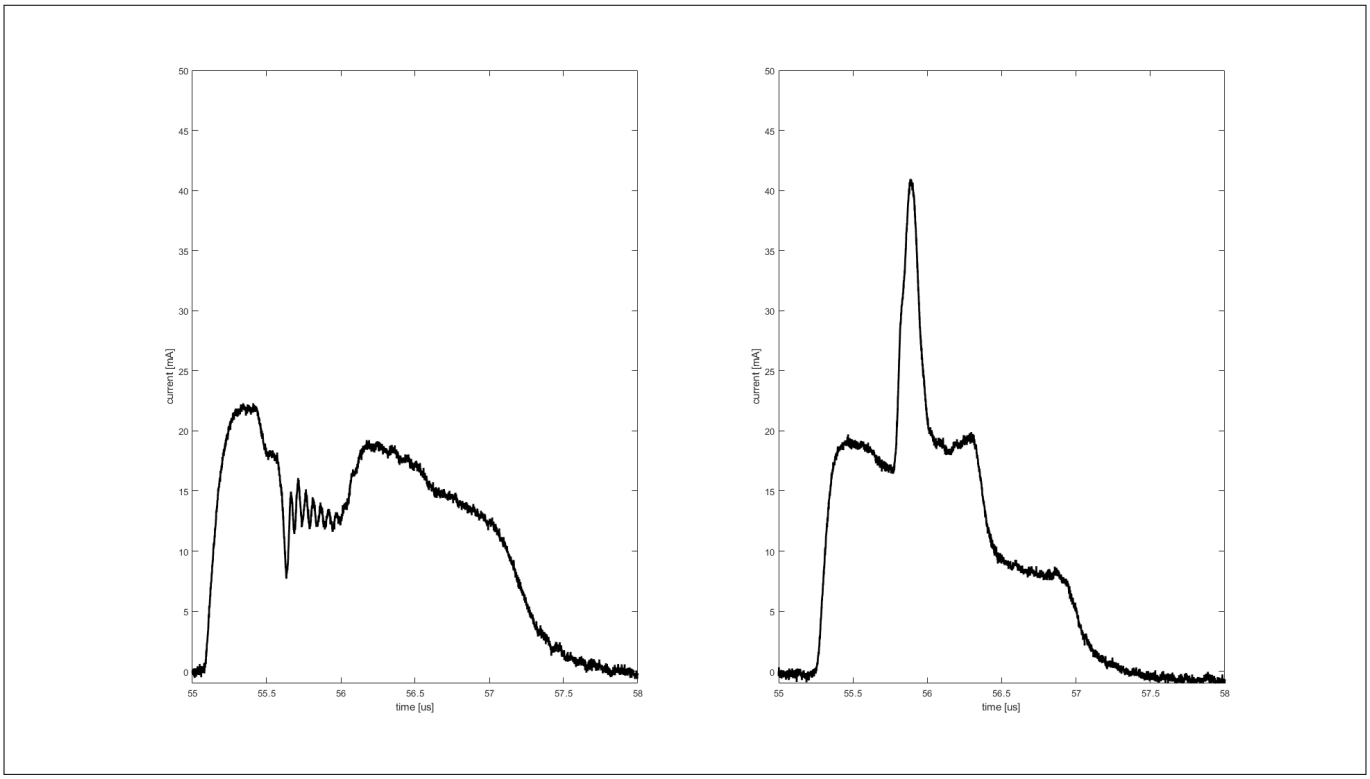

Figure 23 The figure shows the comparison between gate charge current for high-side (left) and low-side MOSFETs (right) waveform at 3 gate charge current setting

Conclusion

To summarize the outcome of measurements, the gate driver is the main contributor to the variation of VDS rise time, VDS fall time, turn ON delay, and turn OFF delay. The MOSFET does not influence the VDS fall time, VDS rise time, turn ON-, and turn OFF delays. Each operational condition has various influences on the VDS fall time, VDS rise time, turn ON-, and turn OFF delays. The VDS rise and fall times are significantly influenced by supply voltages at a constant gate charge/discharge current. On the other hand, turn ON- and OFF delays do not change with supply voltage. The temperature has significant influence on VDS rise time, VDS fall time, and turn OFF delays, especially at lower gate charge current settings. However, turn ON delay does not change much with temperatures. There is no influence of load current on VDS rise- and fall times. The turn ON delay increases with increasing load current. On the other hand, turn OFF delay decreases with increasing load current.

3.2 Characterization

The following sections discuss the characterization results.

3.2.1 Setup information

An automated test setup is used to characterize gate drivers and MOSFETs. With the help of this setup, the switching times for the various combination of gate drivers and MOSFETs are measured for various test conditions.

The automatic test setup consists of a characterization board and the following equipment:

- Differential probes
- Current probes
- 3-phase motor
- 8-channel oscilloscope
- DC power supply
- Thermostream

Characterization methodology

To measure the switching timings, the MOSFET under test is controlled by the gate driver. Depending on the duty cycle, the gate driver turns ON the MOSFET for a particular duration before turning it OFF. The gate charge current, gate to source voltage, drain-to-source voltage and load current waveforms are captured during MOSFET switching as can be seen in Figure 24. These waveforms are then post-processed to measure the switching timings. Note that the testing of MOSFETs is sequential. That means MOSFETs are tested one after another in the full bridge. The gate-source, drain-source, and load current waveforms of active MOSFETs only are captured. The figure below shows the half bridge in which the MOSFET at HS1 position is under test. In this case , the HS1 and LS1 are being driven by complementary PWM mode. HS2 is always OFF and LS2 is always ON. The load current is measured with a current probe at the phase and gate-source voltage, drain-source voltage is measured at the target MOSFET.

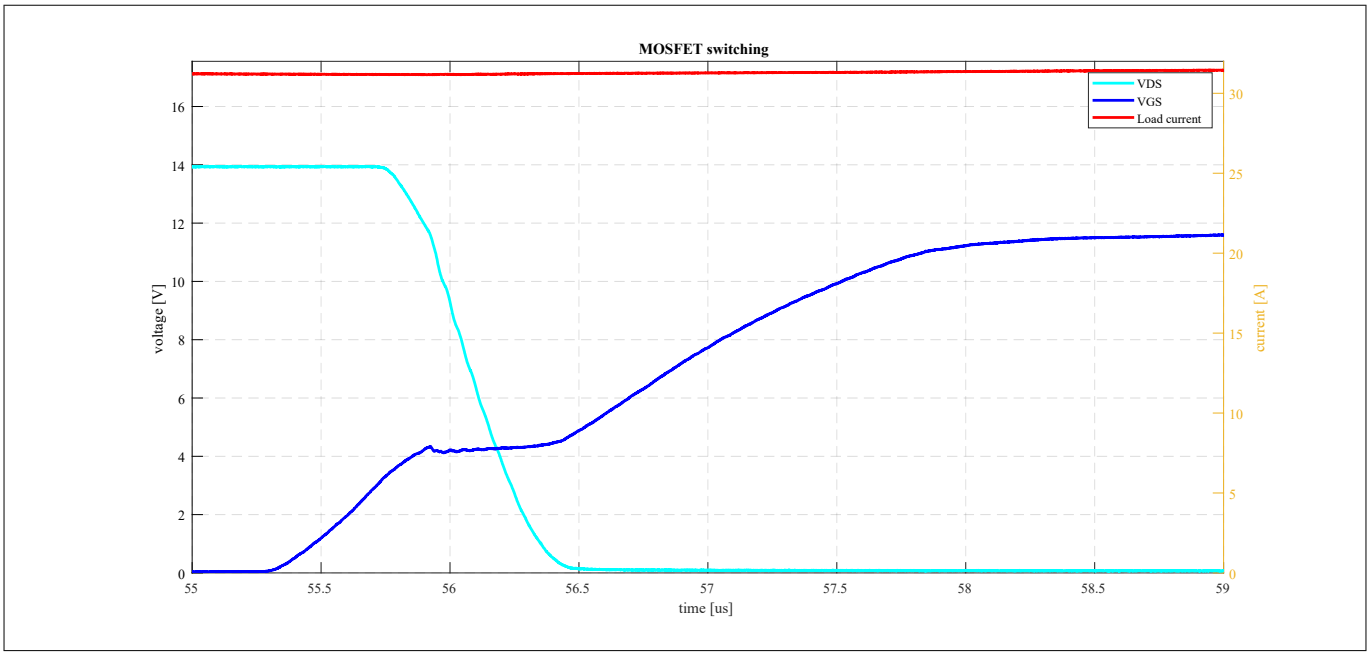

Figure 24 Example of MOSFET switching waveforms during testing

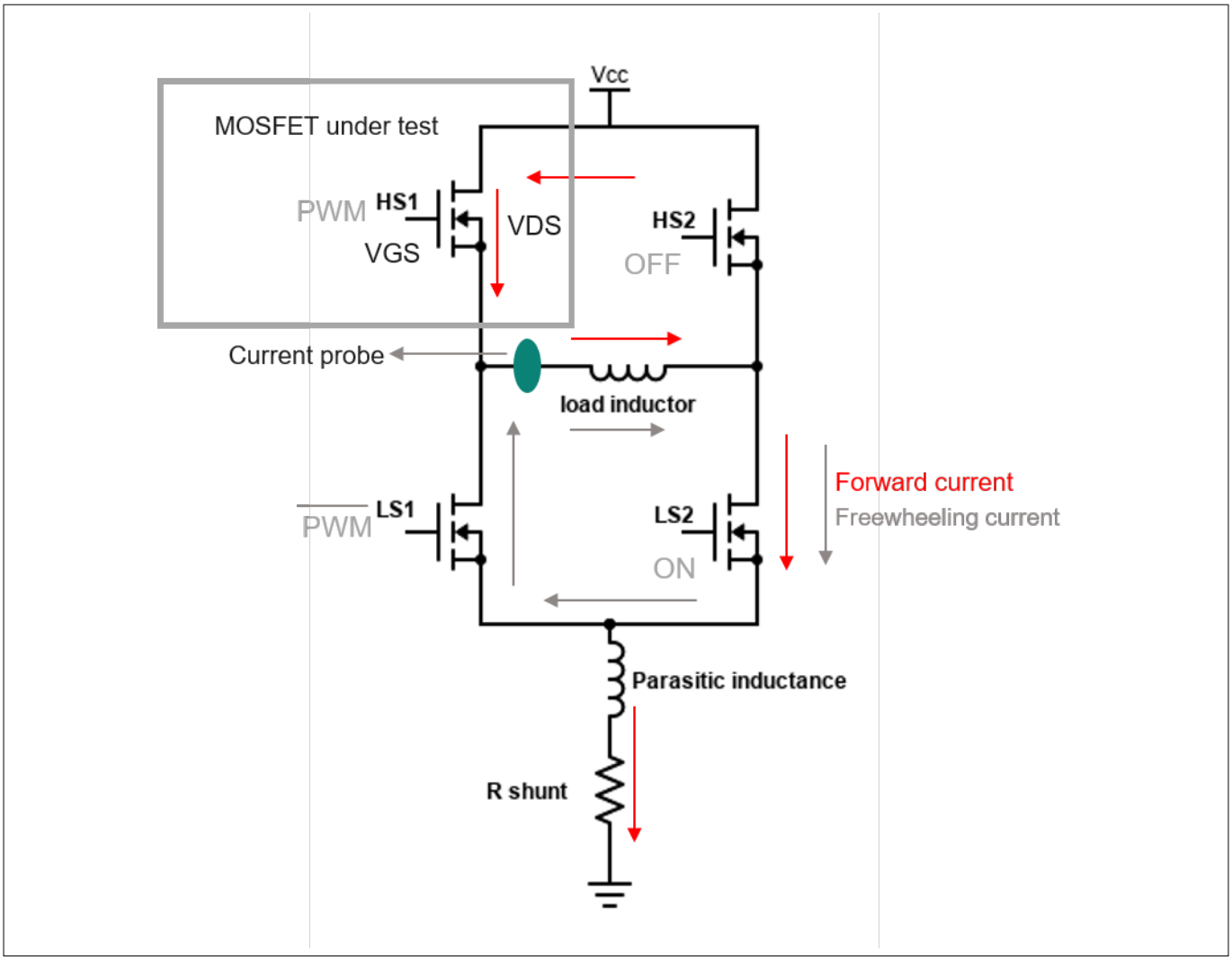

Figure 25 The figure shows the half bridge in which MOSFET at HS1 position is under test.

Structure of characterization results

The characterization results are structured according to the figure below. This provides information about rise and fall times, and turn-on and turn-off delays. For each of these timings, the results distinguish between high-side and low-side MOSFETs and give information about the influence of the driver, MOSFET, supply voltage, temperature, and load current.

3 Configuration-dependent switching behavior

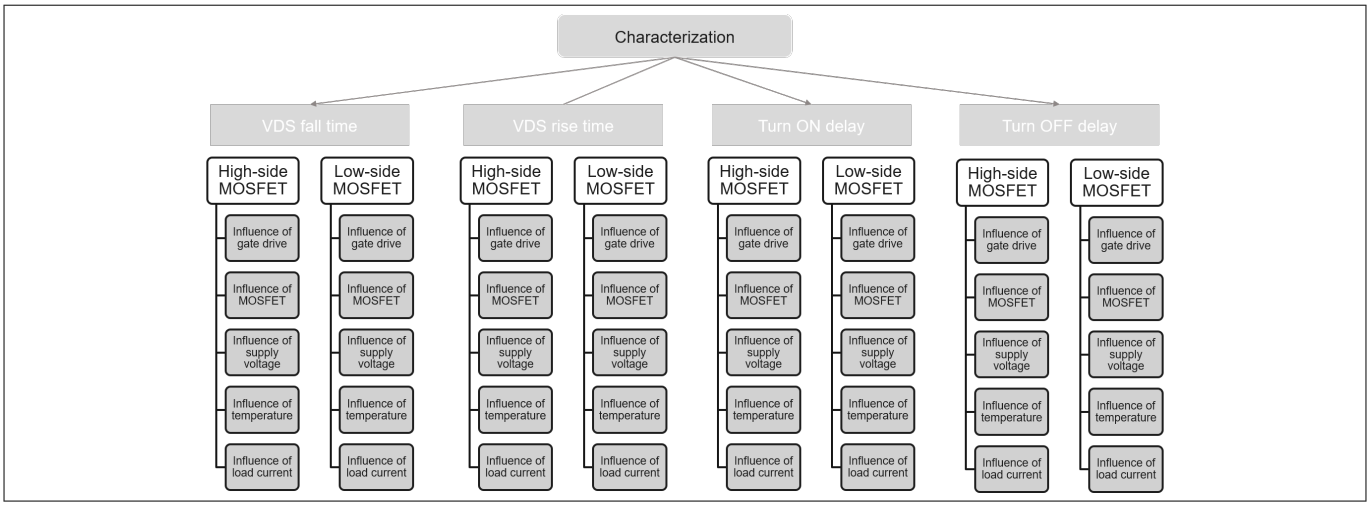

Figure 26 Structure of characterization results

3.2.2 VDS fall time

The VDS fall time is the time that drain-to-source voltage requires to go from 80% to 20% of its nominal value as given in Figure 27. It is one of the key times describing the switching performance of MOSFETs.

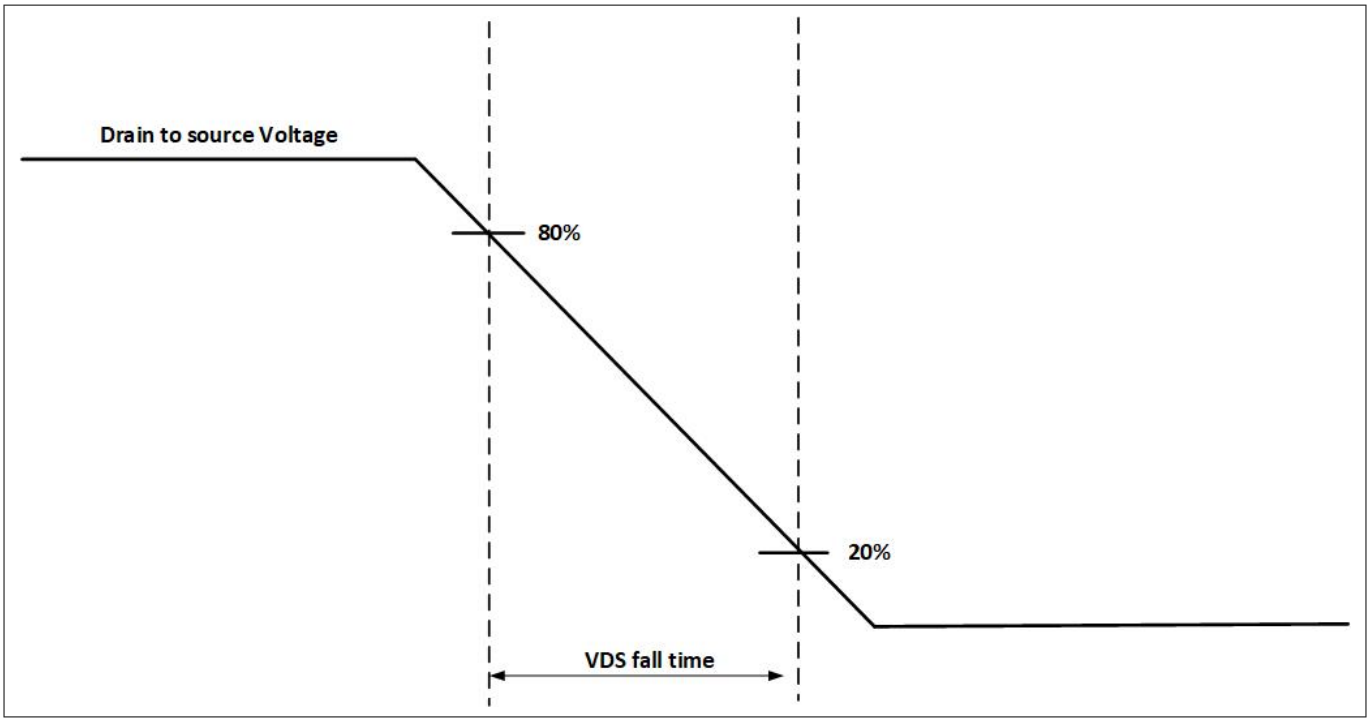

Figure 27 Definition of VDS fall time

The following section discusses measured VDS fall time results.

3.2.2.1 Fall time in high-side MOSFETs

VDS fall time measured with various drivers and MOSFETs at all operational conditions

The VDS fall time of the MOSFET is inversely proportional to the gate charge current. The plot in Figure 28 gives measured VDS fall times at various gate charge current settings. These VDS fall time values are measured when 3 gate driver samples are tested under all Test conditions with all high-side MOSFETs. Each data point in the plot represents VDS fall time measured at one of all the possible combinations of test conditions (supply voltage, temperature, load current, gate drivers, and high-side MOSFETs). The spread in VDS fall times decreases with increasing gate charge current settings. The following sections discuss factors influencing VDS fall time.

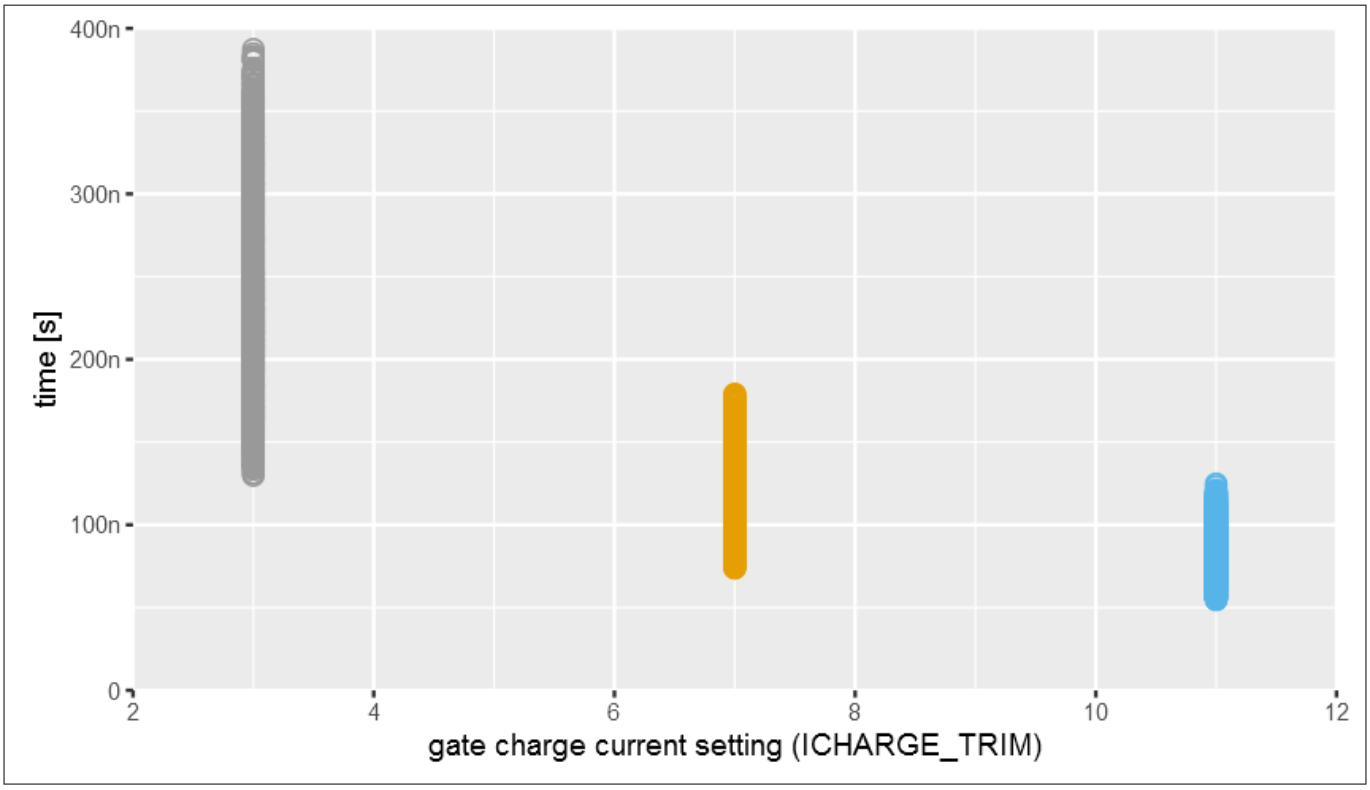

Figure 28 **Measured VDS fall time of high-side MOFSETs at various gate charge current settings. It is measured when various gate driver samples are tested with all high-side MOSFETs under all test conditions**

3.2.2.1.1 The influence of the gate driver

The plot in Figure 29 shows measured VDS fall time of various gate driver samples measured at three gate charge current settings. It is measured when each gate driver is tested with multiple high-side MOSFETs under all Test conditions. The spread of VDS fall time values is different for each gate driver sample. This difference in spread in VDS fall time values directly indicates that the gate driver is the main contributor to variation in measured VDS fall time.

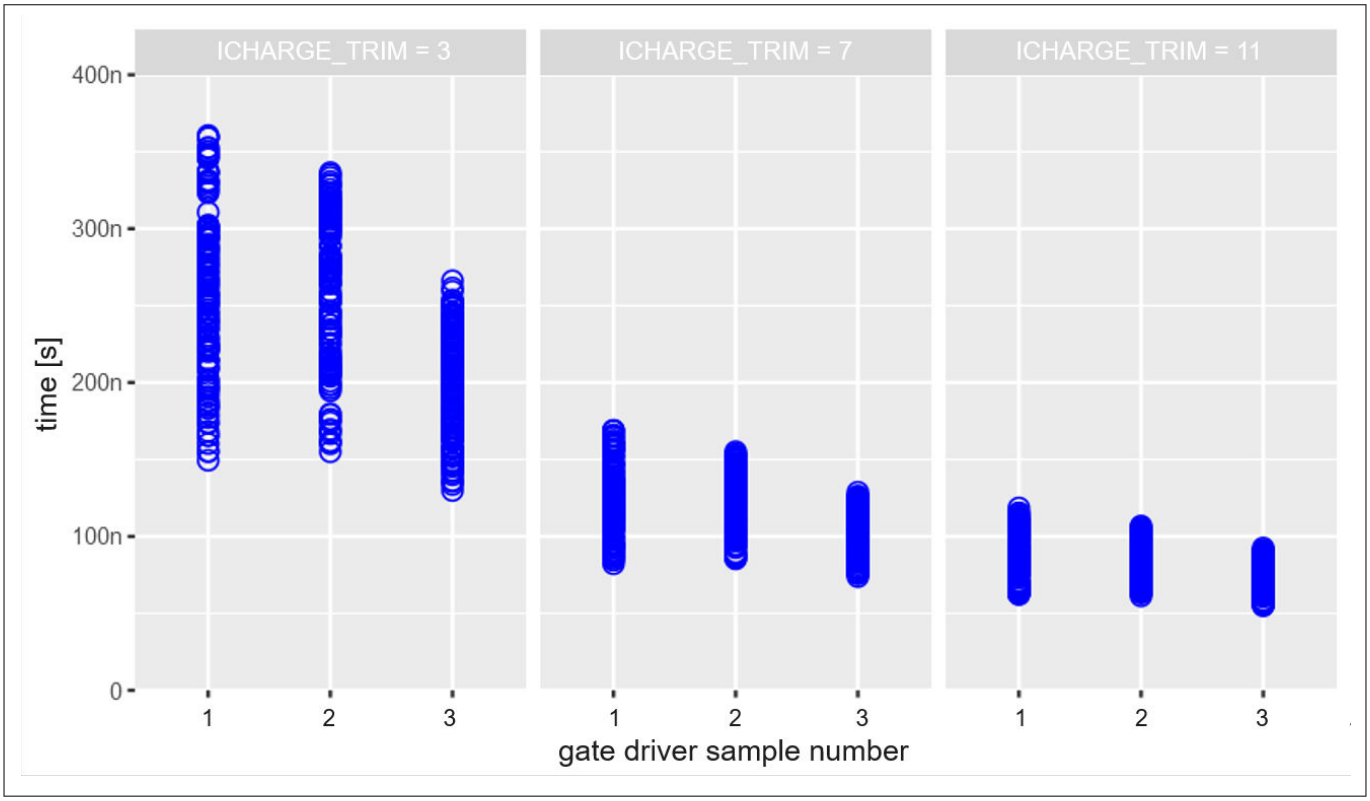

Figure 29 **VDS fall time of various gate driver samples at different gate charge current settings. It is measured when each gate driver is tested with multiple high-side MOSFETs at all operational conditions**

3.2.2.1.2 The influence of the MOSFET

To evaluate the contribution of the MOSFET in VDS fall time spread, refer to Figure 30. The x-axis of the plot represents a PCB with 3-phase bridge configuration of MOSFETs, 3 high-side MOSFETs on each PCB. The given VDS fall time at each x-axis value in the plot is the measured VDS fall time when all three high-side MOSFETs on a PCB are tested with a gate driver under all Test conditions. Note that the MOSFETs from three different lots are mounted on 7 PCB boards. The measured VDS fall times are almost identical for various MOSFETs mounted on PCB boards at each gate charge current setting. Hence, it can be said that MOSFETs do not have a huge influence on the spread of VDS fall time at each gate charge current when compared to the gate driver.

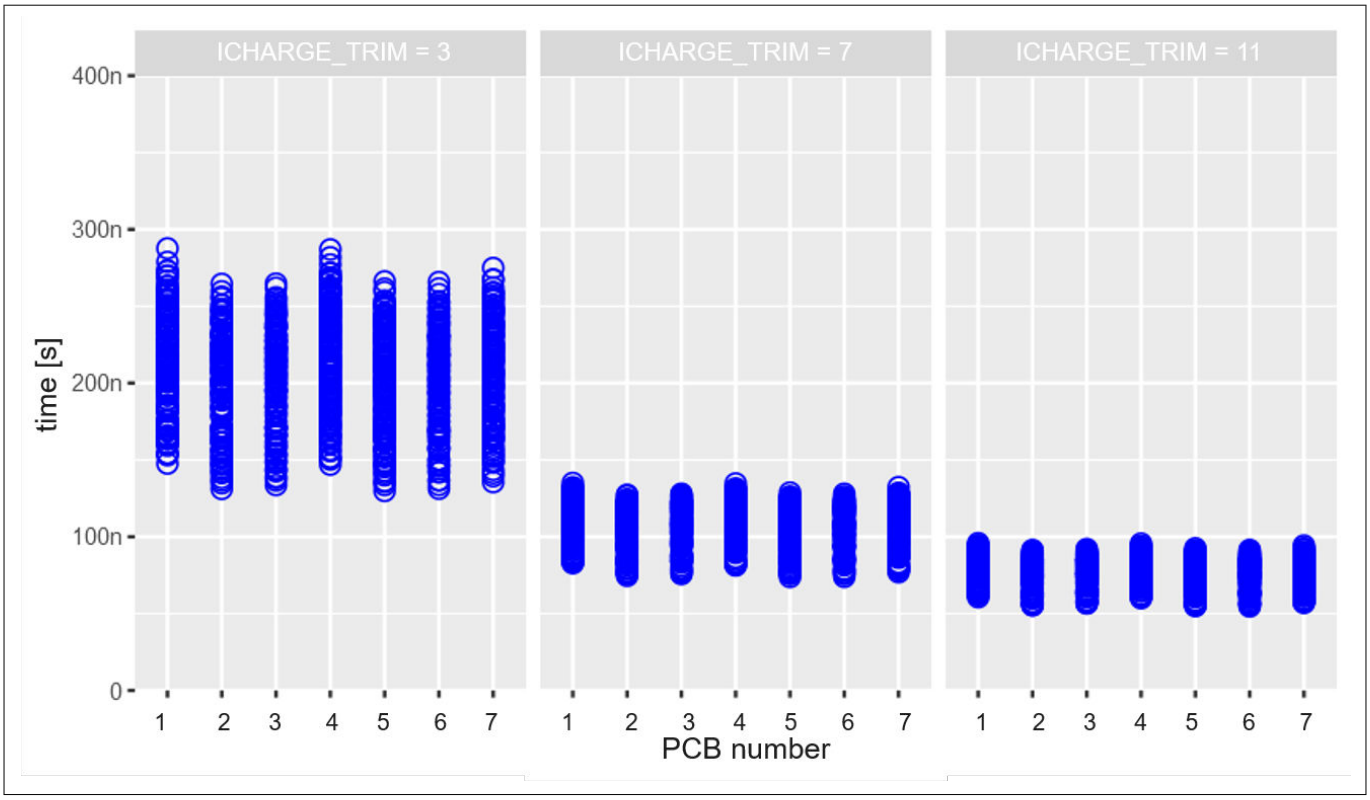

Figure 30 **The plot shows VDS fall times for high-side MOSFETs mounted on various PCB boards . It is measured when each of 3 high-side MOSFETs on a PCB board are tested with a gate driver at all operational conditions**

3.2.2.1.3 The influence of supply voltage

The figure below shows the influence of supply voltages on VDS fall times of high-side MOSFETs at different gate charge currents.. The plot in Figure 31 is divided into three sections. Each section represents a gate charge current setting. All test conditions (temperature, load current, MOSFET, gate driver) except supply voltage - remain constant during testing. The VDS fall time increases as supply voltages are increased at each gate charge current setting, as shown in the figure below. The change in VDS fall time with supply voltage is quite significant, especially at the lowest gate charge current. At medium and higher gate charge currents, the VDS fall times still vary with supply voltage but the dependency is not as significant as it is in the case of lower gate charge current . The VDS fall time is expected to change with supply voltage if gate charge current is constant.

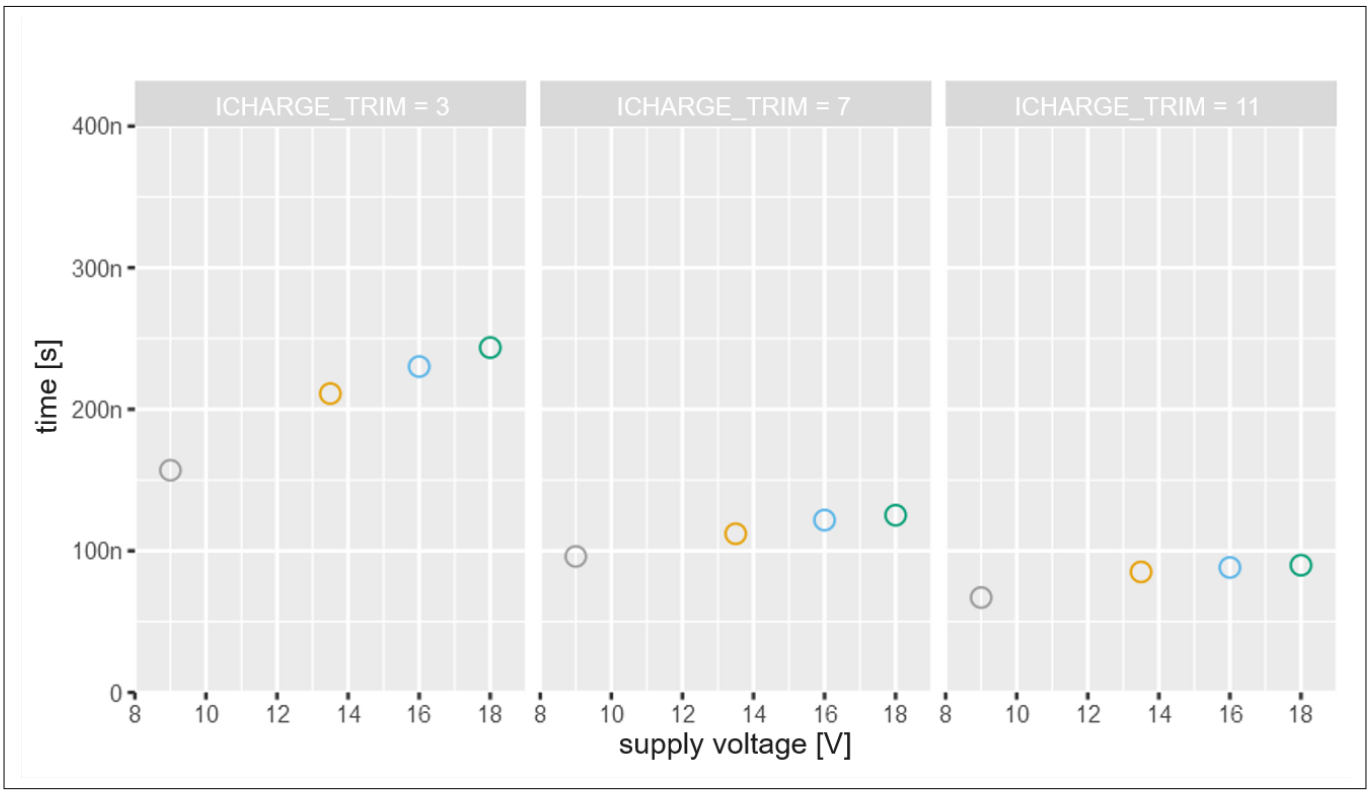

Figure 31 **VDS fall time for high-side MOSFETs. It is measured when a gate driver is tested with a MOSFET at 25°C temperature and 30 A load current**

3.2.2.1.4 The influence of temperature

To see the influence of temperature on VDS fall time, refer to Figure 32. It shows the influence of temperature on VDS fall time at different gate charge current settings. All test conditions, that is, supply voltage, load current, gate driver and MOSFET, but not temperature, remain constant during the test. The VDS fall time increases with rising temperature at all gate charge current settings. However, the rate of charge is different for each gate charge current settings. The delta between maximum and minimum VDS fall time at lower gate charge current setting is 12% of maximum VDS fall time. The difference between maximum and minimum VDS fall times reduces to 6% in the case of a medium gate charge current setting. It is 2% in the case of a higher gate charge current setting.

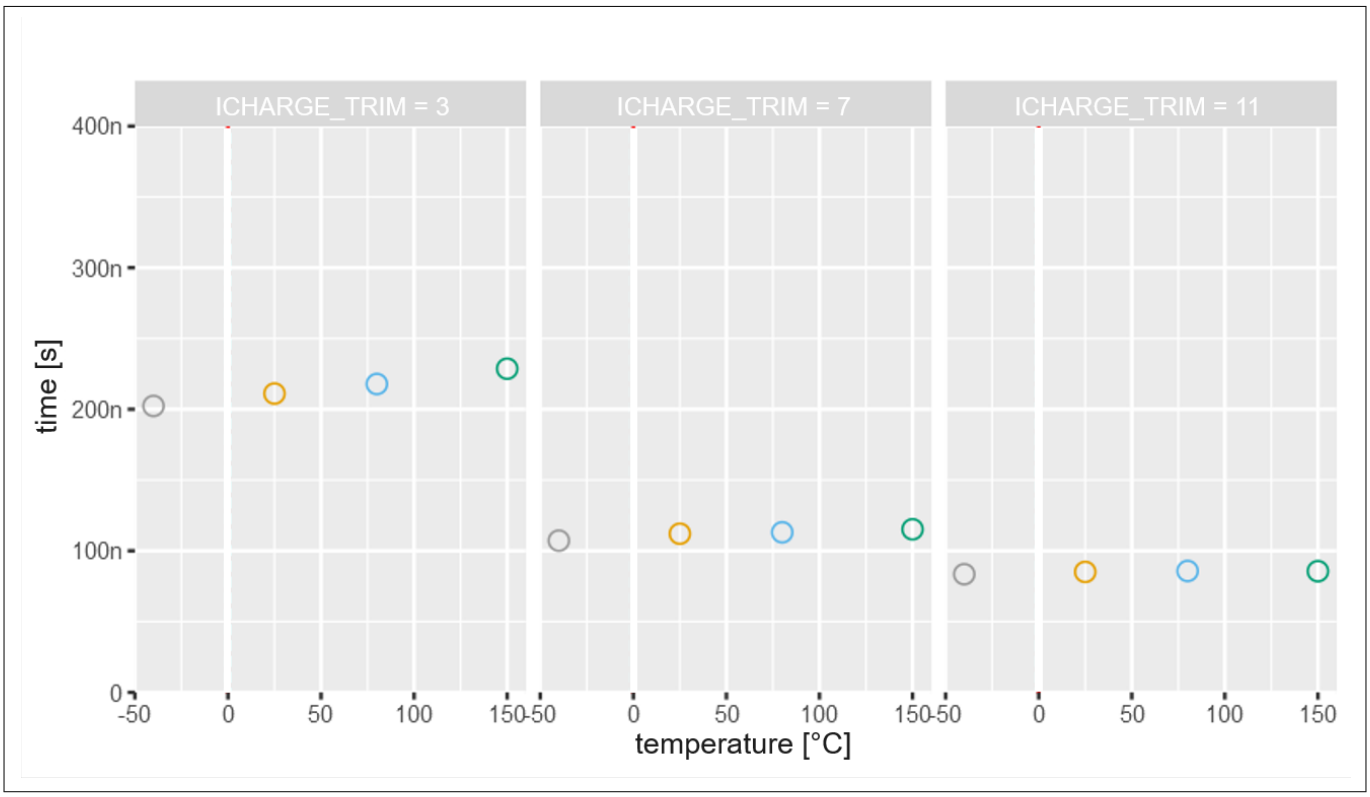

Figure 32 **VDS fall time at various temperatures at various gate charge current settings. It is measured when a gate driver is tested with a MOSFET at 13.5 V supply voltage and 30 A load current**

3.2.2.1.5 The Influence of load current

The figure below shows the dependency of VDS fall time of the high-side MOSFET on load currents. The plot is divided into three sections, each representing a charge current setting. It can be seen from the plot, that the load current has no influence on the VDS fall time at any gate charge current setting.

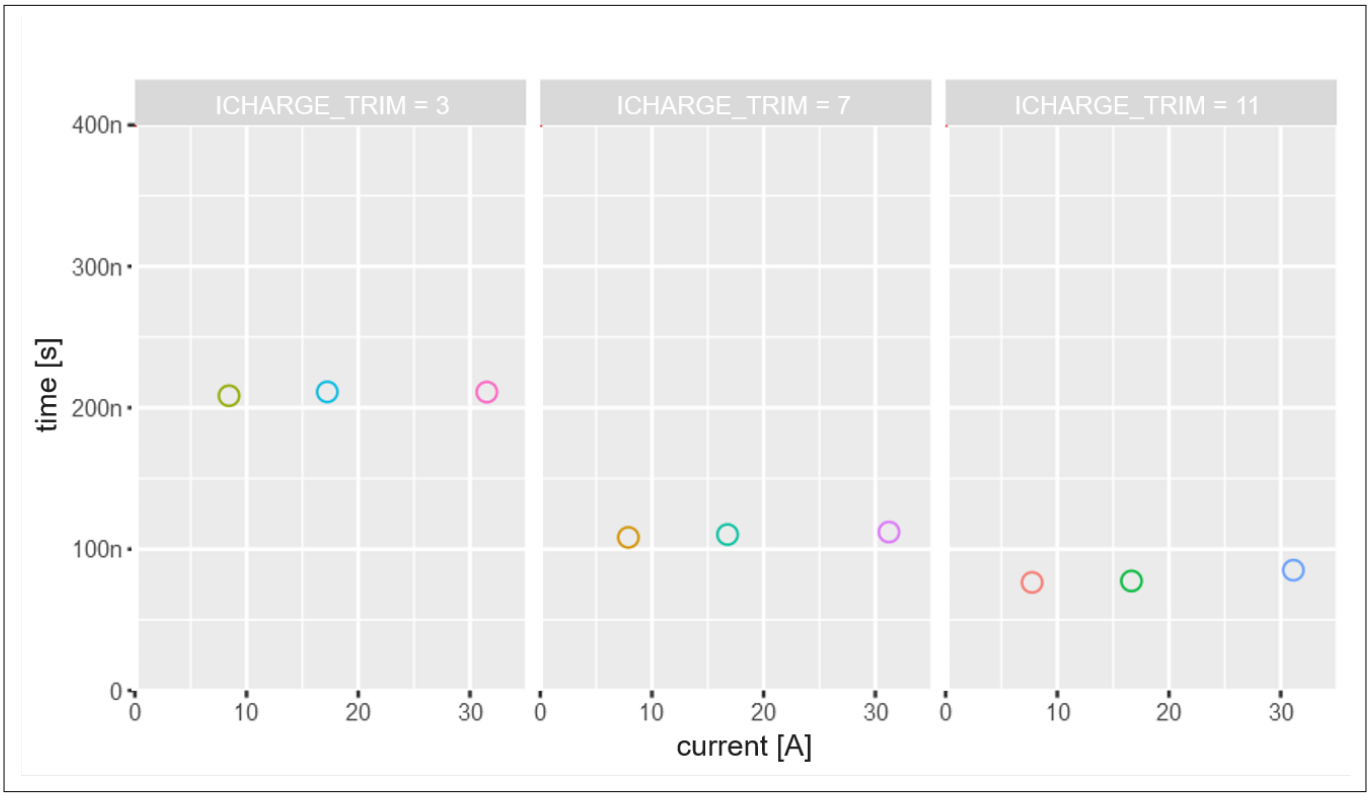

Figure 33 **The plot shows VDS fall time dependency on load current at different gate charge current settings. It is measured when a gate driver is tested with high-side MOSFET at 13.5 V supply voltage and 25°C temperature.**

3.2.2.2 Fall times for low-side MOSFETs

The plot in figure below shows VDS fall times for low-side MOSFETs at different gate charge current settings. The VDS fall times are measured when 3 gate driver samples are tested under Test conditions with all low-side MOSFETs mounted on 7 PCBs in a 3-phase bridge configuration. Consistent with observation in the case of high-side the MOSFETs, the spread in VDS fall time is higher at lower gate charge current settings and it decreases with increasing gate charge current setting. The influence of different factors on VDS fall times of low-side MOSFETs is discussed in the following sections.

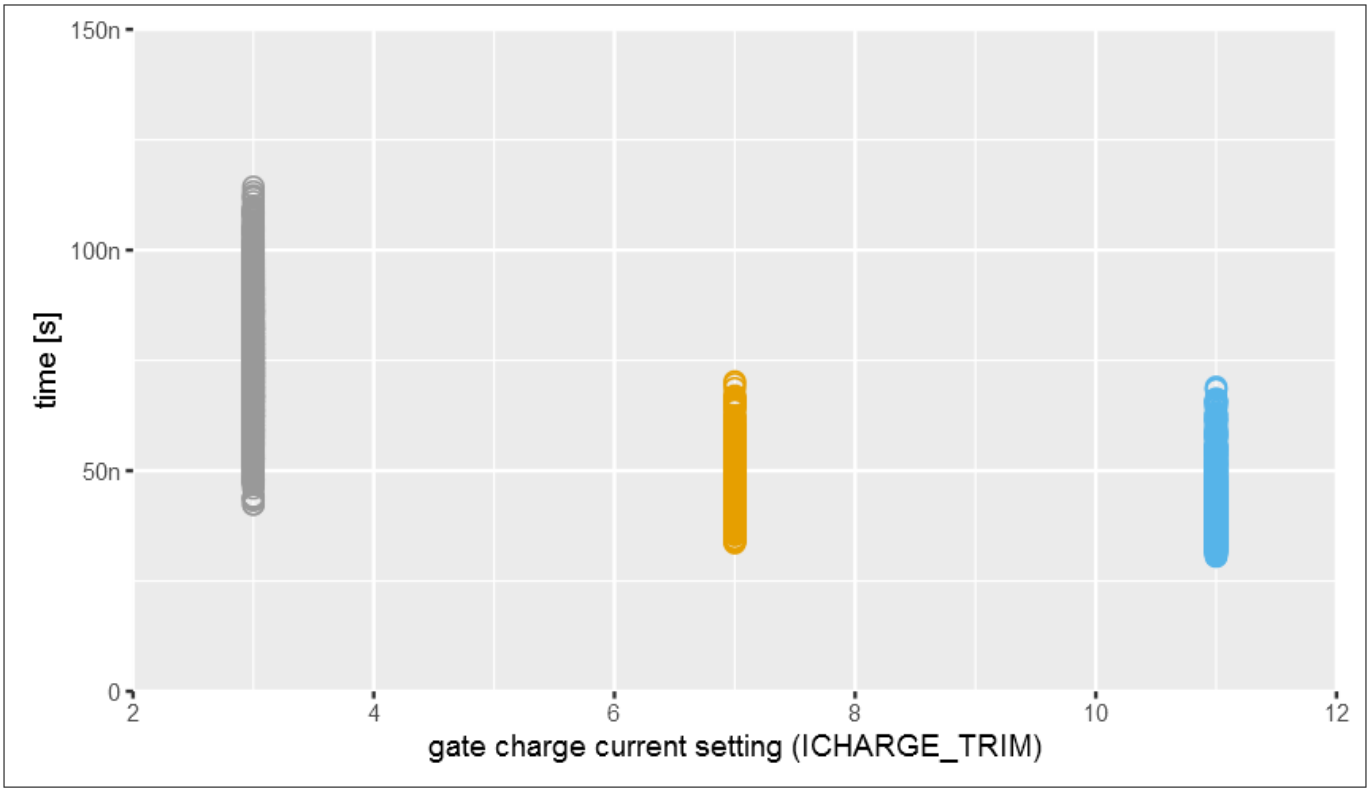

Figure 34 **The plot shows measured VDS fall time of low-side MOFSETs at different gate charge current settings. It is measured when 3 gate driver samples are tested with all low-side MOSFETs under all test conditions**

3.2.2.2.1 The influence of the gate driver

The plot in figure below shows VDS fall time for low-side MOSFETs. It is measured when all gate driver samples are tested under all Test conditions with all 3 low-side MOSFETs in a 3-phase bridge. It can be seen from the figure that the measured VDS fall times are different for each driver sample at lower gate charge current settings, however, it does not seem to be the case for medium and higher gate charge current settings. This behavior is different compared to that of high-side MOSFETs given in the sectionThe influence of the gate driver. The reason for this difference is the parasitic inductance of the PCB. The amplitude of the voltage spike generated by parasitic inductance increases as gate charge current is increased. As a result, measured VDS fall time is higher than actual VDS fall time. The phenomenon is explained in detail in Low-side MOSFET VDS fall time measurement increase.

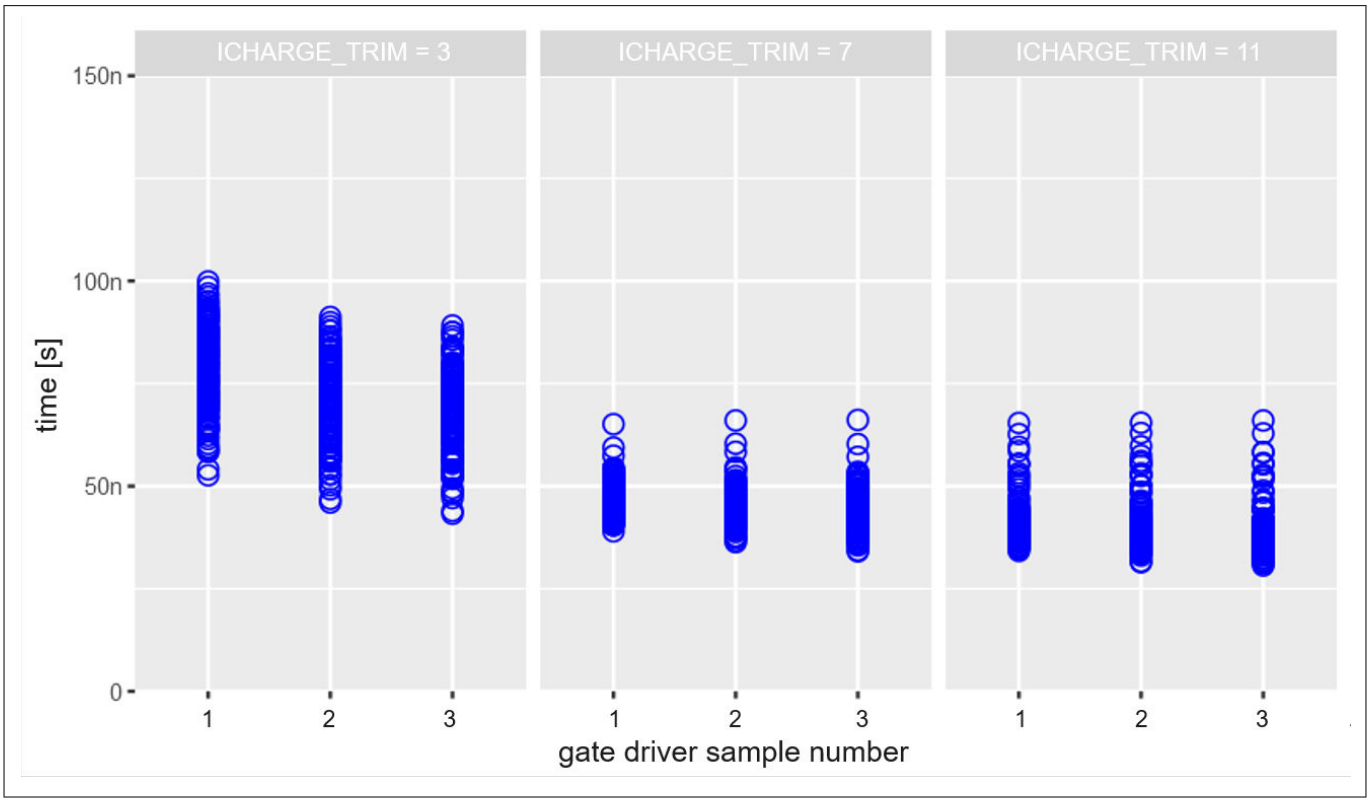

Figure 35 **The plot shows VDS fall times for low-side MOSFETs at different gate charge current settings. It is measured when each gate driver sample is tested with 3 low-side MOSFETs under all test conditions**

3.2.2.2.2 The influence of the MOSFET

To see the influence of MOSFETs on the VDS fall time refer to the plot in the figure below. The VDS fall time is measured when a gate driver sample is tested under all Test conditions with all low-side MOSFETs mounted on 7 PCBs in a 3-phase bridge configuration. The x-axis of the plot represents 3 low-side MOSFETs mounted on a PCB. At lower gate charge current, the measured VDS fall times are slightly different for each PCB, however, the difference is insignificant considering its magnitude. The effect of parasitic inductance on PCB is dominant at medium and higher gate charge current. As a result, measured VDS fall times are higher than actual VDS fall times. This phenomenon is explained in Low-side MOSFET VDS fall time measurement increase. If outlier data points are ignored at the medium gate charge current setting, the VDS fall times look identical for all low-side MOSFETs on each PCB. The same is true for VDS fall times at high gate charge current settings.

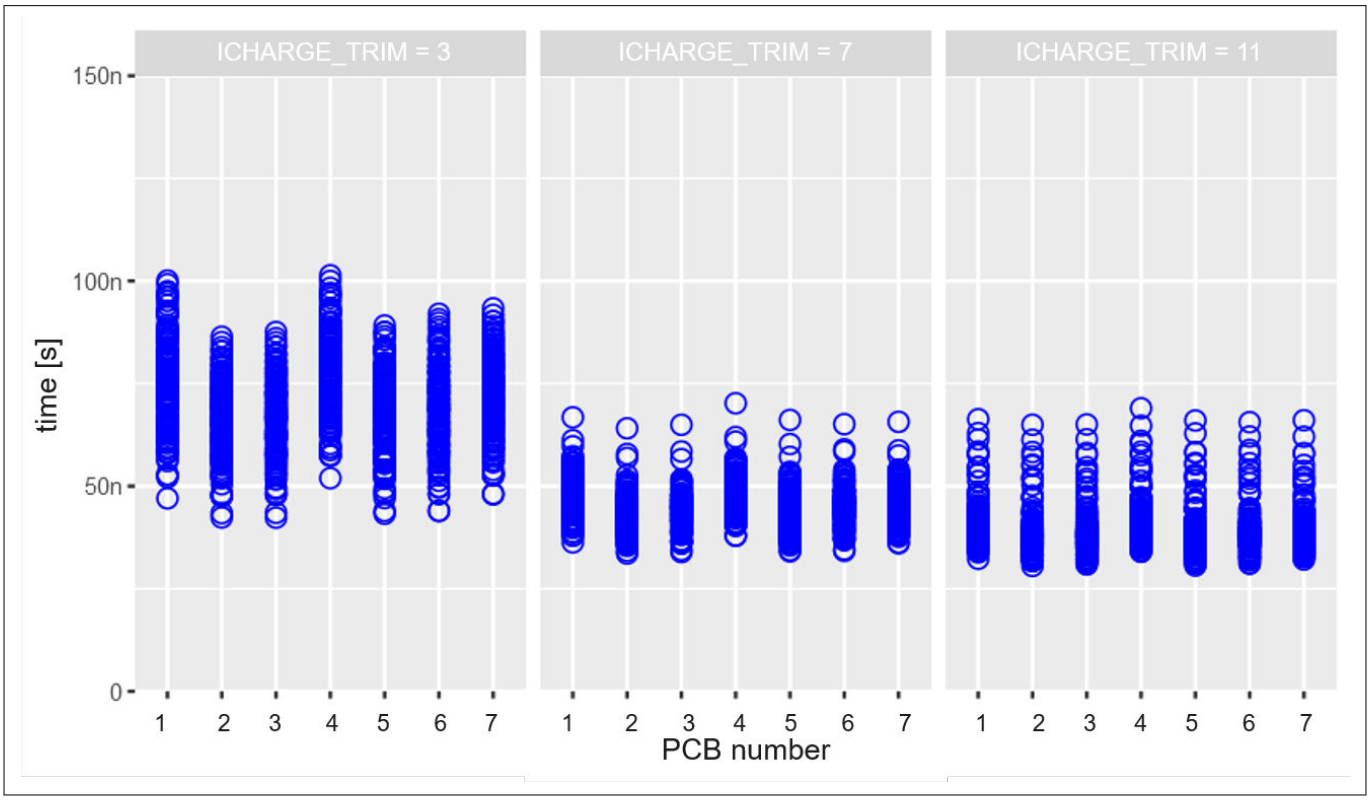

Figure 36 **The plot shows VDS fall time at different gate charge current settings. It is measured when a gate driver is tested with all test conditions with all low -side MOSFETs mounted on each PCB.**

3.2.2.2.3 The influence of supply voltage

The plot in Figure 37 shows the influence of the supply voltage on VDS fall times of low-side MOSFETs. The plot is divided into three sections, one section for each gate charge current setting. All test conditions, that is temperature, load current, MOSFET, gate driver, but not supply voltage, remained constant during the test. Consistent with results of high-side MOSFETs, the VDS fall time for low-side MOSFETs increases with increasing supply voltage at lower gate charge current settings. However, this behavior does not hold at medium and high gate charge current settings, as is evident from the plot below. The root cause of this difference is parasitic inductance at source of low-side MOSFETs. It is explained in detail in Low-side MOSFET VDS fall time measurement increase. Nevertheless, a point worth noting here is that the parasitic inductance of the characterization board starts to dominate as switching times shorten.

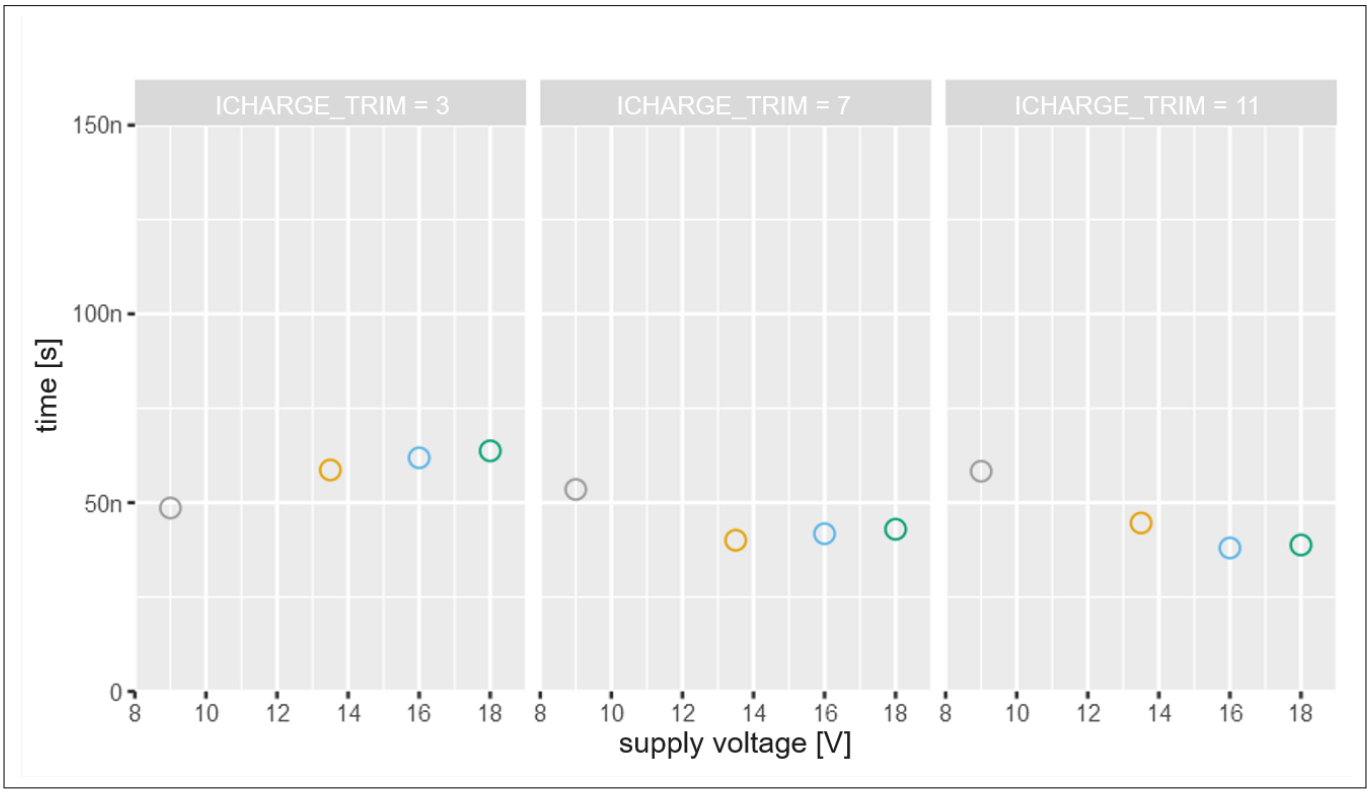

Figure 37 **The plot shows VDS fall time for low-side MOSFETs. It is measured with a gate driver sample and is tested with a MOSFET at 25°C temperature and 30 A load current**

3.2.2.2.4 The influence of temperature

The plot in Figure 38 shows the influence of temperature on the VDS rise time for low-side MOSFETs at different gate charge current settings. The plot is divided into three sections, one for each gate charge current setting. The VDS fall time value is measured when all test conditions, (supply voltage, load current, gate driver, and a MOSFET), except temperature are kept constant during the test. Similar to VDS fall time for high-side MOSFETs, VDS fall time for the low-side MOSFET increases with increasing temperature. The delta between minimum and maximum VDS fall time is nearly 20% of the maximum VDS fall time at each gate charge current setting.

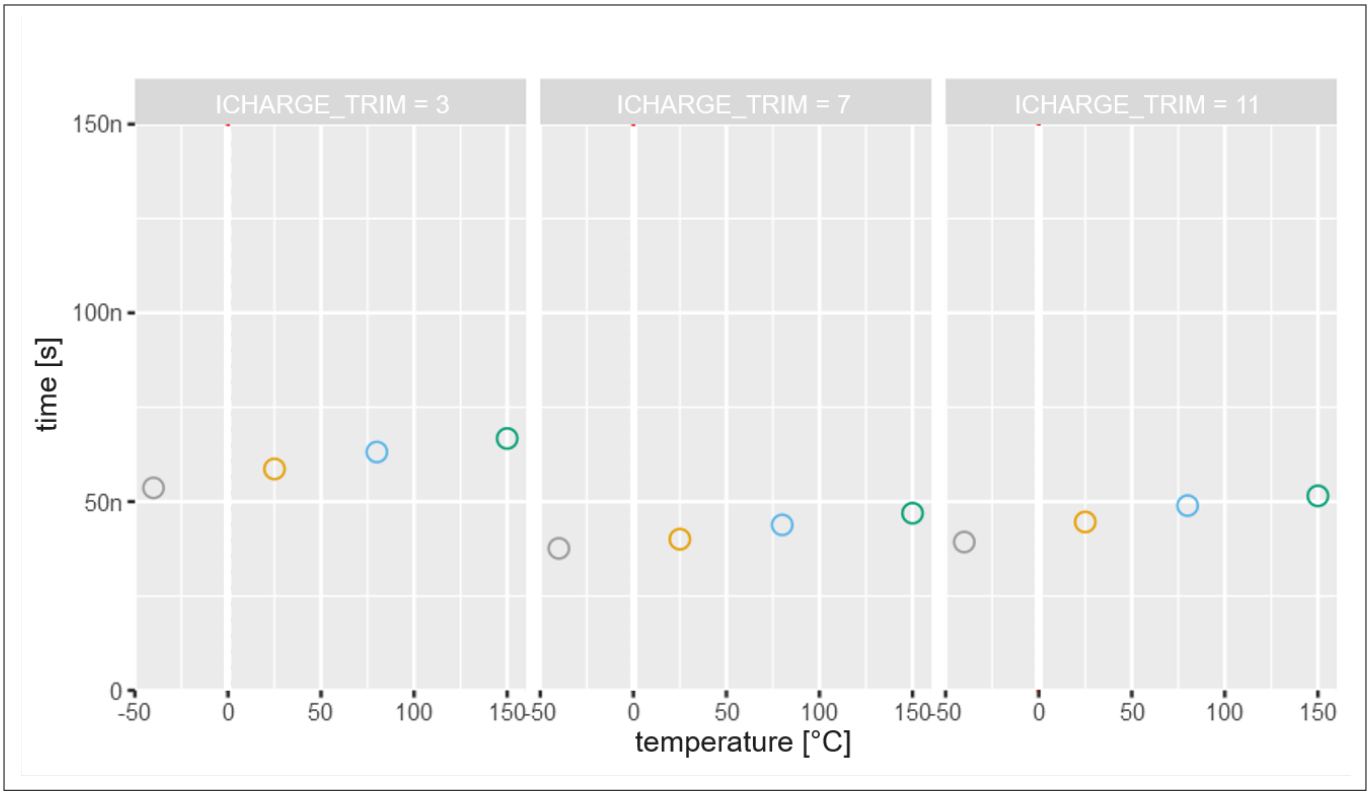

Figure 38 **The plot shows the influence of temperature on the VDS fall time for low-side MOFSETs. It is measured with a gate driver sample that is tested with a MOSFET at 13 V supply voltage and 30 A load current.**

3.2.2.2.5 The influence of the load current

The plot in the figure below shows the influence of the load current on the VDS fall time for low-side MOSFETs at different gate charge current settings. Each section in the plot represents a gate charge current setting. The VDS fall times given in the plot are measured when all conditions (supply voltage, temperature, gate driver, MOSFET) except load current, remain constant during the test. At medium and high gate charge current settings, it can be seen that the load current does not have significant influence on the VDS fall time. However, the VDS fall time changes slightly with load current at the lower gate charge current setting. The difference between maximum and minimum VDS fall time is 18% of maximum VDS fall time at the lower gate charge current setting. There is no change in VDS fall times with load current at the medium gate charge current setting. One point worth mentioning here is that the effects of PCB parasitic inductance become dominant at higher gate charge current settings because of faster switching. The increase in VDS fall time at 30 A current and higher gate charge current setting is a result of two distinctive slopes on the VDS waveform caused by parasitic inductance on PCB. These two slopes falls into the VDS fall time measurement window. This problem is explained in detail in Low-side MOSFET VDS fall time measurement increase.

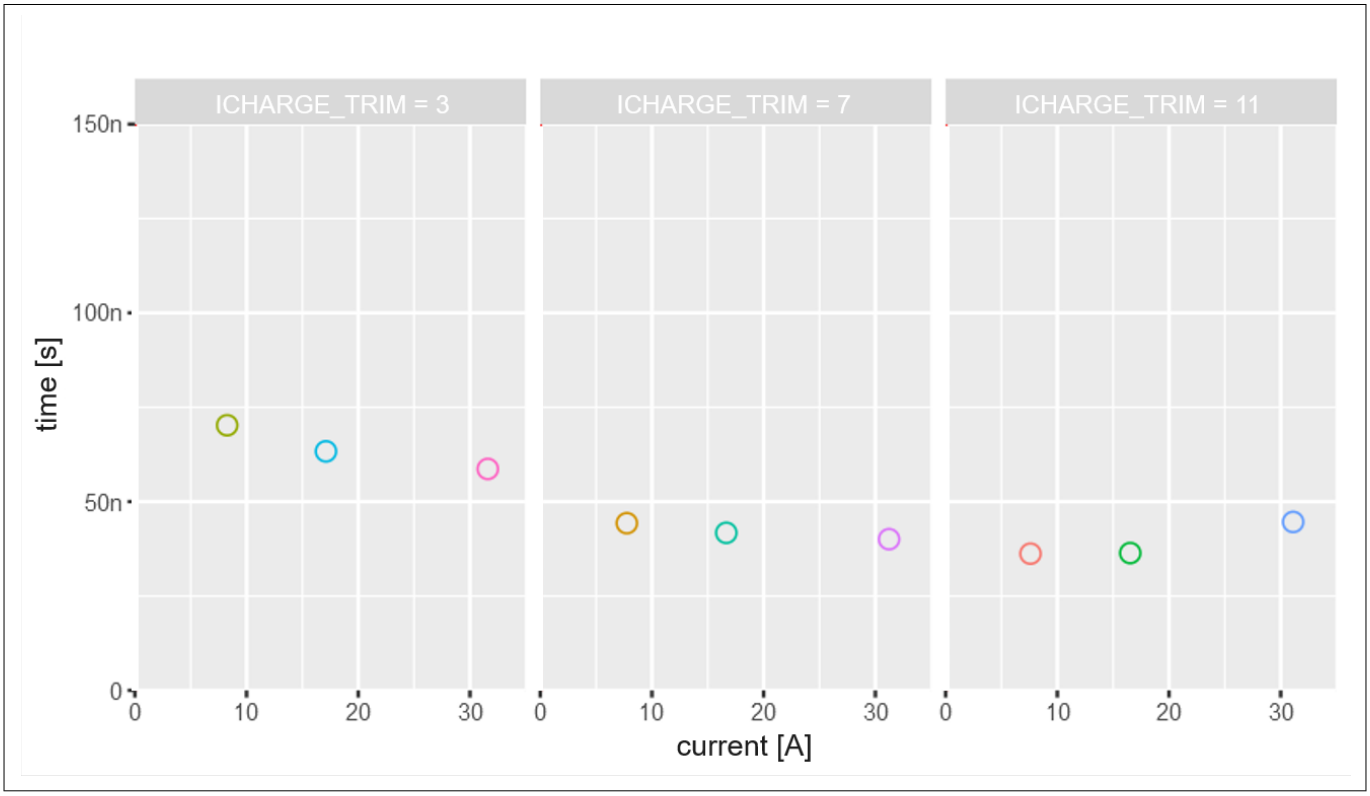

Figure 39 **The plot shows the influence of load current on the VDS fall time for low-side MOSFETs. It is measured when a gate driver is tested with a MOSFET at 13.5 V supply and 25°C temperature.**

3.2.3 VDS rise time

The range of VDS rise time at different gate settings and across different test condition and factors influencing it is given in this section.

The VDS rise time is the time drain-to-source voltage takes to go from 20% to 80% of its nominal value during turn OFF of the MOSFET as can be seen in Figure 40.

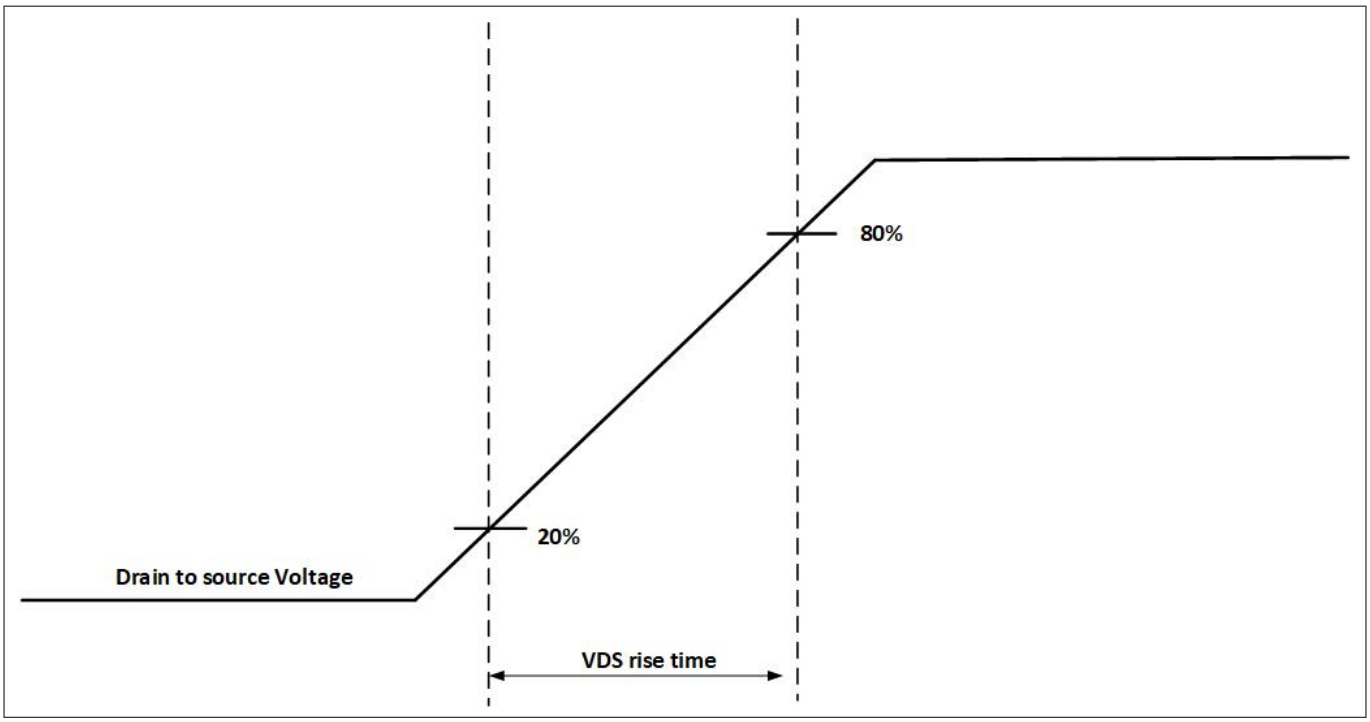

Figure 40 VDS rise time

3.2.3.1 High-side MOSFET

The plot in Figure 41 shows measured VDS rise time when 3 gate driver samples are tested under all Test conditions with all of the high-side MOSFETs . The plot below gives an expected range of VDS rise time at different gate discharge current settings. The influence of different test conditions on VDS rise time of high-side MOFSETs is given in the following sections.

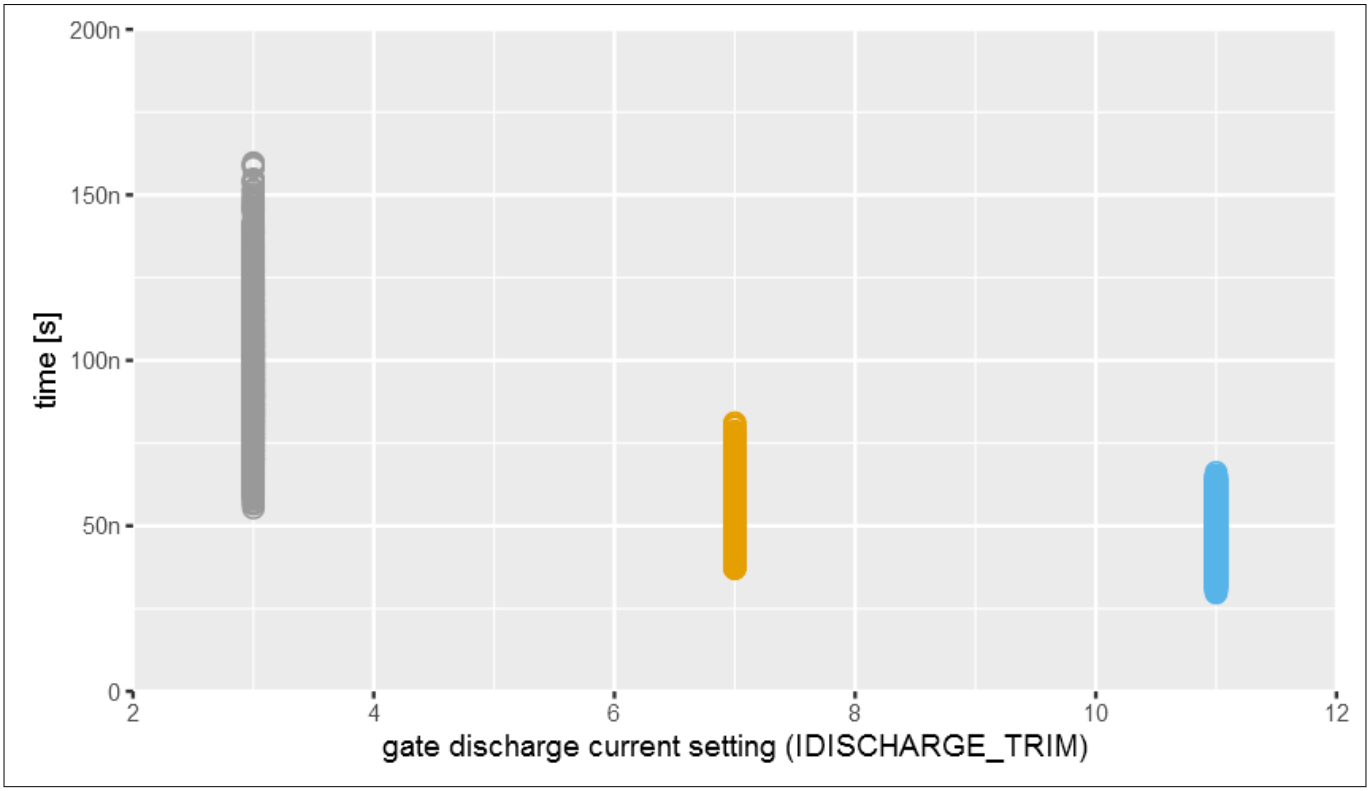

Figure 41 **The plot shows measured VDS rise time for high-side MOFSET at different gate discharge current settings. It is measured when 3 gate driver samples are tested with all high-side MOSFETs under all test conditions**

3.2.3.1.1 The influence of the gate driver

The plot in Figure 42 shows the measured VDS rise time at different gate discharge current settings. It is measured when 3 gate driver samples are tested with all high-side MOSFETs in 3-phase bridges under all Test conditions. Different gate driver samples result in different VDS rise times especially at lower gate discharge current settings. At low gate charge current setting, the longest VDS rise time of the slowest sample is 23% above the longest VDS rise time of the fastest sample. The gate driver's influence on VDS rise time reduces at medium gate discharge current settings and it is negligible at higher gate discharge current settings.

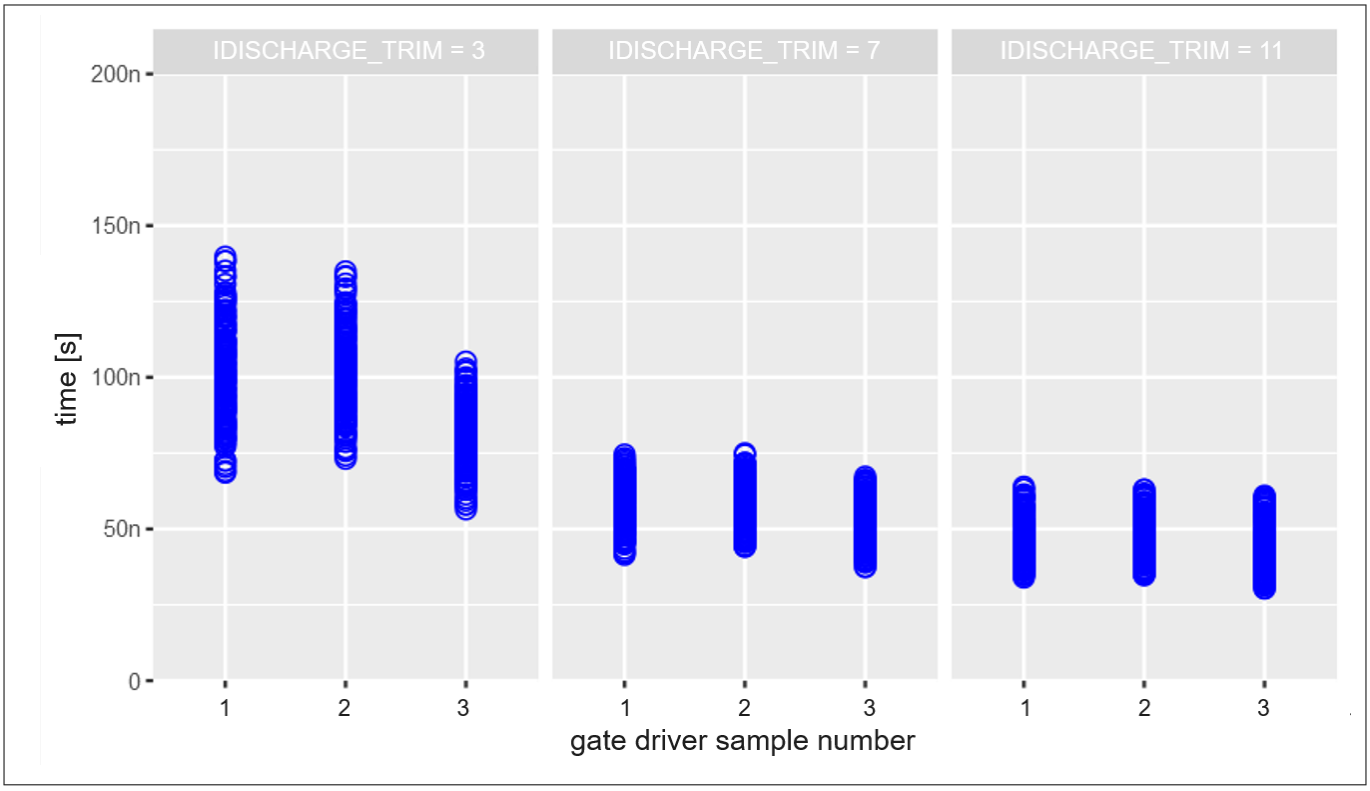

Figure 42 **The plot shows VDS rise time for high-side MOSFETs at different gate discharge current settings. It is measured when different gate driver samples are tested with 3 high-side MOSFET at all test conditions**

3.2.3.1.2 The influence of the MOSFET

To see the influence of high-side MOSFETs on VDS rise time, refer to Figure 43. The plot shows measured VDS rise time when a gate driver is tested under all Test conditions with all high-side MOSFETs mounted on 7 PCBs in a 3-phase bridge configuration. Note that the MOSFETs from three different lots are mounted on 7 PCBs. The spread of measured VDS rise time for all high-side MOSFETs looks almost identical at medium and higher gate discharge current settings. However, there is a slight difference at lower gate discharge current settings. At low gate charge current setting, the longest VDS rise time of the slowest sample is 13% above the longest VDS rise time of the fastest sample. Based on the measured results, the overall influence of MOSFETs on VDS rise time is negligible compared to that of the gate driver.

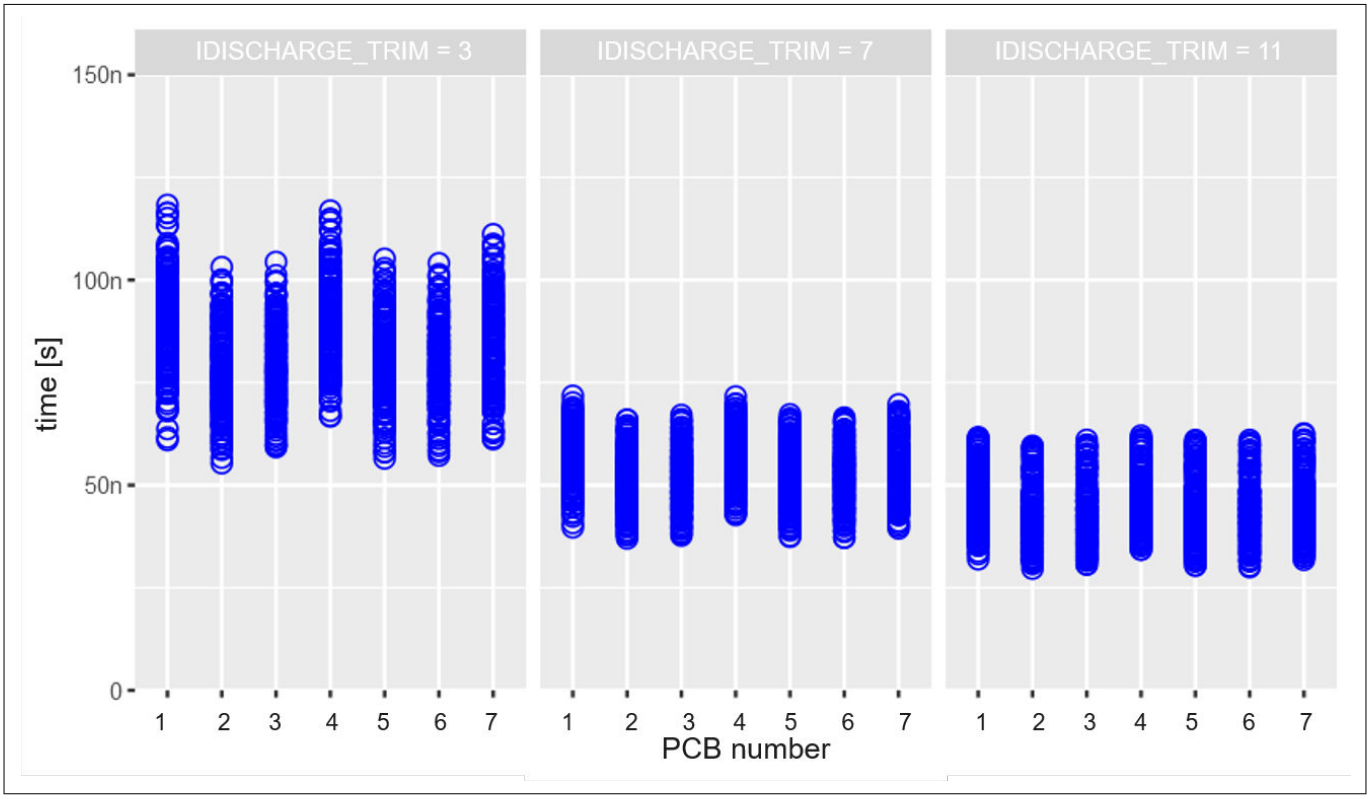

Figure 43 **The plot shows VDS rise time at different gate discharge current settings. It is measured when a gate driver sample is tested with all high-side MOSFETs mounted on various PCBs in a 3-phase bridge configuration.**

3.2.3.1.3 The influence of supply voltage

The plot in Figure 44 shows VDS rise times at different supply voltages. The plot is divided into three sections, one section for a gate discharge current setting. All test conditions (temperature, load current, MOSFET, gate driver) except supply voltage remained constant during the test. The VDS rise time increases with increasing supply voltages. The difference between minimum and maximum VDS fall time is 20 percent of the maximum value at lower and medium gate discharge. It is 23 percent at higher gate discharge current settings. The VDS rise is expected to change with supply voltage when gate discharge current is kept constant.

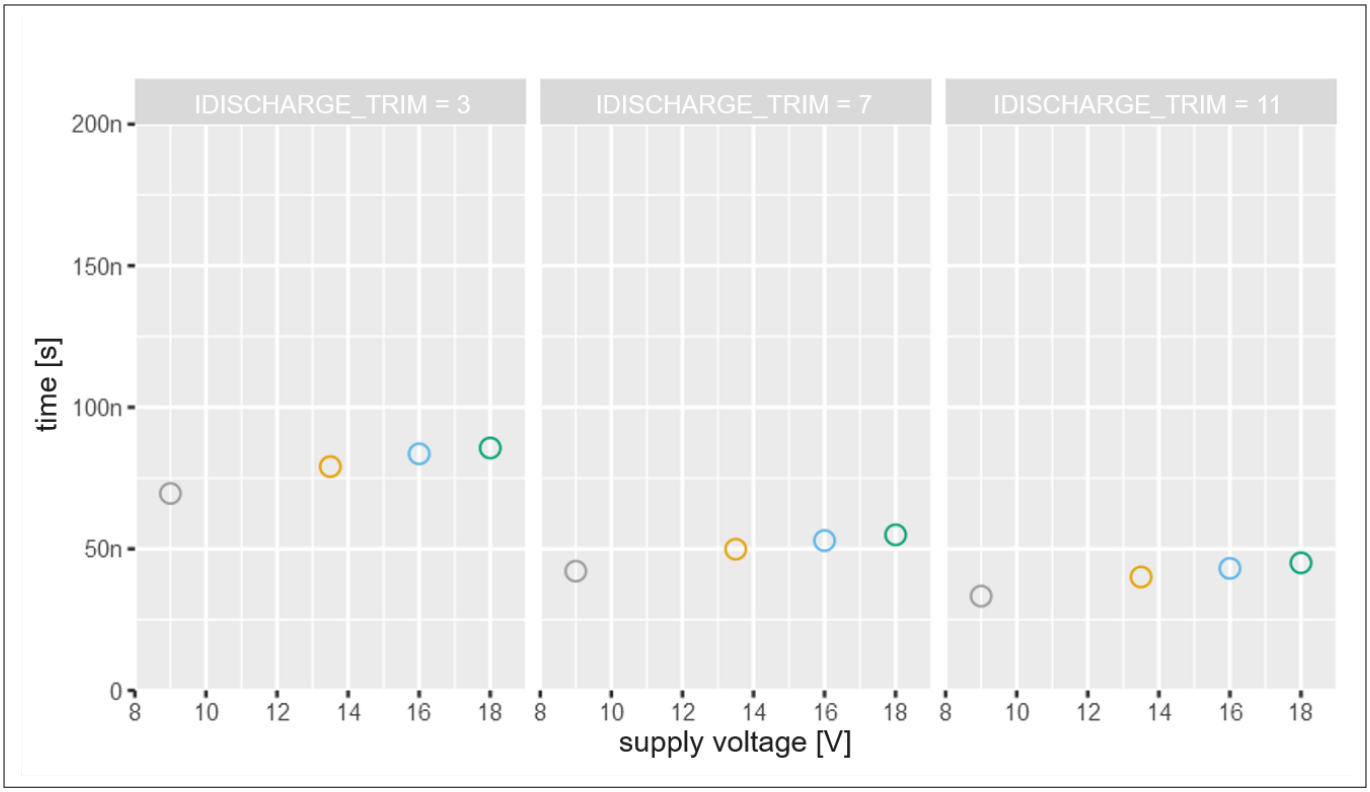

Figure 44 **The plot shows VDS rise time of high-side MOSFET. It is measured with a gate driver sample and is tested with a MOSFET at 25°C temperature and 30 A.**

3.2.3.1.4 The influence of temperature

The plot in Figure 45 shows VDS rise time of high-side MOSFETs at different temperatures. The plot is divided into three sections, one for each gate discharge current setting. The VDS rise time is measured when a gate driver sample is tested with a high-side MOSFET. All test conditions (supply voltage, load current, MOSFET, gate driver), except temperature remained constant during the test. To summarize the test result, the VDS rise time increases with rising temperature. The difference between minimum and maximum VDS rise time is 25 percent of maximum VDS rise time at lower gate discharge current settings. At medium gate discharge, the difference between maximum and minimum VDS rise time is 10 percent of maximum VDS rise time. At higher gate discharge current settings, it is 15 percent.

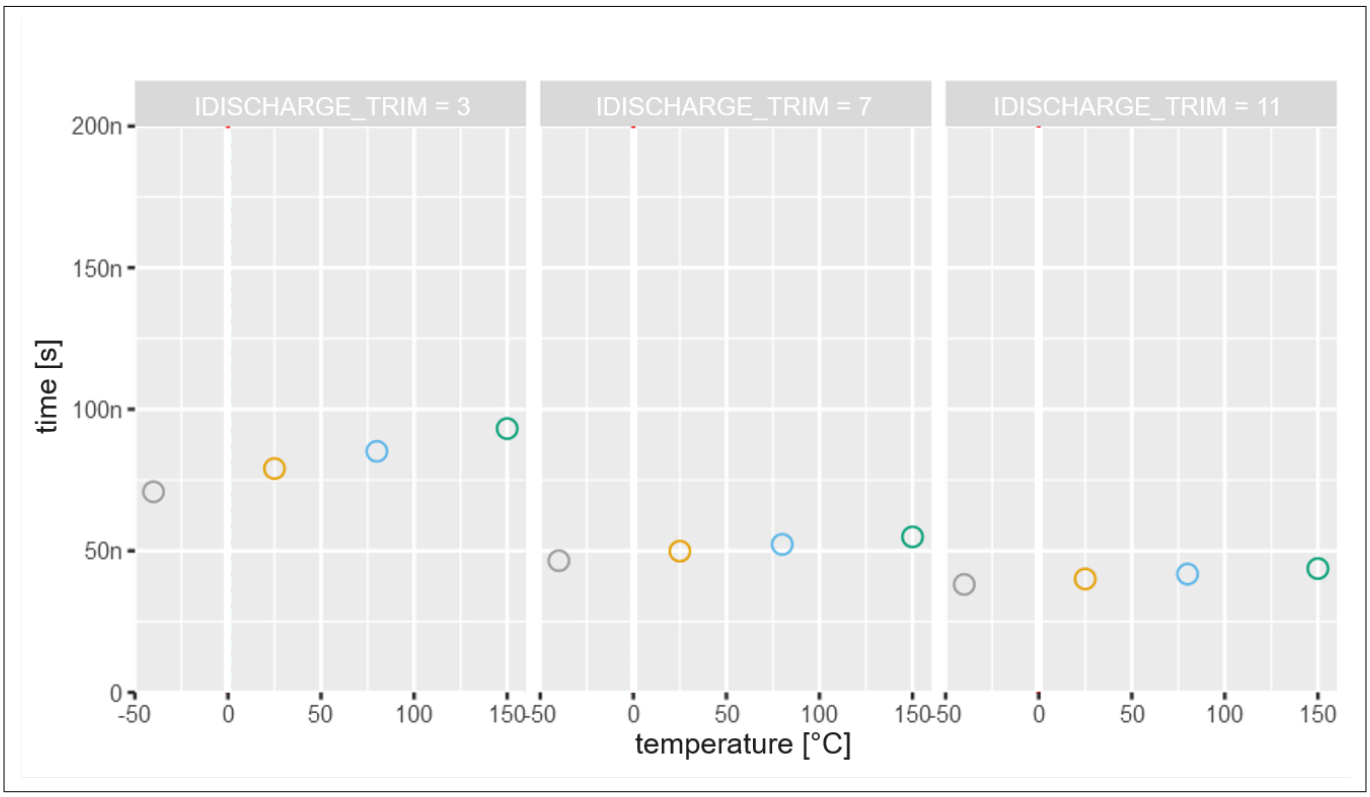

Figure 45 **The plot shows VDS rise time for high-side MOSFETs. It is measured with a gate driver sample and is tested with a MOSFET at 13.5 V supply voltage and 30 A load current**

3.2.3.1.5 The influence of load current

The plot in Figure 46 shows VDS rise time of high-side MOFSETs at different load currents. The plot is divided into three sections, one section for each gate discharge current setting. These VDS fall times are measured when all other parameters (supply voltage, temperature, driver and MOSFET) except load current remain constant during testing. The load current does not have significant influence of VDS rise time. The difference between minimum and maximum VDS rise time values is within 10% of maximum value at lower and medium gate discharge current settings. At higher gate discharge current settings it is 18%.

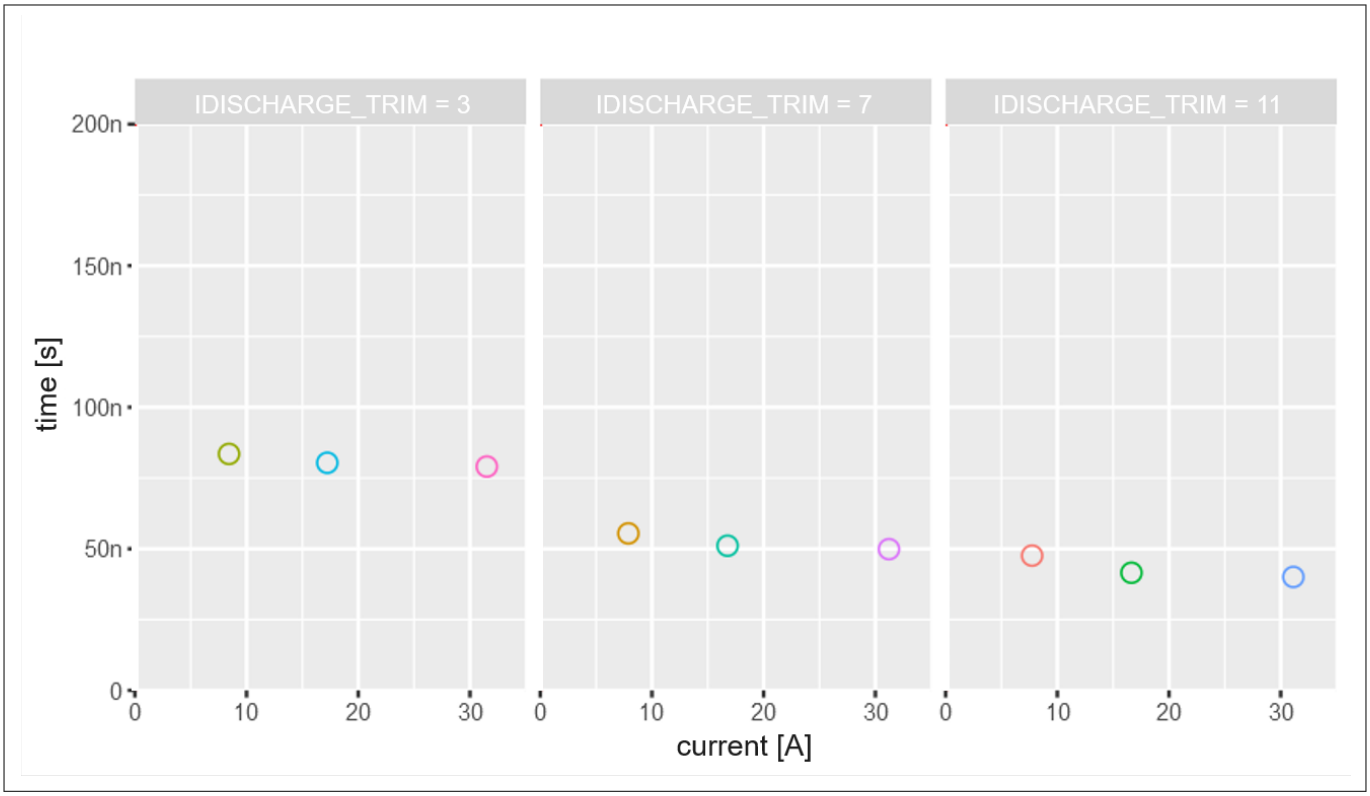

Figure 46 **The figure shows the influence of load current on VDS rise of high-side MOSFET. It is measured when a gate driver is tested with a MOSFET at 13.5 V and 25°C temperature**

3.2.3.2 Low-side MOSFET

The plot in Figure 47 shows VDS rise time of low-side MOFSETs at different gate discharge current setting. The VDS rise time is measured when 2 gate driver samples are tested with low-side MOSFETs under all Test conditions. Therefore, each point in the plot below shows the VDS rise time measured at one of all possible combinations of test conditions. The influence of different test conditions on VDS rise time is given in the following sections.

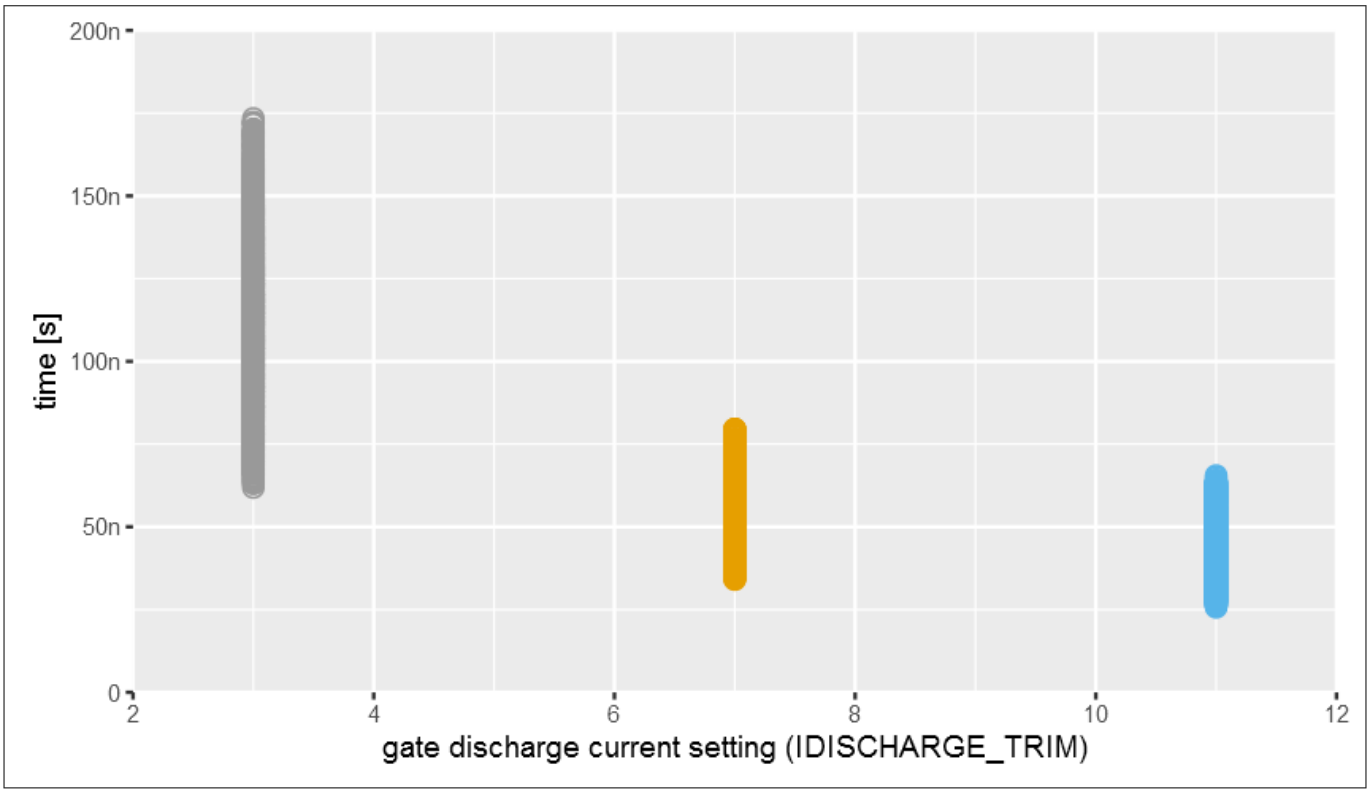

Figure 47 **The plot shows measured VDS rise time for low-side MOFSETs at different gate discharge current settings. 3 gate driver samples were tested with all MOSFETs under all test conditions**

3.2.3.2.1 The influence of the gate driver

The plot below shows the VDS rise time of low-side MOFSETs at different gate discharge current settings. It is measured when 3 gate driver samples are tested with all low-side MOSFETs in a 3-phase bridge under all Test conditions. Note that the MOSFETs from two different lots are mounted on 5 PCBs in a 3-phase bridge configuration and one of the PCBs is used during this test. It can be seen from the plot that each gate driver sample results in different VDS rise times especially at lower gate discharge current settings. At low gate charge current setting, the longest VDS rise time of the slowest sample is 25% above the longest VDS rise time of the fastest sample. The VDS rise times of all 3 samples are slightly different at medium gate discharge current setting. However, the VDS rise times are almost identical for each sample at highest gate discharge current setting. Therefore the gate driver contributes significantly to the variation of the VDS rise time at lower gate discharge current settings but it decreases as the gate discharge current is increased.

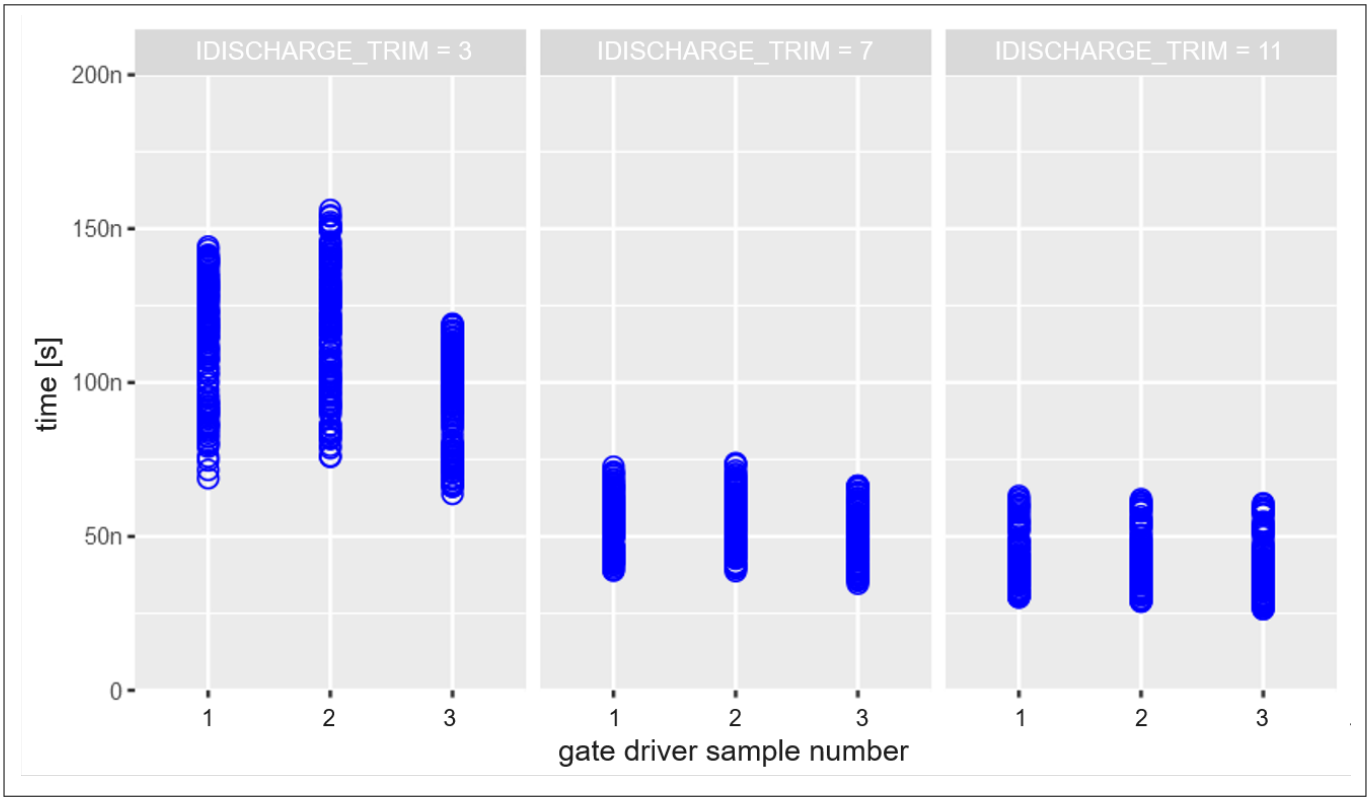

Figure 48 **The plot shows the VDS rise time for low-side MOSFETs at different gate discharge current settings. It is measured when 3 gate driver samples and tested with all low-side MOSFETs in a 3-phase bridge.**

3.2.3.2.2 The influence of the MOSFET

The plot in Figure 36 shows the VDS rise time for low-side MOSFETs at different gate discharge current settings. The VDS rise times are measured when a gate driver sample is tested under all Test conditions with all low-side MOFSETs mounted on 7 PCBs in a 3-phase bridge configuration. Note that the MOSFETs from three different lots are mounted on 7 PCBs. The spread of VDS rise time at all gate discharge current settings looks almost identical for various low-side MOSFETs. There is a slight difference in measured VDS rise time at lower gate discharge current settings but the magnitude of the difference is insignificant. Therefore, the MOSFET's contribution to the variation in VDS rise time is negligible in comparison with that of the gate drivers.

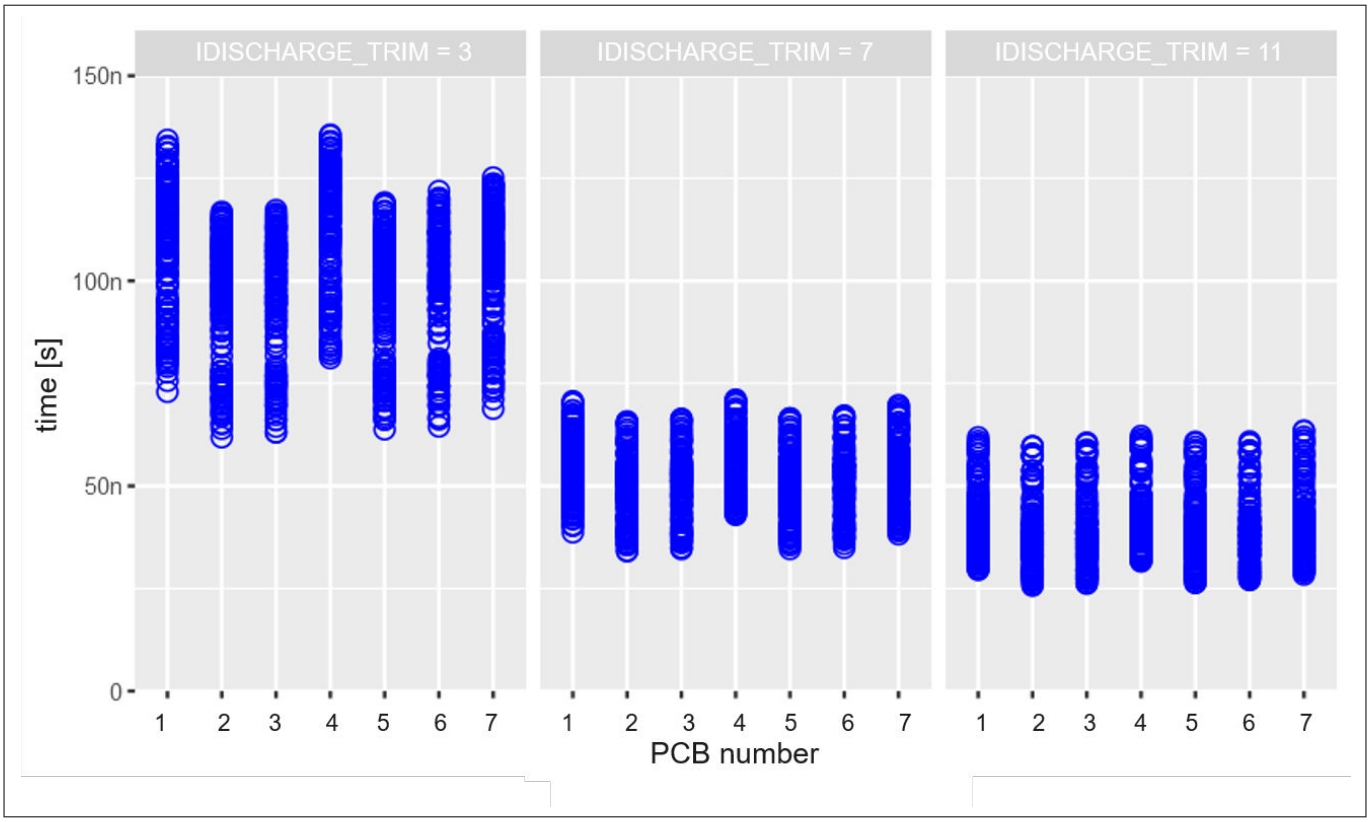

Figure 49 **The plot shows VDS rise time at different gate discharge current settings. It is measured when a gate driver is tested with all low-side MOSFETs mounted on 7 different PCBs in a 3-phase bridge configuration.**

3.2.3.2.3 The influence of the supply voltage

The plot in the figure below shows the VDS rise time at different supply voltages and gate discharge current settings. The plot is divided into three sections, one for each gate discharge current setting. The VDS rise time is measured when a gate driver sample is tested with a low-side MOSFET at constant temperature and load current. It can be seen from the plot that the VDS rise time increases with increasing supply voltage. The increase of VDS rise time with supply voltage is expected at a constant gate discharge current because the slope of the VDS fall depends on the gate discharge current setting.

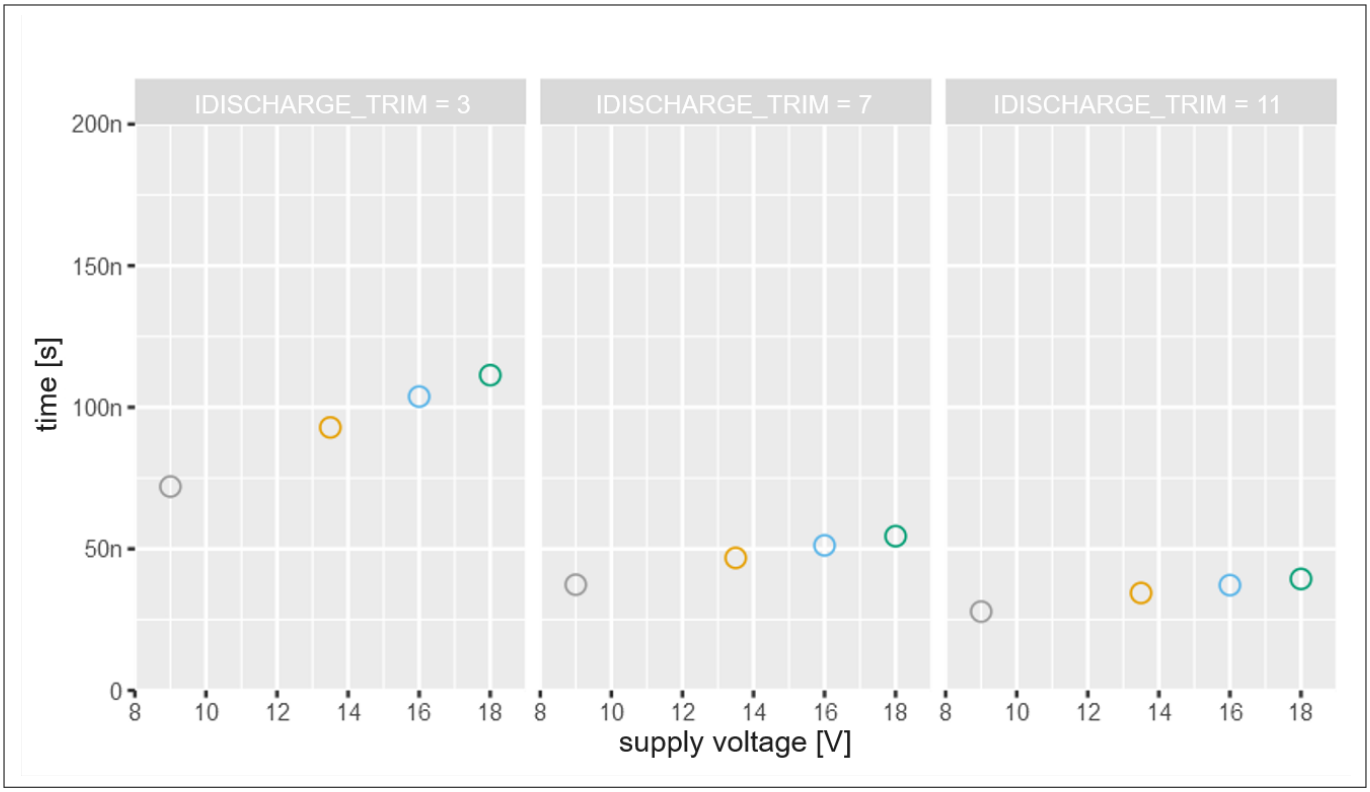

Figure 50 **The plot shows the influence of supply voltage on VDS rise time of a low-side MOSFET. It is measured when a gate driver sample is tested with a MOSFET at 25°C temperature and 30 A current.**

3.2.3.2.4 The influence of temperature

The plot in figure below shows the VDS rise time at different temperatures and gate discharge current settings. The plot is divided into three sections, one for each gate discharge current setting. It contains VDS rise time values measured when all test conditions (supply voltage, load current, gate driver and MOSFET), except temperature remain constant during the test. The VDS rise time changes with temperature. However, the change is insignificant. The difference between minimum and maximum value is 13 percent of maximum value at lower gate discharge current settings. This difference reduces to 6 percent and 3 percent at medium and higher gate discharge current settings respectively.

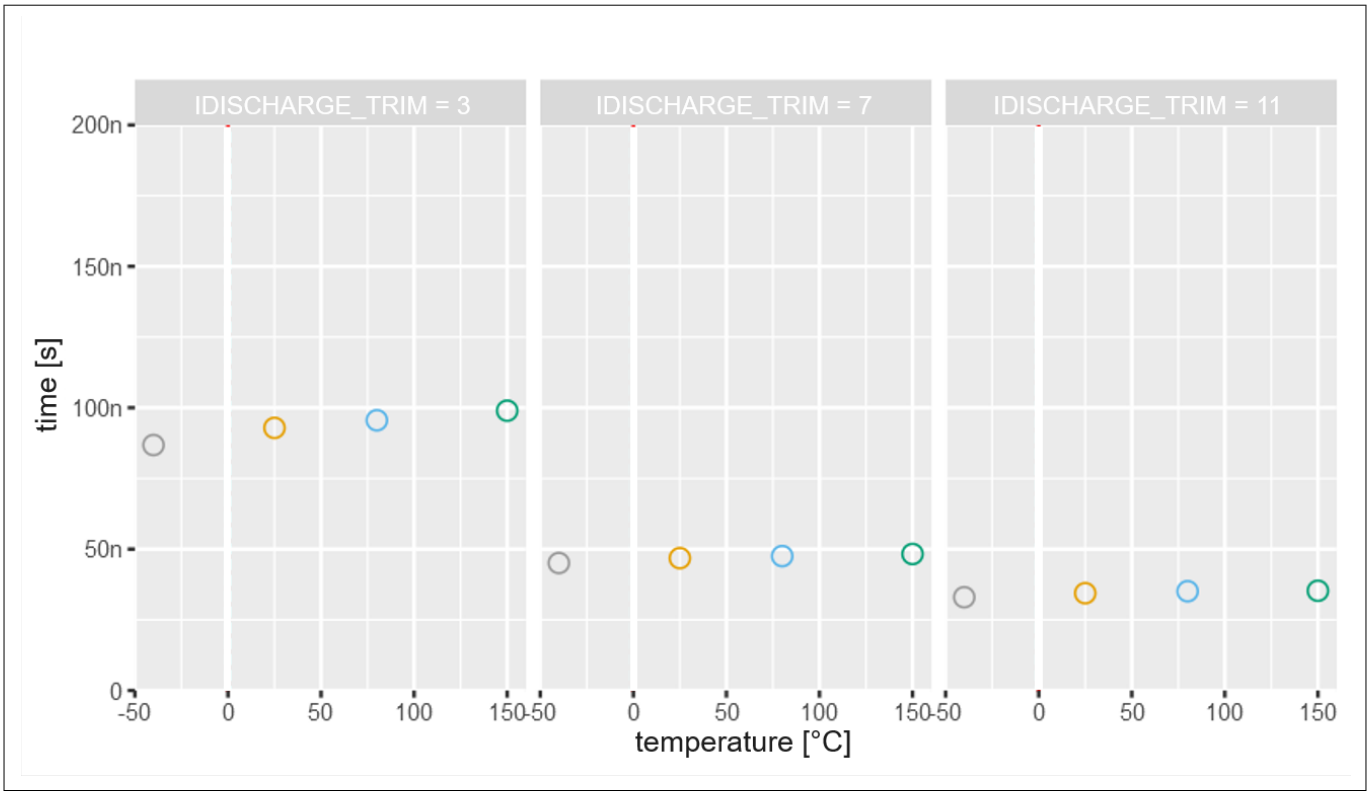

Figure 51 **The plot shows the influence of temperature on the VDS rise time for low-side MOSFETs. It is measured when a gate driver is tested with a MOSFET at 13. V and 30 A load current**

Related information

The influence of temperature on page 37

3.2.3.2.5 The influence of load current

The plot in the figure below shows the VDS rise time at different load currents and gate discharge current settings. The plot is divided into three sections, one for each gate discharge current setting. It contains VDS rise time values measured when a gate driver is tested with a low-side MOSFET at constant supply voltage and temperature. The influence of load current on VDS rise time is insignificant. The difference between minimum and maximum value of VDS rise time is nearly 7 percent of maximum value at lower and medium gate discharge current settings. It is 27% at a high gate charge current setting because the time is very small in this case.

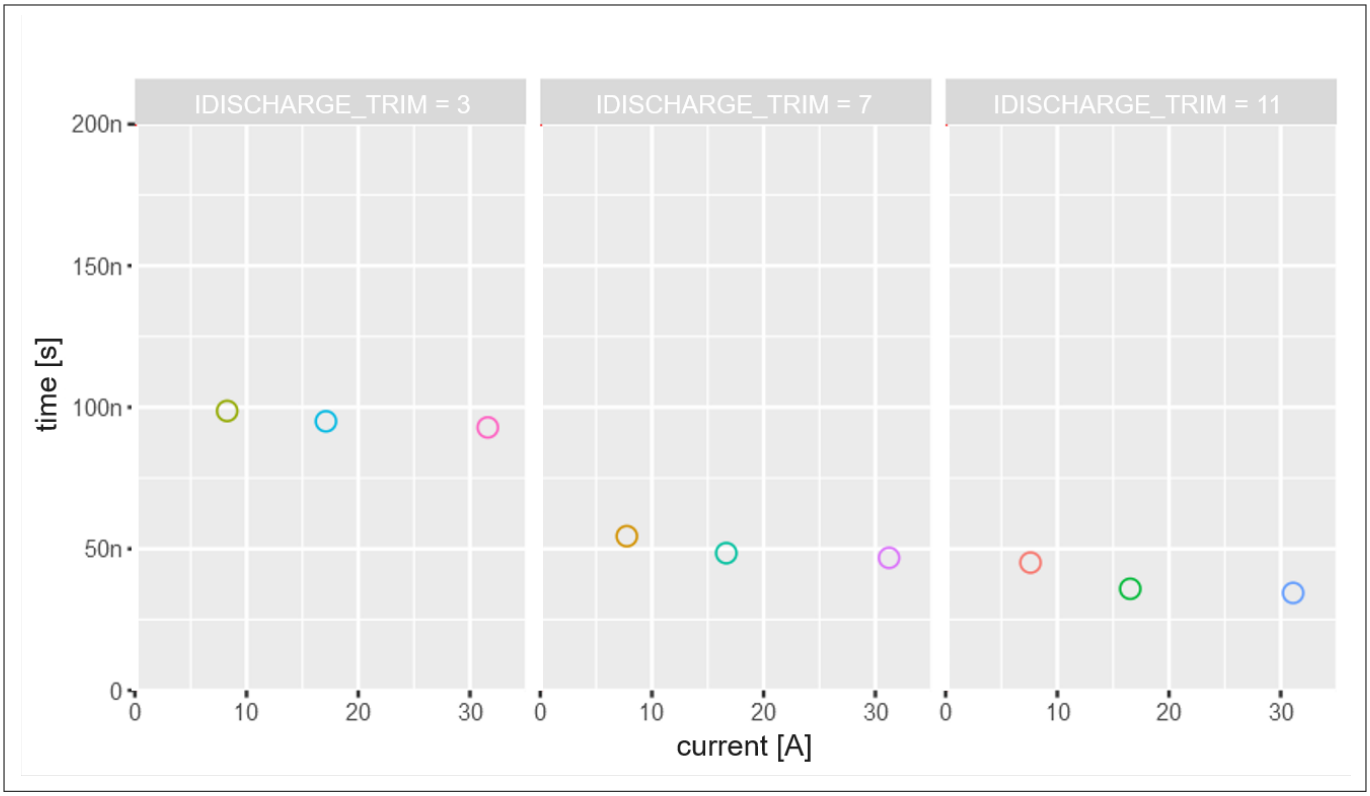

Figure 52 **The plot shows the influence of load current on VDS rise time for low-side MOFSETs. It is measured when a gate driver is tested with a MOSFET at 13.5 V supply voltage at 25°C temperature.**

3.2.4 Turn ON delay

The turn ON delay is the time measured from 10% of gate-source voltage (V_{GS}) nominal value to 90% of drain-source voltage (V_{DS}) nominal value as shown in the figure below.

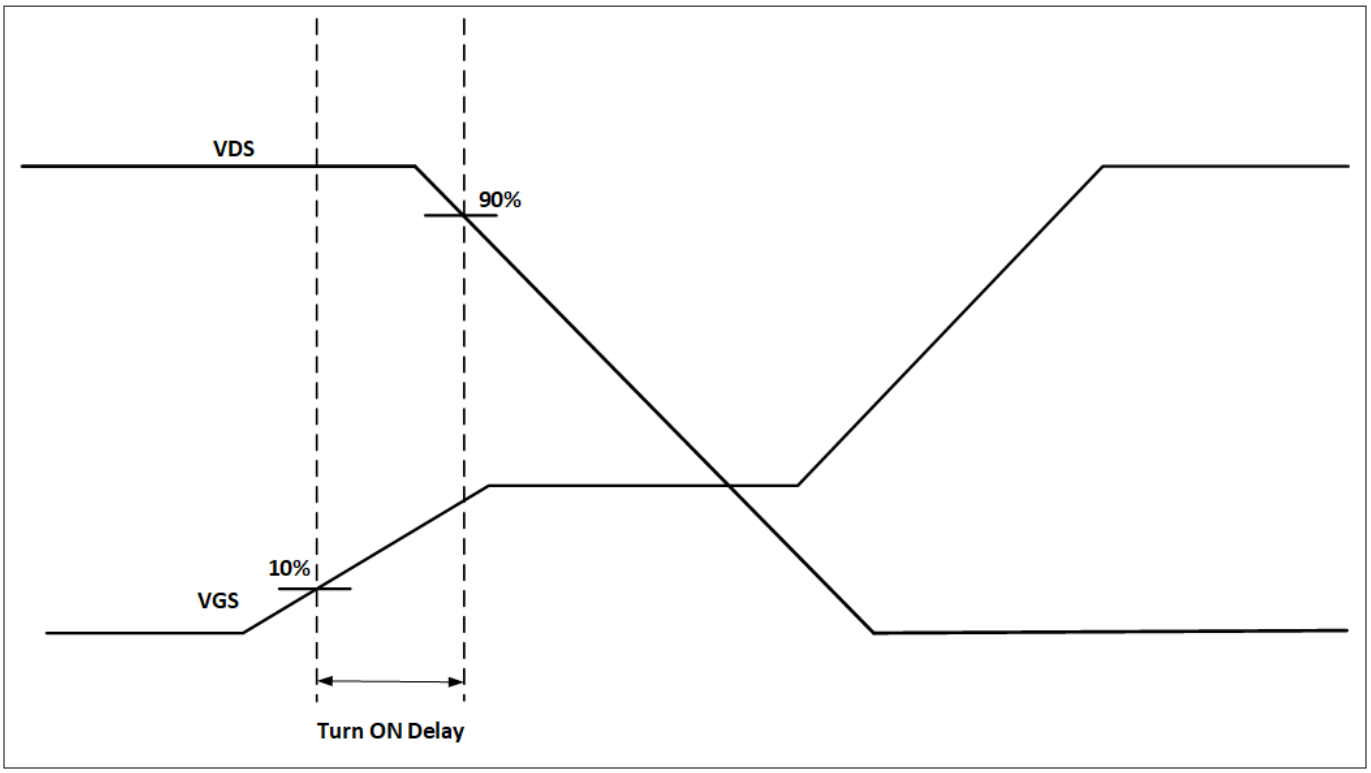

Figure 53 Turn ON delay measurement

3.2.4.1 High-side MOSFET

The figure below shows the measured turn ON delay of high-side MOSFETs when tested with a number of gate drivers under all test conditions. As expected, the VDS fall time decreases with increasing gate currents. The spread in the turn ON delay for each gate charge current setting is due to different MOSFETs, gate drivers, and test conditions. The influence of each variable on turn ON delay is discussed in the following sections.

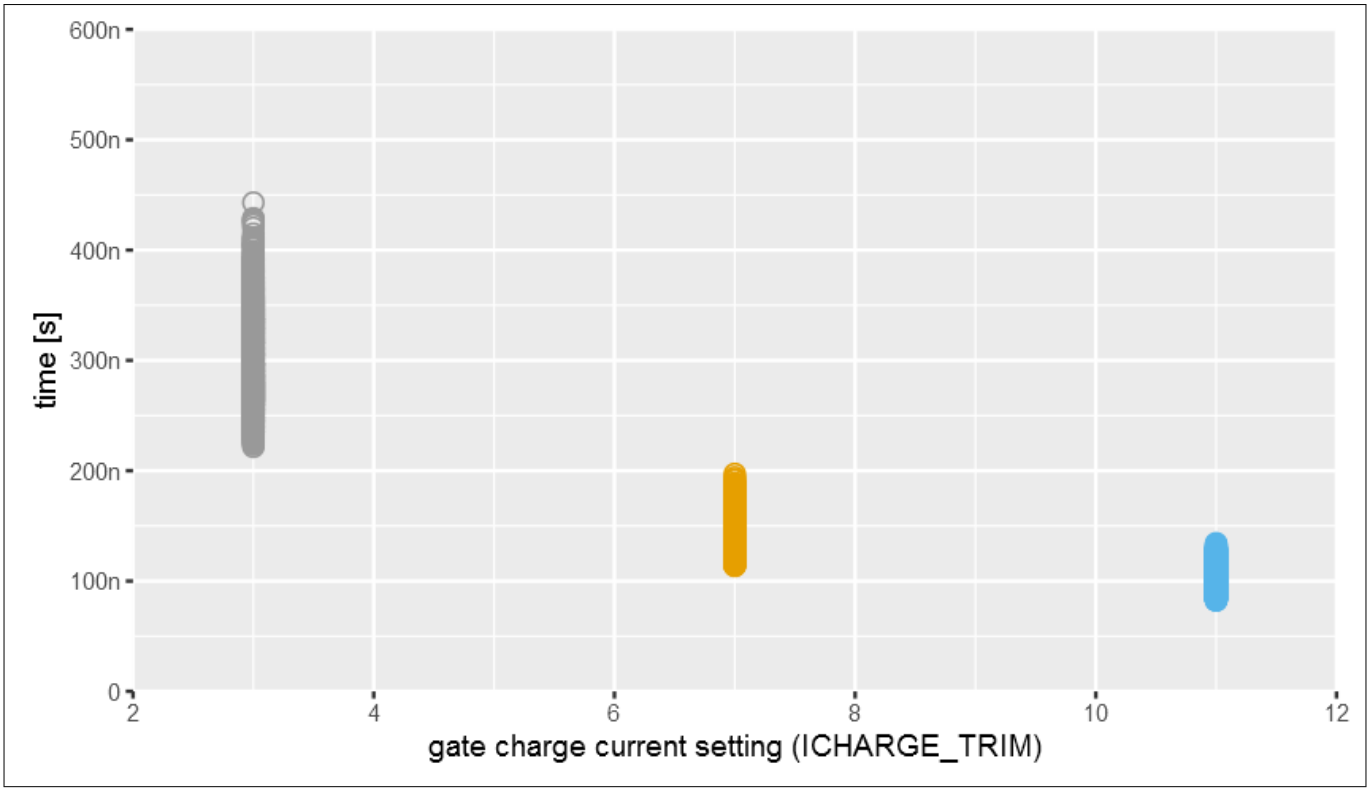

Figure 54 **The plot shows the turn ON delay for high side MOSFETs. It is measured when multiple MOTIX gate drivers are tested with multiple MOSFETs under all test conditions**

3.2.4.1.1 The influence of the gate driver

The figure below shows measured turn ON delay of high-side MOSFETs. It is measured when 3 gate driver samples are tested under all Test conditions with all high-side MOSFETs in a 3-phase bridge. It can be clearly seen that the spread in measured turn ON delay is different for each gate driver in the case of lower gate charge current settings. At low gate charge current setting, the longest turn ON delay of the slowest sample is 30% above the longest turn ON delay of the fastest sample. The difference in turn ON delay between gate driver samples decreases as gate charge current setting is increased. Therefore the gate driver is the main contributor in the spread of measured turn ON delay especially at lower gate charge current settings.

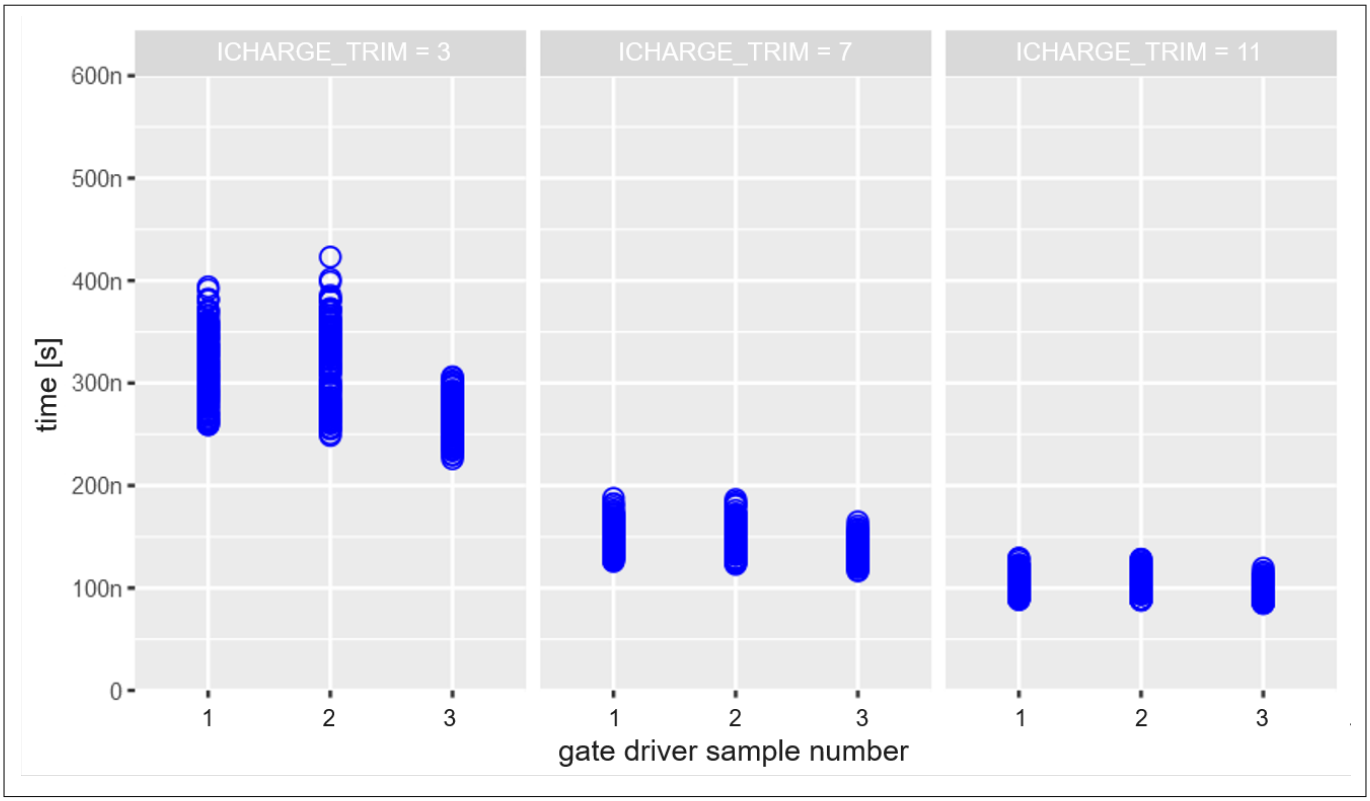

Figure 55 **The plot shows turn ON delay at different gate charge current settings. It is measured when 3 gate driver samples are tested with all high-side MOSFETs in a 3-phase bridge.**

3.2.4.1.2 The influence of the MOSFET

The figure below shows the measured turn ON delay of a high-side MOSFETs at different gate charge current settings. It is measured when a gate driver sample is tested under all Test conditions with all high-side MOSFETs mounted on 7 PCBs in a 3-phase bridge configuration. Note that these PCBs contains MOSFETs from three different lots. The spread of measured turn ON delay looks almost identical for all PCBs containing different MOSFET samples. Therefore, the influence of MOSFETs on the spread of turn ON delay is negligible in comparison with that of the gate driver.

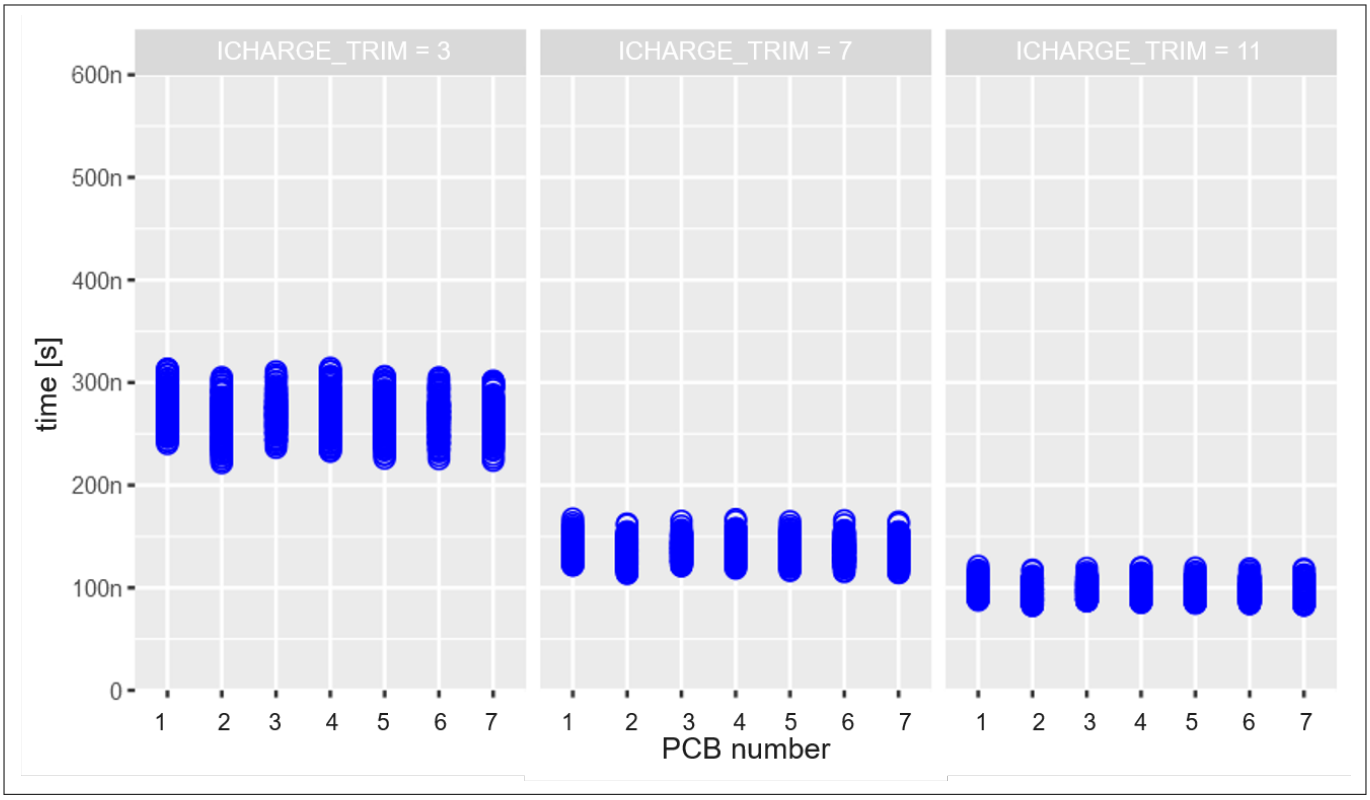

Figure 56 **The plot shows the turn ON delay at different gate charge current settings. It is measured when 3 gate driver samples are tested with all high-side MOSFETs in a 3-phase bridge on a PCB.**

3.2.4.1.3 The influence of supply voltage

The figure below shows the measured turn ON delay of high-side MOSFETs. It is measured when a gate driver is tested with a high-side MOSFET at 25°C temperature and 30 A load current. The measured turn ON looks identical for different supply voltages at medium and higher gate charge current settings. However, it changes slightly for lower gate charge current settings. The delta between minimum and maximum turn ON delay is 9% of maximum value at lower gate charge current settings. Figure 58 shows the gate-source and drain-source waveforms captured during the test at different supply voltages, 25°C temperature, 30 A load current and a lower gate charge current setting. It can be seen from the gate-source waveforms that threshold voltage remains the same at different supply voltages. The only difference is in the VDS waveforms at each supply voltage. The VDS waveform shows a slight double slope at 9 V supply voltage. As a result, the measured turn ON delay is slightly higher as it can be seen from plot in Figure 57 at lower gate charge current settings. For all other supply voltages, there is no double slope on drain-source voltage waveforms.

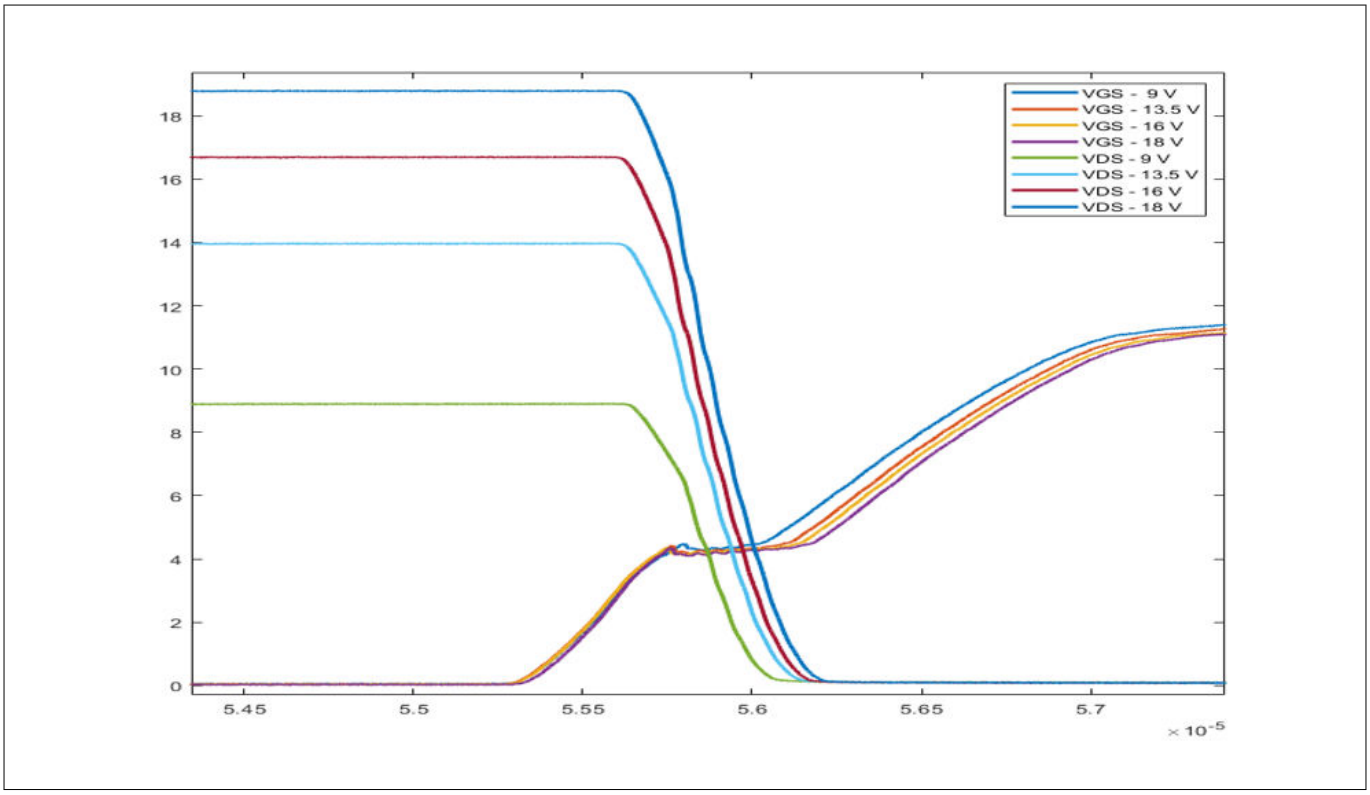

Figure 57 **The plot shows turn ON delay of high-side MOSFETs at different supply voltages. It is measured when a gate driver is tested with a MOSFET at 25°C and 30 A load current.**

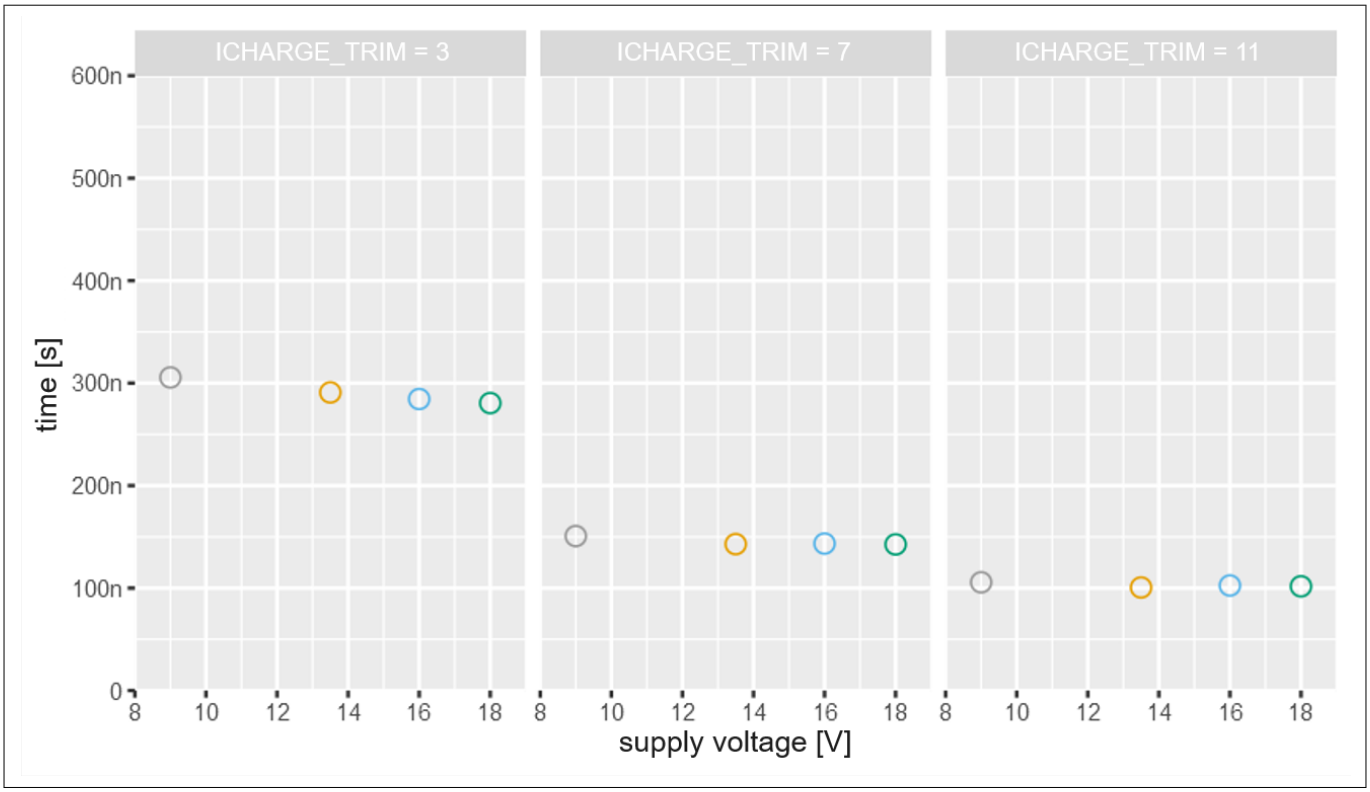

Figure 58 **The captured gate-source and drain-source waveforms during the test at 25°C temperature and 30 A load current**

3.2.4.1.4 The influence of temperature

The figure below shows the dependency of temperature on the turn ON delay. It is measured when a gate driver sample is tested with a high-side MOSFET at 13.5 V supply voltage and 30 A load current. The turn ON delay is expected to change with temperature because increasing temperature reduces the threshold voltage of MOSFETs, as it can be seen from gate-source voltage waveforms in Figure 60 It can be seen from the plot that turn ON delay slightly decreases with increasing temperature at all gate discharge current settings.

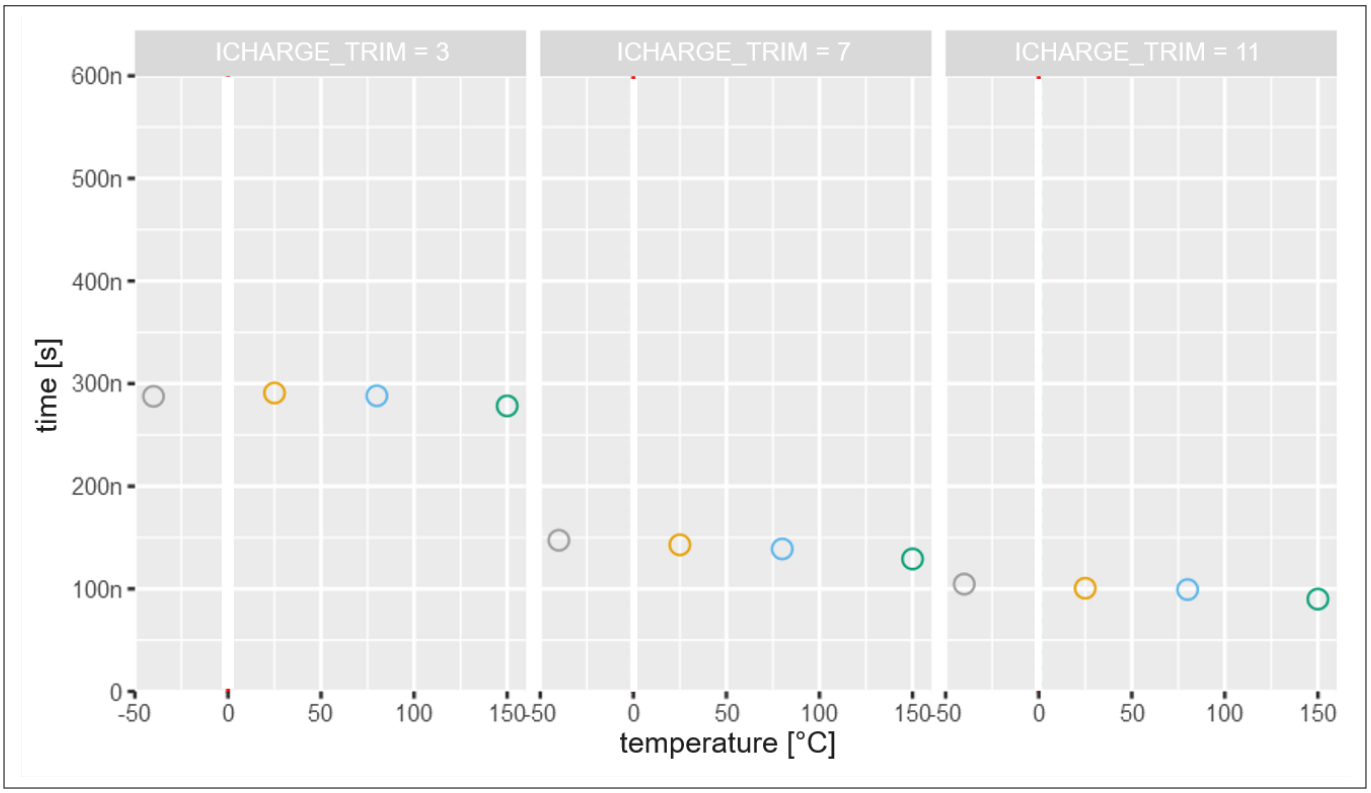

Figure 59 **The plot shows the turn ON delay of high-side MOSFETs at different temperatures. It is measured when a gate driver is tested with a MOSFET at 13.5 V and 30 A load current.**

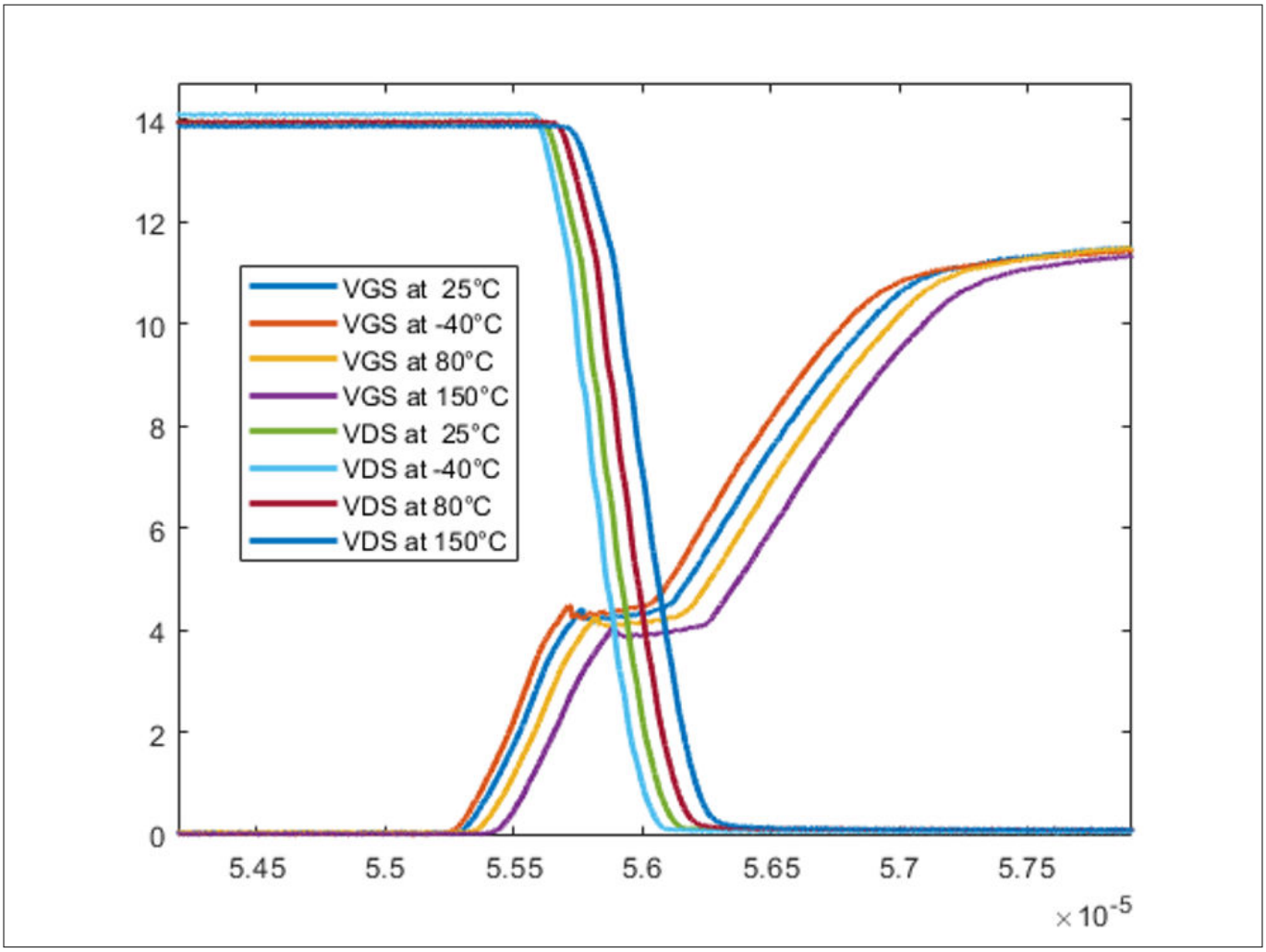

Figure 60 **The captured gate-source voltage and drain-source voltage waveforms at different temperatures when supply voltage is 13.5 V and load current is 30 A.**

3.2.4.1.5 The influence of load current

The figure below shows the measured turn ON delay for a high-side MOSFET when it is tested with a gate driver sample at 13.5 V supply voltage and 25°C temperature. The turn ON delay is expected to change with load current because increasing load current of the MOSFET increases the threshold voltage of the MOSFET at the lower gate charge current setting, It can be clearly seen from the plot that the turn ON delay increases when the load current goes from 8 A to 18 A. However, there is no change in the turn ON delay when load current changes from 18 A to more than 30 A. On the other hand, the turn ON delay does not even change when the load current is increased at medium and higher gate charge current settings. The root cause of this difference is the parasitic inductance of the PCB. The effects of parasitic inductance become dominant as load current, charge current, or both, are increased. The parasitic inductance produces two different slopes on the VDS waveform. As a result of double slopes, the measured turn ON delay remains the same for different load currents. Refer to the captured gate-source and drain-source waveforms at three load currents. It can be clearly seen that the threshold voltage increases with increasing load current. When the load current is 8 A, the gate-source waveform does not have a peak at the start of the Miller plateau and the drain-source waveform has only one slope. However, at 16 A and 30 A of load current, the gate-source waveform has a peak at the start of the Miller plateau and the drain-source waveform has two different slopes as highlighted by the arrows.

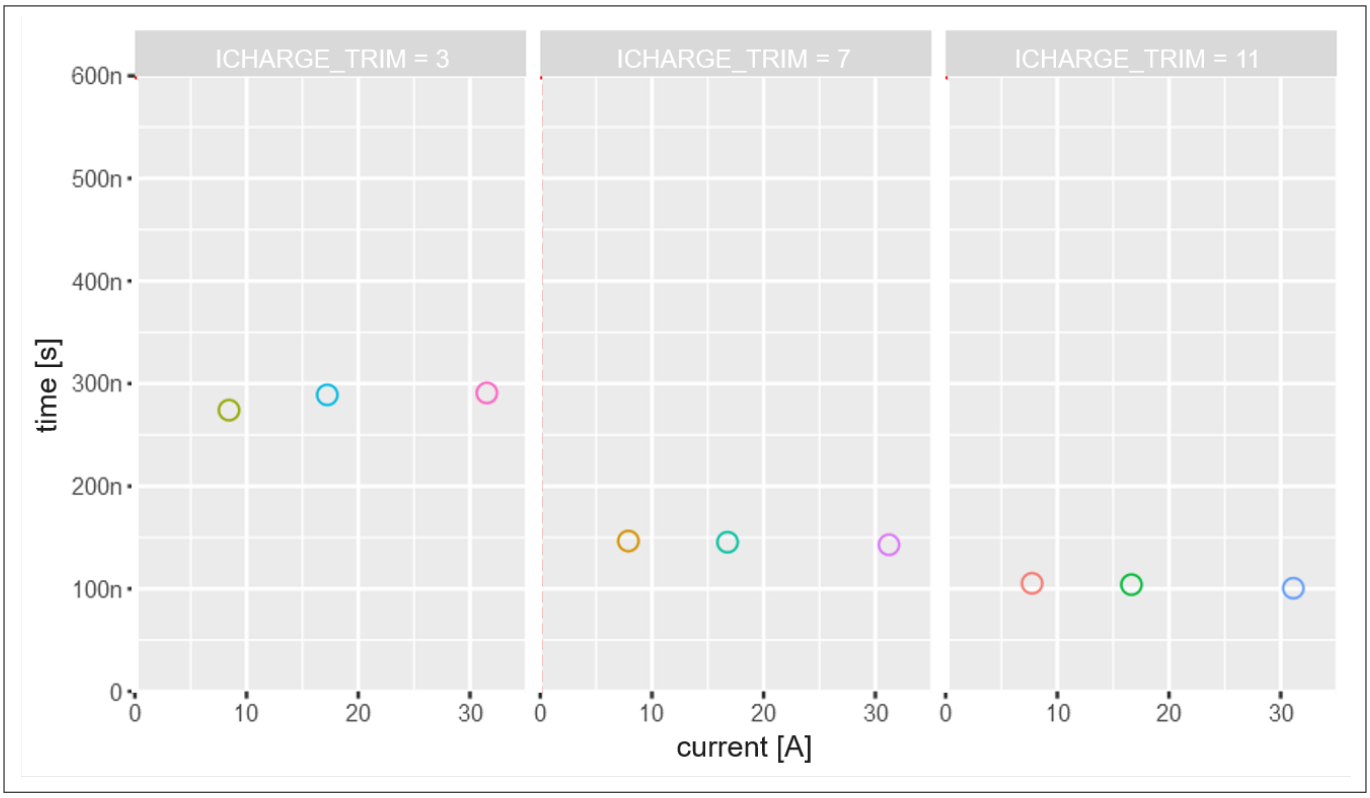

Figure 61 **The plot shows the turn ON delay for the high-side MOSFET at different load currents. It is measured when a gate driver is tested with a MOSFET at 13.5 V and 25°C temperature**

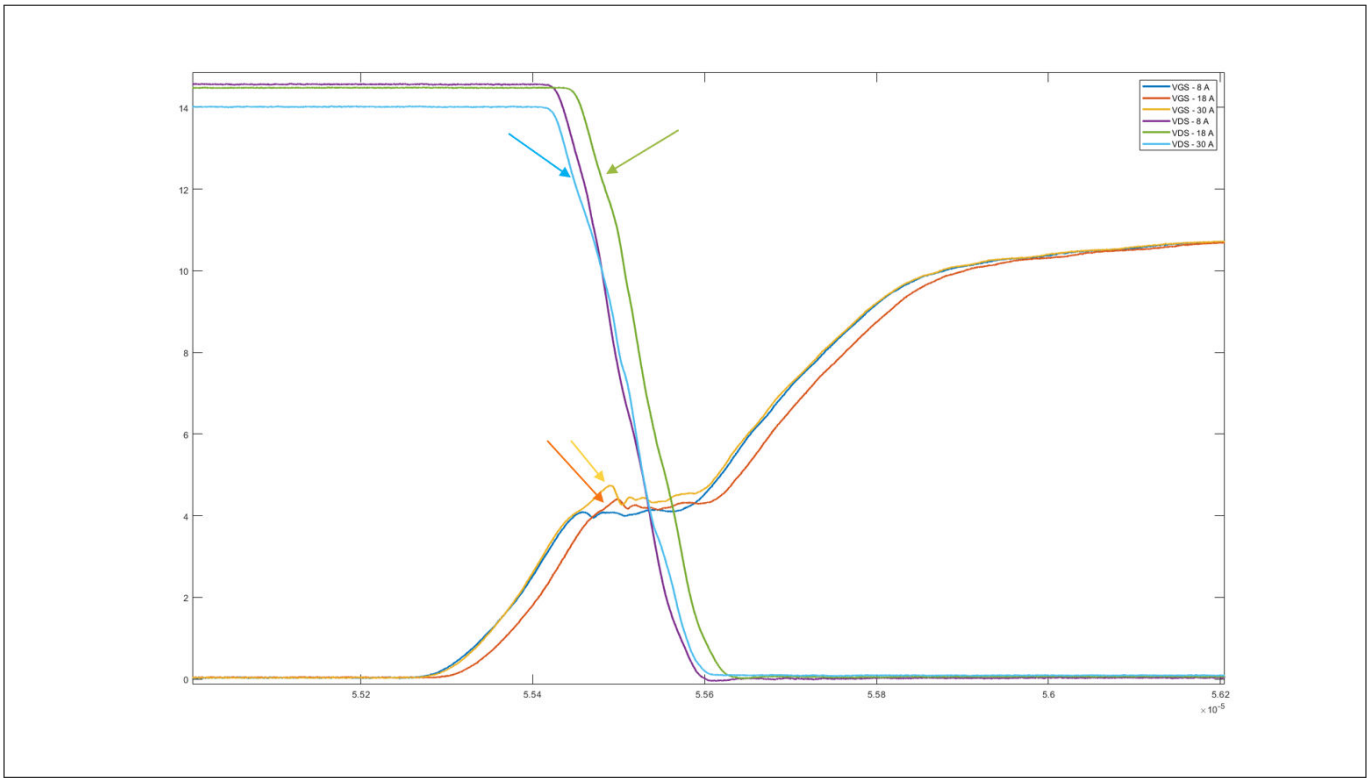

Figure 62 The VGS and VDS waveforms at two different load current values

3.2.4.2 Low-side MOSFET

The figure below shows the measured turn ON delay of low-side MOSFETs. It is measured when a gate driver sample is tested under all Test conditions with all low-side MOSFETs. Each data point shows the turn ON delay of one of all possible test conditions. The spread in measured turn ON delay decreases with increasing gate charge current settings. The influence of gate drivers, MOSFETs and test conditions on the spread of turn ON delay is discussed in the following sections.

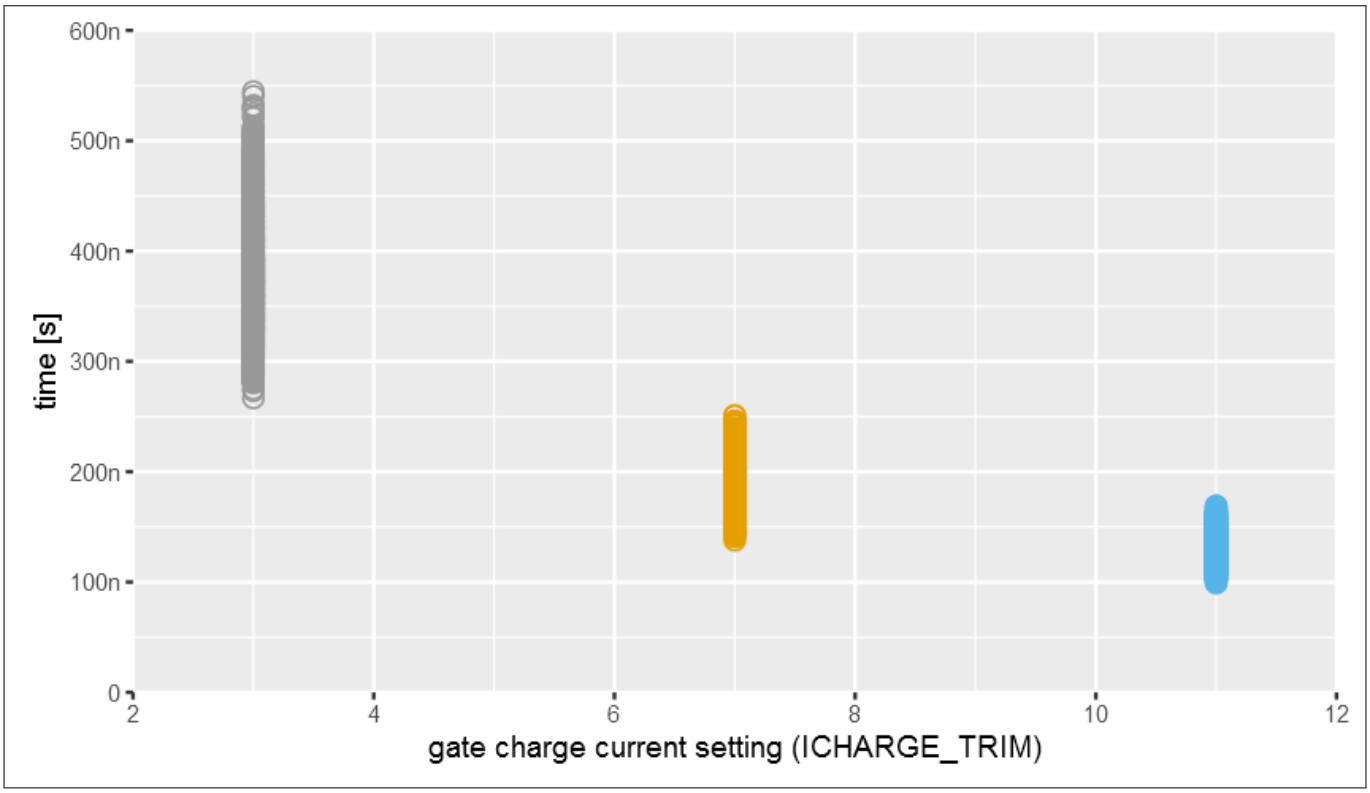

Figure 63 **The plot shows the turn ON delay of low-side MOSFETs when it is tested with multiple gate drivers and under all test conditions**

3.2.4.2.1 The influence of the gate driver

The plot in the figure below shows the turn ON delay of low-side MOSFETs at different gate charge current settings. It is measured with a gate driver sample and is tested under all Test conditions with all low-side MOSFETs in a-3 phase bridge. The turn ON delay looks different for each gate driver sample in the case of lower gate charge current settings. At low gate charge current setting, the longest turn ON delay of the slowest sample is 19% above the longest turn ON delay of the fastest sample. The difference in the turn ON delay among gate driver samples reduces as gate charge current is increased. It can be said the contribution of the gate driver in the spread of turn ON delay is significant, especially at lower gate charge current settings.

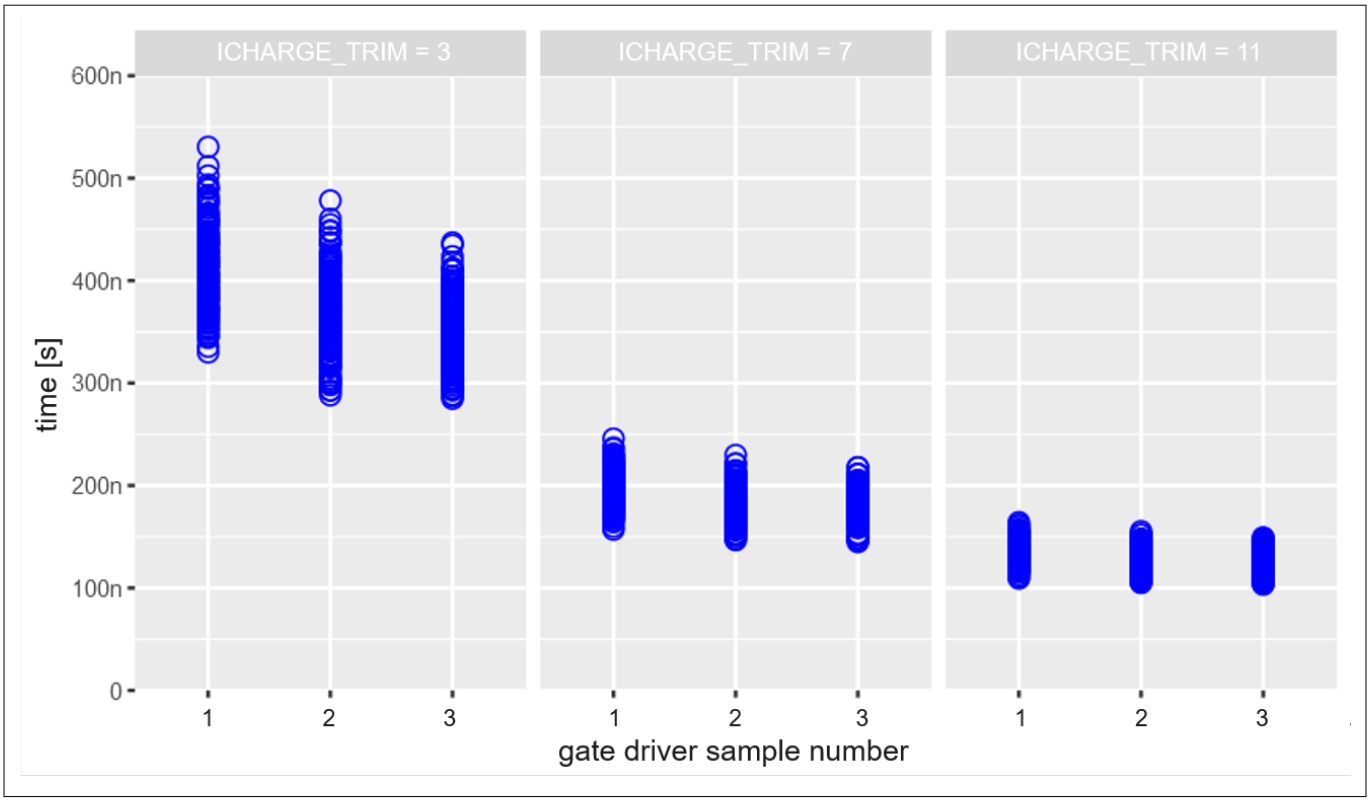

Figure 64 **The plot shows the turn ON delay at different gate charge current settings. It is measured when 3 gate driver samples are tested with all low-side MOSFETs in a 3-phase bridge.**

3.2.4.2.2 The influence of the MOSFET

To see the influence of low-side MOSFETs on the turn ON delay, refer to the plot in the figure below. The plot shows measured turn ON delays when a gate driver sample is tested at all Test conditions with all low-side MOSFETs mounted on 7 PCBs in a 3-phase bridge configuration. The turn ON delays look identical for different MOSFETs mounted on different PCBs at medium and higher gate discharge current settings. There is a slight difference in turn ON delays at lower gate discharge current settings, however, it is insignificant. It can therefore be said that the overall influence of MOSFETs in the variation of the turn ON delay is insignificant when compared to that of the gate driver.

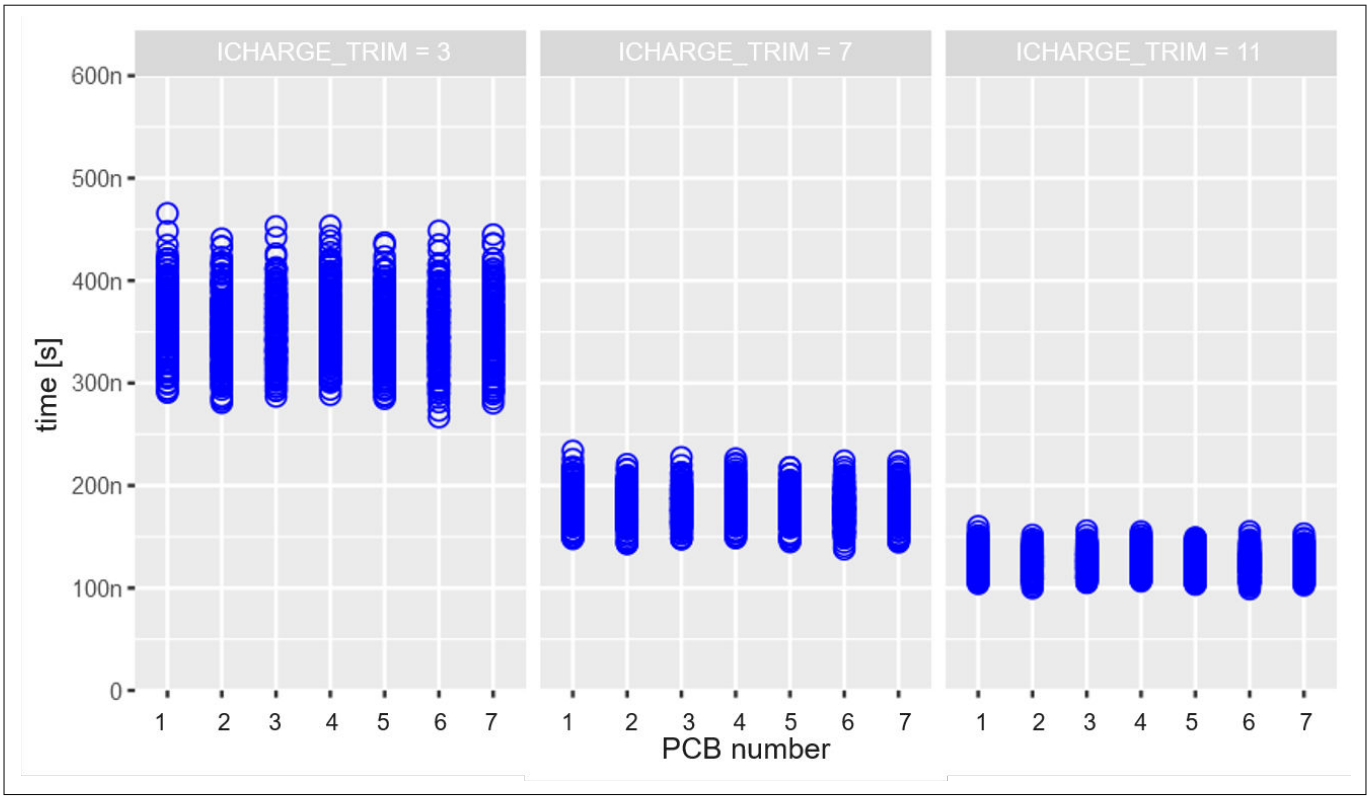

Figure 65 **The plot shows the turn ON delay at different gate discharge current settings. It is measured when a gate driver is tested with all low-side MOSFETs mounted on each PCB.**

3.2.4.2.3 The influence of supply voltage

The plot in figure below shows the measured turn ON delay of low-side MOFSETs when a gate driver and a MOSFET are tested under all test conditions. It can be clearly seen that the supply voltage has negligible effect on the turn ON delay at medium and higher gate charge current settings. The turn ON delay changes with supply voltage at lower gate charge current settings. The delta between minimum and maximum value is 10% of maximum value at low gate charge current setting.

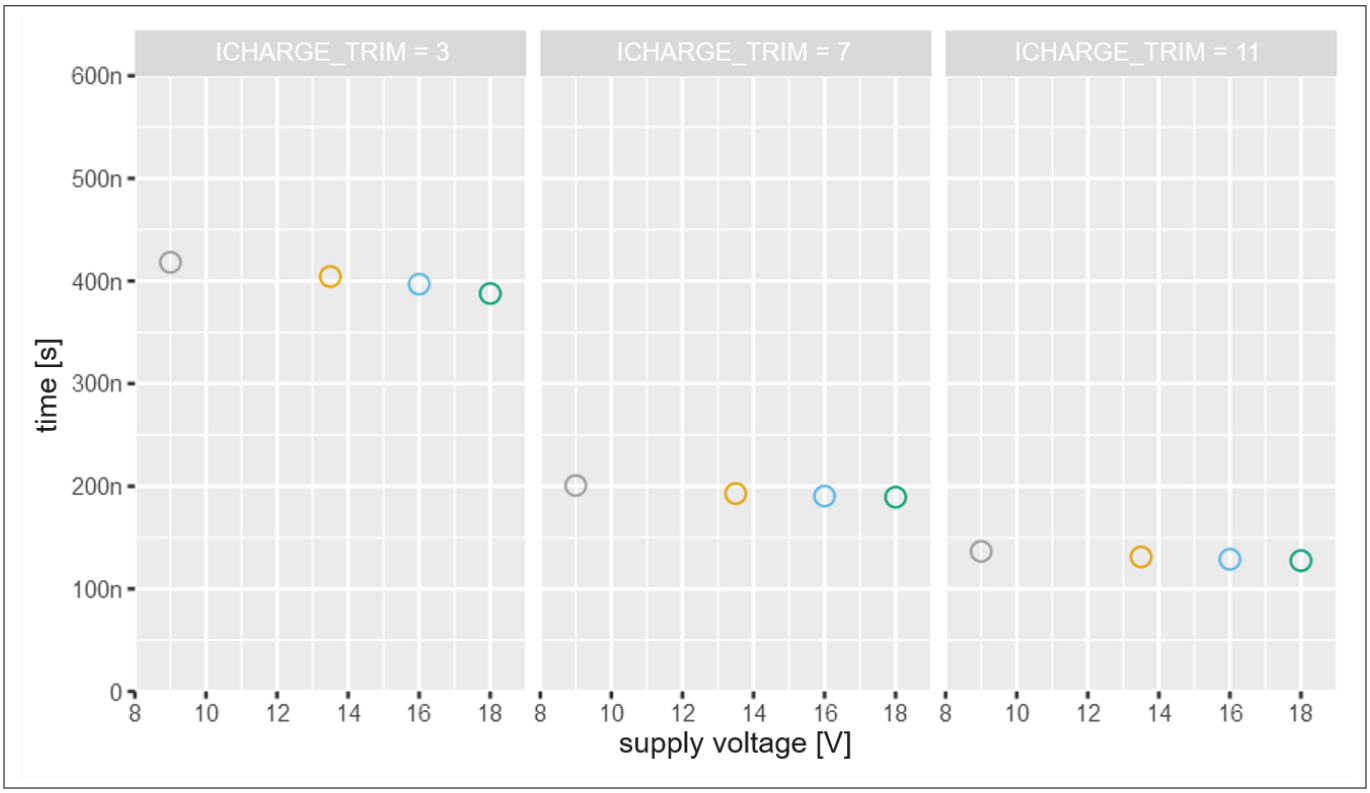

Figure 66 **The plot shows the turn ON delay for low-side MOSFETs when it is tested with a gate driver at 25°C temperature and 30 A load current**

3.2.4.2.4 The influence of temperature

The plot below shows the influence of temperature on measured turn ON delays for low-side MOSFETs. It is measured when a gate driver sample is tested with a MOSFET at 13.5 V supply voltage and 30 A load current. As expected, the turn ON delay decreases with increasing temperature because the threshold voltage of the MOSFET decreases with increasing temperature.

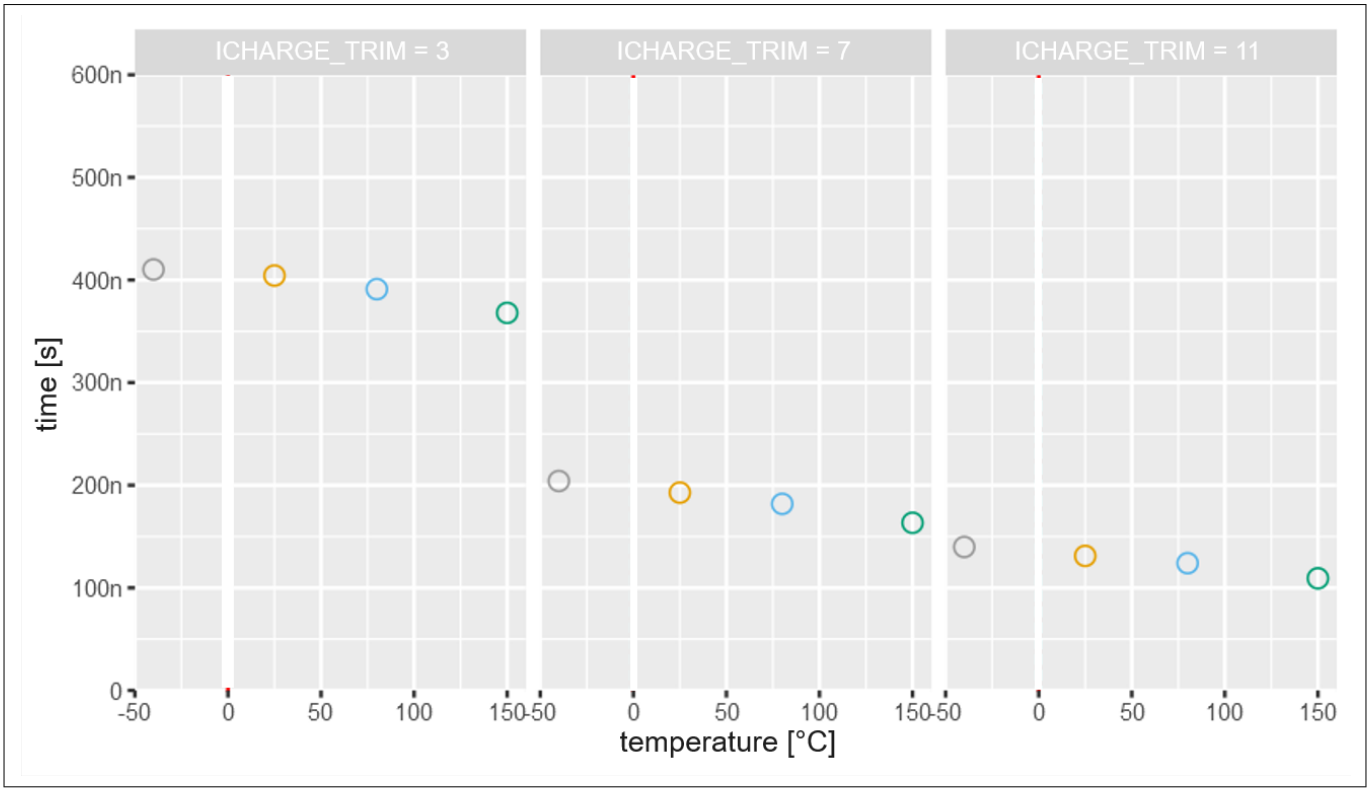

Figure 67 **The plot shows the turn ON delay for the low-side MOSFET. It is measured when a gate driver is tested with a MOSFET at 13.5 V supply voltage and 30 A load current.**

3.2.4.2.5 The influence of load current

The plot below shows the turn ON delay of low-side MOSFETs across different load current values. The plot shows measured turn ON delay when a gate driver sample is tested with a low-side MOSFET at 13.5 V supply voltage and 25°C temperature. It can be seen that the turn ON delay increases with increasing load current at lower and medium gate charge current settings. This is because the threshold voltage of the MOSFET increases with increasing load current. However, load current has no influence on the turn ON delay at high gate charge current settings. This is explained in detail in The influence of load current.

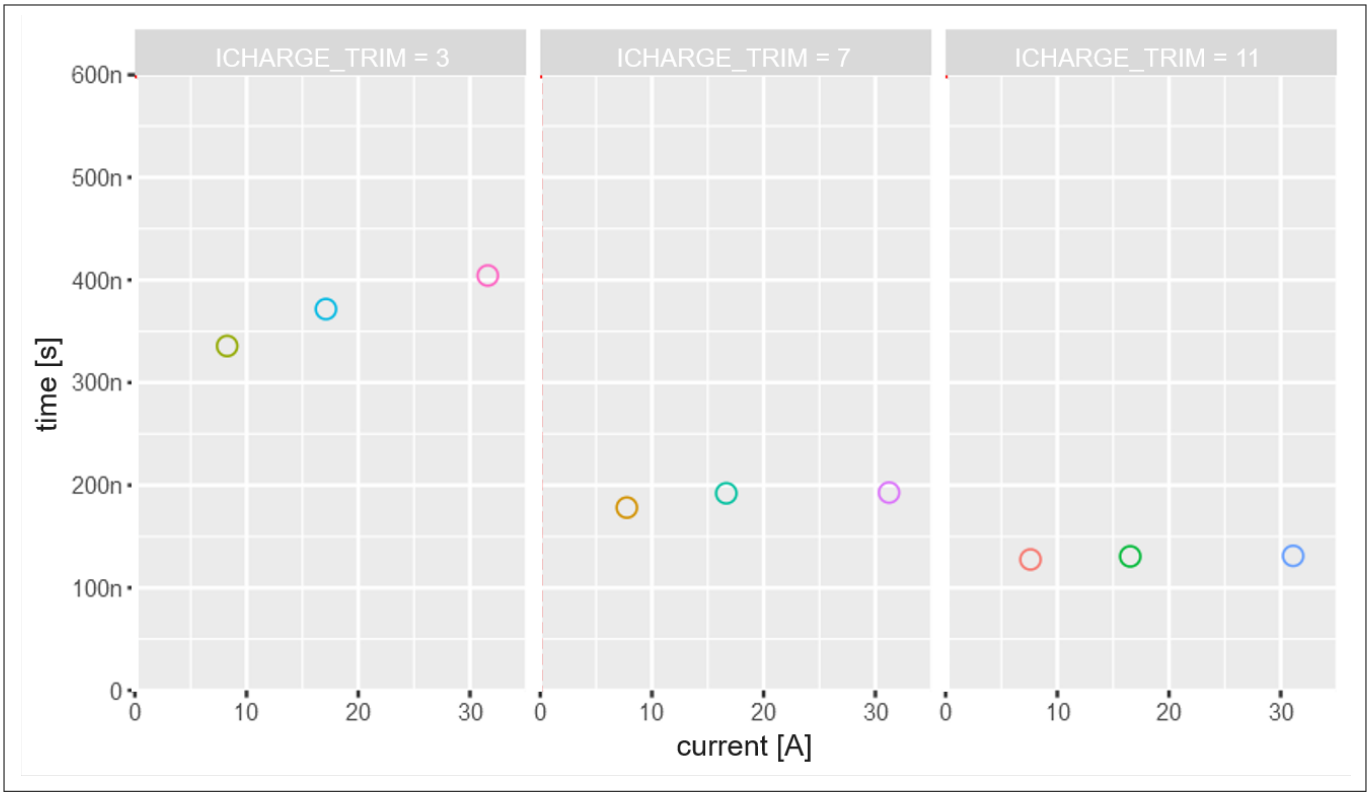

Figure 68 **The plot shows the turn ON delay for low-side MOSFETs at different load currents. It is measured when a gate driver is tested with a MOSFET at 13.5 V and 25°C temperature**

3.2.5 Turn OFF delay

The turn OFF delay is the time from 90% of VGS nominal value to 10% of VDS nominal value, as seen in the figure below

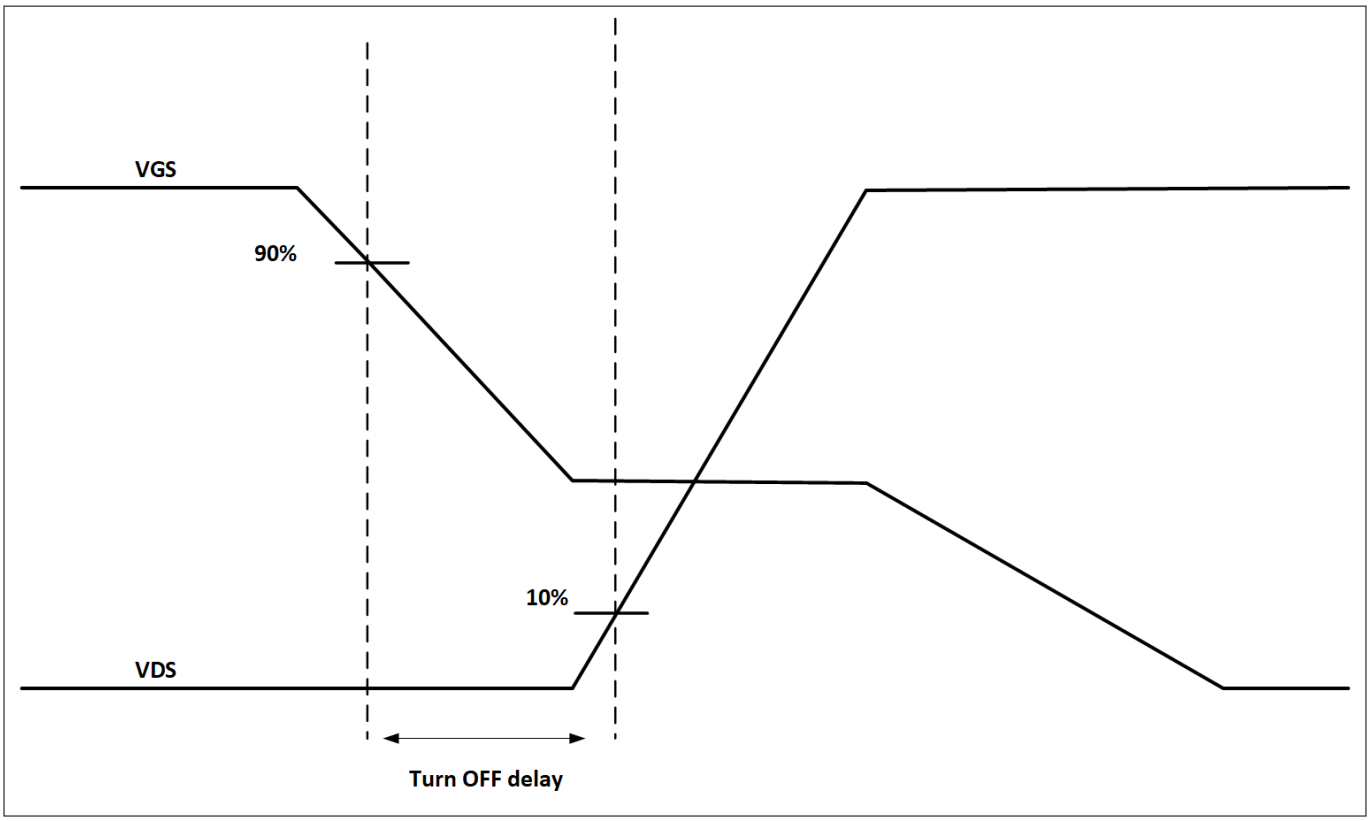

Figure 69 Turn OFF delay

3.2.5.1 High-side MOSFET

The figure below shows the measured turn OFF delay of high-side MOSFETs when tested with a number of gate drivers under all test conditions. As expected, the turn ON delay decreases with increasing gate currents. The spread in the turn ON delay for each gate discharge current setting is due to different MOSFETs, gate drivers, and test conditions. The influence of each variable on the turn ON delay is discussed in the following sections.

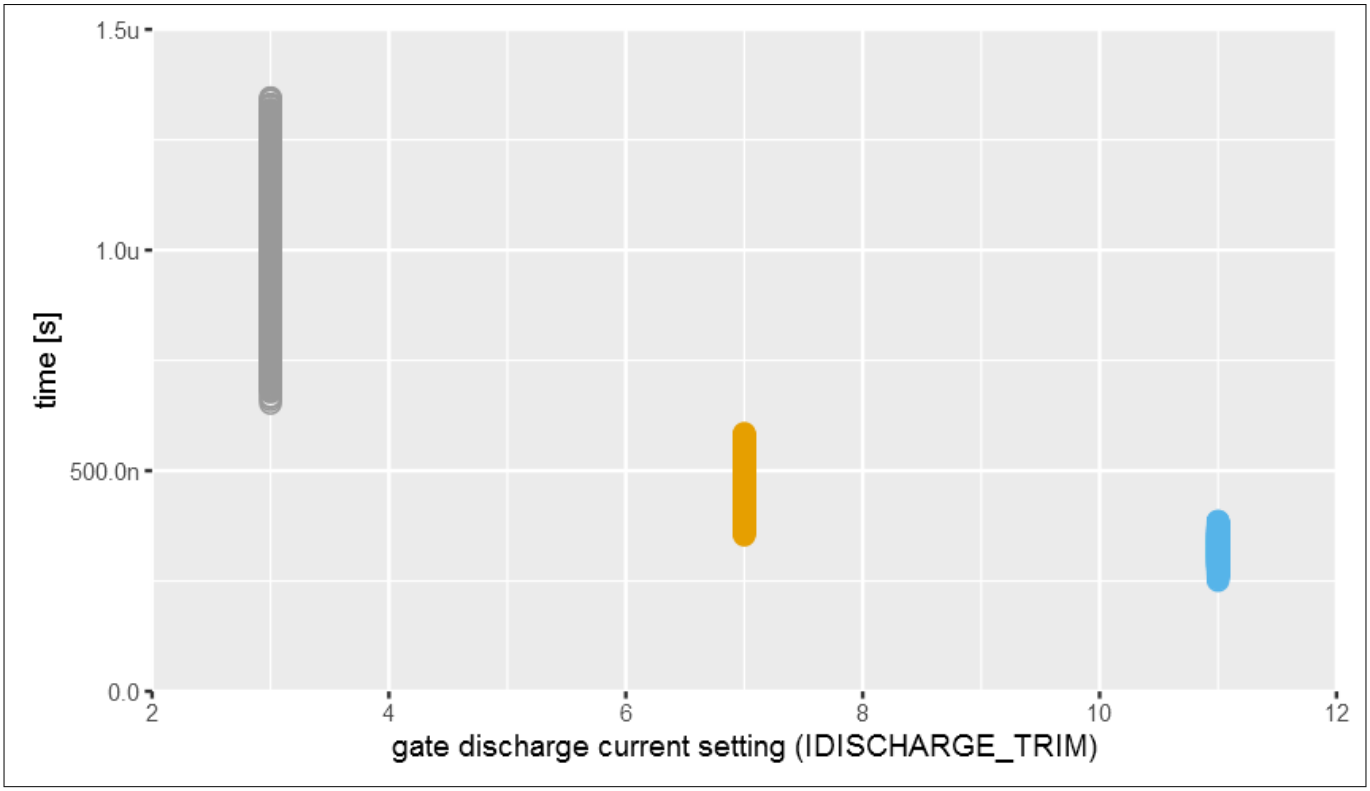

Figure 70 **The plot shows the turn OFF delay of high side MOSFETs when tested with multiple MOTIX gate drivers at all test conditions**

3.2.5.1.1 The influence of the gate driver

The figure below shows the measured turn OFF delays for high-side MOSFETs at different gate discharge current settings. It is measured when 3 gate driver samples are tested under all Test conditions with all high-side MOSFETs in a 3-phase bridge. It is clear from the plot that turn OFF delays are different for each gate driver samples. The difference is quite large in the case of lower gate discharge current settings and it reduces as the gate discharge current setting is increased. Therefore, the influence of the gate driver is significant on turn OFF delays, especially at lower gate discharge current settings.

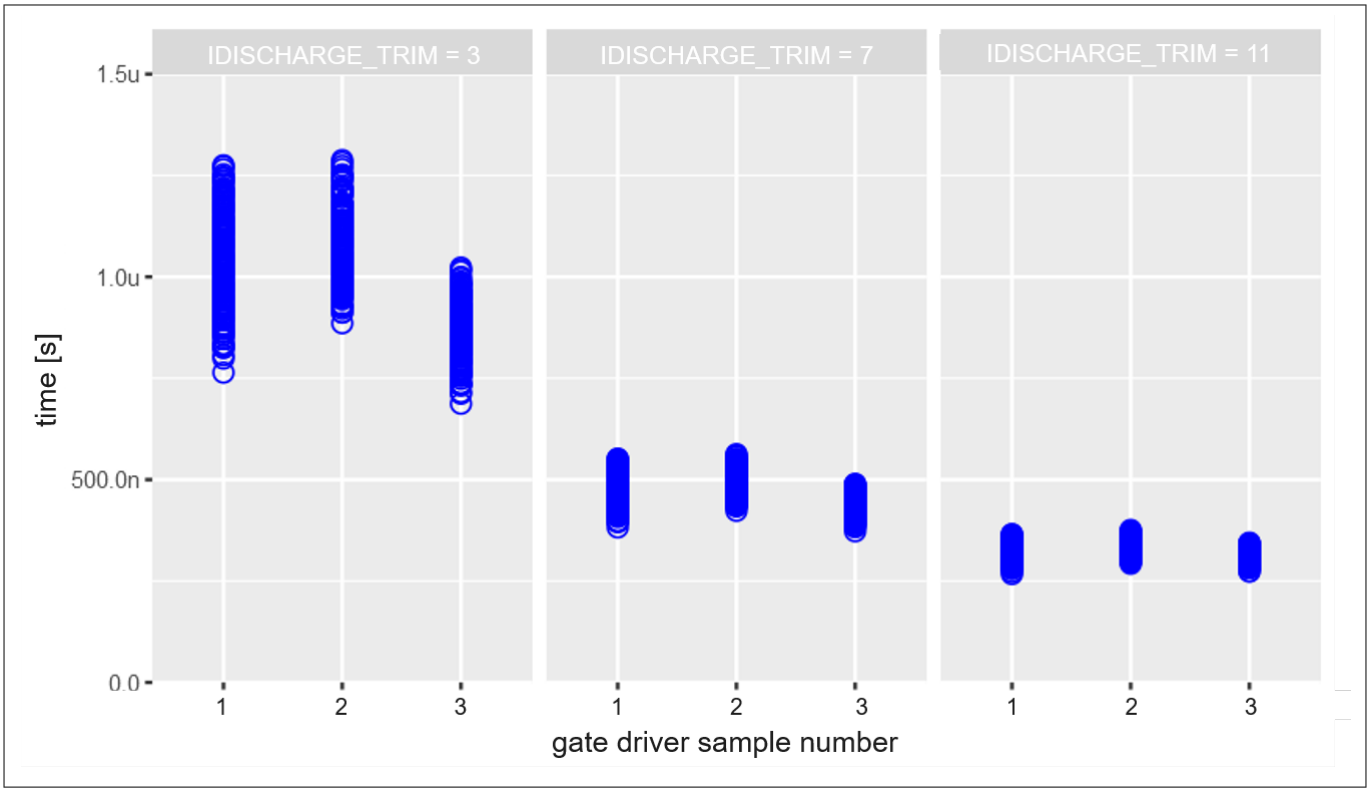

Figure 71 **The plot shows turn OFF delays at different gate discharge current settings. It is measured when 3 gate driver samples are tested with all high-side MOSFETs in a 3-phase bridge.**

3.2.5.1.2 The influence of the MOSFET

The figure below shows the measured turn OFF delay for high-side MOSFETs at different gate discharge current settings. It is measured when a gate driver sample is tested under all Test conditions with all high-side MOSFETs mounted on 7 PCBs in a 3-phase bridge configuration. Note that these PCBs contain MOSFETs from three different lots. The turn OFF delays looks identical for all MOSFETs on various PCBs at all gate discharge currents. Therefore, the influence of the MOSFET on the variation of the turn OFF delay is negligible when compared to that of the gate driver.

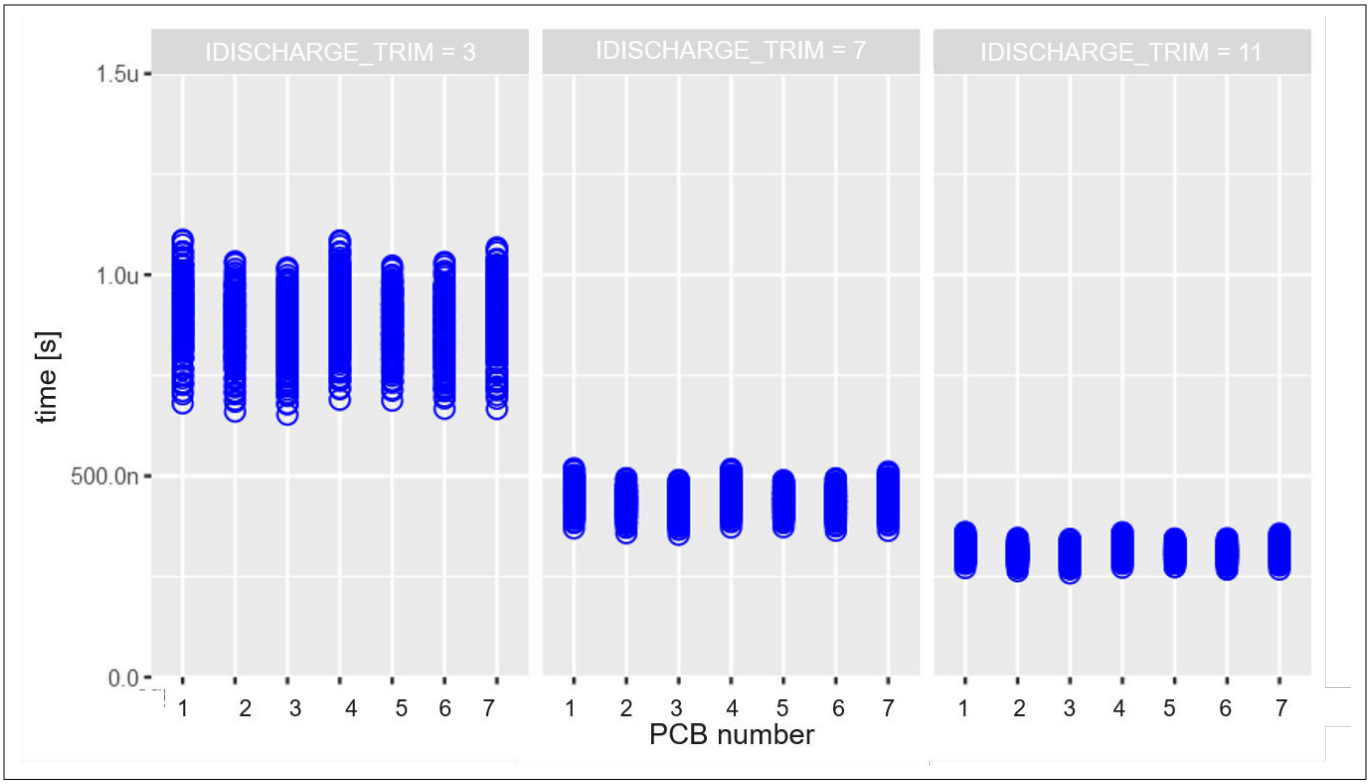

Figure 72 **The plot shows the turn OFF delay at different gate discharge current settings. It is measured using a gate driver that is tested with all high side MOSFETs mounted on various PCBs in a 3-phase configuration.**

3.2.5.1.3 The influence of supply voltage

The figure below shows the measured turn OFF delay for high-side MOSFETs when a single gate driver is tested with a single MOSFET across different supply voltages at 25°C temperature and 30A load current. It can be seen from the plot that supply voltages have negligible influence on the turn OFF delay at medium and high gate discharge current settings. However, the turn OFF delay changes slightly with changing supply voltages. At low gate charge current setting, the longest turn OFF delay of the slowest sample is 16% above the longest turn OFF delay of the fastest sample.

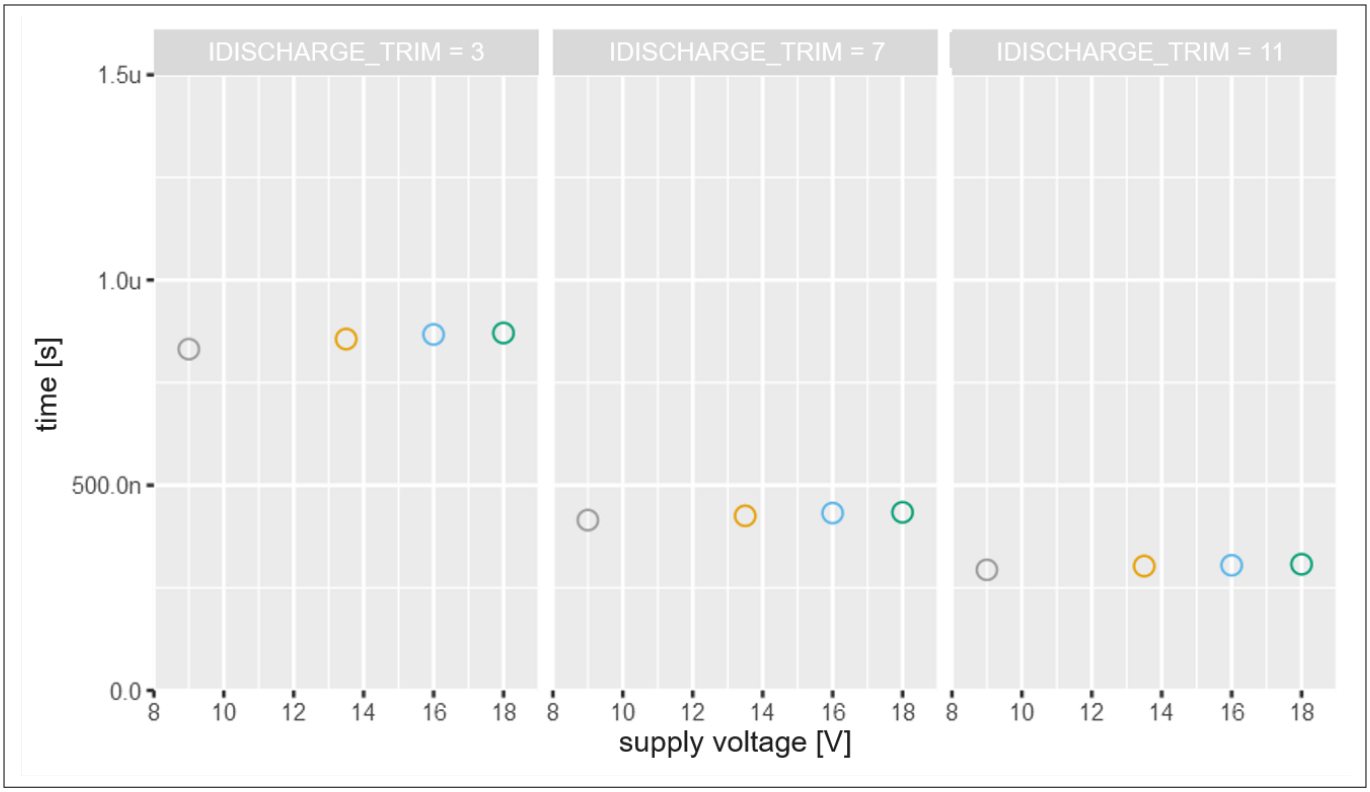

Figure 73 **The influence of the turn OFF delay at different supply voltages. The turn OFF delay is measured when a gate driver sample is tested with a MOSFET at 25°C temperature and 30 A.**

3.2.5.1.4 The influence of temperature

The figure below shows the influence of temperature on the turn OFF delay. It is measured when a gate driver sample is tested with a high-side MOSFET at 13.5 V supply voltage, constant current, and 25°C temperature. It can be clearly seen from the plot that the turn OFF delay increases with increasing temperature. The increase in turn OFF delay with temperature is expected because the threshold voltage of the MOSFET has a negative temperature coefficient.

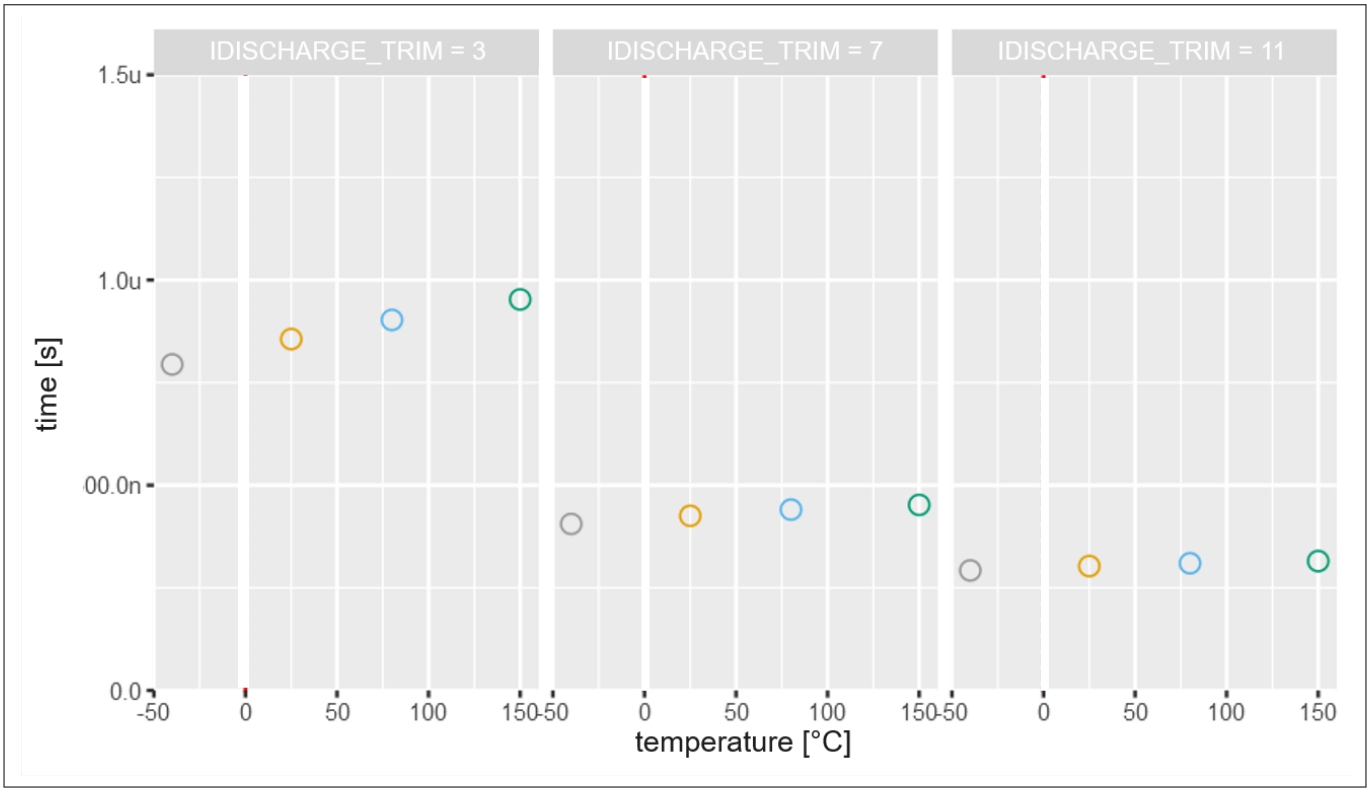

Figure 74 **The plot shows the influence of temperature on the turn OFF delay. The turn OFF delay is measured when a gate driver is tested with a MOSFET at 13.5 V supply voltage and 30 A load current.**

3.2.5.1.5 The influence of load current

The figure below shows the relationship between the turn OFF delay and the load current. The turn OFF delay is measured when a gate driver is tested with a MOSFET at 13.5 V supply voltage and 25°C temperature. It can be seen from the plot that the turn OFF delay decreases with increasing load current. It is expected behavior because the threshold voltage for the MOSFET decreases with increasing load current.

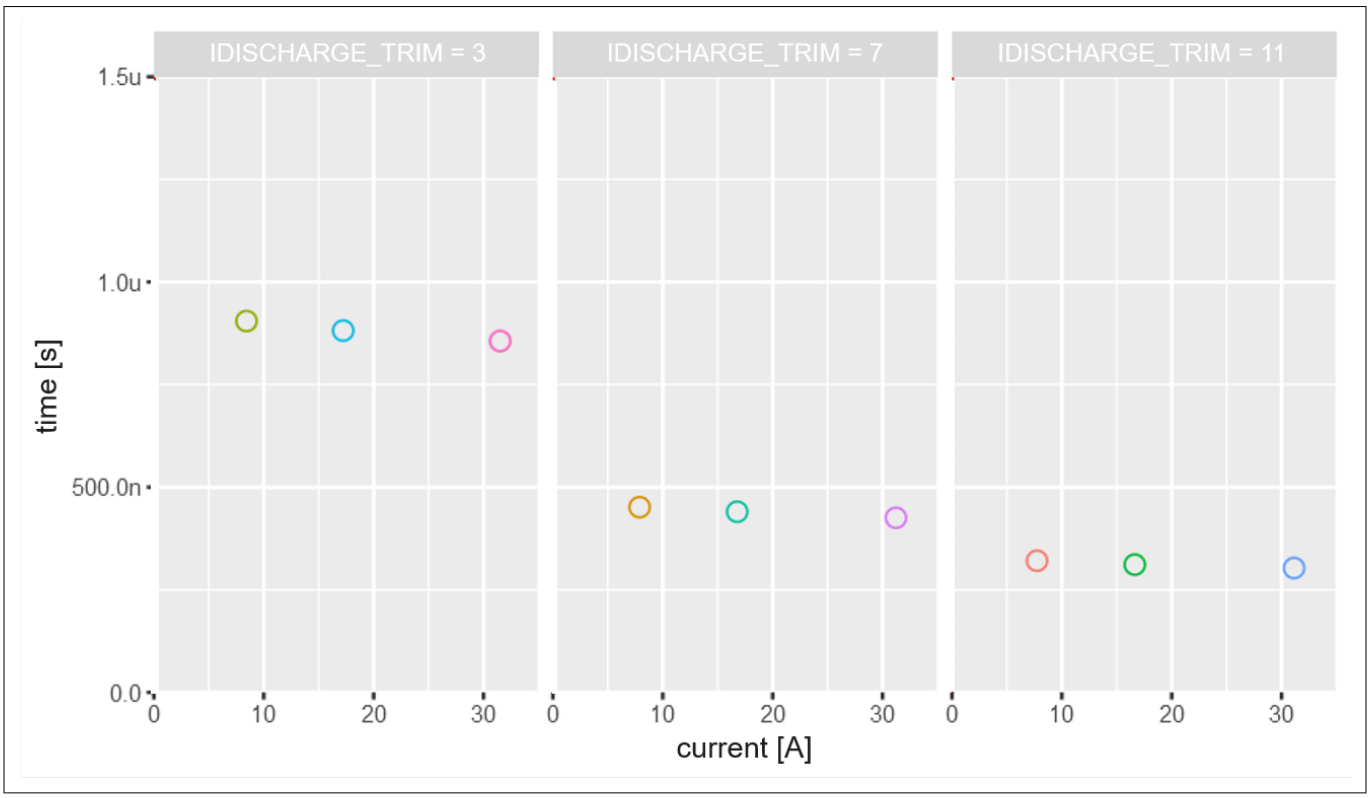

Figure 75 **The plot shows the influence of load current on the turn OFF delay. It is measured when a gate driver is tested with a MOSFET at 13.5 V and 25°C.**

3.2.5.2 Low-side MOSFET

The figure below shows the measured turn OFF delay for low-side MOSFETs when a number of gate drivers are tested with a number of low-side MOSFETs under all test conditions. The spread of measured turn ON delay decreases with increasing gate discharge current settings. The influence of gate drivers, MOSFETs, and test conditions on the spread of turn OFF delay is discussed in the following sections.

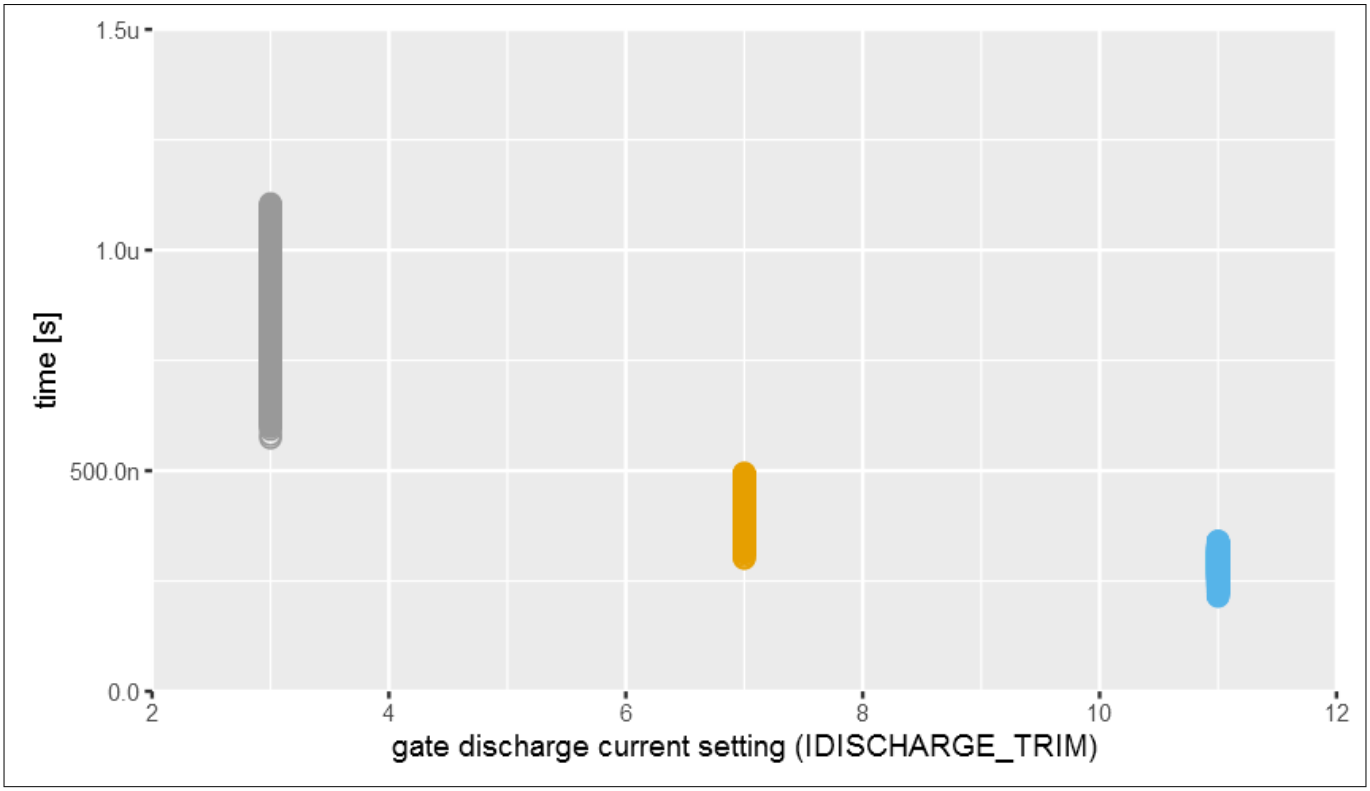

Figure 76 Turn OFF delay for low-side MOSFETs at different gate charge current settings measured with multiple gate drivers are tested with multiple MOSFETs under all test conditions

3.2.5.2.1 The influence of the gate driver

The figure below shows the turn OFF delays for low-side MOSFETs at different gate discharge current settings. The turn OFF delay is measured when various gate driver samples are tested under all Test conditions with all low-side MOSFETs in a 3-phase bridge. The turn OFF delays are different for each gate driver sample at all gate discharge current settings. The difference in turn OFF delay among gate driver samples is quite significant in the case of lower gate discharge current settings. At low gate charge current setting, the longest turn OFF delay of the slowest sample is 10% above the longest turn OFF delay of the fastest sample. The difference in turn OFF delays reduces as gate discharge current is increased. Therefore, the contribution of the gate driver to the variation of turn OFF delay is significant, especially at lower gate discharge current settings.

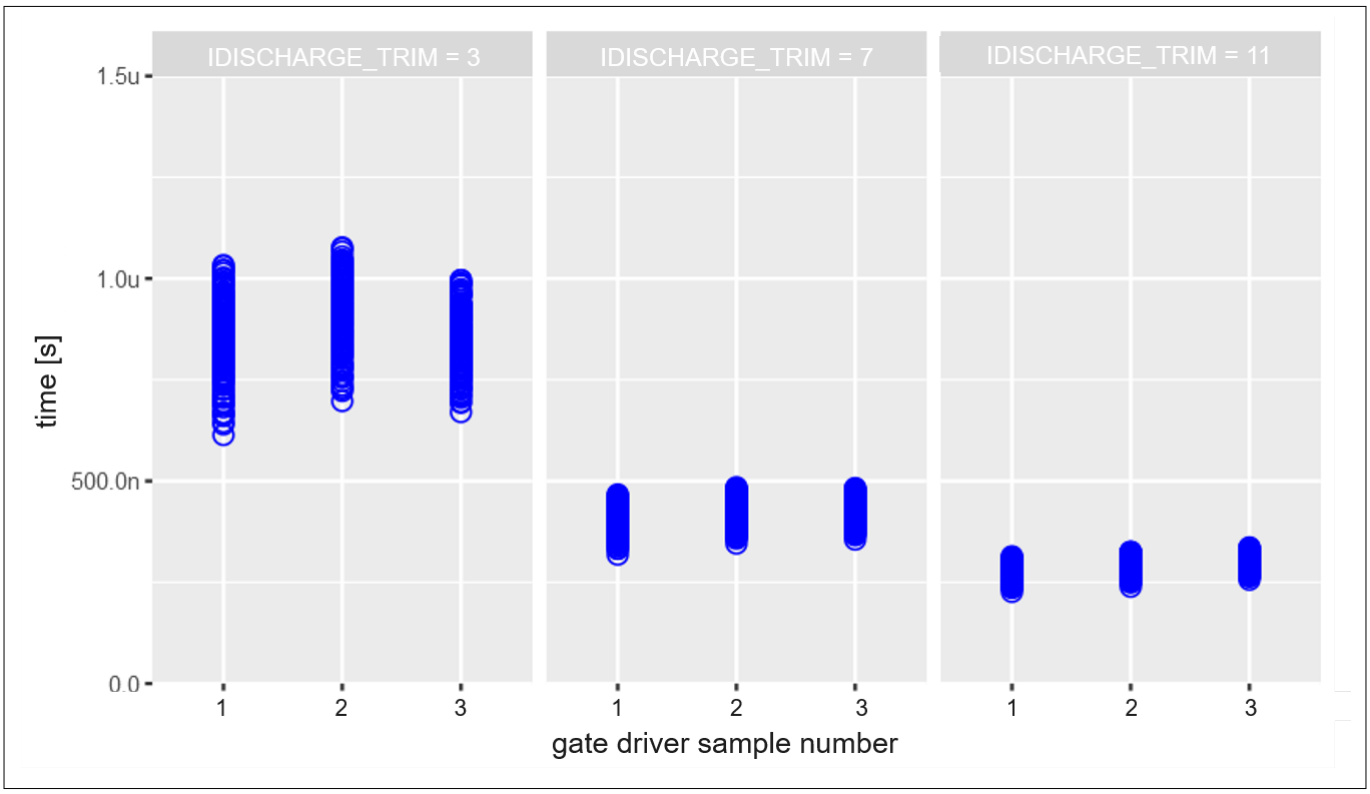

Figure 77 **The plot shows turn OFF delays at different gate discharge current settings. It is measured when 3 gate driver samples are tested with all low-side MOSFETs in a 3-phase bridge.**

3.2.5.2.2 The influence of the MOSFET

To see the influence of low-side MOSFETs on the turn OFF delay, refer to the figure below. The plot shows measured turn OFF delays when a gate driver sample is tested under all Test conditions with all low-side MOSFETs mounted on 7 PCBs in a 3-phase bridge configuration. It is clearly visible from the plot that there is no significant difference in turn OFF delays at any gate discharge current setting. There is a slight difference at lower gate discharge current settings but it is negligible. Therefore, the influence of MOSFETs on the variation of turn OFF delay is insignificant when compared to that of the gate driver.

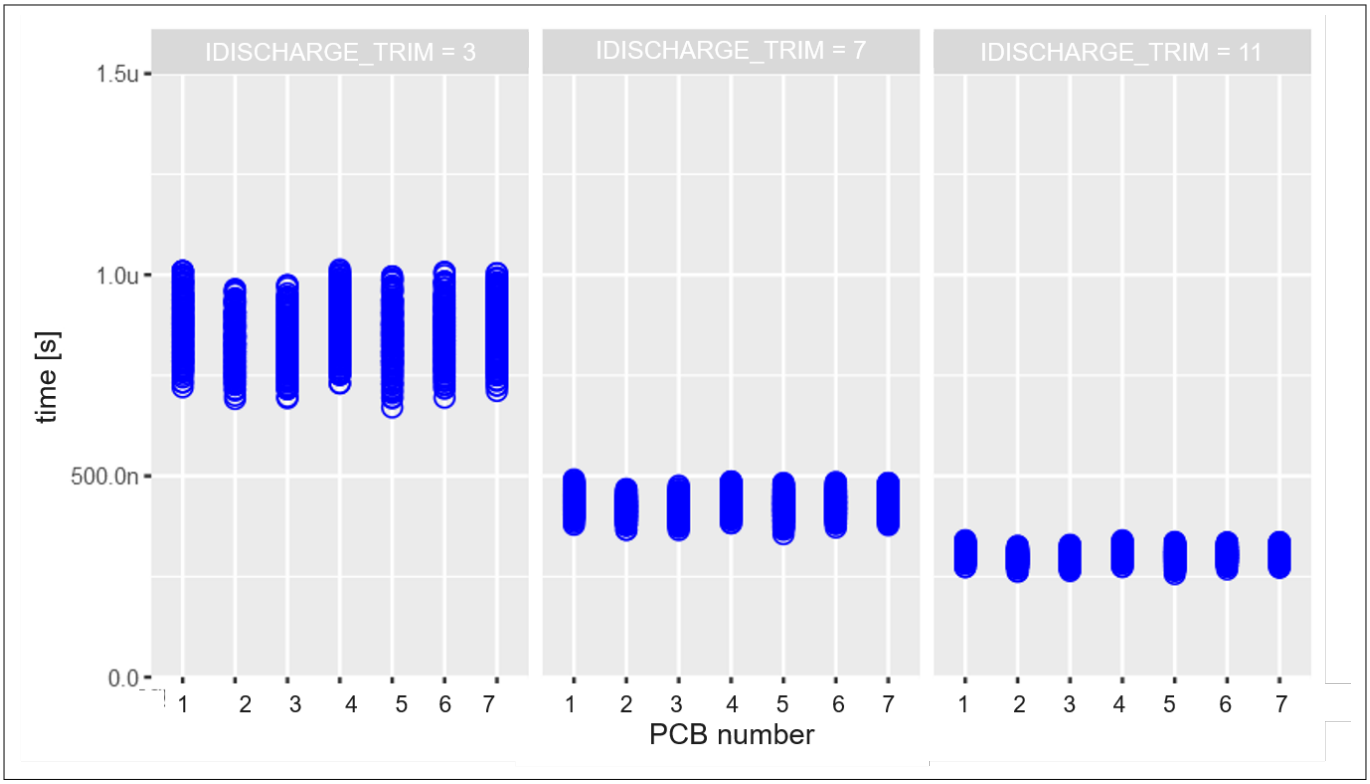

Figure 78 **The plot shows the turn OFF delay at different gate discharge current settings. It is measured when a gate driver sample is tested with all low-side MOSFETs mounted on 7 PCBs in a 3-phase bridge.**

3.2.5.2.3 The influence of supply voltage

The figure below shows the measured turn OFF delay for low-side MOFSETs when a gate driver sample is tested with a MOSFET at 25°C and 30 A load current. The turn OFF delay varies slightly with voltage at medium and higher gate charge current settings, but the change is insignificant. The variation in turn OFF delay with supply voltage increases at lower gate charge current setting. The delta between minimum and maximum turn OFF delay is within 10% of maximum values at lower gate charge current setting.

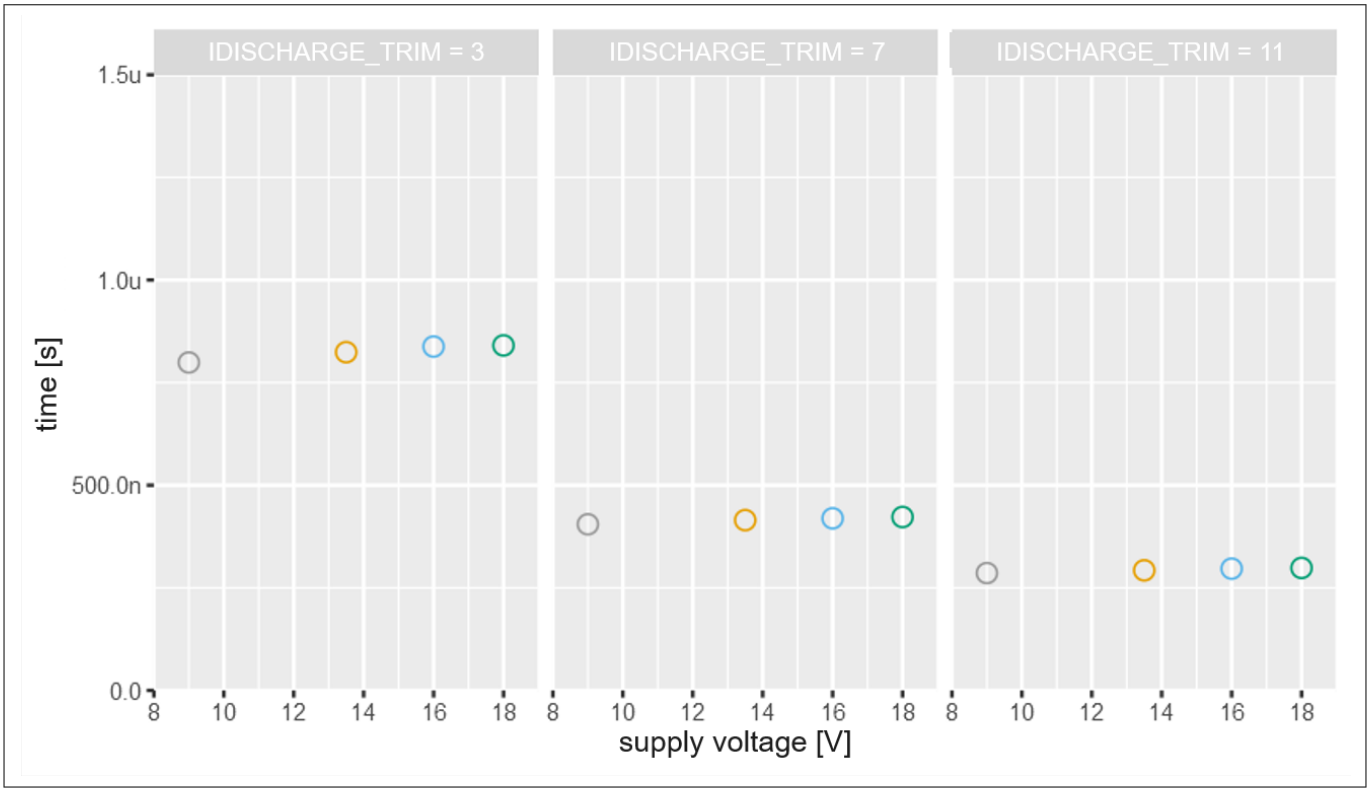

Figure 79 **Turn OFF delay at different supply voltages. The turn OFF delay is measured when a single gate driver is tested with a MOSFET at 25°C and 30 A load current.**

3.2.5.2.4 The influence of temperature

The figure below shows the influence of temperature on measured turn OFF delay at different gate discharge currents. it is measured when a single gate driver is tested with a MOSFET at 13.5 V and 30 A load current. As expected, the turn OFF delay increases with increasing temperature because the threshold voltage of the MOSFET has a negative temperature coefficient.

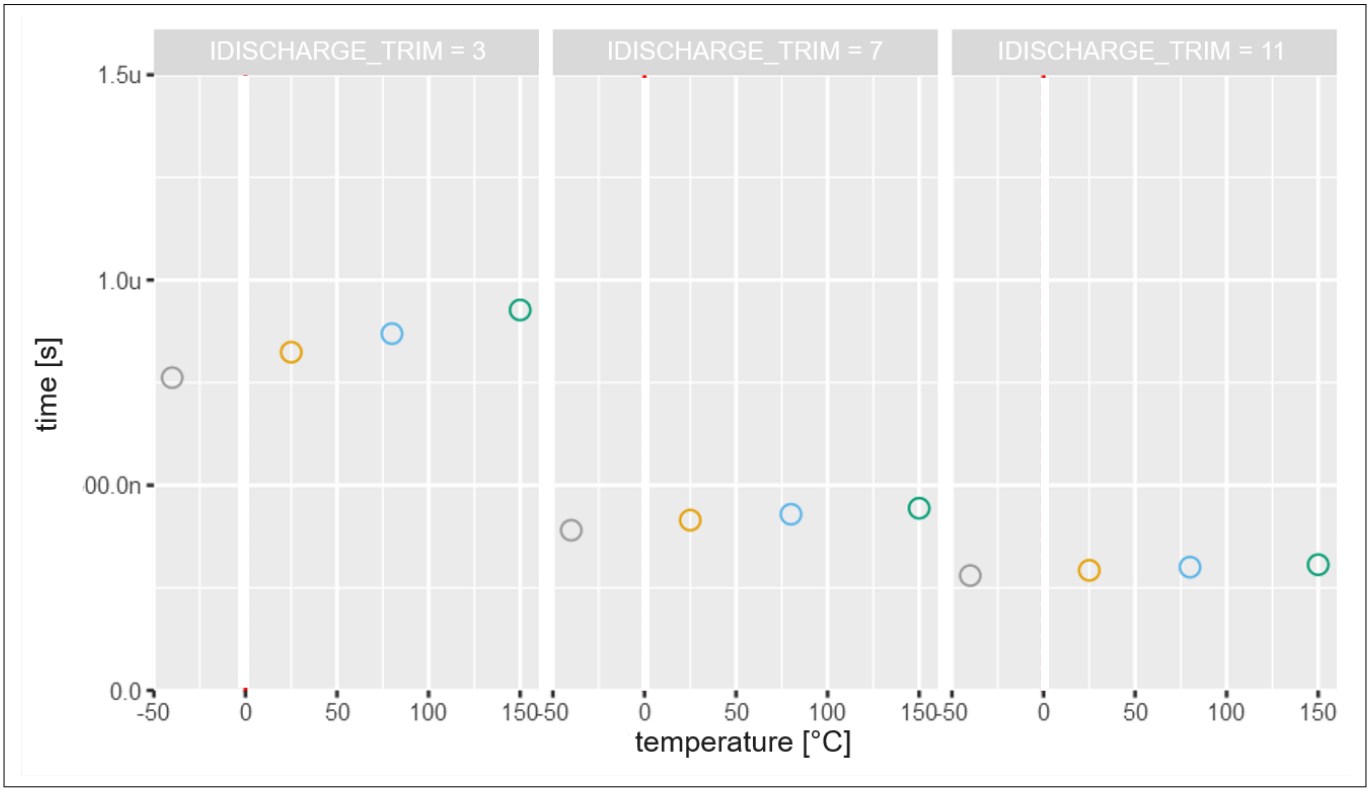

Figure 80 **The plot shows the turn OFF delay for low-side MOSFETs at different gate discharge current settings. It is measured with a gate driver and is tested with a MOSFET at 13.5 V and 25°C temperature**

3.2.5.2.5 The influence of load current

The figure below shows the turn OFF delay for low-side MOSFETs across different load current values. The plot shows the measured turn OFF delay when a gate driver is tested with a MOSFET at 13.5 V supply voltage and 25°C temperature. As expected, the turn OFF delay decreases with increasing load current. However, this influence decreases as the gate charge current setting is increased.

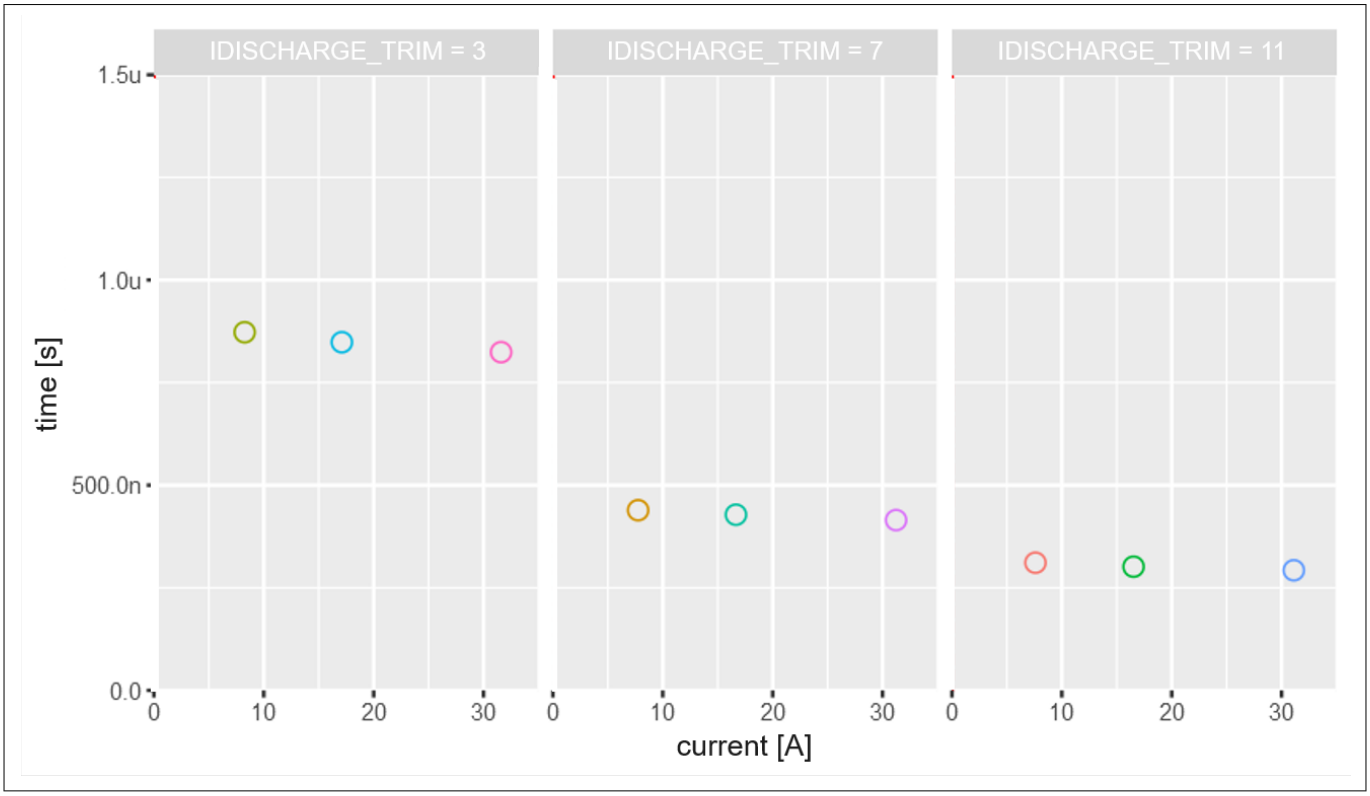

Figure 81 **The plot shows the turn OFF delay for low-side MOSFETs at different load currents. It is measured when a gate driver is tested with a MOSFET at 13.5 V and 25 A load current.**

3.2.6 Low-side MOSFET VDS fall time measurement increase

The figure below shows the drain-to-source voltage of low side MOSFETs. It can be seen that there are two distinctive slopes in the VDS waveform. These two slopes are caused by parasitic inductance at the source of low-side MOSFETs. It is important to understand how low-side MOSFETs operate. When the MOSFET changes state from OFF to ON, the current starts to flow from phase to ground through the low-side MOSFET. Considering the parasitic inductance in the path to ground, the parasitic inductance reacts to the increase in current by inducing a voltage at the source pin of the low-side MOSFET as it can be seen from Figure 83. The amplitude of the voltage is proportional to the rate of change of current. Since VDS voltage is differential voltage, the increase in source voltage impacts its overall shape. The first slope in VDS waveform is dominated by the inductive voltage spike. The real slope of the VDS waveform due to the MOSFET turn ON becomes dominant once the voltage spike at the source pin starts to decay. As a result, the low-side MOSFET VDS fall time calculation gives a higher value.

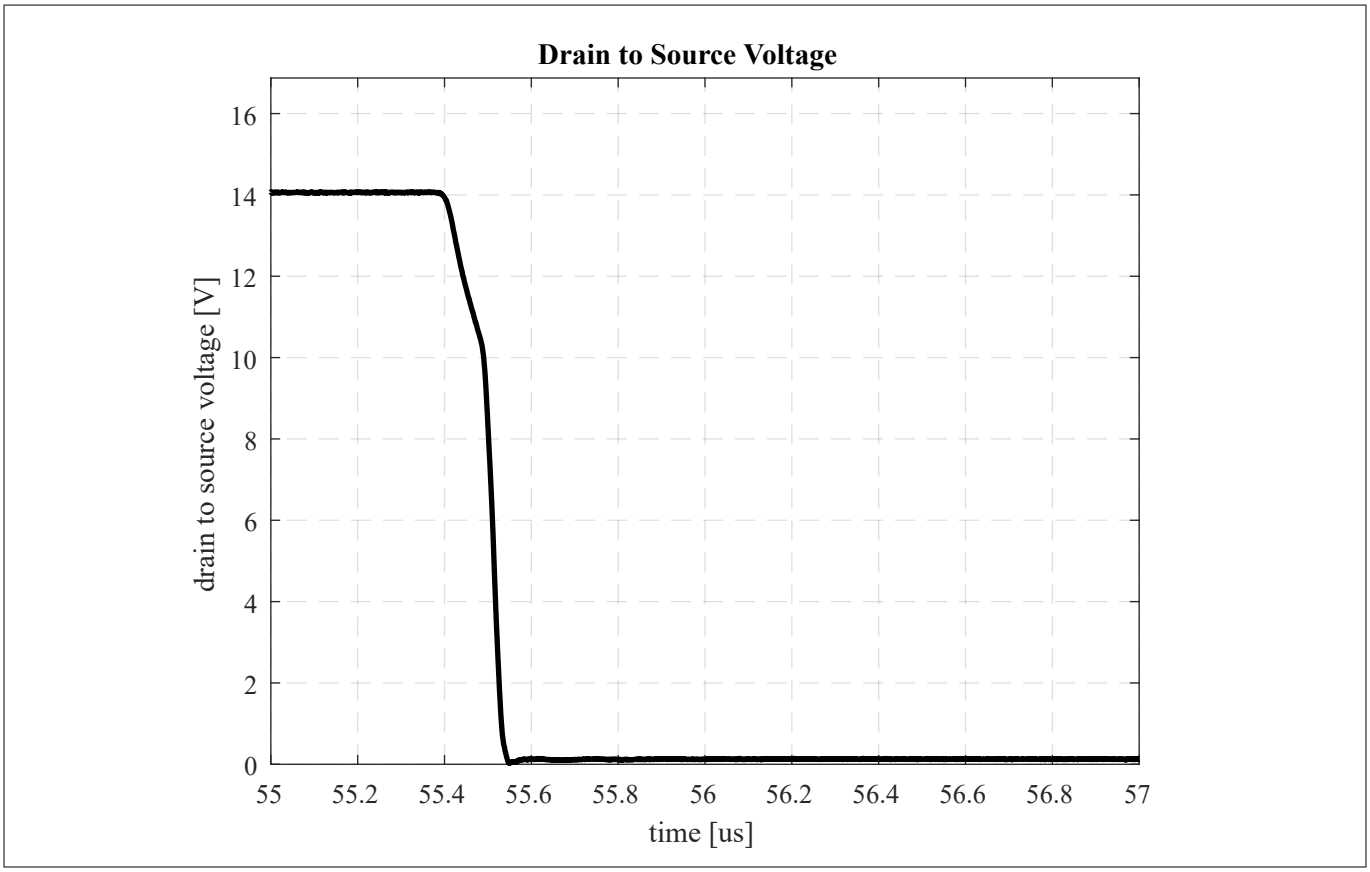

Figure 82 Drain to source voltage of low-side MOSFET

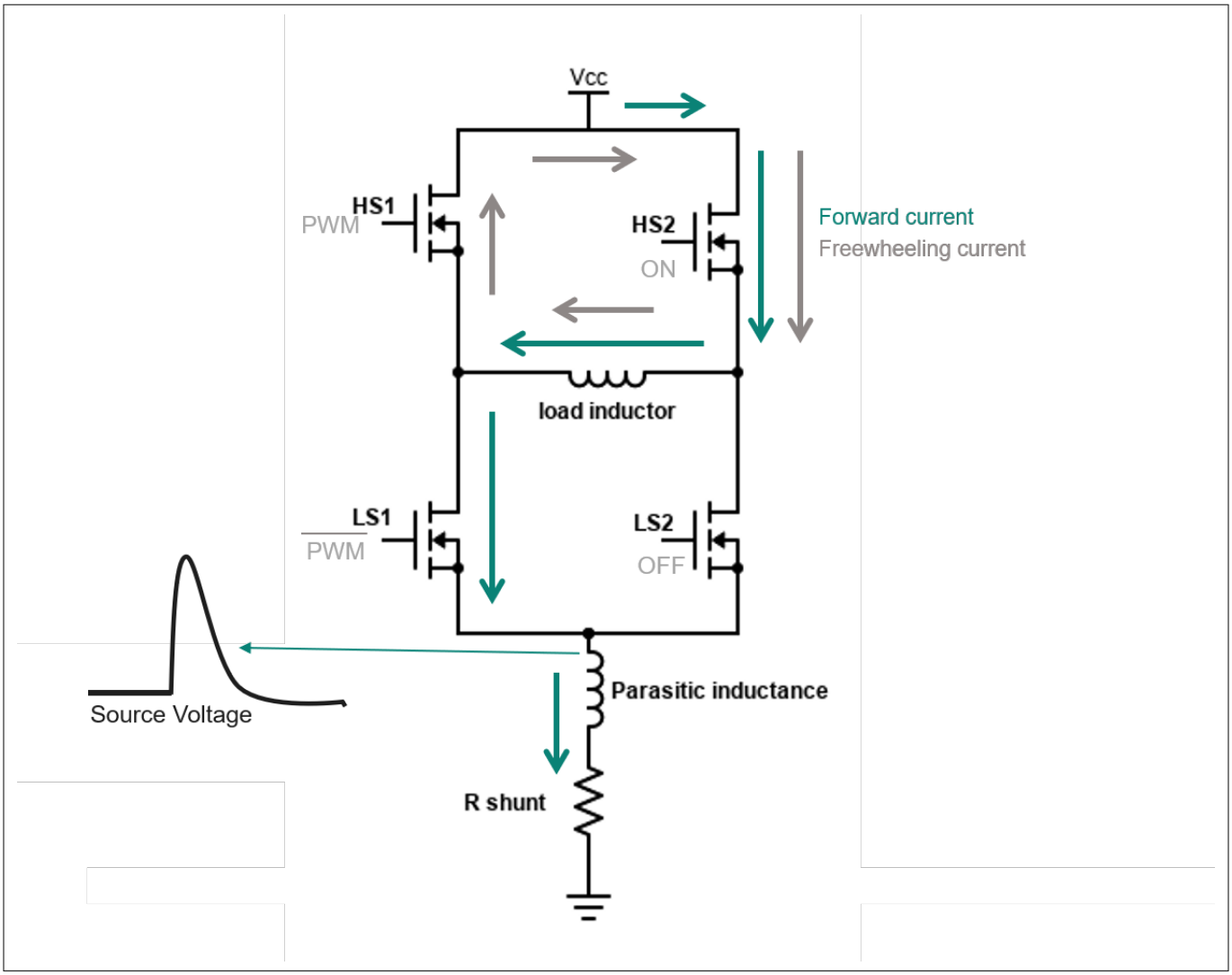

Figure 83 **The schematic shows the parasitic inductance and the voltage transient during the turn ON phase**

3.2.6.1 The influence of supply voltage on low-side MOSFET drain-source voltage waveform

Figure 57 shows the VDS fall time of low-side MOSFETs at various supply voltages when the gate charge setting (11) and load current remain constant (30 A). It can seen from the figure that the VDS fall time measurement window falls into the double slope region if the supply voltage of 9 V and 13.5 V. Consequently it results in longer timing measurements. The VDS fall time for 16 V and 18 V supply are valid in this case because the measurement window is outside the double slope region.

The first slope always has a voltage drop of x v. The 80% threshold for measuring the fall time is dependent on the supply voltage. At 9 V. 20% =1.8 and at 18 V. = 3.6 V therefore the voltage drop due to the first slope is above 1.8 V but below 3.6 V it is only represented in some measurements.

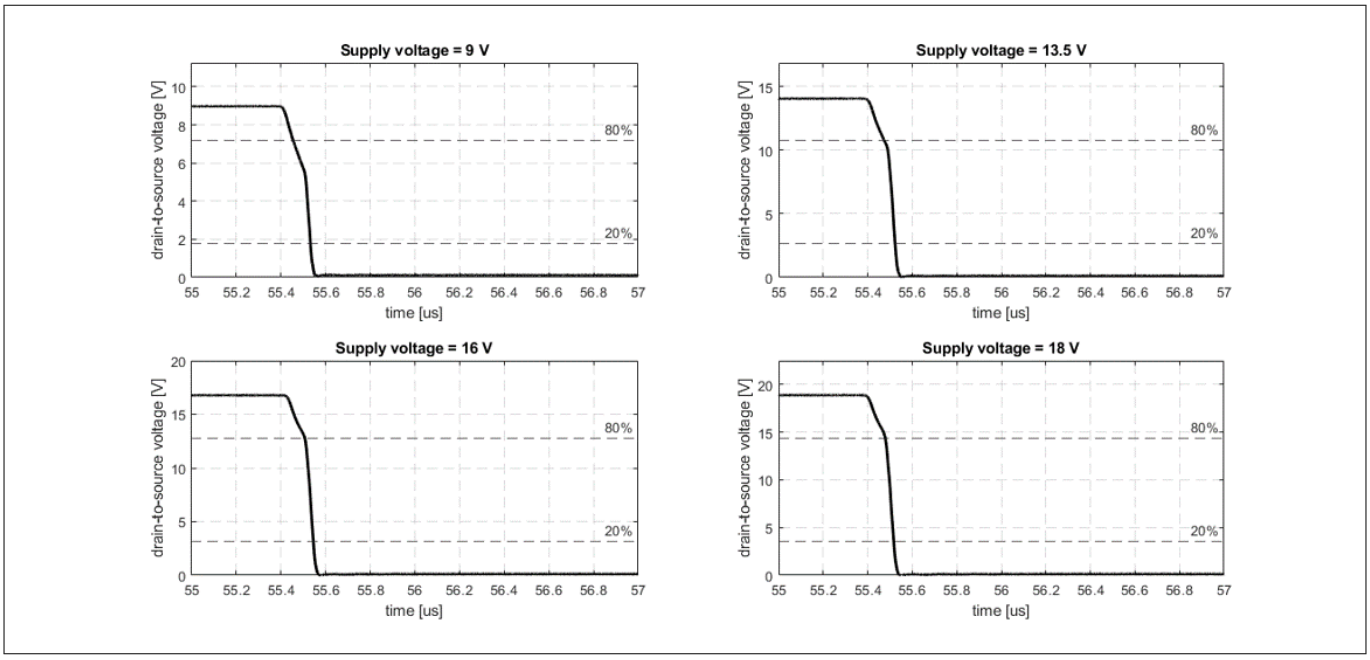

Figure 84 VDS waveform for low-side MOFSET sat different supply voltages, 25°C temperature and 30 A load current

3.2.6.2 The influence of load current on low-side MOSFET drain-source voltage waveform

The plot in Figure 39 shows the VDS waveform for low-side MOSFETs for different load current values when supply voltage and gate charge current are kept constant. The double slope effect on the VDS waveform becomes significant and it also falls in the VDS fall time measurement window when load current is increased to 30 A. Therefore, the measured VDS fall time for low-side MOSFETs is not always the reflection of the actual VDS fall time due to MOSFET switching as can be seen in The influence of the load current.

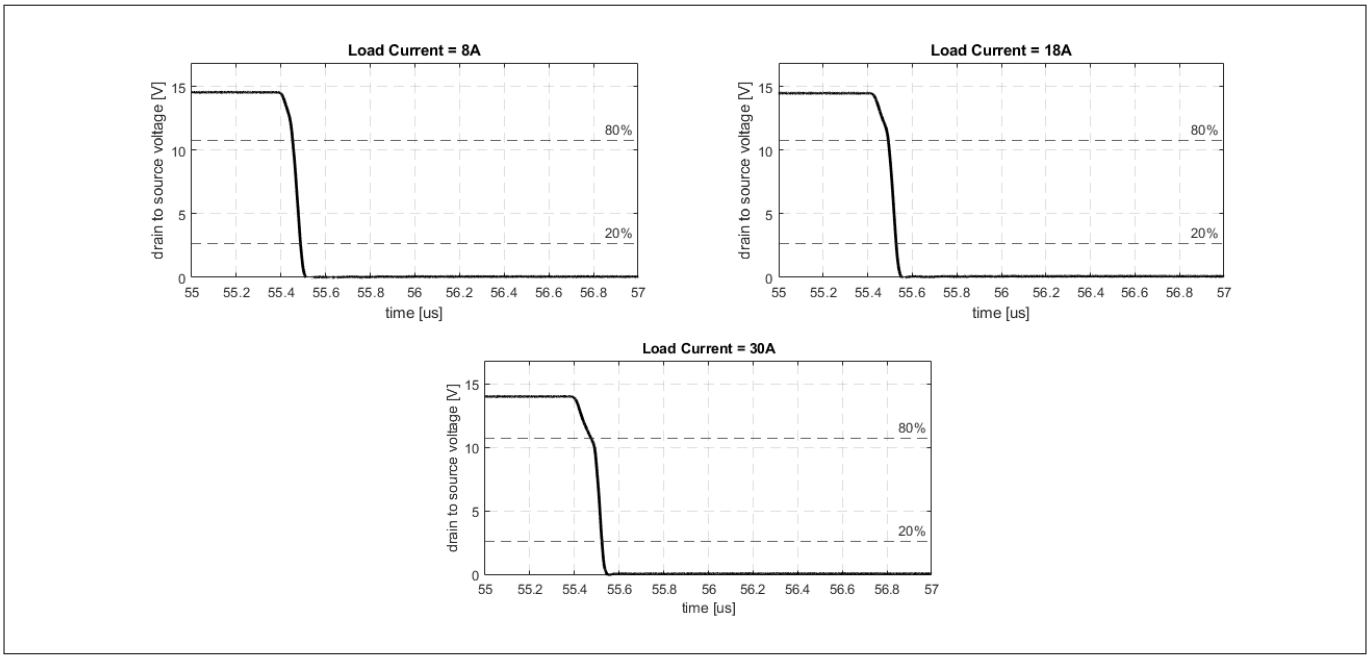

Figure 85 **VDS waveform for low-side MOSFETs at different load current values, 13.5 V supply voltage, and 25°C temperature**

4 The example of the Generic Power Board

4.1 Introduction to the Generic Power Board for 12 V applications

The evaluation board 'Generic Power Board' is made for the easy implementation of an automotive inverter application for controlling fans or pumps driven by BLDC motors. The system is controlled by a MOTIX™ MCU system-on-chip microcontroller with integrated MOSFET drivers in combination with OptiMOS™ 6 leadless MOSFETs.

The inverter design describes a solution for applications for pumps and fans with a capability of up to 400W output power. The solution can be used for similar applications with smaller or equal power consumption. The circuit contains an integrated 3-phase motor control solution. The SoC microcontroller populated to the Generic Power Board is a member of the MOTIX™ MCU family. It combines an Arm® Cortex®-M3 microcontroller with application-specific modules such as an integrated 3-phase MOSFET driver, power supply, and LIN-transceiver. In combination with the OptiMOS™ 6 40V MOSFETs equipped in a PG-TDSON-8 package (SSO8), the system is optimized for a minimum PCB size for this power class. The focus of the demonstrator is to use standard PCB materials and processes.

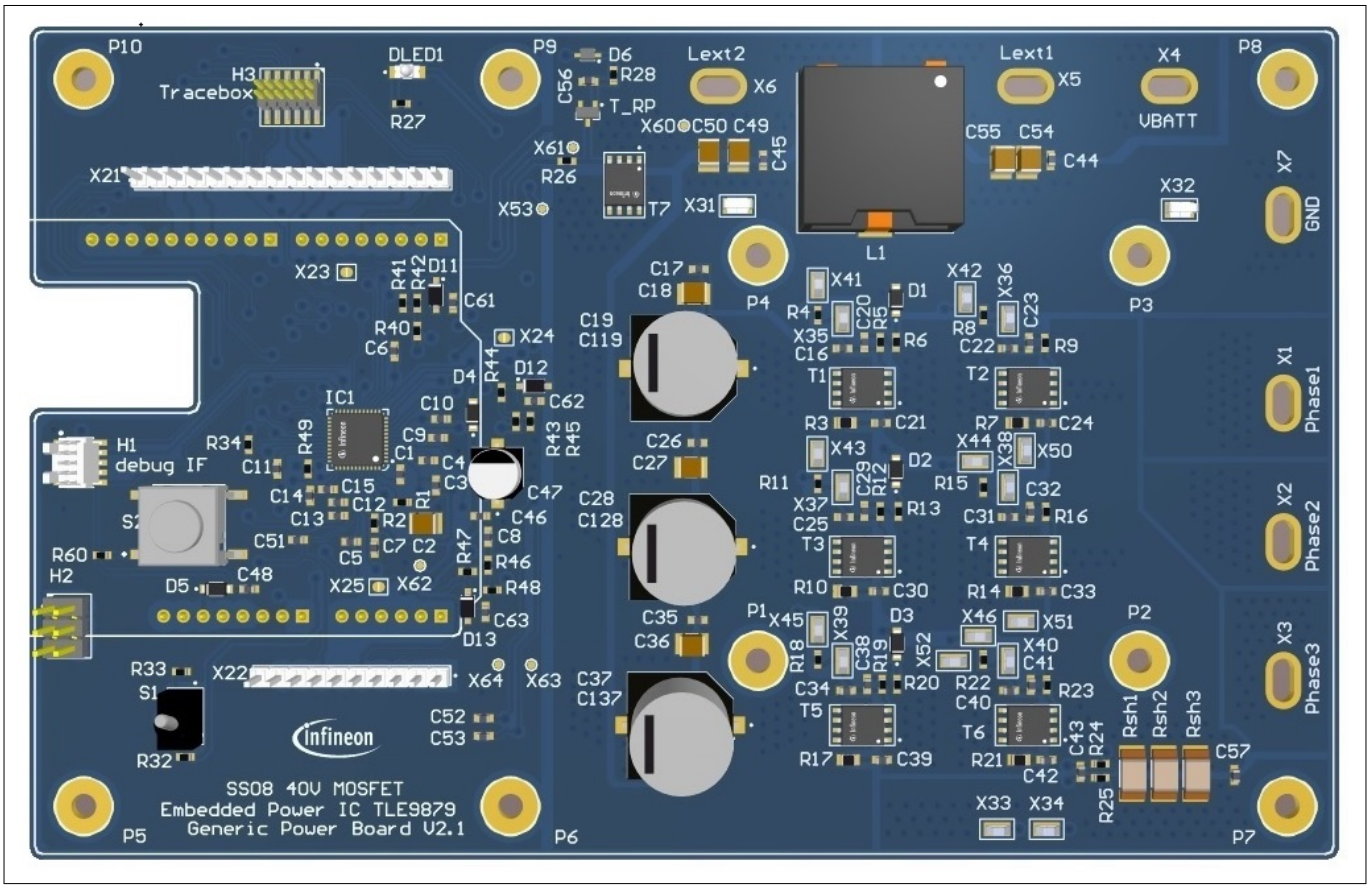

Figure 86 Generic Power Board: Top view design

Purpose of the generic power board

The Generic Power Board provides an inverter solution containing all components to operate a BLDC motor requiring an electric output power to the motor of up to 400W. The components used on the board are selected for the compatibility with each other and tested.

The purpose of the board is to support the customers in rapid development and implementation of inverter prototypes for driving motor loads fulfilling their specific application's requirements. The package incorporates the implementation of the following:

- A suitable motor control algorithm (such as field-oriented control)

- The optimal gate driver configuration (offering a trade-off between possible low power losses and best EMC emissions)
- The most suitable power MOSFET switches (needed in B6-bridge to drive a 3-phase motor)

In addition to the hardware board, a software toolchain is provided.

The table below gives an overview of maximum ratings of parameters related to the board. The design specification relates to the components used on the board and the design considerations. In the case that the values (operational range and maximum rating) in the datasheets have been updated, the datasheet values apply.

Design Specifications

Parameter	Symbol	Values			Unit	Comment
		Min.	Typ.	Max.		
System Parameters						
Input voltage	V_{IN}	-0.3	12	40	V	P_1.1.1 (TLE9879QXA40)
Functional input voltage	V_{IN}	7	12	18	V	Specified for Design
Output current peak	I_{OUT}	-	-	44	A	Peak current (<10 s), air cooling attached (>1.3 m/s)
Output current continous	I_{OUT}	-	20	35	A	Specified for Design
Hall Sensor Inputs	V_{HALL}	-0.3	5	5.5	V	Specification related to GPIO Port 0,1
LIN interface	V_{LIN}	-28	12	40	V	P_1.1.7 (TLE9879QXA40)
ADC Inputs	V_{ADC}	-0.3	5	5.5	V	Specification related to GPIO Port 2
Phase 1,2,3	V_{SH}	-8.0	12	48	V	P_1.1.11 (TLE9879QXA40)
Thermal						
Operating temperature	T_A	-40	25	105	°C	Specified for Design
Electromagnetic Compatibility						
Conducted emissions				Class 2		CISPR25, 150 kHz -108 MHz
Mechanical Specification						
Dimensions	168 mm x 107 mm x 15 mm (L x W x H) [1]					
PCB	6-layer, top/bottom layer 2 oz, inner layers 1 oz, standard FR4, 168mm x 107 mm (L x W), thickness 1.6 mm					

Figure 87 Design specifications

Functional blocks on the board

An overview of the functional components is given in the figure below.

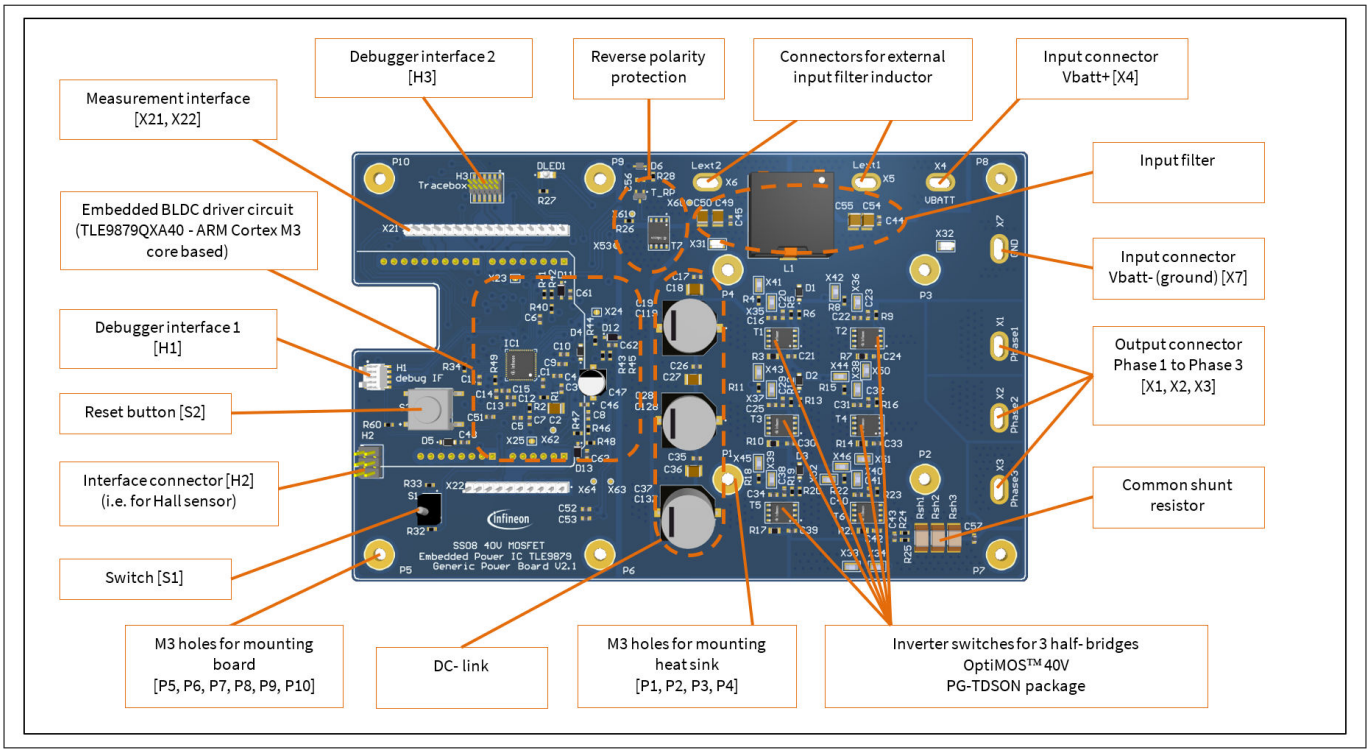

Figure 88 Generic Power Board: Overview

System design

The circuit diagram of the Generic Power Board consists of the following functional groups and partial circuit:

- The low-pass input filter on the board is designed as a PI filter
- The board is equipped with a reverse polarity protection, which prevents damage to the board in case the supply voltage is incorrectly connected to the ground connector. There are separate reverse polarity protection mechanisms for the B6-bridge and the controller circuit
- The DC-link aims to reduce the voltage ripple at the supply voltage line to the inverter. To do this, electrolytic capacitors are used to provide large capacitance to each half-bridge leg. The electrolytic capacitors are complemented by ceramic capacitors providing a very low equivalent series resistance (ESR)
- The three half bridge legs of the B6-bridge use six 40 V OptiMOS ™ 6 MOSFETs in an SSO8 package. In parallel to each MOSFET drain-source, there is a snubber circuit. The snubbers consist of a series resistor ceramic capacitor circuit. The snubber helps to reduce possible oscillation of the drain-source voltage during MOSFET switching. Its values are specified in Schematics
- The shunt resistor is made from a parallel connection of up to three shunt resistors (package type 2512). Depending on the application, you can configure the resistive value to consider:
  - Power loss in the shunt resistor resulting from high load currents
  - Voltage drop across the shunt resistor for the current sense amplifier (CSA) measurement
- The gate driver circuits between the outputs of the gate drivers and MOSFET gates provide test points to measure the charge and discharge current into and out of the gates. Furthermore, you can add external capacitors between gate-source and gate-drain at each B6-bridge MOSFET (though this changes the switching characteristics)
- The controller circuit is based on the TLE9879 device. The MOTIX™ MCU combines a 3-phase bridge driver with a 32-bit Cortex®-M3 core and peripherals such as timer modules, ADCs, double stage charge pump, several voltage regulators, external sensor supply, RAM, flash memory, and a LIN communication module. The IC is capable of performing advanced motor control, such as sensorless FOC with configurable current-controlled gate driving
- If there are requirements for high output power, and depending on the environmental conditions, you can connect a heat sink to the bottom side of the PCB to obtain better cooling of the MOSFETs in the B6-bridge

For a detailed description of all functional groups, refer to https://www.infineon.com/cms/en/product/evaluation-boards/mos_generic_pow_board/.

Layout description

The PCB is designed as a 6-layer, standard FR4 board. The bottom side of the PCB is almost free of components so that you can assemble a heat sink to the board for better cooling of the power switches. The configuration of the PCB stack and the layout printing of the six layers are shown in https://www.infineon.com/cms/en/product/evaluation-boards/mos_generic_pow_board/.

4.2 EMC for various switching timings

This section describes the EMC peak and average emissions of the generic power board for slow-, medium-, and fast-switching. The EMC emission is a result of the PCBs characteristics and the switching time. As described in Configuration-dependent switching behavioreach of the 6 MOSFETs in one B6-brigde generated a different switching time. The fastest switching time will be the dominant one in the generation the of EMC spectrum.

EMC characteristics for a slow-switching configuration

The two figures below show the typical EMC peak and average spectrums of the Generic Power Board for the slow-switching configuration. It was tested at room temperature, 13.5 V supply and 10 A of peak load current at the motor in sensorless FOC control. With this configuration, the board reaches class 4 in peak measurement and class 3 in average measurement according to the International Special Committee on Radio Interference (CISPR).

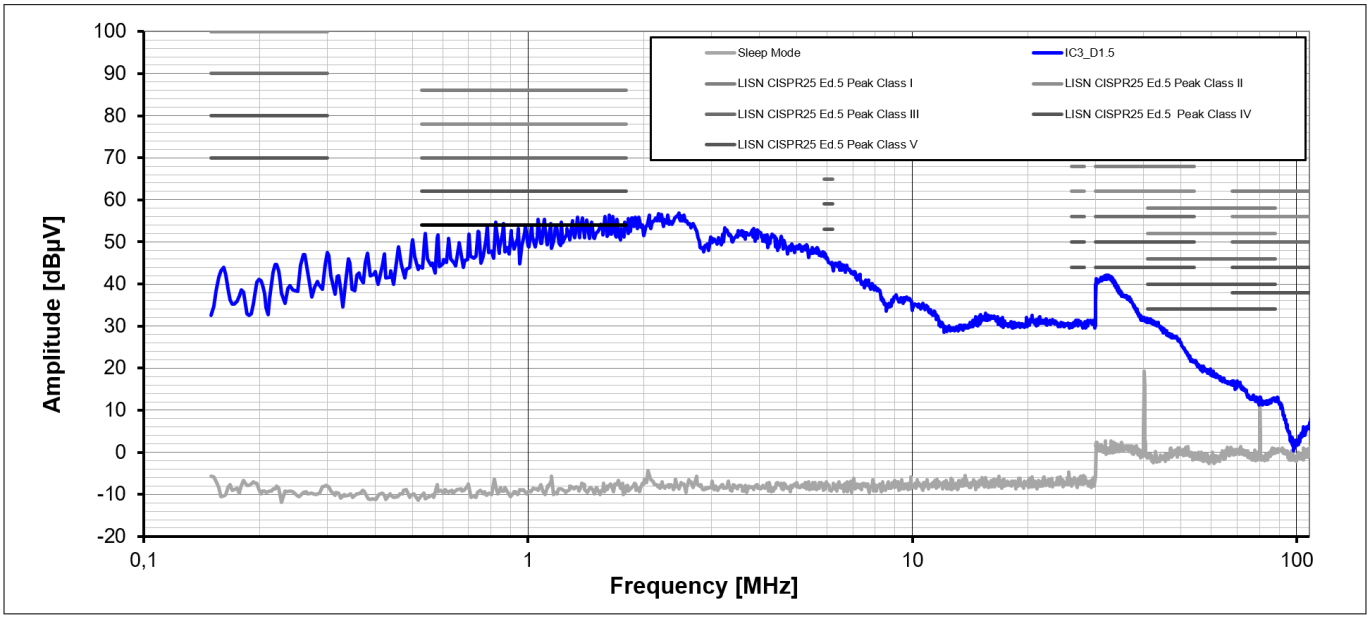

Figure 89 EMC peak emission for a slow-switching configuration

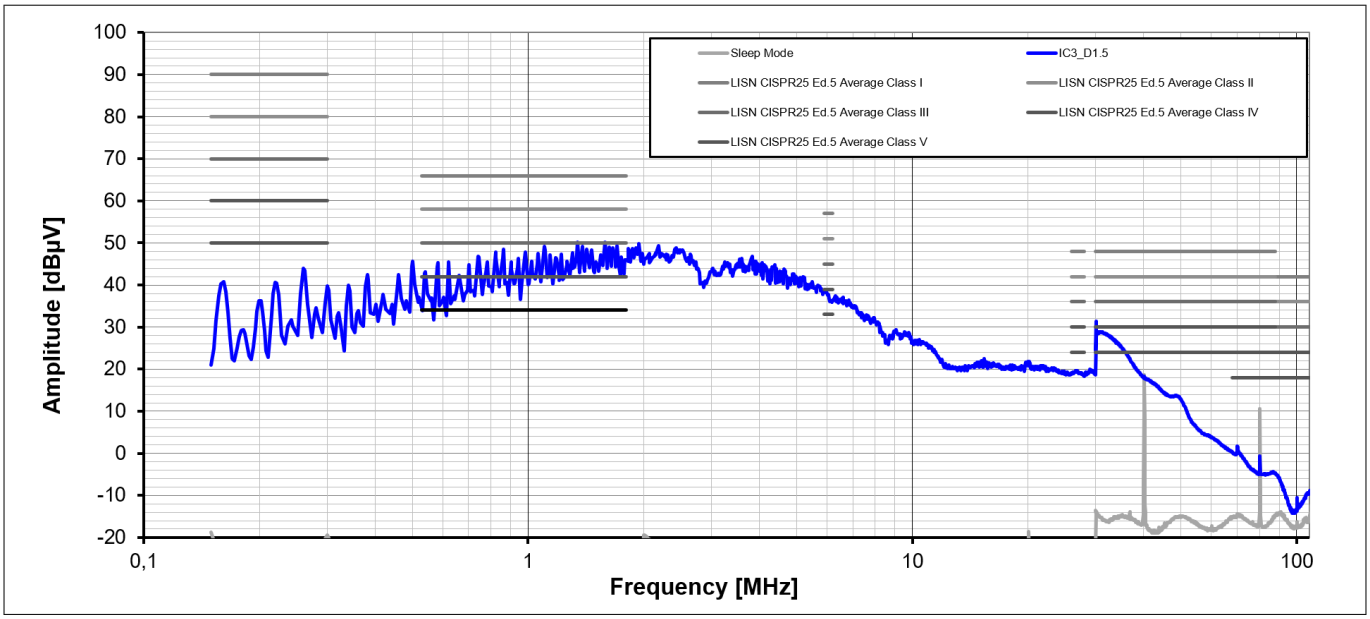

Figure 90 EMC average emission for a slow-switching configuration

EMC characteristics for a medium-switching configuration

The two figures below show the typical EMC peak and average spectrums of the Generic Power Board for the medium-switching configuration. It was tested at room temperature, 13.5 V supply and 10 A of load current at the motor. The board reaches CISPR class 4 in peak measurement and class 3 in average measurement with this configuration.

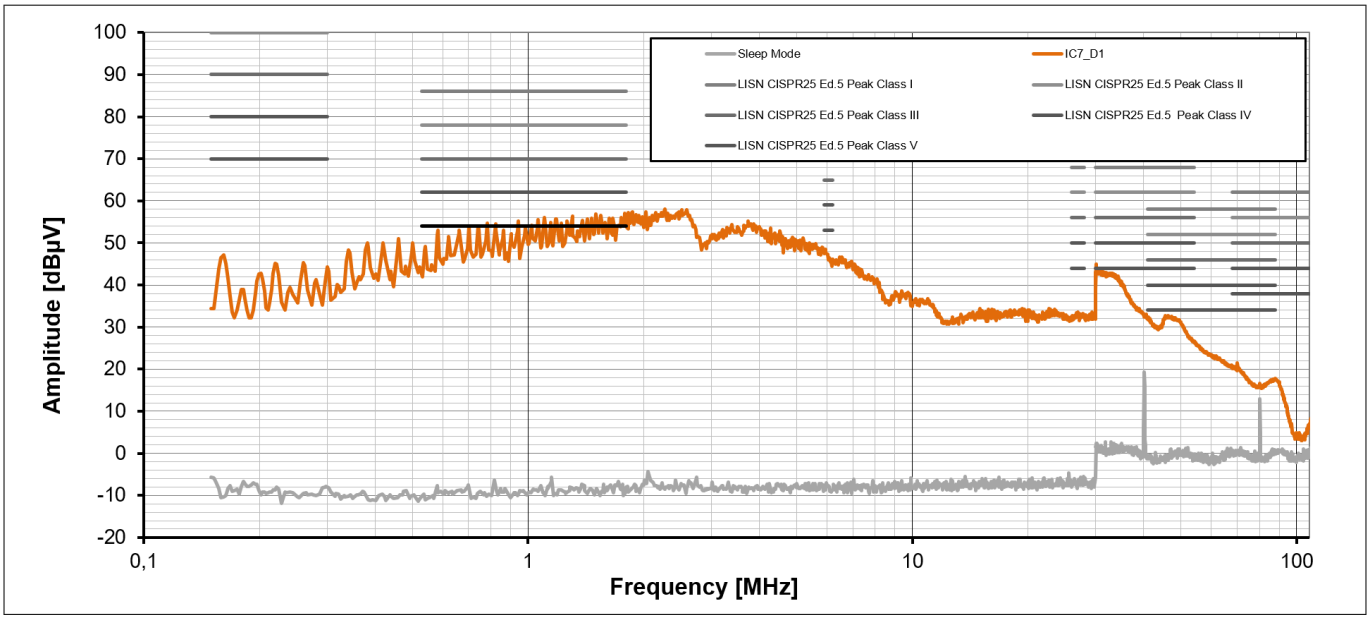

Figure 91 EMC peak emission for medium switching configuration

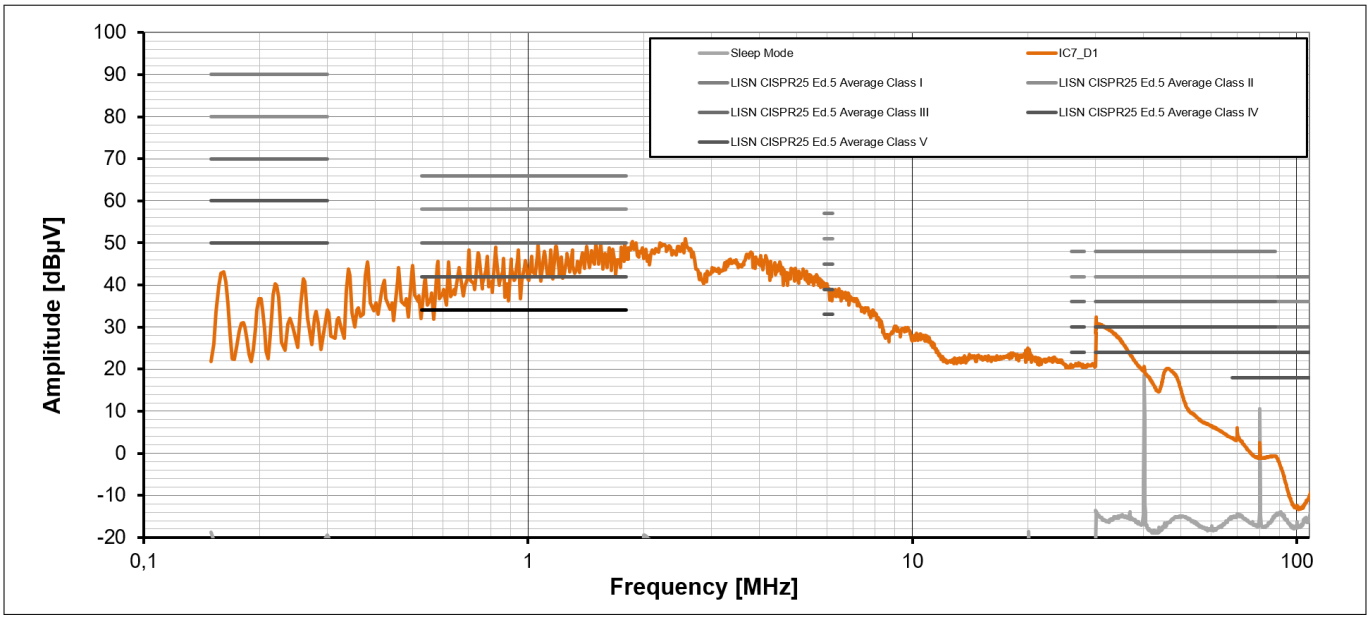

Figure 92 EMC average emission for medium switching configuration

EMC characteristics of fast switching configuration

The two figures below show the typical EMC peak and average spectrums of the Generic Power Board for the fast-switching configuration. It was tested at room temperature, 13.5 V supply and 10 A of load current at the motor. The board reaches CISPR class 4 in peak measurement and class 2 in average measurement with this configuration.

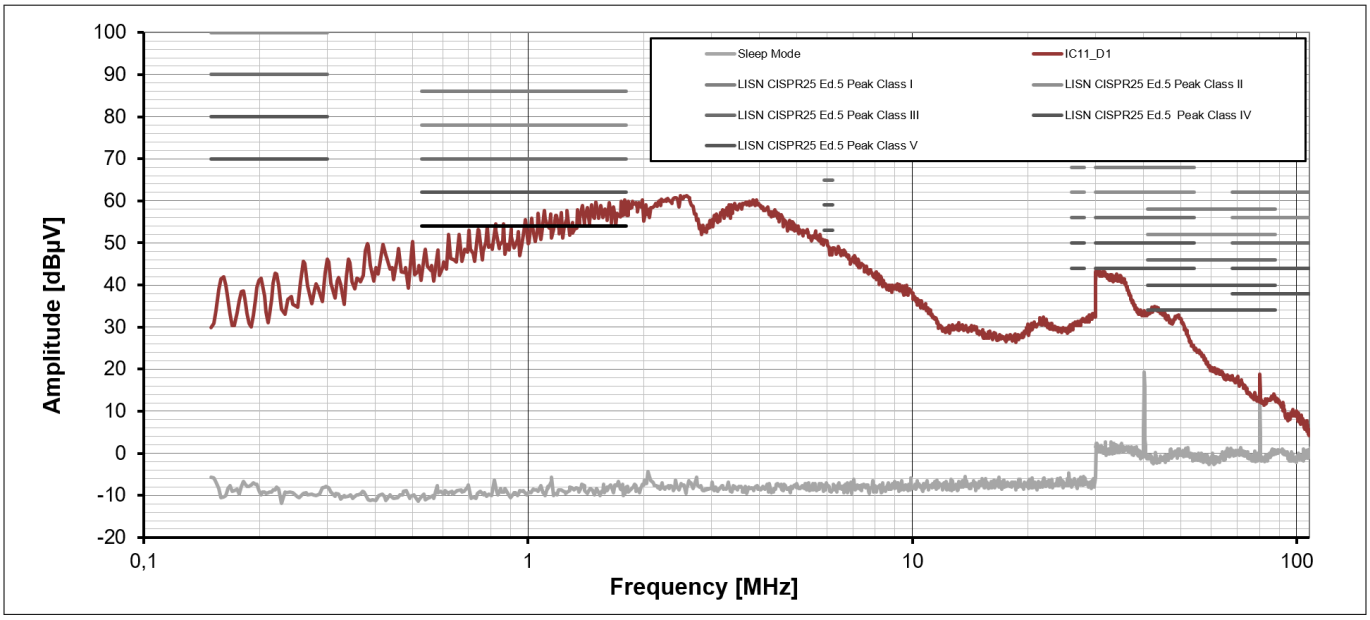

Figure 93 EMC peak emission for fast switching configuration

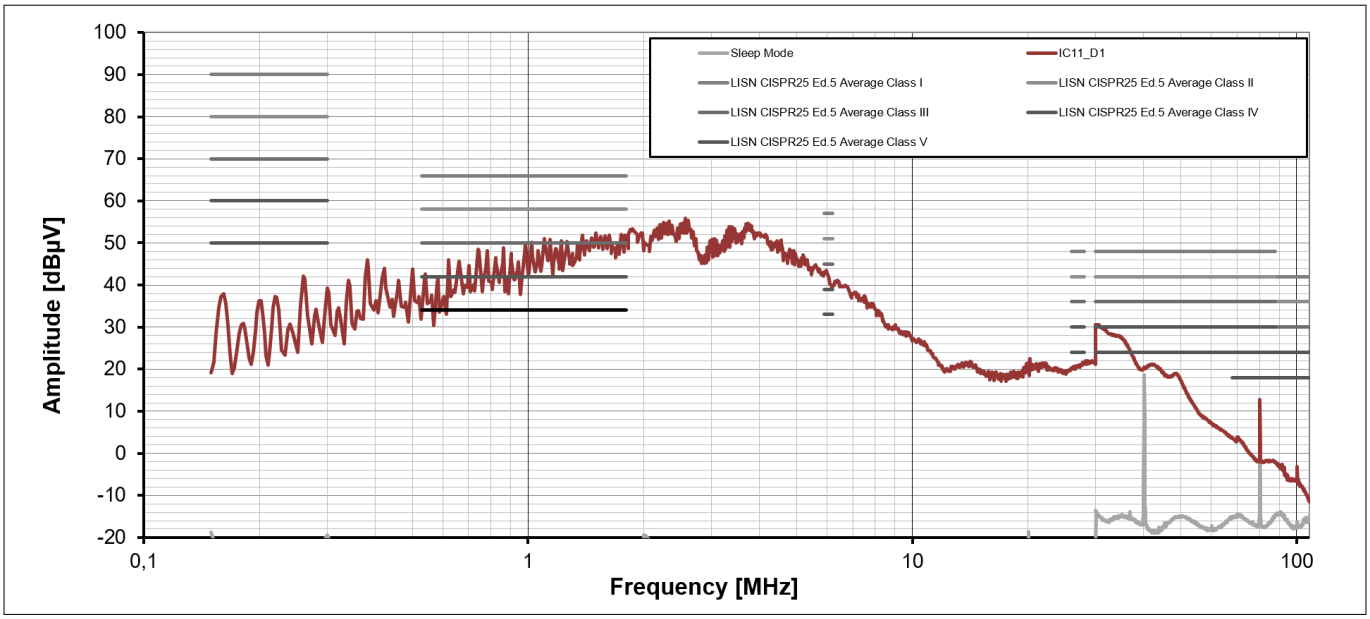

Figure 94 EMC average emission for a fast-switching configuration

Overall, the results show that there is a potential saving in EMC emissions of up to x dBµV between the fast- and slow-switching configuration. Nevertheless, this is only the case for a specific frequency range.

Comparison of slow-, medium- and fast-switching in peak and average EMC spectrums

The figures below Figure 95 and Figure 96 show both peak and average emission overlays of slow-, medium- and fast-switching. You can see that for both peak and average emissions, a saving of up to 6 dBµV can be achieved by jumping from medium- to slow-switching time. Going from fast- to medium-switching time no longer generates any significant improvement. This confirms what you can see in the rise and fall timings in Configuration-dependent switching behavior. Going from a fast-switching configuration has only minor influence on the overall switching timing in comparison to going from medium- to slow-switching time.

Generally you can see that changing the switching times does not have an effect on the full frequency spectrum but only on a specific frequency range. Looking at the EMC results, it is visible that the effect of switching time becomes mainly visible between 1 MHz and 6 MHz

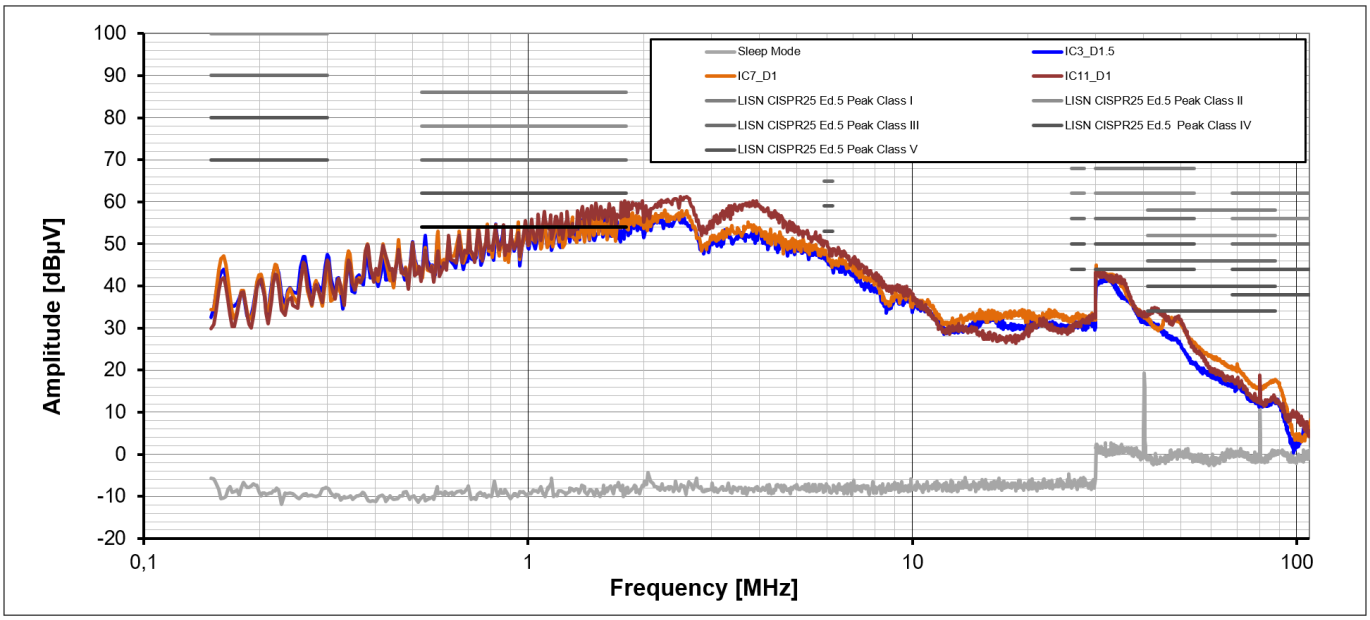

Figure 95 EMC peak emission overlay of configurations

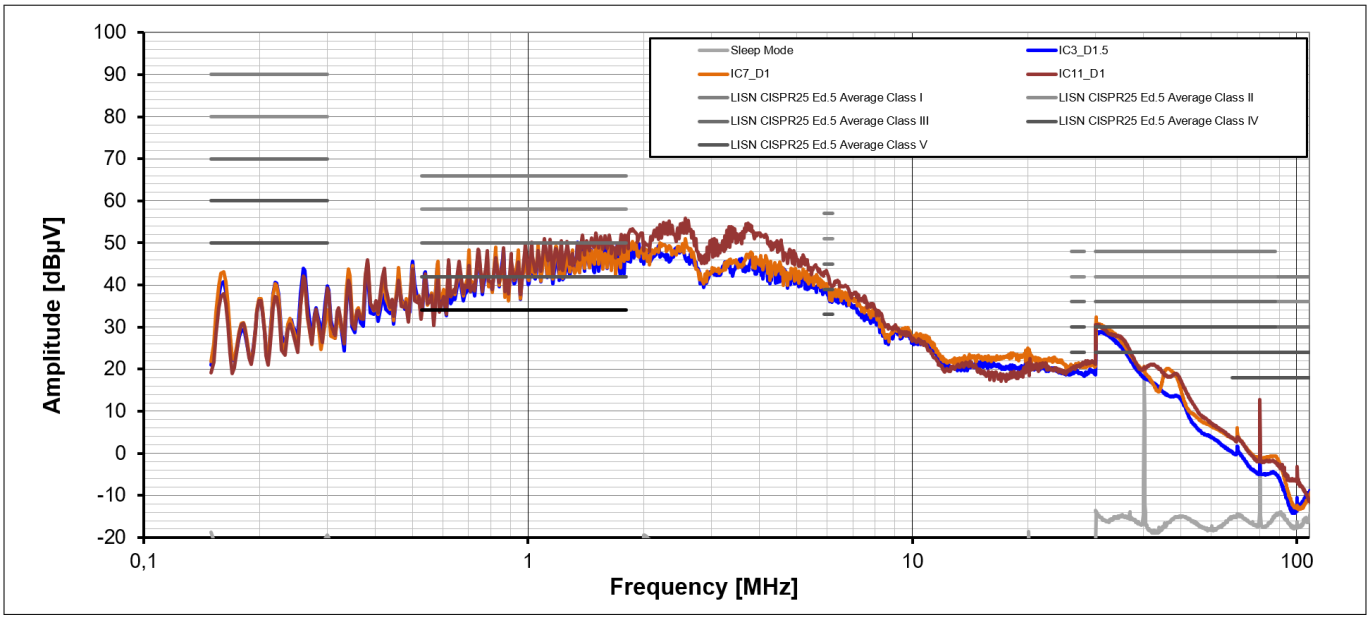

Figure 96 EMC average emission overlay of configurations

On every EMC emission diagram, a jump is visible at 30 MHz. On one hand, this is due to the transition of the measurement equipment from one frequency band to another. This alone results in an increase of 12 dBµV. This can also be observed in the sleep mode capture which is visible in light gray in each of the captures. In addition to the 12 dBµV jump, there is also a small increase in EMC visible slightly below and above 30 MHz, which adds to the spectrum.

4.3 Power dissipation

The power dissipation performance described in this chapter is based on the power dissipation that is generated in the B6-bridge for the switching timings as described in Characterization.

Identifying power dissipation during PWM (conductive losses, switching losses, and active/passive freewheeling losses)

In one half bridge, there is always one active and one freewheeling MOSFET, which alternates based on the direction of the current through the respective phase. During operation in the space vector modulation scheme, both active and freewheeling MOSFETs are always turned on and off once per duty cycle. This results in the MOSFETs having an OFF state, ON state, and two switching transitions, all of which together contribute differently to the power loss of the overall PWM cycle. The figures below show which power losses are generated and when for both the active and the freewheeling MOSFETs.

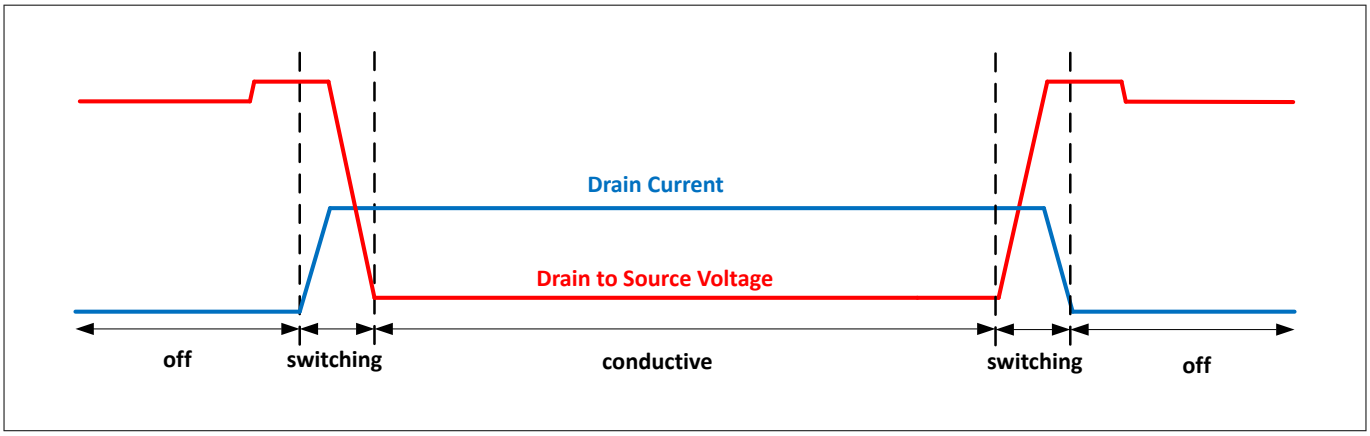

Figure 97 Power losses in the active MOSFET during PWM

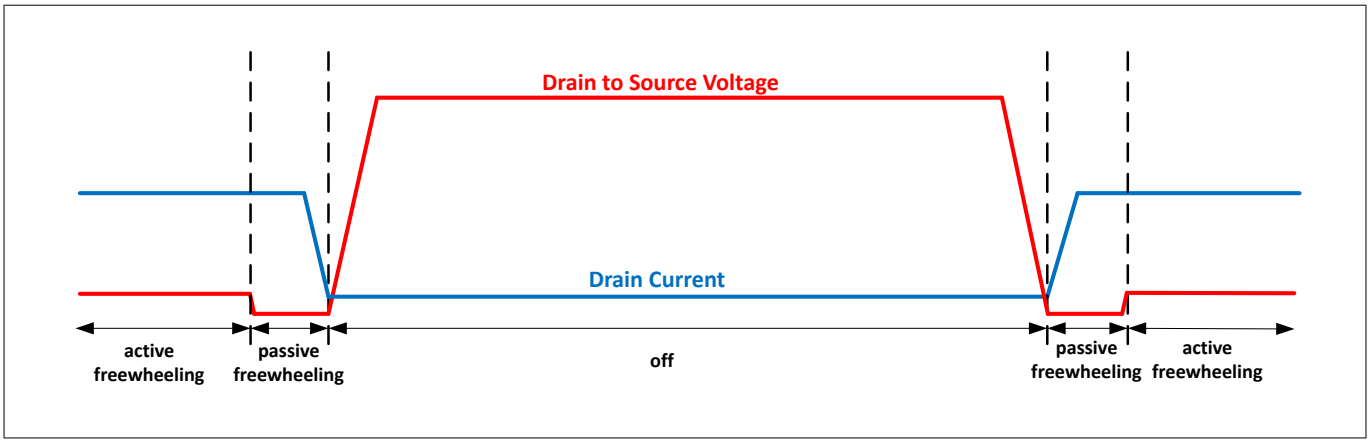

Figure 98 Power losses in Freewheeling MOSFET during PWM

Power dissipation depending on switching timings

As described in the previous paragraph, overall power-losses in each MOSFET are generated by a combination of switching and conductive power-loss. The ratio between these two kinds of power loss depends on two main parameters. One is the switching time, which defines the switching loss, and the other is the $R_{DS(on)}$ of the MOSFET, which defines the conductive loss during the ON state of the MOSFET. This conductive loss is also dependent on the junction temperature of the MOSFETs. The cooler the junction temperature, the lower the conductive loss. In the analysis below, the junction temperature is considered to be fixed at 25°C. The figure below shows the cumulative power loss generated during one PWM period for the active and freewheeling MOSFETs. The freewheeling starts and ends with a horizontal line when the MOSFET is OFF. The active MOSFET starts and ends with a slope when the MOSFET is conducting. In between, a rapid jump in accumulated power loss is visible. These two jumps represent the switching losses during turn ON and turn OFF for the active MOSFET and the passive freewheeling for the freewheeling MOSFET. In between, there is a continuous increase due to the conductive loss during ON-time of the freewheeling MOSFET and a plateau in the active MOSFET because it is OFF.

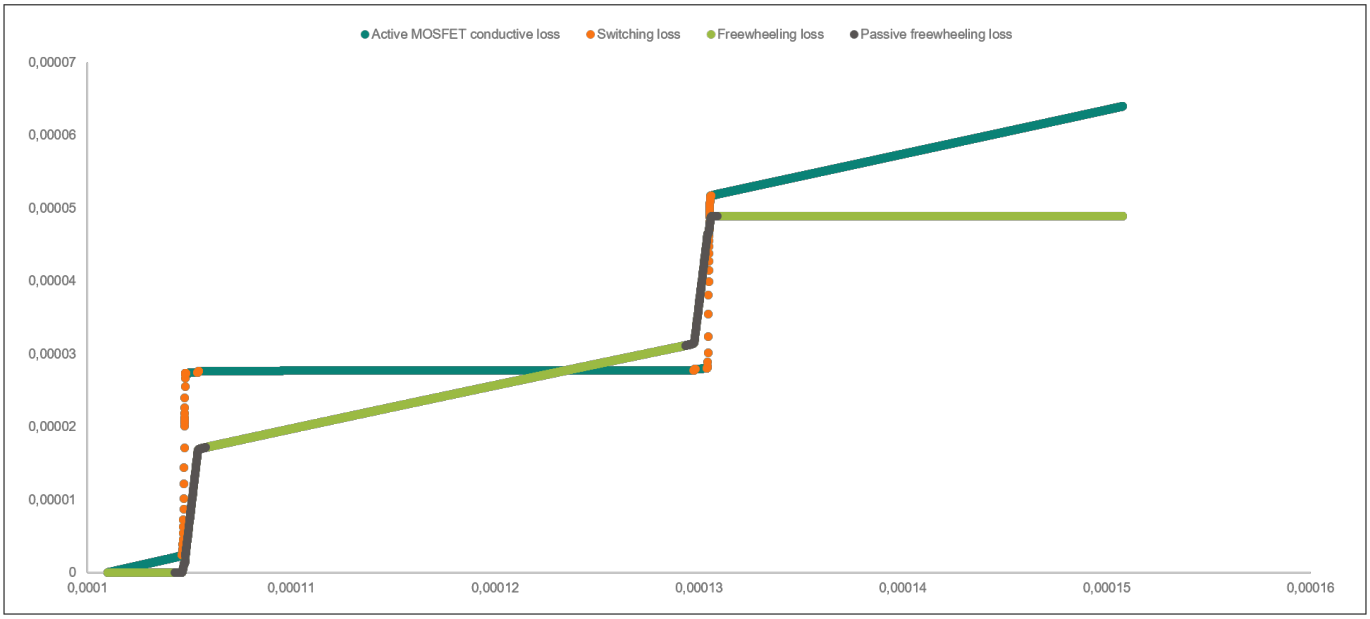

Figure 99 Cumulative power loss at a medium-switching configuration for 1mΩ MOSFET

While turning a motor, the duty-cycle of the PWM is changing continuously. For simplicity, and to enable comparability, these descriptions are based on an average duty-cycle of 50%.

The figure below shows for a 1mΩ MOSFET at 25°C, 13.5 V supply voltage and 30 A load current how the power-loss increases when the switching time increases due to a smaller gate current being used. It is visible that due

to the 50% duty cycle, the conductive loss of active and active freewheeling MOSFET conditions are very similar. Additionally, it is visible that due to the low $R_{DS(on)}$, the switching and passive freewheeling losses are more significant than the conductive losses. Finally, it is visible that changing the gate charge current influences the switching and diode losses only.

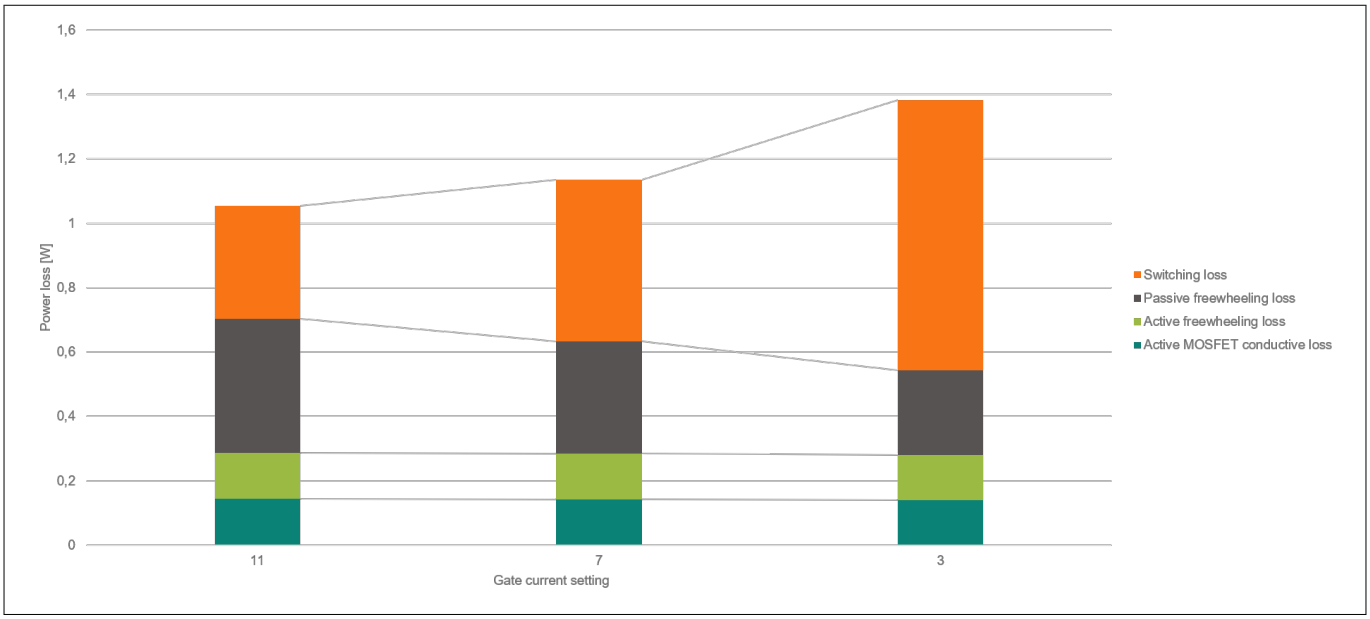

Figure 100 Power dissipation for various switching timings at 30 A, 13.5 V and 25°C

Thermal behavior of the PCB

The previous section describes how power-loss is generated inside of the MOSFET during operation. Equally important is how to dissipate the heat generated by the power-loss. The more efficiently the heat is dissipated away from the MOSFET and the PCB, the lower the settling temperature of the MOSFET.

This section shows how two different approaches on the same PCB give very different results in the heat distribution and absolute settling temperature. It shows a thermal simulation for the Generic Power Board for the following conditions:

- Load current = 21.2 A (rms) which is equivalent to 30 A (peak)
- Power loss at each B6-bridge MOSFET = 0.83 W [1)]
- Power loss at reverse polarity MOSFET = 0.33 W [2)]
- PWM frequency = 20kHz
- Supply voltage = 13.5 V
- Thermal interface material (TIM) = 250µm DOWSIL™ TC-4060

Figure 101 shows the horizontal heat distribution for the generic power board without a heat sink. Figure 102 shows the same simulation with a heat sink added to the bottom of the PCB. First of all, you can see that on the first figure, the main heat is visible at the B6-bridge, distributing heat through the copper planes that are directly connected to the MOSFETs. There is only a small amount of heating visible in the battery supply and ground path and also the reverse polarity MOSFET is significantly cooler than the B6-bridge MOSFETs. The digital side on the left has hardly warmed at all, which can be explained by the separation of the copper planes on the power side vs. the digital side. There is only one small connection between both sides. Looking at the second figure, you can see that the generated heat has spread out towards the copper planes surrounding the B6-bridge. So the heat is more evenly distributed, which causes the hotspots to have a lower temperature overall. The MOSFETs without heat sink reach 58.9°C at junction (die) whereas the MOSFETs with heat sink only reach 48.7°C. For simplification, the power dissipation is the same in both cases. In reality, the MOSFET without heat sink heats up a few degrees more, because the higher settling temperature will cause higher conductive losses, which cause additional heating again.

1 Power losses are estimated by simulation for a typical device
2 Power losses are estimated by simulation for a typical device

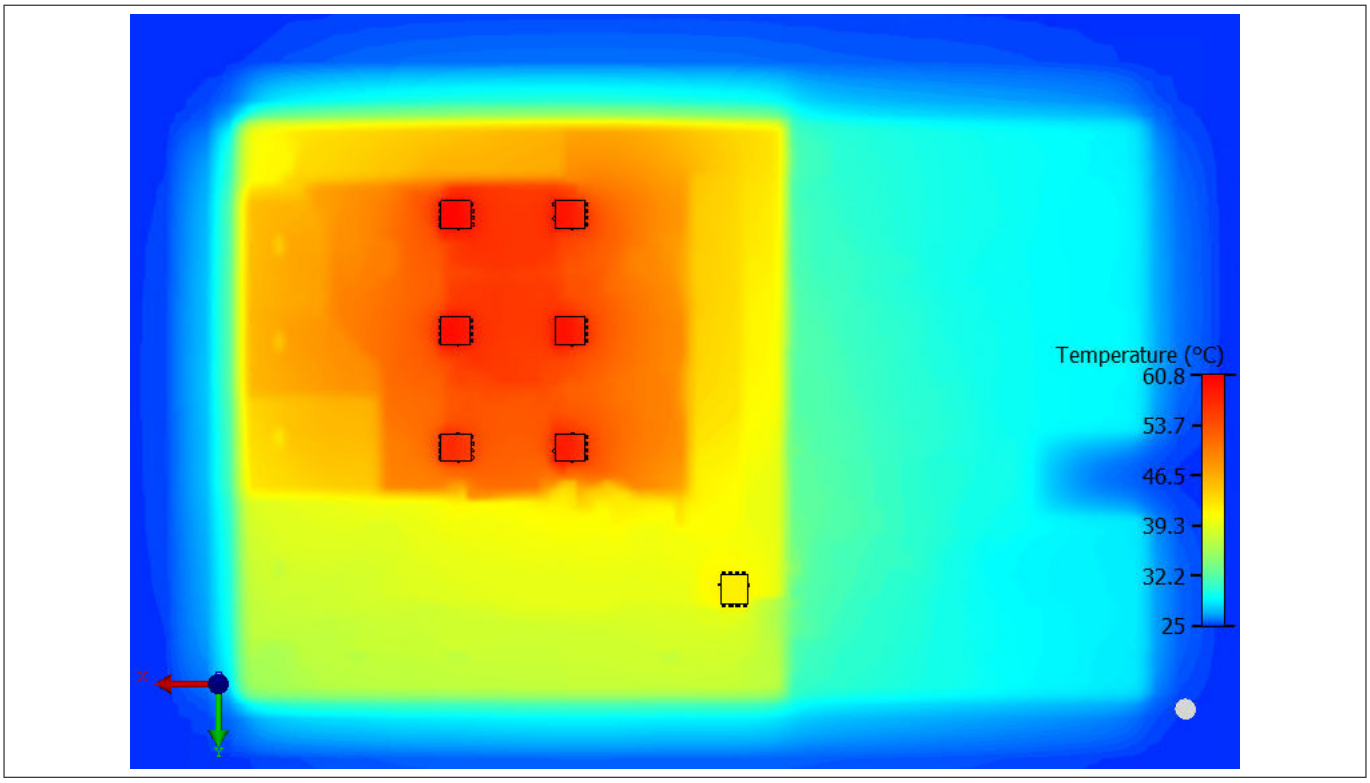

Figure 101 Heat distribution on PCB without heat sink

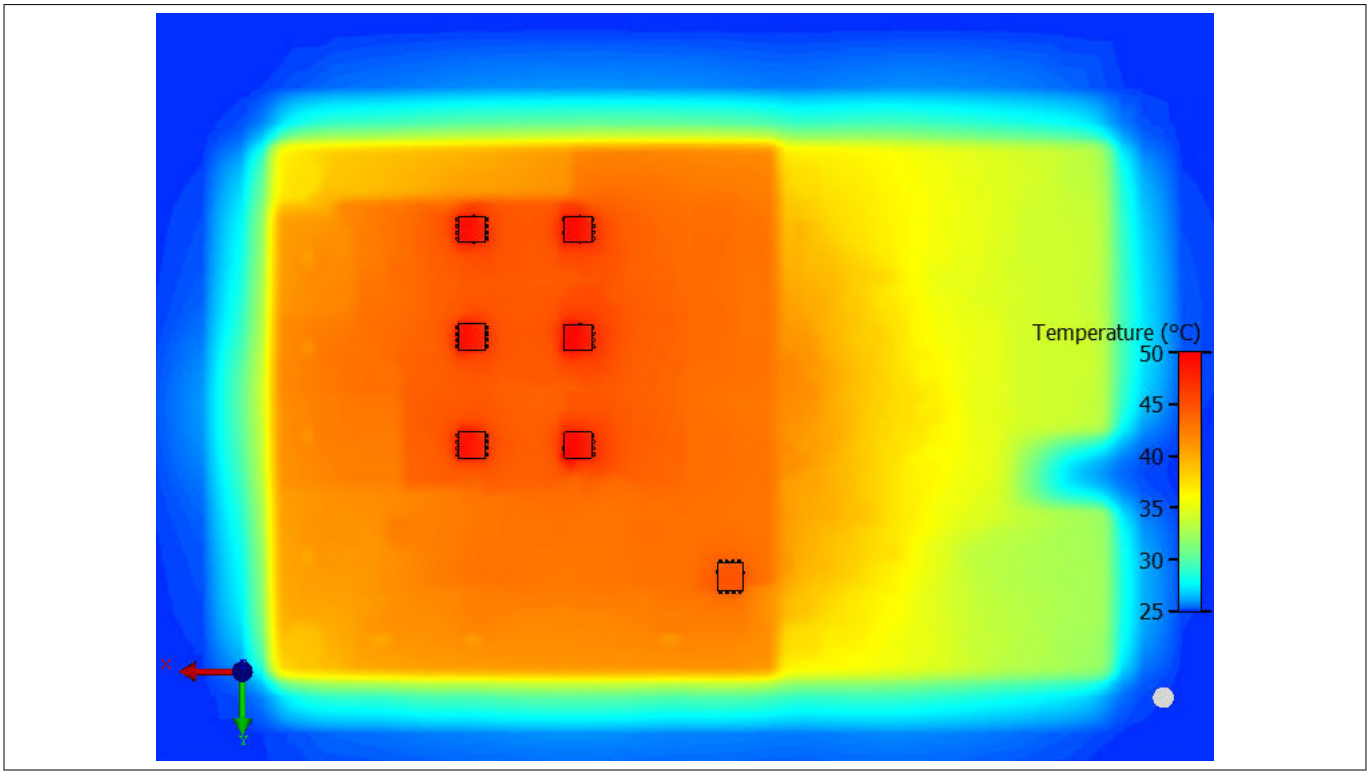

Figure 102 Heat distribution on PCB with heat sink

In addition to the horizontal heat distribution shown above, the figures below shows how the heat dissipates away from the PCB by free convection and radiation. Without a heat sink, the heat dissipates from a very condensed hotspot, whereas the rest of the PCB scarcely contributes to the dissipation. On the other hand, when the heat sink is added, a wide surface of the PCB dissipates the heat in a much more even way. It is also visible that most of the heat still dissipates away from the top side of the PCB due to rising hot air. This

illustrates that for the selected heat sink solution on the bottom, the heat sink itself contributes to the thermal performance by distributing the heat rather than dissipating it. It is important to note that these figures only show the steady state condition after a constant power loss was applied for a long time. When considering shorter but high peaks in power loss, the heat sink also serves as a buffer via its thermal capacitance.

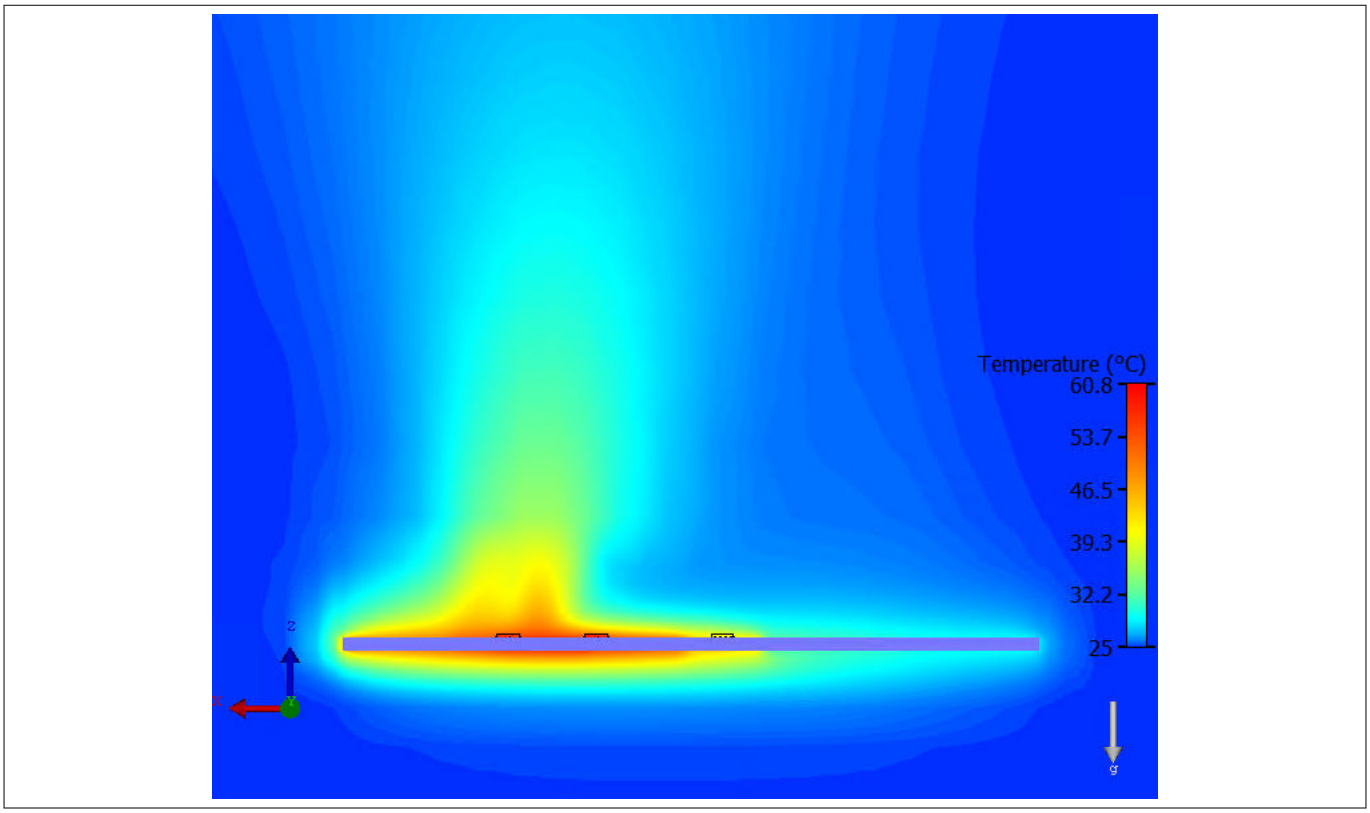

Figure 103 Heat radiation and convection from PCB without heat sink

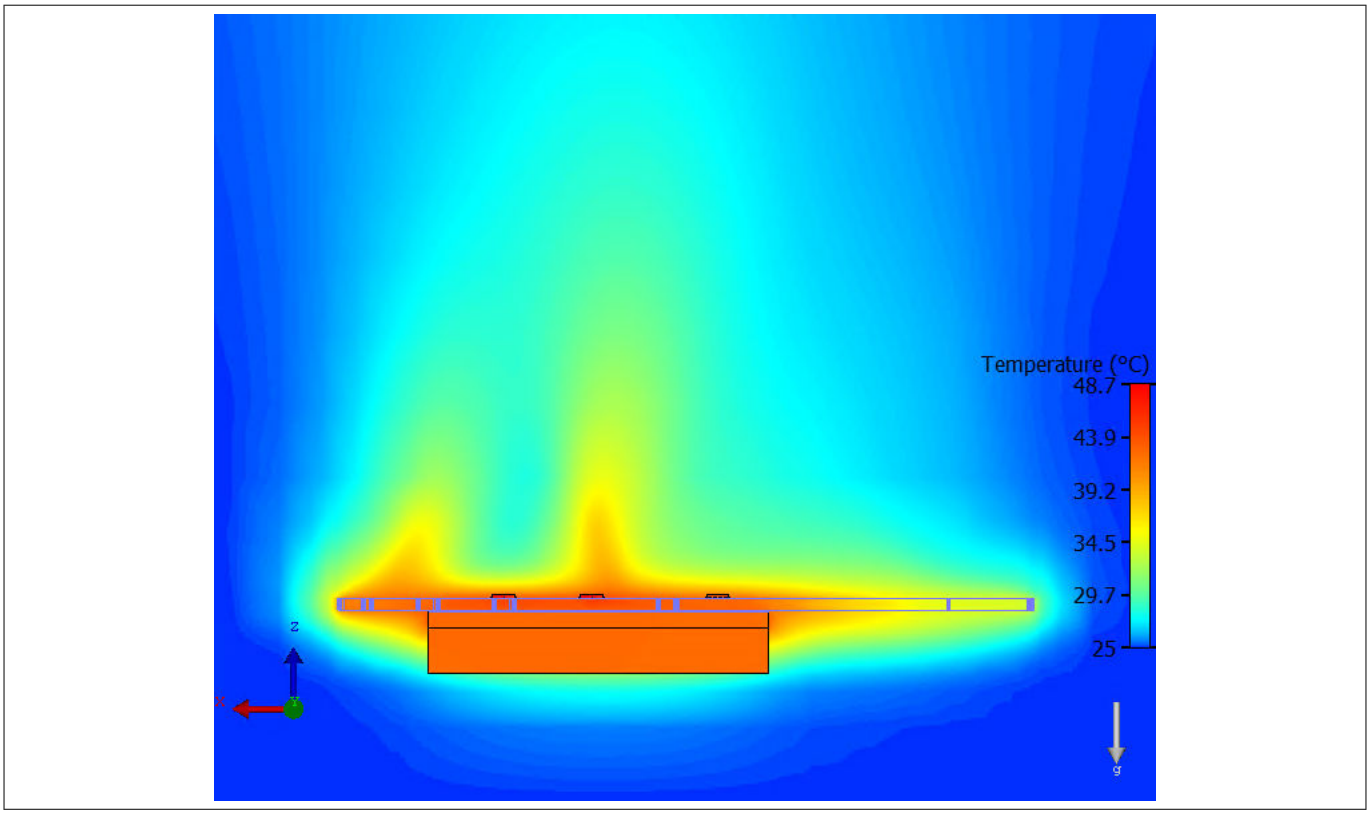

Figure 104 Heat radiation and convection from PCB with heat sink

In addition to the heat distribution described above, the figure below shows details of the Rth values for the PCB at different temperatures, with and without heat sink. The table shows the steady state junction temperatures of the MOSFETs and the power loss considered at each ambient temperature.

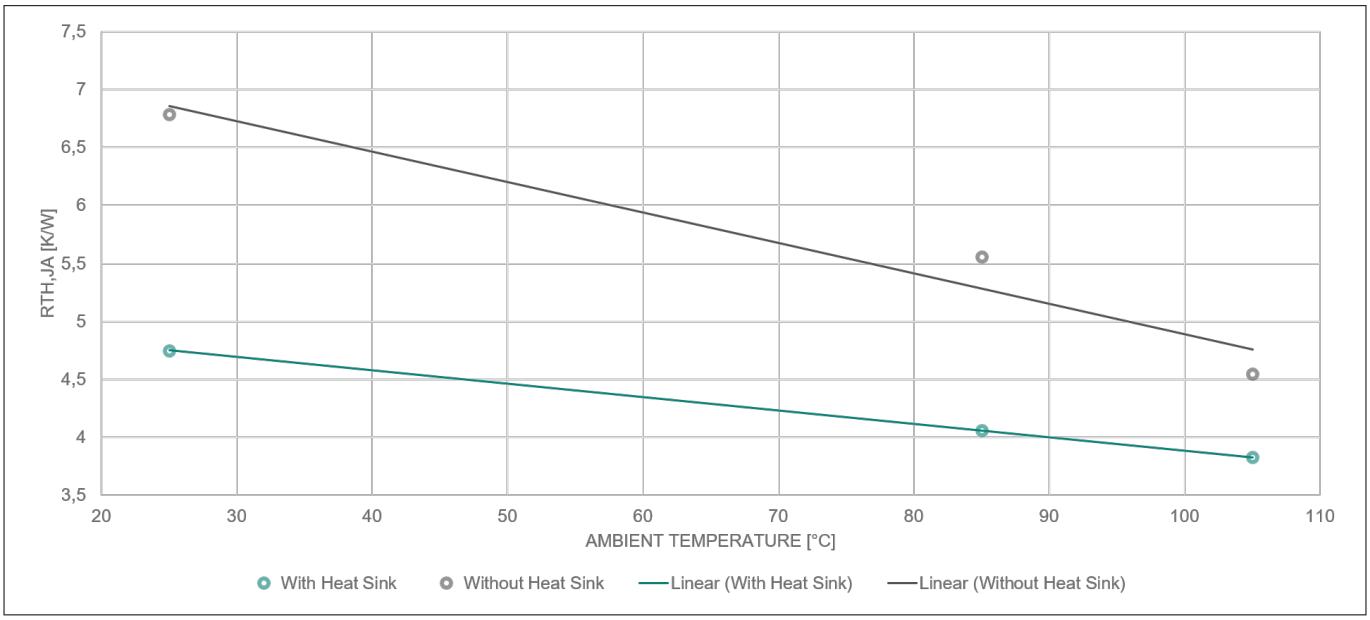

Figure 105 Rth for different ambient temperatures with and without heat sink

Table 3 Thermal simulation results

Ambient temperature [°C]	Heat sink?	Junction temperature [°C]	ΔT [°C]	Power [W][3)]	RthJA[K/W]
25	✓	48.7	23.7	4.99	4.75
25	✗	58.9	33.9	4.99	6.79
85	✓	106.4	21.4	5.27	4.06
85	✗	114.3	29.3	5.27	5.56
105	✓	125.9	20.9	5.45	3.83
105	✗	129.8	24.8	5.45	4.55

Finally, the figure below shows the heating curve over time at 25°C ambient temperature and without a heat sink. It differentiates between individual MOSFETs on the PCB. MOSFETs 1 and 6 represent the hottest and coldest MOSFET in the B6 bridge. It is visible that the majority of the heating occurs during the first 200 to 400 seconds. Additionally it can be observed that the junction temperature is always slightly higher than the case temperature.

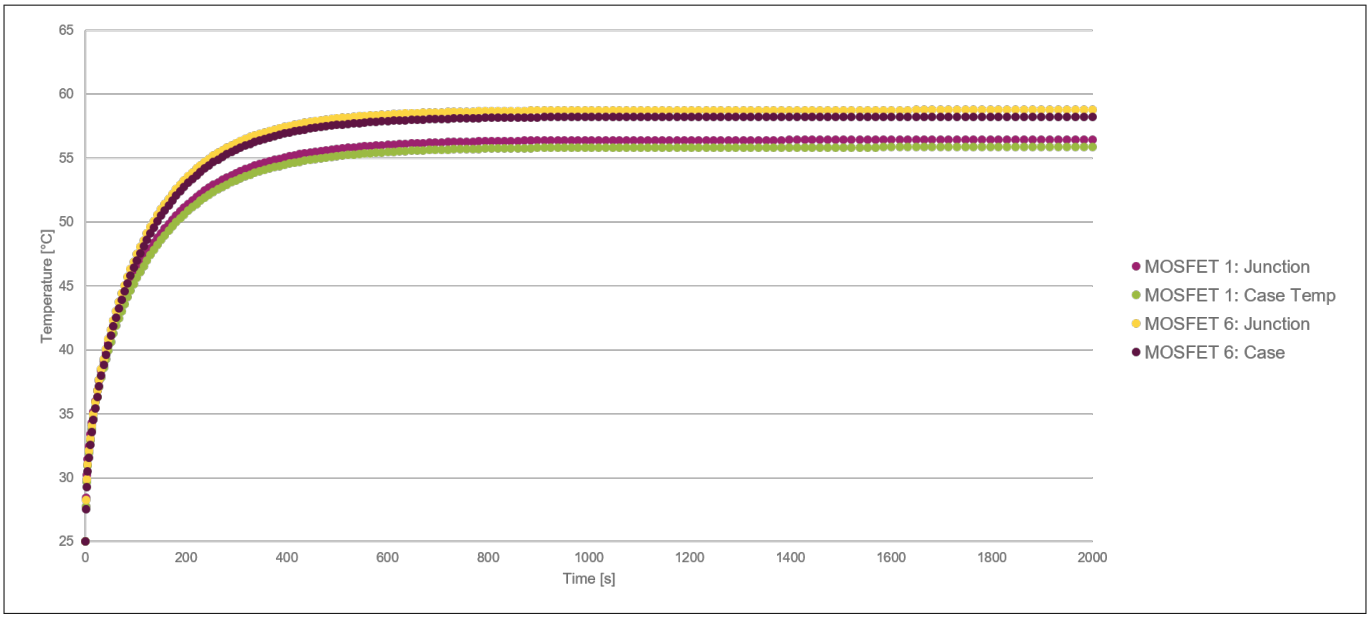

Figure 106 Heating curve for hottest and coldest MOSFET in B6-bridge at 25°C without heat sink

3 for an estimation of power dissipation in MOSFETs, a constant junction temperature was taken for the same ambient temperature for simplification. In reality, due to different heating of MOSFETs with and without heat sink, the power dissipation of the MOSFETs without heat sink will also increase and result in a higher settling temperature.

5 Description of characterized samples and boundary conditions

5.1 Limitations and boundary conditions

This chapter describes how to interpret the information in this report with respect to the datasheets of both driver and MOSFET.

Selection of devices used in characterization

For both the MOSFET and the driver, only a limited number of devices from a limited number of production lots were tested. Therefore, the data provided only shows the behavior of the tested subset of both gate driver and MOSFET for a specific set of application conditions. The data provided does not cover the behavior of all components produced in the future or other application conditions. The goal is to provide some insights into two different conditions. First, to show how the behavior of a specific driver and MOSFET sample combination can change during operation. Second, to show how different samples, even from different production lots, can behave differently under the same application conditions.

If you want to guarantee a specific behavior, refer only to the datasheet parameters. You can also calibrate the switching behavior following an end-of-line test.

Revision history

Document version	Date of release	Description of changes
Rev.1.00	2024-02-12	Editorial updates
Rev. 0.10	2023-08-16	Initial release

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