LITIX™ Power TLD5191ES

LED driver in buck-boost topology

About this document

Scope and purpose

This document covers the design steps for an automotive LED driver with a DC-DC converter in buck-boost configuration using the LITIX™ Power TLD5191ES.

The TLD5191ES is a high power and high efficiency buck-boost controller designed to drive LEDs in automotive applications. It includes built in diagnosis and protection features, embedded PWM engine and spread spectrum modulator.

The application requirements, used as an example, describes a typical automotive low beam LED driver ECU.

Intended audience

Hardware designers

Table of contents

LED driver in buck-boost topology 1
About this document 1
Table of contents 2
1 Introduction 3
1.1 Application example 4
2 External component design 5
2.1 Inductor 5
2.2 Output capacitors 6
2.3 MOSFETs 7
2.4 Switch current limiter R_{SWCS} 8
2.5 Output current sense resistor 9
2.6 Bootstrap diodes and capacitor 10
2.7 Analog dimming 11
2.7.1 Application hint – binning 11
2.8 Embedded PWM engine 12
2.8.1 PWMI resistor divider 13
2.8.2 PWM dimming element 13
2.8.3 Application hint - thermal derating 15
2.8.4 Application hint – fading 17
2.9 Application hint – light off using PWM 17
3 Protections 19
3.1 Overvoltage protection at the output 19
3.2 Soft start capacitor 20
3.1 Input undervoltage protection 21
4 Compensation network 23
4.1 Stability tips 27
5 EMC 28
5.1 Spread spectrum 28
5.2 Gate driver resistors 28
5.3 Layout considerations 29
6 List of references 30
Revision history 31

1 Introduction

Synchronous buck-boost converters with four power switches combines the functionalities of two separate converters (step-down and step-up) with the advantage of reduced size and cost. This topology can deliver very high power with high efficiency while providing both buck, buck-boost and boost DC-DC conversion.

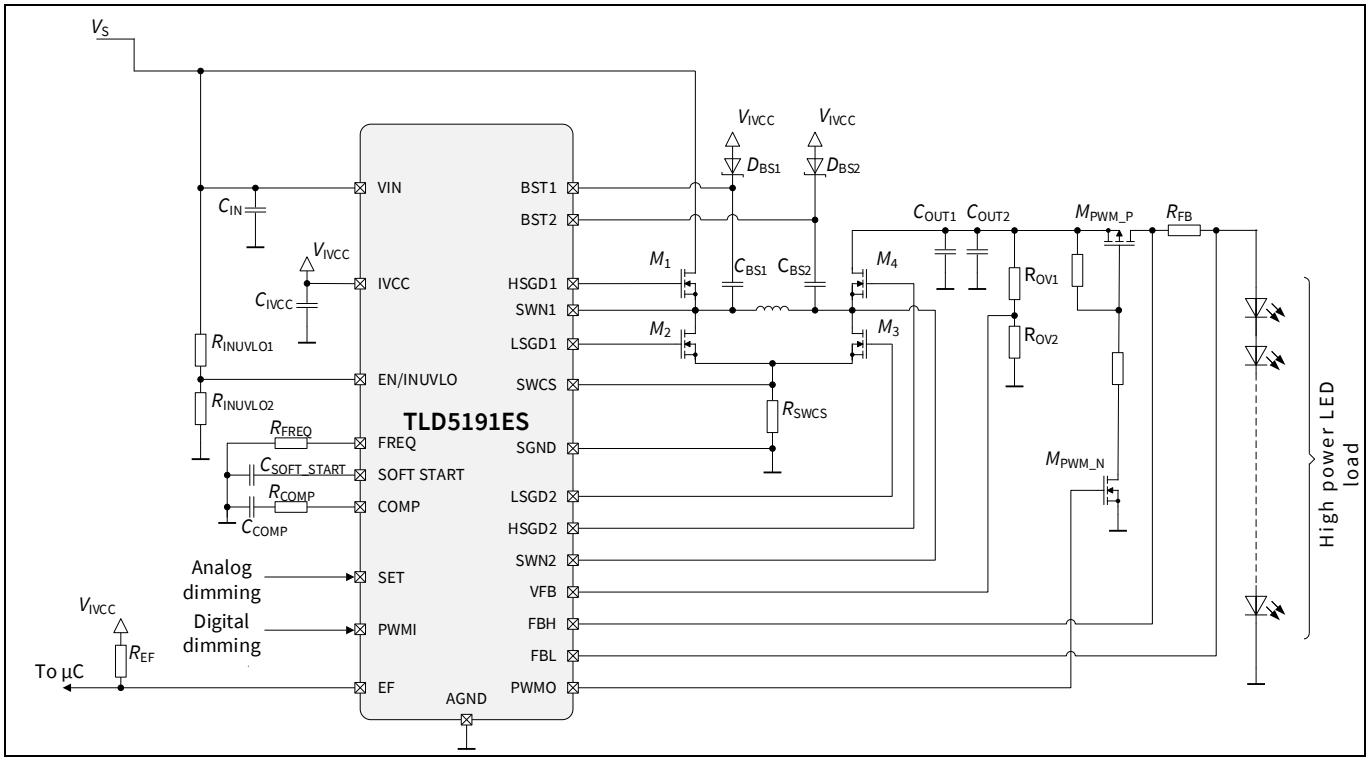

Figure 1 Application diagram – TLD5191ES as LED driver

The core of the DC-DC is a current mode controller with compensation capacitor; the dimensioning of external components is similar to a standard boost converter.

Selection of external components target the best compromise between efficiency, stability and cost in all operating conditions.

For fast calculation it is possible to use the "*Infineon-TLD5191ES_LED_Comp_calc-DevelopmentTools"* excel component calculator [1] available on the TLD5191ES Infineon website. All TLD5191ES external components, currents, efficiency, maximum power and stability are provided with minimum effort.

1.1 Application example

The following specifications are taken to design a LED driver module (LDM) with TLD5191ES to drive an automotive LED light function.

Table 1 LDM requirements

Parameter	Symbol	Value			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input voltage	V_{IN}	6 9	13.5 13.5	35 16	V V	Extended range Operating range
Output voltage	V_{OUT}	–	–	30	V	–
Output current	I_{OUT}	–	–	1500	mA	–
Output power	P_{OUT}	–	–	45	W	V_{IN} 9 V to 35 V, T_A = 25°C Power derating applies for V_{IN} < 9 V
Switching frequency	f_{SW}	–	385	–	kHz	–
System efficiency	η	–	95	–	%	V_{IN} = 13.5 V 6 LED, I_{OUT} = 1500 mA

Note: The same equations shown in this application note can be used to satisfy different requirements

2 External component design

2.1 Inductor

Inductor value depends on the switching frequency, which has been specified as 385 kHz. Increasing the switching frequency allows smaller inductor and output capacitors, however it increases the switching losses.

Increasing the inductor value (µH) results in:

- Reduced core losses (which depend on ripple value)
- Reduced conduction losses on MOSFET (smaller ripple current)
- Improved light load efficiency
- Increased conduction losses on inductor (higher inductor DCR if same dimension is kept)
- Reduced stability (more delay between regulation duty cycle change and effective current change)
- Reduced loop speed

The inductor in a boost converter is designed, based on the specified average and ripple current. Usually, the peak to peak current is in the range of 20% to 40% of the average value at the maximum rated power.

In this application 40% has been chosen, to minimize inductor size. Approximate equations are used assuming an efficiency of 95%.

The following equations are used to design the inductor in order to satisfy the required ripple current considering typical input voltage and maximum output power (P_{OUT_MAX} = 45 W, V_{OUT_MAX} = 30 V, I_{OUT} = 1.5 A), where in boost mode $I_L = I_{IN}$.

$$L_{MIN} = D_{TYP} \cdot \frac{V_{IN\_TYP}}{\Delta I_{L_{pkpk\_TYP}} \cdot f_{SW}} = 0.55 \cdot \frac{13.5\ V}{1.4\ A \cdot 385\ kHz} = 13.7\ \mu H$$

where

$$D_{TYP} = \frac{V_{OUT\_MAX} - V_{IN\_TYP}}{V_{OUT\_MAX}} = 0.55$$

$$\Delta I_{L_{pkpk\_TYP}} = 40\%\ I_L = 0.4 \cdot I_{IN} = 0.4 \cdot \frac{P_{OUT\_MAX}}{V_{IN\_TYP} \cdot \eta} = 0.4 \cdot \frac{45\ W}{13.5\ V \cdot 0.95} = 1.4\ A$$

The closest standard value that satisfies the equation is 15 µH.

The actual peak current in worst case condition (when minimum input voltage and maximum output power is applied) can be calculated as:

$$I_{L\_peak} = I_{IL\_AVG\_MAX} + \frac{\Delta I_{Lpkpk\_VIN\_MIN}}{2} = 5.4\ A + 0.55\ A = 5.95\ A$$

by assuming a lower efficiency of 93% for V_{IN} = 9 V;

$$I_{L\_AVG\_MAX} = I_{IN\_AVG\_MAX} = \frac{P_{OUT\_MAX}}{V_{IN\_MIN} \cdot \eta} = \frac{45\ W}{9\ V \cdot 0.93} = 5.4\ A$$

$$\Delta I_{Lpkpk\_VIN\_MIN} = D_{MAX} \cdot \frac{V_{IN\_MIN}}{L \cdot f_{SW}} = 0.7 \cdot \frac{9\ V}{15\ \mu H \cdot 385\ kHz} = 1.09\ A$$

$$D_{MAX} \approx \frac{V_{OUT\_MAX} - V_{IN\_MIN}}{V_{OUT\_MAX}} = 0.7$$

The important key parameters to select an inductor are then:

- Inductance ≥ 15 µH
- Saturation current and RMS current ≥ 5.95 A

An inductor that fulfills above requirements is the 15 µH TDK SPM10065VT-150M-D.

2.2 Output capacitors

The output capacitors act as an energy tank when the diode is in reverse polarity and for this reason it is subject to a high ripple current. These components affect the bandwidth of the system and also the output current ripple performance. Usually, for this kind of application, multilayer ceramic capacitors (X7R - MLCC) with low ESR are preferred over electrolytic capacitors.

Dimensioning of C_{OUT} is mainly driven by the output voltage ripple ΔV_{OUT}. Worst case condition for the output ripple is when the device is in boost mode (output current is discontinuous), minimum input voltage, maximum output current and maximum output power.

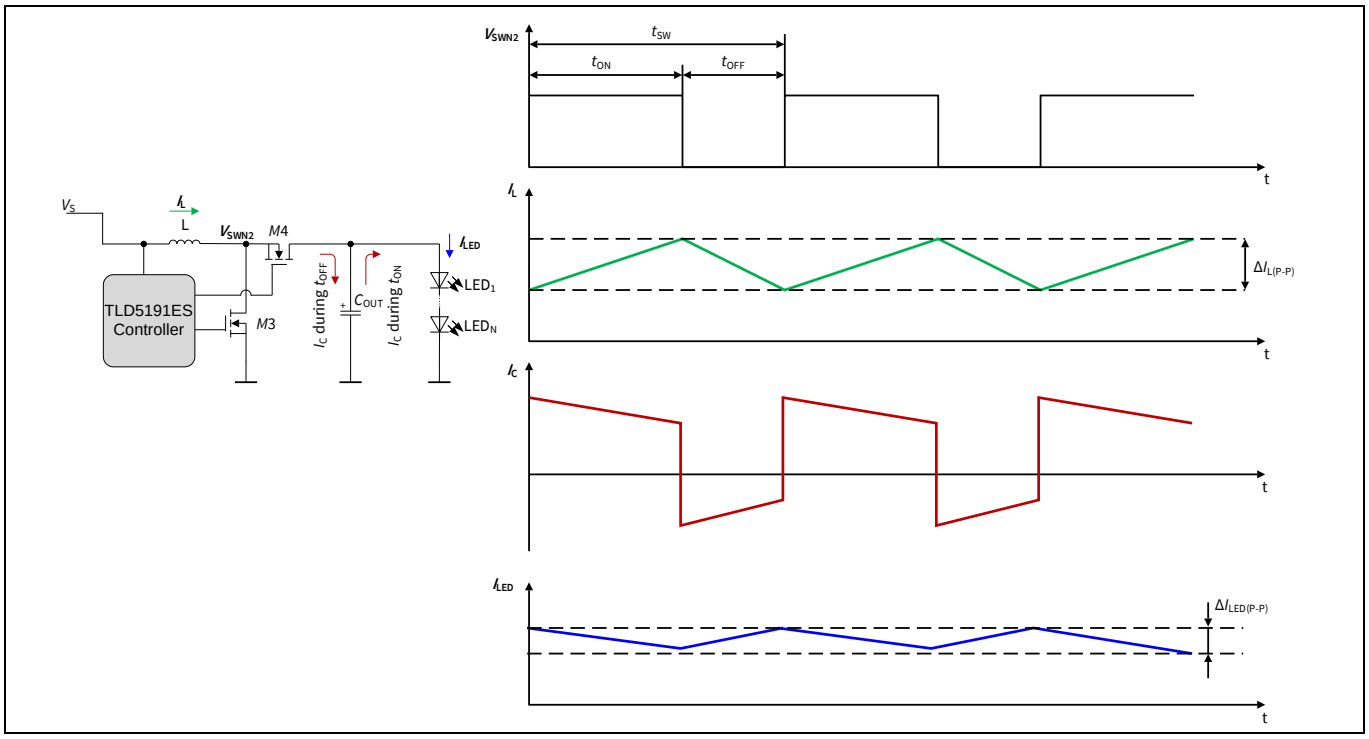

Figure 2 Output capacitors

In boost mode the output capacitors are discharged by a constant current equal to the average output current, for a time equal to $t_{ON} = D_{MAX}/f_{SW}$.

Assuming an ideal capacitor ($R_{ESR} = 0\ \Omega$), and considering $\Delta V_{OUT} = 0.2\ V$, its value can be calculated by the following equation:

$$C \geq \frac{I_{OUT}}{\Delta V_{OUT}} \cdot \frac{D_{MAX}}{f_{SW}} = \frac{1.5A}{0.2\ V} \cdot \frac{0.7}{385\ kHz} = 13.6\ \mu F$$

The ESR of the output capacitor adds more ripple, given with the equation:

$$\Delta V_{OUT\_ESR} = R_{ESR} \cdot I_{L\_peak} = R_{ESR} \cdot I_{IN\_peak} = R_{ESR} \cdot \left(\frac{I_{OUT}}{1 - D_{MAX}} + \frac{\Delta I_{Lpkpk\_VIN\_MIN}}{2}\right)$$

From the equations above, it is possible to calculate the maximum ESR in order to get a contribution of 20% on C_{OUT} ripple.

$$R_{ESR} \leq \frac{\Delta V_{ESR}}{I_{L\_peak}} = \frac{0.2 \cdot \Delta V_{OUT}}{5.95A} = \frac{0.2 \cdot 0.2\ V}{5.95A} = 6.7\ m\Omega$$

A parallel 3 x 4.7 µF X7R capacitors can fulfill required capacitance and series impedance.

Note: *MLCC capacitors show a strong variation of the capacitance as a function of the applied voltage. An X7R 100 V capacitor shows up to 30% drop at 30 V bias*

2.3 MOSFETs

Switching MOSFETs must be logic level, and they must withstand at least the maximum current calculated for the inductor sizing in Chapter 2.1:

$$I_{SW\_peak} = I_{L\_peak} = I_{IL\_AVG\_MAX} + \frac{\Delta I_{Lpkpk\_VIN\_MIN}}{2} = 5.4\ A + 0.55\ A = 5.95\ A$$

Voltage class on the buck (input) side must be higher than the maximum input voltage (35 V), while at the boost (output) side, voltage class must be higher than the maximum output voltage (50 V).

Note: *Choosing low $R_{DS(ON)}$ for the MOSFETs is not always the best choice. The optimum $R_{DS(ON)}$ shall balance switching losses and conduction losses, improving the efficiency. Efficiency on several MOSFETs can easily be compared during MOSFET selection process using the excel component calculator.*

In this design focus is on the highest efficiency, so a 7 mΩ 40 V MOSFET has been chosen for the buck side (Infineon IPZ40N04S5L-7R4) and a 14 mΩ 60 V MOSFET has been chosen for the boost side (Infineon IAUZ30N06S5L140). These MOSFETs have low parasitic capacitances with low reverse recovery charge (Q_{rr}) providing a 96% efficiency at V_{IN} = 13.5 V V_{OUT} = 30 V 1.5 A.

Note: *for EMI reasons, it is common practice to place a resistor (R_{GATE}) of approximately 5 Ω to 15 Ω in series depending on the gate charge and EMI performance of the circuit. This helps to reduce the current spikes into the gate and also to have a smooth transition from OFF state to ON state. On the other hand, this lowers the overall efficiency of the converter.*

2.4 Switch current limiter R_{SWCS}

The TLD5191ES offers a switch current limit protection in all the regulation modes (buck, buck-boost and boost) via the R_{SWCS} resistor.

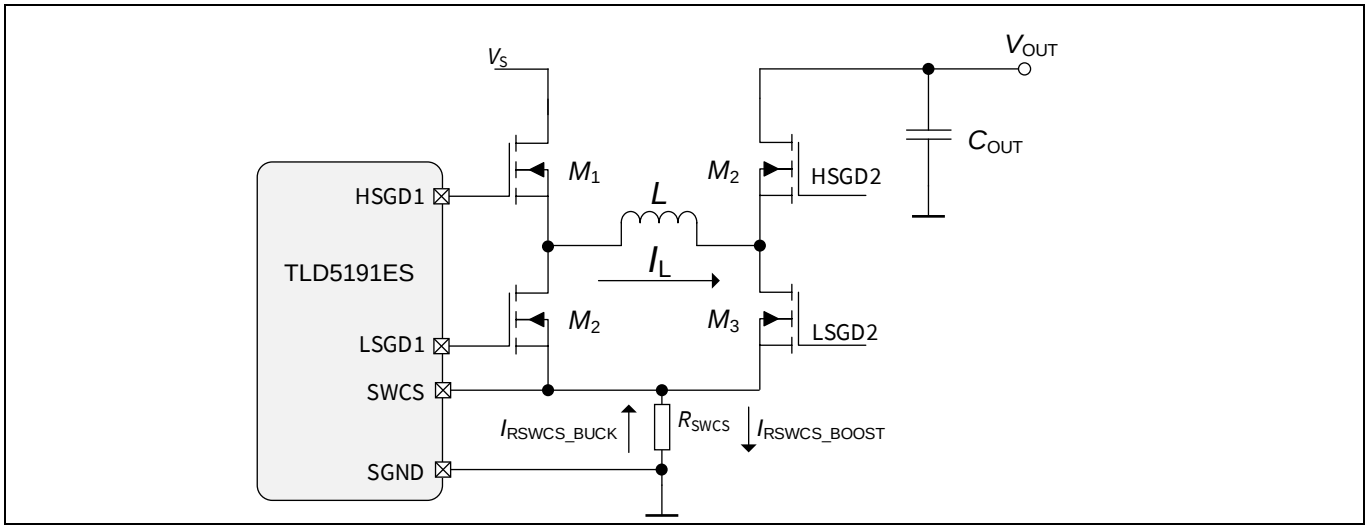

Figure 3 Switch current limiter R_{SWCS}

The current limit has to be set higher than the maximum switch current previously calculated I_{SW_peak} (5.95 A). Since in the design explained in this document the controller works in boost regulation mode and the following formula has to be considered:

$$R_{SWCS} < \frac{V_{SWCS\_BOOST\_MIN}}{I_{L\_peak}} = \frac{70mV}{5.95A} = 11.76m\Omega$$

R_{SWCS} is also the current mode controller sensing resistor, so it impacts stability: the bigger R_{SWCS}, the higher is the phase margin and PSRR. Choose the resistor slightly smaller than the required to fulfill the minimum switch current limit: 10 mΩ Susumu PRL1632-R010-F-T1, which provides a switch current limit in boost mode of:

$$I_{SW\_LIMIT\_TYP} = \frac{V_{SWCS\_BOOST\_TYP}}{R_{SWCS}} = \frac{76mV}{10m\Omega} = 7.6A$$

Note: In buck and buck-boost mode, the switch current limit threshold is decreased to V_{SWCS_BUCK} (typical value of 50 mV), so if the maximum power load it is in the buck-boost region use $V_{SWCS\_BUCK\_MIN}$ to calculate R_{SWCS} properly

Note: Use low inductive resistor on R_{SWCS}, in order to reduce fast transients switching activity noise

2.5 Output current sense resistor

The output current sensing resistor can be easily calculated by imposing the feedback voltage $V_{(FBH-FBL)}$ regulated by the device with the required output current.

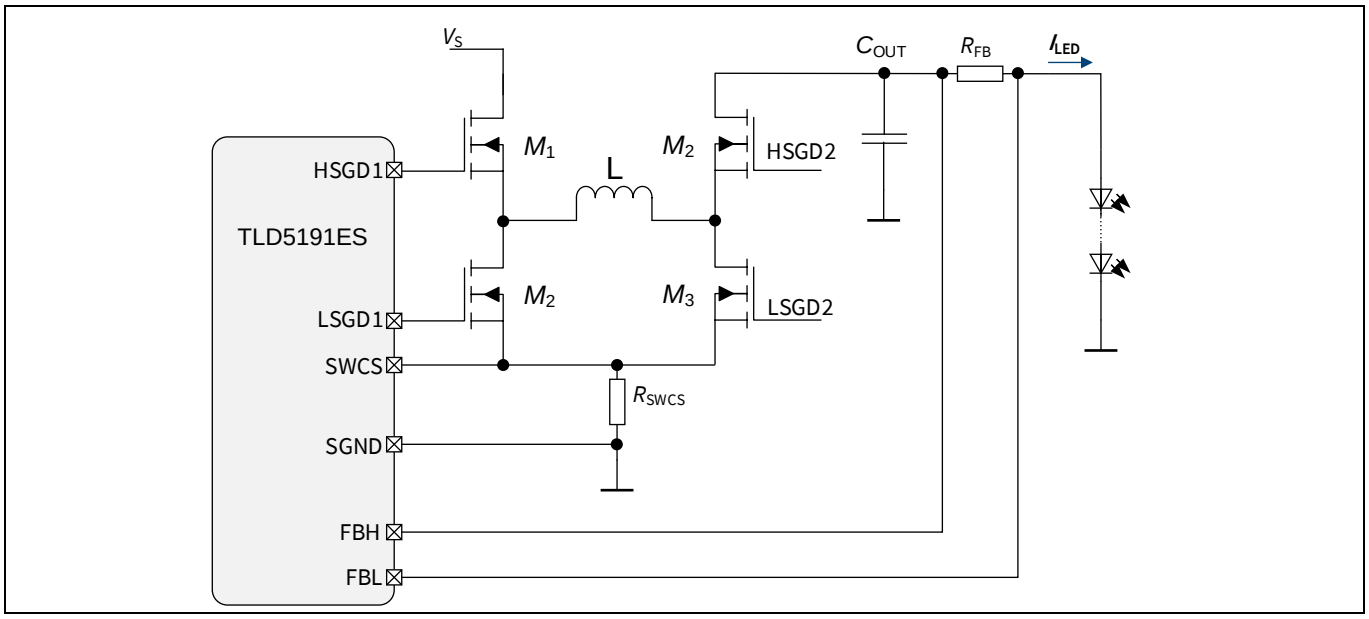

Figure 4 Output current sensing resistor

For this application, the resistor can be calculated as:

$$R_{FB} = \frac{V_{(\mathrm{FBH-FBL})}}{I_{OUT}} = \frac{0.15\ V}{1500\ mA} = 100\ m\Omega$$

The power rating of this device can be calculated as

$P = R_{FB} \cdot I_{OUT}^2 = 0.1\ \Omega\ \cdot (1.5A)^2 = 0.225\ W$

For this application PRL1632-R100-F-T1 from Susumu, satisfies the requirements.

2.6 Bootstrap diodes and capacitor

Bootstrap capacitors and diodes on TLD5191ES follow the standard design rules for any gate driver which uses bootstrap circuitry.

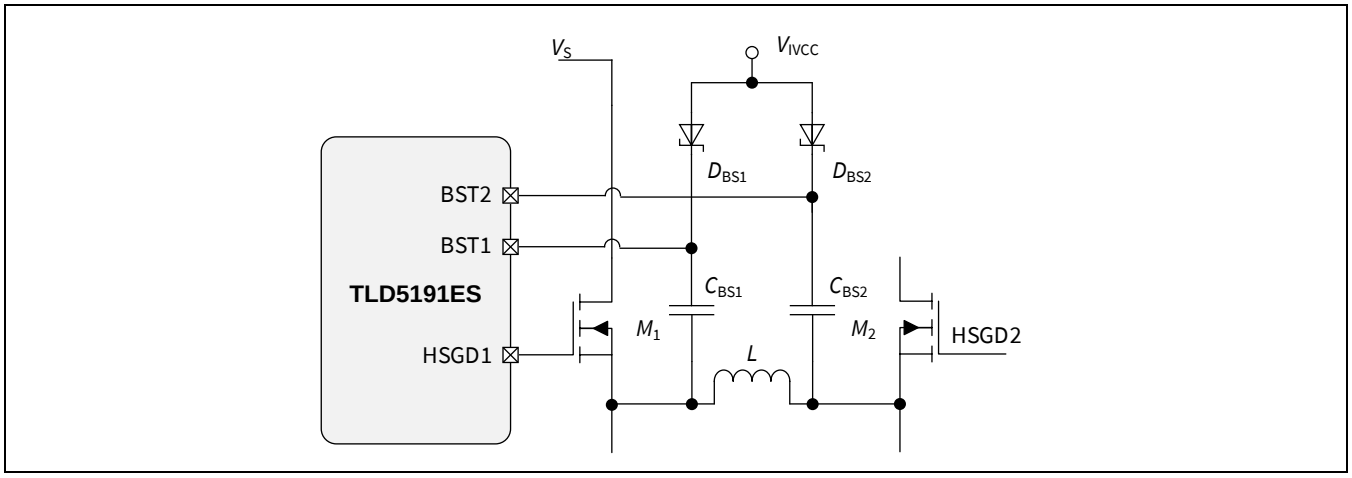

Figure 5 Bootstrap diodes and capacitors

The bootstrap capacitors must have enough energy to drive the gate of the high-side MOSFET without being depleted by more than 10%. Therefore, the bootstrap capacitor should be at least 10 times greater than the equivalent gate capacitance of the high-side FET.

For this application a standard 100 nF 50 V capacitor is chosen, which could drive about any modern generation MOSFET down to few mΩ $R_{DS(ON)}$ for example, 40 V 2Ω IAUC100N04S6L020.

Bootstrap diodes generate the high-side gate driver bias by charging the bootstrap capacitor. In order to minimize losses associated with the reverse recovery, a Schottky diode with low forward voltage drop and low junction capacitance is recommended.

Another requirement that is often overlooked is the diode reverse current at the highest working temperature. Reverse leakage current at high temperature may discharge the bootstrap capacitor and lead to undervoltage of the driver, triggering the shutdown of the gate driver.

A reverse current at maximum application operating temperature smaller than 0.1 mA is recommended for switching frequencies above 250 kHz.

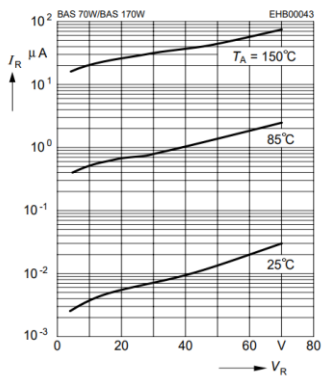

Figure 6 Bootstrap diodes reverse current of the BAS70-02V

For this application a 70 V Infineon BAS70-02V with low reverse current is chosen.

2.7 Analog dimming

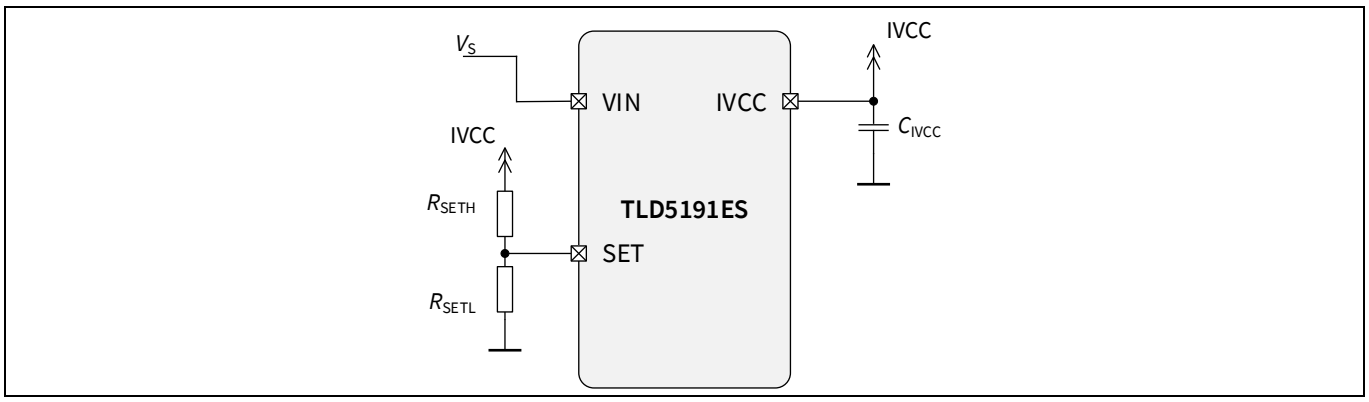

Figure 7 SET resistor divider

A resistor divider can be applied to a reference voltage (example to the 5 V IVCC) in order to set the desired output current $I_{OUT(AD)}$ by means of the SET pin.

To reduce the parasitic effects of the moisture and leakage from the SET pin, it is recommended to choose R_{SETL} equal to 15 kΩ.

Supposing that the requested analog dimming current is $I_{OUT(AD)}$= 0.9 A, then R_{SETH} is calculated using the following formula:

$$R_{SETH} = R_{SETL} \cdot \frac{V_{REF} - \left(I_{OUT(AD)} \cdot RFB \cdot 8 + 0.2\right)}{\left(I_{OUT(AD)} \cdot RFB \cdot 8 + 0.2\right)} = 15\text{k}\Omega \cdot \frac{5V - (0.9A \cdot 0.1\Omega \cdot 8 + 0.2V)}{(0.9A \cdot 0.1\Omega \cdot 8 + 0.2)} = 66.5\text{k}\Omega$$

Choosing 68 kΩ as closest commercial value, the effective output current would be:

$$I_{OUT(AD)} = \frac{V_{SET} - 200mV}{R_{FB} \cdot 8} = \frac{V_{REF} \cdot \frac{R_{SETL}}{R_{SETH} + R_{SETL}} - 200mV}{R_{FB} \cdot 8} = \frac{5V \cdot \frac{15\text{k}\Omega}{68\text{k}\Omega + 15\text{k}\Omega} - 200mV}{0.1\Omega \cdot 8} = 0.88A$$

2.7.1 Application hint – binning

In the manufacturing of LEDs there are always deviations due to the production process because all LEDs in a product batch are different with regard to their characteristics. To avoid big deviations, those similar in performance are grouped together in so-called bins.

Light output and color temperature are the most important bin criteria that directly affect product performance. To compensate the spread of these important parameters, different binning LED currents are usually defined.

The most common method to identify a bin is to assign a dedicated resistor value to each group.

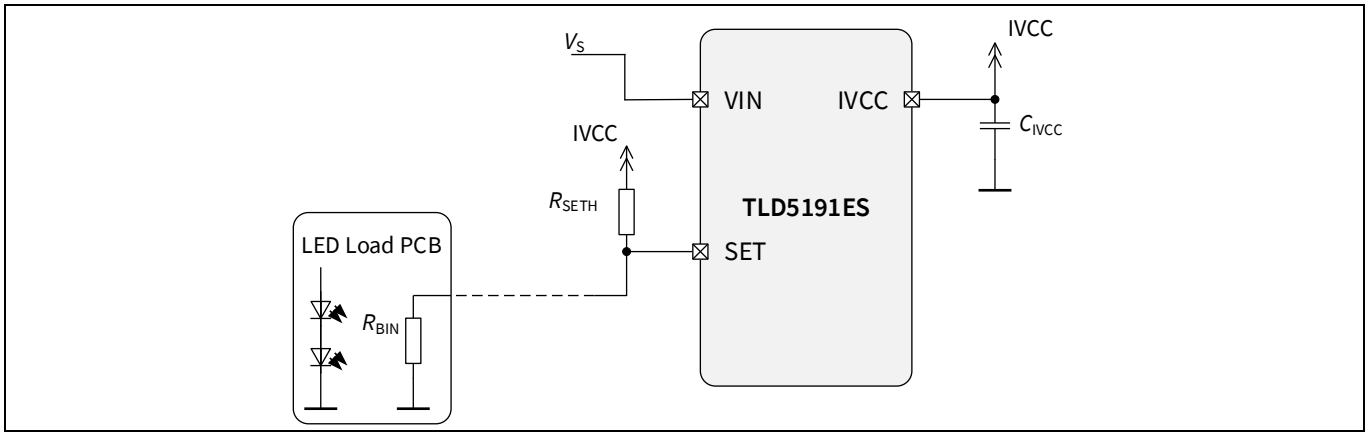

Figure 8 Binning by using the analog dimming feature

The analog dimming feature can be used together with the binning resistor to set the proper output current in order to always obtain the same LED performance allowing the possibility to use different bin groups.

2.8 Embedded PWM engine

Embedded PWM engine provides an internal PWM signal without any external dimming signal required.

A non-linear embedded PWM engine is implemented to guarantee high accuracy for low values of duty cycle. It helps the headlamp designers to achieve high LED brightness accuracy when dimming to low duty cycle values.

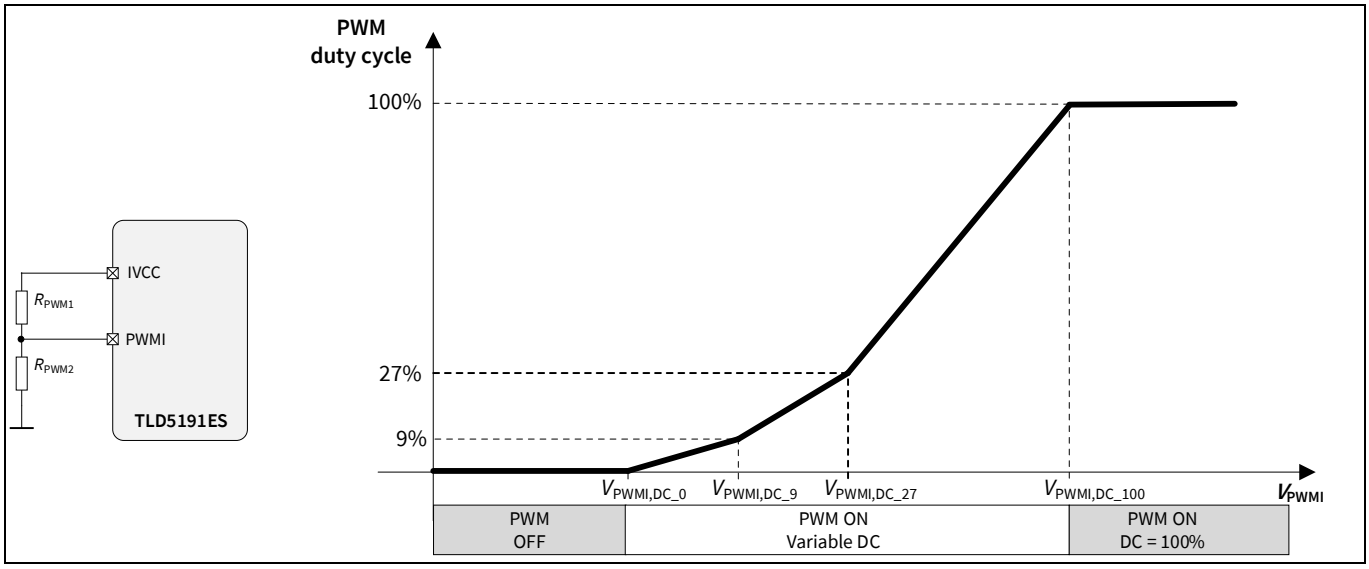

Figure 9 PWMI duty cycle curve

The frequency of the PWM engine has a nominal value of 270 Hz, while the duty cycle is adjusted by a voltage divider on the PWMI pin from IVCC.

2.8.1 PWMI resistor divider

Assuming a dimming duty cycle (DC) of 90% the two resistors R_{PWMI1} and R_{PWMI2} can be calculated using the following formulas:

$$V_{PWMI} = \frac{(DC\% - 27.13)}{72.823} \cdot 0.1 \cdot V_{IVCC} + 0.28 \cdot V_{IVCC} = 1.83\ V$$

Where V_{IVCC} = 5 V.

To reduce the parasitic effects of the moisture and leakage from the PWMI pin, it is recommended to choose R_{PWM2} equal to 11 kΩ. The R_{PWM1} is then obtained:

$$R_{PWM1} = R_{PWM2} \cdot \frac{V_{IVCC} - V_{PWMI}}{V_{PWMI}} = 19.05\ \text{k}\Omega$$

Choosing 19.1 kΩ as closest commercial value, the effective duty cycle would be:

$$DC\%_{TYP} = 27.13 + 72.832 \cdot \frac{\frac{R_{PWM2}}{R_{PWMI} + R_{PWM2}} - 0.28}{0.1} = 89.36\%$$

2.8.2 PWM dimming element

To have a common ground between load and DC-DC a PMOS transistor has to be used as a dimming and a protection device. The level shifter (needed for properly biasing the PMOS) is made up of the transistor M_{PWM_N}, the resistors R_{DIM1} and R_{DIM2} bias the gate of transistor M_{PWM_P} while the 10 V Zener diode protects the gate of PMOS.

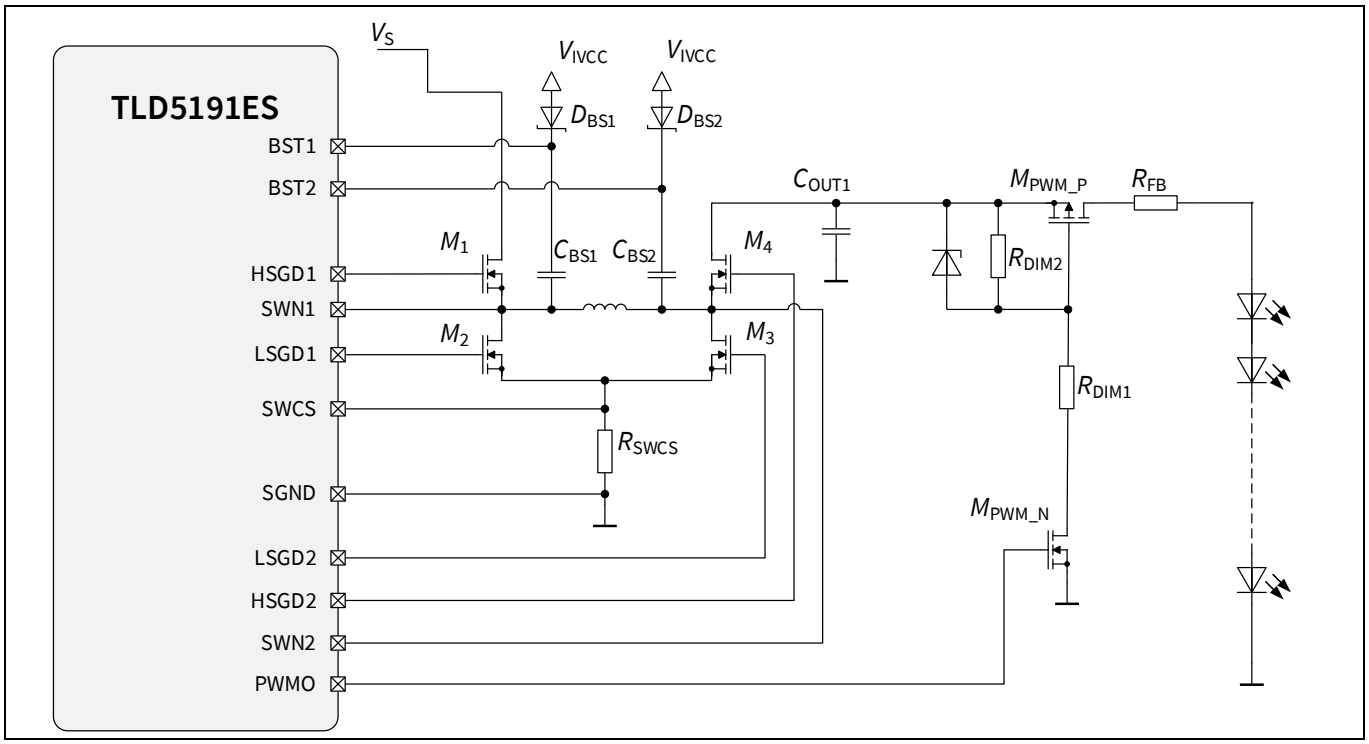

Figure 10 Dimming PMOS setup

M_{PWM_P} has to drive a load current up to 1.5 A during ON state, while when the transistor is in OFF state its V_{DS} can reach the maximum V_{OUT} of 30 V. An Infineon component suitable for this application is BSO615CG. This device contains a PMOS and an NMOS in the same package and can be used as M_{PWM_N}.

Note: *For T_A > 80°C the PMOS component of the BSO615CG device can manage current lower than 1.5 A. Depending on the application requirements, it is then recommended to apply a current derating in order to avoid any damage on the device.*

The threshold voltage of PMOS is 2 V, but to have a low resistance, a gate to source voltage of 10 V can be applied. Fixing the current on the NMOS to 2 mA, R_{DIM2} can easily be calculated as the ratio between the desired V_{GS} of PMOS transistor and the current.

$$R_{DIM2} = \frac{V_{GS-PMOS}}{I_R} = \frac{10\ V}{2\ mA} = 5\ k\Omega$$

The closest commercial value for R_{DIM2} is then 5.6 kΩ.

To calculate R_{DIM2} the lowest V_{OUT} needs to be considered. The applied V_{GS} always needs to be above the threshold voltage, $V_{GS,th}$ of the PMOS, in order to avoid any damage to the device.

The R_{DIM1} can be calculated as follows:

$$R_{DIM1} > R_{DIM2} \cdot \frac{V_{GS\_th}}{V_{OUT\_MIN} - V_{GS\_th}}$$

Consider a minimum V_{OUT} three times larger than the $V_{GS,th}$, the result is:

$$R_{DIM1} > R_{DIM2} \cdot \frac{V_{GS\_th}}{V_{OUT\_MIN} - V_{GS\_th}} = 5.6\ k\Omega \cdot \frac{2\ V}{6\ V - 2\ V} = 2.8\ k\Omega$$

A value of 5.6 kΩ is then selected for R_{DIM1} resistor.

Note: *With the proposed design the minimum V_{OUT} cannot be lower than 6 V otherwise the PMOS could be damaged*

The level shifter to drive the PMOS introduces a delay that could impact the minimum duty cycle observable on the output current.

In case it is of interest to the designer to obtain a precise duty cycle below 1%, it is recommended to implement the dimming element with merely an NMOS transistor as depicted in the figure below.

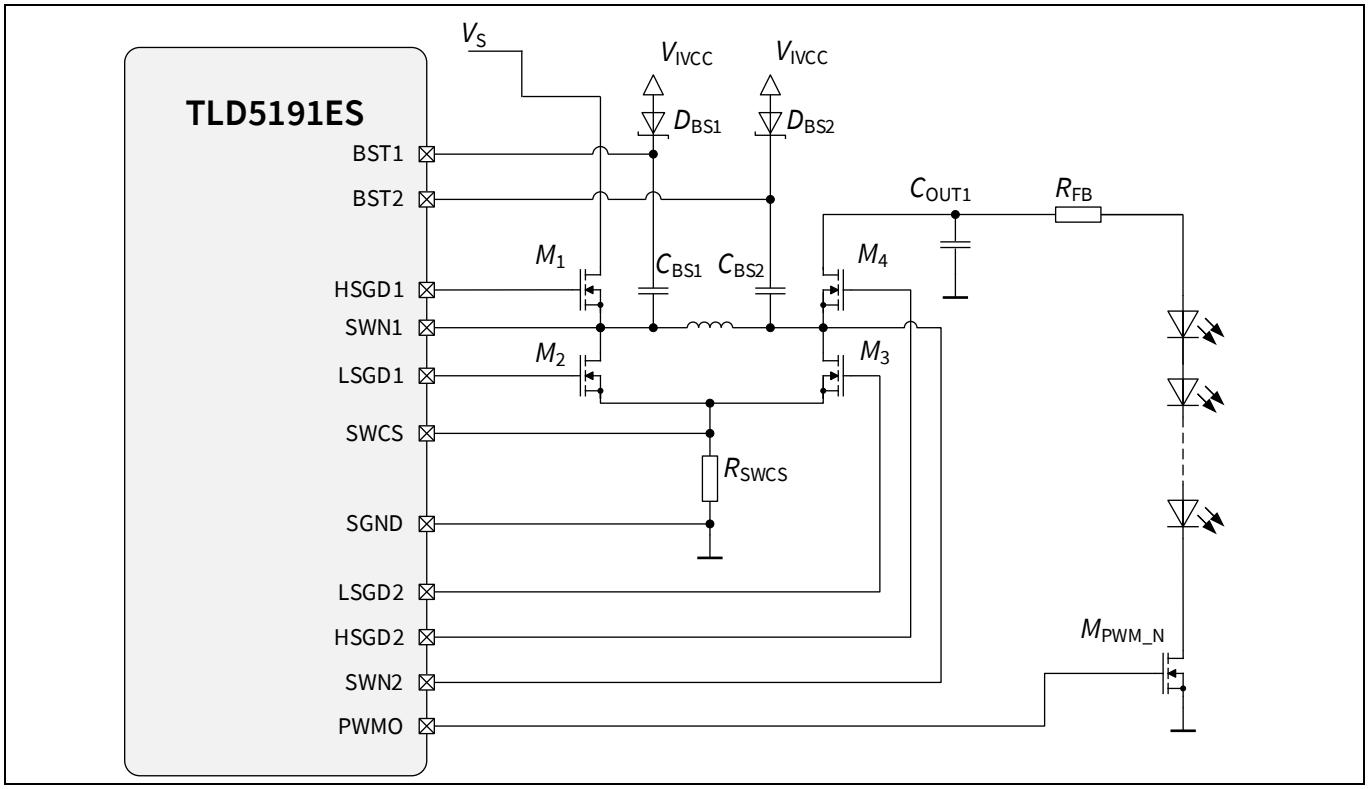

Figure 11 Dimming NMOS setup

2.8.3 Application hint - thermal derating

The introduction of high-power LED technology has raised the need for a proper thermal management design in lighting applications. Like all semiconductors, LEDs must not overheat otherwise their celebrated long lifetimes will be adversely affected. Indeed, a significant amount of the electrical energy flowing through the device is converted into heat. Therefore, it is essential that thermal management and the consideration of the effects of high environmental temperatures are addressed right at the start of the design phase.

The most used solution is to apply a thermal derating profile. The embedded PWM engine of the TLD5191ES can be used to reduce the average current delivered to the load to protect it from overheating.

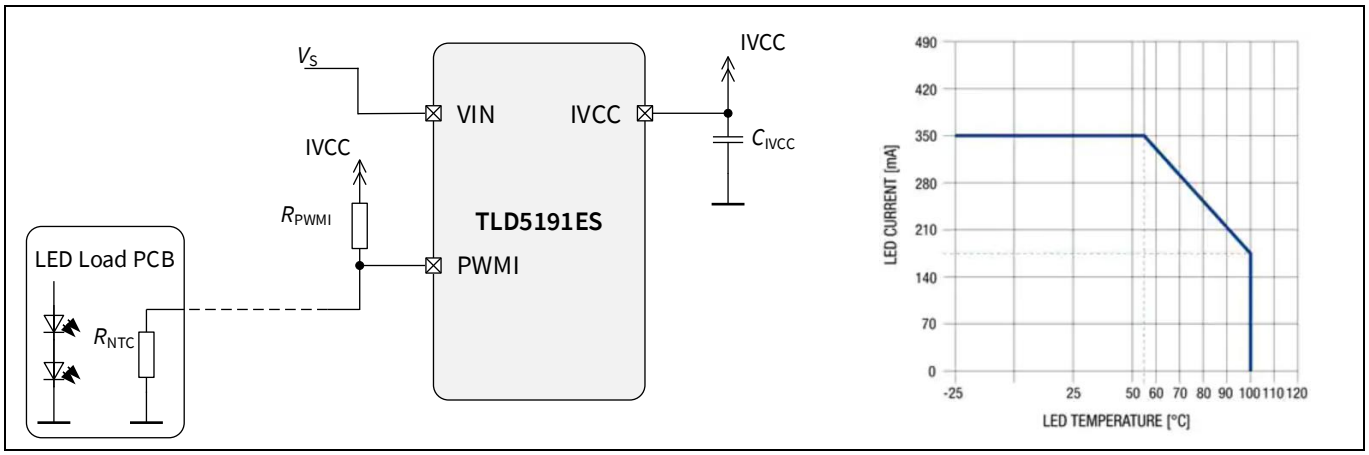

Figure 12 Thermal derating example

For instance, looking at the profile described in Figure 12 the output current needs to be delivered at nominal value until 55°C and then it has to start to decrease linearly.

It implies that the embedded PWM engine has to be set at 100% of duty cycle until 55°C and once the ambient temperature rises above such a temperature it has to decrease the output current.

A case in point is NTCG063JF103FTB from TDK. The following parameters apply:

JIS 0603 [EIA 0201]

Part No.	Resistance value [25°C] (Ω)	Resistance tolerance	B constant [25/50°C] (K)	B constant [25/75°C] (K)	B constant [25/85°C] (K)	B constant [25/100°C] (K)	B constant tolerance	Permissible operating current [25°C] (mA)	Operating temperature range (°C)	RT table
NTCG063EH400HTB	40	+/–3%	3244	3249	3250	3251	+/–3%	5.00	–40 to 125	csv
NTCG063JF103FTB	10,000	+/–1%	3380	3422	3435	3453	+/–1%	0.31	–40 to 125	csv

Figure 13 NTC characteristics

The value of the NTC resistance is given by the following formula:

$$R_{NTC} = R_0 \cdot e^{B \cdot (\frac{1}{T} - \frac{1}{T_0})}$$

The result is a value of 3.69 kΩ for 55°C.

The applied duty cycle is a function of the voltage applied on the PWMI input pin and in particular, based on the requirements, the following equation is deduced:

$$DC\% = 27.13 + 72.832 \cdot \frac{\frac{R_{NTC\_55°C}}{R_{PWMI} + R_{NTC\_55°C}} - 0.28}{0.1} = 100\%$$

R_{PWMI} has to be:

$$R_{PWMI} = \frac{1 - 0.38}{0.38} \cdot R_{NTC\_55°C} \quad = 6.02\ k\Omega$$

The closest commercial value is 6.04 kΩ.

The permissible operating current at 25°C has to be verified in order to avoid NTC self-heating that would lead to a wrong temperature detection due to a degradation of the temperature sensing accuracy:

$$I_{NTC_{25°C}} = \frac{IVCC}{R_{NTC\_25°C} + R_{PWMI}} = \frac{5\ V}{10\ k\Omega + 6.02\ k\Omega} = 0.31\ mA$$

The requirement for the selected NTC is satisfied.

2.8.4 Application hint – fading

The embedded PWM engine can also be used to implement a smooth turn-on (fading) of the LED light function. Indeed, the non-linear embedded PWM engine helps to compensate the logarithmic brightness perception of the light by the human eye, leading to a linear brightness variation.

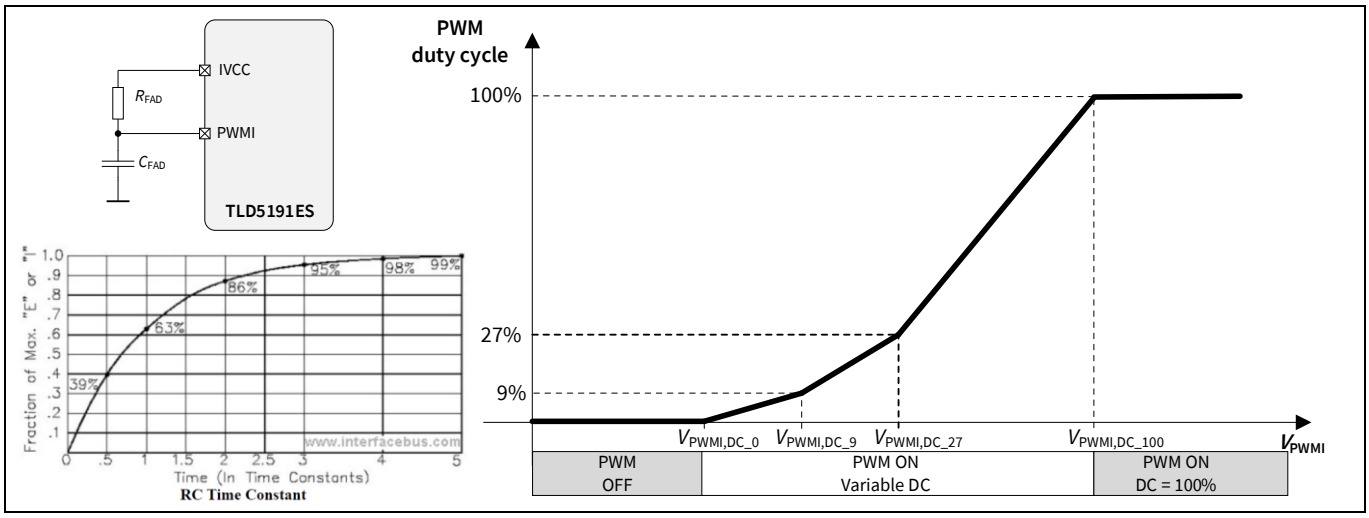

Figure 14 LED light function fading

The applied voltage variation on the PWMI pin (V_{PWMI}) needs to be linear in order to make use of the non-linear embedded PWM engine implementation. The curve of an RC network can be approximated as linear until 0.5 τ.

V_{PWMI,DC_100} has a maximum value of 0.387 ·V_{IVCC} with the consequence that 100% of duty cycle is reached at 0.5 τ. Assuming 1 s fading time for the light function, the following results as the dimension for the RC network:

$$0.5 \cdot \tau = 0.5 \cdot R_{FAD} \cdot C_{FAD} = 1\ s$$

Considering using 10 µF capacitor for C_{FAD} results in:

$$R_{FAD} = \frac{2\ s}{C_{FAD}} = \frac{2\ s}{10\ \mu F} = 200\ k\Omega$$

2.9 Application hint – light off using PWM

In case of multiple functions on the same ECU it is requested to have independent DC-DC channels. The PWMI input pin of the TLD5191ES can be used for both to apply a PWM signal and to enable/disable the light function in a safe manner.

A soft start routine is applied once the channel is enabled via PWMI if the PWM input signal has been kept below V_{PWMI,DC_0} for more than 25 ms ($t_{PWMI,OFF}$).

Only one wire is needed to control the light function and as a consequence, costs are saved compared to two wires where one is used to enable the device and one to apply a digital dimming signal.

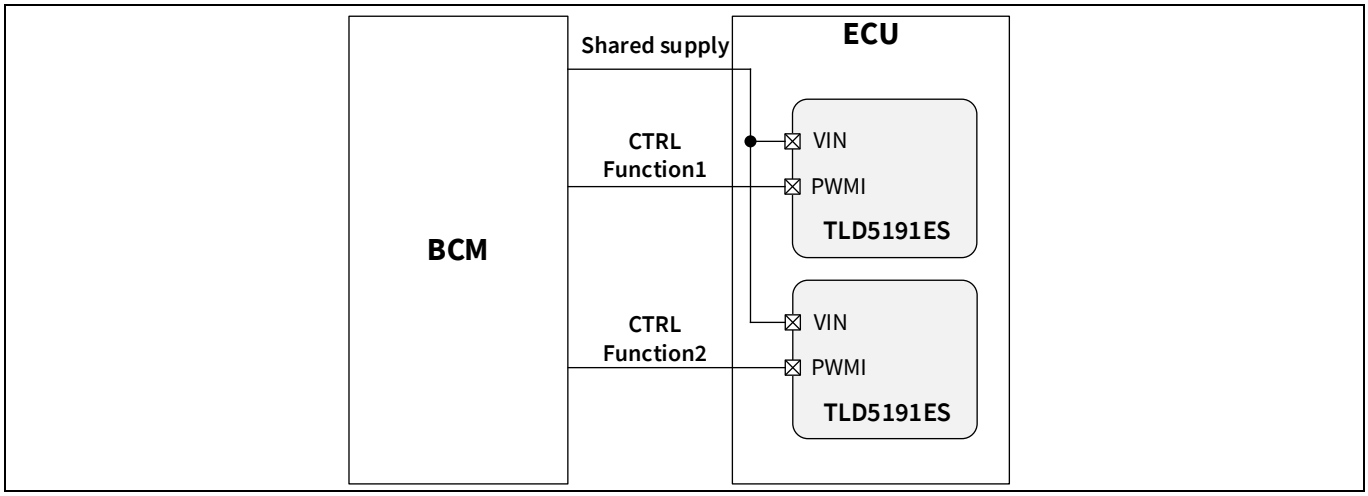

Figure 15 Light function control via PWMI input pin

3 Protections

3.1 Overvoltage protection at the output

This feature protects the LED driver module if the load gets disconnected.

The overvoltage at the output (V_{OUT_MAX}) has to be set:

- higher than the maximum voltage
- lower than the absolute maximum voltage of the TLD5191ES FBH pin (60 V)

Note: During the overvoltage event the inductor current is discharged to the output, thus an output voltage increase may be observed based on the L_{OUT} and C_{OUT} design. The overvoltage threshold must be designed to avoid exceeding the device maximum absolute ratings

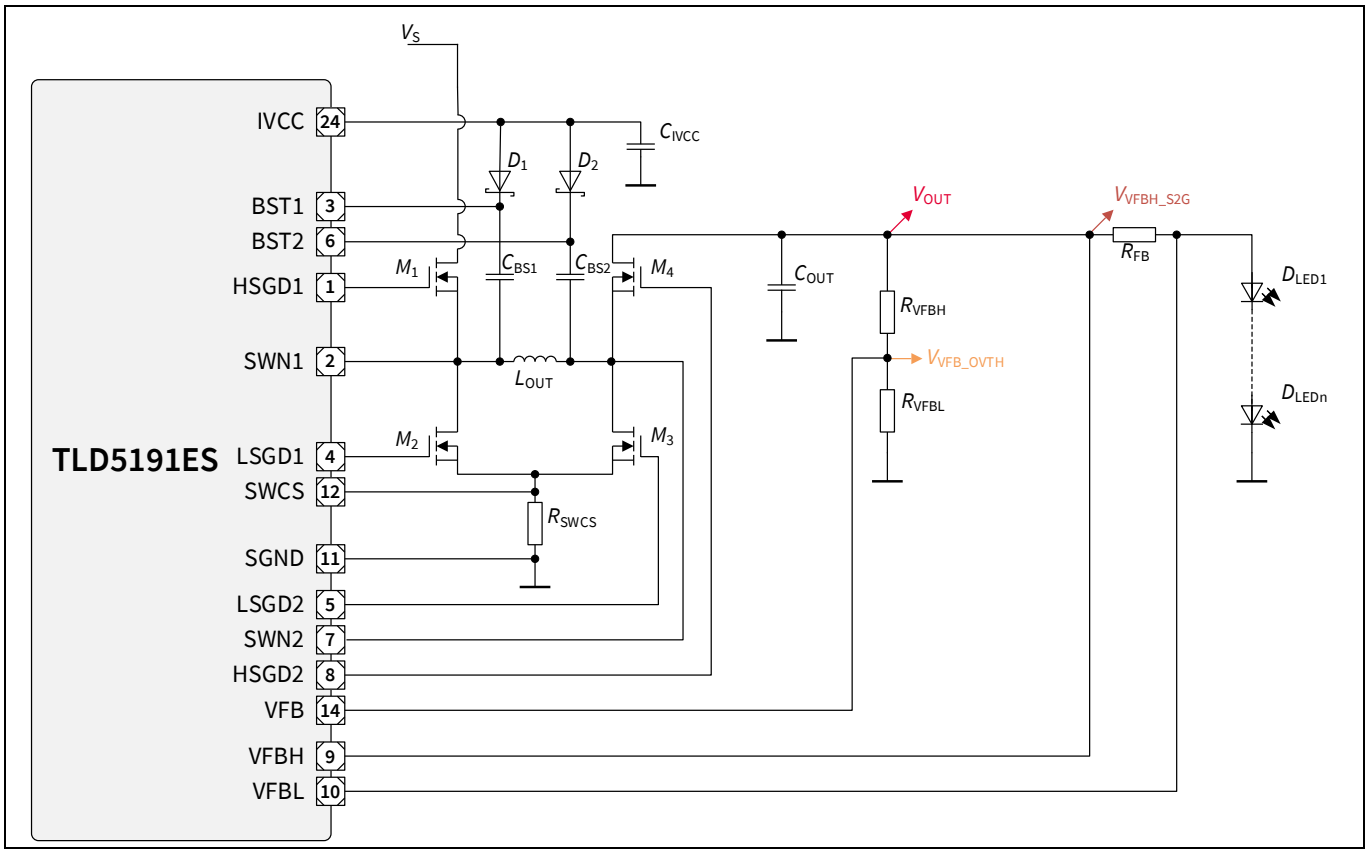

Figure 16 Protections schematic

Overvoltage is triggered when the voltage on VFB pin reaches 1.46 V (typ). The resistor divider to enable this feature, is shown in Figure 16.

To reduce the parasitic effects of the moisture and leakage from the VFB pin, it is recommended to choose R_{VFBL} equal to 1.5 kΩ.

The second resistor (R_{VFBL}); to obtain the desired overvoltage threshold, is calculated as:

$$R_{VFBH} = R_{VFBL} \cdot \frac{V_{OUT\_OV}}{V_{OUT\_OVTH\_TYP}} - R_{VFBL} = 1.5\ \text{k}\Omega \cdot \frac{50\ V}{1.46\ V} - 1.5\ \text{k}\Omega = 49.86\ k\Omega$$

The closest value as off-the-shelf component on E96 series is 49.9 kΩ.

The actual output overvoltage value is calculated using the real component values with the following formula:

$$V_{OUT\_MAX} = V_{OUT\_OVTH} \cdot \frac{R_{VFBL} + R_{VFBH}}{R_{VFBL}}$$

With the above formula it is possible to check the effect of V_{OUT_OVTH} deviations (min to max).

3.2 Soft start capacitor

The soft start routine has 2 functionalities:

- Fault mask and wait-before-retry time
- Limit input inrush current and output overshoots at startup

The most relevant function of the soft start routine for LED drivers is the short to ground (S2G) fault mask. At startup the output voltage is very likely 0 V therefore, without the fault mask, a S2G would be detected.

Soft start duration is determined by the soft start capacitor C_{SST}. Minimum value for soft start capacitor shall be designed such that, at startup, the output voltage exceeds the S2G threshold; $V_{FBH\_S2G\_inc}$, before the soft start expires which is when the voltage reaches $V_{SOFT\_START\_LOFF}$.

A long soft start time has the only side effect of a long fault retry time for a LED driver, therefore, to be on the safe side it is suggested to choose a soft start capacitor larger than the minimum necessary. A simplified formula which provides a sufficient startup fault mask is:

$$C_{SST} > 0.6 \cdot C_{\mathrm{COMP}}$$

Therefore, for this application $C_{SST} = C_{COMP} = 22$ nF has been chosen.

Attention: ***The above formula has been tested for output capacitor below 100 µF, effectiveness of soft start should be tested in the real application. Soft start network validation: Minimum temperature and minimum input voltage shall be considered as worst-case condition for previously mentioned dimensioning***

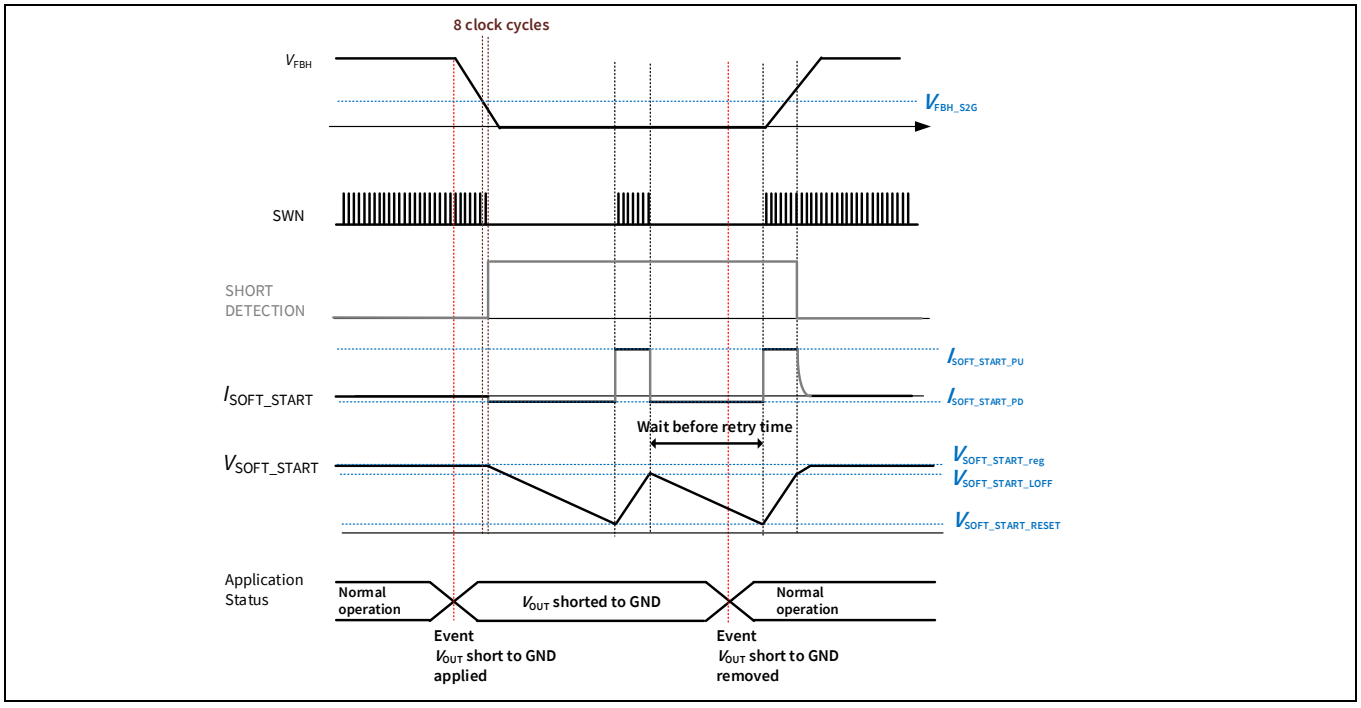

Figure 17 Wait before retry time

Wait time before retry (t_{retry}) in case of a fault is defined by:

$$t_{retry} = (V_{SOFT\_START\_LOFF} - V_{SOFT\_START\_RESET}) \cdot \frac{C_{SST}}{I_{SOFT\_START\_PD}} = (1.75\,V - 0.2V)\,\frac{22nF}{2.6uA} = 13.1\,ms$$

The first retry time after a fault is slightly longer than the following times, because the soft start capacitor during regulation stays at $V_{SOFT\_START\_reg}$ instead of $V_{SOFT\_START\_LOFF}$.

3.1 Input undervoltage protection

The input voltage requirement for the LED driver module is 6 V (extended range) therefore, the input undervoltage protection must be set below this threshold.

Even if theTLD5191ES has switch current limiter (R_{SWCS}) and gate driver undervoltage protection, it is better to set the undervoltage threshold above 5 V. This is to avoid stress on switching MOSFETs, due to increased input current and reduced gate driver voltage.

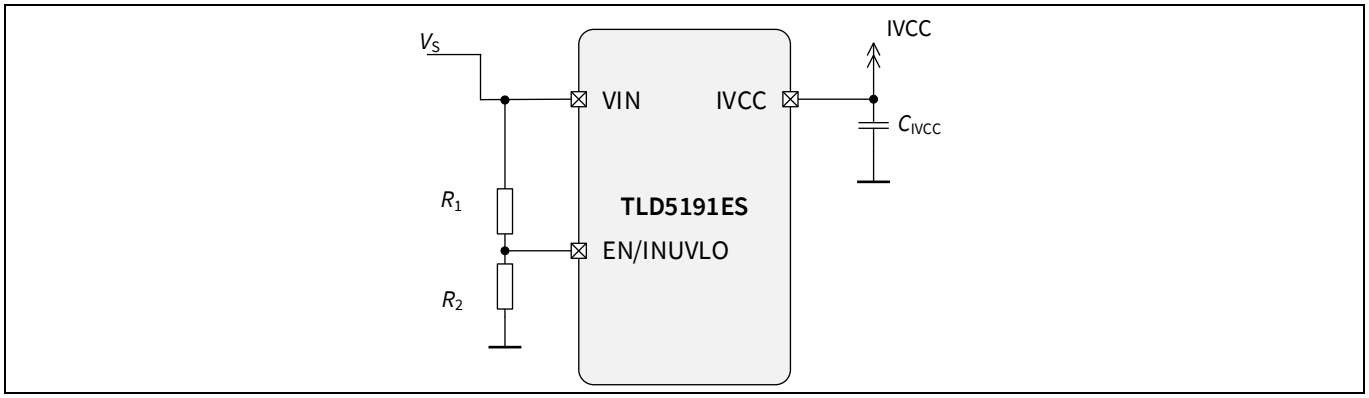

Figure 18 EN/INUVLO resistor divider

For this application an undervoltage threshold of 5.5 V (entry threshold, V_{IN} falling) has been chosen. The low-side resistor should be in the range of 2 kΩ to 10 kΩ to avoid excessive leakage current and to provide an accurate threshold.

Choosing R2 = 2.2 kΩ as low-side resistor, the high-side resistor (R1) is calculated as

$$R1 = R2 \cdot \frac{UV_{th} - V_{EN/INUVLO_{th}}}{V_{EN/INUVLO_{th}}} = 2.2\ k\Omega \cdot \frac{5.5\ V - 1.75\ V}{1.75\ V} = 4714\ \Omega$$

Standard value is R1 = 4.7 kΩ.

4 Compensation network

In this chapter the main stability equations are provided and an analytical approach can be completed in all the operating conditions.

A faster approach is to use the TLD5191ES excel component calculator [1], where several operating conditions and compensation networks can be quickly verified.

Good practice is to dimension the external components and check stability in corner cases, for example at minimum V_{IN} and maximum V_{OUT}, and maximum V_{IN} and minimum V_{OUT}.

The RC compensation network is applied to the COMP pin (proportional and integral compensation). In small signal approximation, the open loop transfer function of a DC-DC is the product of modulator transfer function and the feedback network transfer function.

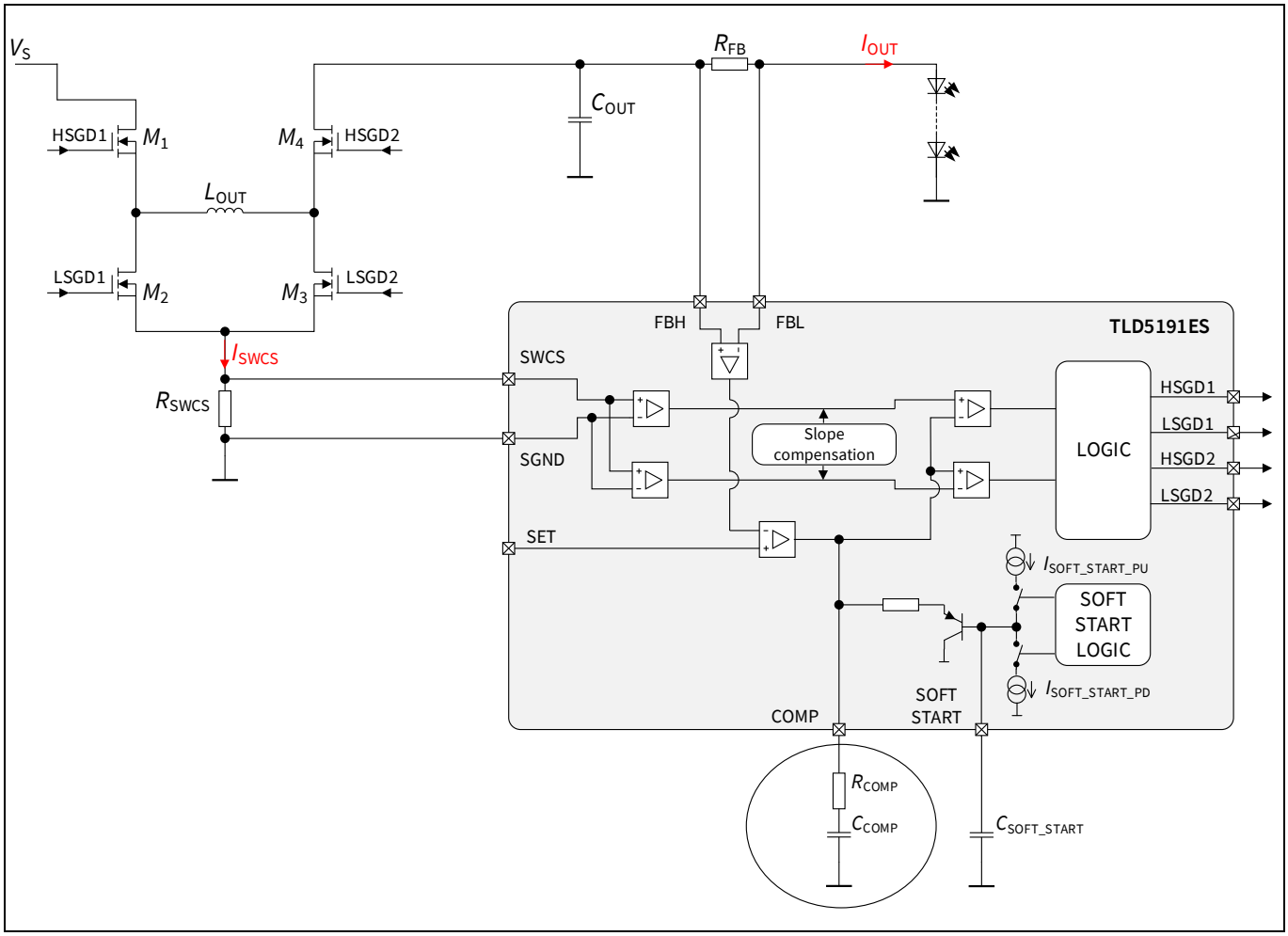

Figure 19 Compensation network schematic

The modulator transfer function can be expressed as the product of two main parts: the gain of the error amplifier and the gain of the current mode modulator. The equations are different if the device operates in boost mode or in buck mode.

Buck operating mode stability equations:

In buck mode, the gain of the error amplifier is described with the following formula:

$$A_{EA}(s) = g_{m\_EA} \cdot R_{EA} \cdot \frac{(1 + s \cdot \tau_{z1})}{(1 + s \cdot \tau_{p1})}$$

Where

- g_{m_EA} is the trans-conductance of the error amp. (A5, A6 with comprehensive gain $IFBx_{gm\_TYP}$ = 890 µs)
- R_{EA} is the output resistance of the error amplifier (R_{EA_TYP}= 6 MΩ)
- $\tau_{z1} = C_{COMP} \cdot R_{COMP}$ is the zero of compensation network
- $\tau_{p1} = (C_{COMP}) \cdot R_{EA}$ is the pole associated to compensation network and the resistor of error amplifier

Boost operating mode stability equations:

The gain of the current mode modulator can be described following the model presented by R.B Ridley [1].

Mathematically for boost, it is described as:

$$A_{CM\_BOOST}(s) = \frac{0.17 \cdot (1 - D) \cdot R_{LOAD}}{\left(1 + \frac{I_L \cdot (1 - D) \cdot R_{LOAD}}{V_{OUT}}\right) \cdot R_{swcs}} \cdot \frac{(1 + s \cdot \tau_{z2})}{(1 + s \cdot \tau_{p3}) \cdot \left(1 + \frac{s}{\omega_n \cdot Q} + \frac{s^2}{\omega_n^2}\right)}$$

$$A_{CM\_BOOST}(s) = \frac{0.17 \cdot (1 - D) \cdot R_{LOAD}}{\left(1 + \frac{V_{REF} \cdot R_{LOAD}}{V_{OUT} \cdot R_{FB}}\right) \cdot R_{swcs}} \cdot \frac{(1 + s \cdot \tau_{z2})}{(1 + s \cdot \tau_{p3}) \cdot \left(1 + \frac{s}{\omega_n \cdot Q} + \frac{s^2}{\omega_n^2}\right)}$$

$$I_L = \frac{V_{REF}}{R_{FB}(1 - D)}$$

Where:

- R_{LOAD} is the total resistor at the output of DC-DC and it is the sum of R_{FB} and R_{LED_string}
- V_{REF} is the voltage reference across FBH and FBL (typical 150 mV)
- V_{OUT} is the voltage on LED string V_{LED} plus input voltage V_{IN} (Voltage across PMOS has been neglected)
- $\tau_{z2} = -\frac{L_{BO}}{(1-D)^2} \cdot \frac{(I_{OUT})}{(V_{OUT})}$ is the zero (RHP) of the boost DC-DC with the return to battery
- $\tau_{p3} = C_{OUT} \cdot R_{LOAD} \cdot \frac{V_{OUT}}{I_{OUT} \cdot R_{LOAD} + V_{OUT}}$ is the pole associated with boost converter with the return to battery
- $\omega_n = \pi \cdot \frac{f_S}{2}$ is the natural pulsation of the system
- $Q = \frac{1}{\pi \cdot \left(\left(1 + \frac{S_e}{S_n}\right) \cdot (1 - D) - 0.5\right)}$ is the quality factor of a second order system, where S_e is the slope of current compensation circuit (coefficient fixed by internal references) and S_n is the slope of the current sensed by R_{SWCS}.

$$S_e = 60 \cdot 10^{-3} \cdot f_{sw}$$

$$S_n = \frac{V_{IN} \cdot R_{SWCS}}{L_{BO}}$$

Using the data previously calculated, it is possible calculate the gain in DC and cross over frequency f_c and the phase margin.

The transfer function of the feedback network is the ratio between R_{FB} and the R_{LED}

$$\beta = \frac{R_{FB}}{R_{FB} + R_{LED_{string}}}$$

For the gain calculation in typical conditions, the three parts ($A_{EA}(0)$, $A_{CM}(0), \beta$) to be calculated are shown below, calculated in an exemplary boost duty cycle of 50%:

$$A_{EA\_BOOST}(0) = g_{m\_EA} \cdot R_{EA} = 0.00089\ S \cdot 6\ M\Omega = 5340$$

$$A_{CM\_BOOST}(0) = \frac{0.17 \cdot (1-D) \cdot R_{LOAD}}{\left(1 + \frac{V_{REF} \cdot R_{LOAD}}{V_{OUT} \cdot R_{FB}}\right) \cdot R_{swcs}} = \frac{0.17 \cdot (1-0.5) \cdot 2.1\ \Omega}{\left(1 + \frac{0.15\ V \cdot 2.1}{27.9\ V \cdot 0.1\Omega}\right) \cdot 0.010\ \Omega} = 16.04$$

$$\beta = \frac{R_{FB}}{R_{FB} + R_{LED\_string}} = \frac{0.1\ \Omega}{2.1\ \Omega} = 0.0476$$

And then the gain in DC can be calculated as:

$$T(0)|_{dB} = 20 \cdot \log\left(A_{EA\_BOOST}(0) \cdot A_{CM\_BOOST}(0) \cdot \beta\right) = 20 \cdot \log(5340 \cdot 16.04 \cdot 0.0476) = 72.2\ dB$$

Poles and zeroes can be calculated with the above formulas.

For this application, with the given inductor and output capacitor, a good compromise for stability and transient response has been found with 22 nF C_{COMP} and 1 kΩ R_{COMP} at the compensation network.

A screenshot of the excel component calculator bode plots, gain&phase margin is shown on Figure 20. The excel on the screenshot was calculated for V_{IN} = 13.5 V, V_{OUT} = 30 V and all the external components as chosen in this application note.

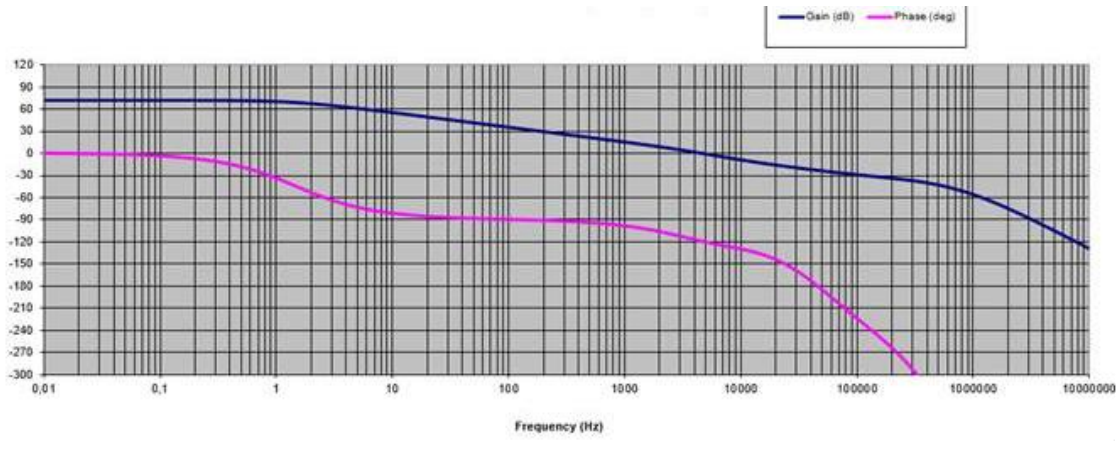

Figure 20 Bode plot and stability section, screenshot from TLD5191ES LED component calculator excel [1]

It is common practice to consider stable a system when the phase margin is above 45° and even better if closer to 60°.

Buck operating mode stability equations:

In buck mode, the gain of the error amplifier remains the same as the boost mode described above.

The current mode gain can be mathematically approximated as:

$$A_{CM\_BUCK}(s) = \frac{0.17 \cdot R_{LOAD}}{R_{swcs}} \cdot \frac{1}{(1 + s \cdot \tau_{p3}) \cdot \left(1 + \frac{s}{\omega_n \cdot Q} + \frac{s^2}{\omega_n^2}\right)}$$

Where:

- R_{LOAD} is the total resistor at the output of DC-DC and it is the sum of R_{FB} and R_{LED_string}
- V_{REF} is the voltage reference across FBH and FBL (typical 150 mV)
- V_{OUT} is the voltage on LED string V_{LED} plus input voltage V_{IN} (Voltage across PMOS has been neglected)
- $\tau_{p3} = C_{OUT} \cdot R_{LED}$ is the pole associated to buck converter with the return to battery
- $\omega_n = \pi \cdot \frac{f_S}{2}$ is the natural pulsation of the system
- $Q = \frac{1}{\pi \cdot \left(\left(1 + \frac{S_e}{S_n}\right) \cdot D - 0.5\right)}$ is the quality factor of a second order system, where S_e is the slope of current

compensation circuit (coefficient fixed by internal references) and S_n is the slope of the current sensed by R_{SWCS}.

$$S_e = 60 \cdot 10^{-3} \cdot f_{sw}$$

$$S_n = \frac{V_{OUT} \cdot R_{SWCS}}{L_{BO}}$$

Using the data previously calculated, it is possible to calculate the gain in DC and cross-over frequency f_c and the phase margin.

The transfer function of the feedback network is the ratio between R_{FB} and the R_{LED}

$$\beta = \frac{R_{FB}}{R_{LED\_string}}$$

For the gain calculation in typical conditions, the three parts $(A_{EA}(0)\ , A_{CM}(0), \beta)$ can be calculated are shown for the boost mode.

4.1 Stability tips

Phase margin could be improved by tuning some key components shown in Table 2. Each component may have some benefit, however there are also drawbacks in other aspects:

Table 2 Effect of tuning key components

Component	Improvement	Drawback
Increasing R_{SWCS}	Phase margin and enhance response to battery variation	Reduced maximum output
Increasing C_{COMP}	Phase margin	Slower response to battery variations
Decreasing R_{COMP}	Could improve margin in buck region	Possible reduced stability in boost mode, worsened response to battery variation
Increasing R_{COMP}	Could improve margin in boost region, enhanced response to battery variation	Possible reduced stability in buck mode
Increasing C_{OUT2} capacitor (capacitor placed after sensing resistor)	Phase margin in both buck and boost mode	Lowers cut frequency

5 EMC

5.1 Spread spectrum

The TLD5191ES offer a spread spectrum modulation that significantly improves the EMC in the lower frequency range of the spectrum (f < 30 MHz).

The effect of the spread spectrum on the output current is a ripple at the f_{DEV} spread frequency, which does not produce any visible flicker. The ripple produced by the spread spectrum is higher in buck mode than in boost mode.

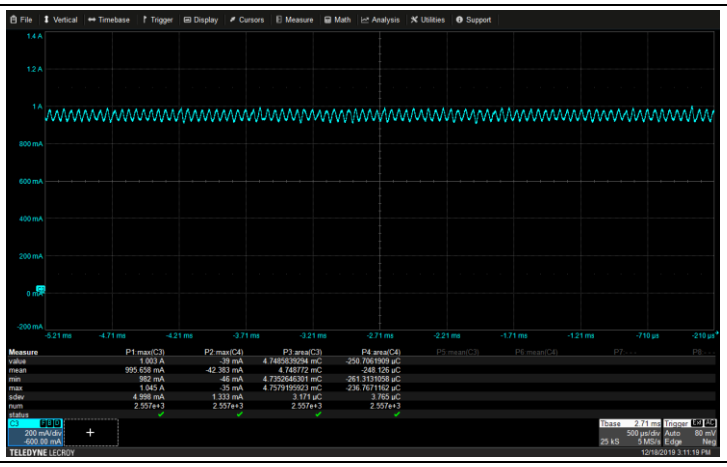

Figure 21 Spread spectrum I_{OUT} ripple

5.2 Gate driver resistors

Gate driver resistors are placed at the gate driver output in order to improve EMC performance. The effect of these resistors is to reduce switching nodes transition speed and ringing. Gate driver resistors impact the efficiency of the DC-DC converter, and they should be increased only to pass the target EMC regulation (for example, CISPR25).

The high-side gate driver resistor R_{G1} impacts only on the rise time for the buck switching node (SWN1), while the low-side gate driver resistor R_{G3} impacts the falling time of the boost switching node (SWN2).

For good EMC performance (Class 5 CISPR 25), the buck switching node rise-time and boost switching node fall-time should be in the 10 ns to 50 ns range.

The final EMC result depends on output voltage, switching frequency, PCB layout, cable length and other application parameters. Therefore, gate resistors should be tuned in the final application, after an EMC measurement.

With the current MOSFET choice, a 22 Ω gate resistor has been selected as starting point, with a measured rise time for the buck switching node of approximately 18 ns with a 4 LED load.

The impact of the efficiency is calculated with the TLD5191ES excel component calculator, at the maximum output power 45 W (30 V 1.5 A):

- 93.4% with 22 Ω gate resistor
- 95.65% with 0 Ω gate resistor

This resistor value could be increased or decreased after EMC measurement.

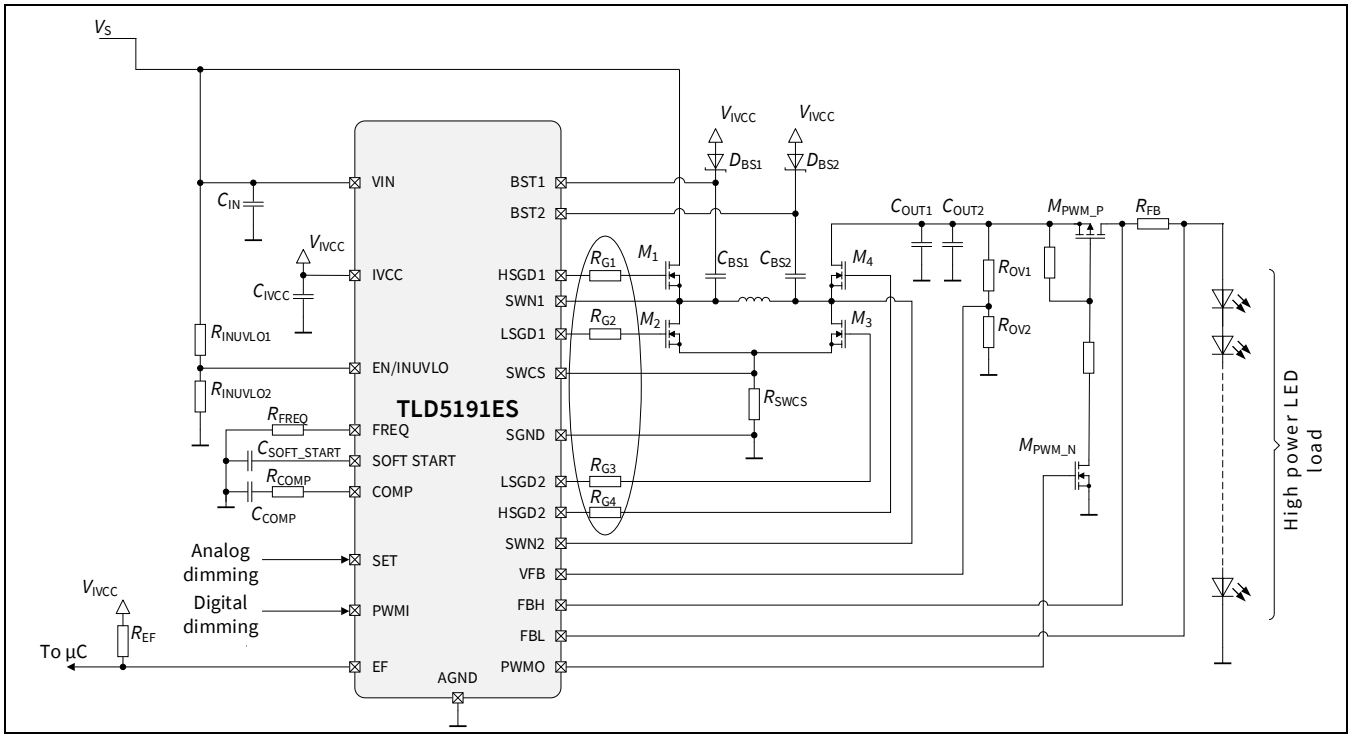

Figure 22 Gate driver resistors

5.3 Layout considerations

For a DC-DC converter, the PCB design is a critical task as well as the component selection. Even if the circuit topology and components selection are good, if the PCB layout is not good enough, the performance of the whole system will be lower than expected.

A proper layout is also the basis for good EMC performances.

In a dedicated application note: LITIX™ PCB design guideline document [3], the most important PCB layout rules are explained.

Figure 23 depicts a screenshot of this application.

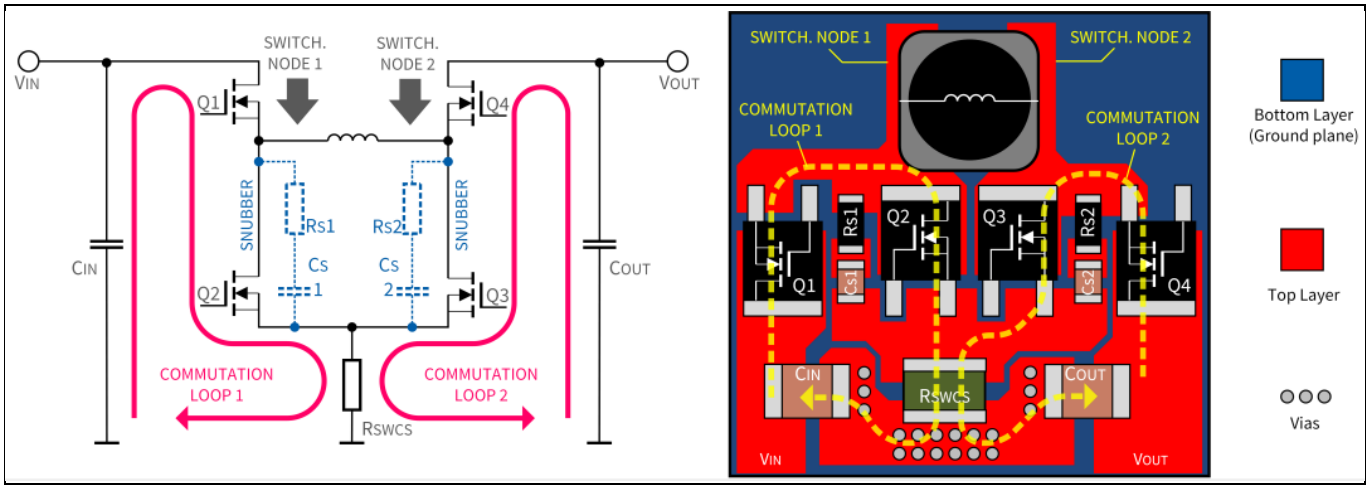

Figure 23 Hot loops and recommended layout for H-bridge topology

6 List of references

[1] Infineon_TLD5191ES_LED_Comp_calc-DevelopmentTools excel component calculator

[2] Ridley, R. B.; *A new Continuous Time Model for Current Mode Control*; IEEE Transaction on Power Electronics; Vol. 6; Issue 2; pp. 271-280; 1991

[3] Infineon-Z8F80033952-LITIX_PCB_design_guidelines-AN-v01_00

Revision history

Major changes since the last revision

Page or Reference	Description of change
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