LITIX™ Power TLD6098-1EP

Boost to ground LED driver for daytime running light

About this document

This document covers the design steps to create a DC-DC LED driver for automotive applications in boost to ground topology with TLD6098-1EP or likewise, each channel of TLD6098-2ES.

The equations for the choice of all the critical components needed are described.

Scope and purpose

The purpose of this application note is to inform the audience about many aspects related to the design of DC-DC converter for automotive lighting application and to offer a reliable solution with Infineon Technologies AG products. Moreover, the document addresses how to enable and to use many features of TLD6098-1EP.

Intended audience

This application note is intended for designer engineers who want to better understand how to design a DC-DC LED driver in boost to ground topology.

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1 Introduction

Boost to ground DC-DC always generates output voltage higher than input voltage. As an LED driver, the system regulates the output current and keeps it constant. TLD6098-1EP is a multitopology controller that can easily address these solutions.

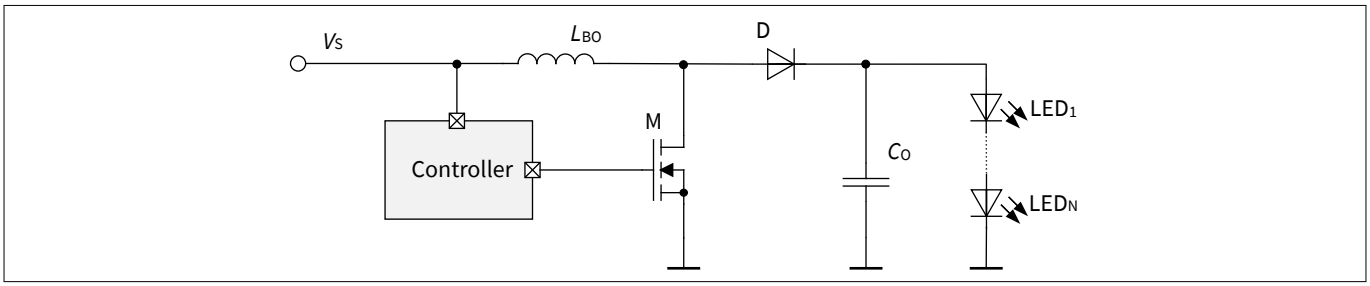

Figure 1 Boost to ground topology simplified

As previously mentioned, the boost DC-DC only generates higher output voltage than input voltage. In case of input voltage higher than output, a direct path from the battery to the output is present. This situation has a high risk of damaging the light source, because the output current flows into the load without any limitation.

1.1 Application assumption

The DC-DC fulfills the following requirements:

Table 1 DC-DC requirements

DC-DC requirements	
Light function	Daytime running light/Position light
LED string	12 x NJSW172CT (Nichia)
LED current	300 mA
LED current ripple	± 2% (peak to peak)
PWM dimming frequency	200 Hz
PWM duty cycle when position light is switched ON	10%
Voltage supply range	8 V to 26 V without performance degradation

The proposed design works with every kind of white LED with 3 V forward voltage and current ratings higher than 300 mA.

Thermal management of LED has to be considered by the user.

2 Main regulator design

A key parameter for the DC-DC design is the duty cycle (DC) of the PWM switching regulator. For a boost DC-DC it is described by means of:

$$D = 1 - \frac{V_{\mathrm{IN}}}{V_{\mathrm{OUT}}} \tag{1}$$

V_{OUT} is the voltage across the LED string that can be considered as an equivalent voltage source with an equivalent series resistor (Thevenin equivalent circuit transformation). The equivalent voltage source is the sum of all forward voltage of the LEDs in the string, while the equivalent resistor is the sum of all LED resistance. The LED resistance is calculated as incremental ratio of current versus voltage at around working point value.

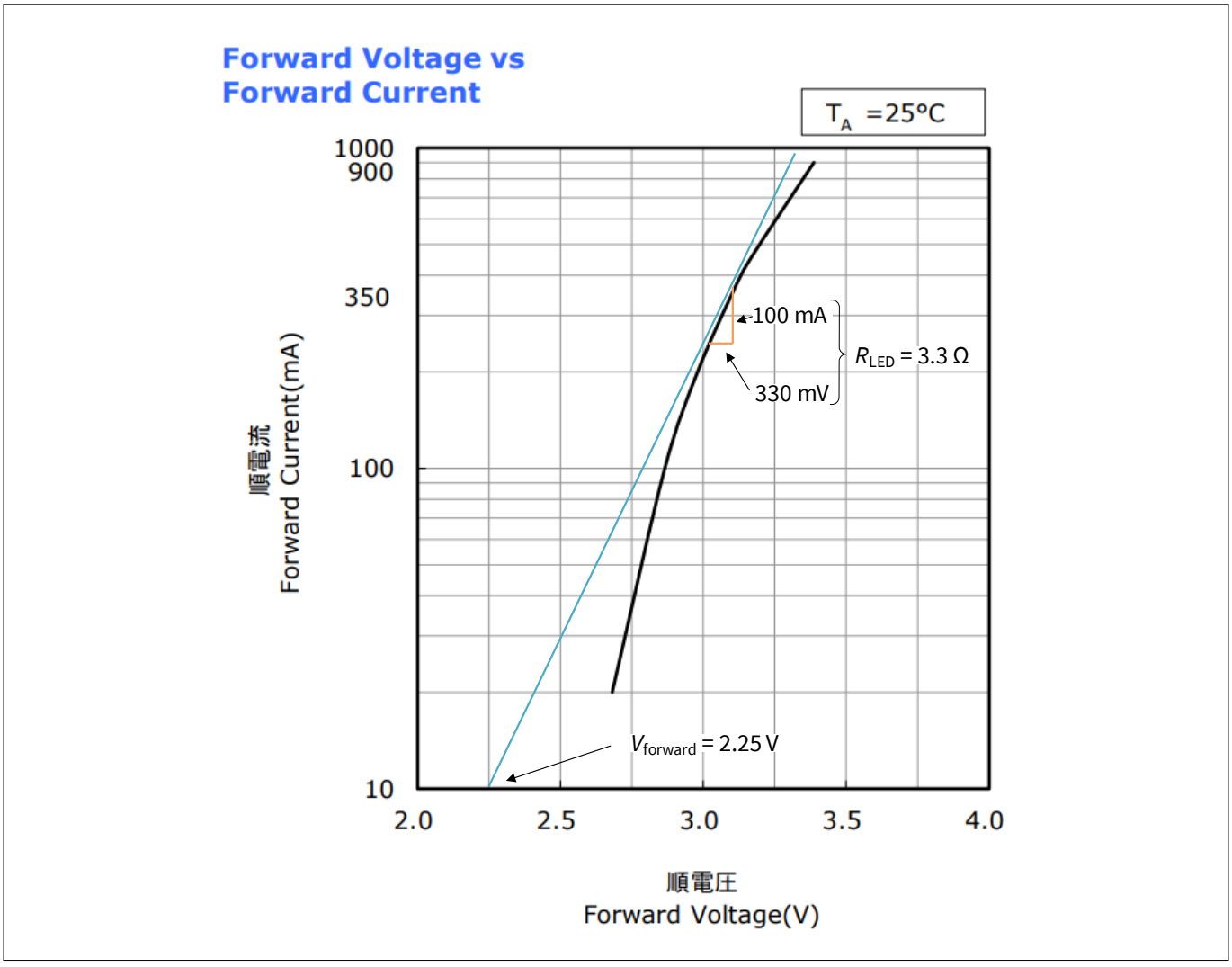

Figure 2 LED characteristic curve

For the LED considered in this application note, the string can be emulated by the equivalent parameters:

$$V_{LED} = \ \#\ LED \bullet V_{forward} = 12 \bullet 2.25\ V = 27.0\ V \tag{2}$$

$$R_{string} = \ \#\ LED \bullet R_{LED} = 12 \bullet 3.3\ \Omega = 39.6\ \Omega \tag{3}$$

With this equivalent circuit, the output voltage is:

$$V_{OUT} = V_{LED} + R_{string} \bullet I_{OUT} = 27.0\ V + 39.6\ \Omega \bullet 0.3\ mA = 38.9\ V \quad (4)$$

The duty cycles calculated at different input voltages are:

Table 2 Duty cycle and input voltage

Input voltage	Duty cycle (DC)
V_{IN} = 8 V (jump start)	0.79
V_{IN} = 13.5 V	0.65
V_{IN} = 26 V (load dump)	0.33

The average input current is also another key parameter to select the inductor and the switching elements. It is calculated in the corner cases battery voltage conditions by supposing 90% of overall efficiency

$$< I_{IN\_MAX} > = \frac{P_{OUT}}{V_{IN\_MIN} \bullet \eta} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN\_MIN} \bullet \eta} = \frac{38.9\ V \bullet 0.30\ A}{8\ V \bullet 0.9} = 1.62\ A \quad (5)$$

$$< I_{IN\_TYP} > = \frac{P_{OUT}}{V_{IN\_TYP} \bullet \eta} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN\_TYP} \bullet \eta} = \frac{38.9\ V \bullet 0.30\ A}{13.5\ V \bullet 0.9} = 0.96\ A \quad (6)$$

$$< I_{IN\_MIN} > = \frac{P_{OUT}}{V_{IN\_MAX} \bullet \eta} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN\_MAX} \bullet \eta} = \frac{38.9\ V \bullet 0.30\ A}{26\ V \bullet 0.9} = 0.50\ A \quad (7)$$

2.1 Inductor selection

The inductor in the boost converter is selected by fixing a certain ratio between average current and ripple current (as peak to peak measurement) in typical condition $\triangle I_{L\_TYP}$. A current ripple in the range of 40% (or ±20%) to 80% (or ± 40%) of the average inductor current is, in general, a good compromise between inductor size (that is proportional to weight and cost), and EMI performances. In this application ±40% ripple current has been chosen. Moreover, a continuous conduction mode (CCM) at all battery levels helps to reduce the electromagnetic interference generated by pulsated input current occurring when the DC-DC works in discontinuous conduction current (DCM). Then two equations are needed to choose he correct inductor value.

The first equation determines the inductor value to fix the ripple current at the typical input voltage:

$$L_{MIN1} \geq D_{TYP} \bullet \frac{V_{IN_{TYP}}}{\Delta I_{L_{TYP}} \bullet f_{SW}} = 0.68 \bullet \frac{13.5\ V}{2 \bullet 0.4 \bullet 0.96\ A \bullet 400\ kHz} = 29.9\ \mu H \quad (8)$$

The second equation determines the minimum inductor value to prevent DCM at the maximum battery voltage (i.e. worst case with minimum inductor current)

$$L_{MIN2} \geq D_{MIN} \bullet \frac{V_{IN_{MAX}}}{2 \bullet < I_{IN_{MIN}} > \bullet f_{SW}} = 0.33 \bullet \frac{26\ V}{2 \bullet 0.50\ A \bullet 400\ kHz} = 21.4\ \mu H \quad (9)$$

The closest standard value that satisfies both equations is 33 µH.

With this value, the actual maximum ripple current (i.e. when input voltage is at minimum) is:

$$\Delta I_{L(P-P)\_MAX} = DC_{MAX} \bullet \frac{V_{IN_{MIN}}}{L \bullet f_{SW}} = 0.79 \bullet \frac{8\ V}{33\ \mu H \bullet 400\ kHz} = 0.48\ A \quad (10)$$

And then, the maximum peak current into inductor is:

$$I_{L\_MAX} = \ < I_{IN\_MAX} > \ + \frac{\Delta I_{L(P-P)\_MAX}}{2} = 1.62\ A + 0.24\ A = 1.86\ A \quad (11)$$

To avoid any performance degradation, the saturation current and the rated current of the inductor have to be higher than 1.86 A.

An inductor that fulfills the above requirements (nominal inductor value and saturation current) is the Coilcraft XAL7050-333ME.

2.2 Output capacitor selection

The output capacitor acts as an energy tank when the rectifier diode D is in reverse polarity and for this reason it has to sustain a high ripple current. This component affects the system bandwidth and also the LED current ripple. Usually, for this kind of application multi-layer ceramic capacitors (MLCC) with low ESR are preferred to the electrolytic capacitors.

The figure below depicts how the system manages the current into reactive components and LED string.

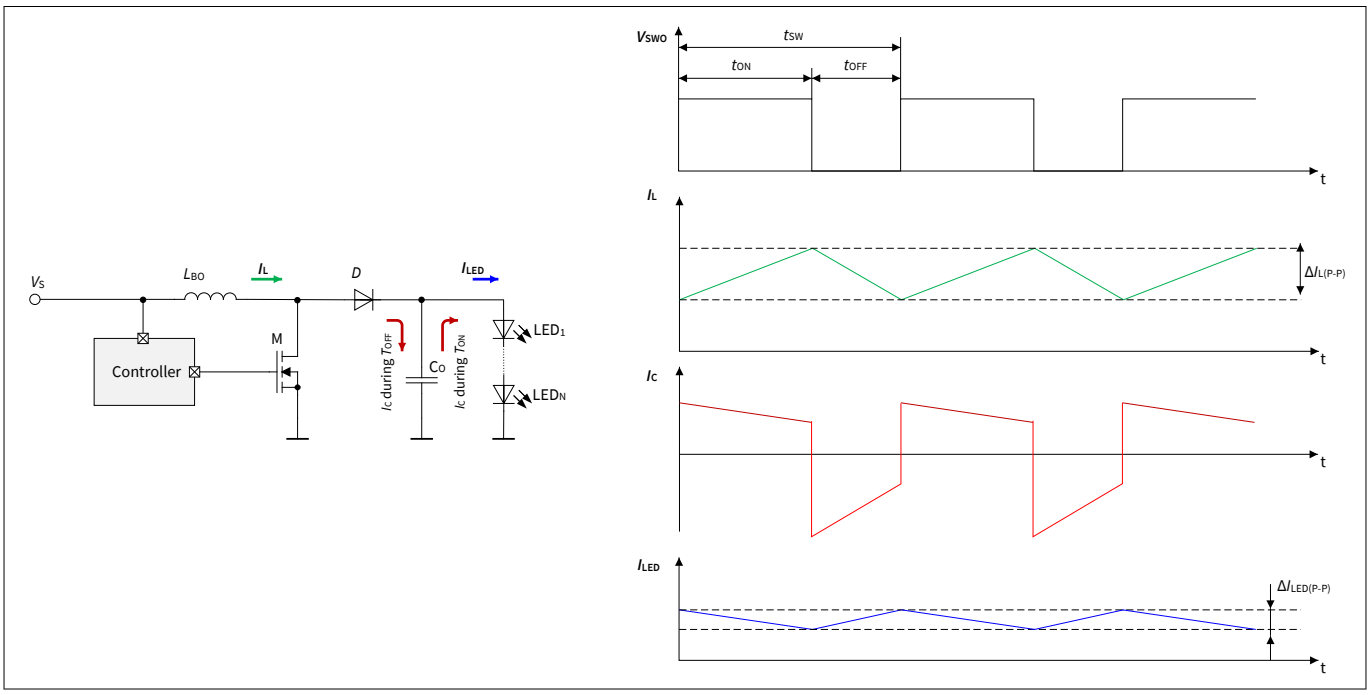

Figure 3 Waveform of current in reactive components and LED string

The output voltage ripple required by the application can be approximated by:

$$\Delta V_{OUT} = \Delta I_{OUT} \bullet R_{LOAD} = 0.30\ A \bullet 2 \bullet 0.02 \bullet 39.6\ \Omega = 0.475\ V \quad (12)$$

The minimum capacitor to ensure such voltage ripple can be calculated by assuming a constant current discharge of the output capacitance (equal to average output current) during the t_{ON}. The worst-case scenario is with the maximum DC and it is calculated by means the formula below:

$$C \geq \frac{I_{OUT}}{\Delta V_{OUT}} \bullet \frac{DC_{MAX}}{f_{SW}} = \frac{0.30\ A}{0.475\ V} \bullet \frac{0.79}{400\ kHz} = 1.25\ \mu F \quad (13)$$

The equivalent series resistor (ESR) of the capacitor affects the output voltage ripple as well.

Its effect can be calculated during two phases:

- During capacitor discharging it can be described by:

$$\Delta V_{ESR\_DIS} = R_{ESR} \bullet I_{OUT} \quad (14)$$

- During the charging phase it can be described by:

$$\Delta V_{ESR\_CHG} = R_{ESR} \bullet (I_L - I_{OUT}) \quad (15)$$

To make it negligible (for example less than 10% of the ripple imposed by capacitor), its contribution has to be lower than ΔV_{OUT} on both cases. From the equations above, it is possible to calculate the maximum ESR acceptable by the application.

$$R_{ESR\_DIS} \leq \frac{\Delta V_{ESR}}{I_{OUT}} = \frac{0.1 \bullet \Delta V_{OUT}}{I_{OUT}} = \frac{0.1 \bullet 0.475\ V}{0.30\ A} = 158\ m\Omega \quad (16)$$

$$R_{ESR\_CHG} \leq \frac{\Delta V_{ESR}}{I_{L\_MAX} - I_{OUT}} = \frac{0.1 \bullet \Delta V_{OUT}}{I_{L\_MAX} - I_{OUT}} = \frac{0.1 \bullet 0.475\ V}{1.86\ A - 0.30\ A} = 30\ m\Omega \quad (17)$$

To fulfil both equations, ESR of capacitor bank has to be lower than 30 mΩ that is a reasonable value for a ceramic capacitor.

Just a reminder: MLCC capacitors shows quite good value of capacitance related to small package and also very good performances related to ESR, but the variation of the capacitance as a function of the applied voltage is very high. During the selection this degradation has to be considered and in such a case, use an adequate parallel of capacitors to overcome this drawback. As an example, here below the behavior of TDK CGA9N2X7R2A475K230KA is shown in the figure below. The capacitor is rated 100 V. When biased at V_{OUT} = 38.9 V, it shows about 30% drop of its nominal value.

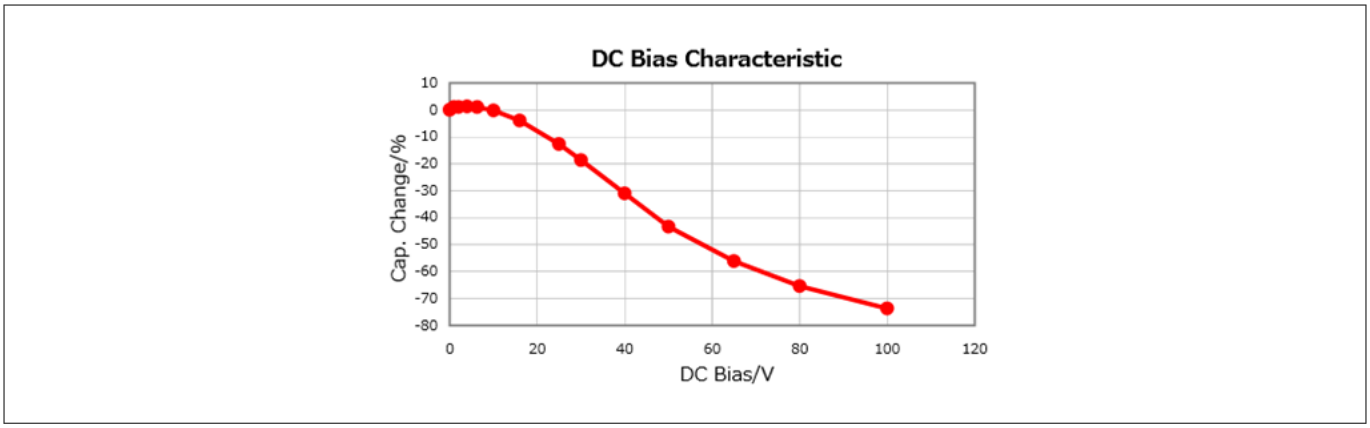

Figure 4 DC bias characteristic of TDK CGA9N2X7R2A475K230KA_pdf

For the application here described, a good choice is to place 2 capacitors in parallel and that means the actual output value at maximum output voltage is

$$1\mu \cdot 2 \cdot (1 - 0.30) = 1.4\mu F \tag{18}$$

2.3 Input PI-filter

The PI filter at the input of the DC-DC is a common choice to filter out the undesired frequency components that affect the spectrum in the standardized bands.

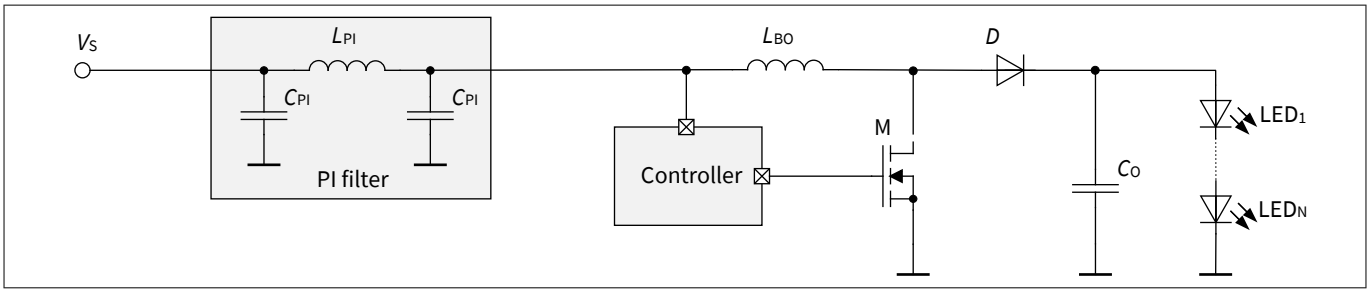

Figure 5 PI filter schematic simplified

Parasitic effects on capacitors C_{PI} and inductor L_{PI} shape the frequency response of the filter and for this reason its maximum absorption is in the frequency window 5 to 10 MHz. A good PCB layout helps to reduce the EMI emission at higher frequency.

To achieve good EMI results, the filter has to reduce the emissions of the switching frequency harmonics usually located in AM band.

To design the PI filter, the following rules of thumb can be used:

- Select L_{PI} equal to $1/10 \cdot L_{BO} = 3.3\mu H$
- Select the corner frequency of PI filter to 1/10 of the switching frequency of DC-DC then:
  $f_{PI} = 0.1 \cdot f_{SW} = 40kHz$
- Have equal capacitance distribution on both sides of PI-Filter and value:

$$C_{PI} = \frac{1}{4 \bullet \pi^2 \bullet L_{PI} \bullet f_{PI}^2} = \frac{1}{4 \bullet \pi^2 \bullet 3.3\ \mu H \bullet (40\ kHz)^2} = 4.8\ \mu F \tag{19}$$

For this purpose, CGA5L3X7R1H475K160AB is a good candidate for the capacitors while the inductor could be SPM4015T-3R3M-LR.

2.4 Transistor selection

The switching behavior is shown in the figure below.

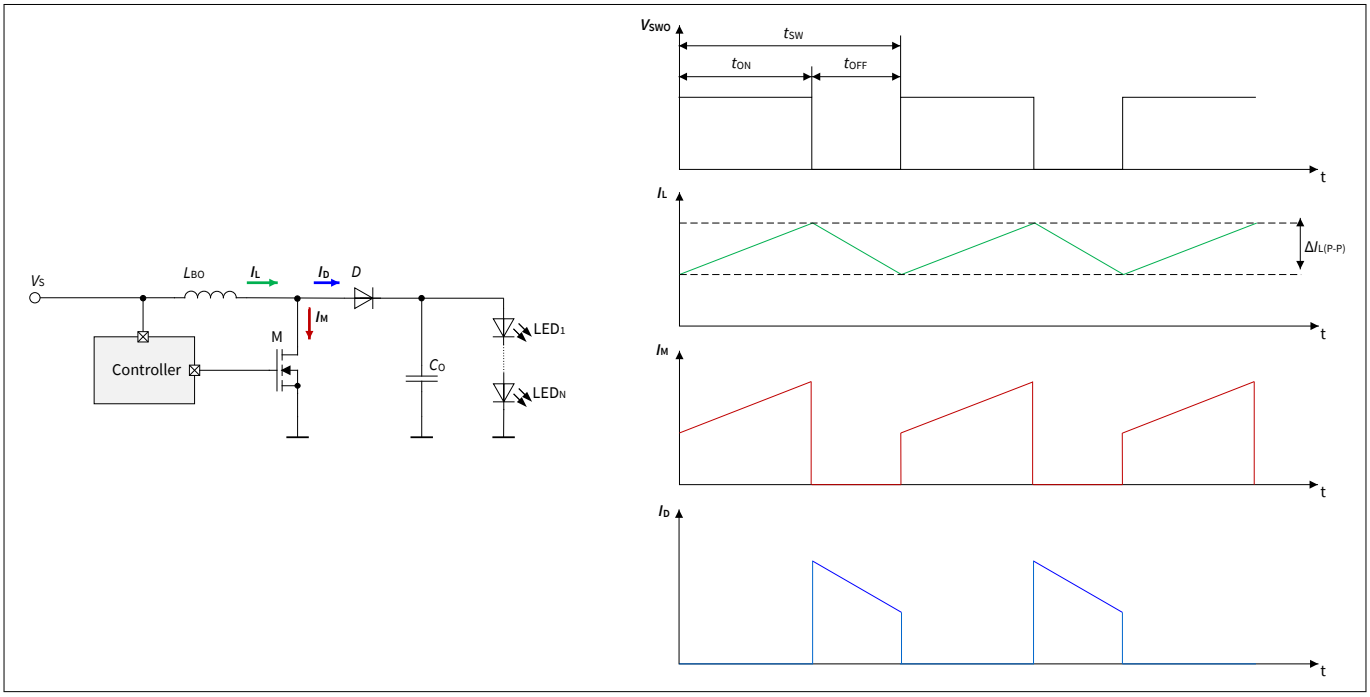

Figure 6 Waveform of current in-power devices and inductor

During the ON state, the current flowing into the MOSFET is the same as the current flowing into the inductor and its maximum is:

$$I_{MOS\_MAX} = I_{L\_MAX} = \ < I_{IN\_MAX} > \ + \frac{\Delta I_{L(P-P)\_MAX}}{2} = 1.62\ A + 0.24\ A = 1.86\ A \quad (20)$$

Moreover, during the OFF state, the MOSFET sustains a voltage between drain and source equal to the output voltage (voltage drop on diode is neglected). For this application it is 41 V and then 60 V rating MOSFET has to be chosen.

For EMI reason, it is common practice to put in series a R_{GATE} resistor of approximately 10 Ω to 20 Ω. This helps in reducing the current spikes into the gate and also having smooth transition from the OFF state to ON state. On the other hand, this lowers the overall efficiency of the converter.

Infineon offers a wide variety of MOSFET suitable for this purpose; IPD25N06S4L-30 is a good compromise of gate charge (to reduce switching losses) and $R_{DS(ON)}$ (to reduce the conduction losses)

2.5 Diode selection

The diode is the rectification device of the asynchronous DC-DC. To reduce losses, Schottky diodes should be used. The forward current rating of the diode has to be higher than the LED current. Selecting a component with low forward voltage helps to reduce the losses and the PCB area as well.

During the ON state of the transistor, the voltage across the diode is V_{OUT} = 38.9 V (voltage drop on the transistor is neglected). To take same margin, 60 V Schottky diode has to be selected.

A good choice for this kind application could be the Vishay VSS8D2M6 that provides quite low forward voltage of about 0.5 V .

2.6 Selection of current sense resistors

Two current sense resistors are needed to detect the current into the switching transistor and the output current.

R_{SWCS} is used to sense the inductor current needed for the current mode control loop. Moreover, it enables the current limit protection when the voltage across the resistor reaches the switch current limit threshold V_{SWCS_TH} (100 mV). This protection disables the gate driver for one clock cycle. For proper behavior, this protection must not be triggered even during the fast input voltage transitions.

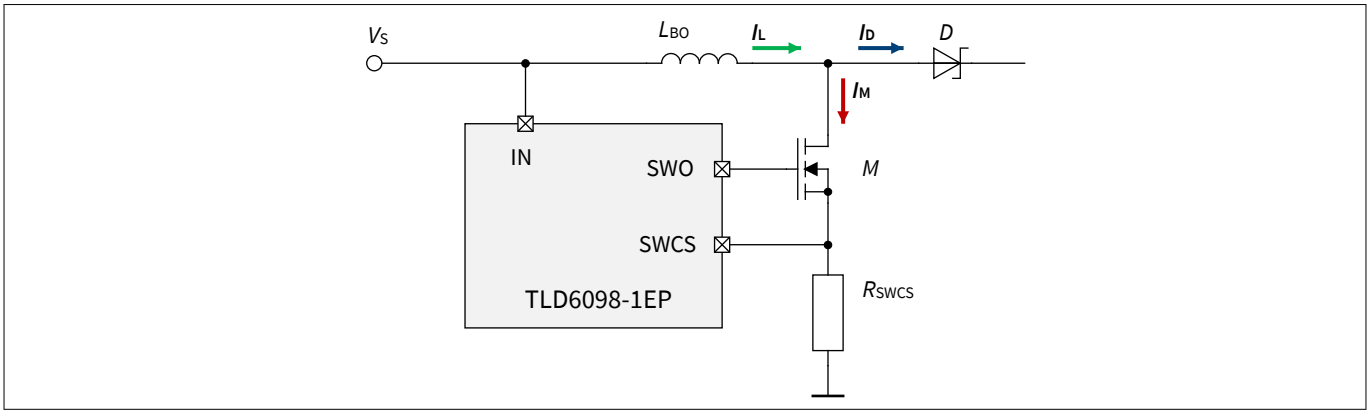

Figure 7 Peak current sensing resistor

Considering the corner case of transition to the minimum V_{IN} (transient undervoltage) the system could face a possible overshoot of the input current up to 150% (if the system has 45° of phase margin). In this case, the R_{SWCS} can be calculated by:

$$R_{SWCS} < \frac{V_{SWCS\_TH}}{1.5 \bullet I_{L\_MAX}} = \frac{100\ mV}{1.5 \bullet 1.86\ A} = 36\ m\Omega \tag{21}$$

To provide for a margin of tolerance, 22 mΩ is a good choice (this choice influences also the stability of DC-DC, that is evaluated in the following chapter). The root mean square (RMS) current that flows into the resistor is equal to the current flowing into power NMOS and its value is:

$$I_{T_{RMS\_MAX}} = \sqrt[2]{\frac{1}{T}\int_0^T I_{MOS}(t)^2 dt} = \sqrt[2]{\frac{1}{T}\int_0^T \left(\frac{(I_T + \Delta I_T - I_T + \Delta I_T) \bullet t}{T_{ON}} + (I_T - \Delta I_T)\right)^2 dt}$$

$$= \sqrt{\frac{D}{3}\left(I_{MOS\_MIN}^2 + I_{MOS\_MIN} \bullet I_{MOS\_MAX} + I_{MOS\_MAX}^2\right)} = \sqrt{\frac{0.79}{3}\left(1.38^2 + 1.38 \bullet 1.86 + 1.86^2\right)} \tag{22}$$

$$= 1.44\ A$$

The power dissipated by R_{SWCS} is then:

$$P = R_{SWCS} \bullet I_{NMOS}^2 = 22\ m\Omega \bullet (1.44\ A)^2 = 45.6\ mW \tag{23}$$

To avoid overheating of the resistor it is a common practice to use resistors with 4-5 times power rating needed; for this application low inductive component has to be chosen, and the RCWL2010R022JQ satisfies the requirements.

R_{FB} is used to sense the output current. The controller adjusts the switching duty cycle to keep the voltage across the resistor R_{FB} equal to the current loop reference voltage $V_{REF(100\%)}$. The sensing resistor can be calculated by:

$$R_{FB} = \frac{V_{REF(100\%)}}{I_{OUT}} = \frac{0.15\ V}{0.30\ A} = 0.5\ \Omega \tag{24}$$

This value is not available in the standard E6 series, but it can be managed with two 1 Ω resistors in parallel. The power rating of these resistors is:

$$P = R_{FB} \bullet I_{OUT}^2 = 1\ \Omega\ \bullet (0.15\ A)^2 = 22.5\ mW \tag{25}$$

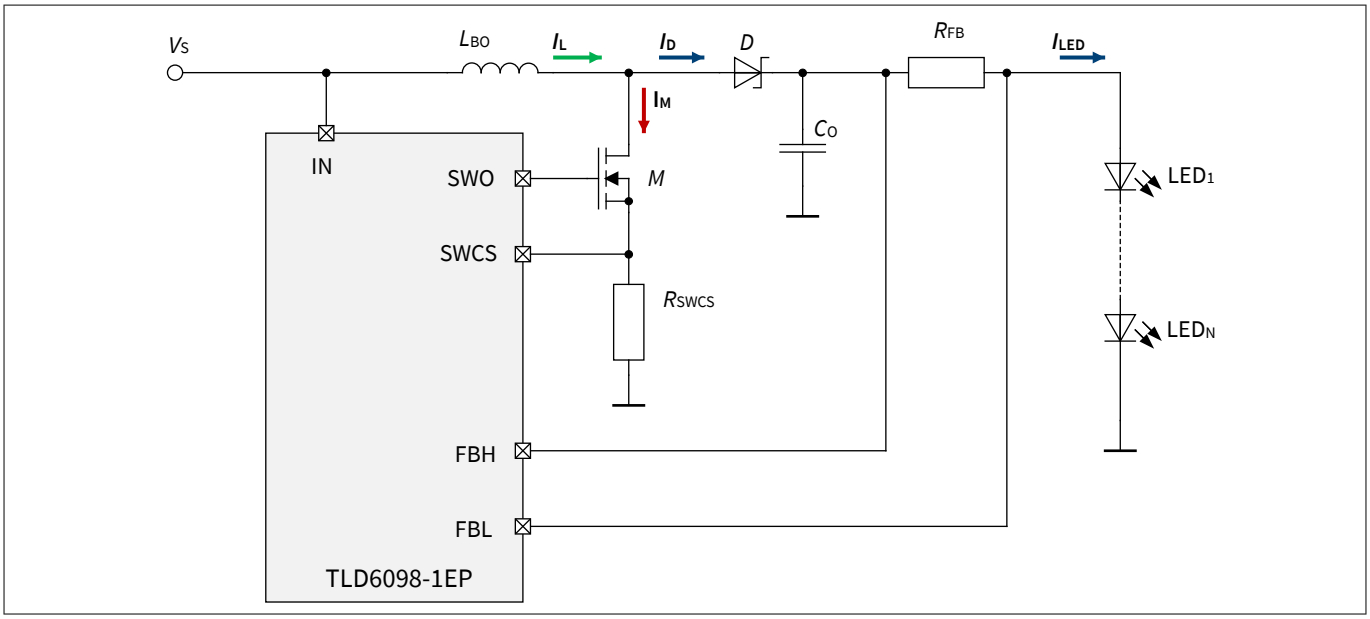

Figure 8 Output current sensing resistor

3 Features of application design

The TLD6098-1EP embeds many features to help the designer to realize a fully working system without the use of a microcontroller or lowering the complexity of the code if microcontroller is used.

3.1 Embedded PWM engine design

Embedded PWM engine is a feature can be used to reduce the LED brightness without showing color shift on LED. A user-case is to reduce the brightness from 100% to 10% when the light source is dimmed from daytime running light (DRL) to a position light (PL).

The PWM signal internally generated controls the gate drivers (connected to SWO pin and PWMO pin) to shape the output current wafer.

The generated duty cycle is proportional to the voltage on DC/PWMI pin. The voltage necessary to achieve the desired DC is:

$$\begin{aligned} V_{DC/PWMI} &= V_{DC/PWMI(0\%)} + DC \bullet \left(V_{DC/PWMI(100\%)} - V_{DC/PWMI(0\%)}\right) \\ &= 1\,V + 0.1 \bullet \left(3.6\;V - 1\,V\right) \\ &= 1.26\,V \end{aligned} \tag{26}$$

This voltage can be generated by a resistor divider from IVCC.

The position light function is enabled with a positive signal higher than the MOSFET threshold on the “Position light terminal”.

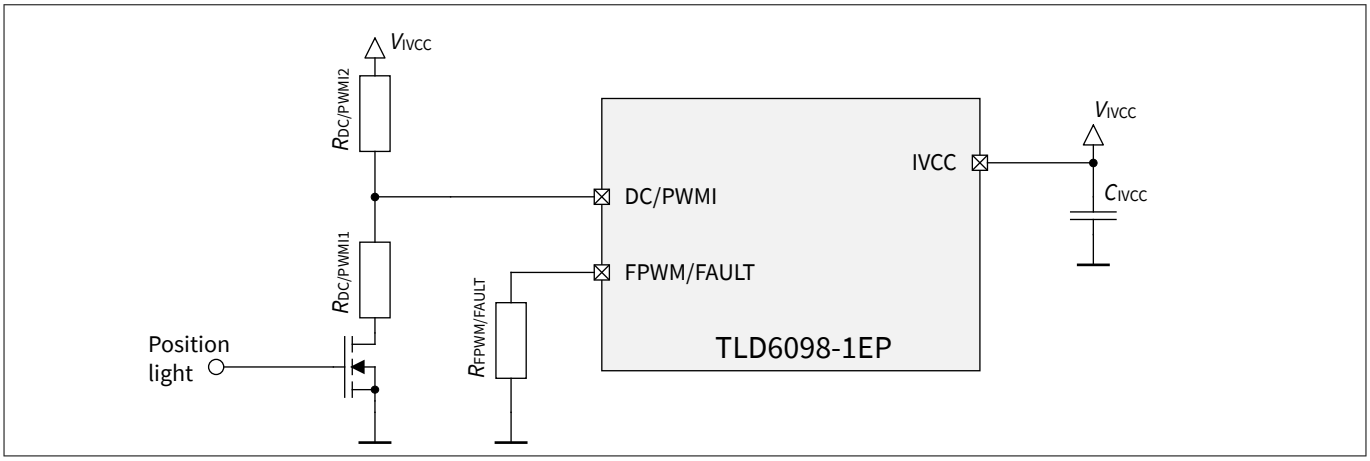

Figure 9 Embedded PWM engine schematic

3.2 Dimming element

The TLD6098-1EP embeds a PMOS gate driver to implement the dimming and the load protection.

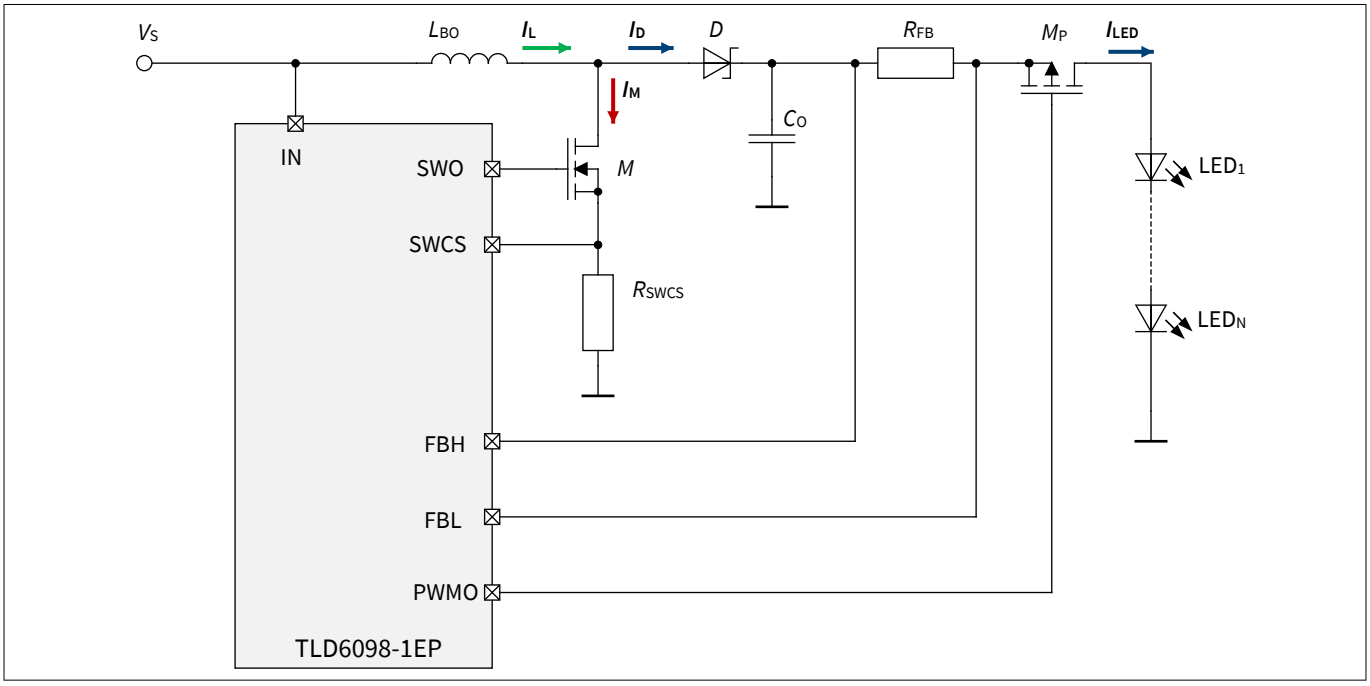

Figure 10 Dimming PMOS setup

T_{DIM2} manages the load current then the rating current of transistor is 300 mA, while when the transistor is in open state, its V_{GS} can reach 60 V. An Infineon component suitable for this application is BSR315P.

3.3 Spread spectrum

The spread spectrum modulator helps the designer to solve the EMI issues by moving the power from the narrow peaks of the spectrum into a broad band signal. It is easily activated by selecting the correct resistor set.

To switch at 400 kHz with spread spectrum activated, a resistor can be selected by equation:

$$R_{FREQ\_SSM(ON)} = \frac{1}{\left(1.11 \bullet 10^{-9} \bullet f_{FREQ}\right)} = \frac{1}{\left(1.11 \bullet 10^{-9} \bullet 400\ kHz\right)} = 2.25\ k\Omega \quad (27)$$

Therefore, 2.26 kΩ (E96 series) has to be selected and connected between pin 11 and ground.

3.4 Overvoltage protection

This feature limits the output voltage in case of open fails of the load (for example if the load is disconnected). This voltage has to be higher than the maximum output voltage. Therefore, 48 V is a good value to account for components spread variations.

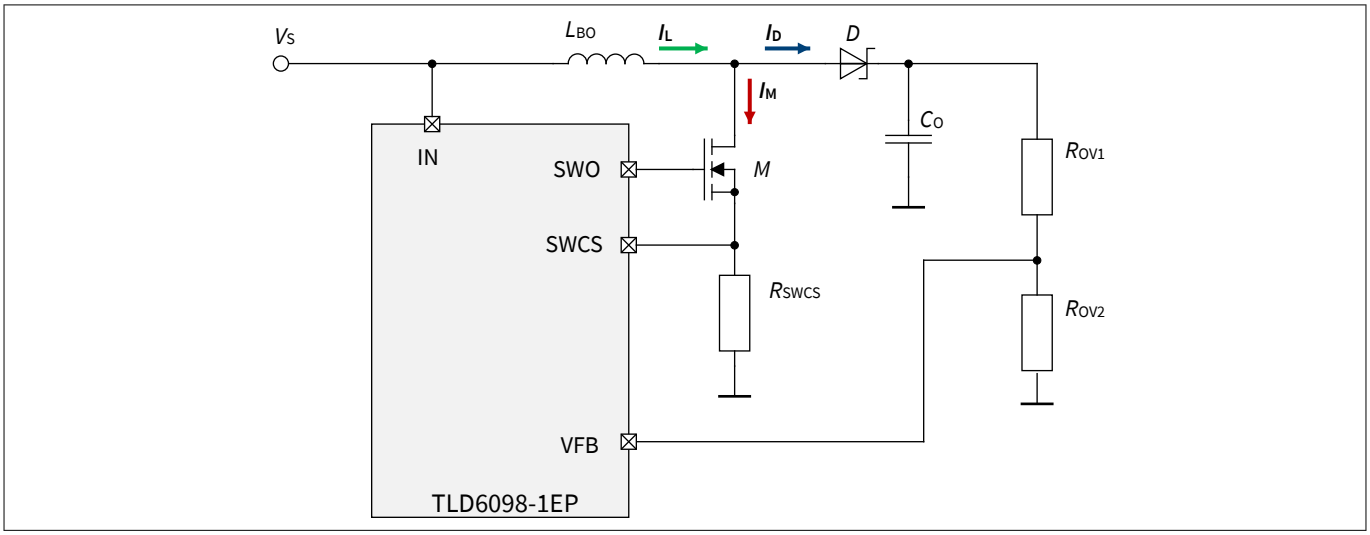

Figure 11 Overvoltage protection schematic

Overvoltage is triggered when the voltage on VFB pin reaches 1.6 V. Fixing R_{OV2} at 2 kΩ to ensure low current consumption and good noise immunity, R_{OV1} can be calculated as:

$$R_{OVH} = \frac{R_{OV2} \bullet (V_{OUT\_MAX} - V_{OVFB\_OV})}{V_{OVFB\_OV}} = \frac{2\ k\Omega\ \bullet (48\ V - 1.6\ V)}{1.6\ V} = 58\ k\Omega \quad (28)$$

3.5 Fault report

The system has been designed to use hard threshold for overvoltage detection. With this option, once the threshold is reached, the gate driver is disabled until the output voltage goes below the reset threshold.

This behavior is selected with a resistor on FPWM/FAULT pin in range 18 kΩ to 90 kΩ. A resistor of 68 kΩ must be used to adjust the PWM dimming frequency at 200 Hz.

In this case each fault type is reported by the FPWM/FAULT pin with a dedicated PWM waveform. Typical values for these waveforms are:

Table 3 Coded PWM pulses on FPWM/FAULT pin

	PWM period	DC (ON time)
Overtemperature	10 ms	100% (10 ms)
Short to ground	10 ms	80% (8 ms)
Overvoltage on FBH pin	10 ms	60 % (6 ms)
Overvoltage on VFB pin	10 ms	40% (4 ms)
Output overcurrent (> 200%)	10 ms	20% (2 ms)

4 Compensation network

The TLD6098-1EP regulates the output current by means of a peak current control loop. This configuration is a multiple-loop control mode method that has two loops:

- The inner current loop
- The outer voltage loop

The benefit of this approach compared with the single voltage loop approach are the increased noise immunity and the better frequency response.

An internal slope compensation avoids any subharmonics oscillations at high duty cycle that are characteristic of this control method.

The device has a dedicated pin where a compensation network is applied.

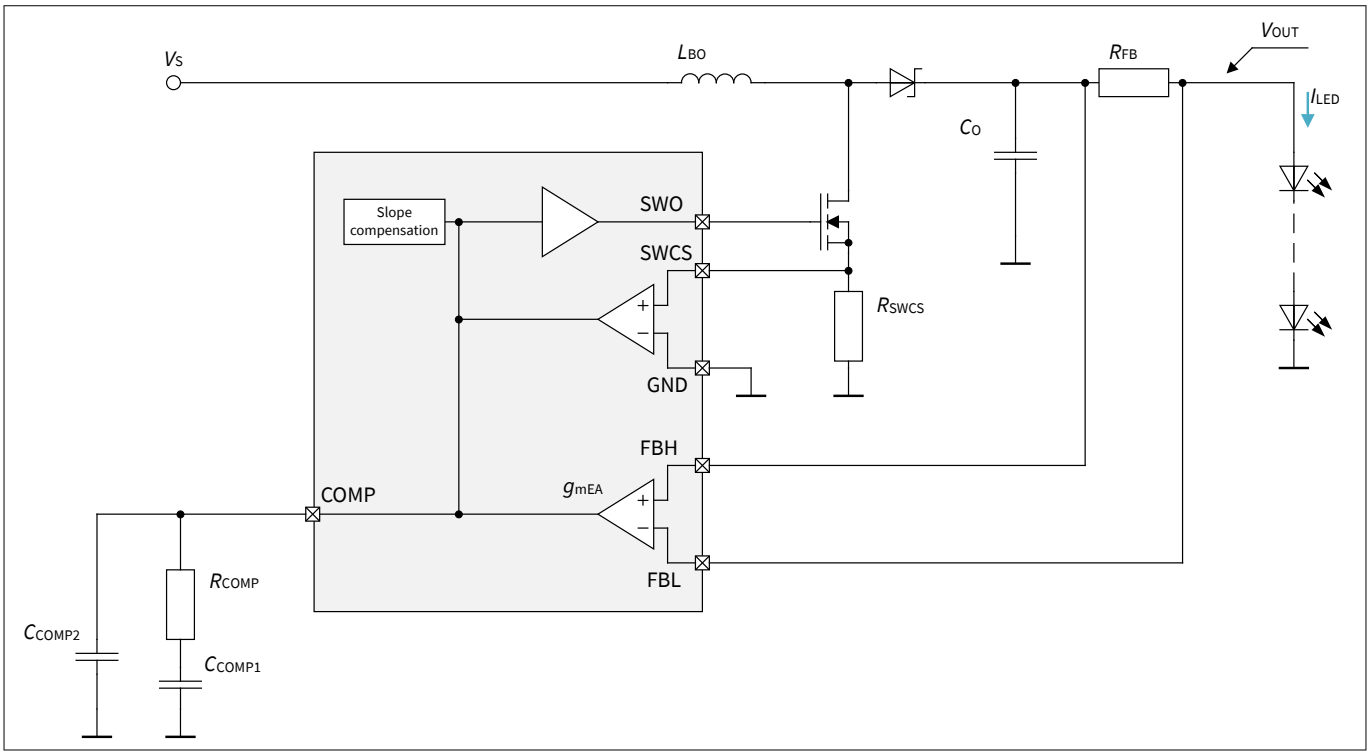

Figure 12 Compensation network schematic

The system can be simulated by using the space averaging model available in literature.

The power stage of the LED driver in boost configuration is mathematically described by:

$$G_{PS}(s) = \frac{\widehat{v_{OUT}}}{\widehat{v_{COMP}}} = \frac{(R_{FB} + R_{string}) \bullet (1 - D)}{2 \bullet R_{SWCS}} \bullet \frac{(1 + s\tau_{ESR})(1 - s\tau_{rhpz})}{1 + s\tau_P} \bullet He\left(s\right) \quad (29)$$

The pole is dominated by the load and the output capacitor:

$$f_P = \frac{1}{R_{LOAD} \bullet C_{OUT}} \quad (30)$$

One zero is generated by the ESR of the output capacitor

$$f_{ESR} = \frac{1}{R_{ESR} \bullet C_{OUT}} \tag{31}$$

And the right half plane zero of the boost converter depends on load, inductor size input and output voltage.

$$f_{rhpz} = \frac{R_{LOAD}}{L} \bullet \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \tag{32}$$

Finally, the He(s) models the inner current loop as well as the slope compensation

$$He(s) = \frac{1}{1 + \frac{s \bullet \left[\left(1 + \frac{S_e}{S_n}\right) \bullet (1 - D) - 0.5\right]}{2\pi \bullet f_{SW}} + \frac{s^2}{(2\pi \bullet f_{SW})^2}} \tag{33}$$

where S_e is the slope of current compensation circuit (coefficient fixed by internal references) and $S_n$is the slope of the current sensed by R_{SWCS}.

$$S_e = 50 \bullet 10^{-6} \bullet f_{SW} \tag{34}$$

$$S_n = \frac{V_{IN} \bullet R_{SWCS}}{L_{BO}} \bullet 10^{-3} \tag{35}$$

To achieve the open loop transfer function, the power stage transfer function has to be multiplied by the voltage gain from *vout(s)* to *vcomp(s)*. With the assumption that $C_{COMP2} << C_{COMP1}$, the gain of the transfer function is:

$$T_{EA}(s) = g_{m2} \bullet R_{EA} \bullet \frac{(1 + sC_{COMP1}R_{COMP})}{(1 + s(C_{COMP1} + C_{COMP2})R_{EA}) \bullet (1 + sC_{COMP2}R_{COMP})} \bullet \frac{R_{FB}}{R_{LED} + R_{FB}} \tag{36}$$

4 Compensation network

By using a mathematical analysis tool (for example MATLAB), it is possible to extract the cutoff frequency and phase margin of the system.

For this application with

- R_{COMP1} = 3300 kΩ
- C_{COMP1} = 22 nF
- C_{COMP2} = 0 F

the frequency response is:

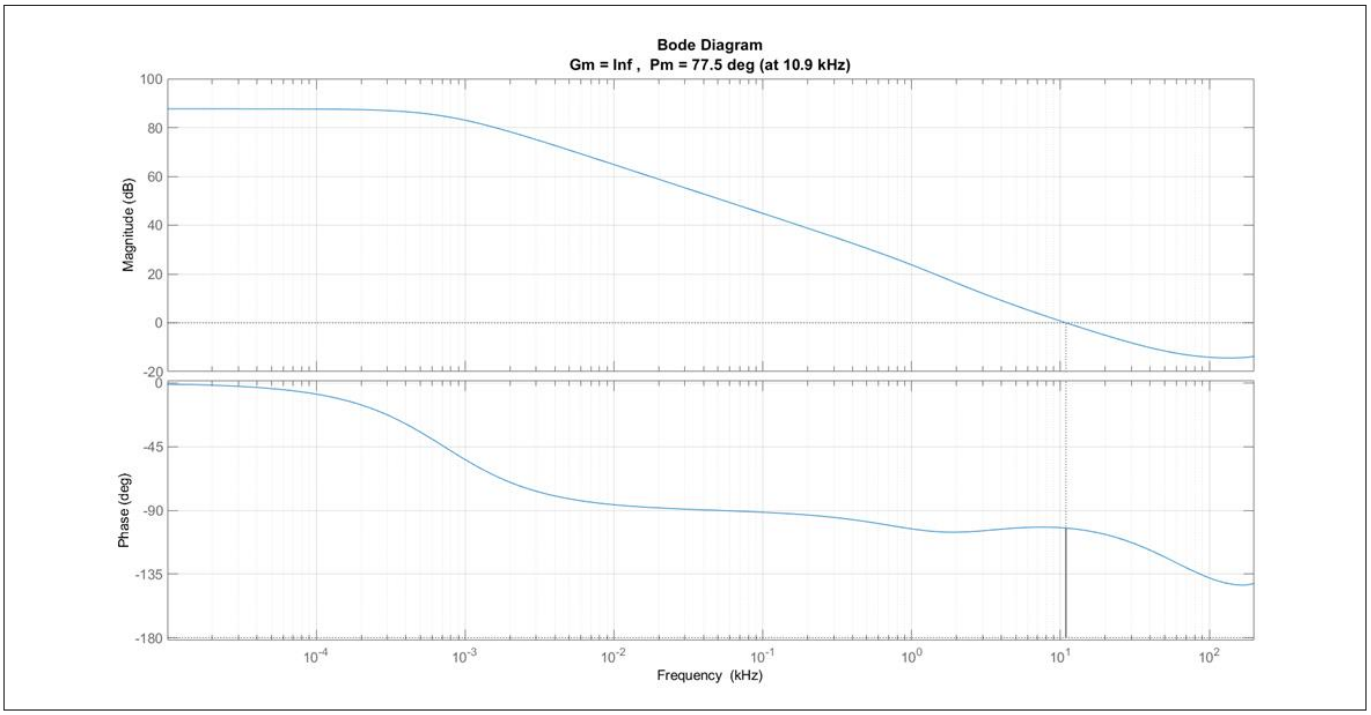

Figure 13 Cutoff frequency and phase margin

Infineon can also provide SPICE models of the device to perform electrical simulation to double check performances.

5 Conclusions

TLD6098-1EP is an automotive qualified multitopology controller for LED application. The device controls the output current by means a current control loop that makes the system easy to compensate. The device also incorporates many features to realize a reliable LED driver for automotive applications.

In this application note a daytime running light (DRL) has been designed. The system proposed has the following benefits:

- The usage of the embedded PWM engine makes the transition from DRL to position light easy to achieve even without the microcontroller support.
- The usage of a PMOS dimming element helps to achieve sharp output current waveform with precise duty cycle control
- The spread spectrum helps to reduce the EMI emission (radiated and conducted)
- A coded fault gives a useful fault indication

Revision history

Document version	Date of release	Description of changes
Rev.1.00	2021-10-19	• Initial application note

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Do you have a question about any aspect of this document?

Email: erratum@infineon.com

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