FAQ Application Note for TLE984xQX

Frequently asked questions and application hints

About this document

Scope and purpose

This Application Note is intended to provide helpful suggestions and hints how to set up and handle specific modules and functionalities which are not subject of the Users Manual or Data Sheet and might be interesting for end users. It is organized in a frequently asked question style and doesn't follow any specific order.

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

Intended audience

This document is intended for Customer and Field Application Engineers to answer frequently asked question for the embedded Power IC, TLE984xQX device family.

Table of Contents

1 GPIO Port Map and Alternate Functions

Topic:

What GPIO is connected to which module of the chip.

Description:

The TLE984xQX has 18 port pins organized in three parallel ports: Port 0 (P0), Port 1 (P1) and Port 2 (P2). Each port pin has a pair of internal pull-up and pull-down devices that can be individually enabled or disabled. Either pull-up or pull-down devices can be enabled at a time, for a single port pin. P0 and P1 are bidirectional and can be used as general purpose input/output (GPIO) or to perform alternate input/output functions for the on-chip peripherals. When configured as an output, the open drain mode can be selected. On Port 2 (P2) analog inputs are shared with general purpose input.

1.1 GPIO Register description

Each port consists of 8-bit control and data registers. The registers are defined in **Table 1**.

Table 1 Port Register

Register Short Name	Register Long Name	Description
Px_DATA	Port x Data Register	x = {0,1,2}
Px_DIR	Port x Direction Register	x = {0,1,2}
Px_OD	Port x Open Drain Control Register	x = {0,1}
Px_PUDSEL	Port x Pull-Up/Pull-Down Select Register	x = {0,1,2}
Px_PUDEN	Port x Pull-Up/Pull-Down Enable Register	x = {0,1,2}
Px_ALTSEL0	Port x Alternate Select Register 0	x = {0,1}
Px_ALTSEL1	Port x Alternate Select Register 1	x = {0,1}

1.2 Alternate Function configuration example

The ports P0 and P1 can be configured to four different output functions. The default configuration is the GPIO function. The three remaining functions are alternate output functions.

The alternate output function selection is splitted in two bitfields (e.g. **P1_ALTSEL0** and **P1_ALTSEL1**). **ALTSEL1** contains the most significant bit. **ALTSEL0** contains the least significant bit. The given example code shows how to configure these bitfields to connect UART2 module (TXD, RXD) with the GPIOs (P1.0, P1.1).

```
/* connect UART2 to GPIO */
/* set P1.0 to UART2_TXD: */
PORT->P1_DIR.bit.PP0 = 1u;  /* PORT P1.0 output configuration */
PORT->P1_ALTSEL0.bit.PP0 = 1u; /* UART2_TXD alternate function 3 */
PORT->P1_ALTSEL1.bit.PP0 = 1u; /* UART2_TXD alternate function 3*/
/* Set P1.1 to UART2_RXD: */
PORT->P1_DIR.bit.PP1 = 0u;  /* PORT P1.1 input configuration */
```

1.3 Port Map implementation of Alternate Functions

Graphical Portmap of Alternate Functions

Each pin is able to handle multiple purposes. **Figure 1** shows the internal signals mapped to GPIOs. The arrow boxes contain the signal names and indicate the data flow direction.

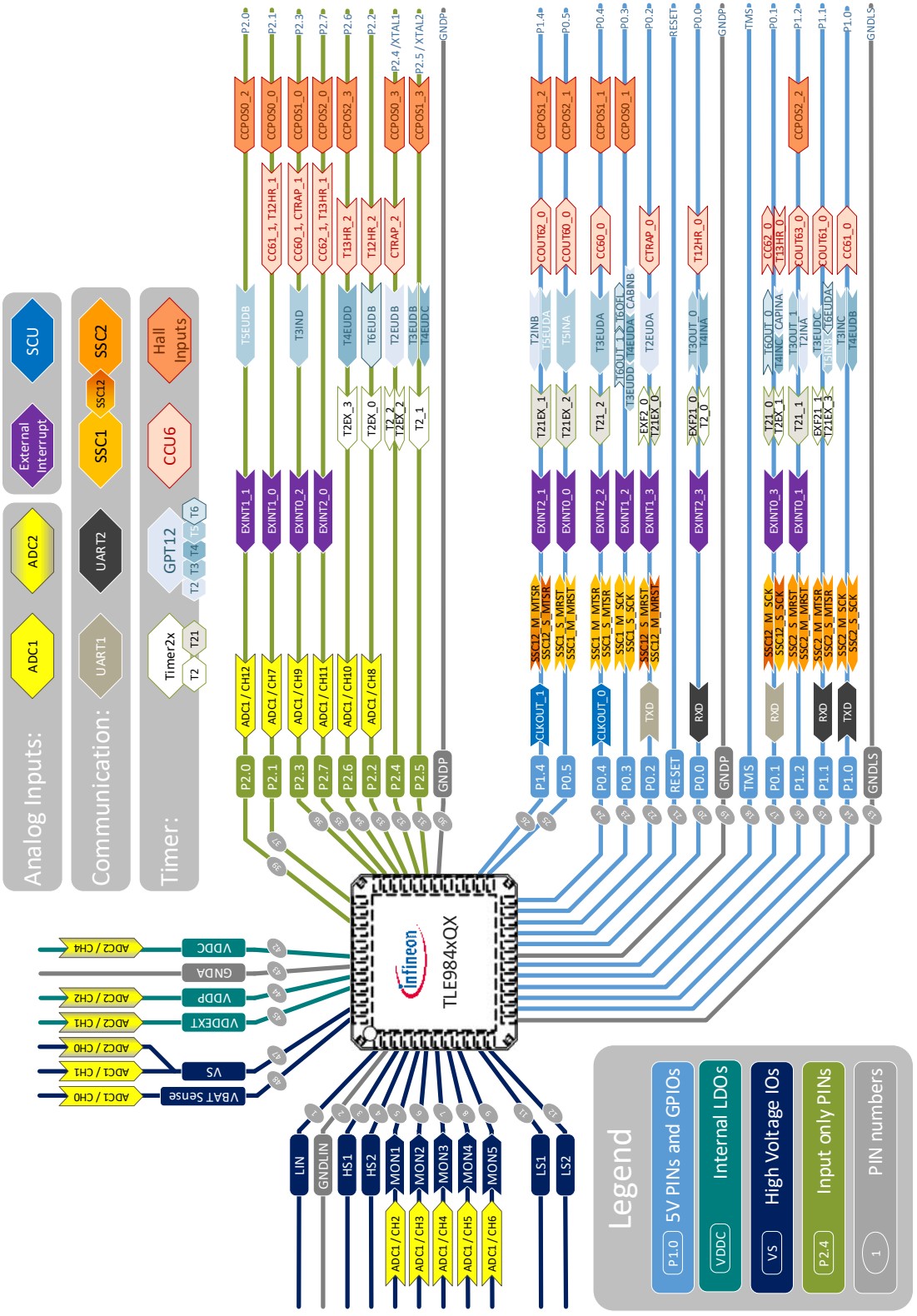

Figure 1 Port Map of Alternate Functions

2 Flash / NVM hints

This chapter lists Flash/NVM related topics.

2.1 Systick during NVM-write cycle

During NVM-write cycle, the Systick is not running. It is not necessary to explicitly disable it.

2.2 Watchdog handling during write cycle

It is recommended to trigger a short open window (SOW) before writing to the NVM.

2.3 Address of Data Flash (emulated EEPROM)

Table 2 shows the variant dependent Data Flash start adress offsets.

Table 2 Data Flash Start Adress

Product name	Flash size [kB]	Data Flash Start Address Offset
TLE9842QX	36	0x8000
TLE9842-2QX	40	0x9000
TLE9843QX TLE9845QX	48	0xB000
TLE9843-2QX	52	0xC000
TLE9844QX TLE9844-2QX	64	0xF000

2.4 Erased NVM

When the algorithm reads from an erased or empty NVM page, there are specified values to expect.
The values differ between Code and Data Flash.

Table 3 Erased NVM values

NVM	Value
Data Flash	0x00
Code Flash	0xFF

3 NMI / Interrupt hint

NMIs have to be enabled seperately via NMICON
The default state is ‘Off’

4 Hard Fault hint

Writing to a protected register will cause a Hard Fault.
Hard Faults will cause a cold reset.

5 High Side Switches HS1/HS2 hint

TLE984x family include devices with one and two High Side Switches. The software handling has to ensure, that the second High Side Switch stays disabled for single High Side Switch devices.

6 Debug Entry Behavior

When the Chip enters debug mode, the core will not be halted immediately. The user code will run for 85ms before the debug interface stops the core. If user code contains data-flash access during this timeframe, the debug connection cannot be established.

7 Layout and Design hints

This section gives Layout hints based on previous design experience.

7.1 VDDC Regulator Routing

VDDC is the core voltage regulator. If the voltage is influenced, for example from GND spikes, a Hard Fault may appear. It is mandatory to pay special attention to the layout of the VDDC stabilisation capacitors.

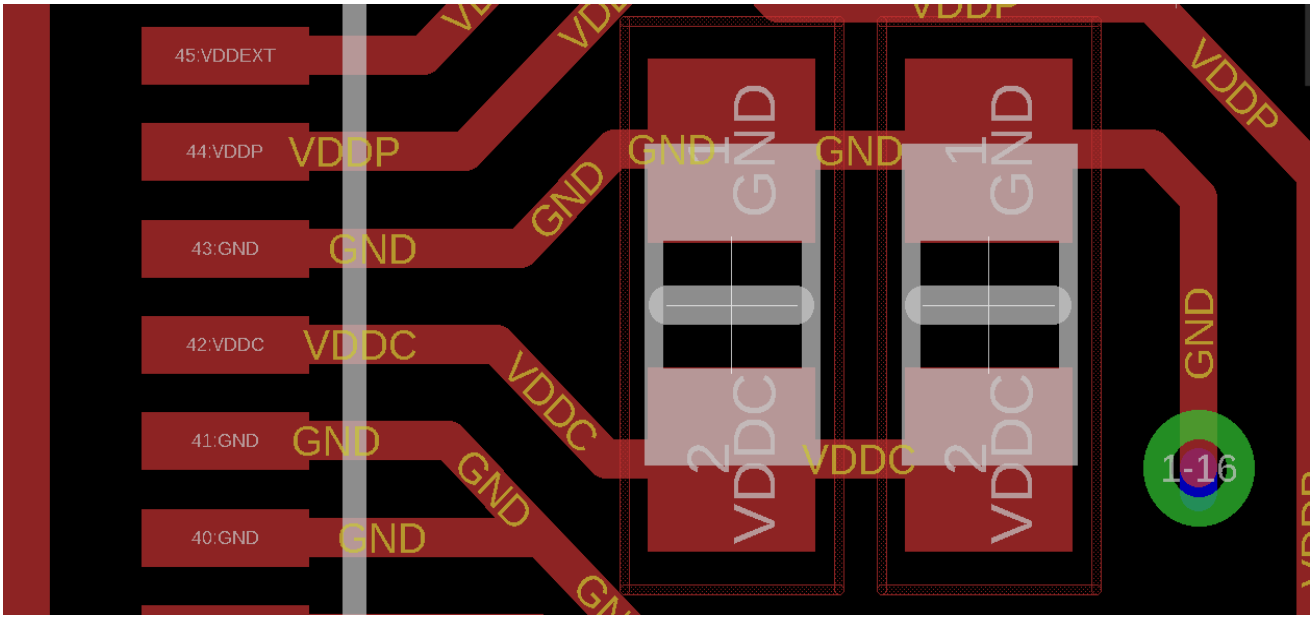

Figure 2 Layout proposal: VDDC Capacitor

Figure 2 shows a PCB layout proposal for VDDC capacitors. It is recommended to place the capacitors as close as possible to the PINs 42 and 43.

The GND PIN 43 shall not be connected to the exposed Pad, to avoid unintended GND coupling.
In this proposal, the GND plane connection is not interrupting the current loop between the VDDC regulator and its stability capacitors. The GND connection is achieved with a seperate wire and a through hole connection to the GND plane. This layout avoids high frequency pulses coupling from the core clock generation to the GND plane.

7.2 EMC improvement of Low Side Switch

It is recommended to place a 2.2nF capacitor at the Low Side Switches (LS1/LS2).

7.3 GPIO Input Filters for Hall Sensors

In case of long GPIO wiring for external sensors, it is recommended to place a filter to improve HF immunity.

Figure 3 shows a simplified filter circuitry. For open Drain Sensor outputs, it is recommended to place an external pull-up resistor instead of using the internal pull-up sources.

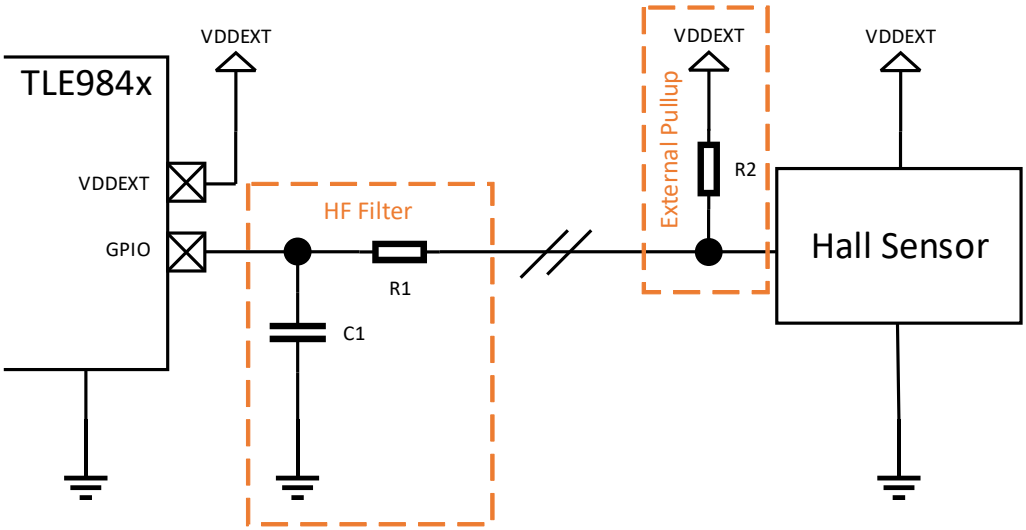

Figure 3 hall sensor filter

The additional RC-filter protects the GPIO from damage based on HF coupling. Example filter values are listed in **Table 4**.

Table 4 Filter Values

Part	Value
R1	1kR
C1	180pF

8 Revision History

Revision	Date	Changes
1.0	2016-09-29	Release state
1.1	2018-08-30	New Revision rev1.1 Changed Document Title Updated: **Figure 1** Added Topics: **Flash / NVM hints** **NMI / Interrupt hint** **Hard Fault hint** **High Side Switches HS1/HS2 hint** **Debug Entry Behavior** **Layout and Design hints**

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