TLE984xQX

Application Hints

About this document

Scope and purpose

Note: *The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

This Application Note is intended to provide helpful suggestions and hints how to set up and handle specific modules and functionalities which are not subject of the Users Manual or Data Sheet and might be interesting for end users. It is organized in a frequently asked question style and doesn't follow any specific order.

Intended audience

This template is intended for Customer and FAE to document frequently asked question and answers for the embedded Power IC, TLE984xQX device family.

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1 Introduction

This Application Note lists topics which emerged from frequently asked questions of users or from changed user requirements. Each topic is organized in three sections:

- **Topic:**
  - Short description of the issue.
- **Description:**
  - More details about the topic
- **Implementation hint (optional):**
  - Instruction how to handle this topic

2 Collection of Topics

2.1 GPIO Port Map and Alternate Functions

Topic:

What GPIO is connected to which module of the chip.

Description:

The TLE984xQX has 18 port pins organized in three parallel ports: Port 0 (P0), Port 1 (P1) and Port 2 (P2). Each port pin has a pair of internal pull-up and pull-down devices that can be individually enabled or disabled. Either pull-up or pull-down devices can be enabled at a time, for a single port pin. P0 and P1 are bidirectional and can be used as general purpose input/output (GPIO) or to perform alternate input/output functions for the on-chip peripherals. When configured as an output, the open drain mode can be selected. On Port 2 (P2) analog inputs are shared with general purpose input.

2.1.1 GPIO Register description

Each port consists of 8-bit control and data registers. The registers are defined in Table 1.

Table 1 Port Register

Register Short Name	Register Long Name	Description
Px_DATA	Port x Data Register	x = {0,1,2}
Px_DIR	Port x Direction Register	x = {0,1,2}
Px_OD	Port x Open Drain Control Register	x = {0,1,2}
Px_PUDSEL	Port x Pull-Up/Pull-Down Select Register	x = {0,1,2}
Px_PUDEN	Port x Pull-Up/Pull-Down Enable Register	x = {0,1,2}
Px_ALTSEL0	Port x Alternate Select Register 0	x = {0,1,2}
Px_ALTSEL1	Port x Alternate Select Register 1	x = {0,1,2}

2.1.2 Alternate Function configuration example

The ports P0 and P1 can be configured to four different output functions. The default configuration is the GPIO function. The three remaining functions are alternate output functions.

The alternate output function selection is splitted in two bitfields (e.g. **P1_ALTSEL0** and **P1_ALTSEL1**). **ALTSEL1** contains the most significant bit. **ALTSEL0** contains the least significant bit. The given example code shows how to configure these bitfields to connect UART2 module (TXD, RXD) with the GPIOs (P1.0, P1.1).

```
/* connect UART2 to GPIO */
/* set P1.0 to UART2_TXD: */
PORT->P1_DIR.bit.PP0 = 1u;  /* PORT P1.0 output configuration */
PORT->P1_ALTSEL0.bit.PP0 = 1u; /* UART2_TXD alternate function 3 */
PORT->P1_ALTSEL1.bit.PP0 = 1u; /* UART2_TXD alternate function 3*/
/* Set P1.1 to UART2_RXD: */
PORT->P1_DIR.bit.PP1 = 0u;  /* PORT P1.1 input configuration */
```

2.1.3 Port Map implementation of Alternate Functions

Graphical Portmap of Alternate Functions

Each pin is able to handle multiple purposes. Figure 1 shows the internal signals mapped to GPIOs. The arrow boxes contain the signal names and indicate the data flow direction.

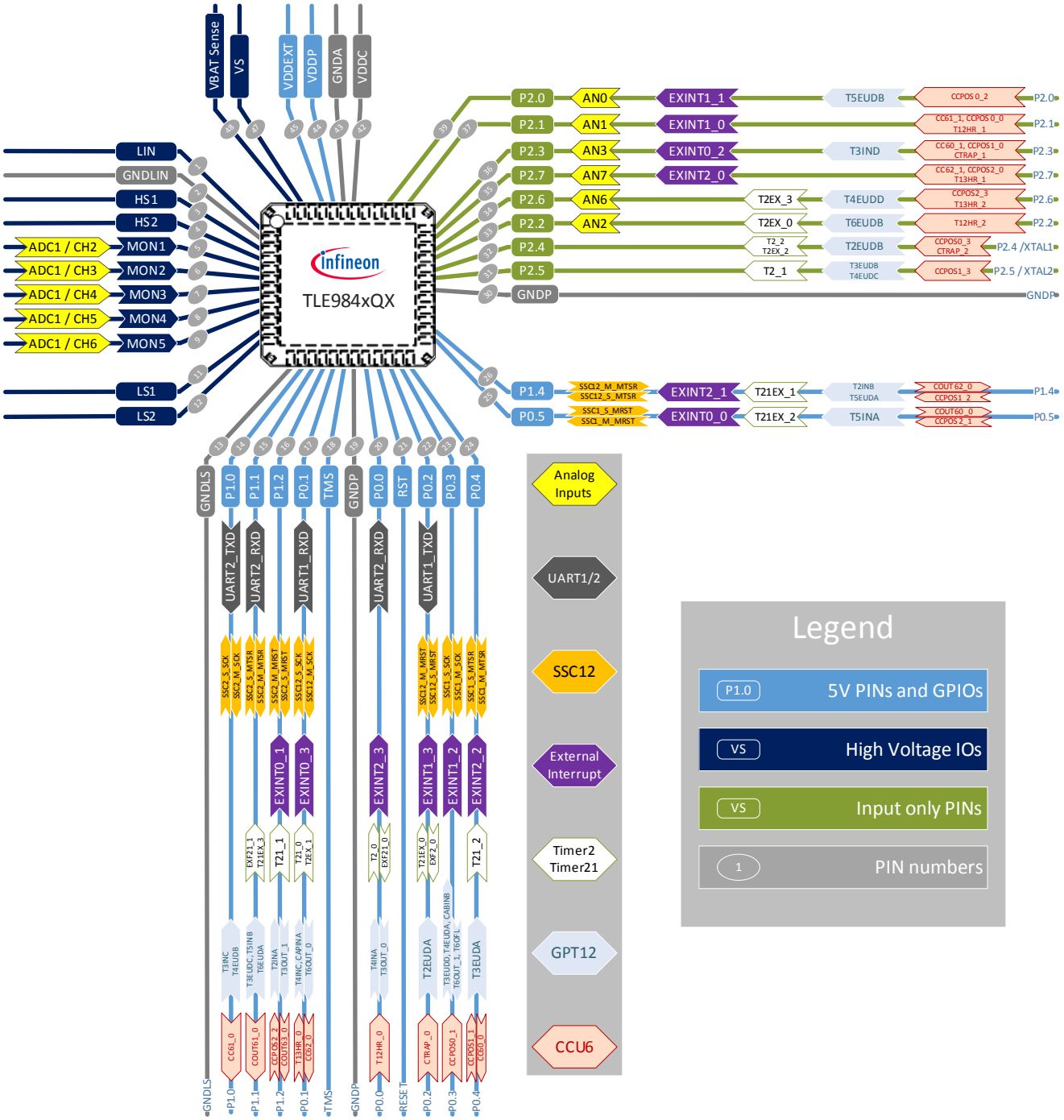

Figure 1 Port Map of Alternate Functions

3 Revision History

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