TLE9012DQU, TLE9015DQU

Z8F80064984

Preface

Scope and purpose

This document describes the usage of the multi-cell monitoring and balancing IC TLE9012DQU and the transceiver TLE9015DQU designed for Li-ion battery packs used in hybrid electric vehicles (HEV), plug-in hybrid electric vehicles (PHEV), battery electric vehicles (BEV) as well as in stationary Lithium-Ion batteries.

Please also refer to the corresponding datasheets.

Intended audience

This document is intended for engineers who develop applications.

Table of contents

1 Demo kit

1.1 Getting started

1.1.1 Hardware elements of the demo kit

Note: All different versions of the evaluation boards are compatible to each other and can be used in the same daisy chain.

The following hardware is necessary to start with the TLE9012DQU demo kit:

- TLE9012DQU demo board
- At least 1x iso UART cable
- TLE9015DQU transceiver board
- AURIX^{TM} TC265 TFT application kit
- 12 V power supply
- Micro USB cable
- Power supply for the resistor ladder (5 V - 60 V)
- Optional: 12 Li-Ion cells (instead of resistor ladder)
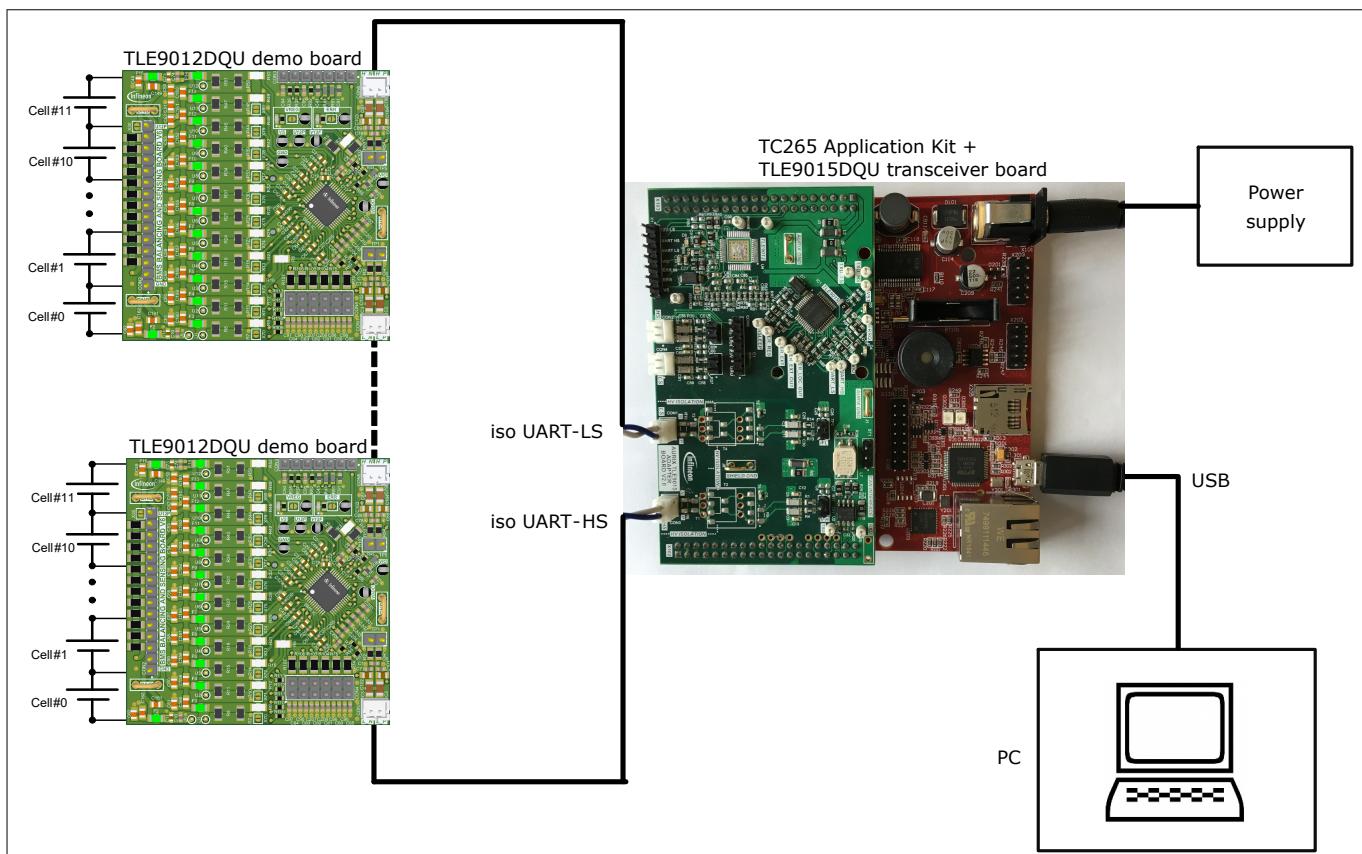
Figure 1   **Demo kit BMS**

1.1.2 Hardware connection

The hardware is connected as follows:

- The TLE9015DQU transceiver board is plugged onto the AURIX^{TM} board (orientation as in figure Demo kit BMS).
- A resistor ladder is included on the sensing IC demo board and already connected through a solder bridge.
- The sensing IC demo board must be supplied with a voltage between 5 V - 60 V.

1 Demo kit

- The AURIX^TM board must be supplied with a 12 V power supply and connected to a PC via a USB cable.
- The iso UART cable (blue/white) cable connects the transceiver board with the sensing board.
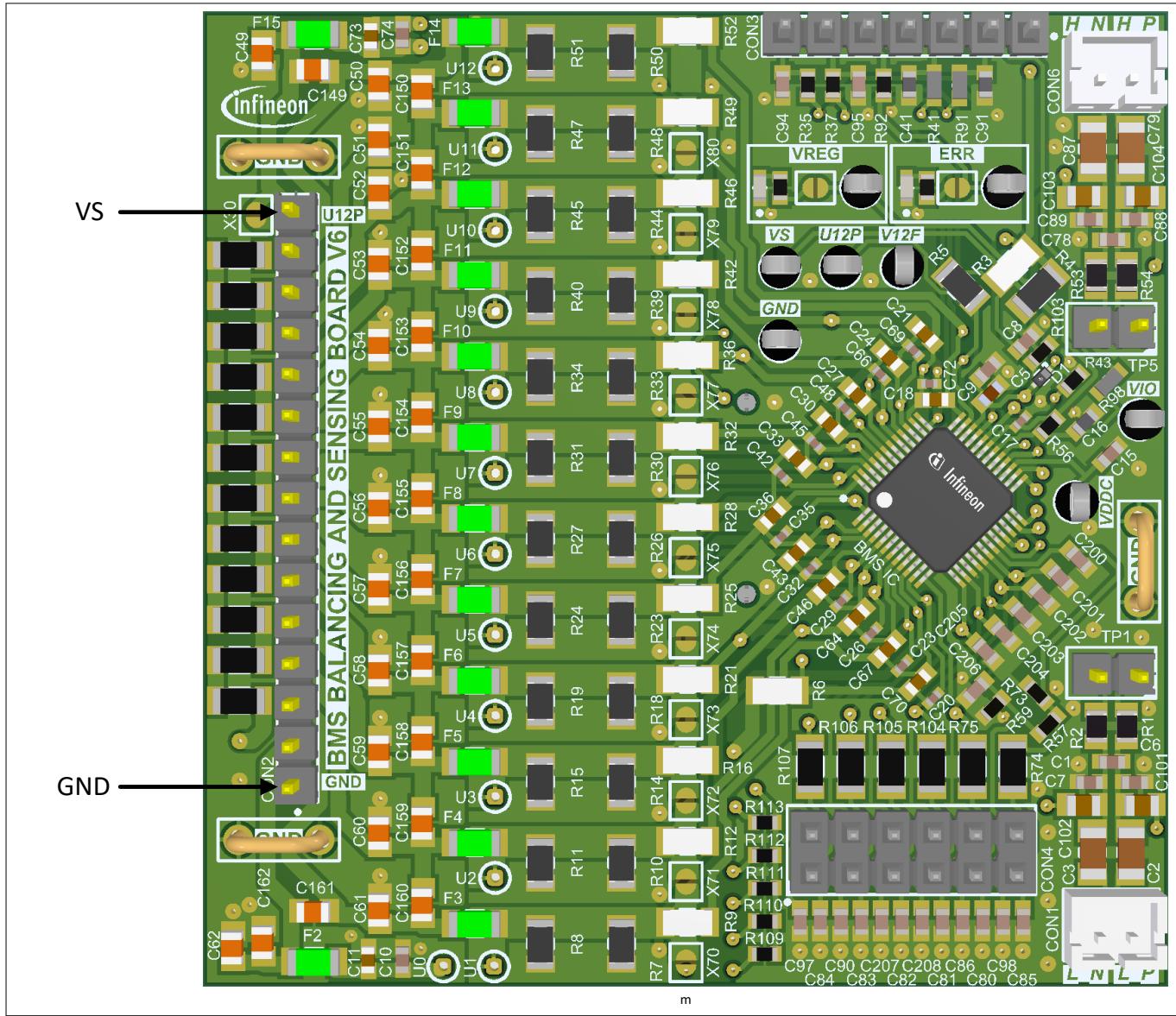
Figure 2   Sensing IC demo board

Note: The sensing IC demo board can be connected either to cells (if the board should be connected to a battery pack, the solder bridges need to be removed see figure Sensing IC demo board solder bridge*) or to a power supply using the on-board resistor ladder. If the resistor ladder is used, an open load error is wrongly detected and the corresponding bit in the general diagnostics register (GEN_DIAG) is set. This is because the internal resistance of Li-Ion cells is much smaller than the resistance of the resistor ladder. The open load error can be deactivated by setting the bitfields OL_OV_THR.OL_THR_MAX and OL_UV_THR.OL_THR_MIN to 00_H. All other functions such as cell voltage measurement, temperature etc. are possible without limitation.*
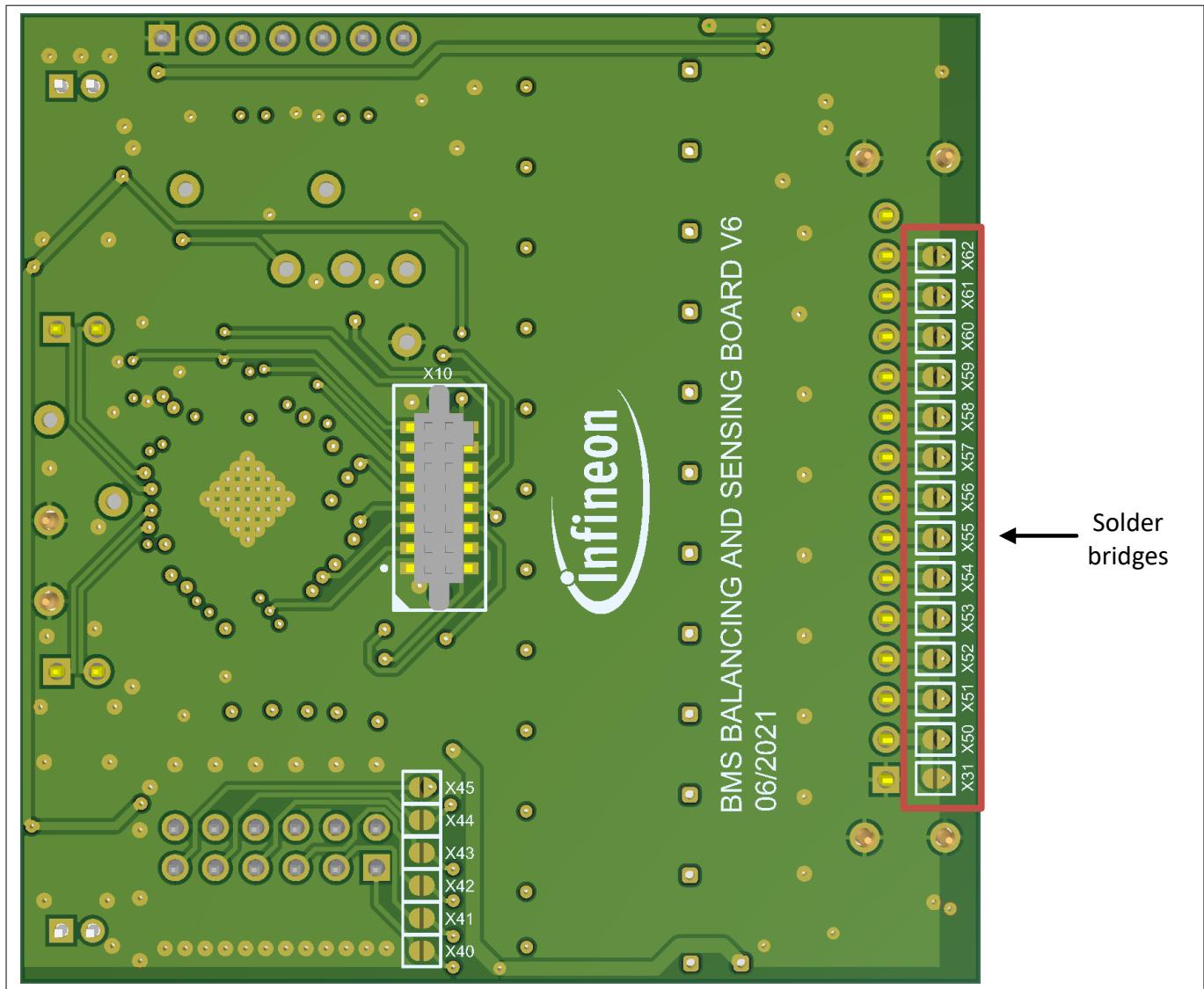
Figure 3   Sensing IC demo board solder bridges

Note: The transceiver IC demo board can be supplemented with additional transformers. In order to be able to use the demo board with transformers, the 0 Ω resistors R99, R100, R101 and R102 must be removed and the transformers have to be place at Tx depending on the footprint (see figure below).
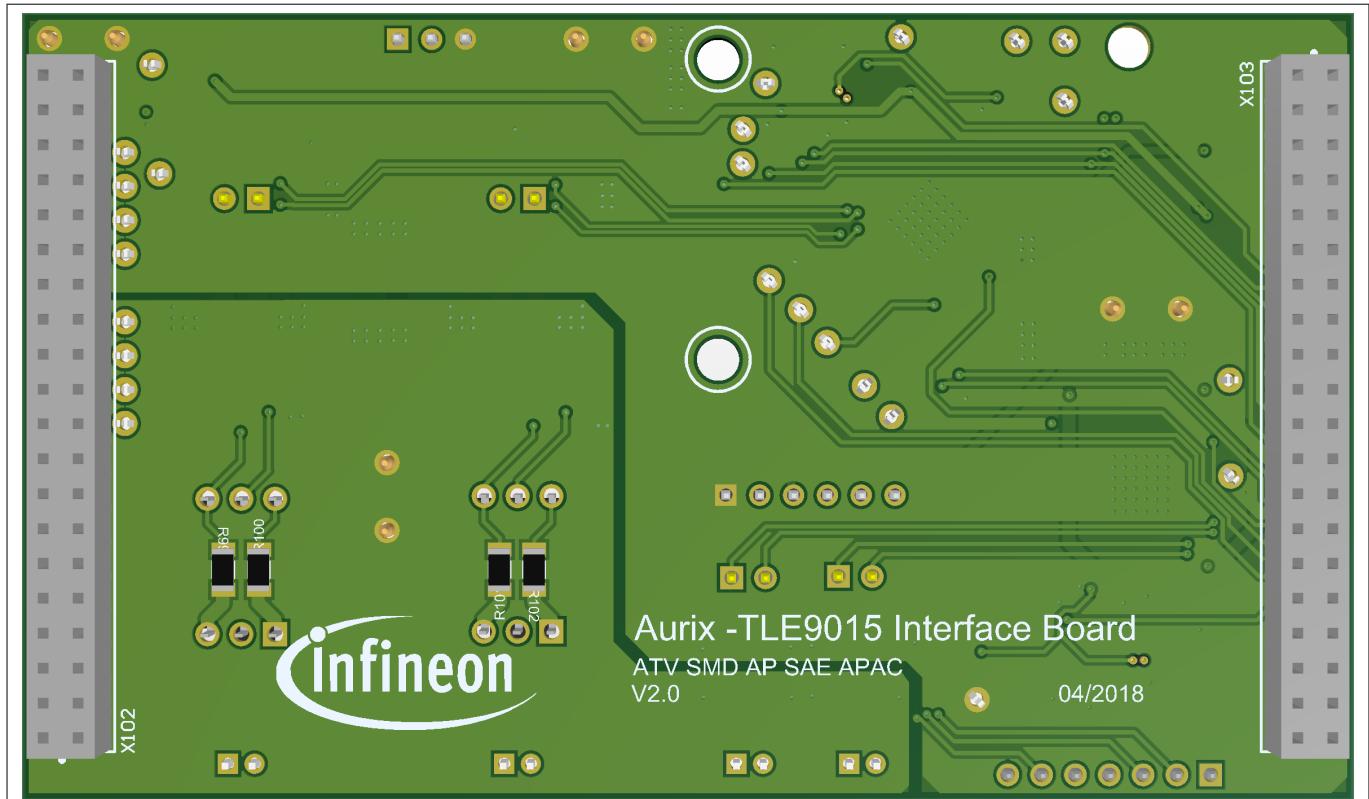
Figure 4   **Transceiver IC demo board bottom**

1.1.3   13-wire setup

The BMS sensing board can be used in a 13-wire or 15-wire configuration (see 13-wire setup). For a 13-wire setup, the solder bridges X30 and X31 must be soldered.
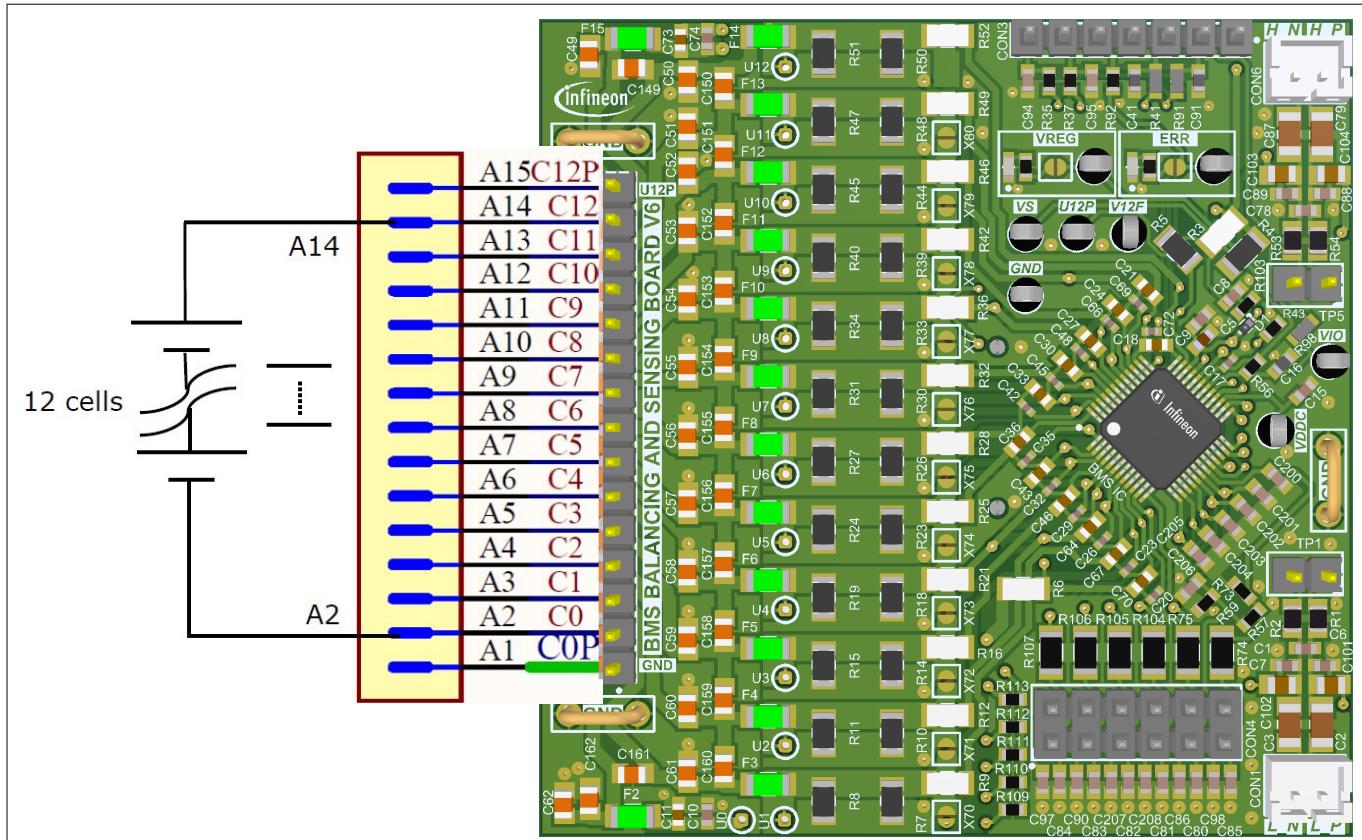
Figure 5   **13-wire setup**

1.1.4   Flashing the AURIX hardware kit

The following steps are required to setup the framework for the demo kit.

1.1.4.1   DAS tool

The DAS tool is a USB driver software provided by Infineon. It is required to connect the AURIX^{TM} hardware kit to the PC environment. The latest version can be found here: Link to

DAS tool

To start the installation, administrator privileges are requirement and the terms of use need to be accepted. After the successful installation of DAS, the PC should be able to detect the AURIX^{TM} kit under the COM port settings in the device manager.

1.1.4.2   MemTool

The MemTool is a software from Infineon for on-chip flash programming. The latest version can be found here: Link to

MemTool

Click "Accept & Open" to download the software and run the installation afterwards.

1.1.4.3   Aurix flashing

The AURIX^{TM} kit needs to be connected to a 12 V power supply. A USB cable connects the board to the PC.

To PC USB
connection

12 V Power
Supply
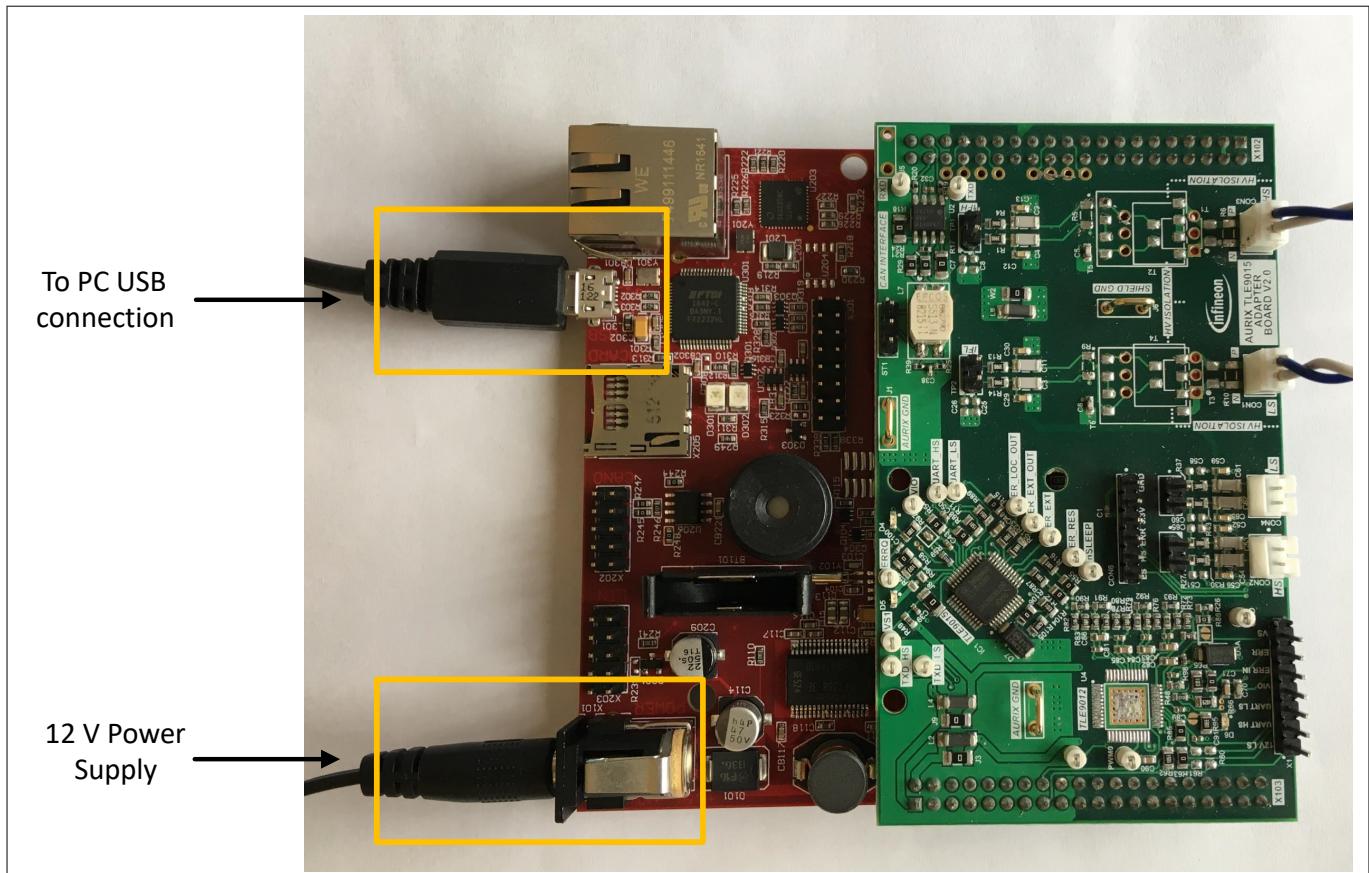
Figure 6 **AURIX^TM power supply and USB connection**

Press the "START" button to initialize. When LED D10 lights up, the AURIX^TM has started up successfully.
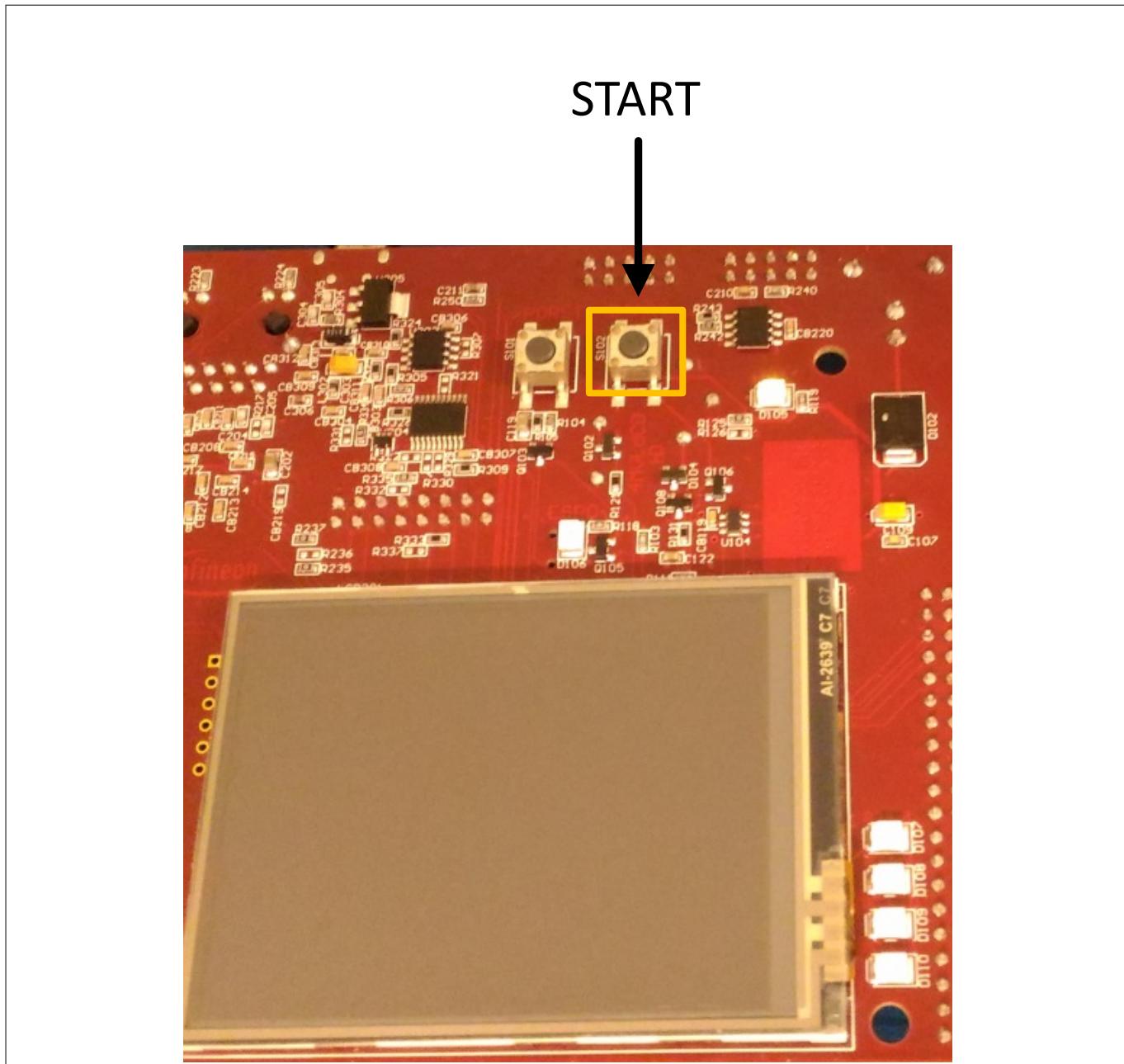
Figure 7   **AURIX initialize**

Open the device manager and expand "Universal Serial Bus controllers". Right click on "Infineon DAS JDS COM" to open the properties. Select the tab "Advanced", check "Load VCP" and click "OK".
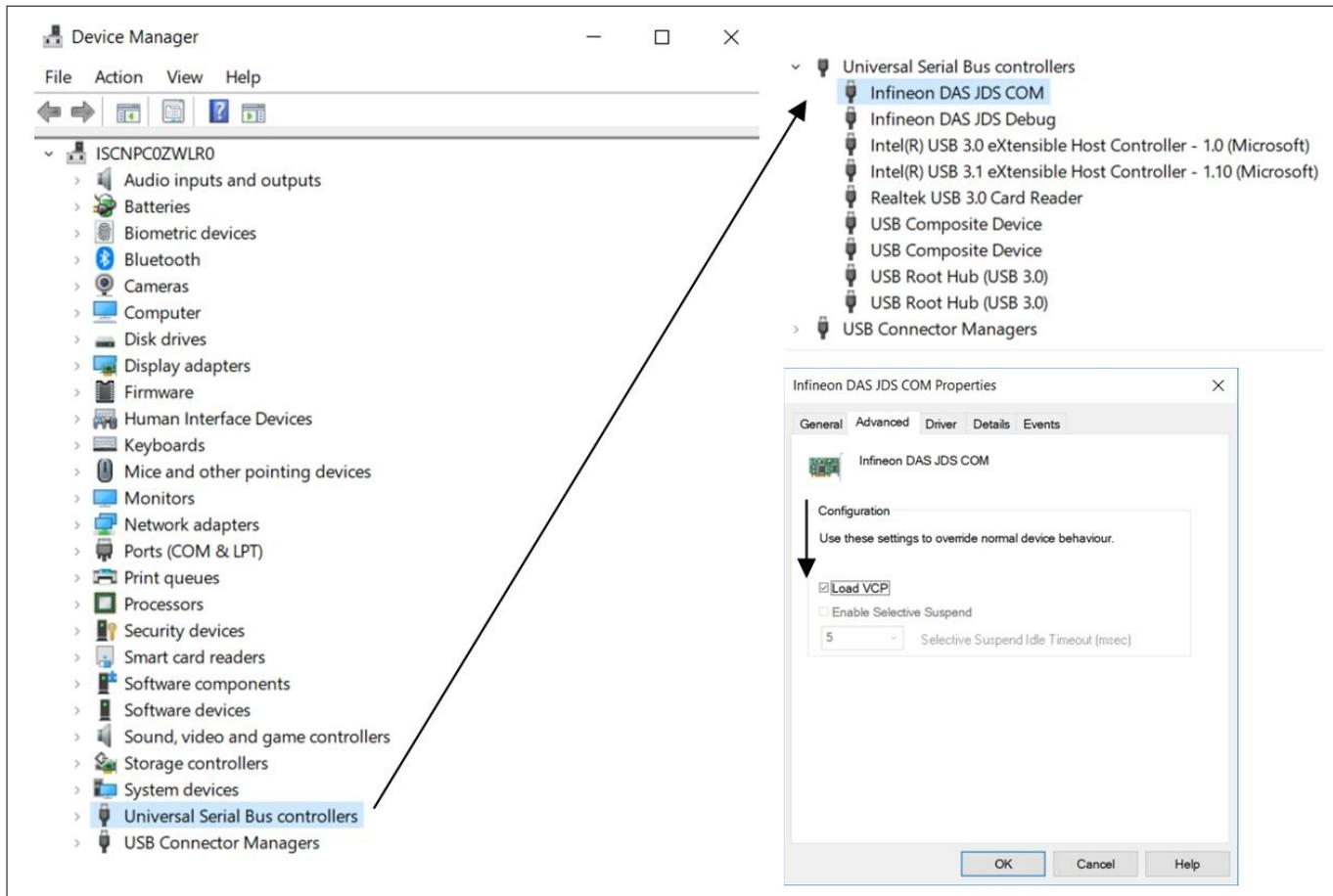
Figure 8   Configuration of the COM port

Disconnect the USB cable and power supply and reconnect. After pressing "START", check the COM port number in the device manager by expanding "Ports (COM & LPT)". A port number is assigned to the AURIX^{TM} kit.
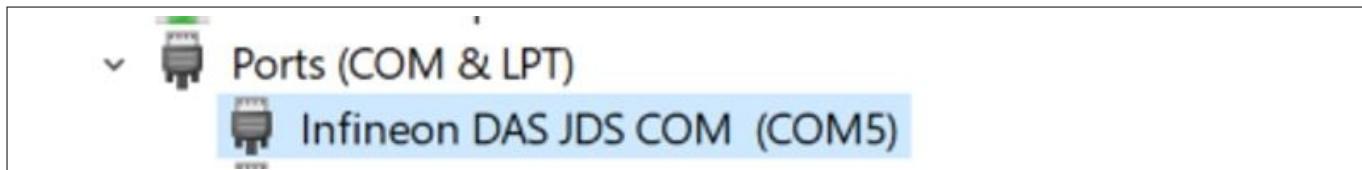
Figure 9   Infineon DAS JDS COM port

Open the MemTool and go to "Target" → "Change...".
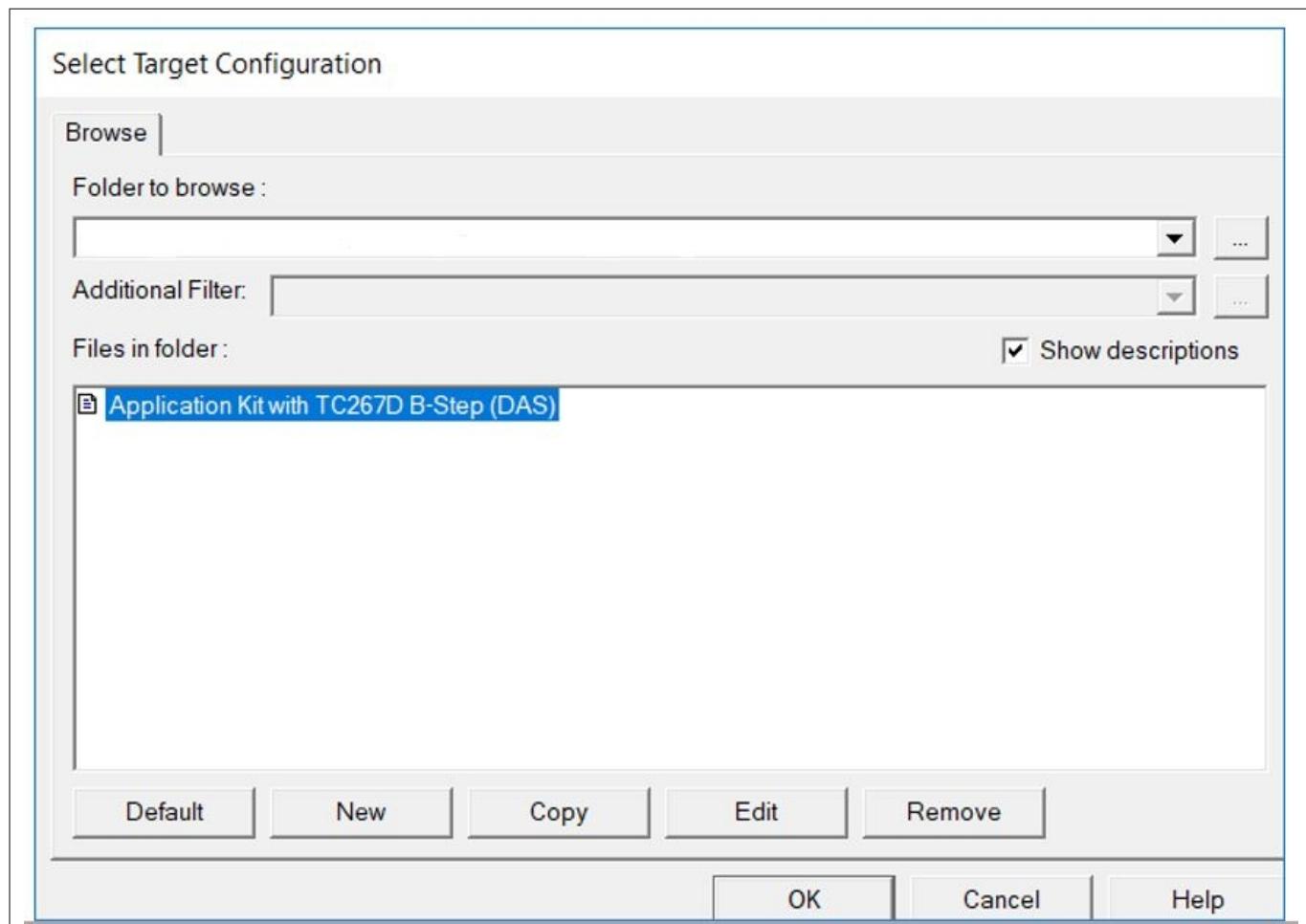
Figure 10   Select target configuration

Click on "New" and select "Use a default target configuration". Expand "TriCore Aurix" → "Application Kits (DAS)". Select "Application Kit with TC267D B-Step(DAS)" as shown in figure Create or use default.
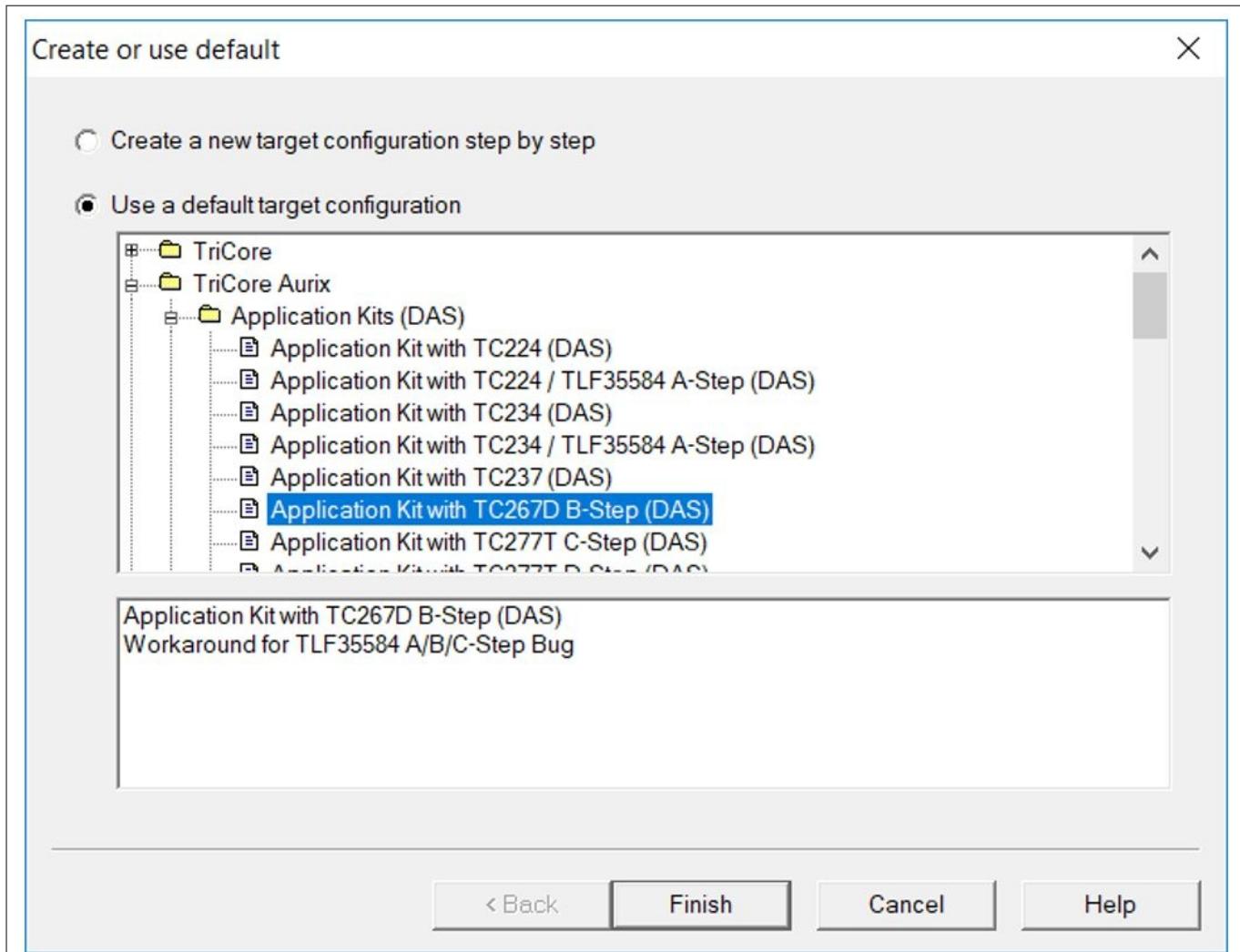
Figure 11   Create or use default

Click "Finish" and save the target configuration file, then select "OK". After selecting the target configuration, click on "Connect". If the connection is successful, you will be able to see this message "ready for MemTool Command". Click on "Open File …".
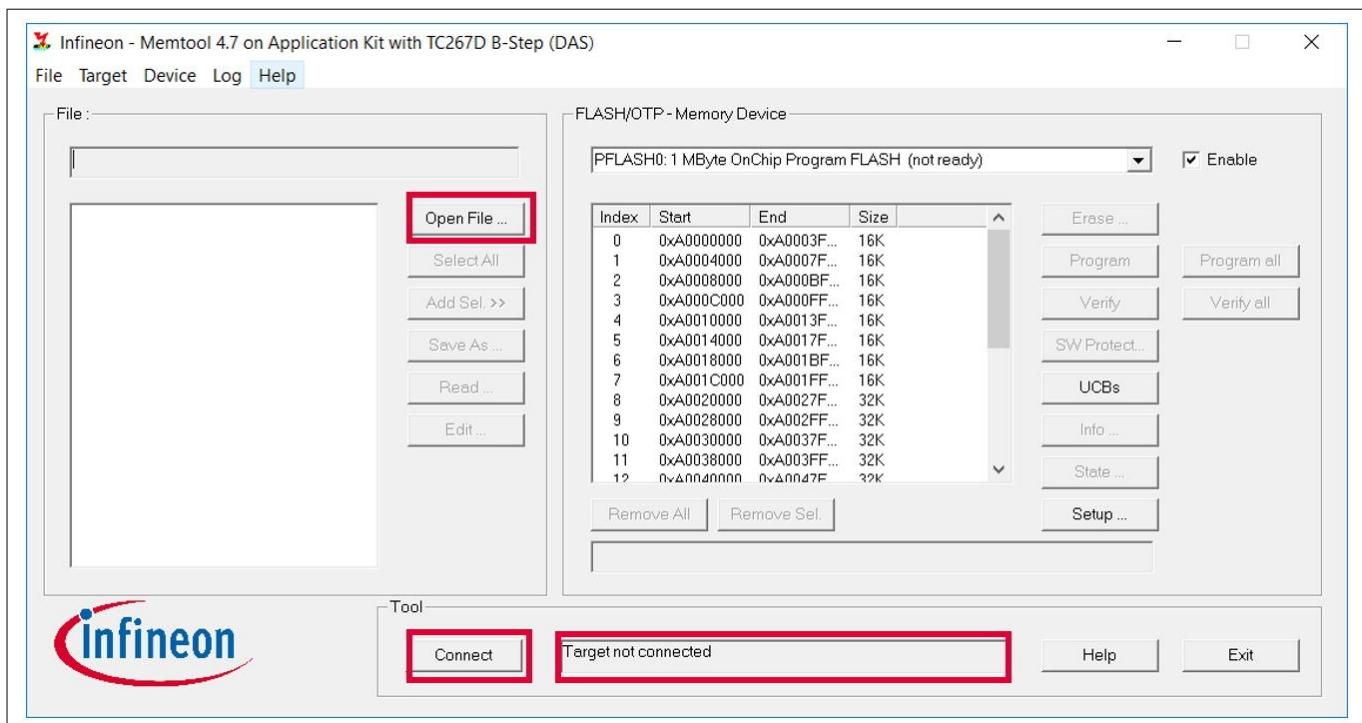
Figure 12   MemTool

Select the *.hex file "Infineon_TLE9015DQU_TLE9012DQU_TC265.hex" stored on MyICP. Click "Select All" and afterwards "Add Sel". To flash the AURIX^{TM}, select "Program all". Once successful, you can see the message shown in figure Execute MemTool command.
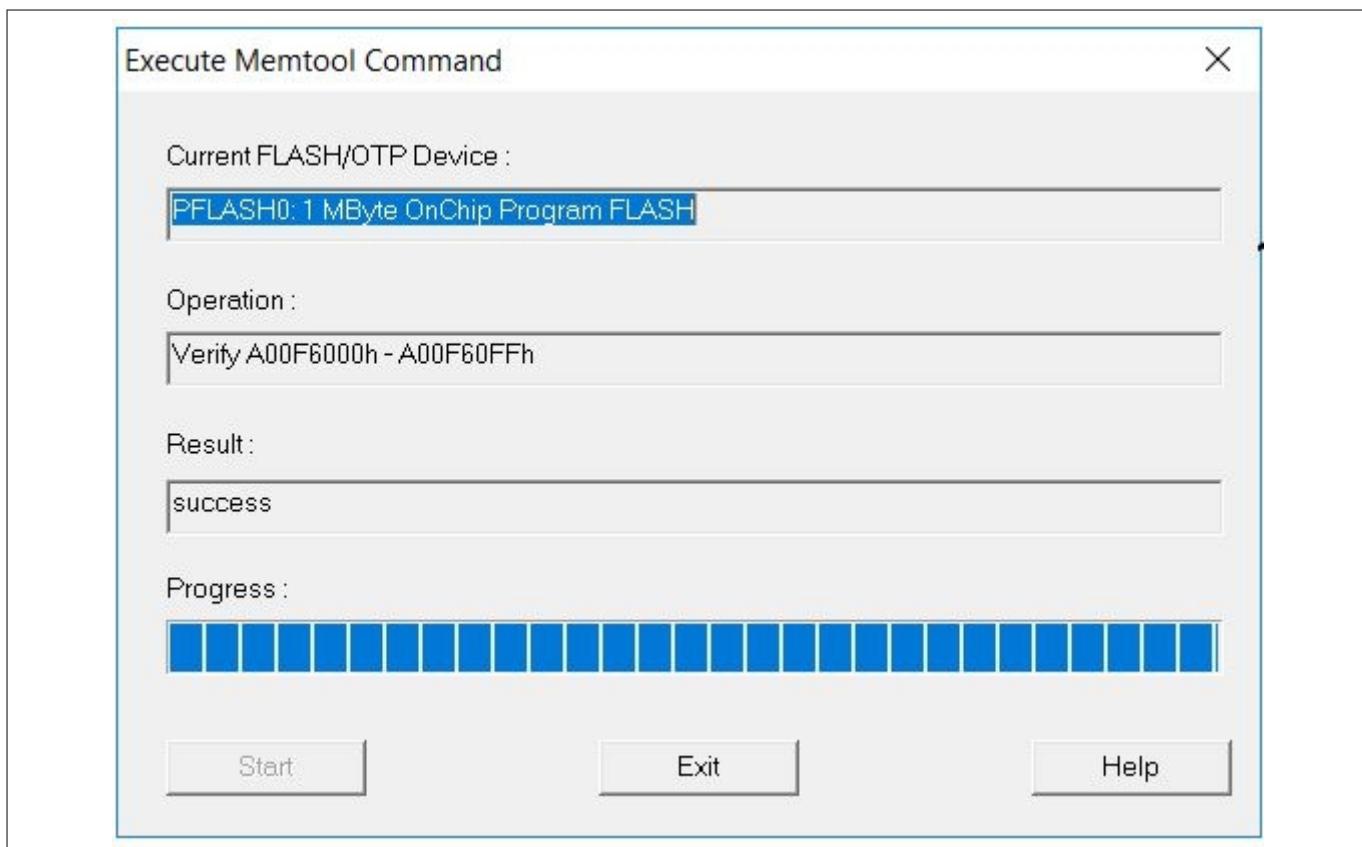
Figure 13   Execute MemTool command

Note: For further details or support on how to flash the AURIX TM TFT kit, please refer to https://www.infineon.com/aurix

1.1.4.4 Terminal

A terminal program (e.g. TeraTerm) can be used to communicate with the BMS IC. The configuration of the serial port is shown in figure Serial port setup.
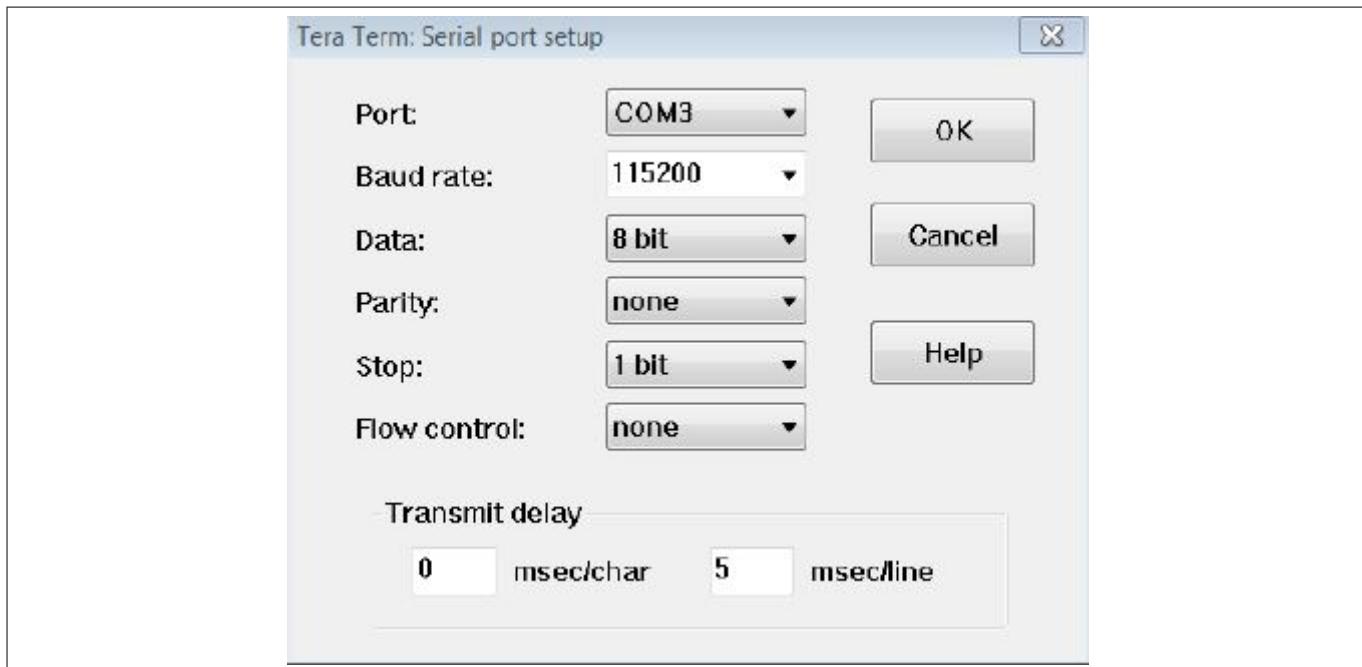
Figure 14 **Serial port setup**

After successful configuration, a user manual is available by sending "?".

Figure 15   **TeraTerm user manual**

There is the possibility to load a script into the terminal, which will perform several lines of commands. Drag & drop can be used to load the script in the terminal. A script, which reads out all the cell voltage is provided on MyICP "TC265TFT_BMS_init_CVM_1_Slave_Terminal.txt".

Figure 16   **Terminal script to read out all PCVMs**

The result registers can be copied into an Excel sheet to calculate the cell voltages (in mV) out of the hex register values. Therefore, the lines shown in figure Terminal script to read out all PCVMs need to be marked and copied by selecting "Edit" → "Copy table". Based on the "TC265TFT_BMS_init_PCVM_1_Slave_Terminal.txt" file is an Excel sheet at the Infineon BMS MyICP available to convert the received register results to cell voltages in mV. The Excel sheet is shown in figure TLE9012DQU_CVM.xlsx Excel sheet to calculate the cell voltages in mV. The copied data has to be pasted at the indicated cell H3.

Figure 17   **TLE9012DQU_CVM.xlsx Excel sheet to calculate the cell voltages in mV**

2 Hardware guideline

2.1 Application schematic of one Cell Supervision Circuit (CSC)
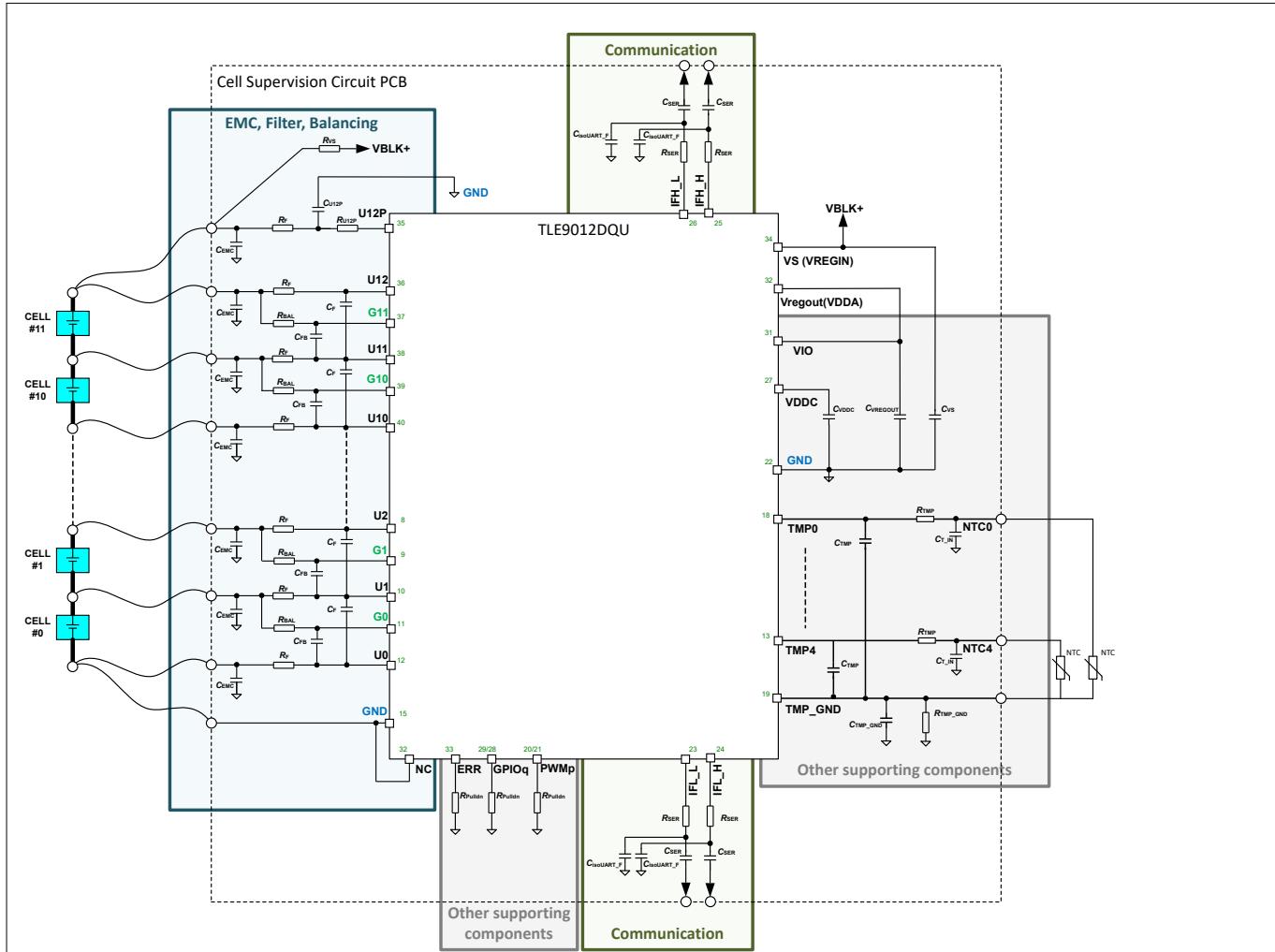
Figure 18 Schematic of one CSC

2.1.1 BOM - EMC, filter and balancing circuit

Table 1 BOM - EMC, filter and balancing circuit

Name	Symbol	Min.	Typ.	Max.	Unit	Status as is on evaluation board			Possible optimization	Layout hints and general comments
						Package	Characteristics	Value		

(table continues...)

2 Hardware guideline

Table 1 (continued) BOM - EMC, filter and balancing circuit

		Min	Typ	Max	Unit	Package	Rating	Value	Comment	Note
Filter capacitor Un+1/Un	C_F	50	330	1000	nF	SM0603	16 V, open mode principal preferred	330 nF	Other voltage rating e.g. 10 V also possible and can be reduced to e.g. 0402.	Should be placed as close as possible to the Un pins, especially important for C_F between U11 and U12 (see Layout guideline)
Filter capacitor Gn/Un	C_{FB}	11	100	500	nF	SM0402	50 V, open mode principal preferred	100 nF	Other voltage rating e.g. 10 V also possible.	Please adjust this capacitor value accordingly if you want to change the balancing resistor value to keep τ constant.
Filter resistor Un	R_F	3	10	62	Ω	SM1206	Anti surge	10 Ω	Can be reduced to e.g. 0805. Please take maximum peak currents during hot plug events into account when choosing resistor package and type.	ADC input impedance during measurement conversion is typically 200 kΩ. This value can be used to calculate the voltage drop over that resistor during measurement conversion.
Filter resistor U12P	R_{U12P}	4.5	5.1	5.6	Ω	SM1206	Anti surge	5.1 Ω	Can be reduced to e.g. 0805. Please take maximum peak currents during hot plug event in account when choosing resistor package and type.	–
Buffer capacitor U12P	C_{U12P}	50	100	130	nF	SM0603	100 V, open mode principal preferred	100 nF	–	–

(table continues…)

Table 1 **(continued) BOM - EMC, filter and balancing circuit**

EMC network capacitor	C_{EMC}	0	1	5	nF	SM0805	100 V, open mode principal preferred	1 nF	Can be reduced to e.g. 0603	This component is optional but it can improve the EMC robustness. It depends on the system setup including PCB layout, BCI injection point etc. whether the component is needed. The component should be placed close to the connector of the sensing wire.
Balancing resistor	R_{BAL}	18	41	200	Ω	SM1206	–	41 Ω	Resistor value in parallel setup is made for max. ~100 mA balancing current. Can be optimized based on balancing current requirement.	–
Filter resistor VS	R_{VS}	4.5	33	100	Ω	SM1206	Anti surge	5.1 Ω	Can be reduced to e.g. 0805. Please take maximum peak currents during hot plug event into account when choosing resistor package and type.	–

2.1.2 BOM - communication circuit between Cell Supervision Circuits

Table 2 **BOM - communication circuit between Cell Supervision Circuits**

						Status as is on evaluation board			Possible optimization	Layout hints and general comments
Name	Symbol	Min.	Typ.	Max.	Unit	Package	Characteristics	Value		

(table continues…)

Table 2 **(continued) BOM - communication circuit between Cell Supervision Circuits**

						Package	Characteristics	Value	Possible optimization	Layout hints and general comments
HF noise bypass capacitor isoUART	$C_{isoUART\_F}$	0	220	286	pF	SM0603	50 V	220 pF	Can be reduced to e.g. 10 V and different package e.g. 0402.	Optional, especially in combination with a transformer. The $C_{isoUART\_F}$ should be placed close to C_{EMC} (if used) and the common GND path should be as short as possible.
isoUART series resistor	R_{SER}	37.05	39	40.95	Ω	SM0805	–	39 Ω	–	Should be placed close to the IC.
isoUART series capacitor	C_{SER}	0.95	1	1.05	nF	SM1206	630 V	1 nF	Can be reduced to e.g. 0805. It depends on the battery system requirement whether a ≥ 500 V voltage rating is needed. With no additional battery system requirement 100 V is sufficient.	Symmetric routing of communication lines improves the EMC robustness. For an improved EMC robustness we propose C0G capacitors with ±5% tolerance.

2.1.3 BOM - other supporting components for Cell Supervision Circuits

Table 3 **BOM - other supporting components for Cell Supervision Circuit**

						Status as is on evaluation board			Possible optimization	Layout hints and general comments
Name	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Package**	**Characteristics**	**Value**		

(table continues…)

Table 3 **(continued) BOM - other supporting components for Cell Supervision Circuit**

Buffer capacitor VS	C_{VS}	50	100	130	nF	SM0603	100 V	100 nF	–	Should be placed as close as possible to the VS pin.
Buffer capacitor VDDC	C_{VDDC}	165	330	430	nF	SM0603	16 V	330 nF	Can be reduced to e.g. 10 V and can be reduced to e.g. 0402.	Should be placed as close as possible to the VDDC pin.
Buffer capacitor VREGOUT	$C_{VREGOUT}$	50	100	130	nF	SM0402	50 V	100 nF	Can be reduced to e.g. 10 V.	Should be placed as close as possible to the VREGOUT pin.
NTC filter capacitor	C_{T_IN}	0	4.7	13	nF	SM0603	50 V	4.7 nF	Can be reduced to e.g. 10 V and can be reduced to e.g. 0402.	Should be placed as close as possible to the NTC connector pins.
Temperature capacitor TMP_GND	C_{TMP_GND}	–	10	–	nF	SM0603	50 V	10 nF	Can be reduced to e.g. 10 V and can be reduced to e.g. 0402.	Should be placed as close as possible to the TMP_GND pin.
Temperature resistor TMP_GND	R_{TMP_GND}	–	100	–	Ω	SM0603	–	100 Ω	Can be reduced to e.g. 0402.	–
NTC filter resistor	R_{TMP}	0	100	1000	Ω	SM1206	–	100 Ω	Optional temperature filter resistor. Can be reduced to e.g. 0402.	–
Input capacitor TMP	C_{TMP}	0	10	13	nF	SM0603	50 V	10 nF	Optional temperature filter capacitor. Can be reduced to e.g. 0402, 10 V.	Should be placed as close as possible to the TMPx pins.
Pull down resistor	R_{Pulldn}	–	33	–	kΩ	–	–	–	–	–

2.1.4 BOM - iso UART termination network

For power-balanced communication, a termination network is required for the last node in the daisy chain. The figure below shows the termination network. The termination network is not required for proper functionality of the device.
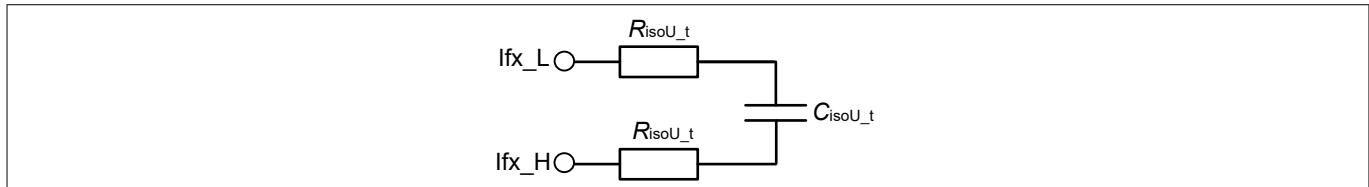
Figure 19   **iso UART termination network**

Table 4   **BOM - iso UART termination network**

Name	Symbol	Min.	Typ.	Max.	Unit	Status as is on evaluation board			Possible optimiz ation	Layout hints and general comments
						Package	Chara cterist ics	Value		
Termination resistor	$R_{\text{isoU\_t}}$	–	100	–	Ω	–	–	–	–	–
Termination capacitor	$C_{\text{isoU\_t}}$	–	250	–	pF	–	–	–	–	–

2.1.5 Layout guideline

The filter capacitors C_F should be placed as close as possible to the IC pins. This is especially important for channel #11 to enable an accurate voltage measurement. The figure below shows an example where the filter capacitor should be placed next to the IC pins (U11, U12).
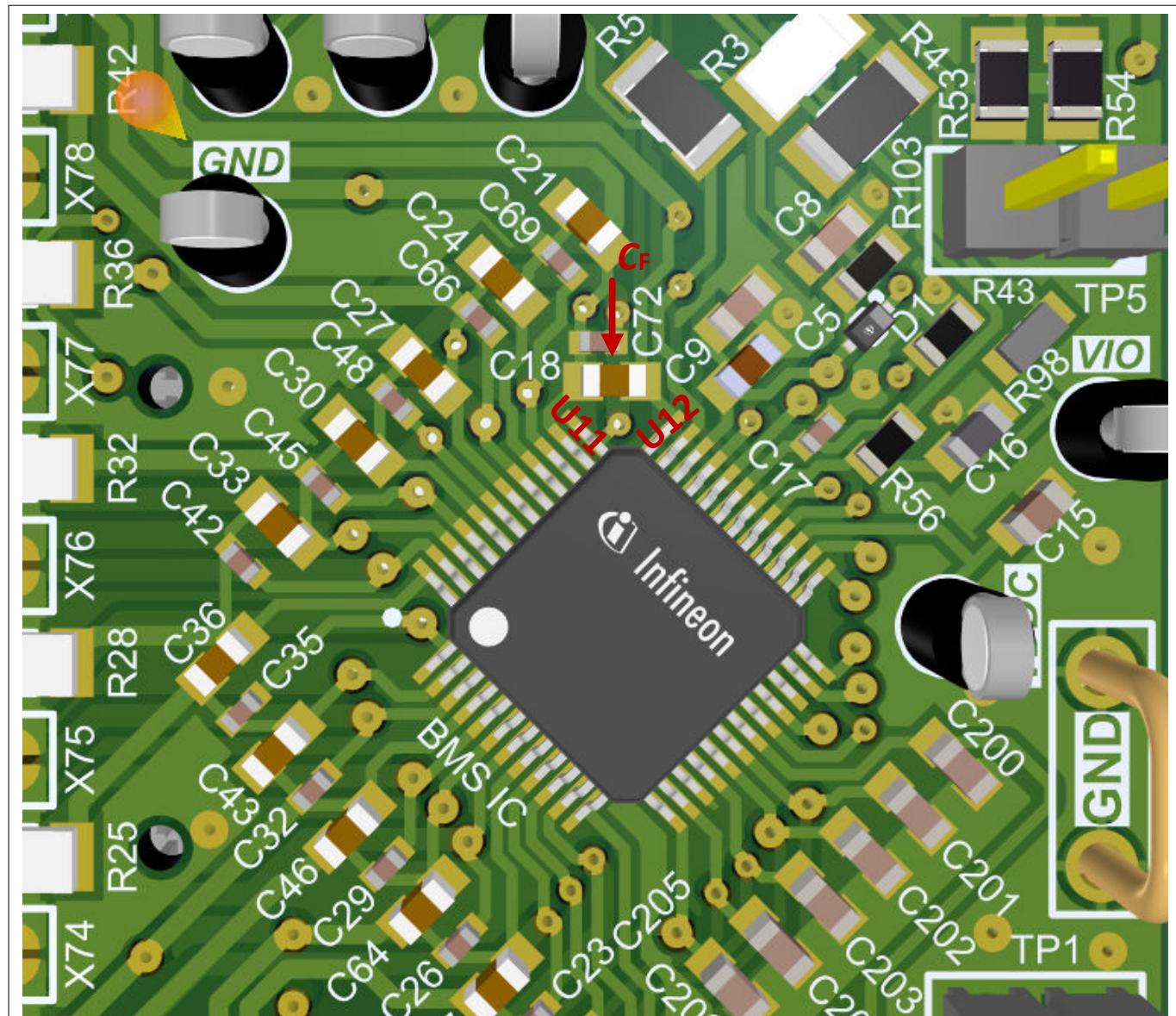
Figure 20   Channel 11 layout guideline

Furthermore, VS and U12 should be separated by routing them away from each other. This is necessary to reduce disturbances (see Figure below).
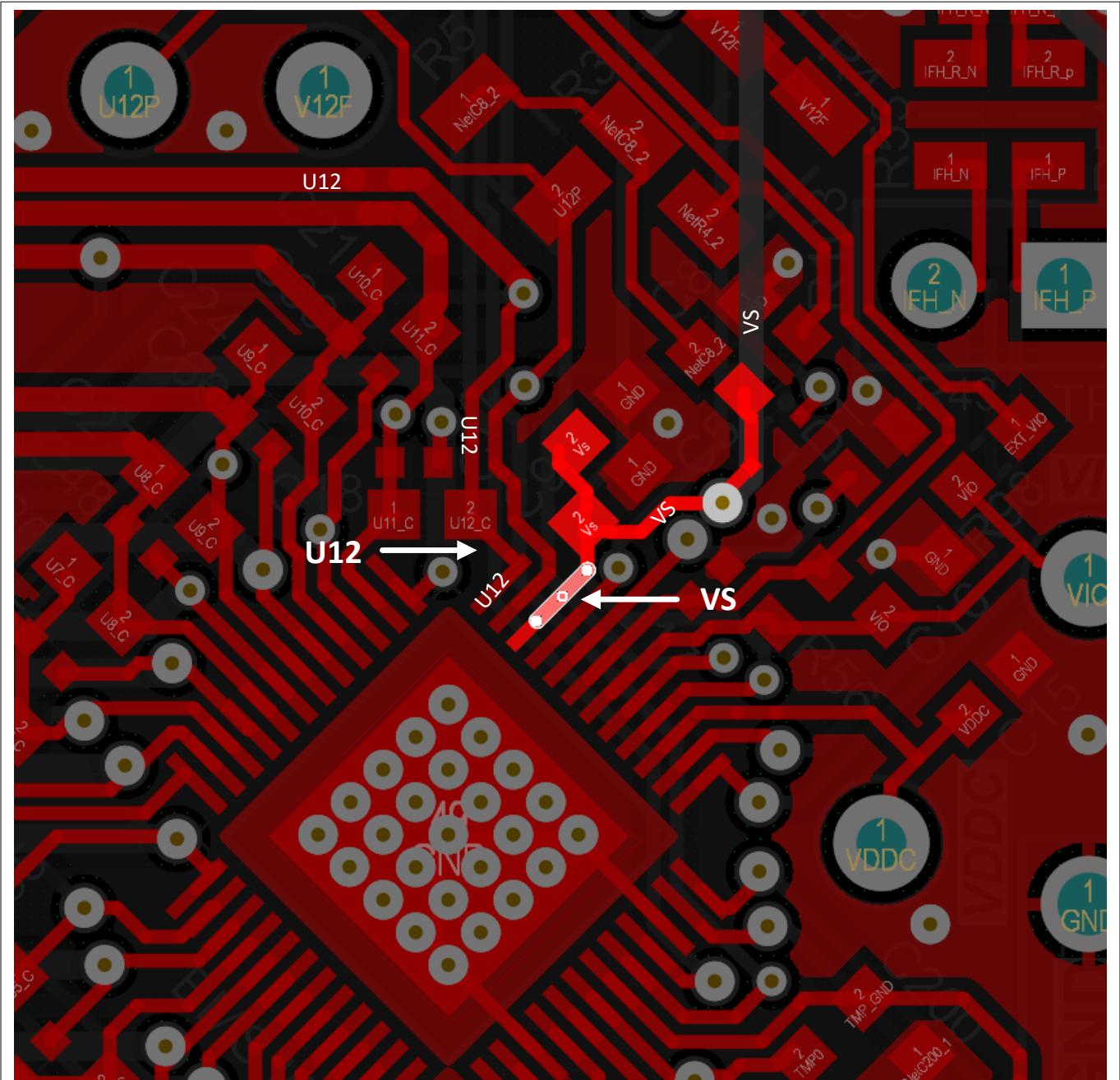
Figure 21   **Routing VS and U12P**

2.1.6   Guidance for unused pins

Note: The n.c. pin 32 shall be connected to GND.

2.1.6.1   Unused input pins

All unused input pins should be connected to GND:

- TMP0, TMP1, TMP2, TMP3, TMP4: directly to GND
- PWM1, PWM0: 33 kΩ to GND (package size e.g. 0603), resistor can be shared.
- GPIO0/UART_LS, GPIO1/UART_HS: 33 kΩ to GND (package size e.g. 0603), resistor from PWM0, PWM1 can be shared.

2.1.6.2 Unused output pins

All unused output pins should remain open.

• ERR

2.1.7 Use of CSC with less than 12 cells

Unused channels shall be connected to the negative potential of the lowest used cell. The connection can be made either directly at the pin or at the connector.
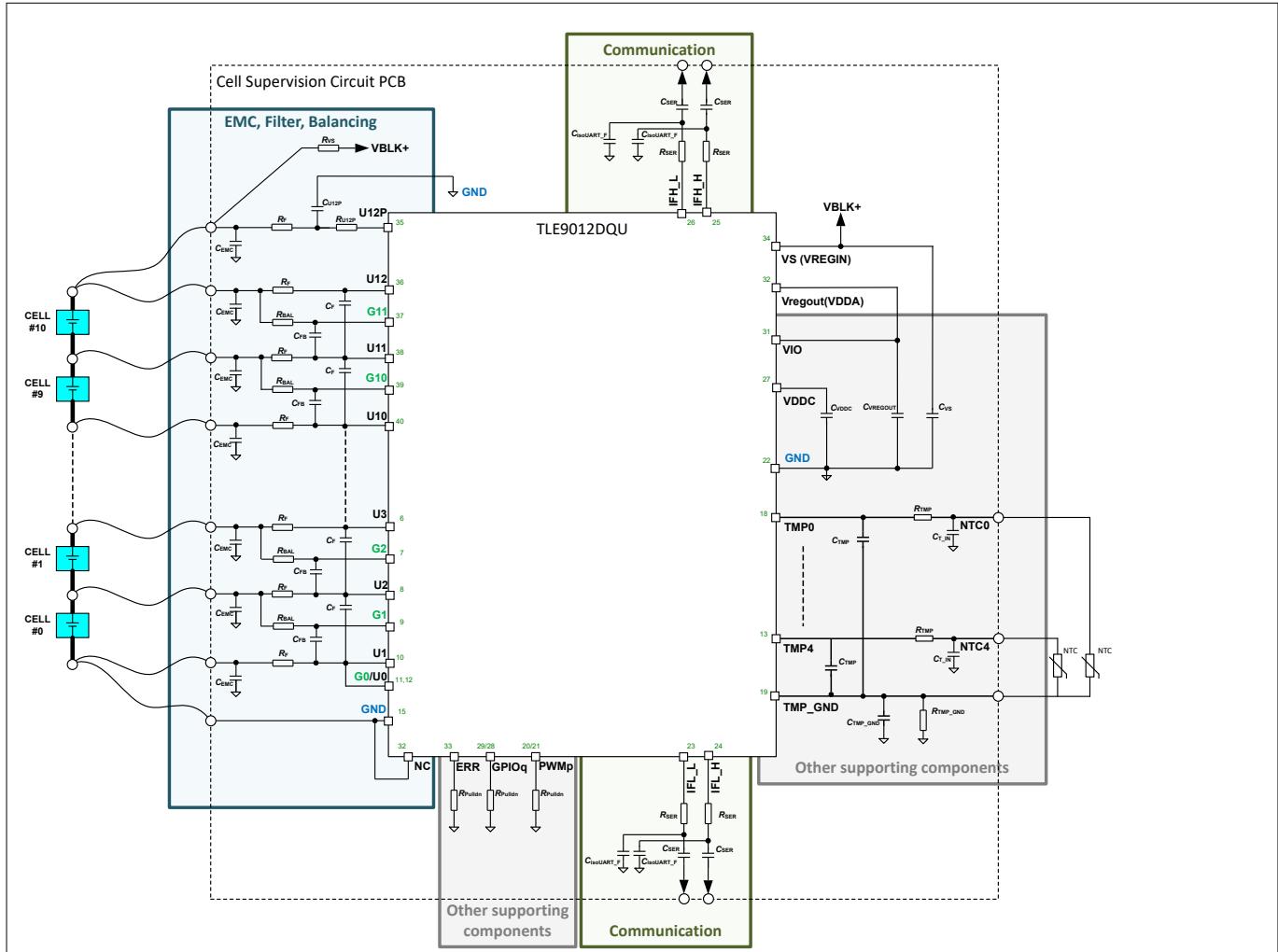
Figure 22 **TLE9012DQU (12 channel) CSC connected to 11 cells (pin)**
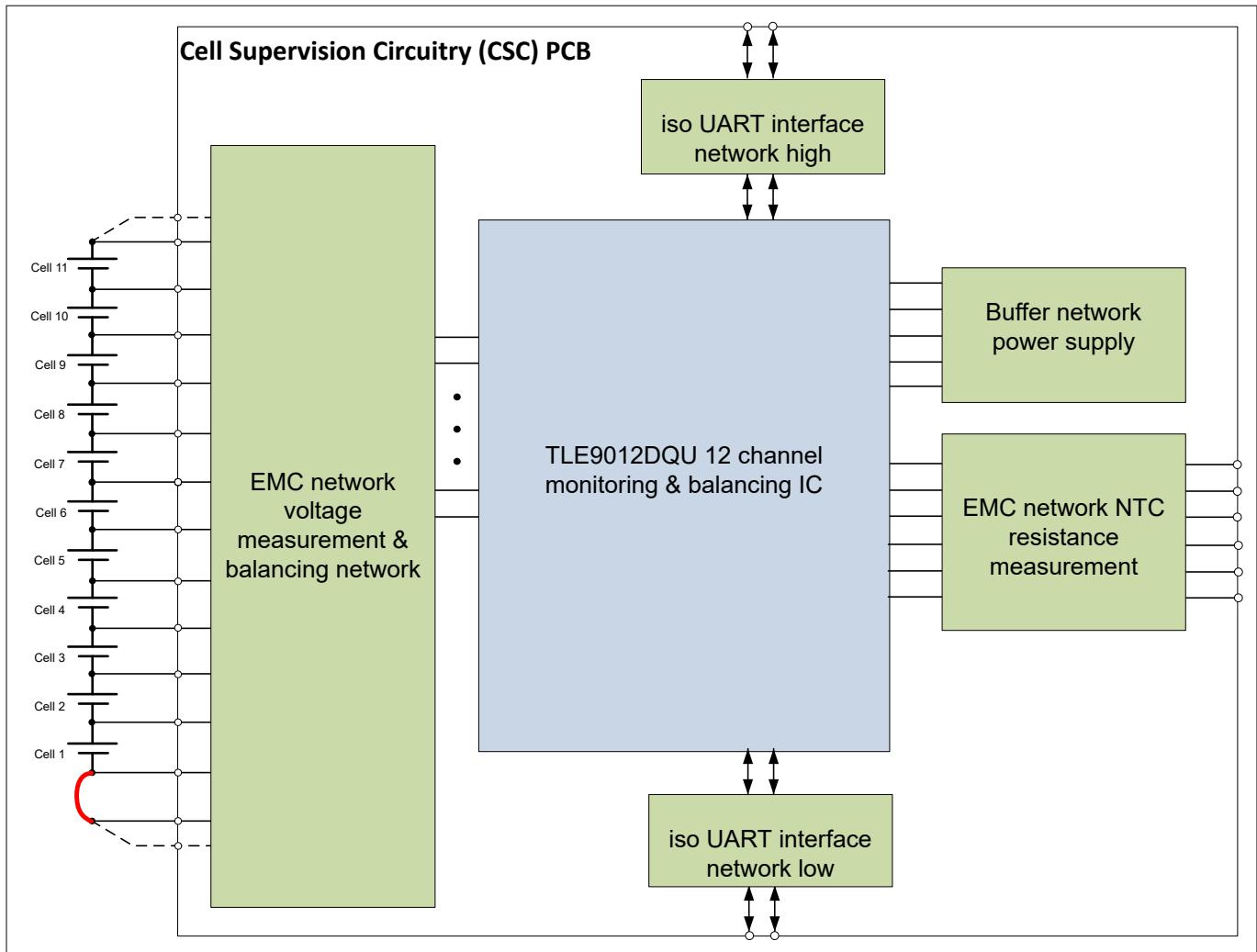
Figure 23   **TLE9012DQU (12 channel) CSC connected to 11 cells (connector)**

2.2 Application schematic transceiver circuit
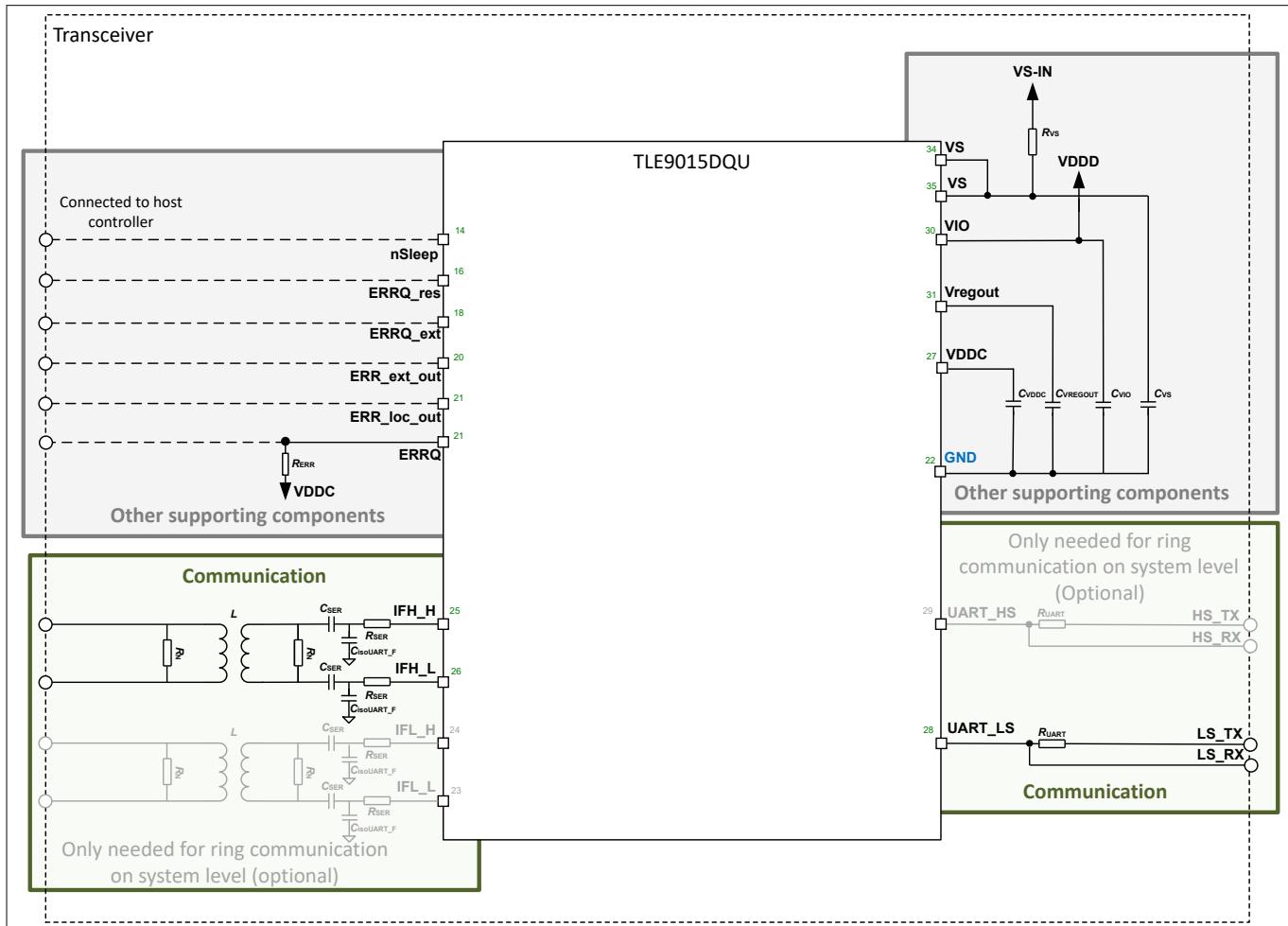
Figure 24 Schematic of the transceiver TLE9015DQU

2.2.1 BOM - communication circuit

Table 5 BOM - communication circuit

Name	Symbol	Min.	Typ.	Max.	Unit	Package	Characteristics	Value	Possible optimization	Layout hints and general comments
						Status as is on evaluation board				
iso UART series resistor	R_{SER}	37.5	39	40.95	Ω	SM0805	–	39 Ω	–	–

(table continues...)

Table 5   **(continued) BOM - communication circuit**

iso UART series capacitor	C_{SER}	0.95	1	1.05	nF	SM1206	500 V	1 nF	100 V can be used because the transformer takes over the galvanic isolation and a 0805 package can be used.	–
HF noise bypass capacitor iso UART	$C_{isoUART\_F}$	0	220	286	pF	SM0603	50 V	220 pF	Can be reduced to e.g. 10 V and different package e.g. 0402.	Optional, especially in combination with a transformer. The $C_{isoUART\_F}$ should be placed close to C_{EMC} (if used) and the common GND path should be as short as possible.
Damping resistor	R_N	–	–	–	–	SM0805	–	240 Ω	–	Depends on used transformer e.g. 1 kΩ with Pulse HM2116ANL transformer.
Transformer	L	–	–	–	–	Available footprint for e.g. • Sumida CEP99P • Pulse HM2106ZNL • Pulse HM2116ANL			–	–
UART network	R_{UART}	0.82	1	5	kΩ	SM0805	–	1.5 kΩ	–	$\tau \leq 50$ ns

2.2.2   BOM - other supporting components

Table 6   **BOM - other supporting components**

						Status as is on evaluation board			Possible optimization	Layout hints and general comments
Name	Symbol	Min.	Typ.	Max.	Unit	Package	Characteristics	Value		

(table continues...)

Table 6   **(continued) BOM - other supporting components**

Buffer capacitor VREGOUT	$C_{VREGOUT}$	50	100	130	nF	SM0402	50 V	100 nF	–	Should be placed as close as possible to the VREGOUT pin.
Buffer capacitor VDDC	C_{VDDC}	165	330	430	nF	SM0603	16 V	330 nF	Can be reduced to e.g. 10 V and can be reduced to e.g. 0402.	Should be placed as close as possible to the VDDC pin.
Buffer capacitor VIO	C_{VIO}	50	100	130	nF	SM0402	50 V	100 nF	Can be reduced to e.g. 10 V	Should be placed as close as possible to the VIO pin. If VIO is connected to VREGOUT, then C_{VIO} is omitted.
Buffer capacitor	C_{VS}	50	100	130	nF	SM0402	50 V	100 nF	–	Should be placed as close as possible to the VS pin.
Filtering resistor	R_{VS}	4.5	5.1	100	Ω	SM0603	–	5.1 Ω	–	–
Error output	R_{ERR}	–	1.5	–	kΩ	–	–	–	A 0402 package can be used.	–

2.3   CSC evaluation board

Physical dimensions: (6.1 x 6.0) cm
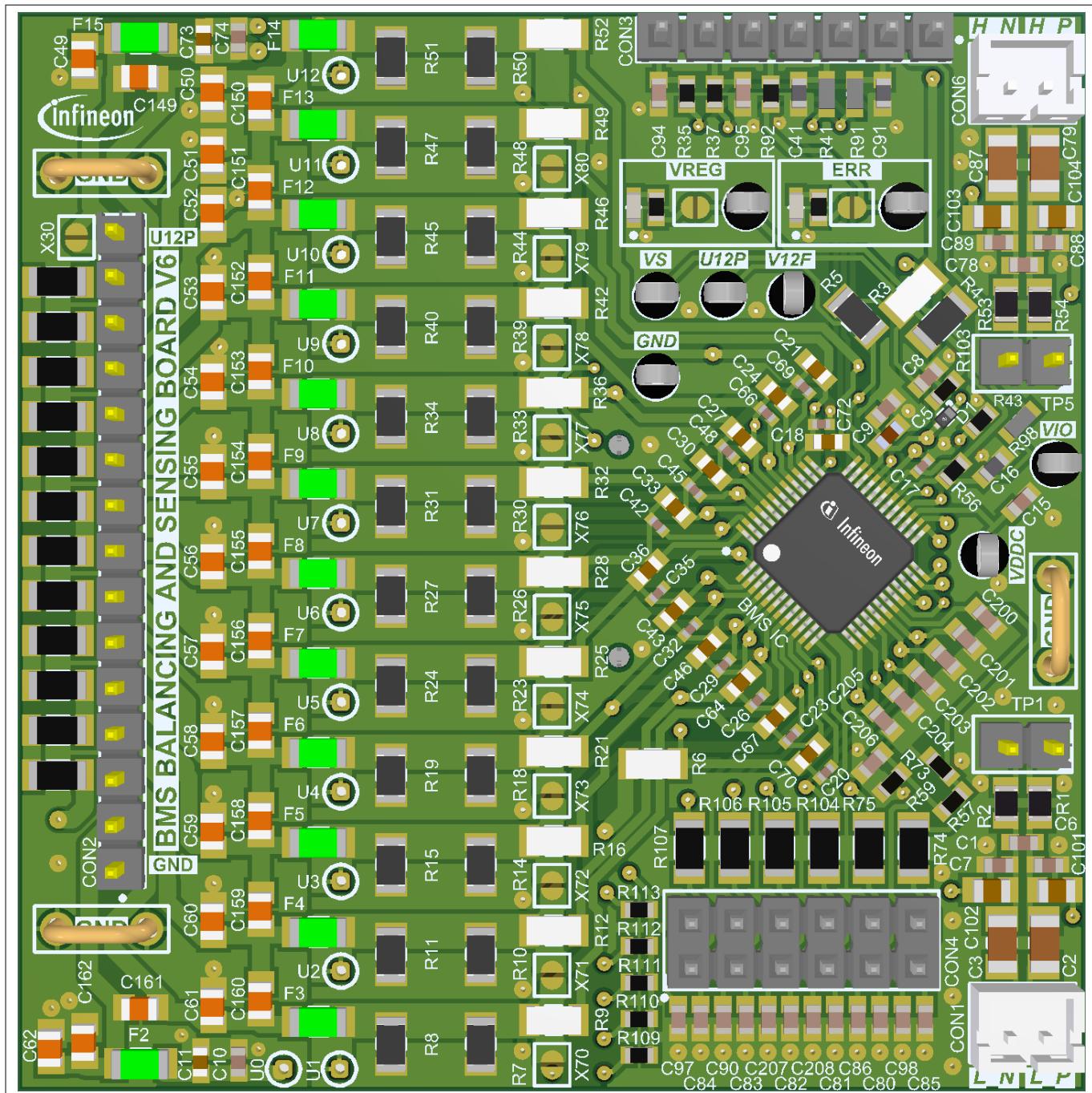
Figure 25 **3D image of CSC evaluation board**

2.4 Transceiver evaluation board

Physical dimensions: (10.0 x 6.0) cm
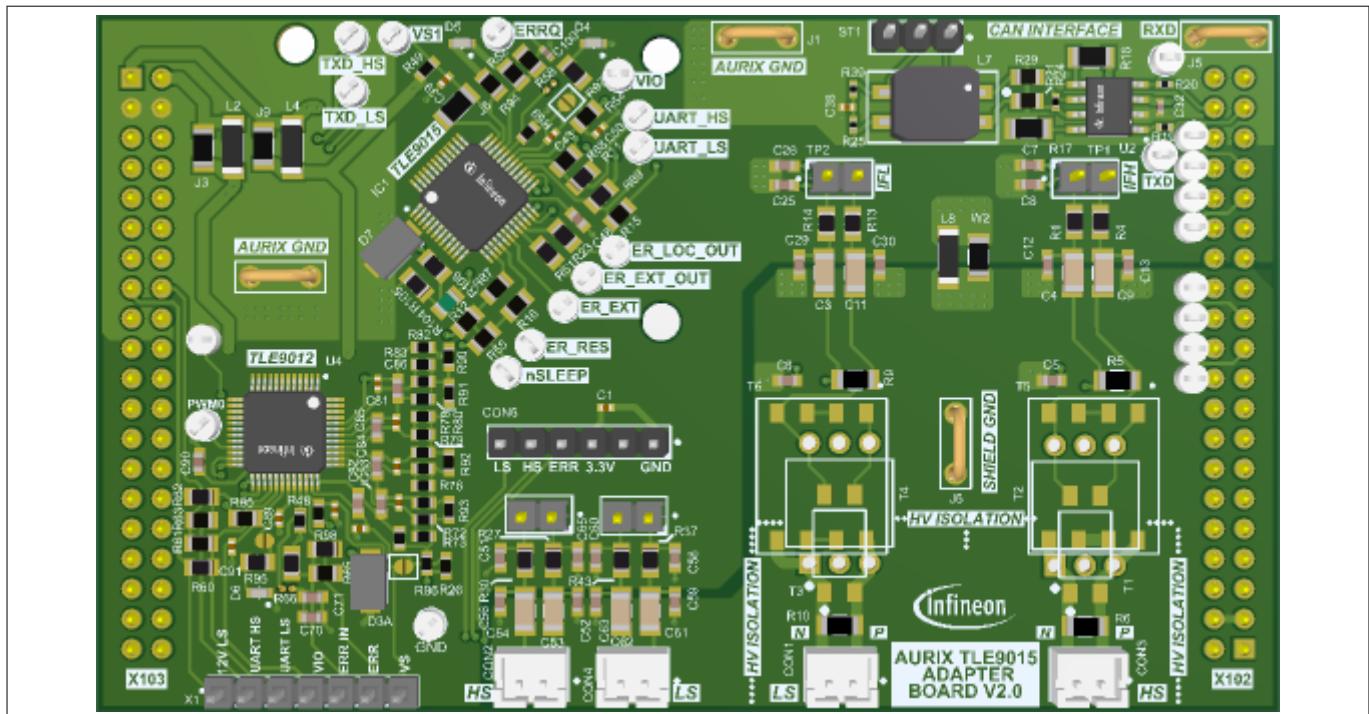
Figure 26   3D image of transceiver evaluation board

2.5   Typical chip performance
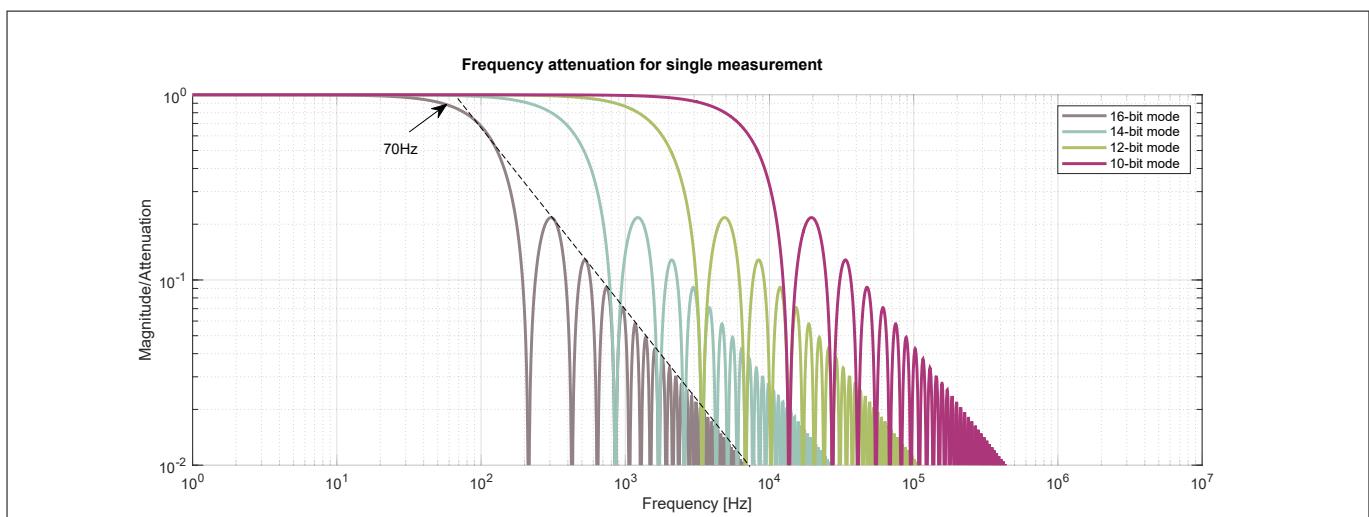
Figure 27   Digital noise filter response for 16-bit, 14-bit, 12-bit and 10-bit mode
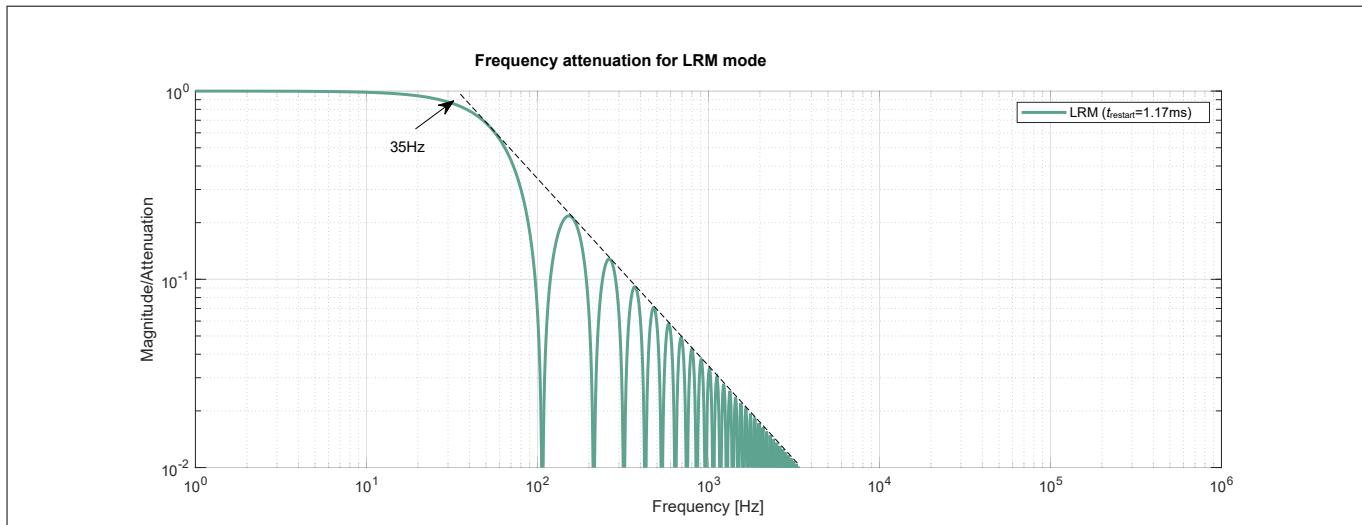
Figure 28   **Digital noise filter response for long running mode ($t_{restart}$ = 1.17 ms)**
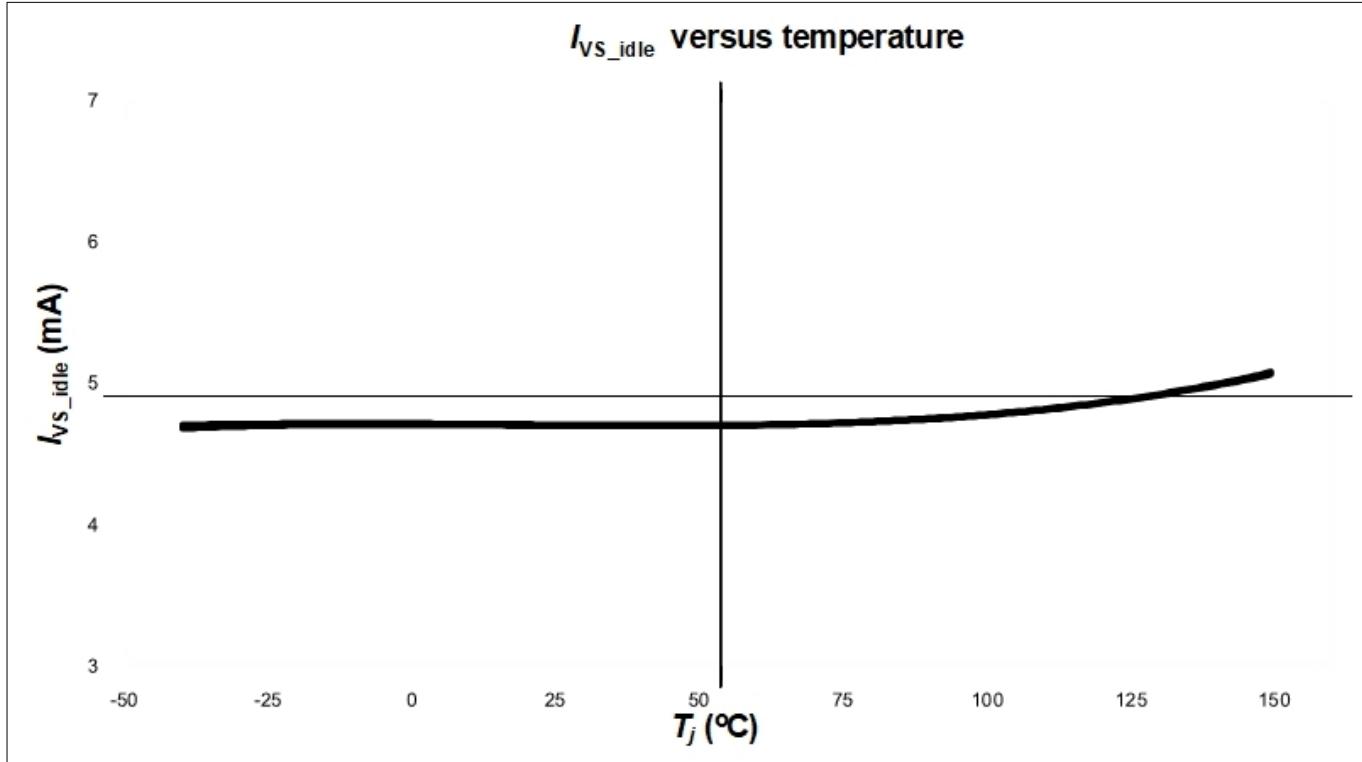
Figure 29   **Typical VS idle current I_{VS_sleep} versus temperature**
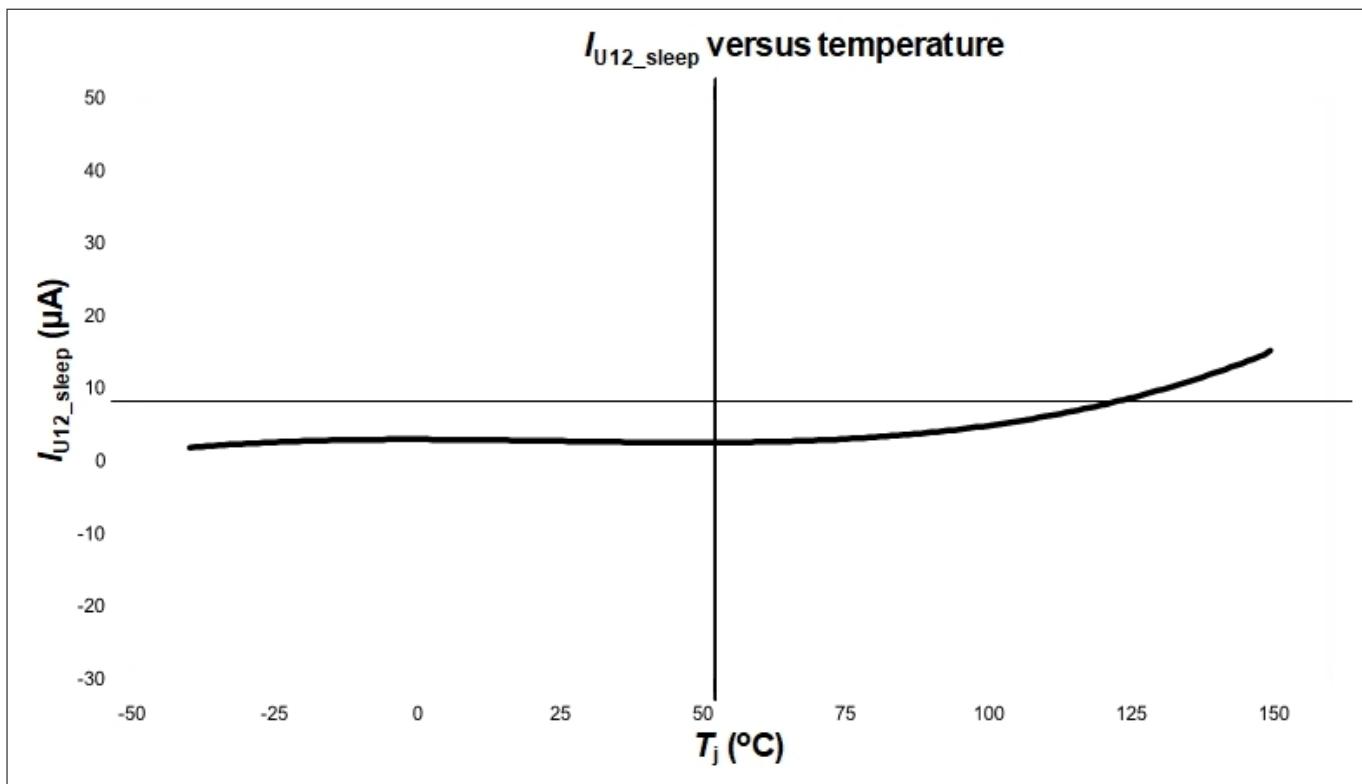
Figure 30   **Typical U12P sleep mode current versus temperature**
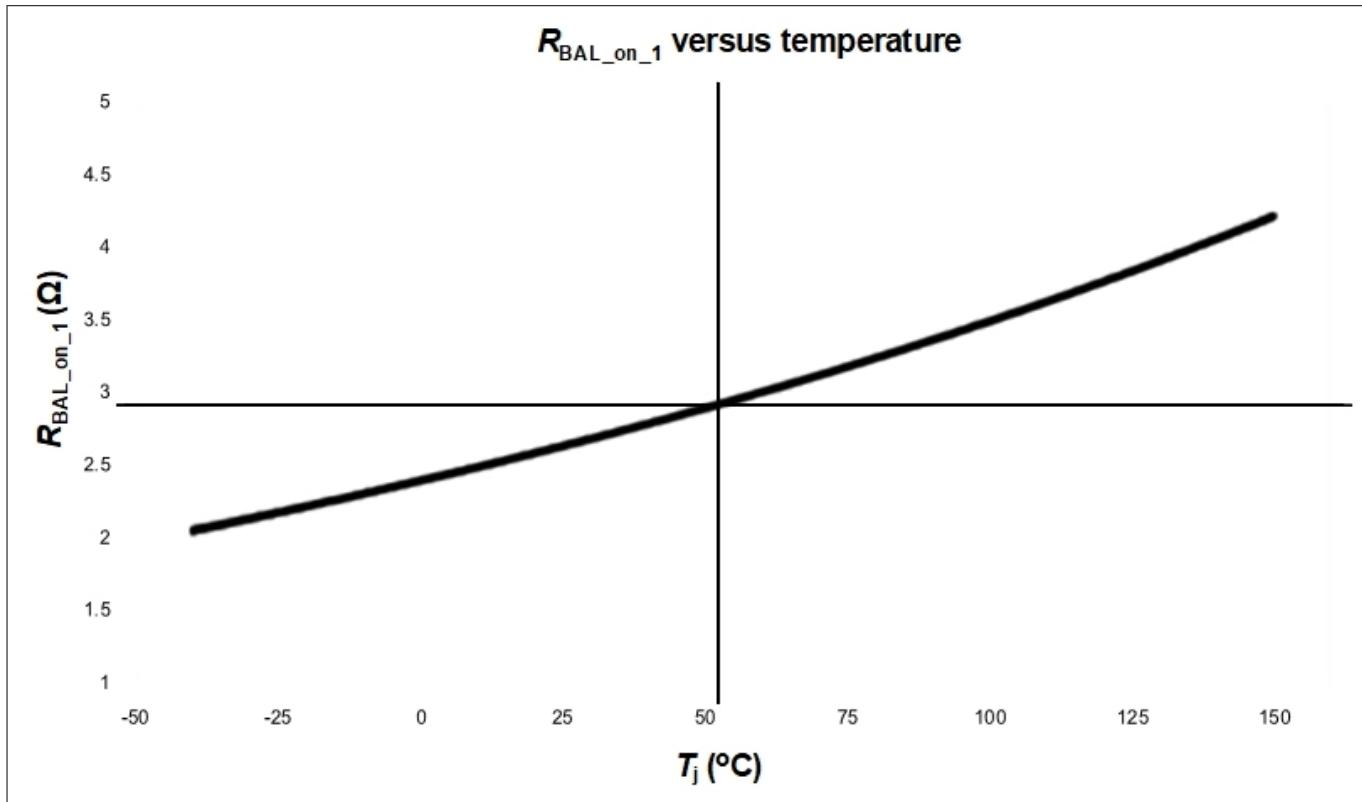
Figure 31   **Typical CB balancing switch on-state resistance - 1 versus temperature**

2.6 EEPROM

If an additional memory is required, an EEPROM can be connected to the TLE9012DQU. The two GPIO pins of the TLE9012DQU can be used for the communication with the memory. For this purpose, the GPIO pins are set and sampled accordingly in order to emulate I2C. Memory requirements:

- I2C interface
- Max. operating current: I_{VIO_comm}
- Supply voltage: $V_{VREGOUT}$
- The minimum clock frequency must be taken into account when choosing the memory. Since the emulation of I2C using bit banging is slow, the minimum clock frequency of the memory should be small.
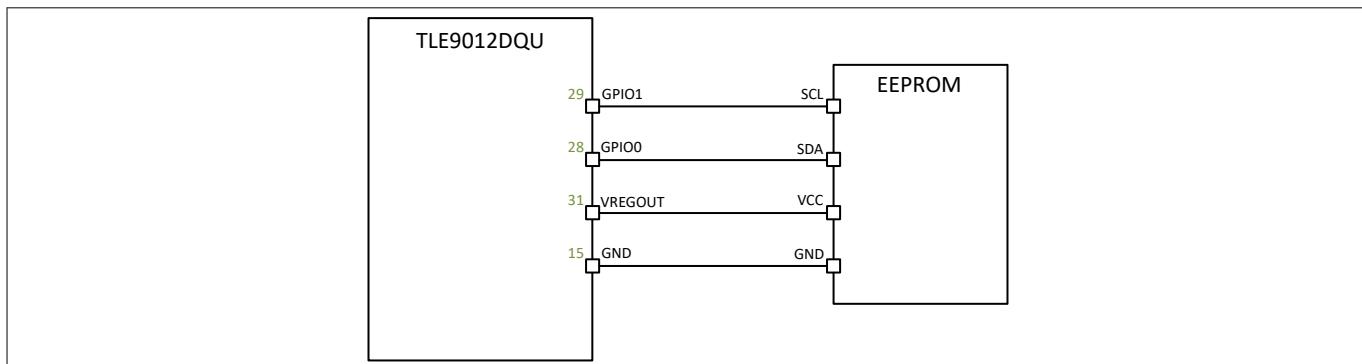
Figure 32   **TLE9012DQU connected to EEPROM**

Note: Instead of using the VREGOUT pin to supply the EEPROM, a third GPIO pin (e.g. PWM0) can be used to supply the memory. When the pin is set to HIGH, the memory is supplied. Otherwise the memory device is switched off. This is beneficial to reduce the supply current.

Depending on the EEPROM used, a defined bit sequence as well as the memory address and the data to be stored must be sent. An example sequence for a write is shown in the figure below.
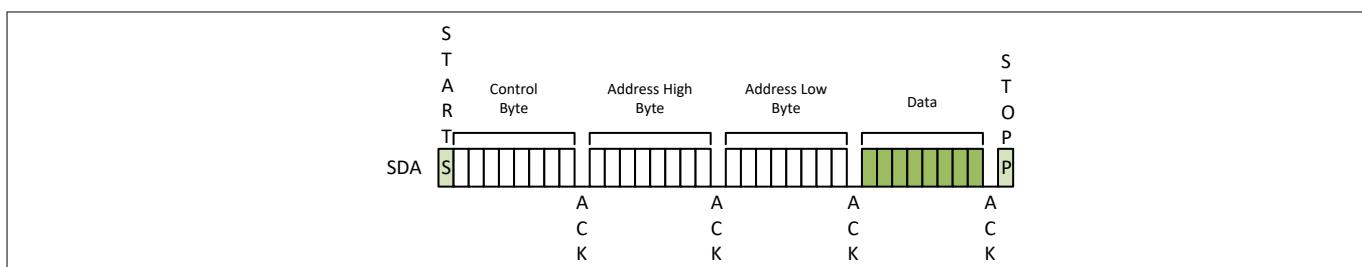
Figure 33   **SDA sequence to write one byte**

The control byte and the address bytes depend on the used memory. With the shown sequence, it takes ~ 15 ms to write one byte. The bit sequence to read one byte is similar to the write sequence. After the memory specific control byte and address bytes, the memory responds with the control byte and the requested data.
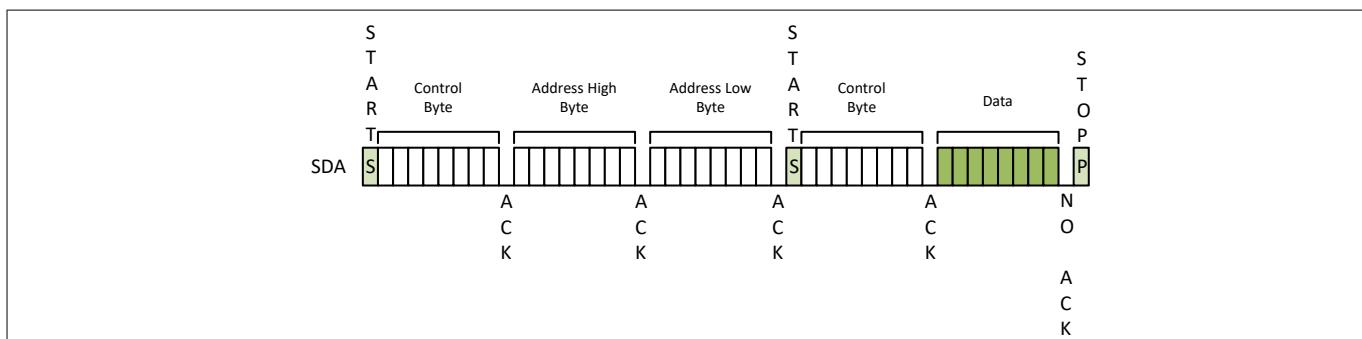
Figure 34   **SDA sequence to read on byte**

With the shown sequence, it takes ~ 18 ms to read one byte.

2.7   13-wire setup

The TLE9012DQU can be also used in a 13-wire setup (the 15-wire setup is shown in Schematic of CSC). In a 13-wire setup, supply and sensing current share one wire for the top and bottom cell. The 13-wire setup influences the PCVM accuracy of the top and bottom cell due to the additional voltage drop forced by the supply current over these wires. A real 15-wire setup (sensing and supply current have separate wires) is used as a reference measurement to have a reference setpoint for PCVM accuracy. For the required voltage stability (dynamic & static), real Li-Ion cells (LFP cells with R_i < 10 mΩ) are used. The intrinsic setup accuracy is 0.5 mV. The figure below shows the difference between the 13-wire and the 15-wire setup for the PCVM accuracy. The cable length from the Li-Ion cells to the BMS Demo Board is 20 cm (3 BMS Demo Board were tested).
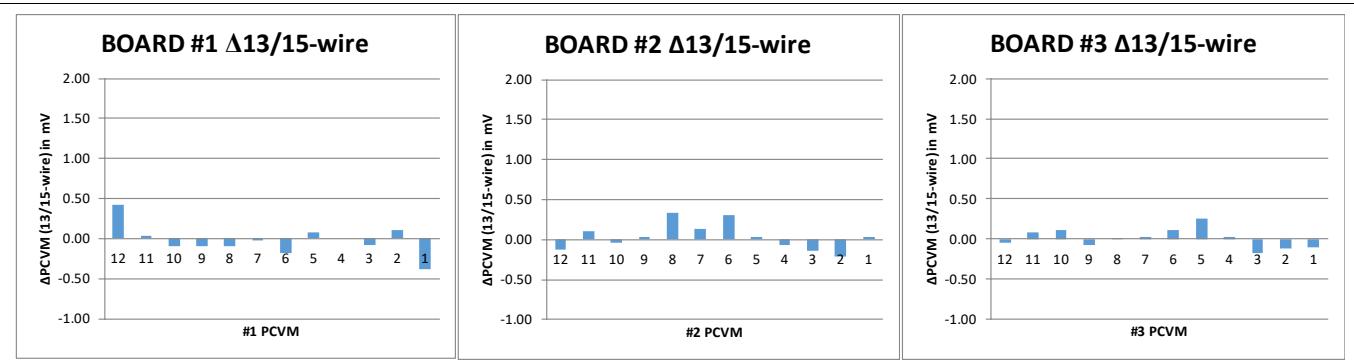
Figure 35   PCVM accuracy Δ 13/15-wire setup with 20 cm cable length

Due to the setup, the differences for a 13 and 15-wire setup are virtually negligible (difference in the range of setup accuracy). As the path from cell to Demo Board is very low ohmic, the supply current has virtually no influence.

The figure below shows the PCVM results for the Demo Board #2 with an increased cable length (cell-to-board) of 1.5 m.
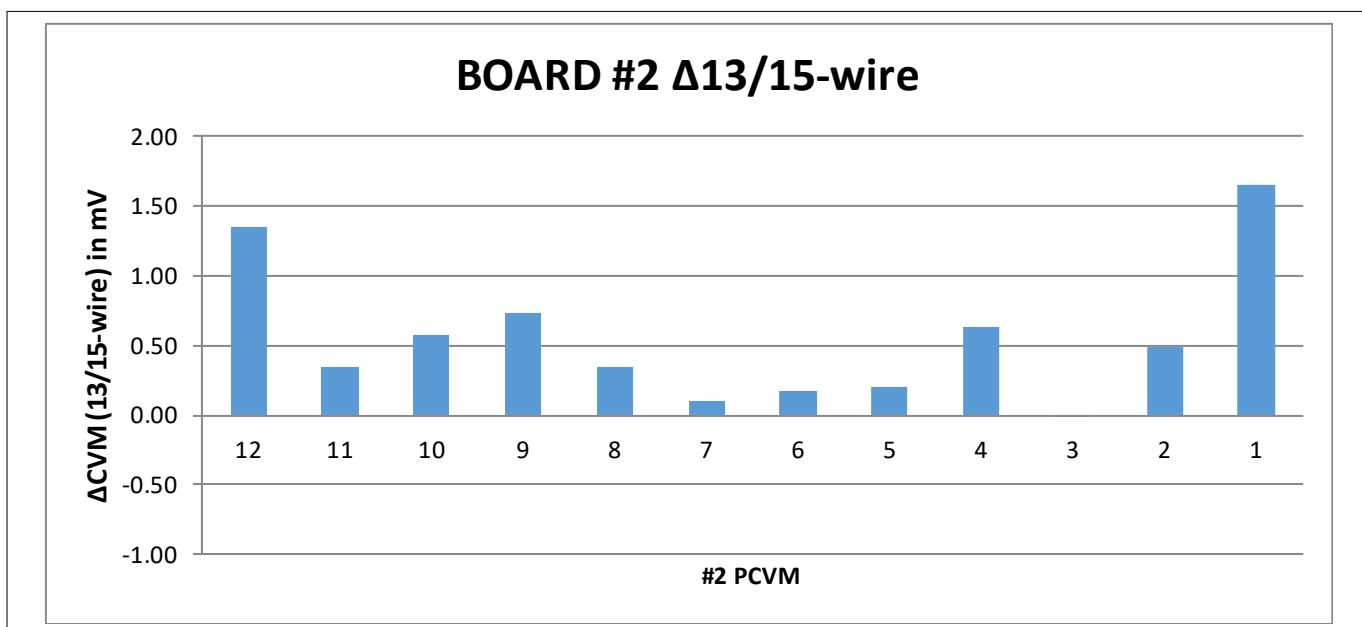
Figure 36   PCVM accuracy Δ 13/15-wire setup with 1.5 m cable length

The comparison of both figures is showing the corner channel effect clearly on channel 1 and channel 12. The effect due to the 13-wire setup (voltage drop over cable) is measurable and equal for the top and bottom channels. To which extent this effect can be observed depends on the setup (cable length, connectors, fuses, voltage stability of source, etc.) and needs to be verified in the real application (in a real car battery). If the

offset at the top and bottom cells in the real car battery is too large to accept, it could also be compensated at the microcontroller as the offset is fixed by system characteristics.

2.8 iso UART communication interface

2.8.1 Introduction

The iso UART protocol is based on a two wire, differential, half duplex physical layer, which the ICs use to communicate between slaves. A more detailed description can be found in the device datasheet. The following section discusses the datasheet specs and how to interpret the iso UART waveforms at different points on the iso UART circuitry for robust communication between the slaves.

2.8.2 Physical layer overview

The datasheet specification states the threshold levels for the iso UART analog receiver interface to convert the analog signals of the physical layer to useful digital signals for the bus timing protocol:

- iso UART current threshold "high" $I_{isoU\_th\_high}$ indicates the positive edge level to trigger a digital "1" signal.

- iso UART current threshold "low" $I_{isoU\_th\_low}$ indicates the negative edge level to trigger a digital "0" signal.

The figure below shows how the iso UART interfaces are configured in the Primary on Bottom (PoB) topology. In this topology, the low side interface is configured as receiver mode (RX) which receives the iso UART physical signals and translates them to digital signals for further interpretation. The high side interface is then configured to transmitter mode (TX) which drives the digital signal on the physical link.
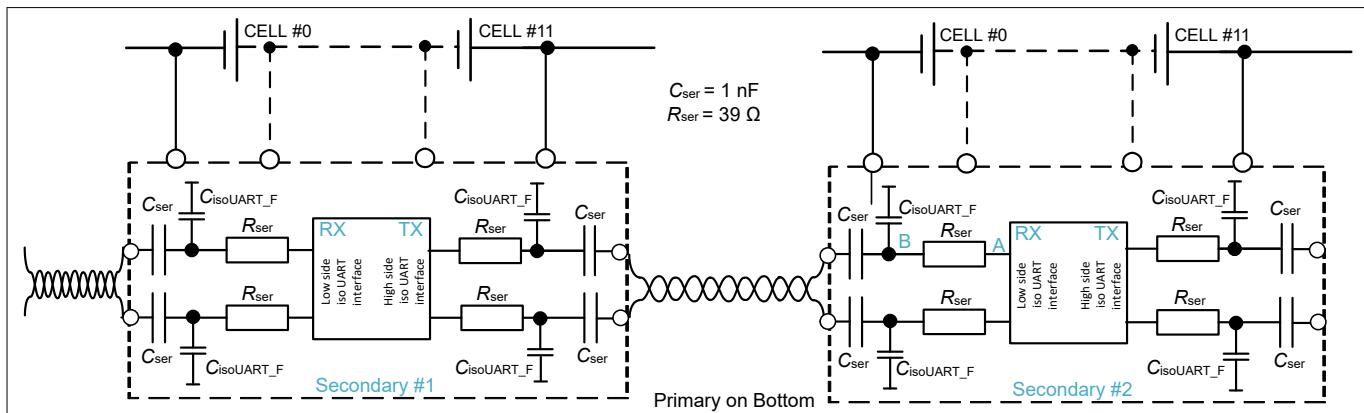
Figure 37   Primary on Bottom communication

The physical and digital signals are illustrated as an example below.
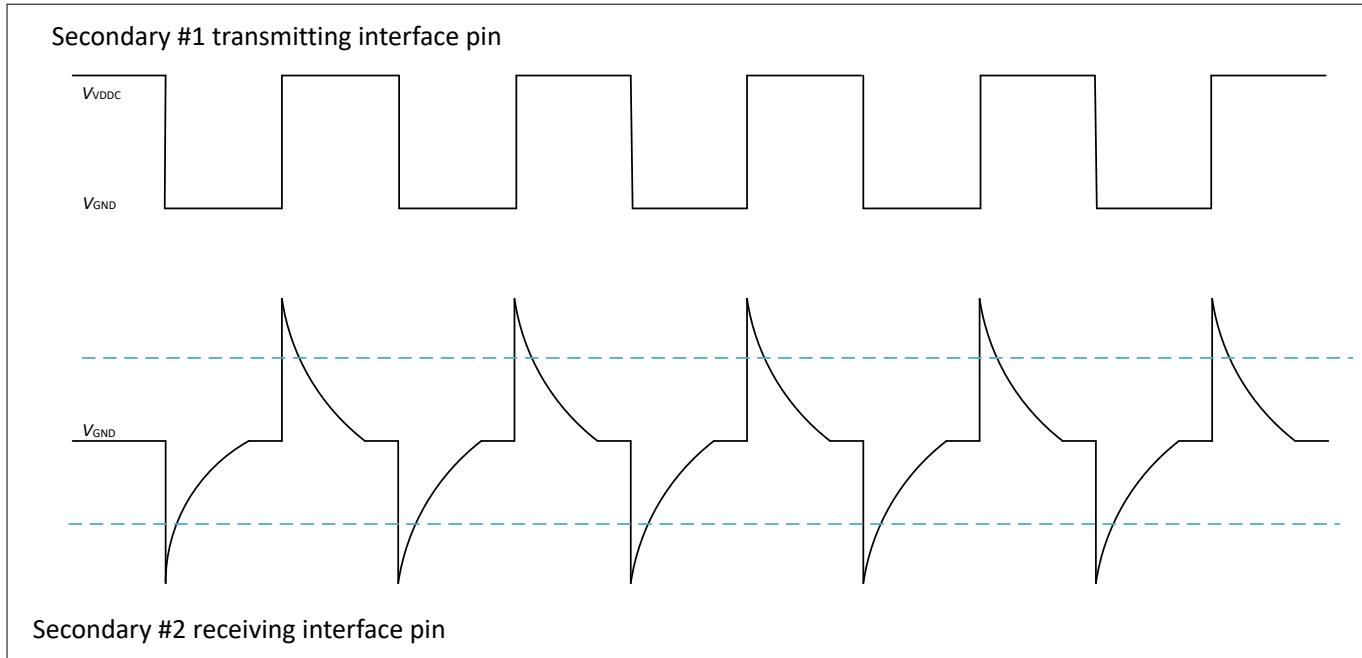
Figure 38　　　**iso UART digital and analog signals**

2.8.3　　iso UART measurement point

In order to enable the secondary #2 to propagate the correct digital signals at its iso UART TX interface, the analog signals at its RX pins must meet the threshold requirements (blue dash line). Measured at point B with respect to ground as shown in the Figure below, the negative signal must cross the blue line $I_{isoUART\_th\_low\_min} \times (R_{on}+R_{ser})$ to trigger a digital "0". For a digital "1" to be successfully triggered, the positive edge signal must cross the blue line $I_{isoUART\_th\_high\_max} \times (R_{on}+ R_{ser})$.
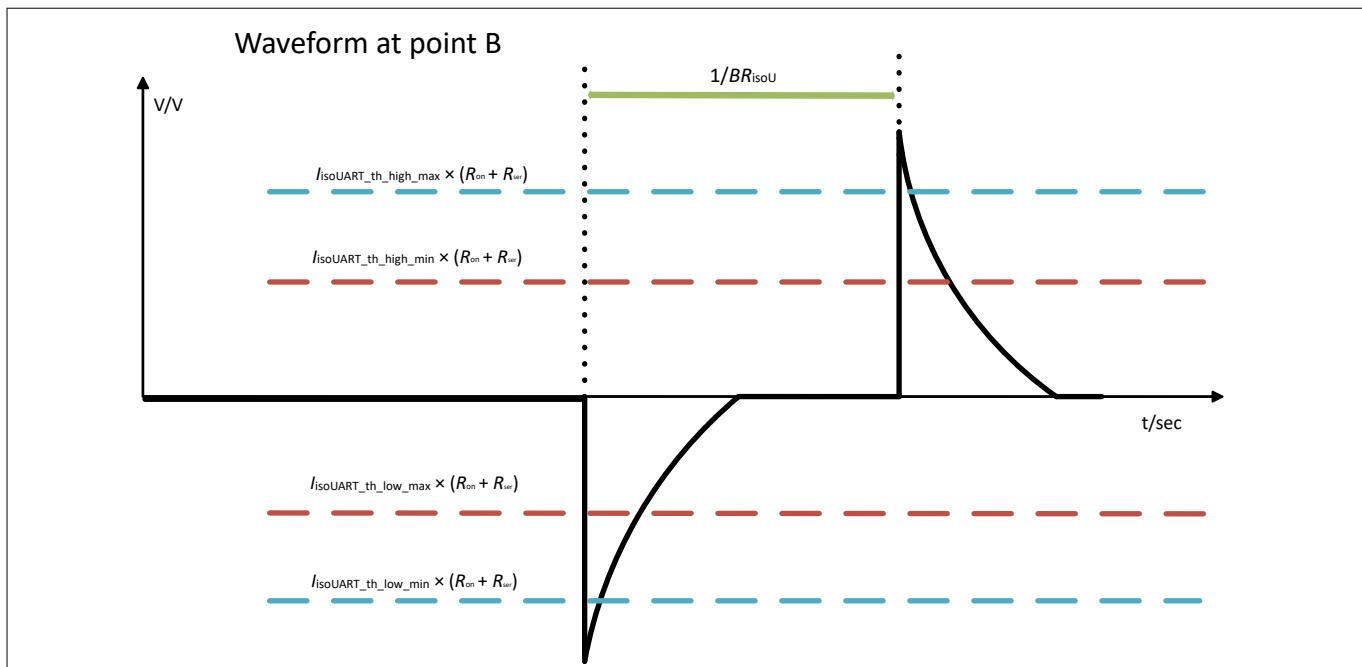
Figure 39　　　**iso UART signal threshold level interpretation at point B**

If the signal is measured at Point A (directly at the IC pin) with respect to ground, the threshold level should be reduced by the value R_{ser} (see Figure below).
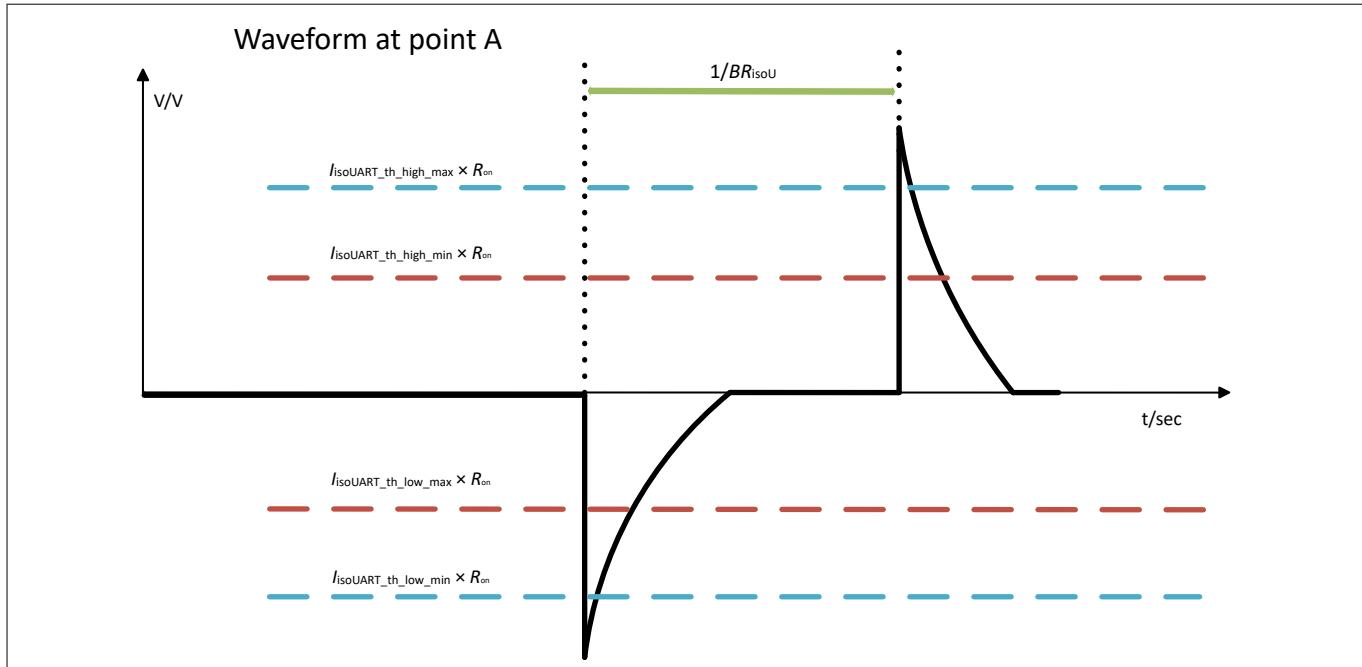
Figure 40   iso UART signal threshold level interpretation at point A

2.8.4   Capacitive coupled signal

For capacitive signals, the guideline is to follow the requirements illustrated in the chapter iso UART measurement point depending on the measurement point. The figure below gives an example of the typical application use case using the sensing IC evaluation board. The C_{ser} and R_{ser} used is 1 nF and 39 Ω respectively. R_{ser} is preferred to be fixed at 39 Ω and the user can tune the C_{ser} to meet the threshold requirement. This tuning may have an impact on the EMC performance, therefore it should be evaluated to fulfill the EMC system level requirements by the user in the final system. In this figure, the green signal at the secondary iso UART receiver input meets the threshold requirements and the secondary is able to transmit the correct red digital signals at its corresponding iso UART TX interface.
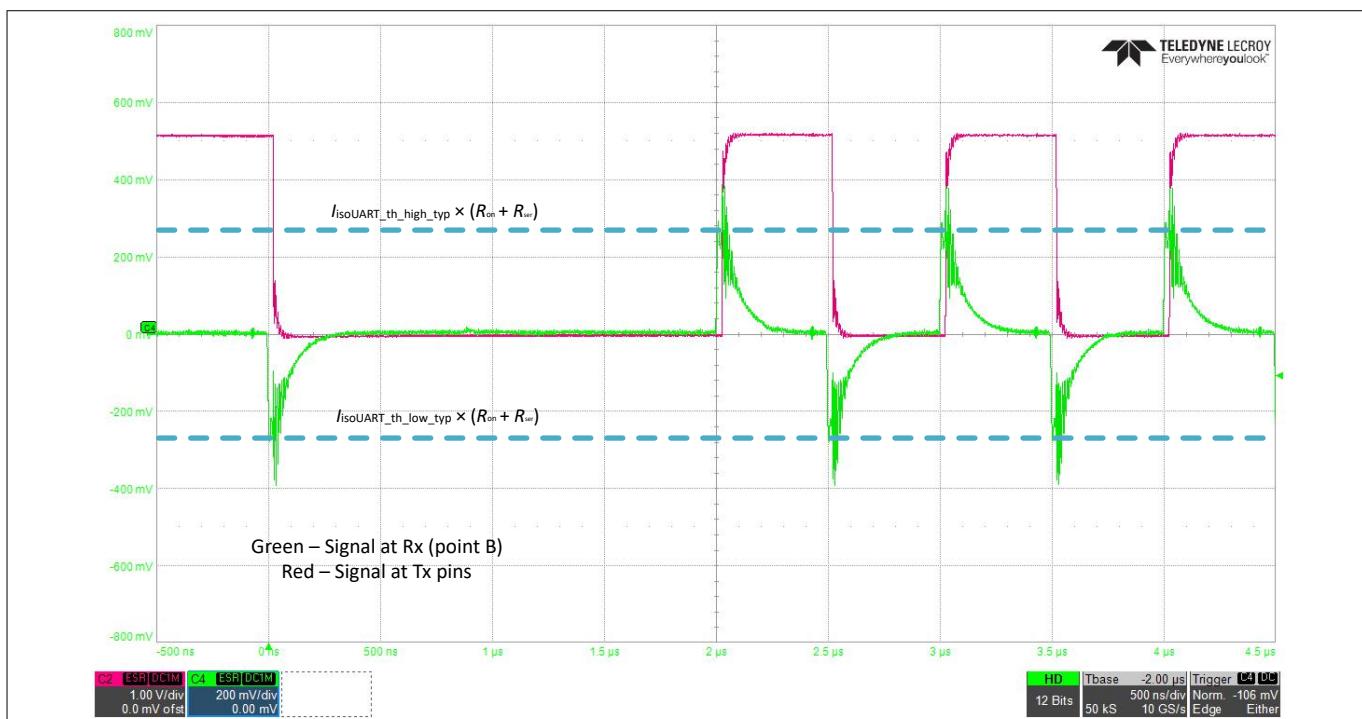
Figure 41   Capacitive coupled iso UART signals between two slave

2.8.5 Transformer coupled signals

Due to the isolation requirement, it may be necessary to implement a transformer between the low voltage and high voltage domain (see Transformer based circuitry at transceiver). In such an application scenario, the iso UART signals have a high tendency to oscillate due to the introduction of high inductance in the communication link.

Note: The information given is as a hint for the implementation of the Infineon Technologies components only and shall not be regarded as any description or warranty of a certain functionality, conditions or quality of the Infineon Technologies component(s). Infineon recommends verifying the transformer selection and tuning also under system level EMC requirements within the real application environment.
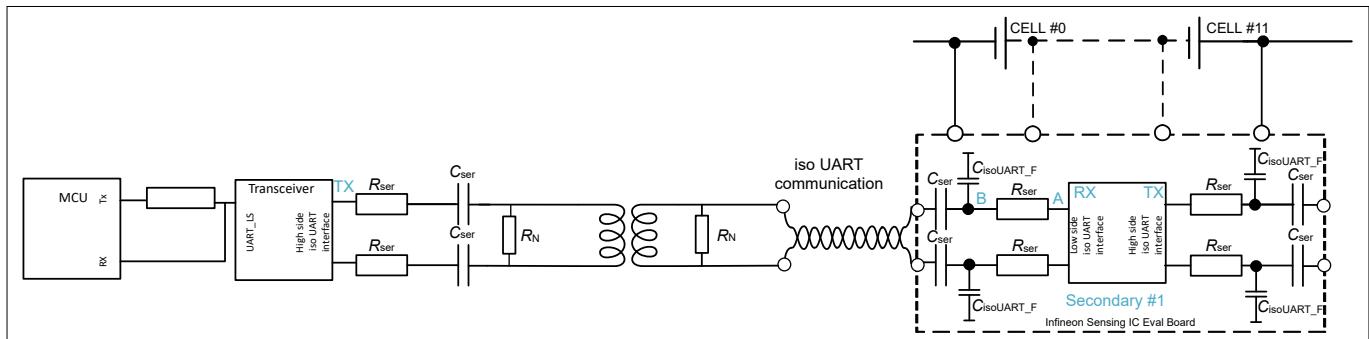
Figure 42   Transformer based circuitry at transceiver

Within a bit duration ($1/BR_{isoU}$), the oscillating iso UART signal should not cross the prohibited threshold $I_{isoUART\_th\_high\_min} \times (R_{on} + R_{ser})$ or $I_{isoUART\_th\_low\_max} \times (R_{on} + R_{ser})$ to avoid false triggering of the digital signal. The oscillation can be damped by adding a damping resistors R_N as shown in

Transformer based circuitry at transceiver

.
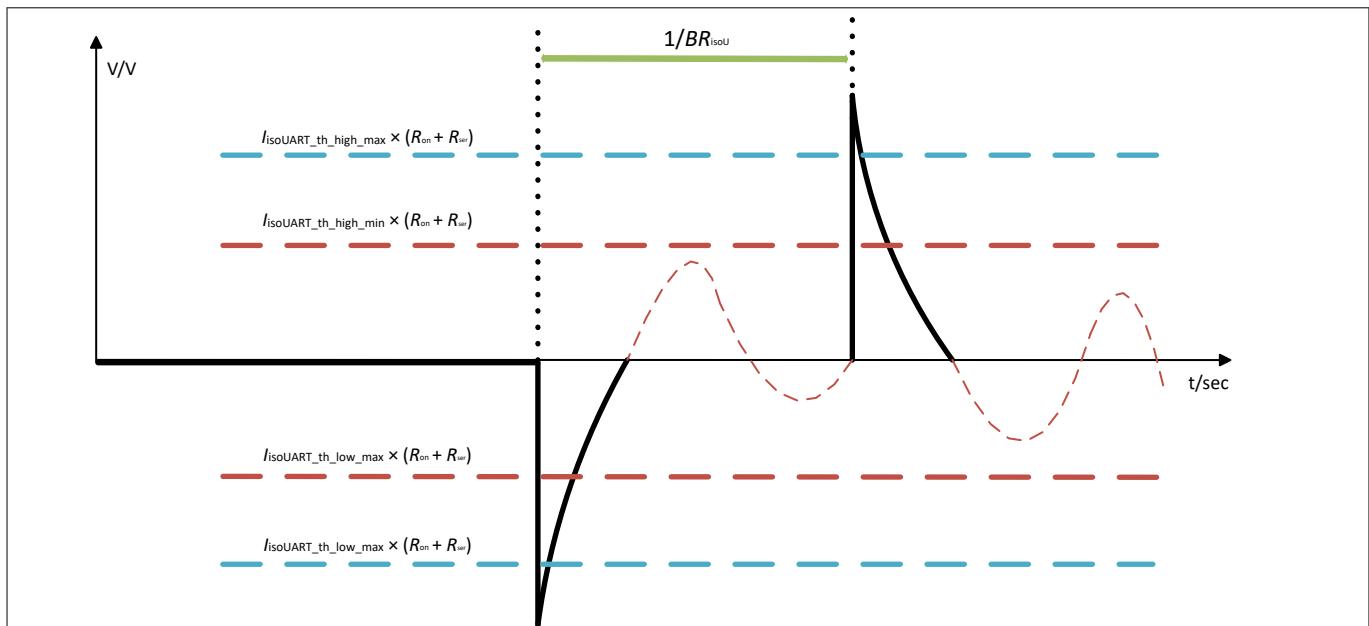
Figure 43   Transformer coupled signal at point B

Figure iso UART waveforms with different damping resistors shows how the damping resistor affects the oscillation waveform. A smaller resistor is able to damp the oscillation better but is also making the first spike narrower.
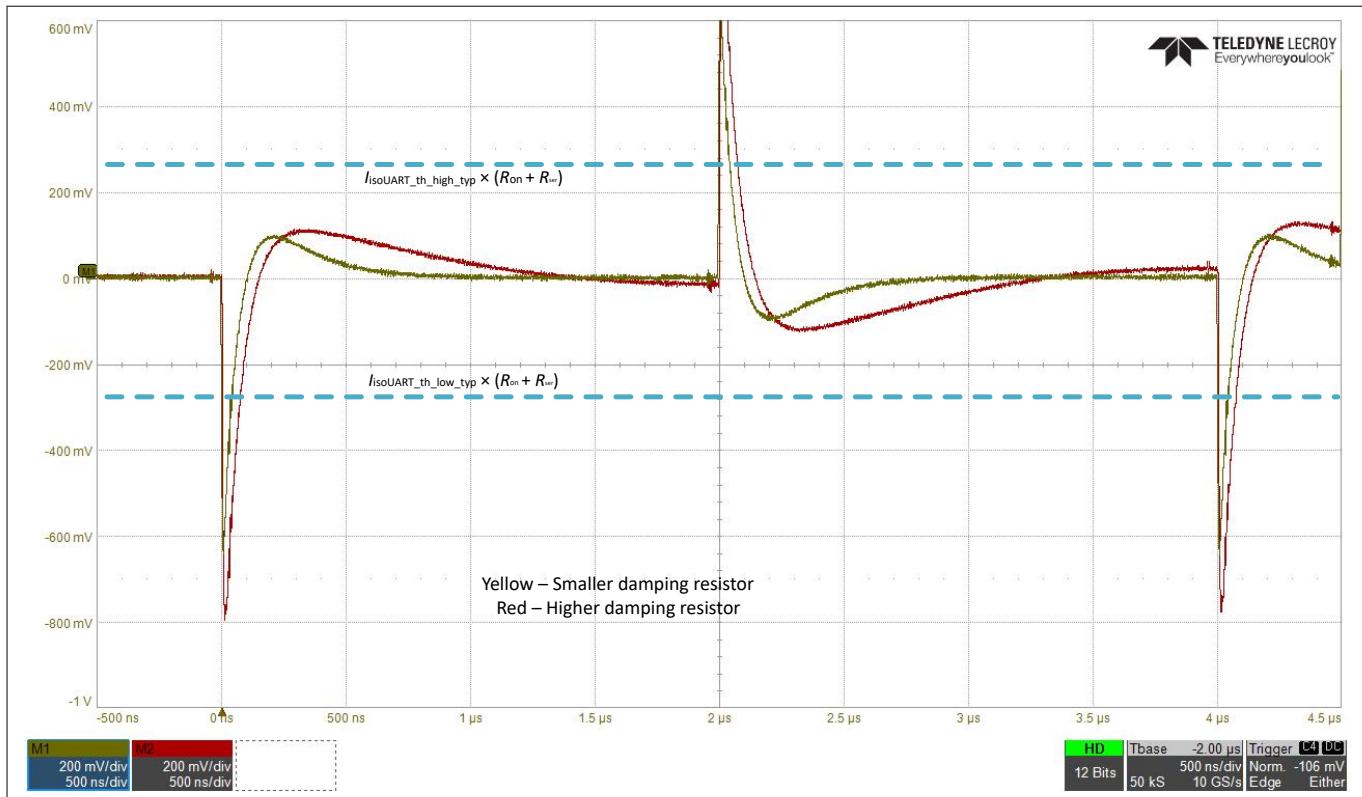
Figure 44 **iso UART waveforms with different damping resistors**

The iso UART physical layer thresholds ($I_{isoUART\_th\_high\_min}$, $I_{isoUART\_th\_high\_max}$, $I_{isoUART\_th\_low\_min}$, $I_{isoUART\_th\_low\_max}$) are defined in the IC datasheet. A high sensitivity current probe can be used to measure the iso UART current in one of the iso UART communication wires (see figure Current probe measurement). In cases where an iso UART current measurement is not possible, the iso UART voltage measurement can be realized with normal oscilloscope probes. *Note: A differential voltage measurement at the R_{ser} (39 Ω) resistor (the differential voltage needs to be divided by 39 Ω) is a good way to measure the current which passes the receiver. If a current probe is used (which is better than just measure the single ended voltage at the iso UART pin), a higher current will be measured (because a part of this current is shorted by EMC caps $C_{isoUART\_F}$ and does not pass the receiver).*
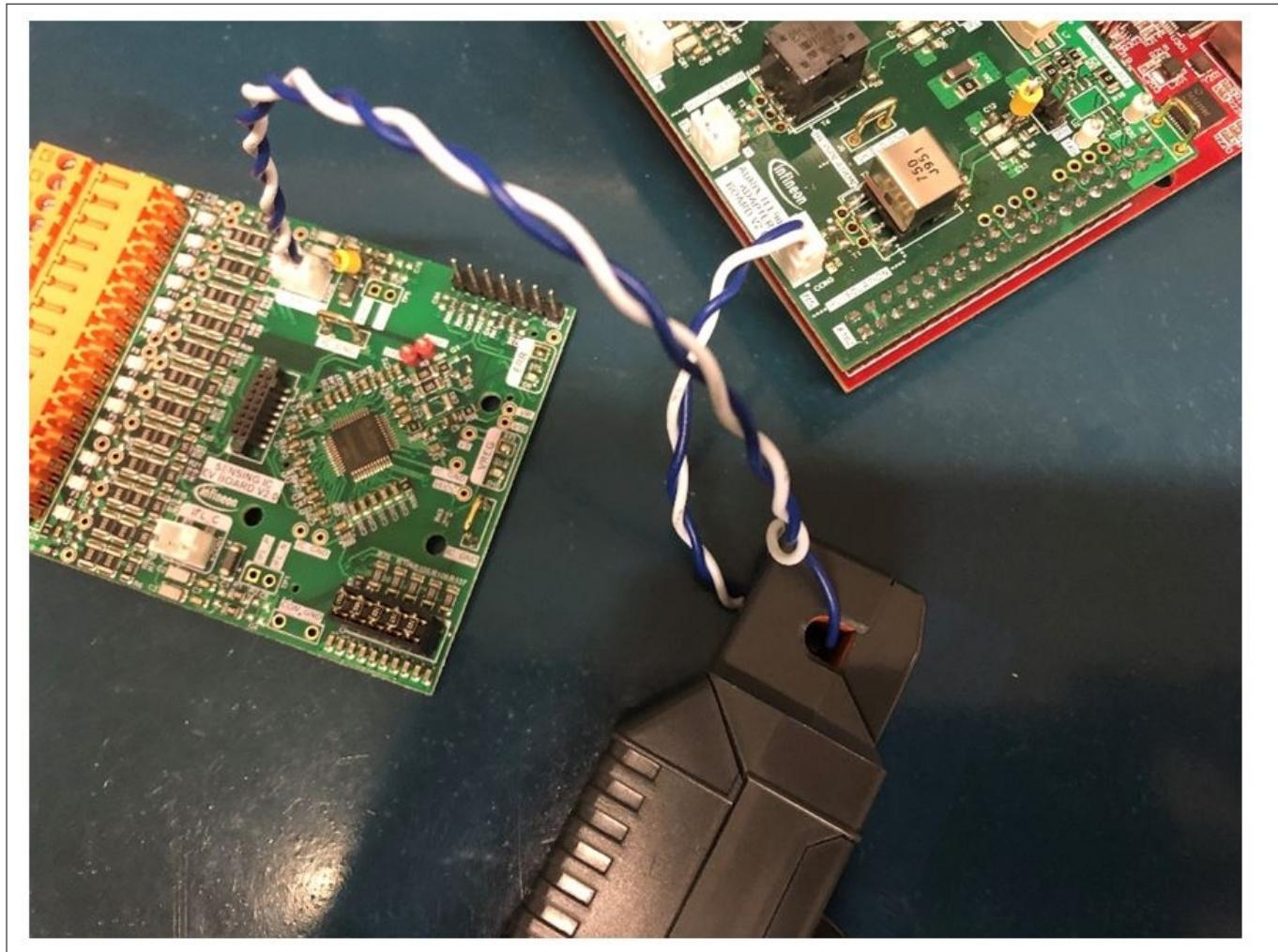
Figure 45   **Current probe measurement**

The iso UART current waveform can be used to determine the overdrive current I_{od} and the pulse duration t_{pulse} (see figure iso UART waveform).
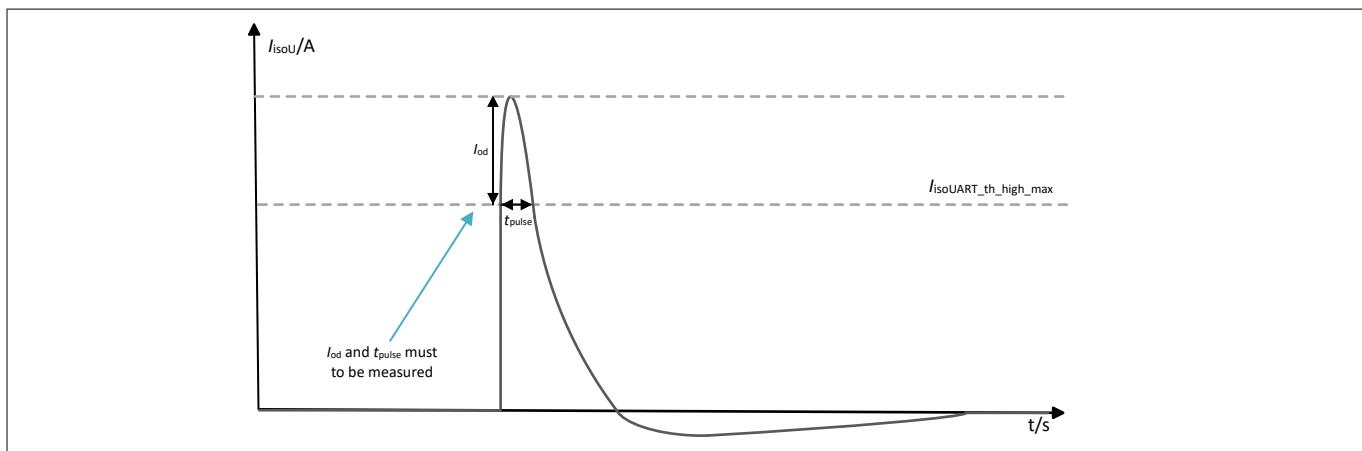
Figure 46   **iso UART waveform**

The resulting I_{od} should fall on the upper right part of the graph in figure Overdrive current to ensure that bits are correctly detected.
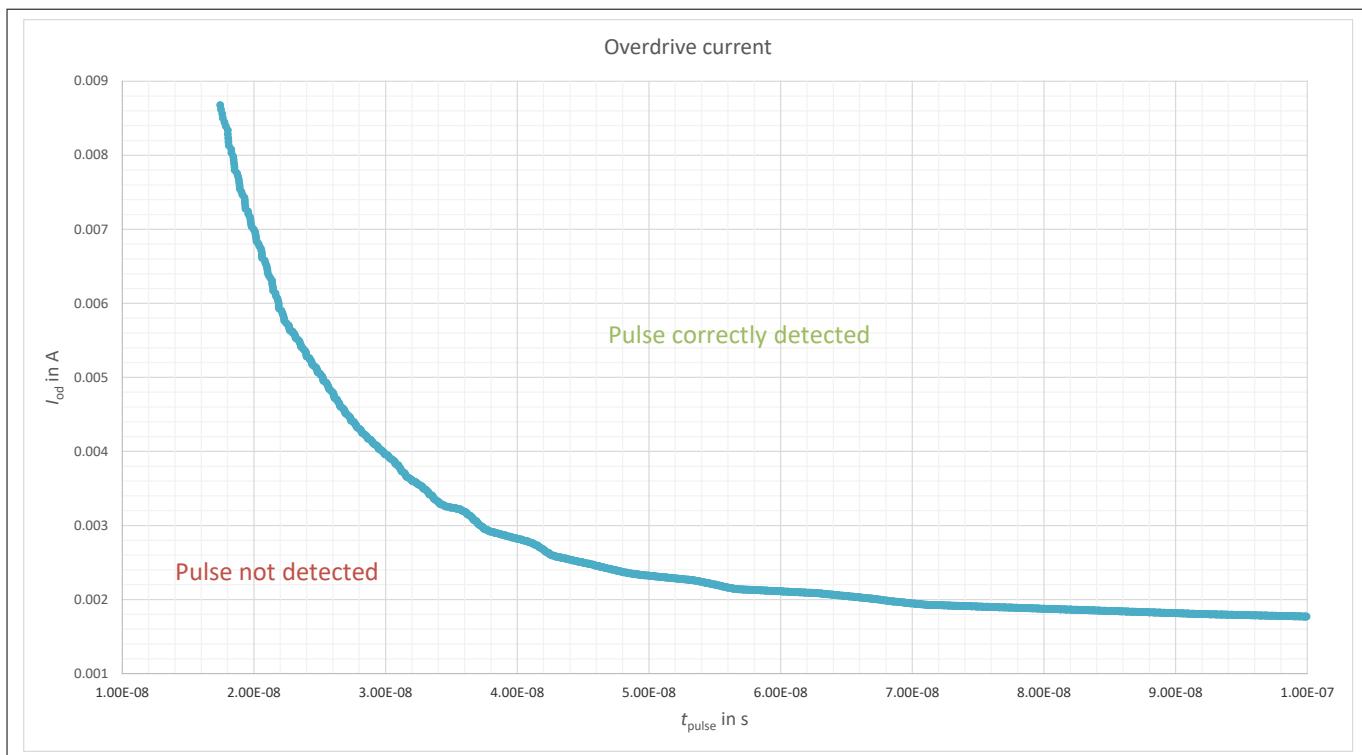
Figure 47   Overdrive current

For example in figure iso UART current probe measurement - CEP99P (2x510R), a peak voltage of 17 mA is measured. It leads to a I_{od} of (17 - 6.25) mA = 10.75 mA and a pulse duration t_{pulse} of 50 ns. This value is on the upper right side of the graph and the bit will be correctly detected. The iso UART propagation delay increases the closer the overdrive current I_{od} is to the pulse detection curve (figure Overdrive current). Therefore, the max. $t_{isoU\_prop\_del}$ for the smallest Iod is shown in figure iso UART propagation delay t_isoU_prop_del_max.
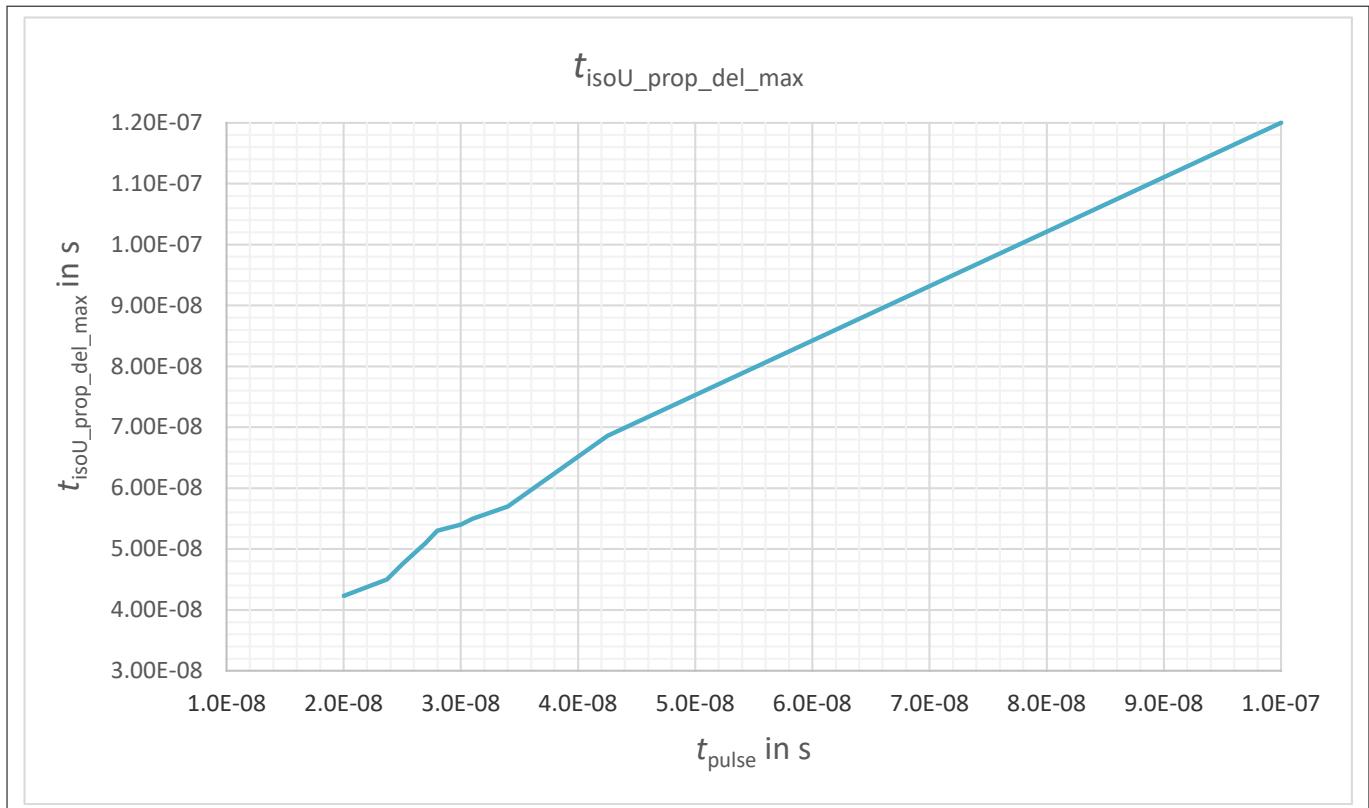
Figure 48   **iso UART propagation delay $t_{isoU\_prop\_del\_max}$**

Figure iso UART current probe measurement - CEP99P (2x510R) and figure iso UART current probe measurement - HM2116ANL (2x510R, without C_isoUART_F) show the current waveform of the iso UART communication with two different transformers (Sumida CEP99P, Pulse HM2116ANL) and R_N/R_N set to 510 Ω (2 × 510 Ω damping resistor).

2 Hardware guideline
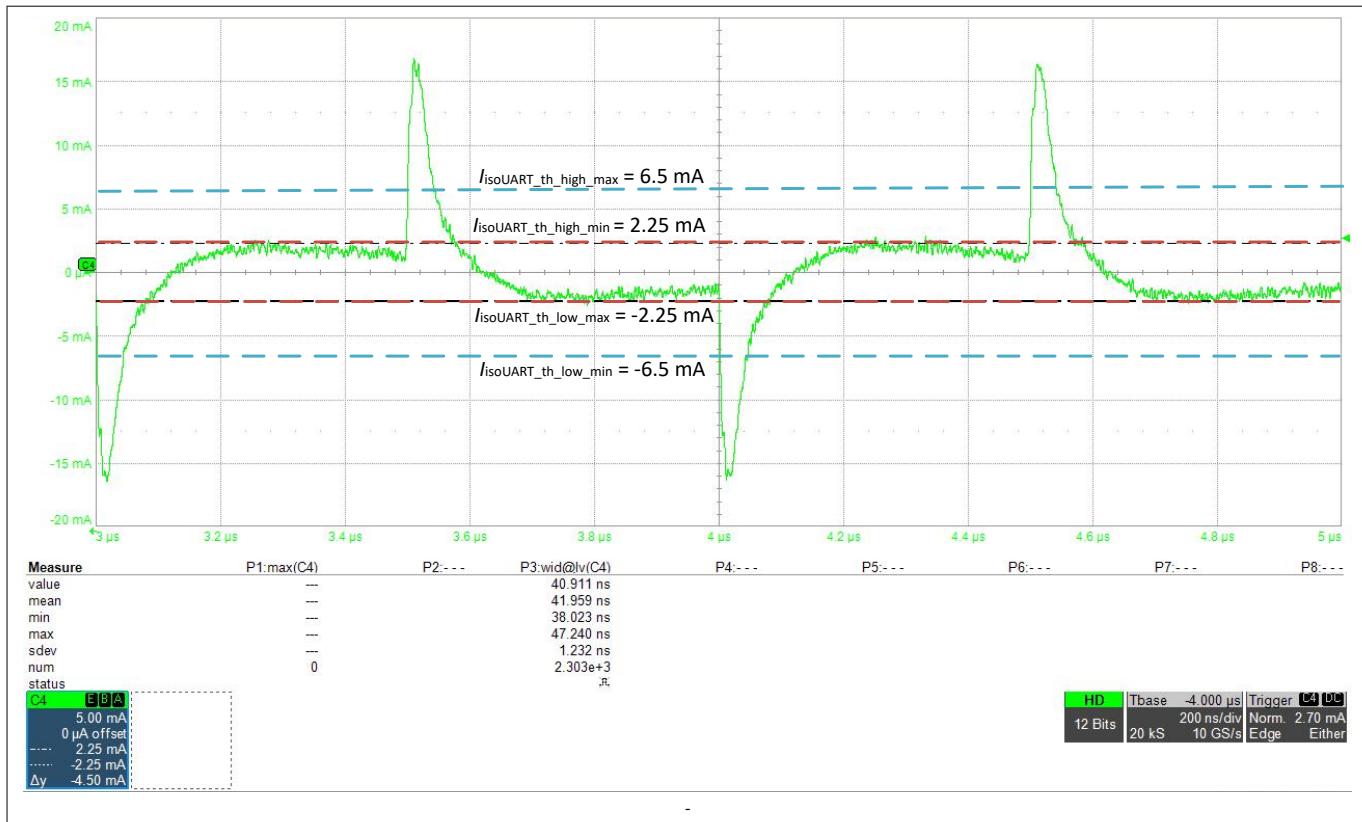
Figure 49   iso UART current probe measurement - CEP99P (2 × 510 Ω)
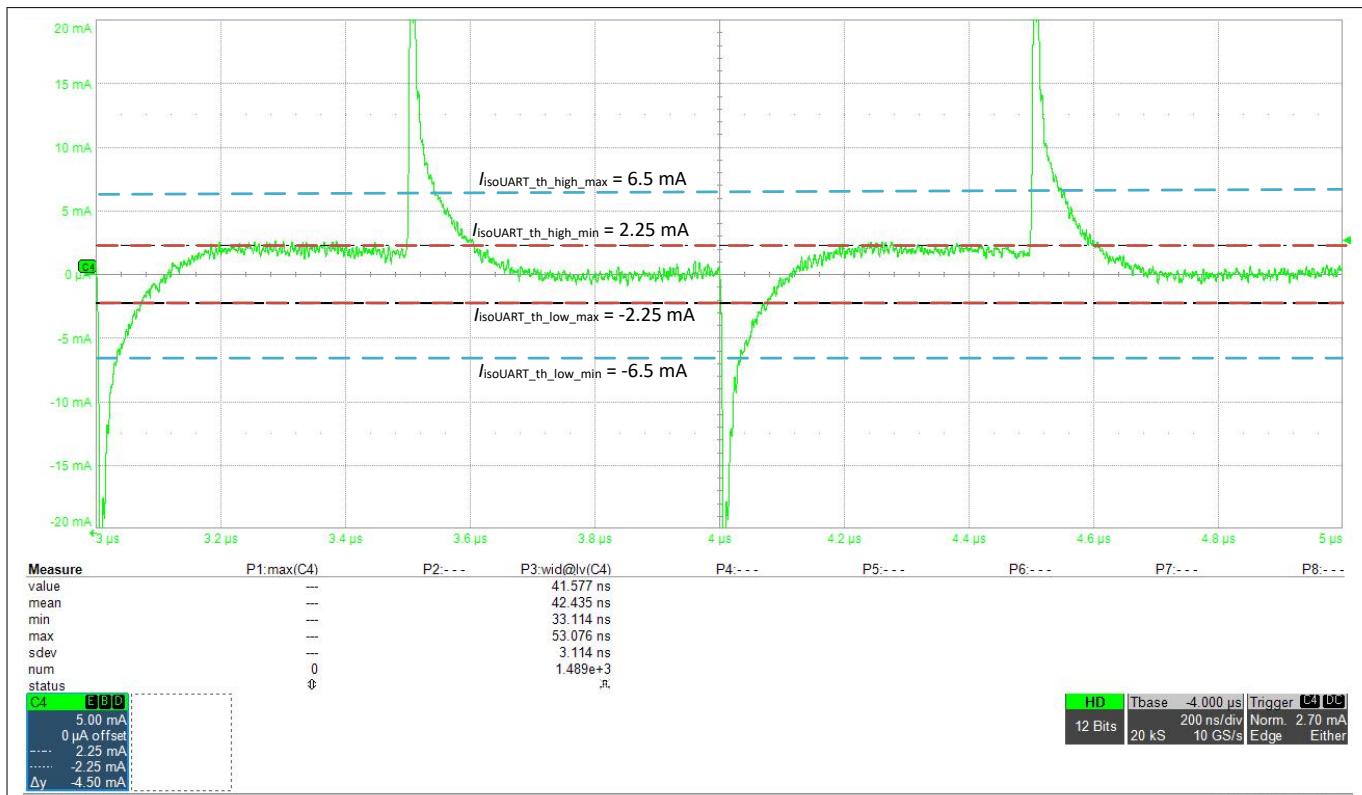
Figure 50   iso UART current probe measurement - HM2116ANL (2 × 510 Ω, without $C_{\text{isoUART\_F}}$)

The waveform in figure Transformer CEP99P with 2x510R damping resistor for the transformer CEP99P from Sumida with 2 × 510 Ω damping resistor shows the reference waveform which has been tested with corner samples.
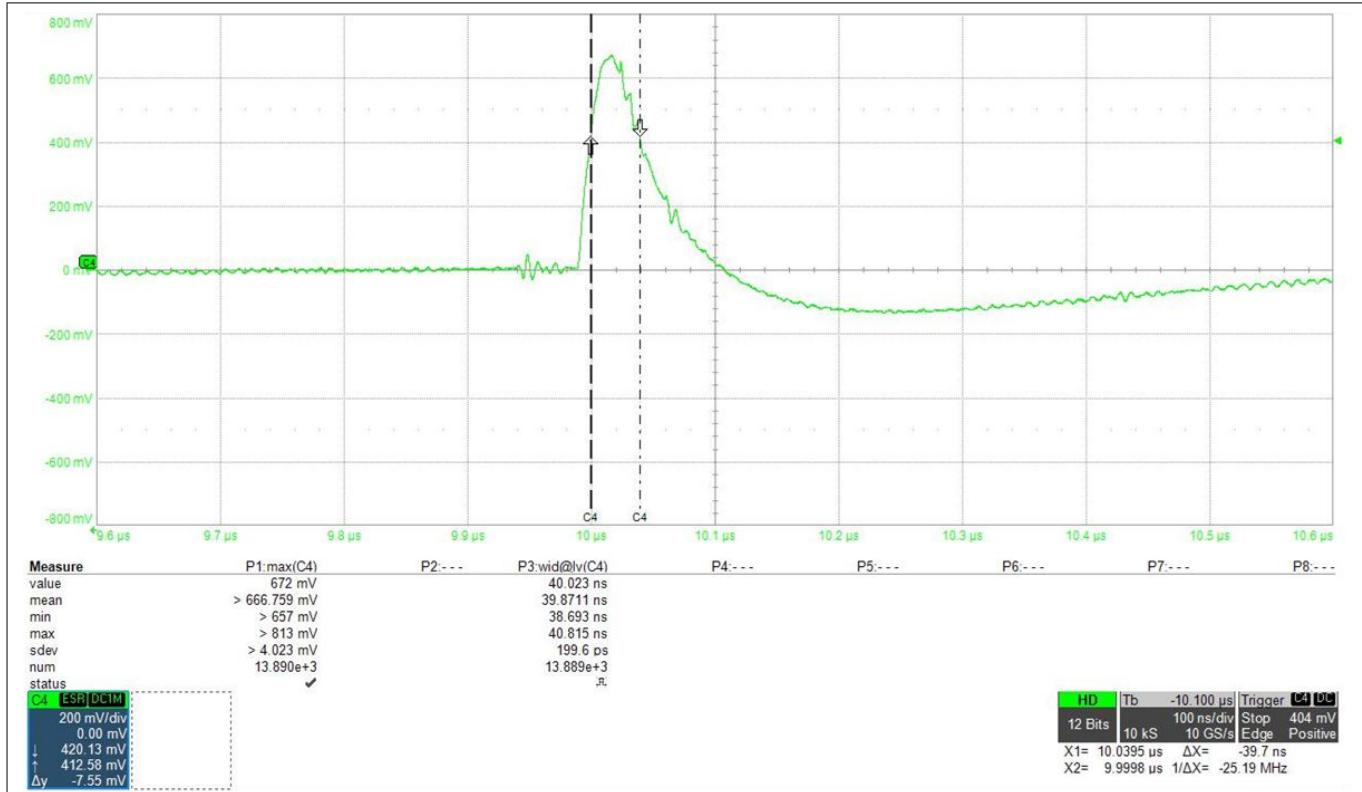
Figure 51   **Transformer CEP99P with 2 × 510 Ω damping resistor**

Figure Transformer HM2116ANL with 2x510R damping resistor, without C_isoUART_F shows the positive pulse with a Pulse HM2116ANL transformer with 2 × 510 Ω. As a guideline, a pulse duration of 40 ns over the temperature range of the application is recommended.
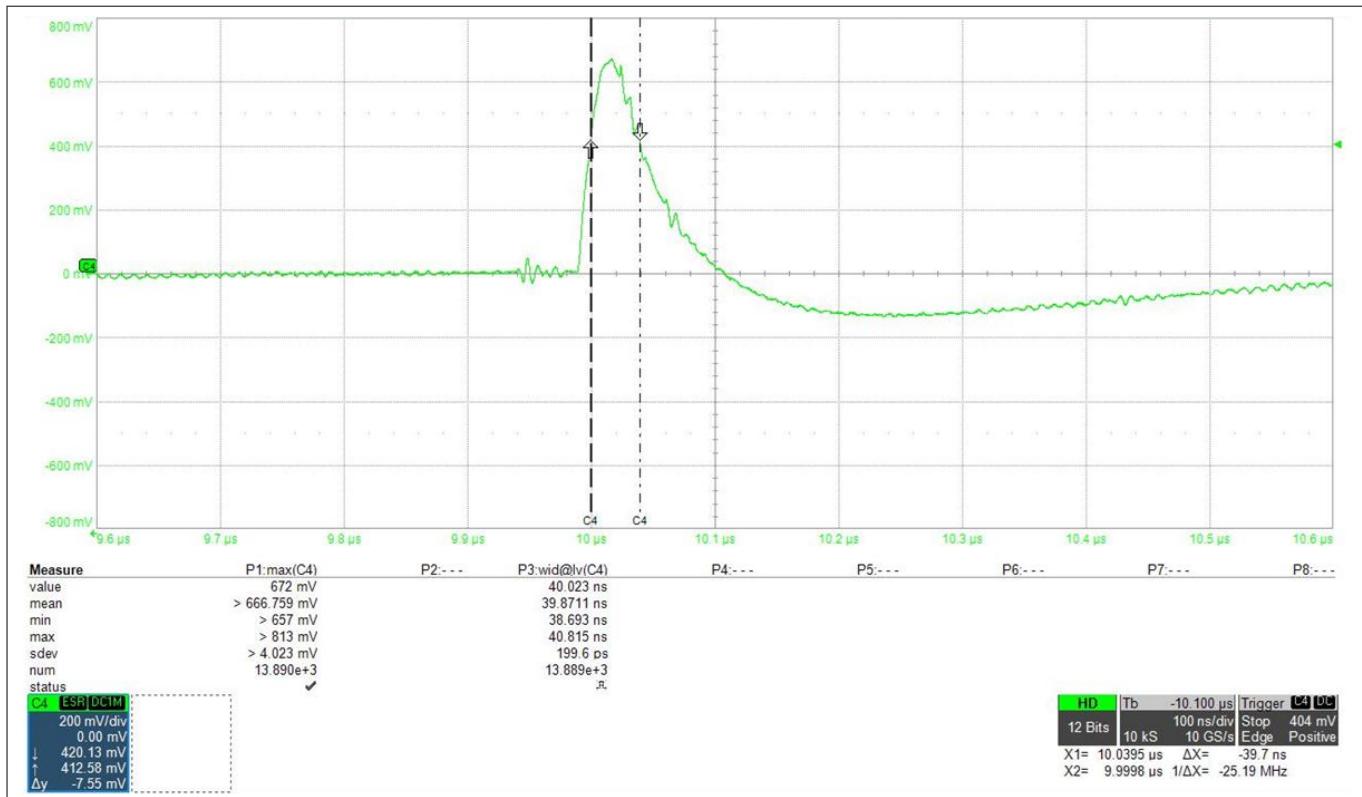
Figure 52   **Transformer HM2116ANL with 2 × 510 Ω damping resistor, without $C_{isoUART\_F}$**

Figure Transformer iso UART waveforms comparison shows the iso UART waveform measurement at point B from two different transformer evaluations. The yellow waveform shows the waveform from Pulse HM2116ANL (without $C_{isoUART\_F}$) while the green waveform shows the transformer from Sumida CEP99P. Both transformers have 2 × 510 Ω damping resistor mounted.
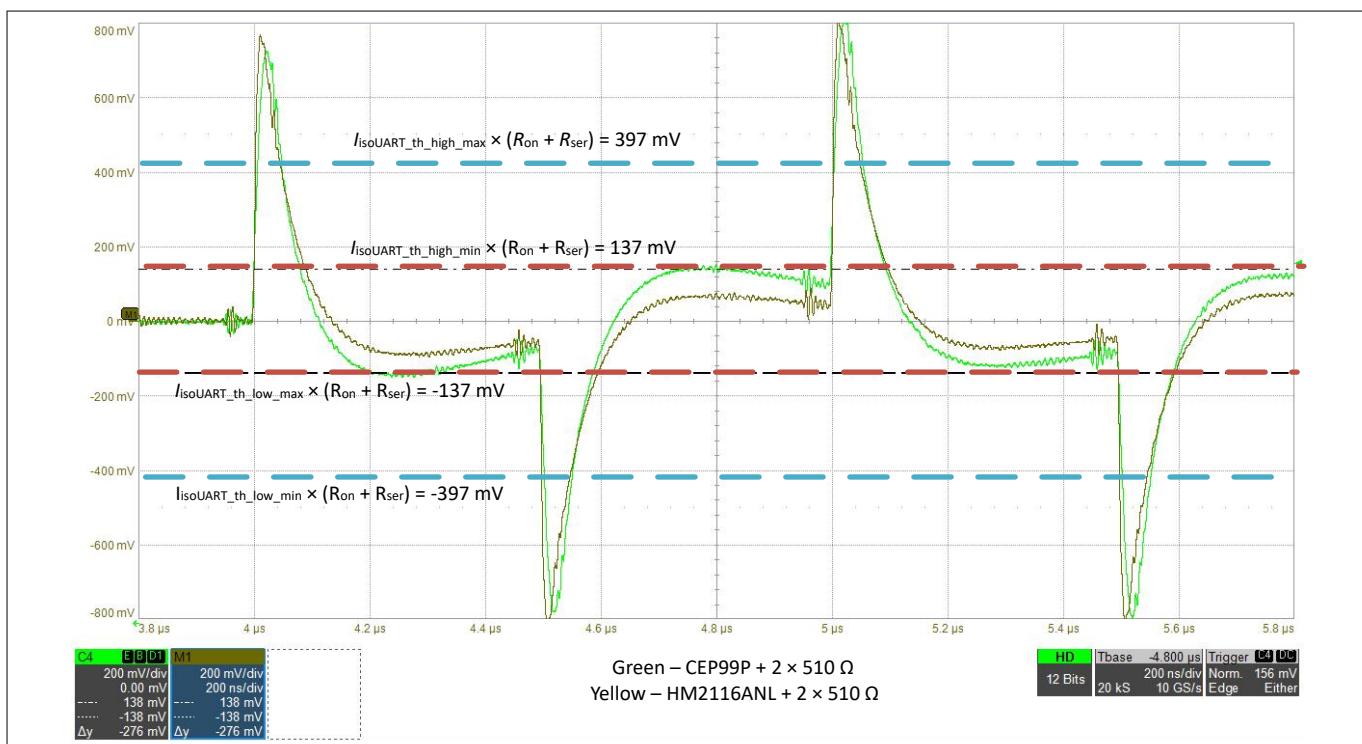
Figure 53   **Transformer iso UART waveforms comparison**

3 Software guideline

3.1 Initialization

In order to be able to communicate with the sensing ICs in the daisy chain, a CONFIG.NODE_ID (36_H) must be assigned. Before the initialization, the NODE_ID of all sensing ICs in the chain is ID = 00_H. If the NODE_ID = 00_H, no iso UART frames are forwarded to the next sensing IC in the chain. The following frame sequence shows an example initialization of four sensing ICs in a chain. The daisy chain is connected to the low-side iso UART interface of the transceiver (see Primary-on-Top application (wake-up via low-side interface)).

Table 7   **Initialize first IC with NODE_ID = 01_H**

Frame-type	Value	Comment
Synchronization	$1E_H$	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	80_H	MSB = 1 indicates a write command; 6-bit device ID = 000000_B.
Address	36_H	Address of CONFIG register.
Data	0001_H	Assigns NODE_ID = 01_H to the first sensing IC in the chain.
CRC	ED_H	CRC-code is based on 8-bit polynomial shown in CRC.

From this point onwards, the sensing IC closest to the transceiver IC has the NODE_ID = 01_H and forwards the messages. Now the next sensing IC in the chain will respond to commands addressed to NODE_ID = 00_H and the aforementioned process must be repeated (see below). *Note: The watchdog for NODE_ID = 01_H must be served if the initialization process takes longer than the predefined watchdog timer (WDOG_CNT.WD_CNT). Otherwise, the sensing IC will go to sleep mode and resets the NODE_ID to 00_H.*

Table 8   **Initialize second IC with NODE_ID = 02_H**

Frame-type	Value	Comment
Synchronization	$1E_H$	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	80_H	MSB = 1 indicates a write command; 6-bit device ID = 000000_B.
Address	36_H	Address of CONFIG register.
Data	0002_H	Assigns NODE_ID = 02_H to the second sensing IC in the chain.
CRC	CA_H	CRC-code is based on 8-bit polynomial shown in CRC.

From this point onwards, the second sensing IC has NODE_ID = 02_H, therefore the same applies as above for IC #1.

Table 9   **Initialize third IC with NODE_ID = 03_H**

Frame-type	Value	Comment
Synchronization	$1E_H$	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	80_H	MSB = 1 indicates a write command; 6-bit device ID = 000000_B.
Address	36_H	Address of CONFIG register.
Data	0003_H	Assigns NODE_ID = 03_H to the third sensing IC in the chain.

(table continues...)

Table 9 **(continued) Initialize third IC with NODE_ID = 03$_H$**

Frame-type	Value	Comment
CRC	D7$_H$	CRC-code is based on 8-bit polynomial shown in CRC.

From this point onwards, the third sensing IC has NODE_ID = 03$_H$, therefore the same applies as above for IC #1.

Table 10 **Initialize fourth IC with NODE_ID = 04$_H$**

Frame-type	Value	Comment
Synchronization	1E$_H$	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	80$_H$	MSB = 1 indicates a write command; 6-bit device ID = 000000$_B$.
Address	36$_H$	Address of CONFIG register.
Data	0804$_H$	Final Node FN = 1$_H$, otherwise no reply frame is sent on broadcast command (iso UART time-out). NODE_ID = 04$_H$ assigned to the fourth sensing IC in the chain.
CRC	DE$_H$	CRC-code is based on 8-bit polynomial shown in CRC.

Note: The initialization process can easily be looped in a software process.
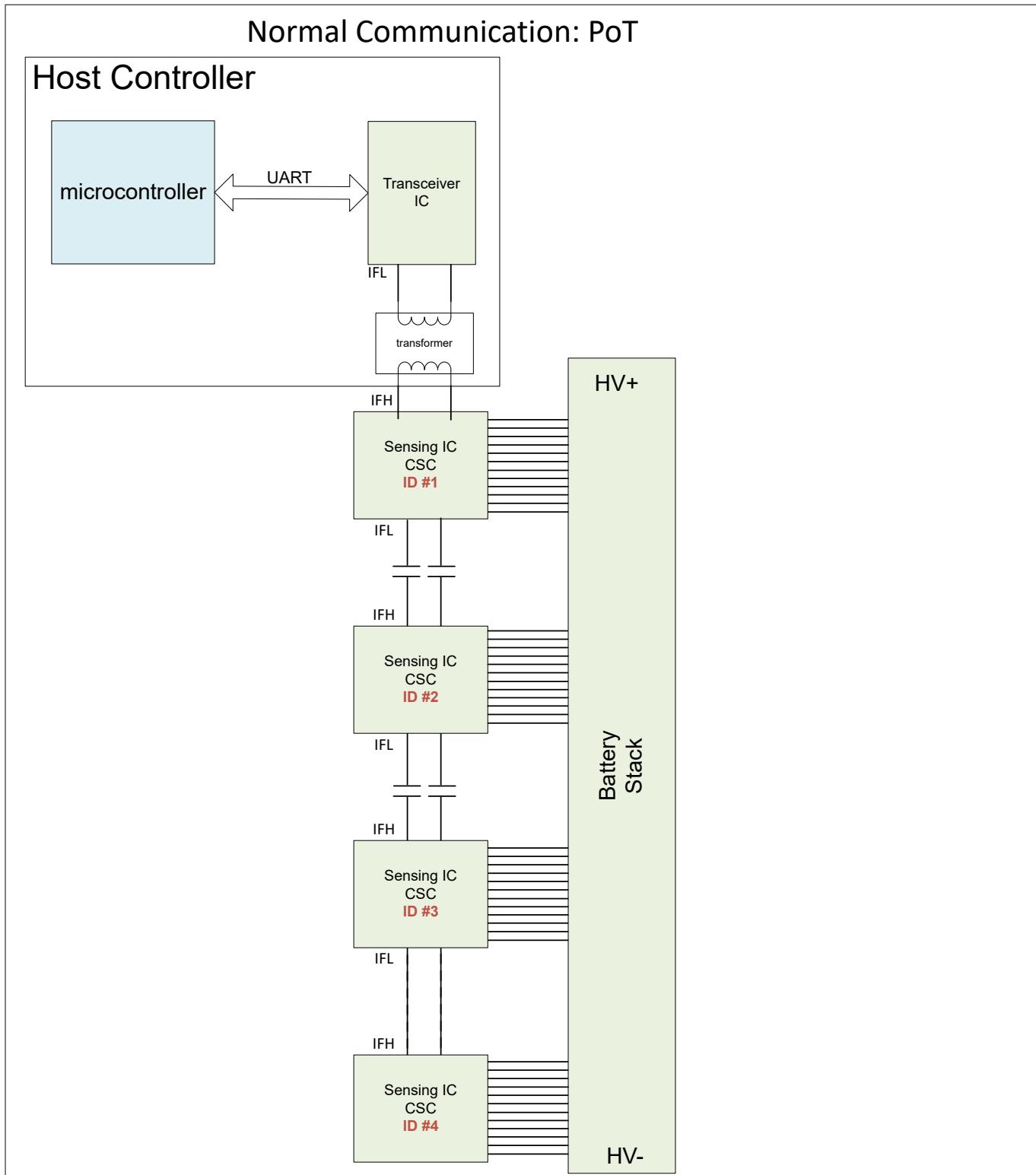
Figure 54   **Primary-on-Top application (wake-up via low-side interface)**

3.1.1   CRC

The CRC for the CRC frame is compliant to the SAE-J1850 standard and is calculated according to the following equation:

$G(z) = z^8 + z^4 + z^3 + z^2 + 1$ (initial value = FF_H; XOR value = FF_H)

3.1.2 Read back of configuration registers

The host controller should read back the register content after writing to a configuration register to check if the write command was successful. The following example shows the read back of the CONFIG 36_H register:

Table 11 **Read back CONFIG register of the first IC**

Frame-type	Value	Comment
Synchronization	$1E_H$	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	01_H	MSB = 0 indicates a read command; 6-bit device ID = 000001_B.
Address	36_H	Address of CONFIG register.
CRC	$A8_H$	CRC-code is based on 8-bit polynomial shown in CRC.

3.2 Configuration

3.2.1 Partitioning config

The PART_CONFIG 01_H register defines how many cells are connected to the sensing IC. This register determines which ADCs are activated during the primary cell voltage measurement (PCVM) and monitored during the round robin scheme. The following frame sequence activates all 12 PCVM channels for the sensing IC with the NODE_ID = 000001_B:

Table 12 **Write PART_CONFIG register for the first IC**

Frame-type	Value	Comment
Synchronization	$1E_H$	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	81_H	MSB = 1 indicates a write command; 6-bit device ID = 000001_B.
Address	01_H	Address of PART_CONFIG register.
Data	$0FFF_H$	Enables cell monitoring for all 12 cells.
CRC	$A8_H$	CRC-code is based on 8-bit polynomial shown in CRC.

Note: In general, this command can be sent as a broadcast write command if it should affect all IC's in the daisy chain. This applies for all other registers as well. An example for a broadcast write command is shown in Primary cell voltage measurement.

3.2.2 Cell voltage thresholds

The cell voltages checked via comparators and a digital-to-analog converter (DAC). The thresholds for the comparators are configured in the overvoltage OL_OV_THR 02_H and undervoltage OL_UV_THR 03_H registers. The following frame sequence configures an undervoltage threshold of e.g. 1.5 V and an overvoltage threshold of e.g. 4.6 V for the first sensing IC:

Table 13   **Overvoltage OL_OV_THR set to 4.6 V**

Frame-type	Value	Comment
Synchronization	$1E_H$	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	81_H	MSB = 1 indicates a write command; 6-bit device ID = 000001_B.
Address	02_H	Address of OL_OV_THR register.
Data	$FFAE_H$	Sets OL_OV_THR = $FFAE_H$ • Calculation OV_THR: 4.6 V / V_{OVUV_LSB} = $3AE_H$ • Default value for OL_THR_MAX used = $3F_H$
CRC	05_H	CRC-code is based on 8-bit polynomial shown in CRC.

Table 14   **Undervoltage OL_UV_THR set to 1.5 V**

Frame-type	Value	Comment
Synchronization	$1E_H$	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	81_H	MSB = 1 indicates a write command; 6-bit device ID = 000001_B.
Address	03_H	Address of OL_UV_THR register.
Data	0134_H	Sets OL_UV_THR = 0134_H • Calculation UV_THR: 1.5 V / V_{OVUV_LSB} = 134_H • Default value for OL_THR_MIN used = 00_H
CRC	BE_H	CRC-code is based on 8-bit polynomial shown in CRC.

3.2.3 Open load diagnostics

The open load diagnostics offers the possibility to automatically detect open wires on Un and Gn pins. Therefore, the open load thresholds needs to be set to define the minimum and maximum voltage drop while open load diagnostics. The configuration of the thresholds depends on the used filter resistor R_F. With the recommended filter resistor of 10 Ω and I_{OL_DIAG} (with $I_{OL\_DIAG\_min}$, $I_{OL\_DIAG\_max}$), the minimum voltage drop is 0.1 V (= 10 Ω × $I_{OL\_DIAG\_min}$) and the maximum voltage drop is 0.183 V (= 10 Ω × $I_{OL\_DIAG\_max}$) (disregarding the variation of the filter resistor). To prevent false triggering of the OL error (due to noise), an additional buffer can be added e.g. 40 mV. The following frame sequences sets the OL_OV_THR.OL_THR_MAX = 0.223 V and the OL_UV_THR.OL_THR_MIN = 0.06 V for the first sensing IC:

Table 15   **Open load maximum voltage drop threshold OL_THR_MAX = 0.223 V**

Frame-type	Value	Comment
Synchronization	$1E_H$	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	81_H	MSB = 1 indicates a write command; 6-bit device ID = 000001_B.
Address	02_H	Address of OL_OV_THR register.

(table continues...)

Table 15 **(continued) Open load maximum voltage drop threshold OL_THR_MAX = 0.223 V**

Frame-type	Value	Comment
Data	$2FFF_H$	Sets OL_OV_THR = $2FFF_H$ • Calculation OL_THR_MAX: 0.223 V / OL_{thr_LSB} = B_H • Default value for OV_THR used = $3FF_H$
CRC	51_H	CRC-code is based on 8-bit polynomial shown in CRC.

Table 16 **Open load minimum voltage drop threshold OL_THR_MIN = 0.06 V**

Frame-type	Value	Comment
Synchronization	$1E_H$	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	81_H	MSB = 1 indicates a write command; 6-bit device ID = 000001_B.
Address	03_H	Address of OL_UV_THR register.
Data	$0C00_H$	Sets OL_UV_THR = $0C00_H$ • Calculation OL_THR_MIN: 0.06 V / OL_{thr_LSB} = 3_H • Default value for UV_THR used = 000_H
CRC	BB_H	CRC-code is based on 8-bit polynomial shown in CRC.

3.2.4 NTC temperature measurement configuration

The sensing IC can measure up to 5 external temperature sensors. As part of the round robin (RR) scheme, up to two temperature measurements can be performed in every RR cycle. The number of external temperature sensors is configured in the TEMP_CONF 04_H register. As an example, all temperature channels are activated for sensing IC 1:

Table 17 **Number of external temperature sensors NR_TEMP_SENSE**

Frame-type	Value	Comment
Synchronization	$1E_H$	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	81_H	MSB = 1 indicates a write command; 6-bit device ID = 000001_B.
Address	04_H	Address of TEMP_CONF register.
Data	5000_H	Sets TEMP_CONF.NR_TEMP_SENSE = 101_B; default values for I_NTC and EXT_OT_THR used.
CRC	18_H	CRC-code is based on 8-bit polynomial shown in CRC.

3.2.5 Balancing current thresholds

A balancing overcurrent OC_THR or undercurrent UC_THR check is performed during the round robin cycle. If the balancing current is lower than the UC_THR or higher than the OC_THR, the corresponding error counter will be incremented. The example shows a threshold configuration for sensing IC 1 with a maximum balancing current I_{BAL_max} = 4.3 V / (R_F + R_{BAL} + $R_{BAL\_on\_min}$) Ω = 83 mA at 4.3V and a minimum balancing current I_{BAL_min} = 2.7 V / (R_F + R_{BAL} + $R_{BAL\_on\_max}$) Ω = 48 mA at 2.7 V (disregarding the variation of the external components). A filter resistor R_F of 10 Ω and a balancing resistor of 41 Ω is assumed and the balancing switch on-state resistance R_{BAL_on} is considered. A voltage of ±100mV is used as voltage drop ($I_{BAL} \times R_F$) buffer, the balancing

current voltage drop must be within minimum ($I_{BAL\_min} \times R_F$ - 0.1 V) = 0.38 V and maximum ($I_{BAL\_max} \times R_F$ + 0.1 V) = 0.93 V.

Table 18   **Balancing current thresholds BAL_CURR_THR 15$_H$**

Frame-type	Value	Comment
Synchronization	1E$_H$	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	81$_H$	MSB = 1 indicates a write command; 6-bit device ID = 000001$_B$.
Address	15$_H$	Address of BAL_CURR_THR register.
Data	1330$_H$	Set BAL_CURR_THR = 1330$_H$ • Calculation UC_THR: 0.38 V / CD_{thr_LSB} = 13$_H$ • Calculation OC_THR: 0.93 V / CD_{thr_LSB} = 30$_H$
CRC	FB$_H$	CRC-code is based on 8-bit polynomial shown in CRC.

3.3   Cell voltage measurement

3.3.1   Primary cell voltage measurement

To initiate a primary cell voltage measurement of the connected cells, the bit-field MEAS_CTRL.PCVM_START needs to be set. The measurement starts after the configurable delay time t_{VM_del}. The delay time allows the external filter to settle to e.g. avoid errors due to prior balancing. t_{VM_del} is active independent of the balancing status. After the measurement, the PCVM_START bit-field is automatically cleared and the result is available in the PCVM_0 - PCVM_11 result registers. The PCVM_0 - PCVM_11 registers will be cleared during the measurement until the measurement is finished. To avoid measurement errors due to passive balancing current, the PBOFF bit-field is by default 1$_B$ to automatically deactivate the passive balancing switches during the cell voltage measurement. The following example shows the initiation of the cell voltage measurement with 16-bit for sensing IC 1:

Table 19   **Measurement control MEAS_CTRL 18$_H$**

Frame-type	Value	Comment
Synchronization	1E$_H$	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	81$_H$	MSB = 1 indicates a write command; 6-bit device ID = 000001$_B$.
Address	18$_H$	Address of MEAS_CTRL register.
Data	E021$_H$	Sets MEAS_CTRL = E021$_H$ • PCVM_START = 1$_B$ • CVM_MODE = 110$_B$ (16-bit) • Default for BVM_START, BVM_MODE, AVM_START, SCVM_START, PBOFF, CVM_DEL
CRC	98$_H$	CRC-code is based on 8-bit polynomial shown in CRC.

A broadcast write command can be used to start the measurement for all ICs in the chain with a single command at the same time. The following example starts the voltage measurements for IC #1 to IC #4 (see Primary-on-Top application (wake-up via low-side interface)):

Table 20 **Broadcast write to measurement control MEAS_CTRL 18$_H$**

Frame-type	Value	Comment
Synchronization	1E$_H$	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	BF$_H$	MSB = 1 indicates a write command; 6-bit device ID = 111111$_B$ indicates a broadcast command.
Address	18$_H$	Address of MEAS_CTRL register.
Data	E021$_H$	Sets MEAS_CTRL = E021$_H$ • PCVM_START = 1$_B$ • CVM_MODE = 110$_B$ (16-bit) • Default for BVM_START, BVM_MODE, AVM_START, SCVM_START, PBOFF, CVM_DEL
CRC	02$_H$	CRC-code is based on 8-bit polynomial shown in CRC.

3.3.2 Block voltage measurement

The 13th ADC can perform different auxiliary voltage measurements including a block voltage measurement (BVM). The voltage is measured between U12P and GND. A BVM measurement is initiated by setting the bit-field MEAS_CTRL.BVM_START and starts after t_{VM_prop}. The measurement result is stored in the BVM 28$_H$ register and the BVM_START bit is automatically cleared after the measurement. The following example shows the initiation of the block voltage measurement with 16-bit for sensing IC 1:

Table 21 **Measurement control MEAS_CTRL 18$_H$**

Frame-type	Value	Comment
Synchronization	1E$_H$	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	81$_H$	MSB = 1 indicates a write command; 6-bit device ID = 000001$_B$.
Address	18$_H$	Address of MEAS_CTRL register.
Data	0E21$_H$	Sets MEAS_CTRL = 0E21$_H$ • BVM_START = 1$_B$ • BVM_MODE = 110$_B$ (16-bit) • Default for PCVM_START, PCVM_MODE, AVM_START, SCVM_START, PBOFF, CVM_DEL
CRC	21$_H$	CRC-code is based on 8-bit polynomial shown in CRC.

3.3.3 Bipolar auxiliary voltage measurement

Additionally, the device can be configured to measure a bipolar voltage. The voltage is measured between TMP4 and TMP3. A BAVM measurement is enabled by setting the AVM_CONFIG.AUX_BIPOLAR bitfield.

Table 22   Auxiliary voltage measurement configuration AVM_CONFIG 17_H

Frame-type	Value	Comment
Synchronization	$1E_H$	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	81_H	MSB = 1 indicates a write command; 6-bit device ID = 000001_B.
Address	17_H	Address of AVM_CONFIG register.
Data	0107_H	Sets AVM_CONFIG = 0107_H • AUX_BIPOLAR = 1_B • Default for TEMP_MUX_DIAG_SEL, AVM_TMPx_MASK, R_DIAG, R_DIAG_SEL_0, R_DIAG_SEL_1, R_DIAG_CUR_SRC
CRC	85_H	CRC-code is based on 8-bit polynomial shown in CRC.

The resolution is set by the MEAS_CTRL.BVM_MODE bitfield and the measurement is triggered by the MEAS_CTRL.BVM_START bitfield after t_{VM_prop}. The following example shows the initiation of the bipolar auxiliary voltage measurement with 16-bit for sensing IC 1:

Table 23   Measurement control MEAS_CTRL 18_H

Frame-type	Value	Comment
Synchronization	$1E_H$	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	81_H	MSB = 1 indicates a write command; 6-bit device ID = 000001_B.
Address	18_H	Address of MEAS_CTRL register.
Data	$0E21_H$	Sets MEAS_CTRL = $0E21_H$ • BVM_START = 1_B • BVM_MODE = 110_B (16-bit) • Default for PCVM_START, PCVM_MODE, AVM_START, SCVM_START, PBOFF, CVM_DEL
CRC	21_H	CRC-code is based on 8-bit polynomial shown in CRC.

The measurement result is stored in the BVM 28_H register and the BVM_START bit is automatically cleared after the measurement.

3.4   Calculations

3.4.1   Voltage, PCVM, SCVM, BVM

After a primary cell voltage measure command (PCVM), an unsigned value is stored in the RESULT bit-fields of the PCVM_0 - PCVM_11 (Offset Address: 19_H - 24_H) registers. The equation to calculate the cell voltage is:

V_{PCVM} [V] = (FSR_{PCVM} / 2^{16}) × RESULT[LSB16]

e.g. PCVM_0 = $ABCD_H$

V_{PCVM} [V] = (5 V / 2^{16}) × $ABCD_H$ = 3.355 V

Using the PCVM formula, a voltage of 3.355 V for cell 0 (PCVM_0) is calculated.

To calculate the block voltage after a block voltage measurement (BVM), a similar formula is used. The RESULT stored in the BVM register (Offset Address: 28_H) is converted to a voltage with BVM formula.

V_{BVM} [V] = (FSR_{BVM} / 2^{16}) × RESULT_BVM [LSB16]

e.g. BVM = $ABCD_H$

V_{BVM} [V] = (60 V / 2^{16}) × $ABCD_H$ = 40.266 V

Using the formula BVM formula, a voltage of 40.266 V for the block voltage is calculated.

To calculate the secondary cell voltage after a secondary cell voltage measurement (SCVM), a similar formula is used. The RESULT stored in the SCVM_HIGH and SCVM_LOW registers (Offset Address: 25_H, 26_H) is converted to a voltage with SCVM formula.

V_{SCVM} [V] = (FSR_{SCVM} / 2^{11}) × RESULT [LSB11]

e.g. SCVM_HIGH = $ABE0_H$

V_{SCVM} [V] = (5 V / 2^{11}) × 1010101111_B = 1.677 V

Using the SCVM formula, a voltage of 1.677 V for the secondary cell voltage SCVM_HIGH is calculated.

To calculate the bipolar auxiliary voltage after a bipolar auxiliary voltage measurement (BAVM), a similar formula is used. The RESULT stored in the BVM register (Offset Address: 28_H) is converted to a voltage with BAVM formula.

V_{BAVM} [V] = (BVM.RESULT [signed LSB15] × 2 V) / 2^{15}[LSB15]

e.g. BVM = 6000_H

V_{BAVM} [V] = (6000_H × 2 V) / 2^{15} = 1.5 V

Using the BAVM formula a voltage of 1.5 V for V_{BAVM} is calculated.

Please note: For BVM_MODE smaller than 16-bit mode, the host controller can set the LSBs of the BVM register value to 0_B for positive results (MSB = 0_B) and 1_B for negative results (MSB = 1_B).

3.4.2 Temperature measurement unit

The results of the NTC resistance measurement are stored in the EXT_TEMP_0 - EXT_TEMP_4 (29_H - $2D_H$) registers. The NTC resistor value is calculated with the following TMP formula:

R_{NTC} [Ω] = EXT_TEMP_z.RESULT [LSB10] × FSR_{TMP} [V] × $4^{EXT\_TEMP\_z.INTC}$) / (2^{10} × 320 µA) - R_{TMP}; INTC = 0 to 3 (used current source).

e.g. EXT_TEMP_0 = 2747_H (RESULT[LSB10] = 347_H; INTC=1_H), R_{TMP} = 100 Ω

R_{NTC} [Ω] = (347_H * 2 V * 4^1) / (2^{10} * 320 µA) - 100 Ω = 20.4 kΩ

3.5 Balancing

Passive balancing can be activated to equalize the voltage levels of the connected battery cells. In the configuration register BAL_SETTINGS 16_H, the cells to be balanced can be selected in any combination including for all channels at the same time. To automatically switch off balancing during a cell voltage measurement and to delay the cell voltage measurement after balancing, see Cell voltage measurement. To select all 12 cell for the first sensing IC in the chain, the following sequence must be send:

Table 24   Write register BAL_SETTINGS 16_H

Frame-type	Value	Comment
Synchronization	$1E_H$	Fixed synchronization frame; necessary to start the communication with a defined scheme.

(table continues…)

Table 24 **(continued) Write register BAL_SETTINGS 16$_H$**

Frame-type	Value	Comment
ID	81$_H$	MSB = 1 indicates a write command; 6-bit device ID = 000001$_B$.
Address	16$_H$	Address of BAL_SETTINGS register.
Data	0FFF$_H$	Sets BAL_SETINGS = 0FFF$_H$ to switch on the balancing drivers for cell 0 to 11.
CRC	3A$_H$	CRC-code is based on 8-bit polynomial shown in CRC.

3.6 Sleep mode and register reset

3.6.1 Sleep mode

The IC can be send into sleep mode by setting the sleep mode bit PD in the OP_MODE register. The registers that are supplied in sleep mode are not reset.

Table 25 **Write register OP_MODE 14$_H$**

Frame-type	Value	Comment
Synchronization	1E$_H$	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	81$_H$	MSB = 1 indicates a write command; 6-bit device ID = 000001$_B$.
Address	14$_H$	Address of OP_MODE register.
Data	C401$_H$	Sets PD = 1$_H$ activate sleep mode (using default values for the remaining bitfields).
CRC	4D$_H$	CRC-code is based on 8-bit polynomial shown in CRC.

3.6.2 Sleep mode registers reset

The bit SLEEP_REG_RESET in the OP_MODE register resets all registers (including registers that are supplied in sleep mode) and activates sleep mode.

Table 26 **Write register OP_MODE 14$_H$**

Frame-type	Value	Comment
Synchronization	1E$_H$	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	81$_H$	MSB = 1 indicates a write command; 6-bit device ID = 000001$_B$.
Address	14$_H$	Address of OP_MODE register.
Data	C404$_H$	Sets SLEEP_REG_RESET = 1$_H$ resets all registers and activates sleep mode (using default values for the remaining bitfields).
CRC	24$_H$	CRC-code is based on 8-bit polynomial shown in CRC.

To reset the sleep mode register for all devices in the daisy chain, the following command sequence must be sent:

1. Set SLEEP_REG_RESET bit in the OP_MODE register for the IC with the highest node ID

2. After 4 ms, check whether the highest NODE_ID has performed the reset and is in sleep mode. To do this, send a read command to this node ID. This wake up the device.

3. The highest node is now configured as NODE_ID = 0 (default) and must therefore be configured with the correct NODE_ID.

4. Repeat the process with the second highest NODE_ID, etc.

Note: The PS_ERR_SLEEP bit in the GEN_DIAG register might be set after a sleep mode register reset. The bit must be manually set to 0_H.

4 Registers

4.1 Registers overview

This chapter gives an overview of the registers of the TLE9012DQU. Empty register bitfields or bitfields labeled "RES" (reserved for future use) are as the name indicates reserved for potential future use. When writing into a register, the "RES" part of the register must always be written with "0". The same applies for read-only bitfields.

When reading, the contents of the "RES" fields should be masked out since the value is not defined.

• r = read access

• w = write access

• wo = write access only one time

• h = the IC hardware can change the contents of the field

• rocw = read-only, clear bit by writing a "0" to the respective bit position

• rocwl = read-only, clear bit by writing a "0", linked register is reset to default state

• rocr = read-only, clearing bit by reading

4.2 Registers overview - REG (ascending offset address)

Table 27   Registers overview - REG (ascending offset address)

Short name	Long name	Offset address	Access mode		Reset	Page number
			Read	Write		
PART_CONFIG	Partitioning config (supplied in sleep)	0001_H	U	U	Reset	64
OL_OV_THR	Cell voltage thresholds (supplied in sleep)	0002_H	U	U	Reset	65
OL_UV_THR	Cell voltage thresholds (supplied in sleep)	0003_H	U	U	Reset	66
TEMP_CONF	Temperature measurement configuration (supplied in sleep)	0004_H	U	U	Reset	67
INT_OT_WARN_CONF	Internal temperature measurement configuration (supplied in sleep)	0005_H	U	U	Reset	68
RR_ERR_CNT	Round robin ERR counters (supplied in sleep)	0008_H	U	U	Reset	69
RR_CONFIG	Round robin configuration (supplied in sleep)	0009_H	U	U	Reset	70
FAULT_MASK	ERR pin / EMM mask (supplied in sleep)	$000A_H$	U	U	Reset	72
GEN_DIAG	General diagnostics (supplied in sleep)	$000B_H$	U	U	Reset	74
CELL_UV	Cell voltage supervision warning flags UV (supplied in sleep)	$000C_H$	U	U	Reset	77

(table continues…)

Table 27 **(continued) Registers overview - REG (ascending offset address)**

Short name	Long name	Offset address	Access mode		Reset	Page number
			Read	Write		
CELL_OV	Cell voltage supervision warning flags OV (supplied in sleep)	000D$_H$	U	U	Reset	78
EXT_TEMP_DIAG	External overtemperature warning flags (supplied in sleep)	000E$_H$	U	U	Reset	79
DIAG_OL	Diagnostics open load (supplied in sleep)	0010$_H$	U	U	Reset	81
REG_CRC_ERR	REG_CRC_ERR (supplied in sleep)	0011$_H$	U	U	Reset	82
CELL_UV_DAC_C OMP	Cell voltage supervision warning flags UV (supplied in sleep)	0012$_H$	U	U	Reset	83
CELL_OV_DAC_C OMP	Cell voltage supervision warning flags OV (supplied in sleep)	0013$_H$	U	U	Reset	84
OP_MODE	Operation mode	0014$_H$	U	U	Reset	85
BAL_CURR_THR	Balancing current thresholds	0015$_H$	U	U	Reset	86
BAL_SETTINGS	Balance settings	0016$_H$	U	U	Reset	87
AVM_CONFIG	Auxiliary voltage measurement configuration	0017$_H$	U	U	Reset	88
MEAS_CTRL	Measurement control	0018$_H$	U	U	Reset	90
PCVM_i	Primary cell voltage measurement i	0019$_H$+i	U	nBE	Reset	92
SCVM_HIGH	SCVM highest cell voltage	0025$_H$	U	nBE	Reset	93
SCVM_LOW	SCVM lowest cell voltage	0026$_H$	U	nBE	Reset	94
STRESS_PCVM	Stress correction PCVM	0027$_H$	U	nBE	Reset	95
BVM	Block voltage measurement	0028$_H$	U	nBE	Reset	96
EXT_TEMP_0	Temp result 0	0029$_H$	U	U	Reset	97
EXT_TEMP_1	Temp result 1	002A$_H$	U	U	Reset	98
EXT_TEMP_2	Temp result 2	002B$_H$	U	U	Reset	99
EXT_TEMP_3	Temp result 3	002C$_H$	U	U	Reset	100
EXT_TEMP_4	Temp result 4	002D$_H$	U	U	Reset	101
EXT_TEMP_R_DI AG	Temp result R diagnose	002F$_H$	U	nBE	Reset	102
INT_TEMP	Chip temperature	0030$_H$	U	nBE	Reset	103
MULTI_READ	Multiread command	0031$_H$	U	nBE	Reset	104
MULTI_READ_CF G	Multiread configuration	0032$_H$	U	U	Reset	105

(table continues...)

Table 27 **(continued) Registers overview - REG (ascending offset address)**

Short name	Long name	Offset address	Access mode		Reset	Page number
			Read	Write		
BAL_DIAG_OC	Passive balancing diagnostics OVERCURRENT	0033_H	U	U	Reset	106
BAL_DIAG_UC	Passive balancing diagnostics UNDERCURRENT	0034_H	U	U	Reset	107
INT_TEMP_2	Chip temperature 2	0035_H	U	nBE	Reset	108
CONFIG	Configuration	0036_H	U	U	Reset	109
GPIO	General purpose input / output	0037_H	U	U	Reset	110
GPIO_PWM	PWM settings	0038_H	U	U	Reset	112
ICVID	IC version and manufacturing ID	0039_H	U	nBE	Reset	113
MAILBOX	Mailbox register	$003A_H$	U	U	Reset	114
CUSTOMER_ID_0	Customer ID 0	$003B_H$	U	nBE	Reset	115
CUSTOMER_ID_1	Customer ID 1	$003C_H$	U	nBE	Reset	116
WDOG_CNT	Watchdog counter	$003D_H$	U	U	Reset	117
SCVM_CONFIG	SCVM configuration	$003E_H$	U	U	Reset	118
STRESS_AUX	Stress correction AUX	$003F_H$	U	nBE	Reset	119
BAL_PWM	Balancing PWM	$005B_H$	U	U	Reset	120
BAL_CNT_0	Balancing counter register 0	$005C_H$	U	U	Reset	121
BAL_CNT_1	Balancing counter register 1	$005D_H$	U	U	Reset	122
BAL_CNT_2	Balancing counter register 2	$005E_H$	U	U	Reset	123
BAL_CNT_3	Balancing counter register 3	$005F_H$	U	U	Reset	124

4.3 Partitioning config (supplied in sleep)

PART_CONFIG

Partitioning config [supplied in sleep)

Offset address: 0001$_H$

Reset value: 0800$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				EN_C ELL1 1	EN_C ELL1 0	EN_C ELL9	EN_C ELL8	EN_C ELL7	EN_C ELL6	EN_C ELL5	EN_C ELL4	EN_C ELL3	EN_C ELL2	EN_C ELL1	EN_C ELL0
				rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
EN_CELLi (i=0-10)	i	rw	**Enable cell monitoring for cell i** 0$_B$ **NO_CELL_ATTACHED**: No cell attached (default) 1$_B$ **CELL_ATTACHED**: Cell attached
EN_CELL11	11	rw	**Enable cell monitoring for cell 11** 0$_B$ **NO_CELL_ATTACHED**: No cell attached 1$_B$ **CELL_ATTACHED**: Cell attached (default)

4.4 Cell voltage thresholds (supplied in sleep)

OL_OV_THR   Offset address: 0002$_H$

Cell voltage thresholds [supplied in sleep)   Reset value: FFFF$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		OL_THR_MAX								OV_THR					
		rw								rw					

Field	Bits	Type	Description
OV_THR	9:0	rw	**Overvoltage fault threshold**
			10-bit overvoltage fault threshold. Battery input voltages (U0 to U11) are tested for overvoltage with given value. OV error is detected and indicated in GEN_DIAG register if cell voltage is higher than OV fault threshold.
			3FF$_H$ **THRESHOLD**: Threshold (default)
OL_THR_MAX	15:10	rw	**Open load maximum voltage drop threshold (LSB8)**
			6-bit (LSB8) to define the maximum threshold for the voltage drop while OL-diagnostics ($I_{OL\_DIAG} * R_F$). If voltage drop > OL_THR_MAX, the OLx bit of channel x is set.
			3F$_H$ **THRESHOLD**: Threshold (default)

4.5 Cell voltage thresholds (supplied in sleep)

OL_UV_THR   Offset address: 0003$_H$

Cell voltage thresholds [supplied in sleep)   Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OL_THR_MIN						UV_THR									
rw						rw									

Field	Bits	Type	Description
UV_THR	9:0	rw	**Undervoltage fault threshold** 10-bit undervoltage fault threshold. Battery input voltages (U0 to U11) are tested for undervoltage with given value. UV error is detected and indicated in GEN_DIAG register if cell voltage is lower than UV fault threshold. 000$_H$ **THRESHOLD**: Threshold (default)
OL_THR_MIN	15:10	rw	**Open load minimum voltage drop threshold (LSB8)** 6-bit (LSB8) to define the minimum threshold for the voltage drop while OL-diagnostics ($I_{OL\_DIAG} * R_F$). If voltage drop < OL_THR_MIN, the OLx bit of channel x is set. 00$_H$ **THRESHOLD**: Threshold (default)

4.6   Temperature measurement configuration (supplied in sleep)

TEMP_CONF   Offset address: 0004$_H$

Temperature measurement configuration [supplied in   Reset value: 0000$_H$
sleep)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	NR_TEMP_SENSE			I_NTC		EXT_OT_THR									
r	rw			rw		rw									

Field	Bits	Type	Description
EXT_OT_THR	9:0	rw	**External overtemperature threshold** 10-bit overtemperature fault threshold. Overtemperature error is detected and indicated in GEN_DIAG register if the external temperature result is lower than the fault threshold. Balancing is deactivated. 000$_H$ **THRESHOLD**: Threshold (default)
I_NTC	11:10	rw	**Current source used for OT fault** 00$_B$ **I_0**: ITMPz_0 used (default) 01$_B$ **I_1**: ITMPz_1 used 10$_B$ **I_2**: ITMPz_2 used 11$_B$ **I_3**: ITMPz_3 used
NR_TEMP_SENSE	14:12	rw	**Number of external temperature sensors** 000$_B$ **NO_EXT_SENSOR**: No external TMP sensor (default) 001$_B$ **TMP0**: TMP0 active 010$_B$ **TMP0_1**: TMP0 + TMP1 active 011$_B$ **TMP0_2**: TMP0 + TMP1 + TMP2 active 100$_B$ **TMP0_3**: TMP0 + TMP1 + TMP2 + TMP3 active 101$_B$ **TMP0_4**: TMP0 + TMP1 +TMP2 + TMP3 + TMP4 active

4.7 Internal temperature measurement configuration (supplied in sleep)

INT_OT_WARN_CONF

Internal temperature measurement configuration
[supplied in sleep)

Offset address: 0005$_H$

Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res						INT_OT_THR									
r						rw									

Field	Bits	Type	Description
INT_OT_THR	9:0	rw	**Internal overtemperature threshold** 10-bit overtemperature fault threshold. Overtemperature error is detected and indicated in GEN_DIAG register if the internal temperature result is LOWER than the fault threshold. Balancing is deactivated. 000$_H$ **THRESHOLD**: Threshold (default)

4.8   Round robin ERR counters (supplied in sleep)

RR_ERR_CNT   Offset address: 0008$_H$

Round robin ERR counters [supplied in sleep)   Reset value: 0002$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RR_SLEEP_CNT										NR_EXT_TEMP_START			NR_ERR		
				rw							rw			rw	

Field	Bits	Type	Description
NR_ERR	2:0	rw	**Number of errors** Number of consecutive detected errors before error is valid and set in GEN_DIAG and individual fault registers. Only used for faults where counter NR_ERR is active (this can be set in register NR_ERR_MASK). Please note: The register CRC errors as well as the internal IC errors do not have an error counter. 000$_B$ **ERR_0**: 0 001$_B$ **ERR_1**: 1 010$_B$ **ERR_2**: 2 (default) 011$_B$ **ERR_3**: 3 100$_B$ **ERR_4**: 4 101$_B$ **ERR_5**: 5 110$_B$ **ERR_6**: 6 111$_B$ **ERR_7**: 7
NR_EXT_TEMP _START	5:3	rw	**External temperature triggering in round robin** 000$_B$ **EVERY_RR**: Every RR (default) 001$_B$ **1RR_1RR_NO_MES**: 1 RR measurement, 1 RR no measurement 010$_B$ **1RR_2RR_NO_MES**: 1 RR measurement, 2 RR no measurement 011$_B$ **1RR_3RR_NO_MES**: 1 RR measurement, 3 RR no measurement 100$_B$ **1RR_4RR_NO_MES**: 1 RR measurement, 4 RR no measurement 101$_B$ **1RR_5RR_NO_MES**: 1 RR measurement, 5 RR no measurement 110$_B$ **1RR_6RR_NO_MES**: 1 RR measurement, 6 RR no measurement 111$_B$ **1RR_7RR_NO_MES**: 1 RR measurement, 7 RR no measurement
RR_SLEEP_CN T	15:6	rw	**Round robin timing in sleep mode** 000$_H$ **DEACT**: RR in sleep mode is deactivated (default). 001$_H$ **RR_SLEEP_1**: tRR_sleep_LSB 3FF$_H$ **RR_SLEEP_1023**: tRR_sleep_LSB*1023

4.9 Round robin configuration (supplied in sleep)

RR_CONFIG

Round robin configuration [supplied in sleep)

Offset address: 0009$_H$

Reset value: 8024$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_NR_ERR_BAL_OC	M_NR_ERR_BAL_UC	M_NR_ERR_CELL_OV	M_NR_ERR_CELL_UV	M_NR_ERR_INT_OT	M_NR_ERR_EXT_T_ERR	M_NR_ERR_OL_ERR	M_NR_ERR_ADC_ERR	RR_SYNC	RR_CNT						
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw						

Field	Bits	Type	Description
RR_CNT	6:0	rw	**Round robin counter** 00$_H$ **RR_0**: Round robin starts every tRR_min. 24$_H$ **RR_36**: Round robin starts every tRR_min + 36 * tRR_LSB (default). 7F$_H$ **RR_127**: Round robin starts every tRR_max.
RR_SYNC	7	rw	**Round robin synchronization** 0$_B$ **NO_SYNC**: No synch with WD_CNT write access (default). 1$_B$ **SYNC**: Synch with WD_CNT write access (RR will be started by write access, if RR is already running the RR will be restarted from beginning again).
M_NR_ERR_ADC_ERR	8	rw	**Mask NR_ERR counter for ADC error** 0$_B$ **DISABLE**: No masking of NR_ERR. Counter is active (default). 1$_B$ **ENABLE**: NR_ERR counter masked. Fault valid after first detection.
M_NR_ERR_OL_ERR	9	rw	**Mask NR_ERR counter for open load error** 0$_B$ **DISABLE**: No masking of NR_ERR. Counter is active (default). 1$_B$ **ENABLE**: NR_ERR counter masked. Fault valid after first detection.
M_NR_ERR_EXT_T_ERR	10	rw	**Mask NR_ERR counter for external temperature error** 0$_B$ **DISABLE**: No masking of NR_ERR. Counter is active (default). 1$_B$ **ENABLE**: NR_ERR counter masked. Fault valid after first detection.
M_NR_ERR_INT_OT	11	rw	**Mask NR_ERR counter for internal temperature error** 0$_B$ **DISABLE**: No masking of NR_ERR. Counter is active (default). 1$_B$ **ENABLE**: NR_ERR counter masked. Fault valid after first detection.
M_NR_ERR_CELL_UV	12	rw	**Mask NR_ERR counter for undervoltage error** 0$_B$ **DISABLE**: No masking of NR_ERR. Counter is active (default). 1$_B$ **ENABLE**: NR_ERR counter masked. Fault valid after first detection.
M_NR_ERR_CELL_OV	13	rw	**Mask NR_ERR counter for overvoltage error** 0$_B$ **DISABLE**: No masking of NR_ERR. Counter is active (default). 1$_B$ **ENABLE**: NR_ERR counter masked. Fault valid after first detection.

(table continues...)

(continued)

Field	Bits	Type	Description
M_NR_ERR_BAL_UC	14	rw	**Mmask NR_ERR counter for balancing error undercurrent** 0_B **DISABLE**: No masking of NR_ERR. Counter is active (default). 1_B **ENABLE**: NR_ERR counter masked. Fault valid after first detection.
M_NR_ERR_BAL_OC	15	rw	**Mask NR_ERR counter for balancing error overcurrent** 0_B **DISABLE**: No masking of NR_ERR. Counter is active. 1_B **ENABLE**: NR_ERR counter masked. Fault valid after first detection (default).

4.10 ERR pin / EMM mask (supplied in sleep)

FAULT_MASK

ERR pin / EMM mask [supplied in sleep)

Offset address: 000A$_H$

Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_BAL_ERR_OC	M_BAL_ERR_UC	M_CELL_OV	M_CELL_UV	M_INT_OT	M_EXT_T_ERR	M_REG_CRC_ERR	M_INT_IC_ERR	M_OL_ERR	M_ADC_ERR	ERR_PIN		Res			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		r			

Field	Bits	Type	Description
ERR_PIN	5	rw	**Enable Error PIN functionality**
			0$_B$ **DISABLE**: ERR pin deactivated, EMM signal active. Device goes back to the mode as it was before the EMM (default).
			1$_B$ **ENABLE**: ERR Pin function enabled. Fault indication only via ERR Pin. EMM signal deactivated. If ERR PIN triggered, pin stays high (device is then in normal mode) until watchdog runs out or pin is cleared.
M_ADC_ERR	6	rw	**EMM/ERR mask for ADC error**
			0$_B$ **DISABLE**: ERR/EMM will NOT be set if this type of error occurs (default).
			1$_B$ **ENABLE**: ERR/EMM will be set for this type of error.
M_OL_ERR	7	rw	**EMM/ERR mask for open load error**
			0$_B$ **DISABLE**: ERR/EMM will NOT be set if this type of error occurs (default).
			1$_B$ **ENABLE**: ERR/EMM will be set for this type of error.
M_INT_IC_ERR	8	rw	**EMM/ERR mask for internal IC error**
			0$_B$ **DISABLE**: ERR/EMM will NOT be set if this type of error occurs (default).
			1$_B$ **ENABLE**: ERR/EMM will be set for this type of error.
M_REG_CRC_ERR	9	rw	**EMM/ERR mask for register CRC error**
			0$_B$ **DISABLE**: ERR/EMM will NOT be set if this type of error occurs (default).
			1$_B$ **ENABLE**: ERR/EMM will be set for this type of error.
M_EXT_T_ERR	10	rw	**EMM/ERR mask for external temperature error**
			0$_B$ **DISABLE**: ERR/EMM will NOT be set if this type of error occurs (default).
			1$_B$ **ENABLE**: ERR/EMM will be set for this type of error.
M_INT_OT	11	rw	**EMM/ERR mask for internal temperature error**
			0$_B$ **DISABLE**: ERR/EMM will NOT be set if this type of error occurs (default).
			1$_B$ **ENABLE**: ERR/EMM will be set for this type of error.

(table continues...)

(continued)

Field	Bits	Type	Description
M_CELL_UV	12	rw	**EMM/ERR mask for cell undervoltage error** 0_B **DISABLE**: ERR/EMM will NOT be set if this type of error occurs (default). 1_B **ENABLE**: ERR/EMM will be set for this type of error.
M_CELL_OV	13	rw	**EMM/ERR mask for cell overvoltage error** 0_B **DISABLE**: ERR/EMM will NOT be set if this type of error occurs (default). 1_B **ENABLE**: ERR/EMM will be set for this type of error.
M_BAL_ERR_UC	14	rw	**EMM/ERR mask for balancing error undercurrent** 0_B **DISABLE**: ERR/EMM will NOT be set if this type of error occurs (default). 1_B **ENABLE**: ERR/EMM will be set for this type of error.
M_BAL_ERR_OC	15	rw	**EMM/ERR mask for balancing error overcurrent** 0_B **DISABLE**: ERR/EMM will NOT be set if this type of error occurs (default). 1_B **ENABLE**: ERR/EMM will be set for this type of error.

4.11 General diagnostics (supplied in sleep)

GEN_DIAG
Offset address: 000B$_H$

General diagnostics [supplied in sleep)
Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAL_ERR_OC	BAL_ERR_UC	CELL_OV	CELL_UV	INT_OT	EXT_T_ERR	REG_CRC_ERR	INT_IC_ERR	OL_ERR	ADC_ERR	PS_ERR_SLEEP	RR_ACTIVE	LOCK_MEAS	BAL_ACTIVE	MOT_MOB_N	UART_WAKEUP
rocwl	rocwl	rocwl	rocwl	rocw	rocwl	rocwl	rocw	rocwl	rocw	rocw	rh	rh	rh	rh	rh

Field	Bits	Type	Description
UART_WAKEUP	0	rh	**Wake-up via UART** 0_B **ISOUART**: Wake-up via iso UART (default) 1_B **UART**: Wake-up via UART (GPIO)
MOT_MOB_N	1	rh	**Primary on Top/Bottom configuration** 0_B **BOTTOM**: Configured as primary on bottom (default) 1_B **TOP**: Configured as primary on top
BAL_ACTIVE	2	rh	**Balancing active** 0_B **OFF**: No balancing ongoing (default) 1_B **ON**: Balancing ongoing, at least one channel is on
LOCK_MEAS	3	rh	**Lock measurement** This bit indicates an ongoing PCVM, SCVM, BVM or AVM measurement or a delayed RR. 0_B **MEAS_OFF**: No measurement ongoing (default) 1_B **MEAS_ON**: PCVM, SCVM, BVM or AVM measurement ongoing
RR_ACTIVE	4	rh	**Round robin active** This bit indicates if the round robin was active during read. 0_B **OFF**: No round robin active (default) 1_B **ON**: Round robin active
PS_ERR_SLEEP	5	rocw	**Power supply error induced sleep** 0_B **NO_ERR**: No power supply error induced sleep (default) 1_B **ERR_OCCURED**: Power supply error induced sleep occured
ADC_ERR	6	rocw	**ADC Error** 0_B **NO_ERR**: No ADC mismatch between sum of PCVM and BVM (default) 1_B **ERR_OCCURED**: ERROR of ADC-result comparison. Balancing deactivated.

(table continues…)

(continued)

Field	Bits	Type	Description
OL_ERR	7	rocwl	**Open load error** Please note: Resetting the error here resets also the respective detailed error register. 0_B **NO_ERR**: No open load error (default) 1_B **ERR_OCCURED**: Open load error occured. Detailed information in the respective error register. Balancing deactivated.
INT_IC_ERR	8	rocw	**Internal IC error** 0_B **NO_ERR**: No internal error (default) 1_B **ERR_OCCURED**: Internal IC check error occurred. Balancing is deactivated.
REG_CRC_ERR	9	rocwl	**Register CRC error** Please note: Resetting the error here resets also the respective detailed error register. 0_B **NO_ERR**: No CRC check error (default) 1_B **ERR_OCCURED**: CRC check error occured. Detailed information in the respective error register. Balancing deactivated.
EXT_T_ERR	10	rocwl	**External temperature error** Please note: Resetting the error here resets also the respective detailed error register. 0_B **NO_ERR**: No external temperature error (default) 1_B **ERR_OCCURED**: External temperature error occured. Detailed information in the respective error register. Balancing is deactivated.
INT_OT	11	rocw	**Internal temperature (OT) error** 0_B **NO_ERR**: No internal OT error (default) 1_B **ERR_OCCURED**: Internal OT error occured. Balancing is deactivated.
CELL_UV	12	rocwl	**Cell undervoltage (UV) error** Please note: Resetting the error here resets also the respective detailed error register. 0_B **NO_ERR**: No UV error (default) 1_B **ERR_OCCURED**: UV error occured. Detailed information in the respective error register.
CELL_OV	13	rocwl	**Cell overvoltage (OV) error** Please note: Resetting the error here resets also the respective detailed error register. 0_B **NO_ERR**: No OV error (default) 1_B **ERR_OCCURED**: OV error occured. Detailed information in the respective error register.
BAL_ERR_UC	14	rocwl	**Balancing error undercurrent (will be reset in sleep mode)** Please note: Resetting the error here resets also the respective detailed error register. 0_B **NO_ERR**: No balancing error (default) 1_B **ERR_OCCURED**: Balancing error occured. Detailed information in the respective error register.

(table continues...)

(continued)

Field	Bits	Type	Description
BAL_ERR_OC	15	rocwl	**Balancing error overcurrent (will be reset in sleep mode)** Please Note: Resetting the error here resets also the respective detailed error register. 0_B **NO_ERR**: No balancing error (default) 1_B **ERR_OCCURED**: Balancing error occured. Detailed information in the respective error register.

4.12 Cell voltage supervision warning flags UV (supplied in sleep)

CELL_UV

Cell voltage supervision warning flags UV [supplied in sleep)

Offset address: 000C$_H$

Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				UV_11	UV_10	UV_9	UV_8	UV_7	UV_6	UV_5	UV_4	UV_3	UV_2	UV_1	UV_0
				rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw

Field	Bits	Type	Description
UV_i (i=0-11)	i	rocw	**Undervoltage in cell i** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0$_B$ **NO_UV**: No undervoltage detected in respective cell (default) 1$_B$ **UV**: Undervoltage detected in respective cell. Balancing is deactivated.

4.13 Cell voltage supervision warning flags OV (supplied in sleep)

CELL_OV   Offset address: 000D$_H$

Cell voltage supervision warning flags OV [supplied in   Reset value: 0000$_H$
sleep)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				OV_11	OV_10	OV_9	OV_8	OV_7	OV_6	OV_5	OV_4	OV_3	OV_2	OV_1	OV_0
				rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw

Field	Bits	Type	Description
OV_i (i=0-11)	i	rocw	**Overvoltage in cell i** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0$_B$ **NO_OV**: No overvoltage detected in respective cell (default) 1$_B$ **OV**: Overvoltage detected in respective cell. Balancing is deactivated.

4.14 External overtemperature warning flags (supplied in sleep)

EXT_TEMP_DIAG

External overtemperature warning flags [supplied in sleep)

Offset address: 000E$_H$

Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	OT4	SHO RT4	OPE N4	OT3	SHO RT3	OPE N3	OT2	SHO RT2	OPE N2	OT1	SHO RT1	OPE N1	OT0	SHO RT0	OPE N0
r	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw

Field	Bits	Type	Description
OPEN0	0	rocw	**Open load in external temp 0** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0$_B$ **NO_OL**: No open load in external temp 0 (default) 1$_B$ **OL_OCCURED**: Open load in external temp 0
SHORT0	1	rocw	**Short in external temp 0** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0$_B$ **NO_SHORT**: No short in external temp 0 (default) 1$_B$ **SHORT_OCCURED**: Short in external temp 0
OT0	2	rocw	**Overtemperature in external temp 0** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0$_B$ **NO_OT**: No overtemperature in external temp 0 (default) 1$_B$ **OT_OCCURED**: ADC conversion of external temp 0 measurement < overtemperature threshold EXT_OT_THR
OPEN1	3	rocw	**Open load in external temp 1** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0$_B$ **NO_OL**: No open load in external temp 1 (default) 1$_B$ **OL_OCCURED**: Open load in external temp 1
SHORT1	4	rocw	**Short in external temp 1** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0$_B$ **NO_SHORT**: No short in external temp 1 (default) 1$_B$ **SHORT_OCCURED**: Short in external temp 1
OT1	5	rocw	**Overtemperature in external temp 1** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0$_B$ **NO_OT**: No overtemperature in external temp 1 (default) 1$_B$ **OT_OCCURED**: ADC conversion of external temp 1 measurement < overtemperature threshold EXT_OT_THR
OPEN2	6	rocw	**Open load in external temp 2** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0$_B$ **NO_OL**: No open load in external temp 2 (default) 1$_B$ **OL_OCCURED**: Open load in external temp 2

(table continues…)

(continued)

Field	Bits	Type	Description
SHORT2	7	rocw	**Short in external temp 2** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0_B **NO_SHORT**: No short in external temp 2 (default) 1_B **SHORT_OCCURED**: Short in external temp 2
OT2	8	rocw	**Overtemperature in external temp 2** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0_B **NO_OT**: No overtemperature in external temp 2 (default) 1_B **OT_OCCURED**: ADC conversion of external temp 2 measurement < overtemperature threshold EXT_OT_THR
OPEN3	9	rocw	**Open load in external temp 3** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0_B **NO_OL**: No open load in external temp 3 (default) 1_B **OL_OCCURED**: Open load in external temp 3
SHORT3	10	rocw	**Short in external temp 3** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0_B **NO_SHORT**: No short in external temp 3 (default) 1_B **SHORT_OCCURED**: Short in external temp 3
OT3	11	rocw	**Overtemperature in external temp 3** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0_B **NO_OT**: No overtemperature in external temp 3 (default) 1_B **OT_OCCURED**: ADC conversion of external temp 3 measurement < overtemperature threshold EXT_OT_THR
OPEN4	12	rocw	**Open load in external temp 4** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0_B **NO_OL**: No open load in external temp 4 (default) 1_B **OL_OCCURED**: Open load in external temp 4
SHORT4	13	rocw	**Short in external temp 4** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0_B **NO_SHORT**: No short in external temp 4 (default) 1_B **SHORT_OCCURED**: Short in external temp 4
OT4	14	rocw	**Overtemperature in external temp 4** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0_B **NO_OT**: No overtemperature in external temp 4 (default) 1_B **OT_OCCURED**: ADC conversion of external temp 4 measurement < overtemperature threshold EXT_OT_THR

4.15 Diagnostics open load (supplied in sleep)

DIAG_OL   Offset address: 0010$_H$
Diagnostics open load [supplied in sleep)   Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				OL_11	OL_10	OL_9	OL_8	OL_7	OL_6	OL_5	OL_4	OL_3	OL_2	OL_1	OL_0
				rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw

Field	Bits	Type	Description
OL_i (i=0-11)	i	rocw	**Open load channel i** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0$_B$ **NO_OL**: No open load detected for respective channel (default) 1$_B$ **OL**: Open load detected for respective channel

4.16 REG_CRC_ERR (supplied in sleep)

REG_CRC_ERR   Offset address: 0011_H

REG_CRC_ERR [supplied in sleep)   Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res									ADDR						

	Res									ADDR					
				r						rocw					
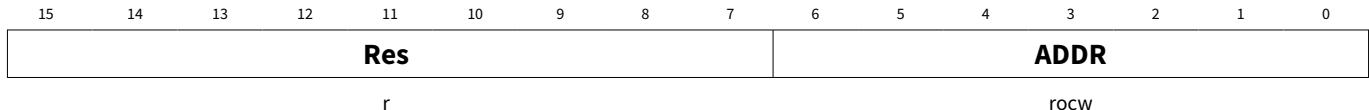
Field	Bits	Type	Description
ADDR	6:0	rocw	**Register address of register where CRC check failed** Register address of CRC check fail, can also be cleared on write '0' to connected GEN_DIAG register bit. 00_H **DEFAULT**: Register address

4.17 Cell voltage supervision warning flags UV (supplied in sleep)

CELL_UV_DAC_COMP   Offset address: 0012_H

Cell voltage supervision warning flags UV [supplied in   Reset value: 0000_H
sleep)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				UV_11	UV_10	UV_9	UV_8	UV_7	UV_6	UV_5	UV_4	UV_3	UV_2	UV_1	UV_0
				rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw

Field	Bits	Type	Description
UV_i (i=0-11)	i	rocw	**Undervoltage in cell i** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0_B **NO_UV**: No undervoltage detected in respective cell (default) 1_B **UV**: Uundervoltage detected in respective cell

4.18 Cell voltage supervision warning flags OV (supplied in sleep)

CELL_OV_DAC_COMP

Cell voltage supervision warning flags OV [supplied in sleep)

Offset address: 0013$_H$

Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				OV_11	OV_10	OV_9	OV_8	OV_7	OV_6	OV_5	OV_4	OV_3	OV_2	OV_1	OV_0
				rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw

Field	Bits	Type	Description
OV_i (i=0-11)	i	rocw	**Overvoltage in cell i** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0$_B$ **NO_OV**: No overvoltage detected in respective cell (default) 1$_B$ **OV**: Overvoltage detected in respective cell

4.19 Operation mode

OP_MODE
Operation mode

Offset address: 0014$_H$
Reset value: C400$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			LR_TIME					Res				I_DIAG_EN	SLEEP_REG_RESET	EXT_WD	PD
			rw					r				rw	rwh	rw	rw
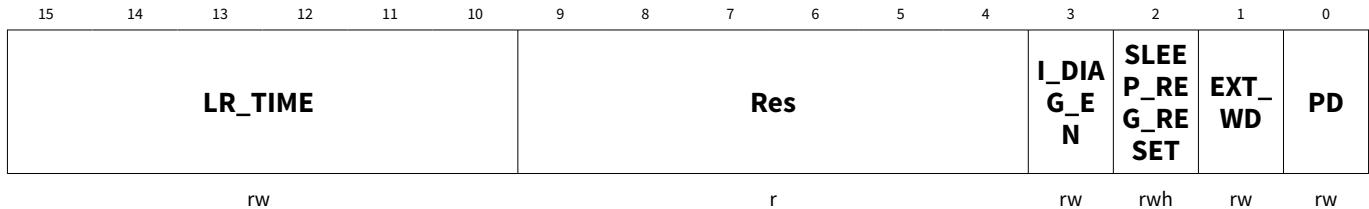
Field	Bits	Type	Description
PD	0	rw	**Activate sleep mode** 0$_B$ **NORMAL_OP**: Chip operating in normal mode (default) 1$_B$ **PWD_OP**: Chip is set to sleep mode. No further communication possible after bit is set to '1'.
EXT_WD	1	rw	**Extended watchdog** 0$_B$ **NOT_ACTIVE**: No extended watchdog (default) 1$_B$ **ACTIVE**: Extended watchdog active
SLEEP_REG_RESET	2	rwh	**Sleep mode registers reset** 0$_B$ **NORMAL_OP**: Chip operating in normal mode (default) 1$_B$ **SLEEP_REG_RESET_OP**: Resets all registers that are supplied in sleep mode. No further communication possible after bit is set to '1'.
I_DIAG_EN	3	rw	**Force OL diagnostics currents** 0$_B$ **OFF**: Diagnostics currents switched via round robin (default) 1$_B$ **ON**: Diagnostics currents enabled for all channels
LR_TIME	15:10	rw	**Long-running mode measurement restart time** 00$_H$ **MIN**: Minimum (1.17ms) 31$_H$ **DEFAULT**: 6.25 ms

4.20 Balancing current thresholds

BAL_CURR_THR   Offset address: 0015$_H$

Balancing current thresholds   Reset value: 00AC$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UC_THR								OC_THR							
rw								rw							
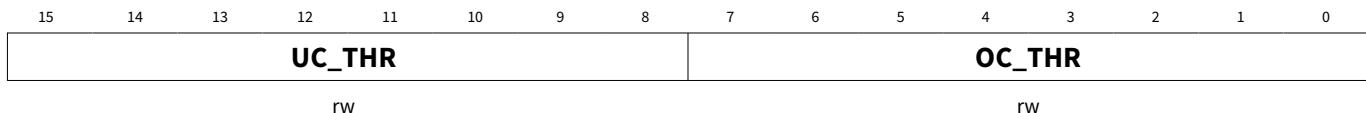
Field	Bits	Type	Description
OC_THR	7:0	rw	**Overcurrent fault threshold** 8-bit to define the maximum voltage drop during balancing diagnostics. If the voltage drop ($I_{Bal}*R_F$) > OC_THR the overcurrent is detected. AC$_H$ **DEFAULT**: Default
UC_THR	15:8	rw	**Undercurrent fault threshold** 8-bit to define the minimum voltage drop during balancing diagnostics. If the voltage drop ($I_{Bal}*R_F$) < UC_THR the undercurrent is detected. 00$_H$ **DEFAULT**: Default

4.21 Balance settings

BAL_SETTINGS

Offset address: 0016_H

Balance settings

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				ON11	ON10	ON9	ON8	ON7	ON6	ON5	ON4	ON3	ON2	ON1	ON0
				rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
ONi (i=0-11)	i	rwh	**Switching state of balancing switch i** 0_B **OFF**: Respective balancing switch off (default) 1_B **ON**: Respective balancing switch on

4.22 Auxiliary voltage measurement configuration

AVM_CONFIG   Offset address: 0017$_H$

Auxiliary voltage measurement configuration   Reset value: 0007$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R_DIAG_CUR_SRC	R_DIAG_SEL_1		R_DIAG_SEL_0		Res	R_DIAG	AUX_BIPOLAR	AVM_TMP4_MASK	AVM_TMP3_MASK	AVM_TMP2_MASK	AVM_TMP1_MASK	AVM_TMP0_MASK	TEMP_MUX_DIAG_SEL		
rw	rw		rw		r	rw	rwh	rw	rw	rw	rw	rw	rw		

Field	Bits	Type	Description
TEMP_MUX_DIAG_SEL	2:0	rw	**Selector for external temp diagnose** 000$_B$ **PD_EXT_TEMP_0**: Pulldown for external temp 0 measurement is active. 001$_B$ **PD_EXT_TEMP_1**: Pulldown for external temp 1 measurement is active. 010$_B$ **PD_EXT_TEMP_2**: Pulldown for external temp 2 measurement is active. 011$_B$ **PD_EXT_TEMP_3**: Pulldown for external temp 3 measurement is active. 100$_B$ **PD_EXT_TEMP_4**: Pulldown for external temp 4 measurement is active. 111$_B$ **NO_PD**: No pulldown is active (default),
AVM_TMP0_MASK	3	rw	**Activate auxiliary measurement via deactive TMP0 as part of AVM** 0$_B$ **MASKED**: Manual AVM TMP0 measurement masked out when AVM_START bit triggered (default). 1$_B$ **PERFORMED**: Manual AVM TMP0 measurement performed when AVM_START bit triggered.
AVM_TMP1_MASK	4	rw	**Activate auxiliary measurement via deactive TMP1 as part of AVM** 0$_B$ **MASKED**: Manual AVM TMP1 measurement masked out when AVM_START bit triggered (default). 1$_B$ **PERFORMED**: Manual AVM TMP1 measurement performed when AVM_START bit triggered.
AVM_TMP2_MASK	5	rw	**Activate auxiliary measurement via deactive TMP2 as part of AVM** 0$_B$ **MASKED**: Manual AVM TMP2 measurement masked out when AVM_START bit triggered (default). 1$_B$ **PERFORMED**: Manual AVM TMP2 measurement performed when AVM_START bit triggered.
AVM_TMP3_MASK	6	rw	**Activate auxiliary measurement via deactive TMP3 as part of AVM** 0$_B$ **MASKED**: Manual AVM TMP3 measurement masked out when AVM_START bit triggered (default). 1$_B$ **PERFORMED**: Manual AVM TMP3 measurement performed when AVM_START bit triggered.

(table continues…)

(continued)

Field	Bits	Type	Description
AVM_TMP4_MASK	7	rw	**Activate auxiliary measurement via deactive TMP4 as part of AVM** 0_B **MASKED**: Manual AVM TMP4 measurement masked out when AVM_START bit triggered (default). 1_B **PERFORMED**: Manual AVM TMP4 measurement performed when AVM_START bit triggered.
AUX_BIPOLAR	8	rwh	**Bipolar AUX measurement instead of BVM** 0_B **BVM**: Normal BVM measurement 1_B **AUX**: Bipolar AUX measurement instead of BVM (Bit is reset when NR_TEMP_SENSE > 3, this can cause a REG_CRC_ERR).
R_DIAG	9	rw	**Masking diagnostics resistor as part of AVM** 0_B **MASKED**: Manual AVM diagnostics resistor measurement masked out when AVM_START bit triggered (default) 1_B **PERFORMED**: Manual AVM diagnostics resistor measurement performed when AVM_START bit triggered
R_DIAG_SEL_0	12:11	rw	**R_DIAG current source 0** 00_B **I_0**: Source ITMP0_0: 320uA (default) 01_B **I_1**: Source ITMP0_1: 80uA 10_B **I_2**: Source ITMP0_2: 20uA 11_B **I_3**: Source ITMP0_3: 5uA
R_DIAG_SEL_1	14:13	rw	**R_DIAG current source 1** 00_B **I_0**: Source ITMP1_0: 320uA (default) 01_B **I_1**: Source ITMP1_1: 80uA 10_B **I_2**: Source ITMP1_2: 20uA 11_B **I_3**: Source ITMP1_3: 5uA
R_DIAG_CUR_SRC	15	rw	**R_DIAG current source selection** 0_B **SRC_0**: Current source 0 (default) 1_B **SRC_1**: Current source 1

4.23 Measurement control

MEAS_CTRL   Offset address: 0018$_H$

Measurement control   Reset value: 0021$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCVM_START	CVM_MODE			BVM_START	BVM_MODE			AVM_START	SCVM_START	PBOFF	CVM_DEL				
rwh	rw			rwh	rw			rwh	rwh	rw	rw				

Field	Bits	Type	Description
CVM_DEL	4:0	rw	**Wait time before CVM and/or BVM is started when PBOFF=1** 00$_H$ **NO_SETTLING_TIME**: No settling time 01$_H$ **1**: tVM_del_LSB (default) 1F$_H$ **31**: 31 x tVM_del_LSB
PBOFF	5	rw	**Enable PBOFF** 0$_B$ **BAL_CONTINUE**: Keep balancing state for PCVM/SCVM/BVM, no CVM_DEL. 1$_B$ **BAL_INTERRUPT**: Switch off balancing before conversion starts (default).
SCVM_START	6	rwh	**Start secondary cell voltage measurement** Bit cleared if conversion done 0$_B$ **NO_MEAS**: No measurement ongoing (default) 1$_B$ **TRIG_MEAS**: Trigger measurement
AVM_START	7	rwh	**Start auxillary voltage measurement** Bit cleared if conversion done 0$_B$ **NO_MEAS**: No measurement ongoing (default) 1$_B$ **TRIG_MEAS**: Trigger measurement if BVM_START=0
BVM_MODE	10:8	rw	**Block voltage measurement mode** 000$_B$ **10_BIT**: 10 bit (default) 001$_B$ **11_BIT**: 11 bit 110$_B$ **16_BIT**: 16 bit 111$_B$ **LONG**: Long-running mode
BVM_START	11	rwh	**Start block voltage measurement** Bit cleared if conversion done 0$_B$ **NO_MEAS**: No measurement ongoing (default) 1$_B$ **TRIG_MEAS**: Trigger measurement
CVM_MODE	14:12	rw	**Cell voltage measurement mode** 000$_B$ **10_BIT**: 10 bit (default) 001$_B$ **11_BIT**: 11 bit 110$_B$ **16_BIT**: 16 bit 111$_B$ **LONG**: Long-running mode

(table continues...)

(continued)

Field	Bits	Type	Description
PCVM_START	15	rwh	**Start primary cell voltage measurement** Bit cleared if conversion done 0_B **NO_MEAS**: No measurement ongoing (default) 1_B **TRIG_MEAS**: Trigger measurement

4.24 Primary cell voltage measurement i

PCVM_i (i=0-11)   Offset address: 0019_H+i
Primary cell voltage measurement i   Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							RESULT								

rh

Field	Bits	Type	Description
RESULT	15:0	rh	**Result of cell voltage measurement** 0000_H **DEFAULT**: Default

4.25   SCVM highest cell voltage

SCVM_HIGH   Offset address: 0025$_H$

SCVM highest cell voltage   Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESULT											Res			UPD_CNT	
rh											r			rh	

Field	Bits	Type	Description
UPD_CNT	1:0	rh	**Update counter**
RESULT	15:5	rh	**Result of SCVM measurement (highest cell voltage)**

4.26   SCVM lowest cell voltage

SCVM_LOW   Offset address: 0026$_H$

SCVM lowest cell voltage   Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESULT											Res			UPD_CNT	
					rh							r		rh	

Field	Bits	Type	Description
UPD_CNT	1:0	rh	**Update counter**
RESULT	15:5	rh	**Result of SCVM measurement (lowest cell voltage)**

4.27 Stress correction PCVM

STRESS_PCVM   Offset address: 0027$_H$

Stress correction PCVM   Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							STRESS_CORRECTION								

rh

Field	Bits	Type	Description
STRESS_CORRECTION	15:0	rh	**Stress correction value PCVM** 0000$_H$ **DEFAULT**: Default

4.28 Block voltage measurement

BVM   Offset address: 0028$_H$

Block voltage measurement   Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							RESULT								

rh

Field	Bits	Type	Description
RESULT	15:0	rh	**Result of block voltage measurement**
			0000$_H$ **DEFAULT**: Default

4.29 Temp result 0

EXT_TEMP_0   Offset address: 0029$_H$

Temp result 0   Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	**PD_ERR**	**VALID**	**PULL DOWN**	**INTC**					**RESULT**						
r	rocw	rocr	rh	rh						rh					

Field	Bits	Type	Description
RESULT	9:0	rh	**Result of external temp measurement** SD-ADC result of resistance or voltage measurement. 000$_H$ **DEFAULT**: Default
INTC	11:10	rh	**Indicates which current source was used** Number of current source that was active for latest measurement. 00$_B$ **I_0**: Source ITMPz_0 used (default) 01$_B$ **I_1**: Source ITMPz_1 used 10$_B$ **I_2**: Source ITMPz_2 used 11$_B$ **I_3**: Source ITMPz_3 used
PULLDOWN	12	rh	**Indicating pull-down switch state** 0$_B$ **NORMAL_MEAS**: Normal measurement done (default) 1$_B$ **PULL_DOWN**: Pull-down for Mux-test was active during conversion.
VALID	13	rocr	**Indicating a valid result** 0$_B$ **NO_NEW_RESULT**: No new result available (default) 1$_B$ **NEW_RESULT_STORED**: A new result is stored in the register, cleared automatically after readout of the result register.
PD_ERR	14	rocw	**Pull-down error** Can also be cleared on write '0' to GEN_DIAG.EXT_T_ERR register bit. 0$_B$ **NO_ERR**: No pulldown error 1$_B$ **ERR**: Pulldown error

4.30   Temp result 1

EXT_TEMP_1   Offset address: 002A$_H$

Temp result 1   Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	**PD_ERR**	**VALID**	**PULL DOWN**	**INTC**						**RESULT**					
r	rocw	rocr	rh	rh						rh					

Field	Bits	Type	Description
RESULT	9:0	rh	**Result of external temp measurement** SD-ADC result of resistance or voltage measurement. 000$_H$ **DEFAULT**: Default
INTC	11:10	rh	**Indicates which current source was used** Number of current source that was active for latest measurement. 00$_B$ **I_0**: Source ITMPz_0 used (default) 01$_B$ **I_1**: Source ITMPz_1 used 10$_B$ **I_2**: Source ITMPz_2 used 11$_B$ **I_3**: Source ITMPz_3 used
PULLDOWN	12	rh	**Indicating pull-down switch state** 0$_B$ **NORMAL_MEAS**: Normal measurement done (default) 1$_B$ **PULL_DOWN**: Pull-down for Mux-test was active during conversion.
VALID	13	rocr	**Indicating a valid result** 0$_B$ **NO_NEW_RESULT**: No new result available (default) 1$_B$ **NEW_RESULT_STORED**: A new result is stored in the register, cleared automatically after readout of the result register.
PD_ERR	14	rocw	**Pull-down error** Can also be cleared on write '0' to GEN_DIAG.EXT_T_ERR register bit. 0$_B$ **NO_ERR**: No pulldown error 1$_B$ **ERR**: Pulldown error

4.31 Temp result 2

EXT_TEMP_2   Offset address: 002B$_H$

Temp result 2   Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	**PD_ERR**	**VALID**	**PULL DOWN**	**INTC**		**RESULT**									
r	rocw	rocr	rh	rh						rh					

Field	Bits	Type	Description
RESULT	9:0	rh	**Result of external temp measurement** SD-ADC result of resistance or voltage measurement. 000$_H$ **DEFAULT**: Default
INTC	11:10	rh	**Indicates which current source was used** Number of current source that was active for latest measurement. 00$_B$ **I_0**: Source ITMPz_0 used (default) 01$_B$ **I_1**: Source ITMPz_1 used 10$_B$ **I_2**: Source ITMPz_2 used 11$_B$ **I_3**: Source ITMPz_3 used
PULLDOWN	12	rh	**Indicating pull-down switch state** 0$_B$ **NORMAL_MEAS**: Normal measurement done (default) 1$_B$ **PULL_DOWN**: Pull-down for Mux-test was active during conversion.
VALID	13	rocr	**Indicating a valid result** 0$_B$ **NO_NEW_RESULT**: No new result available (default) 1$_B$ **NEW_RESULT_STORED**: A new result is stored in the register, cleared automatically after readout of the result register.
PD_ERR	14	rocw	**Pull-down error** Can also be cleared on write '0' to GEN_DIAG.EXT_T_ERR register bit. 0$_B$ **NO_ERR**: No pulldown error 1$_B$ **ERR**: Pulldown error

4.32 Temp result 3

EXT_TEMP_3   Offset address: 002C$_H$

Temp result 3   Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	**PD_ERR**	**VALID**	**PULL DOWN**	**INTC**					**RESULT**						
r	rocw	rocr	rh	rh					rh						

Field	Bits	Type	Description
RESULT	9:0	rh	**Result of external temp measurement** SD-ADC result of resistance or voltage measurement. 000$_H$ **DEFAULT**: Default
INTC	11:10	rh	**Indicates which current source was used** Number of current source that was active for latest measurement. 00$_B$ **I_0**: Source ITMPz_0 used (default) 01$_B$ **I_1**: Source ITMPz_1 used 10$_B$ **I_2**: Source ITMPz_2 used 11$_B$ **I_3**: Source ITMPz_3 used
PULLDOWN	12	rh	**Indicating pull-down switch state** 0$_B$ **NORMAL_MEAS**: Normal measurement done (default) 1$_B$ **PULL_DOWN**: Pull-down for Mux-test was active during conversion.
VALID	13	rocr	**Indicating a valid result** 0$_B$ **NO_NEW_RESULT**: No new result available (default) 1$_B$ **NEW_RESULT_STORED**: A new result is stored in the register, cleared automatically after readout of the result register.
PD_ERR	14	rocw	**Pull-down error** Can also be cleared on write '0' to GEN_DIAG.EXT_T_ERR register bit. 0$_B$ **NO_ERR**: No pulldown error 1$_B$ **ERR**: Pulldown error

4.33 Temp result 4

EXT_TEMP_4   Offset address: 002D$_H$

Temp result 4   Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	PD_ERR	VALID	PULL DOWN	INTC					RESULT						
r	rocw	rocr	rh	rh					rh						

Field	Bits	Type	Description
RESULT	9:0	rh	**Result of external temp measurement** SD-ADC result of resistance or voltage measurement. 000$_H$ **DEFAULT**: Default
INTC	11:10	rh	**Indicates which current source was used** Number of current source that was active for latest measurement. 00$_B$ **I_0**: Source ITMPz_0 used (default) 01$_B$ **I_1**: Source ITMPz_1 used 10$_B$ **I_2**: Source ITMPz_2 used 11$_B$ **I_3**: Source ITMPz_3 used
PULLDOWN	12	rh	**Indicating pull-down switch state** 0$_B$ **NORMAL_MEAS**: Normal measurement done (default) 1$_B$ **PULL_DOWN**: Pull-down for Mux-test was active during conversion.
VALID	13	rocr	**Indicating a valid result** 0$_B$ **NO_NEW_RESULT**: No new result available (default) 1$_B$ **NEW_RESULT_STORED**: A new result is stored in the register, cleared automatically after readout of the result register2.
PD_ERR	14	rocw	**Pull-down error** Can also be cleared on write '0' to GEN_DIAG.EXT_T_ERR register bit. 0$_B$ **NO_ERR**: No pulldown error 1$_B$ **ERR**: Pulldown error

4.34 Temp result R diagnose

EXT_TEMP_R_DIAG Offset address: 002F$_H$

Temp result R diagnose Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res		VALID	CUR_SRC	INTC		RESULT									
r		rocr	rh	rh		rh									

Field	Bits	Type	Description
RESULT	9:0	rh	**Result of diagnostics resistor measurement** SD-ADC result of diagnostics resistor measurement. 000$_H$ **DEFAULT**: Default
INTC	11:10	rh	**Indicates which current source was used** Number of current source that was active for latest measurement. 00$_B$ **I_0**: Source ITMPz_0 used (default) 01$_B$ **I_1**: Source ITMPz_1 used 10$_B$ **I_2**: Source ITMPz_2 used 11$_B$ **I_3**: Source ITMPz_3 used
CUR_SRC	12	rh	**Indicates which current source was used** 0$_B$ **SRC_0**: Source 0 (default) 1$_B$ **SRC_1**: Source 1
VALID	13	rocr	**Indicating a valid result** 0$_B$ **NO_NEW_RESULT**: No new result available (default) 1$_B$ **NEW_RESULT_STORED**: A new result is stored in the register, cleared automatically after readout of the result register.

4.35 Chip temperature

INT_TEMP   Offset address: 0030$_H$

Chip temperature   Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res		VALID	Res			RESULT									
r		rocr	r			rh									
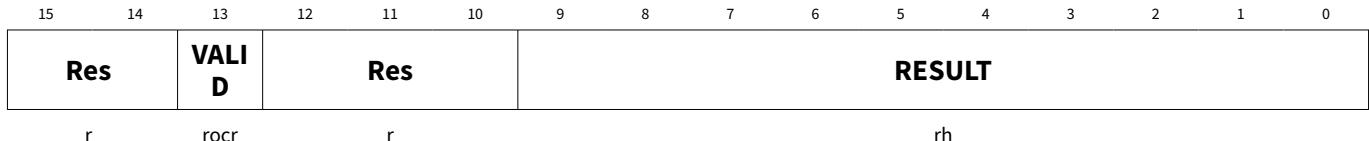
Field	Bits	Type	Description
RESULT	9:0	rh	**Result of internal temperatur measurement** SD-ADC result of internal temperature measurement. 000$_H$ **DEFAULT**: Default
VALID	13	rocr	**Indicating a valid result** 0$_B$ **NO_NEW_RESULT**: No new result available (default) 1$_B$ **NEW_RESULT_STORED**: A new result is stored in the register, cleared automatically after readout of the result register.

4.36 Multiread command

MULTI_READ   Offset address: 0031$_H$

Multiread command   Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							RES								

rh

Field	Bits	Type	Description
RES	15:0	rh	**Used in combination with MULTI_READ_CFG** Reading this register by the host starts the multiple register read routine which got define in the MULTI_READ_CFG register. 0000$_H$ **DEFAULT**: Not defined (default)

4.37 Multiread configuration

This register must be written with a broadcast write command.

MULTI_READ_CFG   Offset address: 0032$_H$

Multiread configuration   Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		Res		STRESS_PCVM_SEL	SCVM_SEL	INT_TEMP_SEL	EXT_TEMP_R_SEL		EXT_TEMP_SEL			BVM_SEL		PCVM_SEL		

| | | | | r | | | | | | | | rw | rw | rw | rw | | rw | | | rw | | rw | | | |

Field	Bits	Type	Description
PCVM_SEL	3:0	rw	**Selects which PCVM results are part of the multiread** No PCVM result for 1101$_B$...1111$_B$ 0$_H$ **NO_PCVM**: No PCVM result (default) 1$_H$ **RES_CELL_11**: Only result for cell 11 2$_H$ **RES_CELL_11_10**: Result of Cell 11-10 3$_H$ **RES_CELL_11_9**: Result of Cell 11-9 C$_H$ **RES_CELL_11_0**: Result of Cell 11-0
BVM_SEL	4	rw	**Selects if BVM result is part of multiread** 0$_B$ **NO_RESULT**: No BVM result (default) 1$_B$ **RESULT**: Result of BVM
EXT_TEMP_SEL	7:5	rw	**Selects which TEMP result is part of the multiread** 000$_B$ **NO_TEMP**: No TEMP result (default) 001$_B$ **RES_TMP0**: Result of TEMP_0 010$_B$ **RES_TMP0_1**: Result of TEMP_0 & TEMP_1 011$_B$ **RES_TMP0_2**: Result of TEMP_0 & TEMP_1 & TEMP_2 100$_B$ **RES_TMP0_3**: Result of TEMP_0 & TEMP_1 & TEMP_2 & TEMP_3 101$_B$ **RES_TMP0_4**: Result of TEMP_0 & TEMP_1 & TEMP_2 & TEMP_3 & TEMP_4
EXT_TEMP_R_SEL	8	rw	**Selects if R_DIAG result is part of the multiread** 0$_B$ **NO_R_DIAG_RES**: No R_DIAG result (default) 0$_B$ **R_DIAG_RES**: Result of R_DIAG
INT_TEMP_SEL	9	rw	0$_B$ **NO_INT_TMP_RES**: No INT_TEMP result (default) 1$_B$ **INT_TMP_RES**: Result of INT_TEMP
SCVM_SEL	10	rw	**Selects if SCVM results are part of the multiread** 0$_B$ **NO_RESULT**: No SCVM result (default) 1$_B$ **RESULT**: Result of SCVM_HIGH and SCVM_LOW
STRESS_PCVM_SEL	11	rw	**Selects if PCVM stress correction value is part of the multiread** 0$_B$ **NO_RESULT**: No STRESS_PCVM result (default) 1$_B$ **RESULT**: Result of STRESS_PCVM

4.38 Passive balancing diagnostics OVERCURRENT

BAL_DIAG_OC

Passive balancing diagnostics OVERCURRENT

Offset address: 0033$_H$

Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				OC_11	OC_10	OC_9	OC_8	OC_7	OC_6	OC_5	OC_4	OC_3	OC_2	OC_1	OC_0
				rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw

Field	Bits	Type	Description
OC_i (i=0-11)	i	rocw	**Balancing overcurrent in cell i** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0$_B$ **NO_OC**: No balancing overcurrent detected in respective cell (default) 1$_B$ **OC**: Balancing overcurrent detected in respective cell. Balancing is deactivated for this cell.

4.39 Passive balancing diagnostics UNDERCURRENT

BAL_DIAG_UC Offset address: 0034$_H$

Passive balancing diagnostics UNDERCURRENT Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				UC_11	UC_10	UC_9	UC_8	UC_7	UC_6	UC_5	UC_4	UC_3	UC_2	UC_1	UC_0
				rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw

Field	Bits	Type	Description
UC_i (i=0-11)	i	rocw	**Balancing undercurrent in cell i** Can also be cleared on write '0' to connected GEN_DIAG register bit. 0$_B$ **NO_UC**: No balancing undercurrent detected in respective cell (default) 1$_B$ **UC**: Balancing undercurrent detected in respective cell. Balancing is deactivated for this cell.

4.40 Chip temperature 2

INT_TEMP_2

Chip temperature 2

Offset address: 0035_H

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res		VALI D	Res			RESULT									
r		rocr	r			rh									

Field	Bits	Type	Description
RESULT	9:0	rh	**Result of internal temperatur 2 measurement** SD-ADC result of internal temperature 2 measurement. 000_H **DEFAULT**: Default
VALID	13	rocr	**Indicating a valid result** 0_B **NO_NEW_RESULT**: No new result available (default) 1_B **NEW_RESULT_STORED**: A new result is stored in the register, cleared automatically after readout of the result register.

4.41　　　Configuration

CONFIG　　　　　　　　　　　　　　　　　　　　　　　Offset address:　　　　0036$_H$

Configuration　　　　　　　　　　　　　　　　　　　　　Reset value:　　　　　0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				FN	Res	EN_ALL_ADC	Res			NODE_ID					
r				rwo	r	rw	r			rwo					
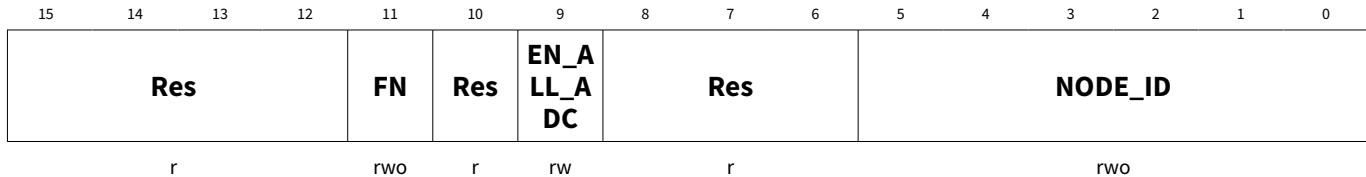
Field	Bits	Type	Description
NODE_ID	5:0	rwo	**Address (ID) of the node, distributed during enumeration** NODE_ID = 0 --> iso UART signals are not forwarded NODE_ID = 63 --> reserved for broadcast commands
EN_ALL_ADC	9	rw	**Enable all ADCs** If this bit is set, PCVM is done for each channel, independent of PART_CONFIG setup. 0$_B$　**SEL_ADC**: Only ADCs enabled which are defined in PART_CONFIG as active cell 1$_B$　**ALL_ADC**: All ADCs enabled
FN	11	rwo	**Final Node** The final node in stack must have this bit set. If final node does not have FN set, no reply frame on broadcast will be sent. 0$_B$　**NOT_FN**: Not the final node (default) 1$_B$　**FN**: Final node

Infineon

4.42 General purpose input / output

GPIO   Offset address: 0037$_H$

General purpose input / output   Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIO_UV	Res	DIR_PWM0	OUT_PWM0	PWM_PWM0	IN_PWM0	DIR_PWM1	OUT_PWM1	PWM_PWM1	IN_PWM1	DIR_GPIO1	OUT_GPIO1	IN_GPIO1	DIR_GPIO0	OUT_GPIO0	IN_GPIO0
rocw	r	rw	rw	rw	rh	rw	rw	rw	rh	rw	rw	rh	rw	rw	rh

Field	Bits	Type	Description
IN_GPIO0	0	rh	**GPIO 0 input state (ignored if communication over GPIO pins)** 0_B **LOW**: Pin reads L (default) Also active for DIR_GPIO0 =1 (reading back driven value). 1_B **HIGH**: Pin reads H
OUT_GPIO0	1	rw	**GPIO 0 output setting (ignored if communication over GPIO pins)** 0_B **LOW**: Drive L (default) 1_B **HIGH**: Drive H
DIR_GPIO0	2	rw	**GPIO 0 direction (ignored if communication over GPIO pins)** 0_B **INPUT**: Input (output stage = HiZ) (default) 1_B **OUTPUT**: Output (output stage enabled)
IN_GPIO1	3	rh	**GPIO 1 input state (ignored if communication over GPIO pins)** 0_B **LOW**: Pin reads L (default) Also active for DIR_GPIO1 =1 (reading back driven value). 1_B **HIGH**: Pin reads H
OUT_GPIO1	4	rw	**GPIO 1 output setting (ignored if communication over GPIO pins)** 0_B **LOW**: Drive L (default) 1_B **HIGH**: Drive H
DIR_GPIO1	5	rw	**GPIO 1 direction (ignored if communication over GPIO pins)** 0_B **INPUT**: Input (output stage = HiZ) (default) 1_B **OUTPUT**: Output (output stage enabled)
IN_PWM1	6	rh	**PWM 1 input state** 0_B **LOW**: Pin reads L (default) Also active for DIR_PWM1 =1 (reading back driven value). 1_B **HIGH**: Pin reads H
PWM_PWM1	7	rw	**PWM 1 enable PWM function** 0_B **DISABLE**: No PWM function (default) 1_B **ENABLE**: If DIR_PWM1 = 1, then PWM output regarding PWM_GPIO register and OUT_PWM1 is ignored. If DIR_PWM1 = 0, GPIO input and no PWM function.

(table continues…)

(continued)

Field	Bits	Type	Description
OUT_PWM1	8	rw	**PWM 1 output setting** 0_B **LOW**: Drive L (default) 1_B **HIGH**: Drive H
DIR_PWM1	9	rw	**PWM 1 direction** 0_B **INPUT**: Input (output stage = HiZ) (default) 1_B **OUTPUT**: Output (output stage enabled)
IN_PWM0	10	rh	**PWM 0 input state** 0_B **LOW**: Pin reads L (default) Also active for DIR_PWM0 =1 (reading back driven value). 1_B **HIGH**: Pin reads H
PWM_PWM0	11	rw	**PWM 0 enable PWM function** 0_B **DISABLE**: No PWM function (default) 1_B **ENABLE**: If DIR_PWM0= 1, then PWM output regarding PWM_GPIO register and OUT_PWM0 is ignored. If DIR_PWM0= 0, GPIO input and no PWM function.
OUT_PWM0	12	rw	**PWM 0 Output Setting** 0_B **LOW**: Drive L (default) 1_B **HIGH**: Drive H
DIR_PWM0	13	rw	**PWM 0 direction** 0_B **INPUT**: Input (output stage = HiZ) (default) 1_B **OUTPUT**: Output (output stage enabled)
VIO_UV	15	rocw	**VIO undervoltage error** 0_B **NO_ERR**: No VIO undervoltage error (default) 1_B **ERR**: VIO undervoltage error occurred

4.43 PWM settings

GPIO_PWM Offset address: 0038$_H$

PWM settings Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res			**PWM_PERIOD**					**Res**			**PWM_DUTY_CYCLE**				
r			rw					r			rw				

Field	Bits	Type	Description
PWM_DUTY_CYCLE	4:0	rw	**PWM duty cycle** 0 - 100% 00$_H$ **OFF**: No PWM (default) 01$_H$ **3_5**: 3.57% 02$_H$ **7_1**: 7.14% 1C$_H$ **100**: 100% 1F$_H$ **100_**: 100%
PWM_PERIOD	12:8	rw	**PWM period time setting** 2µs - 62µs 00$_H$ **OFF**: No PWM (default) 01$_H$ **2us**: 2µs 02$_H$ **4us**: 4 µs 1F$_H$ **62us**: 62µs

4.44 IC version and manufacturing ID

ICVID   Offset address: 0039$_H$

IC version and manufacturing ID   Reset value: C140$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MANUFACTURER_ID								VERSION_ID							
rh								rh							
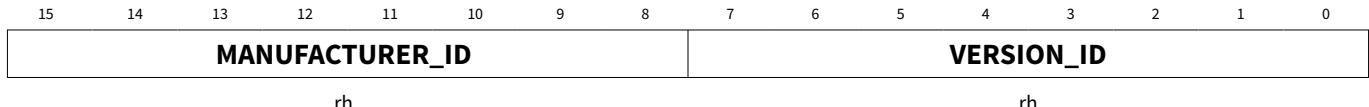
Field	Bits	Type	Description
VERSION_ID	7:0	rh	**Version ID** Read only version ID. 40$_H$ **DEFAULT**: Default
MANUFACTUR ER_ID	15:8	rh	**Manufacturer ID** Read only manufacture ID. C1$_H$ **DEFAULT**: Default

4.45   Mailbox register

MAILBOX   Offset address: 003A$_H$
Mailbox register   Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							DATA								

rw
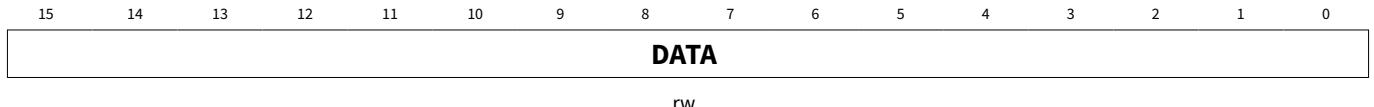
Field	Bits	Type	Description
DATA	15:0	rw	**Data storage register** 2 data byte data storage

4.46 Customer ID 0

CUSTOMER_ID_0   Offset address: 003B$_H$
Customer ID 0   Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							DATA								

rh
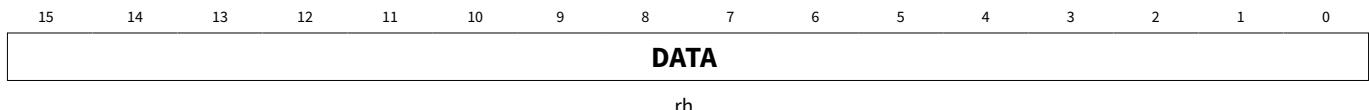
Field	Bits	Type	Description
DATA	15:0	rh	**Unique ID part 1**

## 4.47 Customer ID 1

CUSTOMER_ID_1   Offset address: 003C$_H$
Customer ID 1   Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																

rh
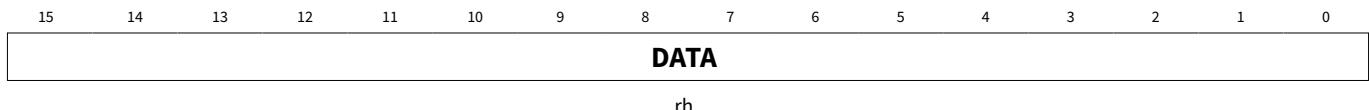
Field	Bits	Type	Description
DATA	15:0	rh	**Unique ID part 2**

4.48 Watchdog counter

WDOG_CNT

Watchdog counter

Offset address: 003D$_H$

Reset value: 007F$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAIN_CNT									WD_CNT						
rh									rwh						
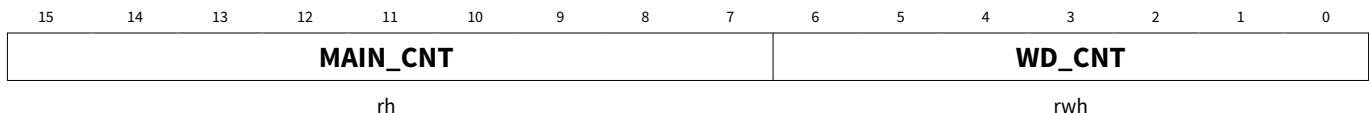
Field	Bits	Type	Description
WD_CNT	6:0	rwh	**Watchdog counter** 00$_H$ **SLEEP**: Device goes to sleep 01$_H$ **1**: tWD_LSB (EXT_WD = 0) / tWD_EXT_LSB (EXT_WD = 1) 7F$_H$ **127**: tWD_LSB * 127 (EXT_WD = 0) / tWD_EXT_LSB * 127 (EXT_WD = 1) (default)
MAIN_CNT	15:7	rh	**Main counter** Used to enable host controller to measure the main oscillator frequency. LSB = t_{Count_LSB}. Reset by write access to WD_CNT if RR_SYNC=1. 000$_H$ **DEFAULT**: Default

4.49 SCVM configuration

SCVM_CONFIG

SCVM configuration

Offset address:

Reset value:

003E$_H$

0FFF$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				EN_S CVM 11	EN_S CVM 10	EN_S CVM 9	EN_S CVM 8	EN_S CVM 7	EN_S CVM 6	EN_S CVM 5	EN_S CVM 4	EN_S CVM 3	EN_S CVM 2	EN_S CVM 1	EN_S CVM 0
				rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
EN_SCVMi (i=0-11)	i	rw	**Enable SCVM for cell i** 0$_B$ **DIS**: SCVM disabled 1$_B$ **EN**: SCVM enabled (default)

4.50 Stress correction AUX

STRESS_AUX   Offset address: 003F$_H$

Stress correction AUX   Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STRESS_CORRECTION																

rh

Field	Bits	Type	Description
STRESS_CORRECTION	15:0	rh	**Stress correction value PCVM** 0000$_H$ **DEFAULT**: Default

4.51 Balancing PWM

BAL_PWM   Offset address: 005B$_H$

Balancing PWM   Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						Res								BAL_PWM	
						r								rw	
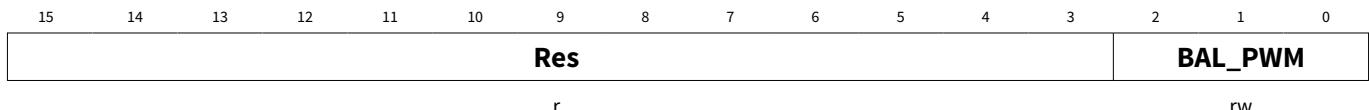
Field	Bits	Type	Description
BAL_PWM	2:0	rw	**PWM balancing, starts with off-phase** 000$_B$ **VAL_0**: 100% duty cycle (function disabled) 001$_B$ **VAL_1**: 87,5% duty cycle 111$_B$ **VAL_7**: 12.5% duty cycle

4.52　　Balancing counter register 0

BAL_CNT_0　　　　　　　　　　　　　　　　　　　Offset address:　　　　005C$_H$
Balancing counter register 0　　　　　　　　　　　Reset value:　　　　　0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	BAL_CNT_2					BAL_CNT_1					BAL_CNT_0				
r	rw					rw					rw				

Field	Bits	Type	Description
BAL_CNT_0	4:0	rw	**Balancing counter to switch off balancing after a certain time, counter is (re-)started by a write access to WDOG_CNT when EXT_WD=1.** 01$_H$　**VAL_1**: 7.5 min 1F$_H$　**VAL_31**: 3.87 h
BAL_CNT_1	9:5	rw	**Balancing counter to switch off balancing after a certain time, counter is (re-)started by a write access to WDOG_CNT when EXT_WD=1.** 01$_H$　**VAL_1**: 7.5 min 1F$_H$　**VAL_31**: 3.87 h
BAL_CNT_2	14:10	rw	**Balancing counter to switch off balancing after a certain time, counter is (re-)started by a write access to WDOG_CNT when EXT_WD=1.** 01$_H$　**VAL_1**: 7.5 min 1F$_H$　**VAL_31**: 3.87 h

4.53 Balancing counter register 1

BAL_CNT_1

Offset address: 005D$_H$

Balancing counter register 1

Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res		BAL_CNT_5					BAL_CNT_4					BAL_CNT_3			
r		rw					rw					rw			

Field	Bits	Type	Description
BAL_CNT_3	4:0	rw	**Balancing counter to switch off balancing after a certain time, counter is (re-)started by a write access to WDOG_CNT when EXT_WD=1.** 01$_H$ **VAL_1**: 7.5 min 1F$_H$ **VAL_31**: 3.87 h
BAL_CNT_4	9:5	rw	**Balancing counter to switch off balancing after a certain time, counter is (re-)started by a write access to WDOG_CNT when EXT_WD=1.** 01$_H$ **VAL_1**: 7.5 min 1F$_H$ **VAL_31**: 3.87 h
BAL_CNT_5	14:10	rw	**Balancing counter to switch off balancing after a certain time, counter is (re-)started by a write access to WDOG_CNT when EXT_WD=1.** 01$_H$ **VAL_1**: 7.5 min 1F$_H$ **VAL_31**: 3.87 h

4.54 Balancing counter register 2

BAL_CNT_2   Offset address: 005E$_H$

Balancing counter register 2   Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	BAL_CNT_8					BAL_CNT_7					BAL_CNT_6				
r	rw					rw					rw				

Field	Bits	Type	Description
BAL_CNT_6	4:0	rw	**Balancing counter to switch off balancing after a certain time, counter is (re-)started by a write access to WDOG_CNT when EXT_WD=1.** 01$_H$ **VAL_1**: 7.5 min 1F$_H$ **VAL_31**: 3.87 h
BAL_CNT_7	9:5	rw	**Balancing counter to switch off balancing after a certain time, counter is (re-)started by a write access to WDOG_CNT when EXT_WD=1.** 01$_H$ **VAL_1**: 7.5 min 1F$_H$ **VAL_31**: 3.87 h
BAL_CNT_8	14:10	rw	**Balancing counter to switch off balancing after a certain time, counter is (re-)started by a write access to WDOG_CNT when EXT_WD=1.** 01$_H$ **VAL_1**: 7.5 min 1F$_H$ **VAL_31**: 3.87 h

4.55 Balancing counter register 3

BAL_CNT_3

Offset address: 005F$_H$

Balancing counter register 3

Reset value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	BAL_CNT_11					BAL_CNT_10					BAL_CNT_9				
r	rw					rw					rw				

Field	Bits	Type	Description
BAL_CNT_9	4:0	rw	**Balancing counter to switch off balancing after a certain time, counter is (re-)started by a write access to WDOG_CNT when EXT_WD=1.** 01$_H$ **VAL_1**: 7.5 min 1F$_H$ **VAL_31**: 3.87 h
BAL_CNT_10	9:5	rw	**Balancing counter to switch off balancing after a certain time, counter is (re-)started by a write access to WDOG_CNT when EXT_WD=1.** 01$_H$ **VAL_1**: 7.5 min 1F$_H$ **VAL_31**: 3.87 h
BAL_CNT_11	14:10	rw	**Balancing counter to switch off balancing after a certain time, counter is (re-)started by a write access to WDOG_CNT when EXT_WD=1.** 01$_H$ **VAL_1**: 7.5 min 1F$_H$ **VAL_31**: 3.87 h

Revision history

Revision	Date	Changes
1.0	2022-01-24	Initial release

Trademarks

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