

Infineon Power Solutions for Xilinx Zynq UltraScale+ MPSoC

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Advanced Information



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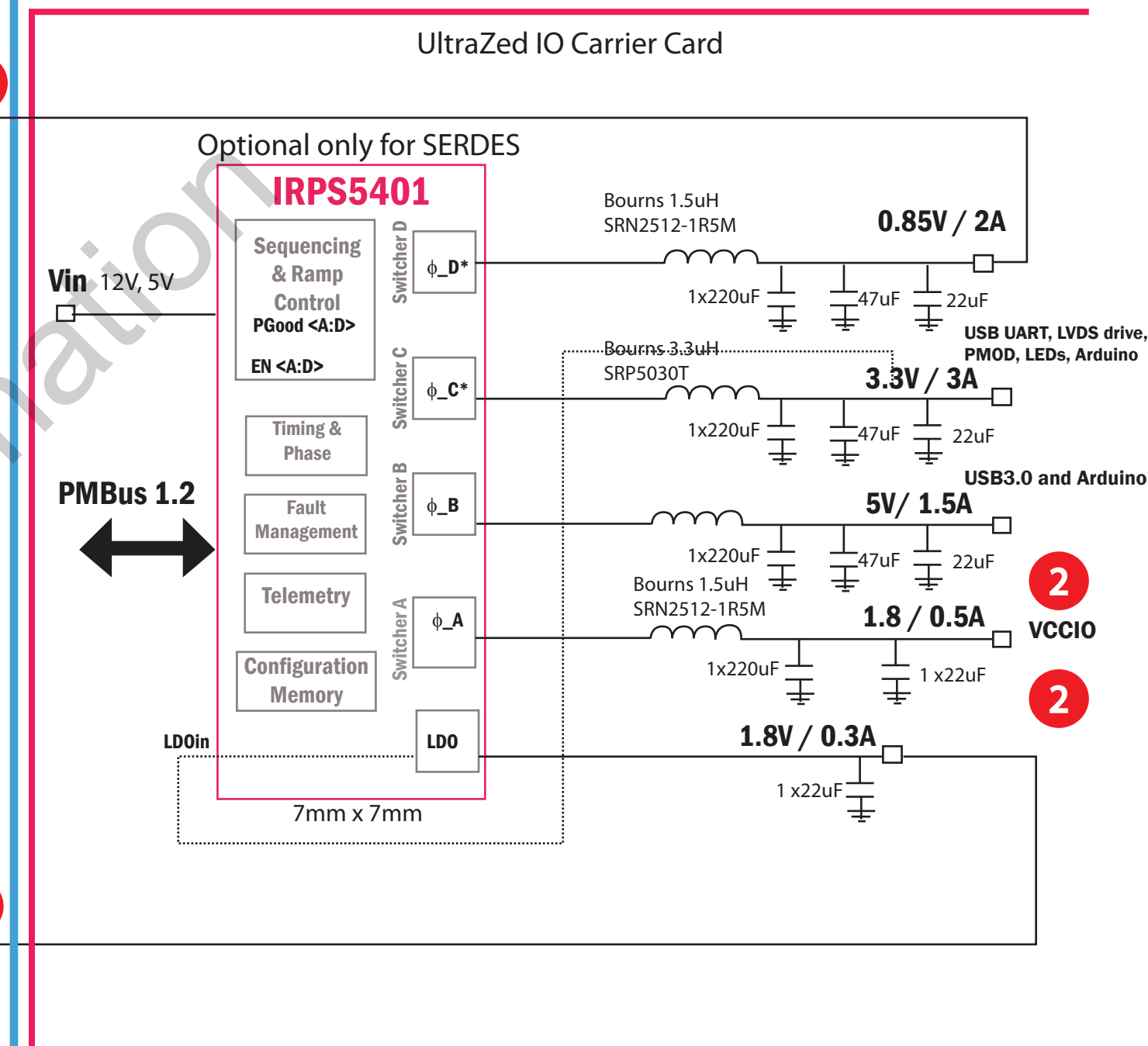
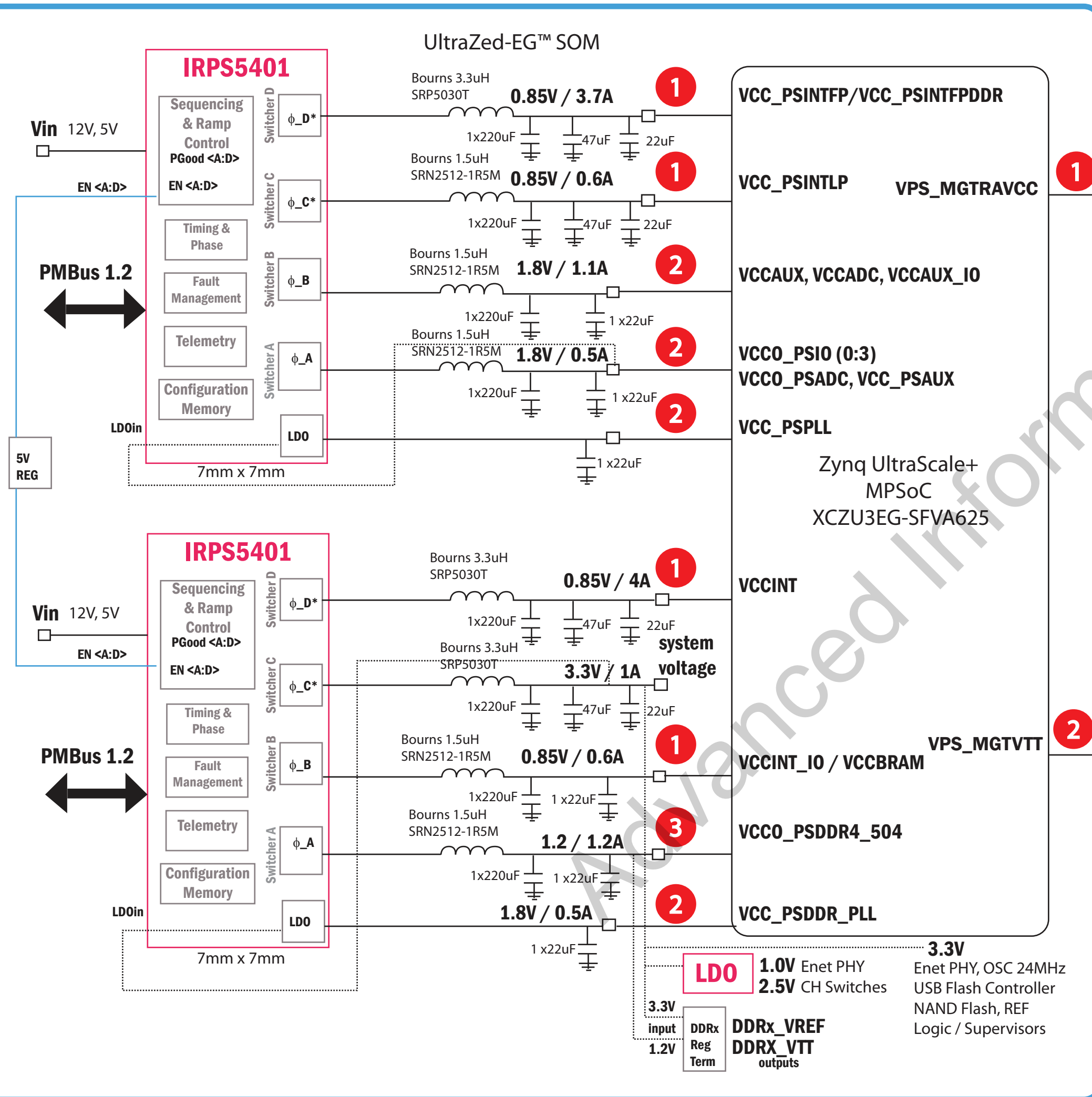
Introduction

- › Infineon power solutions focusing on tight board space applications
- › Featuring 5 output PMIC, IRPS5401
- › Power solutions for Xilinx Zynq Ultrascale+ MPSoC from Zu02 to Zu19
- › Power maps are optimized for power rail consolidation
- › Sequencing for power up and power down shown with delay estimates
- › Infineon power solutions provide scalable power for core voltage vs. Zynq Ultrascale+ MPSoC family
- › PCB board size estimates provided. Usually the size estimate provide fits the largest power stage and Cout
- › Estimated values for inductors and output capacitors based upon Xilinx DC, AC and voltage ripple requirements
- › IRPS5401 digital compensation values calculated for Xilinx power requirements vs. L vs. C.

Infinion Power Solution for Xilinx
Zynq UltraScale+ MPSoC
Zu03_Zu02

Flexible Mode: Always on - Cost Optimized
Always on - Efficiency Optimized, and Full Power / Low Power Mode Capable

<http://zedboard.org/product/ultrazed-EG>



The Zynq UltraScale+ power rails can be turned ON/OFF for LP (low power) or FP (full power modes) via IRPS5401 PMBus or if desired via Enables.

	Power Mode	
SOM	LP	FP
VCCPSINTLP	on	on
VCCPSINTFP	off	on
VCCINT_IO / VCCBRAM	off	on
VCCINT	off	on
VCCPSAUX / VCCPSIO (0:2:3) / PSBATT	on	on
VCCPLL	on	on
VCCDDR / VCCO / DDR4 devices	off	on
VCCAUX / AUX_IO / VCCO / ENET PHY	off	on
VCCO	off	on
VCCO / ENET PHY	off	on
VTERM	off	on
ENET PHY	off	on

- Power sequencing initiated by 5V Enable/Disabled to all IRPS5401's
- All regulators and LDO is turned on/off via internal settable timers integrated into the IRPS5401 PMICs.
- No external sequencing components are required.
- Power Off is the reverse order.

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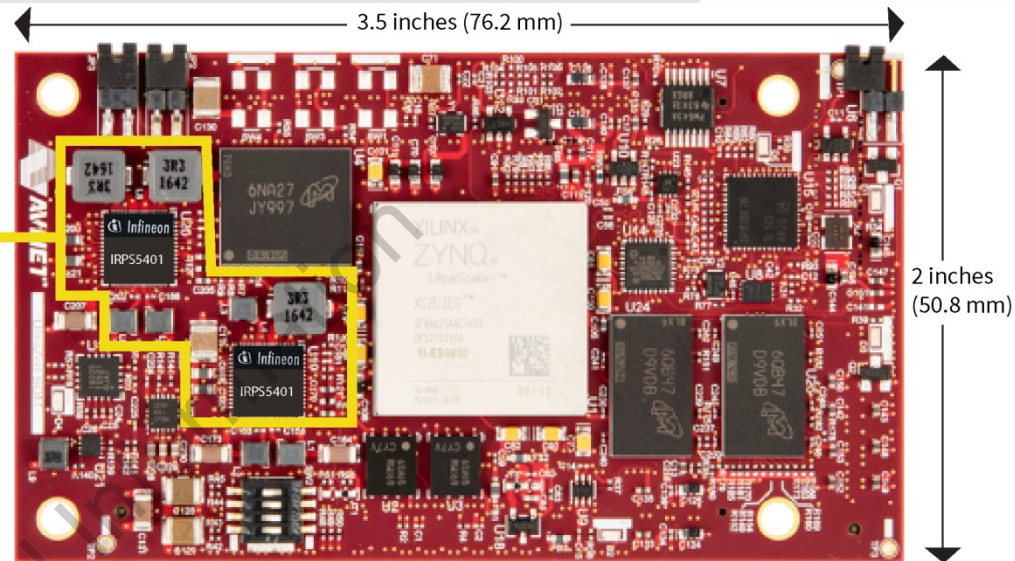
Reference Design Example:

Zynq MPSoC Ultrascale+, Zu02/Zu03



<http://zedboard.org/product/ultrazed-EG>

Infineon
Compact
Power
Design for
FPGA/SoCs,
IRPS5401

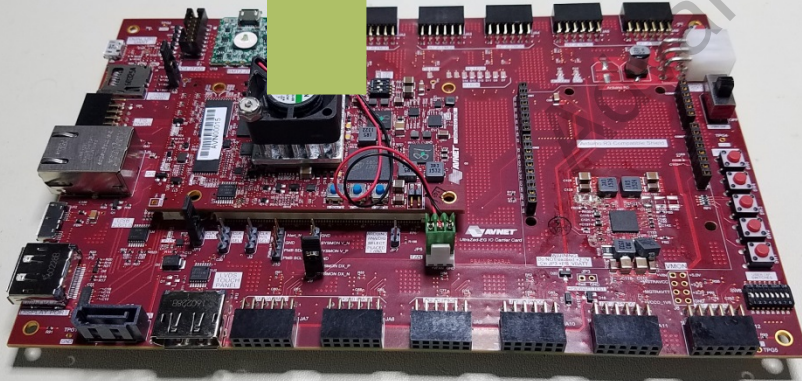


DESIGN NOTES

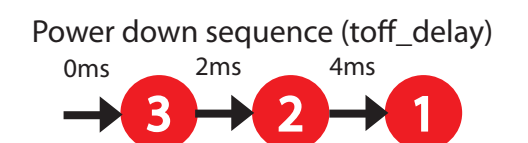
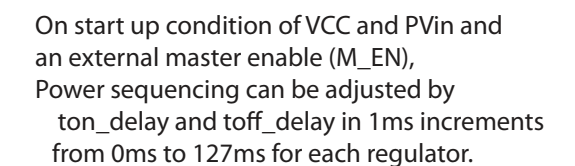
1) 3 x IRPS5401 5 output PMICs
PMBus Capable. 15 outputs.

2) Zynq Ultra Scale SOM & Carrier Card

Lower current Zynq Ultra Scale+ Series
examples: ZUEG2, ZEUG3

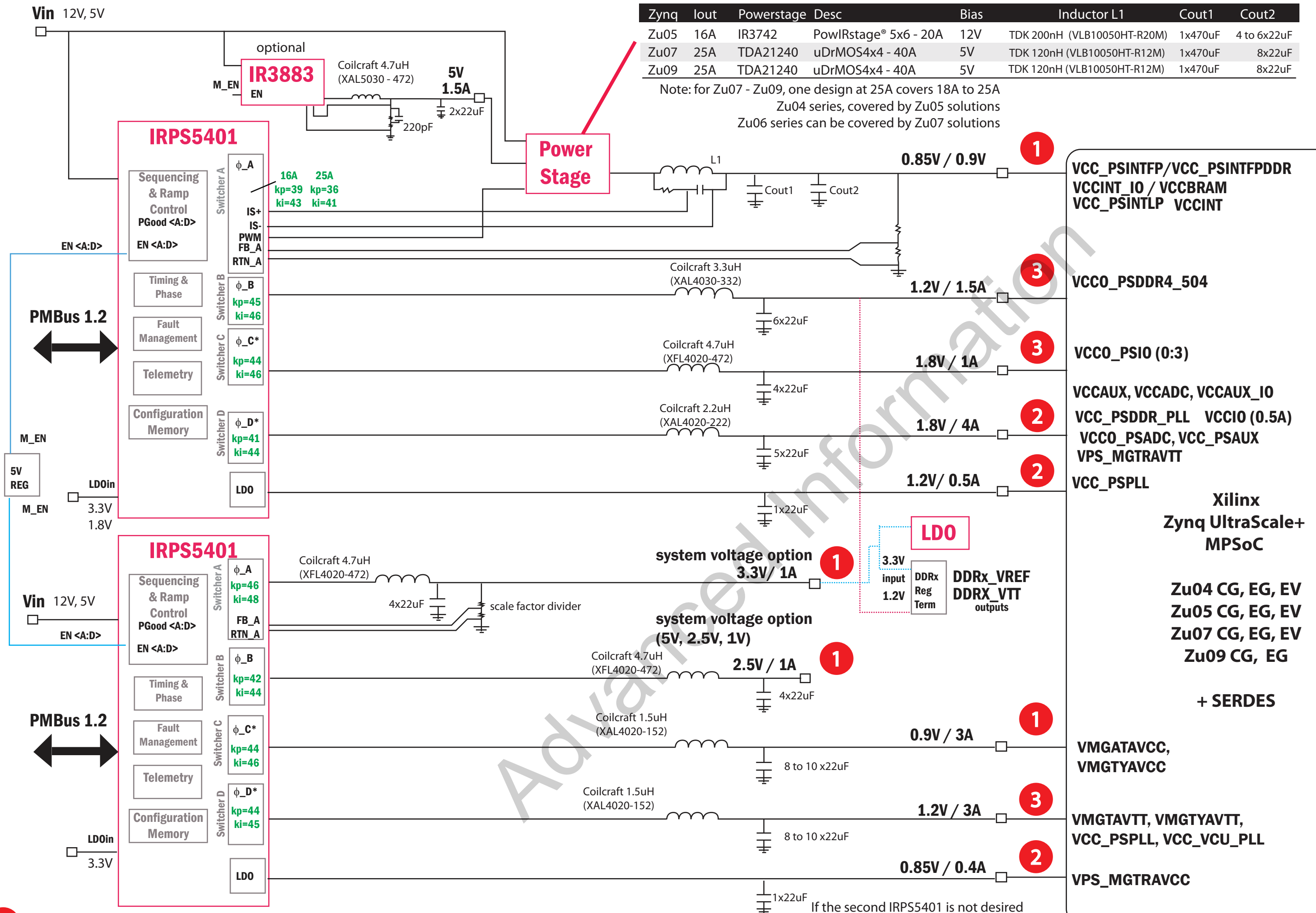


Infinion Power Solution for Xilinx Zynq UltraScale+ MPSoC

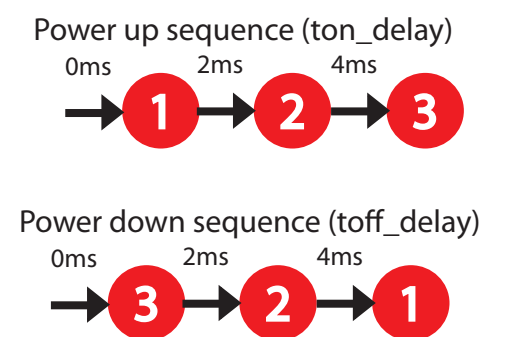


PCB space estimates:
 IRP55401 with Power Stage + L's, C's: 35mm x 40mm
 IRP55401 without Power Stage + L's, C's: 30mm x 30mm
 IR3883 with L, C's: 15mm x 10mm

**Infinion Power Solution for Xilinx
Zynq UltraScale+ MPSoC**
Zu04_Zu05_Zu07_Zu09 CG EG EV Series - **with SERDES**
Always On: Cost-Optimized Power Rail Consolidation



On start up condition of VCC and PVin and an external master enable (M_EN), Power sequencing can be adjusted by ton_delay and toff_delay in 1ms increments from 0ms to 127ms for each regulator.



**Xilinx
Zynq UltraScale+
MPSoC**

**Zu04 CG, EG, EV
Zu05 CG, EG, EV
Zu07 CG, EG, EV
Zu09 CG, EG**

+ SERDES

**VMGATAVCC,
VMGTAVCC**

**VMGTAVTT, VMGTAVTT,
VCC_PSPLL, VCC_VCU_PLL**

VPS_MGTRAVCC

Power sequencing initiated by 5V Enable/Disabled to all IRPS5401's
All regulators and LDO is turned on/off via internal settable timers integrated into the IRPS5401 PMICs.
No external sequencing components are required.
Power Off is the reverse order.

The IRPS5401 regulators do not require external loop compensation components.
The digital compensation kp, ki listed are estimations for the target regulation and may require adjustment.

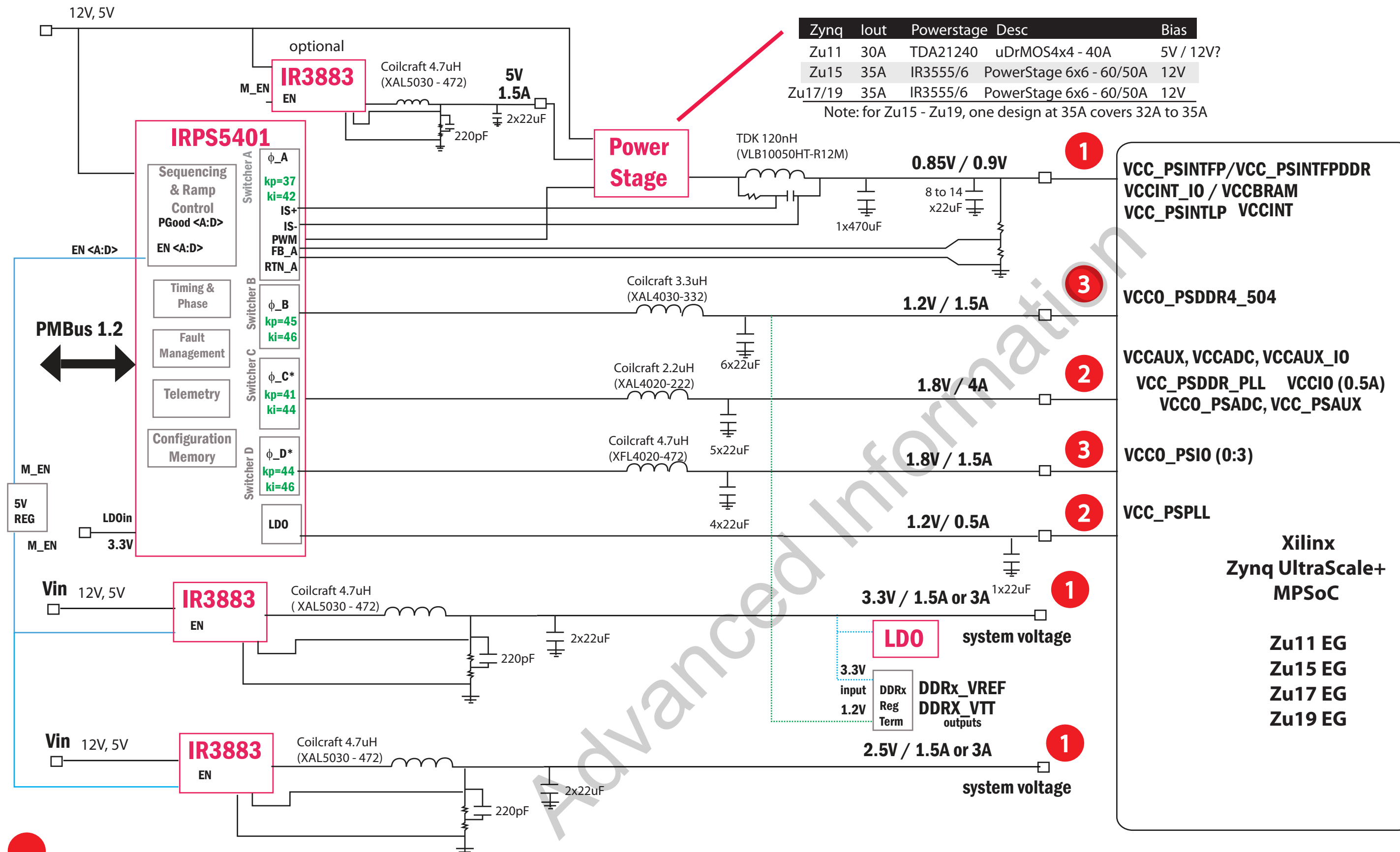
- If the second IRPS5401 is not desired the below are regulator options for SERDES:
- 1) IR3891 Dual 1.2V/1.8V or 0.9V/0.85V for VMGATAVCC, and VMGTAVTT
 - 2) IR3823 for any SERDES < 3A

If more 3.3V system voltage and higher current: 1.5A/3A, 3.3V IR3883

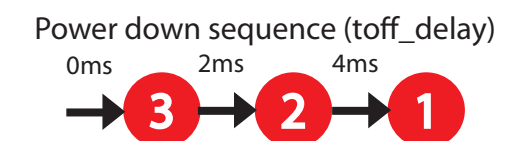
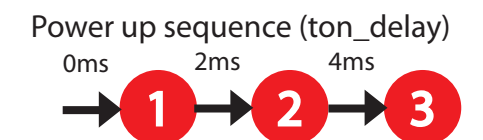
PCB space estimates:

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IRPS5401 without Power Stage + L's, C's: 30mm x 30mm
IR3883 with L, C's: 15mm x 10mm

Infineon Power Solution for Xilinx Zynq UltraScale+ MPSoC Zu11_Zu15_Zu17_Zu19 EG Series - **No SERDES** Always On: Cost-Optimized Power Rail Consolidation



On start up condition of VCC and PVin and an external master enable (M_EN), Power sequencing can be adjusted by ton_delay and toff_delay in 1ms increments from 0ms to 127ms for each regulator.



**Xilinx
Zynq UltraScale+
MPSoC**

**Zu11 EG
Zu15 EG
Zu17 EG
Zu19 EG**

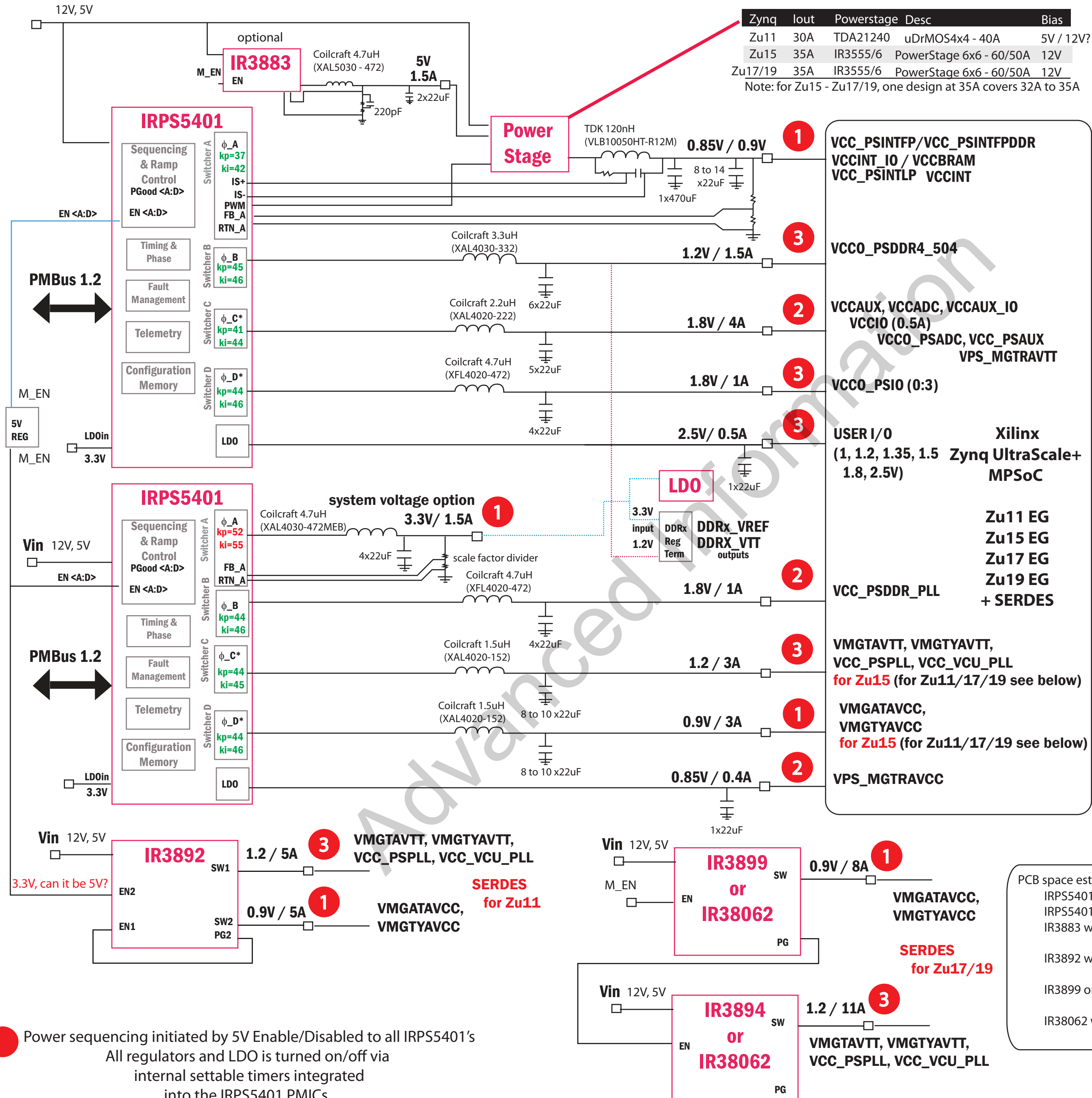
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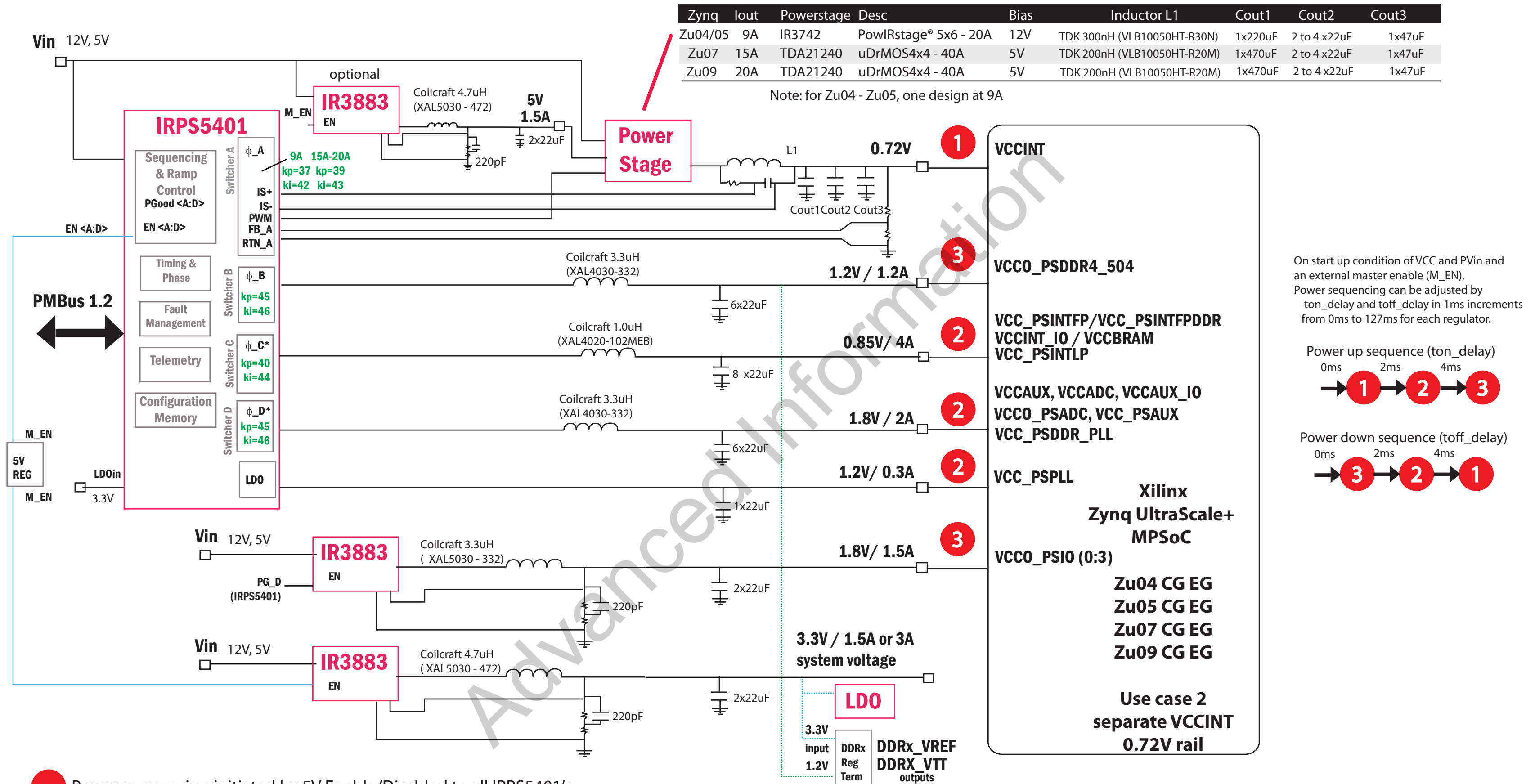
Infineon Power Solution for Xilinx Zynq UltraScale+ MPSoC Zu11_Zu15_Zu17_Zu19 EG Series - **with SERDES** Always On: Cost-Optimized Power Rail Consolidation



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Infineon Power Solution for Xilinx
Zynq UltraScale+ MPSoC
Zu04_Zu05_Zu07_Zu09 CG EG Series - No SERDES
Always On: Power and/or Efficiency-Optimized Power Rail Consolidation



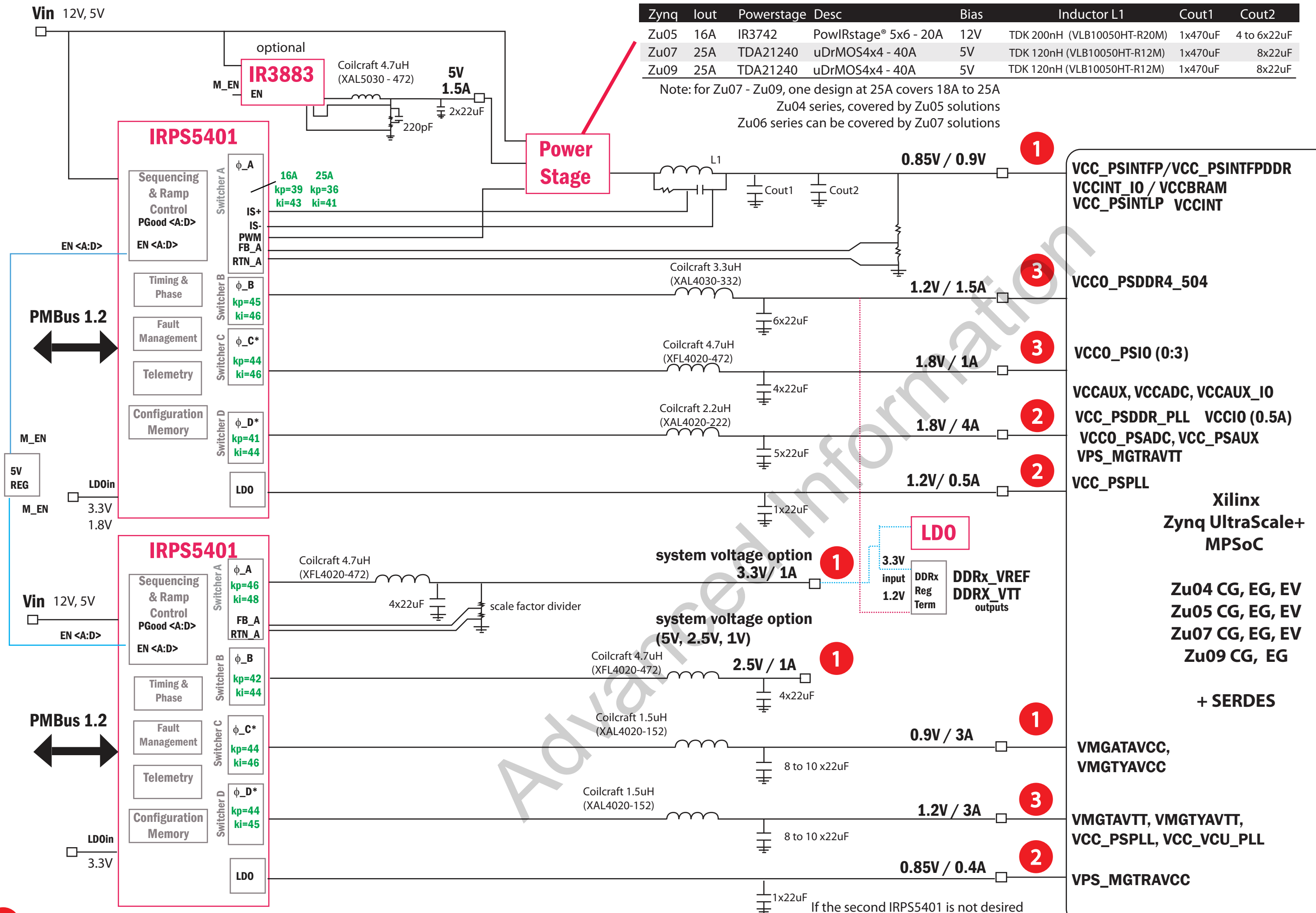
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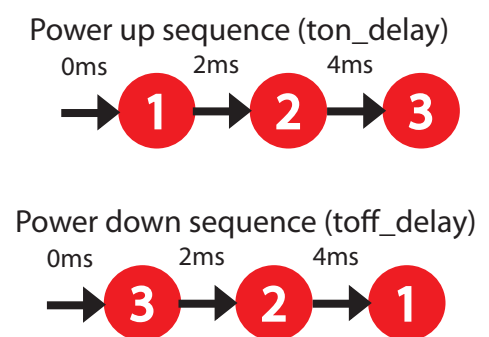
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Infineon Power Solution for Xilinx
Zynq UltraScale+ MPSoC
Zu04_Zu05_Zu07_Zu09 CG EG EV Series - **with SERDES**
Always On: Cost-Optimized Power Rail Consolidation



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**Xilinx
Zynq UltraScale+
MPSoC**

**Zu04 CG, EG, EV
Zu05 CG, EG, EV
Zu07 CG, EG, EV
Zu09 CG, EG**

+ SERDES

**VMGATAVCC,
VMGTAVCC**

**VMGTAVTT, VMGTAVTT,
VCC_PSPLL, VCC_VCU_PLL**

VPS_MGTRAVCC

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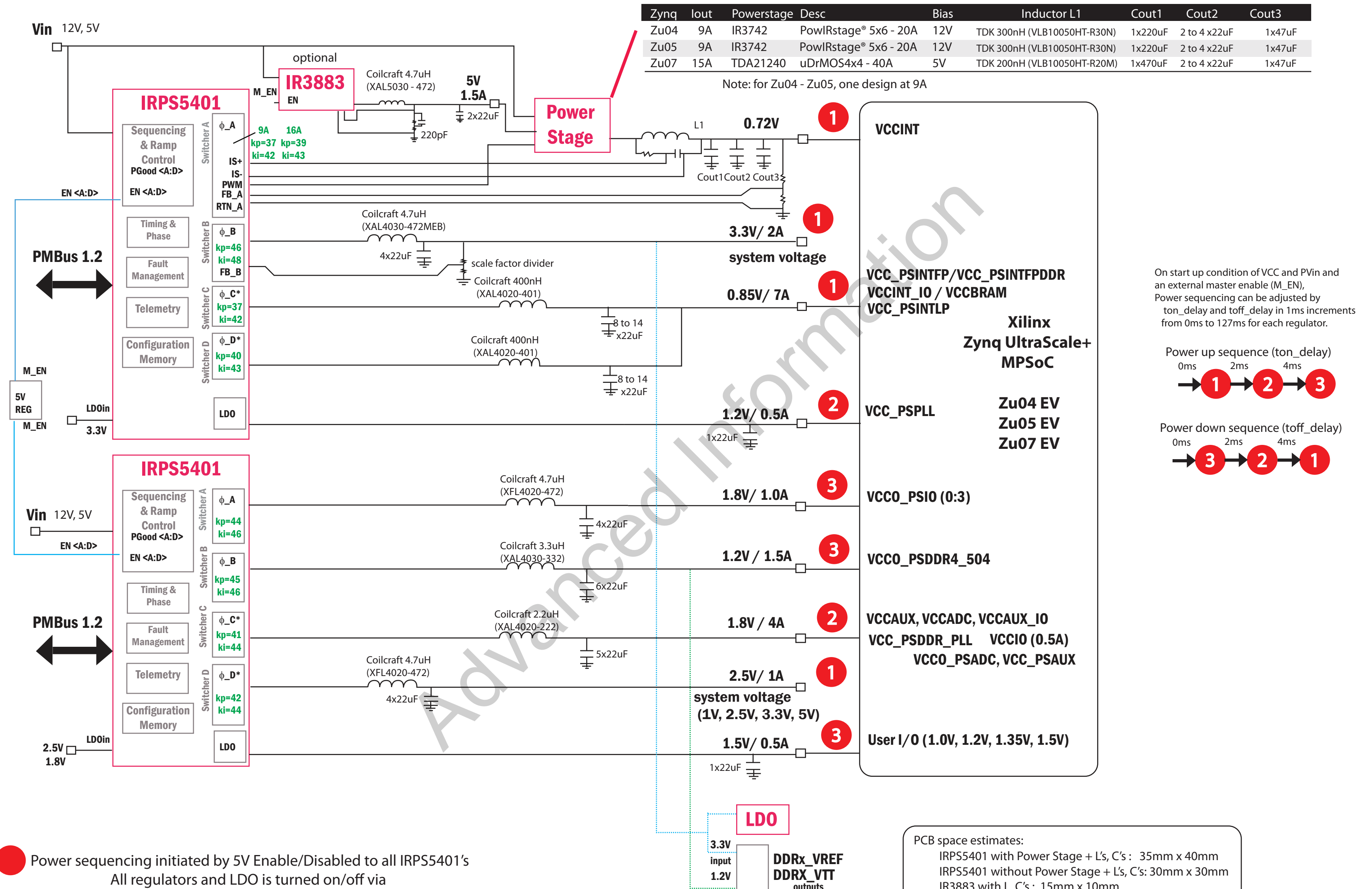
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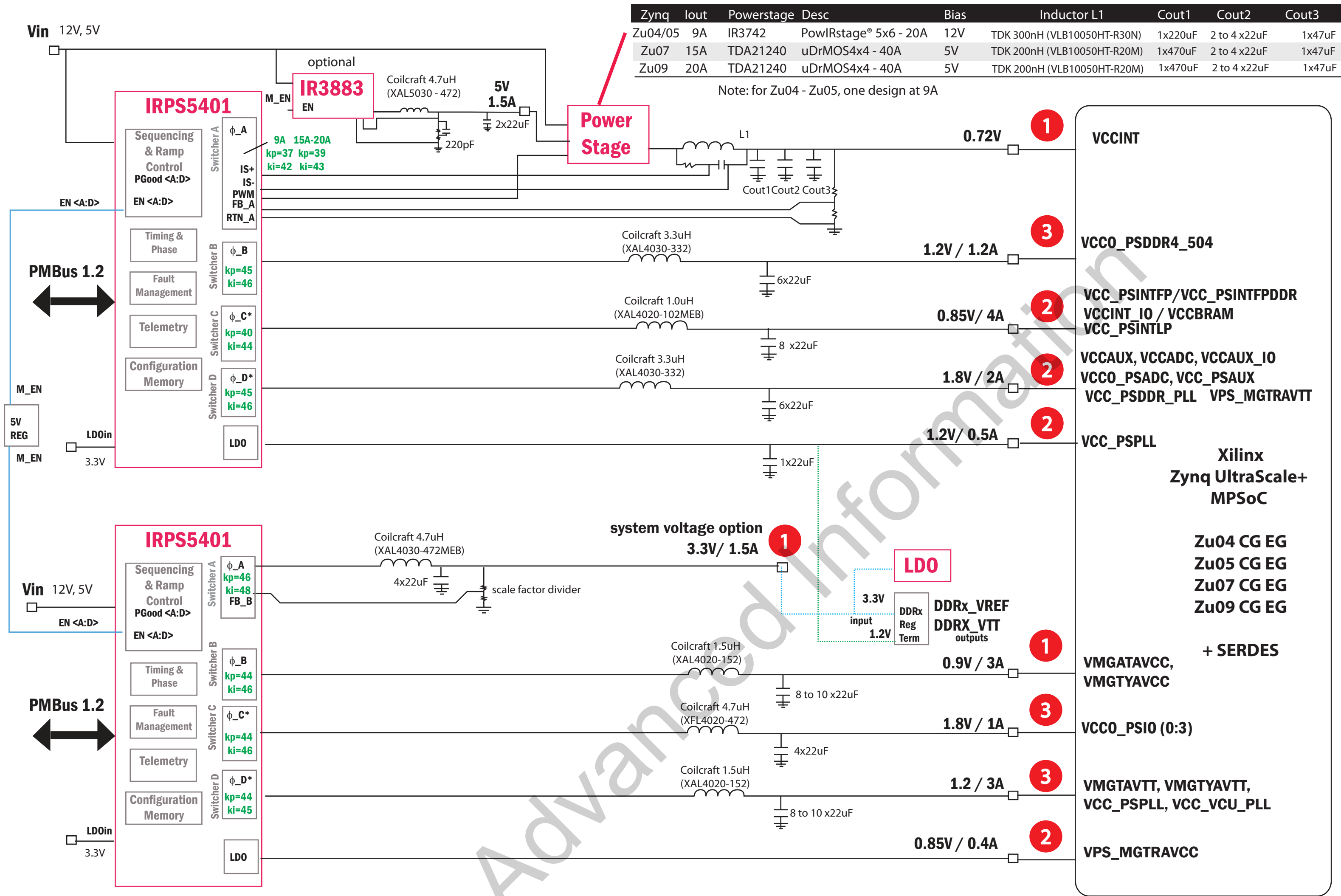
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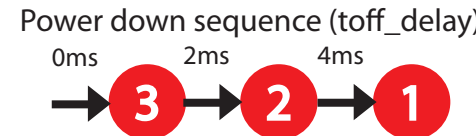
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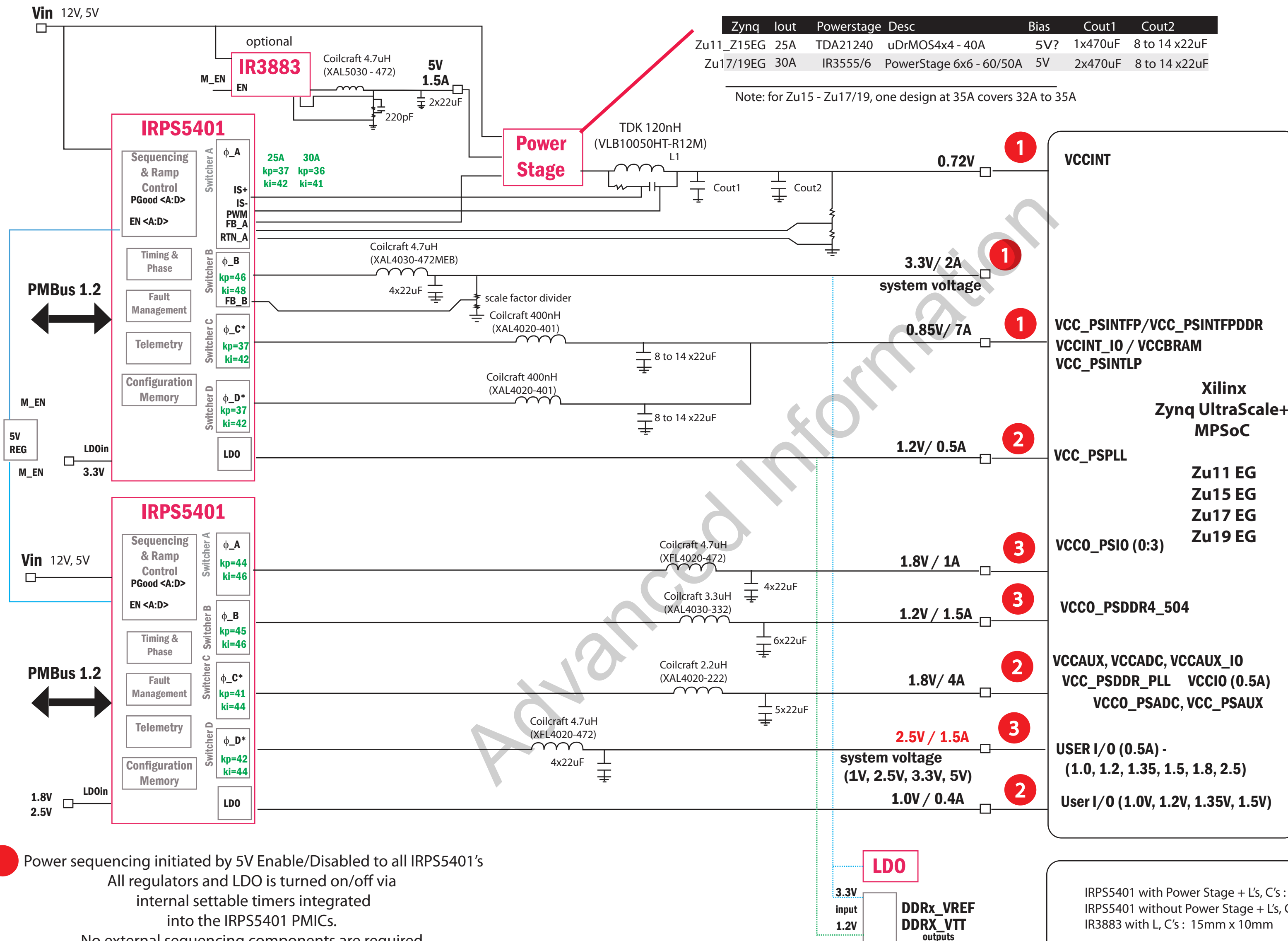
For second IRPS5401, if board ambient >50C and no airflow consider external 3.3V Regulator (IR3883)

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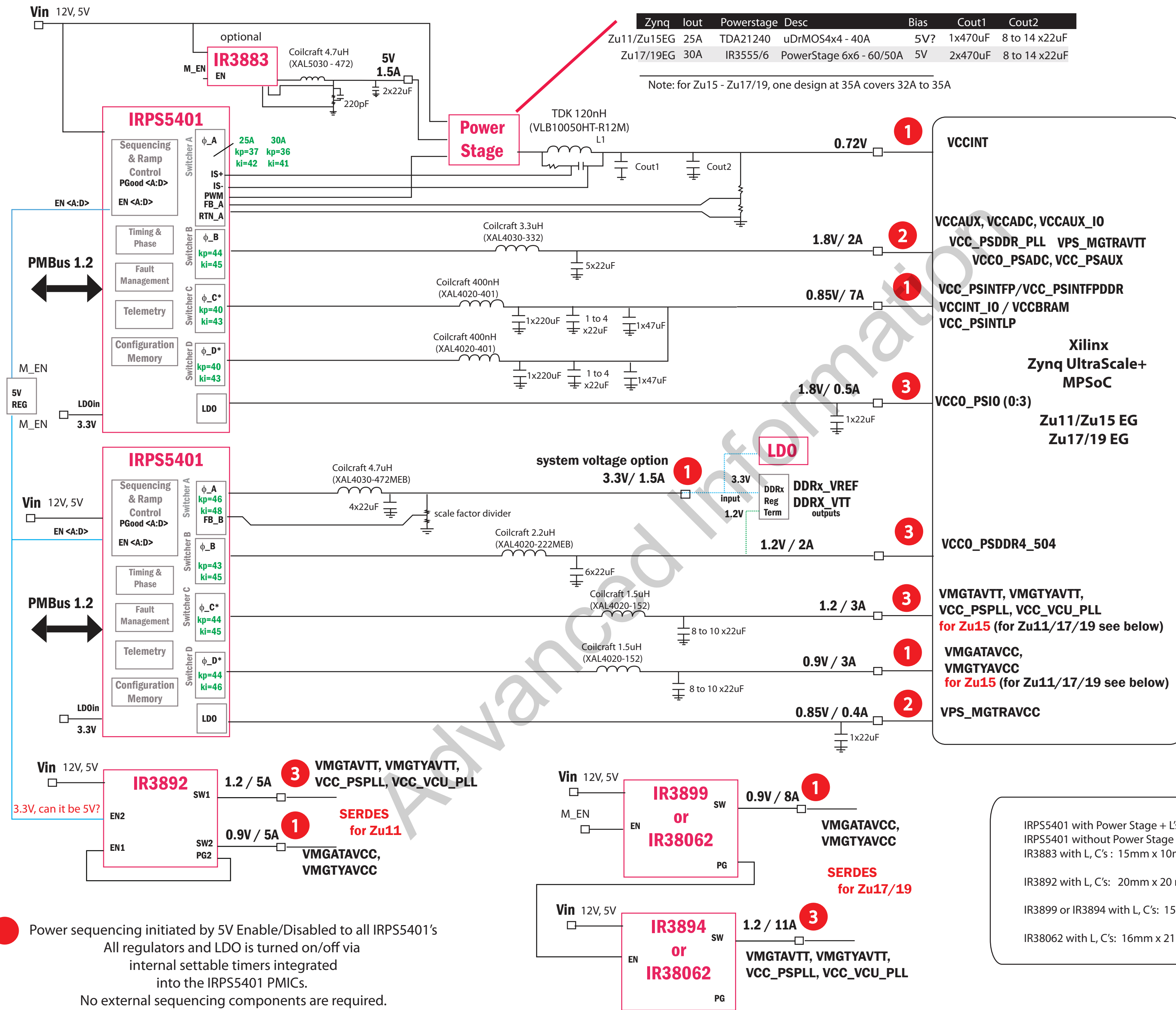
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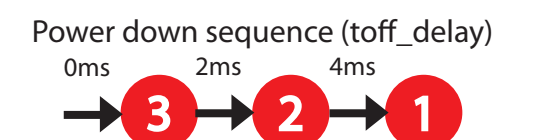
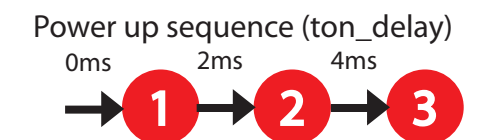
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If additional 3.3V required: 1.5A/3A - IR3883





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