Infineon Power Cookbook
DC-DC Power Solutions for FPGAs:

Xilinx Zynq UltraScale+ MPSoC

revision 0.1

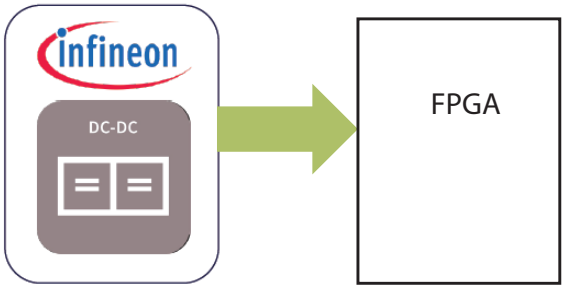
Solution Brief

DC-DC Power Solutions for FPGAs

Infineon Power for Xilinx Zynq UltraScale+ MPSoC

Infineon offers Scalable Solutions for SoC

Infineon offers scalable power solutions for Xilinx Zynq UltraScale from Zu02 to Zu19 for the CG, EG and EV series featuring our new Multi-output PMIC, IRPS5401.



Highlights

> IRPS5401 5 Output DC/DC PMIC
Four Regulators and LDO. Full PMBus ready
Integrated sequencer eliminates need for external controller
Full Digital compensation. No external components
Compact space design: 19.3 mm x 15mm

> IR3883 Easy COT DC/DC Regulator, 1A to 3A

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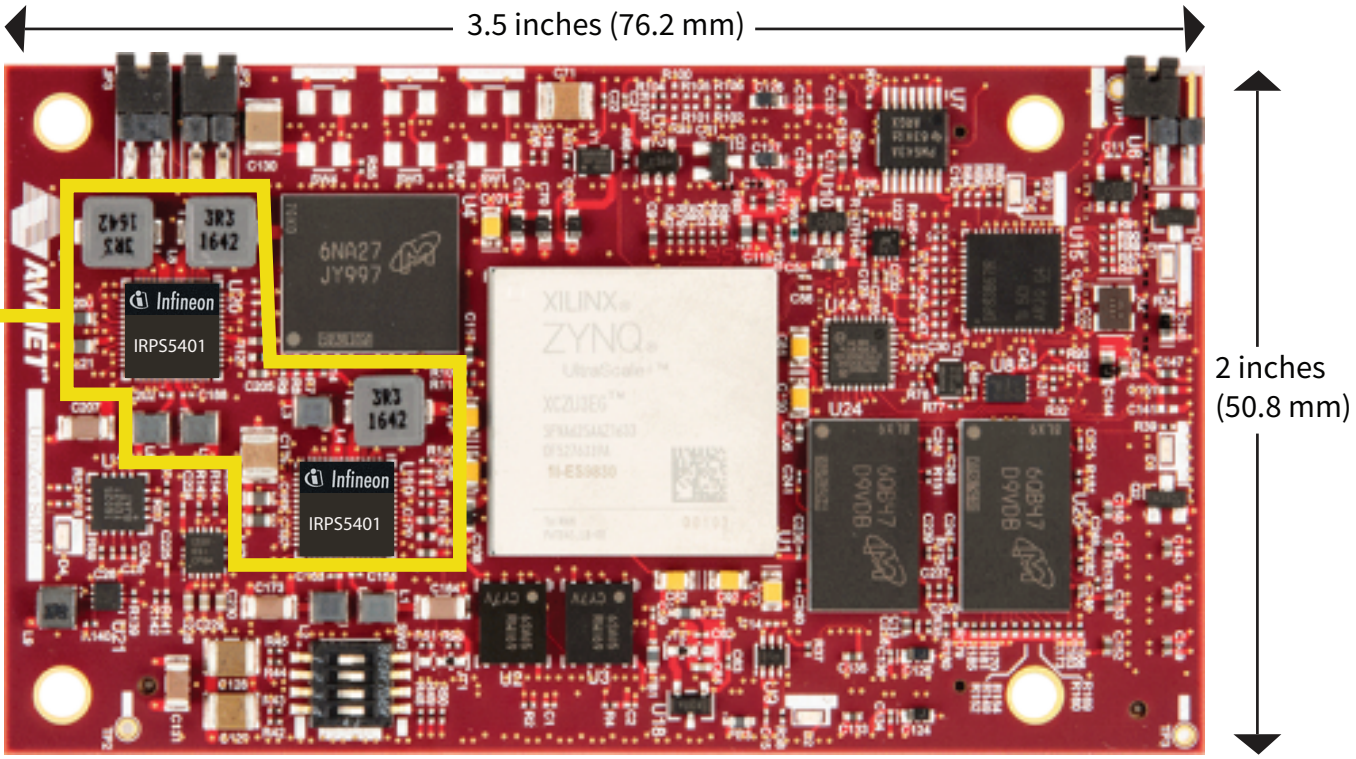

DC-DC Power Solutions for FPGAs

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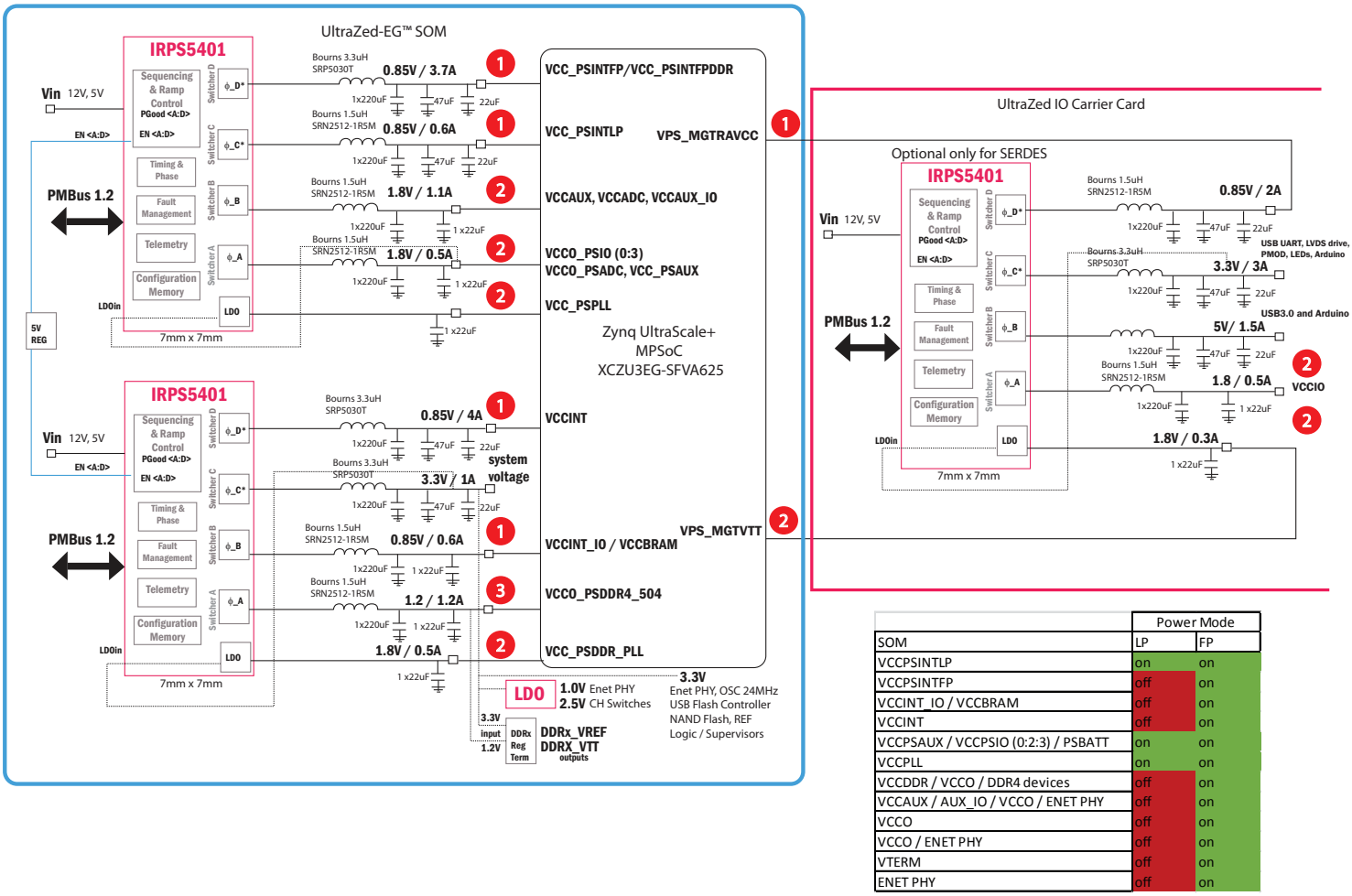
Infineon Power for Xilinx Zynq UltraScale+ MPSoC

Power Map - Zynq UltraScale+ MPSoC - Zu02 and Zu03 with Low Power and Full Power Control



	Power Mode	
SOM	LP	FP
VCCPSINTLP	on	on
VCCPSINTFP	off	on
VCCINT_IO / VCCBRAM	off	on
VCCINT	off	on
VCCPSAUX / VCCPSIO (0:2:3) / PSBATT	on	on
VCCPLL	on	on
VCCDDR / VCCO / DDR4 devices	off	on
VCCAUX / AUX_IO / VCCO / ENET PHY	off	on
VCCO	off	on
VCCO / ENET PHY	off	on
VTERM	off	on
ENET PHY	off	on

Fully integrated power sequencer - shown Infineon PowIRCenter GUI to set sequencing - 15 power rails

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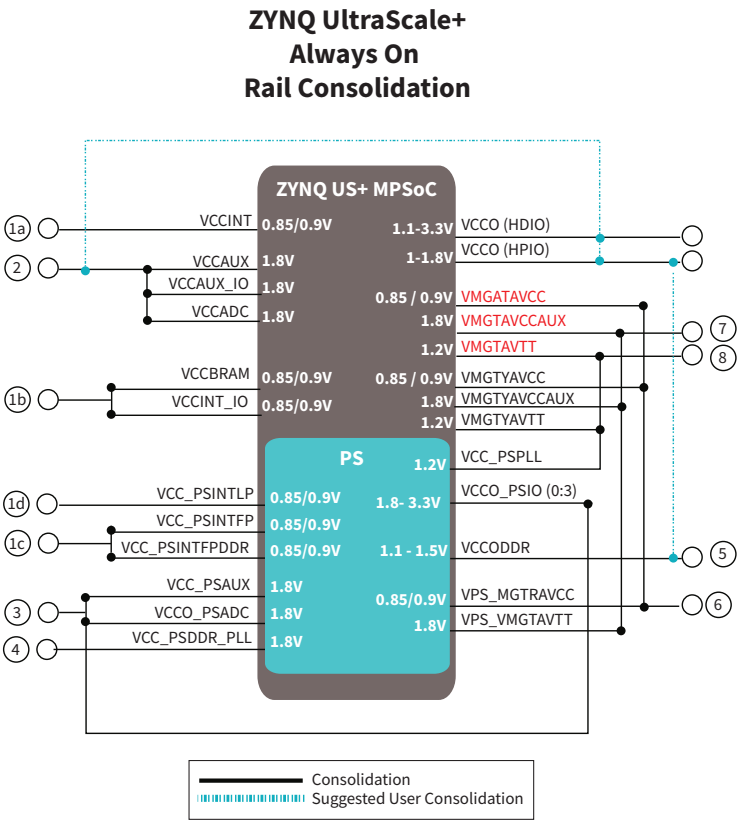
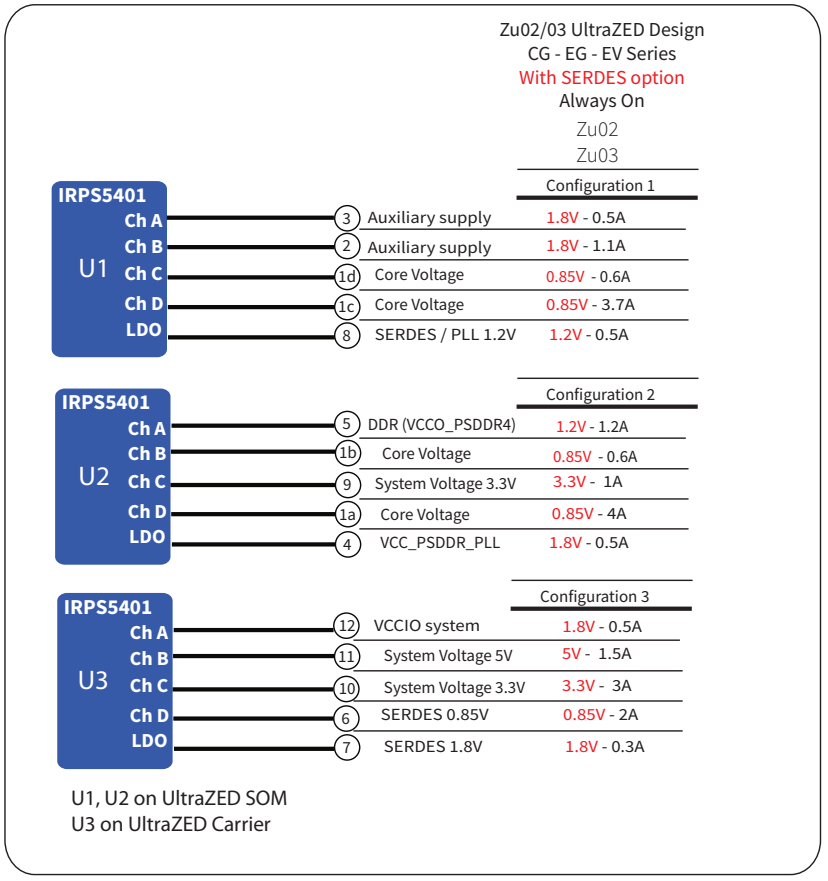
Infineon Power for Xilinx Zynq UltraScale+ MPSoC

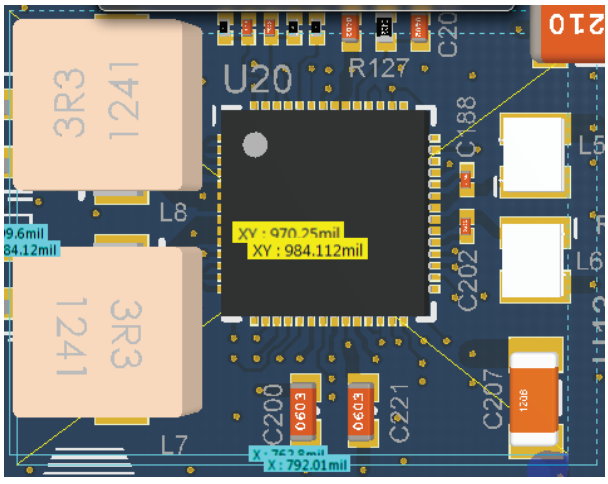
Power Solution - High Level - Zynq UltraScale+ - Zu02 / Zu03 - CG / EG / EV Series
UltraZED Reference Design





Example Layout Design Per IRPS5401 PMIC
UltraZED Reference Design
(including inductors and capacitors):

19.3mm x 15.3mm - 5 Outputs



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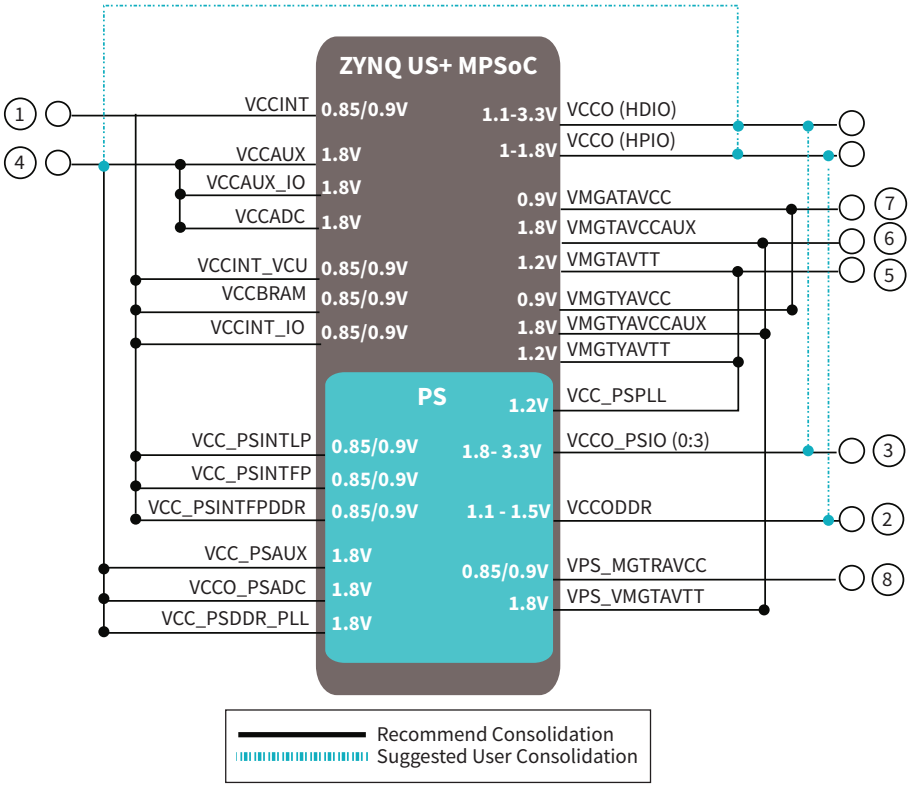
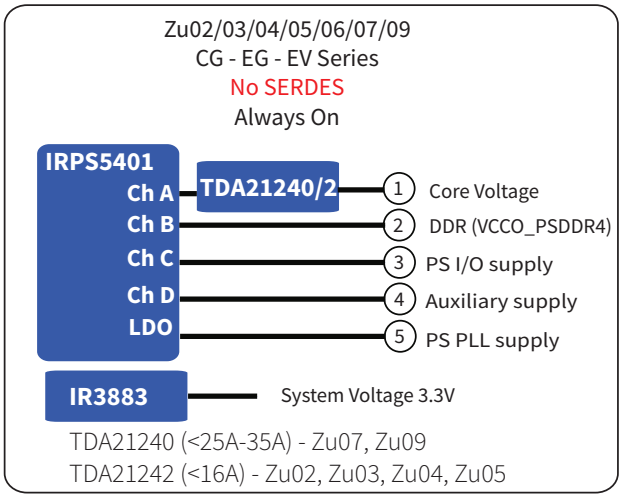
DC-DC Power Solutions for FPGAs

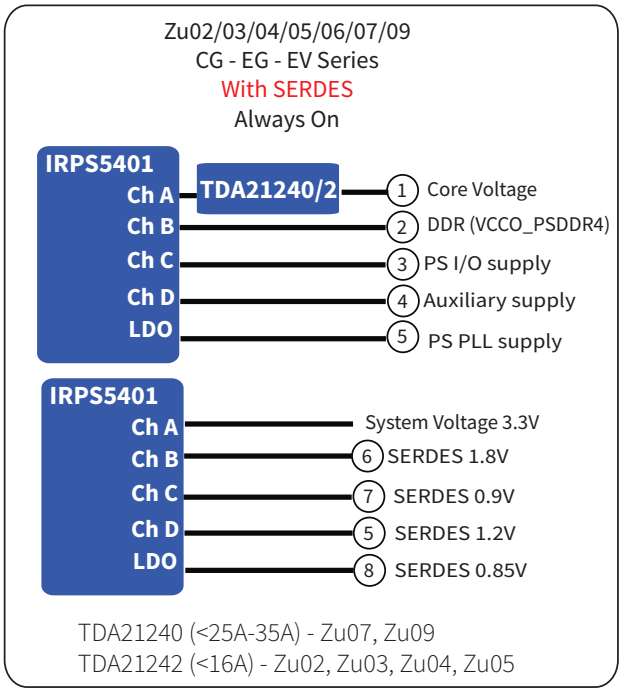
Infineon Power for Xilinx Zynq UltraScale+ MPSoC

Power Solution - High Level - Zynq UltraScale+ - Zu02 to Zu09 - CG / EG / EV Series
Power Always On

ZYNQ UltraScale+
Always On
Rail Consolidation







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DC-DC Power Solutions for FPGAs

Infineon Power for Xilinx Zynq UltraScale+ MPSoC

Power Solution - High Level - Zynq UltraScale+ - Zu02 to Zu09 - CG / EG / EV Series

Power Always On

Use Case 1: Always On Zu02 to Zu09

			Zu02_04_05-CG-EG-EV No SERDES				
Rocky#	**Vin**	**Channel**	**Rails**	**Vout**	**Pwr Specs**	**Power Stage**	**Iout (A)**
IRPS5401 U1	**5V/15V**	**Ch A**	VCC_PSINTFP/VCC_PSINTFPDDR, VCCINT_IO / VCCBRAM, VCC_PSINTLP, VCCINT	0.85V	0.85/0.9 +/-1% (AC 2%), 1/3 Imax step	TDA2124x	16A
		Ch B	VCCO_PSDDR4_504	1.2V	1.2V 1% DC; 3%AC	Integrated	1.5A
		Ch C	VCCO_PSIO (0:3)	1.8V	1.8V 2% DC; 3%AC	Integrated	1A
		Ch D	VCCAUX, VCCADC, VCCAUX_IO, VCC_PSDDR_PLL, VCCO_PSADC, VCC_PSAUX, VCCIO (0.5A)	1.8V	1.8 +/-1% (AC 2%), 1/3 Imax step	Integrated	4A
		LDO out	VCC_PSPLL	1.2V		Integrated	0.5A
		LDO in	3.3V / IR3883 system voltage				

Use Case 1: Always On Zu02 to Zu09

			Zu07CG-EG-EV No SERDES				
Rocky#	**Vin**	**Channel**	**Rails**	**Vout**	**Pwr Specs**	**Power Stage**	**Iout**
IRPS5401 U1	**5V/15V**	**Ch A**	VCC_PSINTFP/VCC_PSINTFPDDR, VCCINT_IO / VCCBRAM, VCC_PSINTLP, VCCINT	0.85V	0.85/0.9 +/-1% (AC 2%), 1/3 Imax step	TDA2124x	25A
		Ch B	VCCO_PSDDR4_504	1.2V	1.2V 1% DC; 3%AC	Integrated	1.5A
		Ch C	VCCO_PSIO (0:3)	1.8V	1.8V 2% DC; 3%AC	Integrated	1A
		Ch D	VCCAUX, VCCADC, VCCAUX_IO, VCC_PSDDR_PLL, VCCO_PSADC, VCC_PSAUX, VCCIO (0.5A)	1.8V	1.8 +/-1% (AC 2%), 1/3 Imax step	Integrated	4A
		LDO out	VCC_PSPLL	1.2V		Integrated	0.5A
		LDO in	3.3V / IR3883 system voltage				

Use Case 1: Always On Zu02 to Zu09

			Zu09CG-EG-EV No SERDES				
Rocky#	**Vin**	**Channel**	**Rails**	**Vout**	**Pwr Specs**	**Power Stage**	**Iout (A)**
IRPS5401 U1	**5V/15V**	**Ch A**	VCC_PSINTFP/VCC_PSINTFPDDR, VCCINT_IO / VCCBRAM, VCC_PSINTLP, VCCINT	0.85V	0.85/0.9 +/-1% (AC 2%), 1/3 Imax step	TDA2124x	25A
		Ch B	VCCO_PSDDR4_504	1.2V	1.2V 1% DC; 3%AC	Integrated	1.5A
		Ch C	VCCO_PSIO (0:3)	1.8V	1.8V 2% DC; 3%AC	Integrated	1A
		Ch D	VCCAUX, VCCADC, VCCAUX_IO, VCC_PSDDR_PLL, VCCO_PSADC, VCC_PSAUX, VCCIO (0.5A)	1.8V	1.8 +/-1% (AC 2%), 1/3 Imax step	Integrated	4A
		LDO out	VCC_PSPLL	1.2V		Integrated	0.5A
		LDO in	3.3V / IR3883				

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DC-DC Power Solutions for FPGAs

Infineon Power for Xilinx Zynq UltraScale+ MPSoC

Power Solution - High Level - Zynq UltraScale+ - Zu02 to Zu09 - CG / EG / EV Series
Power Always On

Use Case 2: Always On, Power Efficiency, Zu04 to Zu07 with Video Codec

			Zu04_05EV No SERDES, Video codec					Zu07EV No SERDES, Video Codec				
Rocky#	Vin	Channel	Rail	Vout	Pwr Specs	Power Stage	Iout (A)	Rails	Vout	Pwr Specs	Power Stage	Iout (A)
IRPS5401 U1	5V/15V	Ch A	VCCINT	**0.72V**	0.72V +/-1% (AC 2%), 1/3 Imax step	TDA2124x	9A	VCCINT	**0.72V**	0.72V +/-1% (AC 2%), 1/3 Imax step	TDA2124x	15A
		Ch B	system voltage 3.3V	**3.3V**	5%	**Integrated**	1.1A (2A)	system voltage 3.3V	**3.3V**	5%	Integrated	1.1A (2A)
		Ch C	VCC_PSINTFP/ VCC_PSINTFPDDR, VCCINT_IO / VCCBRAM, VCC_PSINTLP	**0.85V**	0.85/0.9 +/-1% (AC 2%), 1/3 Imax step	**Integrated**	7A	VCC_PSINTFP/ VCC_PSINTFPDDR, VCCINT_IO / VCCBRAM, VCC_PSINTLP	**0.85V**	0.85/0.9 +/-1% (AC 2%), 1/3 Imax step	Integrated	7A
		Ch D				**Integrated**					Integrated	
		LDO out	VCC_PSPLL	**1.2V**	1.2V 1% DC; 3%AC	**Integrated**	0.5A	VCC_PSPLL	**1.2V**	1.2V 1% DC; 3%AC	Integrated	0.5A
		LDO in		**3.3V / Ch B**					**3.3V / Ch B**			
IRPS5401 U2	5V/15V	Ch A	VCCO_PSIO (0:3)	1.8	1.2V 1% DC; 3%AC	Integrated	1A	VCCO_PSIO (0:3)	1.8	1.2V 1% DC; 3%AC	Integrated	1A
		Ch B	VCCO_PSDDR4_504	1.2	1.2V 1% DC; 3%AC	Integrated	1.5A	VCCO_PSDDR4_504	1.2	1.2V 1% DC; 3%AC	Integrated	1.5A
		Ch C	VCCAUX, VCCADC, VCCAUX_IO, VCC_PSDDR_PLL, VCCO_PSADC, VCC_PSAUX, VCCIO (0.5A)	1.8	1.8 +/-1% (AC 2%), 1/3 Imax step	Integrated	2A	VCCAUX, VCCADC, VCCAUX_IO, VCC_PSDDR_PLL, VCCO_PSADC, VCC_PSAUX, VCCIO (0.5A)	1.8	1.8 +/-1% (AC 2%), 1/3 Imax step	Integrated	2A
		Ch D	system voltage 2.5V	2.5	5%	Integrated	1A	system voltage 2.5V	2.5	5%	Integrated	1A
		LDO out	User I/O: 1.5V	1.5V			0.5A	User I/O: 1.5V	1.5V			0.5A
		LDO in		2.5V / Ch D					2.5V / Ch D			

Use Case 2: Always On, Power Efficiency, Zu04 to Zu07 with Video Codec

			Zu04_05EV With SERDES, Video codec					Zu07EV With SERDES, Video Codec				
Rocky#	Vin	Channel	Rails	Vout	Pwr Specs	Power Stage	Iout (A)	Rails	Vout	Pwr Specs	Power Stage	Iout (A)
IRPS5401 U1	5V/15V	Ch A	VCCINT	**0.72V**	0.72V +/-1% (AC 2%), 1/3 Imax step	TDA2124x	9A	VCCINT	**0.72V**	0.72V +/-1% (AC 2%), 1/3 Imax step	**TDA21240**	15A
		Ch B	System Voltage 3.3V	**3.3V**	5%	**Integrated**	2A	System Voltage 3.3V	**3.3V**	5%	Integrated	2A
		Ch C	VCC_PSINTFP/ VCC_PSINTFPDDR, VCCINT_IO / VCCBRAM, VCC_PSINTLP	**0.85V**	0.85/0.9 +/-1% (AC 2%), 1/3 Imax step	**Integrated**	7A	VCC_PSINTFP/ VCC_PSINTFPDDR, VCCINT_IO / VCCBRAM, VCC_PSINTLP	**0.85V**	0.85/0.9 +/-1% (AC 2%), 1/3 Imax step	Integrated	7A
		Ch D				**Integrated**					Integrated	
		LDO out	VCC_PSPLL	**1.2V**	1.2V 1% DC; 3%AC	Integrated	0.5A	VCC_PSPLL	**1.2V**	1.2V 1% DC; 3%AC	Integrated	0.5A
		LDO in	**3.3V / Ch B, PS I/O Supply: VCCO_PSIO (0:3) use LDO or IR3883 (<200mA)**					**3.3V / Ch B, PS I/O Supply: VCCO_PSIO (0:3) use LDO or IR3883 (<200mA)**				
IRPS5401 U2	5V/15V	Ch A	VMGATAVCC, VMGTYAVCC	0.9V	0.9 +/-1% (AC 2%), <10mVpp ripple 1/2 Imax step	Integrated	2A	VMGATAVCC, VMGTYAVCC	0.9V	0.9 +/-1% (AC 2%), <10mVpp ripple 1/2 Imax step	Integrated	2A
		Ch B	VCCO_PSDDR4_504	1.2V	1.2V 1% DC; 3%AC	Integrated	1.5A	VCCO_PSDDR4_504	1.2V	1.2V 1% DC; 3%AC	Integrated	1.5A
		Ch C	VCCAUX, VCCADC, VCCAUX_IO, VCC_PSDDR_PLL, VCCO_PSADC, VCC_PSAUX, VCCIO (0.5A)	1.8V	1.8 +/-1% (AC 2%), 1/3 Imax step	Integrated	2A	VCCAUX, VCCADC, VCCAUX_IO, VCC_PSDDR_PLL, VCCO_PSADC, VCC_PSAUX, VCCIO (0.5A)	1.8V	1.8 +/-1% (AC 2%), 1/3 Imax step	Integrated	2A
		Ch D	VMGTAVTT, VMGTYAVTT, VCC_PSPLL, VCC_VCU_PLL	1.2V	1.2 +/-1% (AC 2%), <10mVpp ripple 1/2 Imax step	Integrated	2A	VMGTAVTT, VMGTYAVTT, VCC_PSPLL, VCC_VCU_PLL	1.2V	1.2 +/-1% (AC 2%), <10mVpp ripple 1/2 Imax step	Integrated	2A
		LDO out	VPS_MGTRAVCC	0.85V			0.5A	VPS_MGTRAVCC	0.85V			0.5A
		LDO in	use 3.3V input; use LDO for SERDES 1.8V (100mA) - VPS_MGTRAVTT, VMGTAVCCAUX VMGTYAVCCAUX					use 3.3V input; use LDO for SERDES 1.8V (100mA) - VPS_MGTRAVTT, VMGTAVCCAUX VMGTYAVCCAUX				

DC-DC Power Solutions for FPGAs

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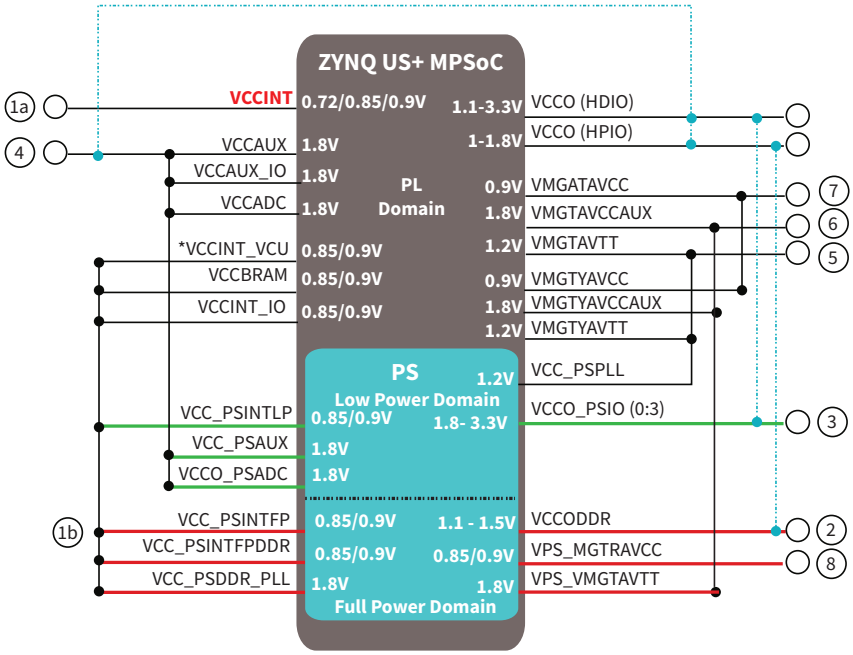
Infineon Power for Xilinx Zynq UltraScale+ MPSoC

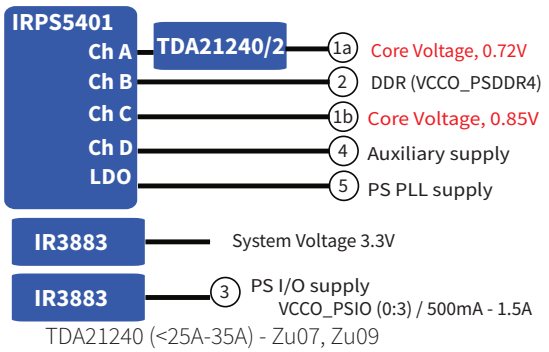
Power Solution - High Level - Zynq UltraScale+ - Zu02 to Zu09 - CG / EG Series
Power Always On - Power Efficiency - Separate Vcore voltage, 0.72V & 0.85V

ZYNQ UltraScale+
Always On - Power Efficiency
Separate Core Voltage @ 0.72V
Rail Consolidation



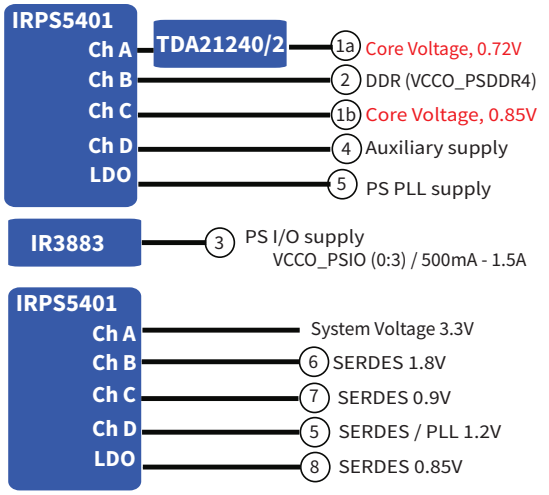
*EV Series Only use Video Codec

Zu04/05/06/07/09
CG - EG Series
No SERDES
Always On - Power Efficiency



TDA21240 (<25A-35A) - Zu07, Zu09
TDA21242 (<16A) - Zu02, Zu03, Zu04, Zu05

Zu02/03/04/05/06/07/09
CG - EG Series
With SERDES
Always On - Power Efficiency



TDA21240 (<25A-35A) - Zu07, Zu09
TDA21242 (<16A) - Zu02, Zu03, Zu04, Zu05

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Infineon Power for Xilinx Zynq UltraScale+ MPSoC

Power Solution - High Level - Zynq UltraScale+ - Zu02 to Zu09 - CG / EG Series
Power Always On - Power Efficiency - Separate Vcore voltage, 0.72V & 0.85V

Use Case 2: Always On, Power Efficiency, Zu04 to Zu09

			Zu04_05 CG EG No SERDES					Zu07 (15A)_Zu09 (20A) CG EG No SERDES				
Rocky#	Vin	Channel	Rails	Vout	Pwr Specs	Power Stage	Iout (A)	Rails	Vout	Pwr Specs	Power Stage	Iout (A)
IRPS5401 U1	5V/15V	Ch A	VCCINT	**0.72V**	0.72V +/-1% (AC 2%), 1/3 Imax step	TDA2124x	9A	VCCINT	**0.72V**	0.72V +/-1% (AC 2%), 1/3 Imax step	**TDA2124x**	20A
		Ch B	VCCO_PSDDR4_504	1.2	1.2V 1% DC; 3%AC	Integrated	1.5A	VCCO_PSDDR4_504	1.2	1.2V 1% DC; 3%AC	Integrated	1.5A
		Ch C	VCC_PSINTFP/ VCC_PSINTFPDDR, VCCINT_IO / VCCBRAM, VCC_PSINTLP	**0.85V**	0.85/0.9 +/-1% (AC 2%), 1/3 Imax step	**Integrated**	4A	VCC_PSINTFP/ VCC_PSINTFPDDR, VCCINT_IO / VCCBRAM, VCC_PSINTLP	**0.85V**	0.85/0.9 +/-1% (AC 2%), 1/3 Imax step	**Integrated**	4A
		Ch D	VCCAUX, VCCADC, VCCAUX_IO, VCC_PSDDR_PLL, VCCO_PSADC, VCC_PSAUX, VCCIO (0.5A)	**1.8**	1.8 +/-1% (AC 2%), 1/3 Imax step	**Integrated**	2A	VCCAUX, VCCADC, VCCAUX_IO, VCC_PSDDR_PLL, VCCO_PSADC, VCC_PSAUX, VCCIO (0.5A)	**1.8**		**Integrated**	2A
		LDO out	VCC_PSPLL	**1.2V**	1.2V 1% DC; 3%AC	**Integrated**	0.5A	VCC_PSPLL	**1.2V**	1.2V 1% DC; 3%AC	**Integrated**	0.5A
		LDO in	**3.3V system voltage / IR3883 also additional 1.8V/IR3883 (for VCCO_PSIO)**					**3.3V system voltage / IR3883 also additional 1.8V/IR3883 (for VCCO_PSIO)**				

Use Case 2: Always On, Power Efficiency, Zu04 to Zu09

			Zu04_05 CG EG with SERDES					Zu06_07 (15A)_Zu09 (20A) CG EG with SERDES				
Rocky#	Vin	Channel	Rails	Vout	Pwr Specs	Power Stage	Iout (A)	Rails	Vout	Pwr Specs	Power Stage	Iout (A)
IRPS5401 U1	5V/15V	Ch A	VCCINT	**0.72V**	0.72V +/-1% (AC 2%), 1/3 Imax step	**TDA2124x**	9A	VCCINT	**0.72V**	0.72V +/-1% (AC 2%), 1/3 Imax step	**TDA21240**	20A
		Ch B	VCCO_PSDDR4_504	1.2	1.2V 1% DC; 3%AC	Integrated	1.2A	VCCO_PSDDR4_504	1.2	1.2V 1% DC; 3%AC	Integrated	1.2A
		Ch C	VCC_PSINTFP/ VCC_PSINTFPDDR, VCCINT_IO / VCCBRAM, VCC_PSINTLP	**0.85V**	0.85/0.9 +/-1% (AC 2%), 1/3 Imax step	**Integrated**	4A	VCC_PSINTFP/ VCC_PSINTFPDDR, VCCINT_IO / VCCBRAM, VCC_PSINTLP	**0.85V**	0.85/0.9 +/-1% (AC 2%), 1/3 Imax step	**Integrated**	4A
		Ch D	VCCAUX, VCCADC, VCCAUX_IO, VCC_PSDDR_PLL, VCCO_PSADC, VCC_PSAUX, VCCIO (0.5A)	**1.8**	1.8 +/-1% (AC 2%), 1/3 Imax step	**Integrated**	2A	VCCAUX, VCCADC, VCCAUX_IO, VCC_PSDDR_PLL, VCCO_PSADC, VCC_PSAUX, VCCIO (0.5A)			**Integrated**	2A
		LDO out	VCC_PSPLL	**1.2V**	1.2V 1% DC; 3%AC	Integrated	0.5A	VCC_PSPLL	**1.2V**	1.2V 1% DC; 3%AC	Integrated	0.5A
		LDO in	**1.8V/IR3883 (for VCCO_PSIO)**					1.8V/IR3883 (for VCCO_PSIO)				
IRPS5401 U2	5V/15V	Ch A	system voltage 3.3V	3.3V	5%	Integrated	1A	system voltage 3.3V	3.3V	5%	Integrated	1A
		Ch B	VPS_MGTRAVTT, VMGTAVCCAUX VMGTYAVCCAUX	1.8V	1.8+/-1% (AC 2%), <10mVpp ripple 1/2 Imax step	Integrated	1A	VPS_MGTRAVTT, VMGTAVCCAUX VMGTYAVCCAUX	1.8V	1.8+/-1% (AC 2%), <10mVpp ripple 1/2 Imax step	Integrated	1A
		Ch C	VMGATAVCC, VMGTYAVCC	0.9V	0.9 +/-1% (AC 2%), <10mVpp ripple 1/2 Imax step	Integrated	2A	VMGATAVCC, VMGTYAVCC	0.9V	0.9 +/-1% (AC 2%), <10mVpp ripple 1/2 Imax step	Integrated	2A
		Ch D	VMGTAVTT, VMGTYAVTT, VCC_VCU_PLL	1.2V	1.2 +/-1% (AC 2%), <10mVpp ripple 1/2 Imax step	Integrated	2A	VMGTAVTT, VMGTYAVTT, VCC_VCU_PLL	1.2V	1.2 +/-1% (AC 2%), <10mVpp ripple 1/2 Imax step	Integrated	2A
		LDO out	VPS_MGTRAVCC	0.85V	0.85 +/-1% (AC 2%), <10mVpp ripple 1/2 Imax step	Integrated	0.5A	VPS_MGTRAVCC	0.85V	0.85 +/-1% (AC 2%), <10mVpp ripple 1/2 Imax step	Integrated	0.5A
		LDO in		3.3V / Ch A					3.3V / Ch A			

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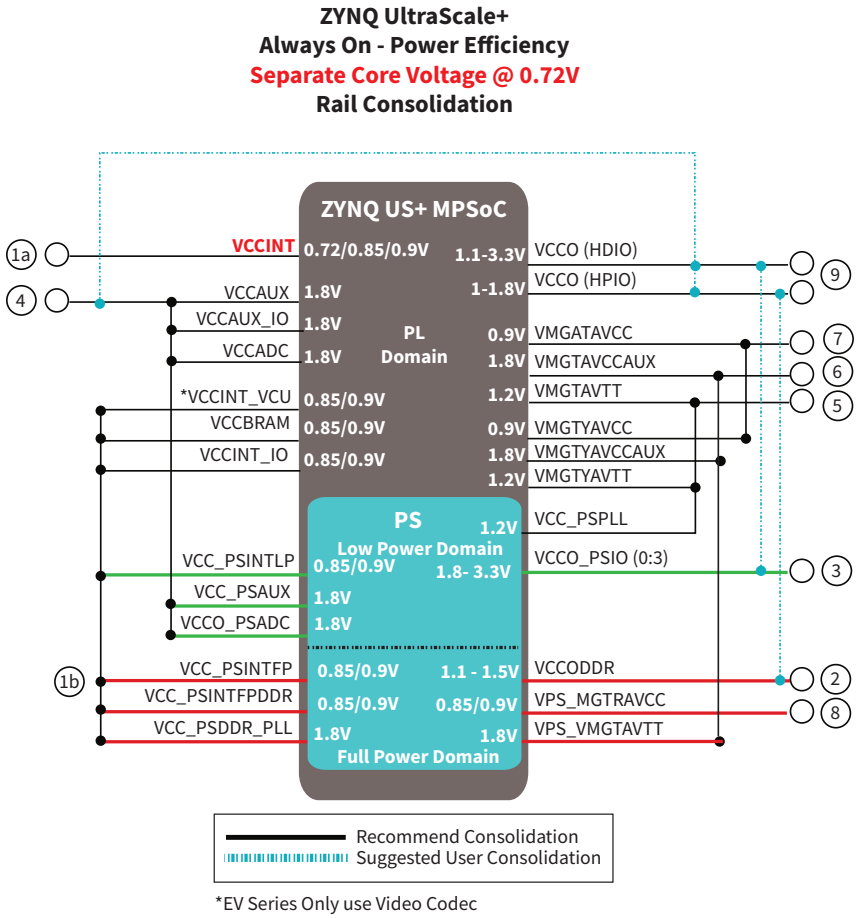
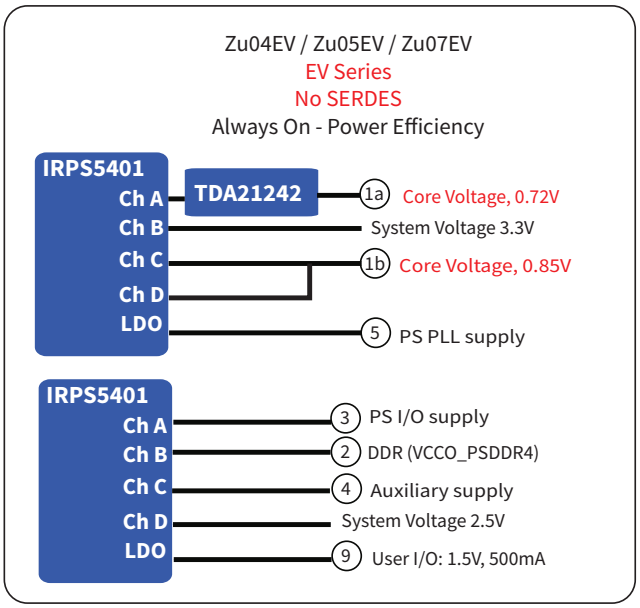
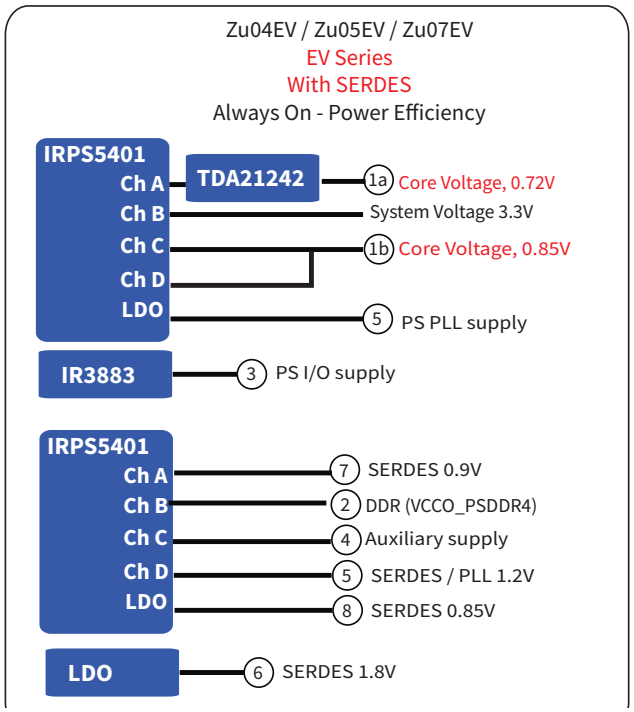
Infineon Power for Xilinx Zynq UltraScale+ MPSoC

Power Solution - High Level - Zynq UltraScale+ - Zu04, Zu05, Zu07 EV Series - Video Codec
Power Always On - Power Efficiency - Separate Vcore voltage, 0.72V & 0.85V



*EV Series Only use Video Codec





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DC-DC Power Solutions for FPGAs

Infineon Power for Xilinx Zynq UltraScale+ MPSoC

Power Solution - High Level - Zynq UltraScale+ - Zu04, Zu05, Zu07 EV Series - Video Codec
Power Always On - Power Efficiency - Separate Vcore voltage, 0.72V & 0.85V

Use Case 2: Always On, Power Efficiency, Zu04 to Zu07 with Video Codec

			Zu04_05EV No SERDES, Video codec					Zu07EV No SERDES, Video Codec				
Rocky#	Vin	Channel	Rail	Vout	Pwr Specs	Power Stage	Iout (A)	Rails	Vout	Pwr Specs	Power Stage	Iout (A)
IRPS5401 U1	5V/15V	Ch A	VCCINT	**0.72V**	0.72V +/-1% (AC 2%), 1/3 Imax step	TDA2124x	9A	VCCINT	**0.72V**	0.72V +/-1% (AC 2%), 1/3 Imax step	TDA2124x	15A
		Ch B	system voltage 3.3V	**3.3V**	5%	**Integrated**	1.1A (2A)	system voltage 3.3V	**3.3V**	5%	Integrated	1.1A (2A)
		Ch C	VCC_PSINTFP/ VCC_PSINTFPDDR, VCCINT_IO / VCCBRAM, VCC_PSINTLP	**0.85V**	0.85/0.9 +/-1% (AC 2%), 1/3 Imax step	**Integrated**	7A	VCC_PSINTFP/ VCC_PSINTFPDDR, VCCINT_IO / VCCBRAM, VCC_PSINTLP	**0.85V**	0.85/0.9 +/-1% (AC 2%), 1/3 Imax step	Integrated	7A
		Ch D				**Integrated**					Integrated	
		LDO out	VCC_PSPLL	**1.2V**	1.2V 1% DC; 3%AC	**Integrated**	0.5A	VCC_PSPLL	**1.2V**	1.2V 1% DC; 3%AC	Integrated	0.5A
		LDO in		**3.3V / Ch B**					**3.3V / Ch B**			
IRPS5401 U2	5V/15V	Ch A	VCCO_PSIO (0:3)	1.8	1.2V 1% DC; 3%AC	Integrated	1A	VCCO_PSIO (0:3)	1.8	1.2V 1% DC; 3%AC	Integrated	1A
		Ch B	VCCO_PSDDR4_504	1.2	1.2V 1% DC; 3%AC	Integrated	1.5A	VCCO_PSDDR4_504	1.2	1.2V 1% DC; 3%AC	Integrated	1.5A
		Ch C	VCCAUX, VCCADC, VCCAUX_IO, VCC_PSDDR_PLL, VCCO_PSADC, VCC_PSAUX, VCCIO (0.5A)	1.8	1.8 +/-1% (AC 2%), 1/3 Imax step	Integrated	2A	VCCAUX, VCCADC, VCCAUX_IO, VCC_PSDDR_PLL, VCCO_PSADC, VCC_PSAUX, VCCIO (0.5A)	1.8	1.8 +/-1% (AC 2%), 1/3 Imax step	Integrated	2A
		Ch D	system voltage 2.5V	2.5	5%	Integrated	1A	system voltage 2.5V	2.5	5%	Integrated	1A
		LDO out	User I/O: 1.5V	1.5V			0.5A	User I/O: 1.5V	1.5V			0.5A
		LDO in		2.5V / Ch D					2.5V / Ch D			

Use Case 2: Always On, Power Efficiency, Zu04 to Zu07 with Video Codec

			Zu04_05EV With SERDES, Video codec					Zu07EV With SERDES, Video Codec				
Rocky#	Vin	Channel	Rails	Vout	Pwr Specs	Power Stage	Iout (A)	Rails	Vout	Pwr Specs	Power Stage	Iout (A)
IRPS5401 U1	5V/15V	Ch A	VCCINT	**0.72V**	0.72V +/-1% (AC 2%), 1/3 Imax step	TDA2124x	9A	VCCINT	**0.72V**	0.72V +/-1% (AC 2%), 1/3 Imax step	**TDA21240**	15A
		Ch B	System Voltage 3.3V	**3.3V**	5%	**Integrated**	2A	System Voltage 3.3V	**3.3V**	5%	Integrated	2A
		Ch C	VCC_PSINTFP/ VCC_PSINTFPDDR, VCCINT_IO / VCCBRAM, VCC_PSINTLP	**0.85V**	0.85/0.9 +/-1% (AC 2%), 1/3 Imax step	**Integrated**	7A	VCC_PSINTFP/ VCC_PSINTFPDDR, VCCINT_IO / VCCBRAM, VCC_PSINTLP	**0.85V**	0.85/0.9 +/-1% (AC 2%), 1/3 Imax step	Integrated	7A
		Ch D				**Integrated**					Integrated	
		LDO out	VCC_PSPLL	**1.2V**	1.2V 1% DC; 3%AC	Integrated	0.5A	VCC_PSPLL	**1.2V**	1.2V 1% DC; 3%AC	Integrated	0.5A
		LDO in	**3.3V / Ch B, PS I/O Supply: VCCO_PSIO (0:3) use LDO or IR3883 (<200mA)**					**3.3V / Ch B, PS I/O Supply: VCCO_PSIO (0:3) use LDO or IR3883 (<200mA)**				
IRPS5401 U2	5V/15V	Ch A	VMGATAVCC, VMGTYAVCC	0.9V	0.9 +/-1% (AC 2%), <10mVpp ripple 1/2 Imax step	Integrated	2A	VMGATAVCC, VMGTYAVCC	0.9V	0.9 +/-1% (AC 2%), <10mVpp ripple 1/2 Imax step	Integrated	2A
		Ch B	VCCO_PSDDR4_504	1.2V	1.2V 1% DC; 3%AC	Integrated	1.5A	VCCO_PSDDR4_504	1.2V	1.2V 1% DC; 3%AC	Integrated	1.5A
		Ch C	VCCAUX, VCCADC, VCCAUX_IO, VCC_PSDDR_PLL, VCCO_PSADC, VCC_PSAUX, VCCIO (0.5A)	1.8V	1.8 +/-1% (AC 2%), 1/3 Imax step	Integrated	2A	VCCAUX, VCCADC, VCCAUX_IO, VCC_PSDDR_PLL, VCCO_PSADC, VCC_PSAUX, VCCIO (0.5A)	1.8V	1.8 +/-1% (AC 2%), 1/3 Imax step	Integrated	2A
		Ch D	VMGTAVTT, VMGTYAVTT, VCC_PSPLL, VCC_VCU_PLL	1.2V	1.2 +/-1% (AC 2%), <10mVpp ripple 1/2 Imax step	Integrated	2A	VMGTAVTT, VMGTYAVTT, VCC_PSPLL, VCC_VCU_PLL	1.2V	1.2 +/-1% (AC 2%), <10mVpp ripple 1/2 Imax step	Integrated	2A
		LDO out	VPS_MGTRAVCC	0.85V			0.5A	VPS_MGTRAVCC	0.85V			0.5A
		LDO in	use 3.3V input; use LDO for SERDES 1.8V (100mA) - VPS_MGTRAVTT, VMGTAVCCAUX VMGTYAVCCAUX					use 3.3V input; use LDO for SERDES 1.8V (100mA) - VPS_MGTRAVTT, VMGTAVCCAUX VMGTYAVCCAUX				

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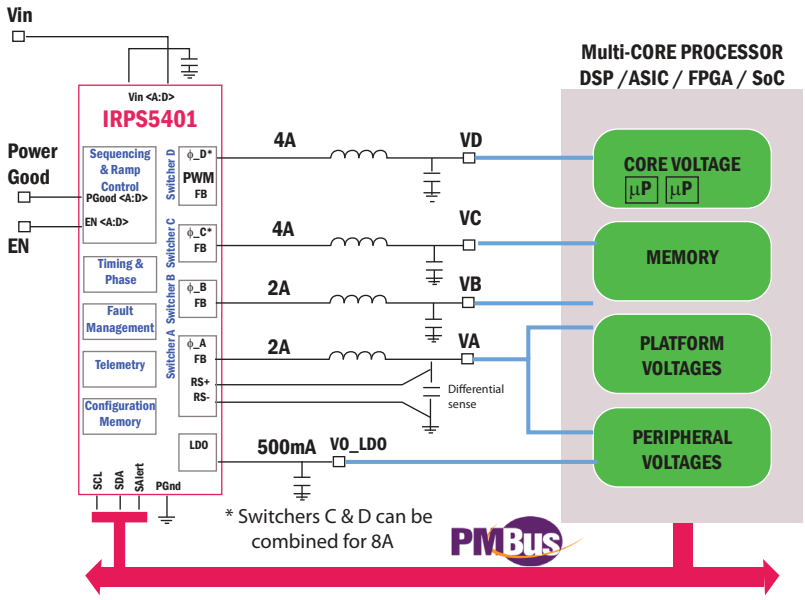
Go to IRPS5401

IRPS5401 Multi-output PMIC



IRPS5401 PMBus Command Set PMBus 1.2 Compliant - Advanced Digital Power				
PAGE	VOUT_MODE	VOUT_OV_FAULT_LIMIT	STATUS_BYTE	PMBUS_REVISION
OPERATION	VOUT_COMMAND	VOUT_OV_FAULT_RESPONSE	STATUS_WORD	MFR_ID
ON_OFF_CONFIG	VOUT_TRIM	VOUT_OV_WARN_LIMIT	STATUS_VOUT	MFR_MODEL
CLEAR_FAULTS	VOUT_MAX	VOUT_UV_WARN_LIMIT	STATUS_IOUT	MFR_REVISION
WRITE_PROTECT	VOUT_MARGIN_HIGH	VOUT_UV_FAULT_LIMIT	STATUS_INPUT	IC_DEVICE_ID
CAPABILITY	VOUT_MARGIN_LOW	VOUT_UV_FAULT_RESPONSE	STATUS_TEMPERATURE	IC_DEVICE_REV
SMBALERT_MASK	VOUT_TRANSITION_RATE	IOUT_OC_FAULT_LIMIT	STATUS_CML	MFR_SPECIFIC_00 r/w access to all registers
	VOUT_SCALE_LOOP	IOUT_OC_FAULT_RESPONSE	READ_VIN	MFR_SPECIFIC_01 r/w access to all registers
	FREQUENCY_SWITCH	IOUT_OC_WARN_LIMIT	READ_IIN	MFR_SPECIFIC_02 MFR_I2C_ADDRESS
	VIN_ON	OT_FAULT_LIMIT	READ_VOUT	MFR_SPECIFIC_03 MFR_TPGDLY
	VIN_OFF	OT_FAULT_RESPONSE	READ_IOUT	MFR_SPECIFIC_09 MFR_FCCM
	INTERLEAVE	OT_WARN_LIMIT	READ_TEMPERATURE_1	MFR_SPECIFIC_11 MFR_VOUT_PEAK
	IOUT_CAL_OFFSET	VIN_OV_FAULT_LIMIT	READ_POUT	MFR_SPECIFIC_12 MFR_IOUT_PEAK
		VIN_OV_FAULT_RESPONSE	READ_PIN	MFR_SPECIFIC_13 MFR_TEMPERATURE_PEAK
		VIN_UV_WARN_LIMIT		MFR_SPECIFIC_14 MFR_LDO_MARGIN
		POWER_GOOD_ON		
		POWER_GOOD_OFF		
		TON_DELAY		
		TON_RISE		
		TON_MAX_FAULT_LIMIT		
		TON_MAX_FAULT_RESPONSE		
		TOFF_DELAY		
		TOFF_FALL		

Example: Designing for Power Sequencing via PMBus using *PowIRCenter* GUI

FEATURES

- 5 integrated outputs
  4A, 4A, 2A and 2A Switching Regulators
  500mA Source/Sink Linear regulator
- Single rail operation 5V to 12
- Output Range 0.25V to 5.5V for outputs A-D 3.6V for LDO
- Digital Compensation: No externals required
- Differential voltage sensing on Switcher A for accuracy
- I2C / PMBus 1.2 Full Digital Power Command Set
- I2C level shift allows i/f to any I/O voltage from the SoC
- Integrated Sequencing, Telemetry, Fault Management, Inventory Management
- Switching Frequency from 200 kHz to 2MHz
- Regulators operated at different phases
- Flexible I2C and PMBus address schemes with base and offset addressing allowing for 15 offsets per base.
- Optional: Allows use of an external PowIRstage to 50A
- Optional: Switchers C & D can be combined for 8A
- Rated for -40°C to +125°C T_J operation
- Pb-Free, RoHS6, 7x7mm, 56-pin, 0.4mm pitch QFN

APPLICATIONS

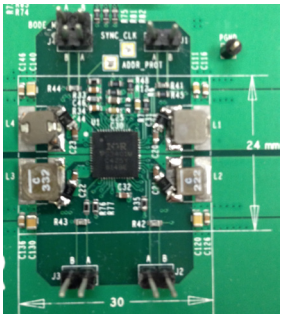
- Server / Microserver
- Storage
- Network Infrastructure
- Video / Image Processing
- FPGA accelerators

DESIGN TOOLS

- *PowIRCenter* GUI DESIGN TOOL
- IRPS5401 EVALUATION BOARDS

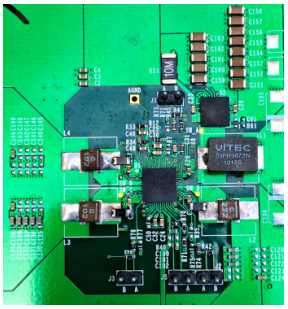
Eval Board - DB296

IRPS5401 only
4 regulators
1 LDO



Eval Board - DB295

IRPS5401 + external PowIRstage
4 regulators
1 LDO



DC-DC Power Solutions for FPGAs

Go to IRPS5401

IRPS5401 Multi-output PMIC