ISOFACE™ digital output Evaluation Board EVAL_ISO2H823V2.5_B user guide

EVAL_ISO2H823V2.5_B Rev 2.0

About this document

Scope and purpose

This user guide describes the features, hardware details, and the usage of the ISOFACE™ EVAL ISO2H823V2.5 Evaluation Board (version B) to understand the features of the innovative isolated eight channel high-side driver with integrated isolation.

Note: *The board is provided for evaluation purposes only. Do not use the evaluation board in continuous operation because it is not designed for this.*

Intended audience

The operation and use of the evaluation board is restricted to engineers and technicians in a laboratory environment, following appropriate safety measures.

Important notice

“Evaluation Boards and Reference Boards” shall mean products embedded on a printed circuit board (PCB) for demonstration and/or evaluation purposes, which include, without limitation, demonstration, reference and evaluation boards, kits and design (collectively referred to as “Reference Board”).

Environmental conditions have been considered in the design of the Evaluation Boards and Reference Boards provided by Infineon Technologies. The design of the Evaluation Boards and Reference Boards has been tested by Infineon Technologies only as described in this document. The design is not qualified in terms of safety requirements, manufacturing and operation over the entire operating temperature range or lifetime.

The Evaluation Boards and Reference Boards provided by Infineon Technologies are subject to functional testing only under typical load conditions. Evaluation Boards and Reference Boards are not subject to the same procedures as regular products regarding returned material analysis (RMA), process change notification (PCN) and product discontinuation (PD).

Evaluation Boards and Reference Boards are not commercialized products, and are solely intended for evaluation and testing purposes. In particular, they shall not be used for reliability testing or production. The Evaluation Boards and Reference Boards may therefore not comply with CE or similar standards (including but not limited to the EMC Directive 2004/EC/108 and the EMC Act) and may not fulfill other requirements of the country in which they are operated by the customer. The customer shall ensure that all Evaluation Boards and Reference Boards will be handled in a way which is compliant with the relevant requirements and standards of the country in which they are operated.

The Evaluation Boards and Reference Boards as well as the information provided in this document are addressed only to qualified and skilled technical staff, for laboratory usage, and shall be used and managed according to the terms and conditions set forth in this document and in other related documentation supplied with the respective Evaluation Board or Reference Board.

It is the responsibility of the customer’s technical departments to evaluate the suitability of the Evaluation Boards and Reference Boards for the intended application, and to evaluate the completeness and correctness of the information provided in this document with respect to such application.

The customer is obliged to ensure that the use of the Evaluation Boards and Reference Boards does not cause any harm to persons or third party property.
The Evaluation Boards and Reference Boards and any information in this document is provided "as is" and Infineon Technologies disclaims any warranties, express or implied, including but not limited to warranties of noninfringement of third party rights and implied warranties of fitness for any purpose, or for merchantability.

Infineon Technologies shall not be responsible for any damages resulting from the use of the Evaluation Boards and Reference Boards and/or from any information provided in this document. The customer is obliged to defend, indemnify and hold Infineon Technologies harmless from and against any claims or damages arising out of or resulting from any use thereof.

Infineon Technologies reserves the right to modify this document and/or any information provided herein at any time without further notice.

Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety precautions

	**Caution:** *The device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*

Table of contents

1 Introduction

The EVAL_ISO2H823V2.5_B establishes a new standard in diagnostics for digital outputs inside industrial control applications. For example, in industrial plants with capital-intensive single-tool equipment at work or with time critical chemical processes running, obtaining in real-time differentiated feedback from the factory floor enables both preventive maintenance and drastic reduction of the time to fix a problem. This is where the ISO2H823V is a highly desirable system solution. Typical applications are digital I/O modules of PLC systems but the device is equally suited for the usage inside industrial robots, industrial machinery, or as an isolated high-side driver. System designers benefit from the ISO2H823V2.5 through short time to market, reduced PCB area, and uncompromised product reliability.

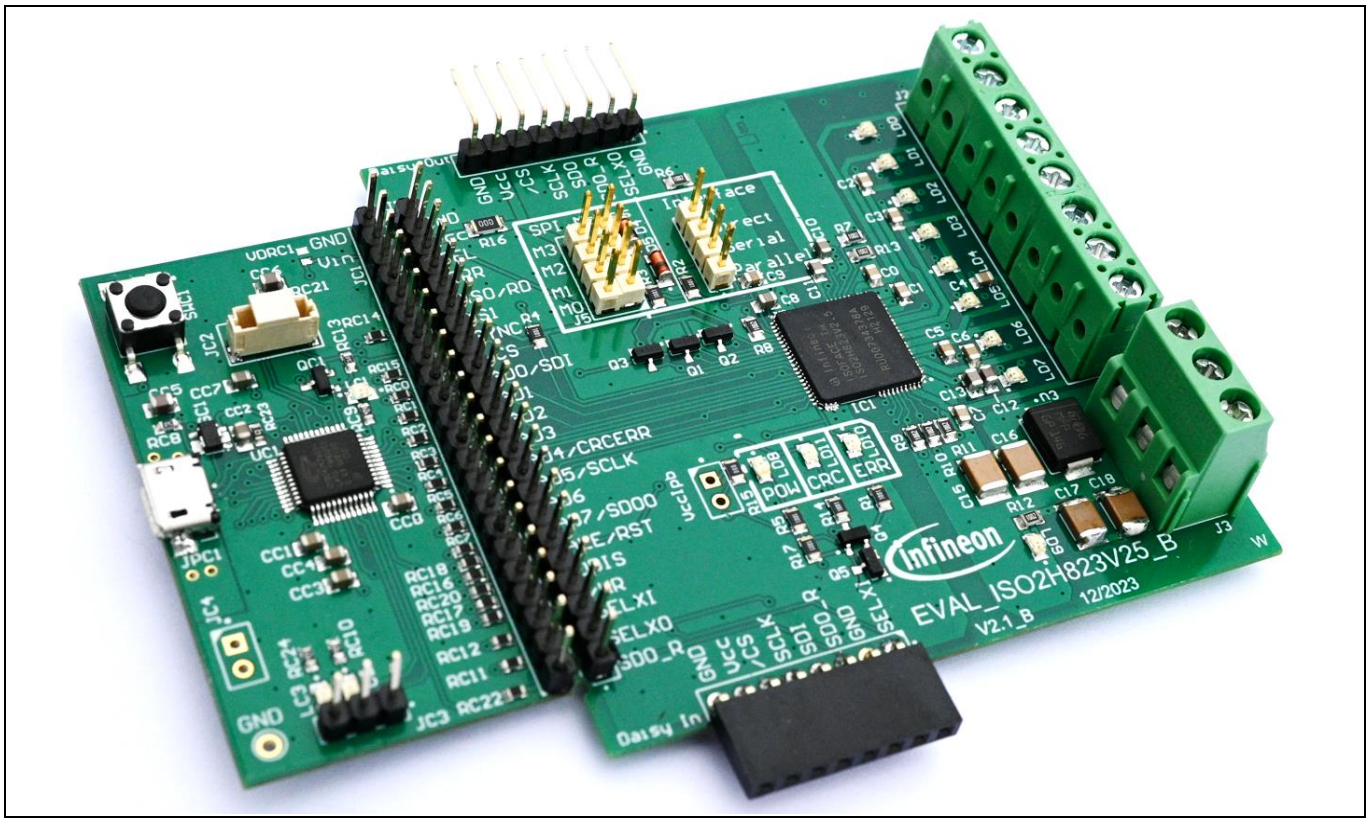

Figure 1 EVAL_ISO2H823V2.5_B

2 Board description and specifications

The ISO2H823V2.5 IC on this evaluation board is a digital output IC that provides eight output channels for a nominal load current of 0.5 A at 24 V. The output channels are suited for resistive, inductive, and capacitive loads with the limits described in the datasheet.

For further safety information, see the Safety limits for ISO2H8xx-ICs application note.

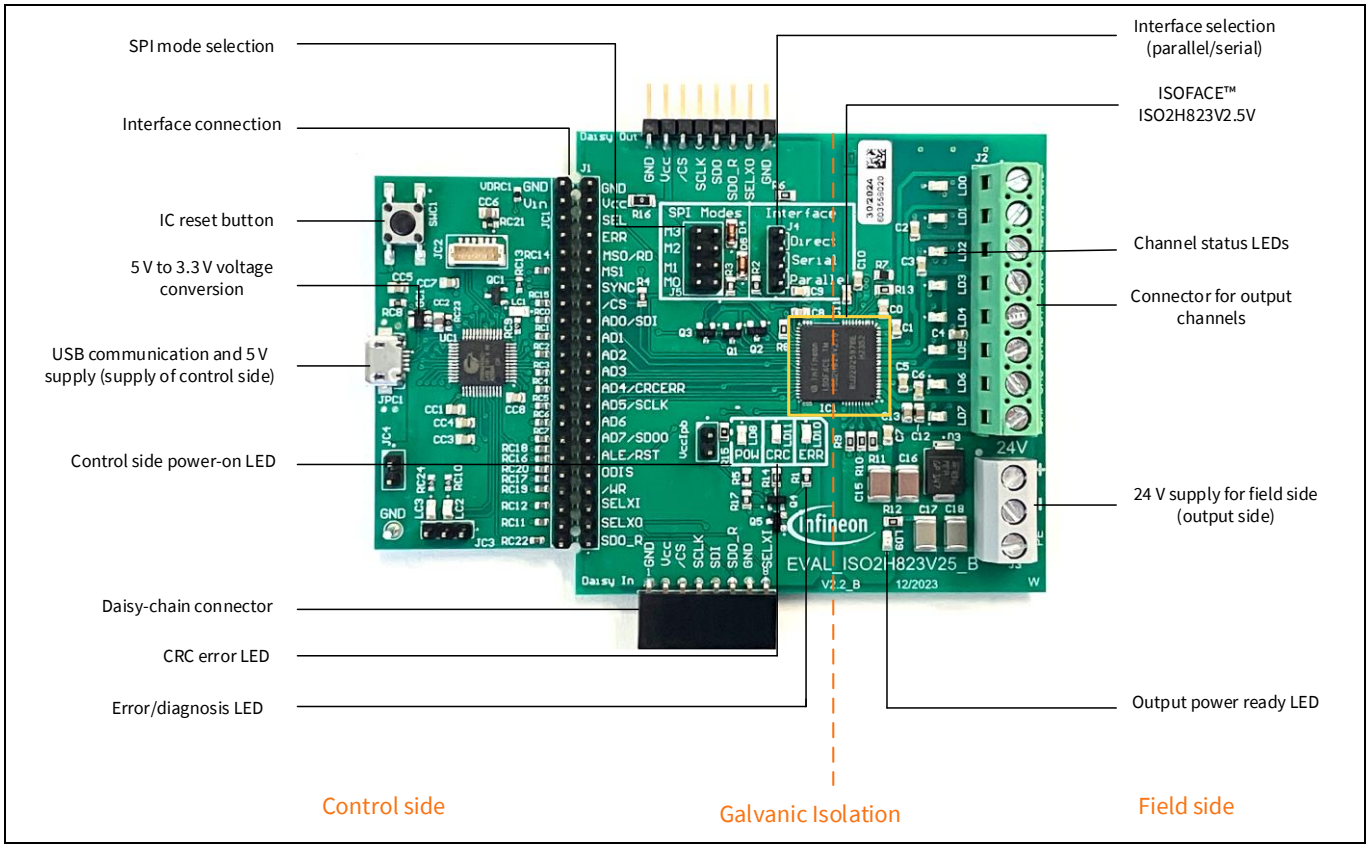

Figure 2 Evaluation board overview

Table 2 Electrical characteristics

Parameter	Min.	Typ.	Max.
V_{CC} supply voltage of control side [1]	2.75 V	3.3 V	3.6 V
Supply current of control side	–	–	10 mA
V_{BB} supply voltage of field side (= output side)	11 V	–	30 V
Supply current output side	15 mA	–	Output current + 15 mA
Output current per channel	–	–	0.65 A
Maximum output power	–	100 W	Maximum power depends on working temperature; see the Safety limits for ISO2H8xx-ICs application note

[1] Supply of V_{CC} pin is not needed if USB is connected because in this case the control side is directly supplied from the USB port.

3 Board functionality

The EVAL_ISO2H823V2.5_B includes the IC and all the external components required to set up a complete digital output application that can control eight output channels with a nominal load up to 0.5 A at 24 V each.

With this board, you can evaluate all IC functions from the eight output channels' turn on/off to the controller interface selection and the diagnostics status. You can access to all registers of the IC via serial or parallel interface and all the information about IC status and configuration.

To demonstrate the IC functionality in an application like environment and to facilitate a simplified and convenient evaluation of the IC with a PC, an Infineon PSOC™ 4 microcontroller is added on the board as a gateway. The communication between PC and controller can be handled with a terminal software tool. The microcontroller section of the evaluation board can also be broken apart to allow the evaluation with other microcontroller types or as a break-out board.

3.1 Connector for the eight output channels

The primary function of the ISO2H823V2.5 is to control the eight output channels with 0.5 A current capability at 24 V. The control of the output switches is done by accessing the IC register named "DRIVE" and writing the desired 8-bit configuration for the output status ('1' for channel ON, '0' for channel OFF). The datasheet contains the complete description of all registers and the possibilities to access them for reading or writing.

The connector of the eight output channels can be wired individually with different load types, resistive, inductive, or capacitive loads. For IC maximum load capability but also for the maximum allowed switch-off energy, see the datasheet and Safety limits for ISO2H8xx-ICs application note.

The GND of the eight loads attached to the board can either be connected to the GND_{BB} terminal of the board or to the GND terminal of the V_{BB} power supply.

3.2 Connector for the 24 V field side supply

A nominal voltage supply of 24 V has to be provided at the 24 V output-side connector. This connector supplies V_{BB} of the output-side of the IC and sources all eight output channels. Therefore, the total current supply capability must be at least the sum of all eight applied output load currents plus 15 mA to supply the IC.

3.3 Isolation barrier

The IC has an integrated galvanic basic isolation rated at 2.5 kV_{rms} that isolates the 3.3 V control side of the IC from the 24 V field side. In an industrial automation application, this isolation is required to protect the low voltage controllers from the harsh factory floor environment (according to IEC 61131-2 standards).

Being galvanically separated, all the voltages at the control-side are referred to GND and all the voltages at the output-side are referred to output-side supply negative (GND_{BB} in the IC datasheet).

3.4 3.3 V control side

The control pins of the eight output channels are located on the control side, which is powered with nominal 3.3 V. If the board is connected via USB to the PC, its 5 V supplies power to the board and in this case no other supply is needed for the control side. Otherwise 3.3 Vcc needs to be supplied via a J1 jumper from an external power supply.

3.5 Diagnostics

The ISO2H823V2.5 provides next to global diagnostic features like V_{BB}-monitoring and channel resolved diagnostic capability. The latter allows to derive diagnostic information for each individual channel comprising short-circuit to GND, short circuit to V_{BB}, open load condition in off and in on state as well as channel overtemperature. The diagnostic information is transferred across the isolation and can be retrieved from the 3.3 V controller side by reading the corresponding IC register contents.

3.6 Side connectors for daisy chain

The ISO2H823V2.5 IC supports SPI in daisy chain configuration in SPI Mode 0 and SPI Mode 1. Daisy chain configuration allows to control multiple ICs with the lowest number of GPIOs. The daisy chain configuration is not supported by the current firmware version of the uC but the board is prepared to support the hardware-based daisy-chaining of ICs through the side connectors for the usage as breakout-boards in conjunction with custom software.

3.7 PSOC™4 MCU as gateway between board and PC

The protocols used for the information exchange between the microcontroller and the IC are described in the datasheet. The data transfer can be monitored by probing the pins of the interface connector for protocol functionalities and timings (see Figure 2 for details).

The controller is preloaded with firmware. The task of this firmware is only to provide a gateway functionality between the IC and the USB port so that the board can be used with also with a terminal software tool without further programming effort. You can overwrite the firmware via the PSOC™ 4 programmer port connector using the Infineon MiniProg programmer tool to use your own software.

The description and the examples of usage shown later in this document are based on firmware version ISO2H823.11.10A_EVAL.

The PSOC™ 4 MCU board can be separated from the IC board by breaking it apart across the holes aligned parallel to the interface connection. This allows to apply a different microcontroller by wiring the new controller GPIOs to the interface connection on the IC board edge. The I/O pin functionalities are described in detail in the datasheet of the ISO2H823V2.5. When the two sections of the boards are separated, a dedicated 3.3 V supply is needed for the ISO2H823V2.5 board at the V_{CC} pin of the interface connection that replaces the USB supply of the microcontroller board.

Note:

- Do not invert the supply polarity of V_{BB} at J3 jumper (24 V supply the output side) because the board is not protected against reverse polarity.
- At the output eight-channel connector, do not apply voltages higher than supply voltage V_{BB} as this leads to an inverse current condition due to conduction over the body diodes and can cause excessive or even destructive power dissipation.
- The interface selection connector is read during startup to configure the IC. To switch between parallel and serial (SPI) or direct, change the jumper position J4 and press the reset button to re-initialize the IC. For changing the SPI interface (J4 selected correspondingly) from one mode to another, follow the same sequence after changing SPI-mode via J5 jumper.

4 Set up the evaluation board interface to the PC

4.1 Configuring the evaluation board interface to the PC

4.1.1 Install the terminal software

Several terminal software tools are available on the Internet. Setup the software with the USB HID ID: **Cypress Semi (VID:04B4) MyUSB (PID:00AA)**.

The following description uses the YAT terminal software as an example.

For using the board with YAT terminal, create a setup file or load an existing setup file. To simplify the usage of YAT, Infineon provides a setup file as a download that provides all commands needed to communicate with the evaluation board (*ISO2H823V_B1v0.yat)*. To load the setup that configures the connection to the ISOFACE™ evaluation board, choose **File** > **Open**, browse, and select the *filename.yat* file.

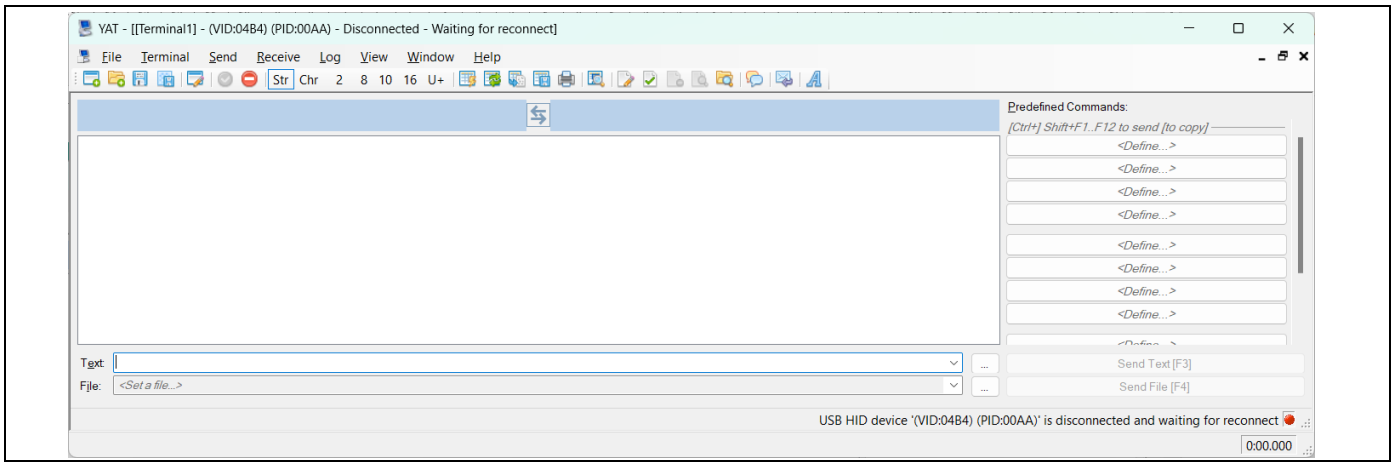

Figure 3 YAT terminal software tool after startup

The provided configuration file can be modified according to individual needs or a new file can be generated from scratch by choosing **File** > **New Terminal** and then following the steps as shown in Figure 4 after the board has been connected to the USB port of the computer.

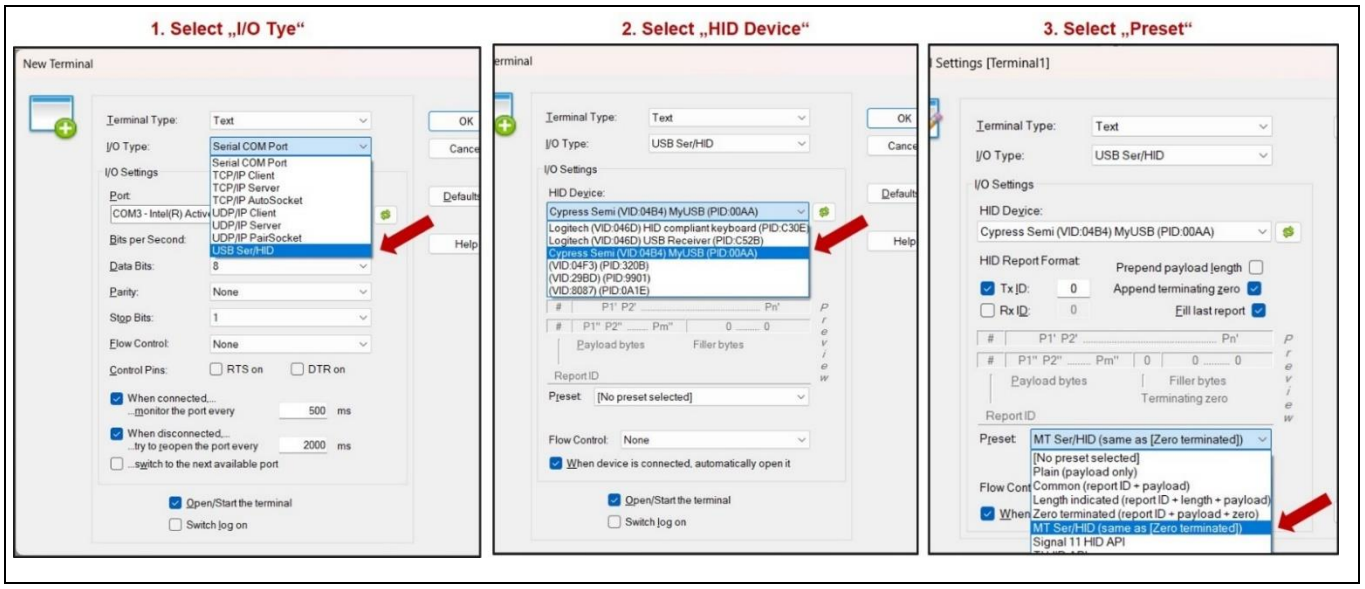

Figure 4 **Creating a new YAT terminal for communication with the ISOFACE™ evaluation board**

Note: *When the YAT terminal is closed and started again, it automatically loads the last-used configuration; you do not need to load it manually again.*

4.1.2 Configure jumper settings of the board

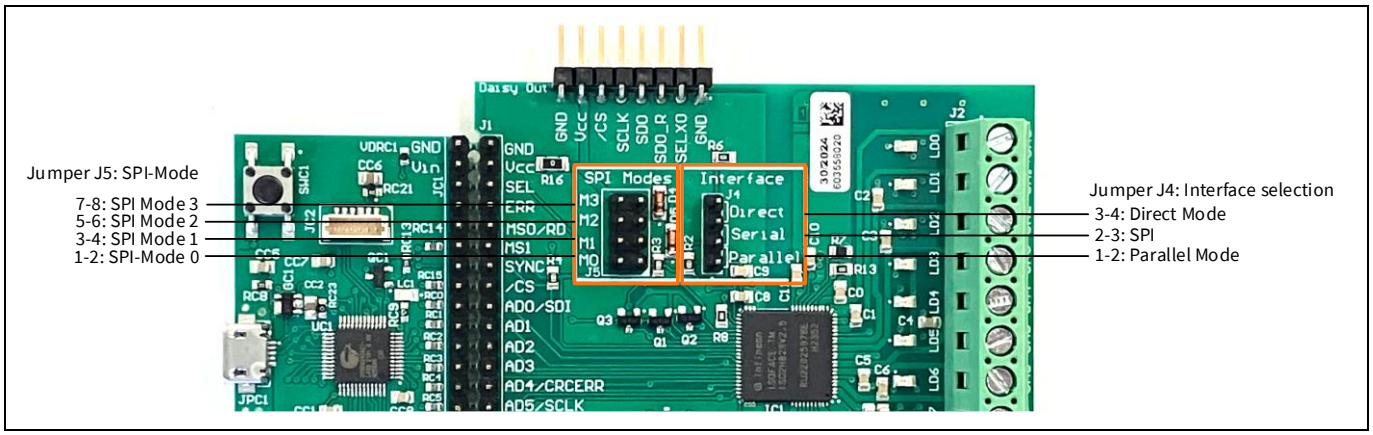

Figure 5 **Interface selection configuration via jumpers**

Modes

Before using the board, configure the desired interface by selecting the corresponding jumper settings. The board supports all three available interface options, serial (SPI), parallel, and direct (parallel) interface to control the IC and therefore, the related output switches.

Serial mode

The serial interface (SPI) supports 4 different SPI modes for 8, 16, and 24-bit transfer per frame. Select the individual SPI-mode by J5 jumper after the J4 jumper has been configured to **Serial**. The SPI interface allows a very efficient control of the IC with the lowest number of control pins and at the same time supports the usage of the sophisticated pin-resolved diagnosis including overload, short-circuit, and open load (in active and inactive mode) as well as overtemperature for each individual output channel.

Parallel mode

Select the parallel interface by setting the J4 jumper to **Parallel**. The parallel mode uses next to eight I/O pins (AD0-AD7) four additional logic signals (/CS, ALE, /WT, and /RD) to control the IC. By this, write- and read-access to the registers are possible and the complete set of pin-resolved diagnosis features are available to full extent also in parallel mode. If the parallel interface is selected via J4 jumper, leave the unused J5 jumper open.

Changing from serial mode to parallel mode and vice versa is possible while the board is supplied via the USB connection but after having changed the interface type via the J4 jumper a reset has to be executed to re-configure the IC. This can be done by pressing the IC-reset button of the microcontroller section of the board. The same holds true if in serial mode, the SPI mode is changed via the J5 jumper from one SPI mode to another. The SPI modes and the parallel interface types are explained in the datasheet.

Direct mode

The direct parallel mode is an optocoupler emulation function where the behavior is similar as if the switches were controlled via optocouplers. In this mode, the eight output switches will follow continuously the logic levels of the signals that are applied to the input pins (AD0-AD7) without a protocol. No other logic signals next to the input signals are needed in this case and the microcontroller is idle. This mode can also be used if the MCU part of the evaluation board has been removed. In contrast to the other interface modes, in direct mode, the inputs are not bidirectional. This means that in direct mode the channel resolved diagnostic information cannot be read and therefore, channel resolved diagnostics are not available. For the same reason no register accesses (Read or Write) can be made to the device. Only a global diagnosis flag on the /ERR pin is available in direct mode.

Connecting the evaluation board

When the evaluation board is connected to a USB port of the PC, the YAT terminal software will start and the configuration file *ISO2H823V_B1v0.yat* is loaded, the evaluation board will be detected automatically. The dot at the bottom right turns to green and a message appears to indicate a successful connection on the YAT terminal.

4.1.3 Communication with the evaluation board

When using the SPI or the parallel interface, the evaluation board can be accessed in the following three ways:

1. **Read or Write register commands**

- **READ(register short name)**: Data read from the corresponding register is provided in hexadecimal format. Depending on the selected interface or SPI mode, the answer will consist of 8, 16, or 24 bits.
- **WRITE(register short name, data(XX_H))**: Hexadecimal XX_H data will be written to the corresponding register.

Table 3 READ or WRITE registers

Short name	Register name	Read/write
DRIVE	Output Driver Register	rw
DRIVE_RESYNCH	Output Driver Register for Resynchronization	rw
COLDIAG	Collective Diagnostics Register	r
GLERR	Global Error Register	r
DIAGCFG	Channel Diagnostics Configuration Register	rw
DIAG0	Diagnostics Register for Channel-0	r
DIAG1	Diagnostics Register for Channel-1	r
DIAG2	Diagnostics Register for Channel-2	r
DIAG3	Diagnostics Register for Channel-3	r
DIAG4	Diagnostics Register for Channel-4	r
DIAG5	Diagnostics Register for Channel-5	r
DIAG6	Diagnostics Register for Channel-6	r
DIAG7	Diagnostics Register for Channel-7	r
INTERR	Internal Error Register	r
GLCFG	Global Configuration Register	rw

2. **Queries for IC status information (command_name+?)**

- **FLAGS?**: This command reads and outputs the logic state values of the relevant configuration pins and the error flag
- **MODE?**: Outputs the selected interface mode
- **FW?**: Outputs the firmware version
- **HW?**: Outputs the hardware version
- **IC?**: Outputs name of the IC

3. **Specific pin commands (command_name+logic_state)**

- **ODIS+logic_state**
  - ODIS0: Sets ODIS-pin to logic state ‘0’ (disables immediately all outputs)
  - ODIS1: Sets ODIS-pin to logic state ‘1’ (resets the deactivation of the outputs, outputs can be switched on again)
- **SYNC+logic_state**
  - SYNC0: Sets SYNC-pin to logic state ‘0’
  - SYNC1: Sets SYNC-pin to logic state ‘1’
- **ALE/RST+logic_state**
  - ALE/RST0: Sets ALE/RST-pin to logic state ‘0’
  - ALE/RST1: Sets ALE/RST-pin to logic state ‘1’

Note that those means of communication with the IC are not available in direct mode. In direct mode, only the output switches can be controlled by applying the corresponding logic signals to the input pins (A0 to A7).

Diagnostic capabilities in direct mode are limited to the global error flag (/ERR) indicating an overtemperature incident or a non-powered field side (W4P).

4.2 Board startup procedure

After providing the supply voltage at the V_{BB} and GND connectors and connecting the USB cable to the PC, the LEDs on the board should light up as shown in Figure 6. Note that after startup the diagnostic bits for W4P (Wait for Power), TE (Transmission Error) of the Internal Error Register INTERR as well as the bits for UV (V_{BB}-Undervoltage), and MV (V_{BB}-Missing Voltage) of the Global Error Register GLERR are set by default. The mentioned diagnostic bits that are stored in the corresponding registers are flagged in addition as a logic low state on the /ERR pin (red LED lights up).

As these diagnostic register bits are sticky bits the corresponding registers have to be read twice after startup to obtain the actual situation. The first read will show accumulated fault information during power up (i.e., MV, UV, TE, and W4P). After reading the diagnostic information, the corresponding bits will be cleared in the registers if the fault condition has been resolved prior to the read access. Any subsequent read access consequently will deliver the actual condition after power up. The flag on the /ERR pin however will be reset already after the first read as the diagnostic register bits are cleared after the first read. The sticky behavior of these diagnostic bits ensures that also transient problems can be tracked by the system. Therefore, the sticky diagnosis bits will be cleared only if the diagnostics event has vanished AND the corresponding bits of the registers have been read by the master.

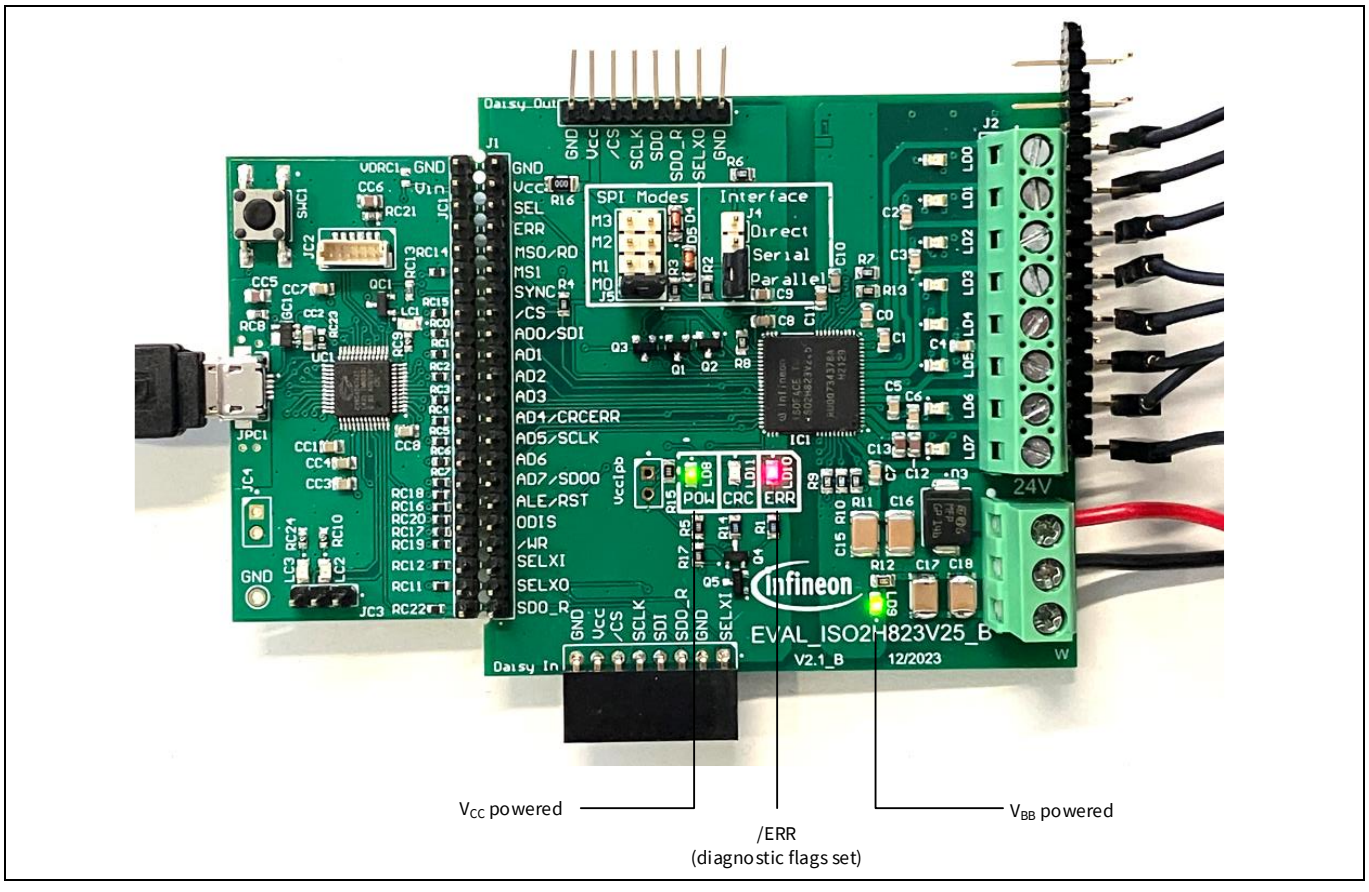

Figure 6 Board status after startup

In general, the occurrence of diagnostic events will be OR-wired and reported as a logic low state on the /ERR pin. However, depending on the used interface mode different diagnostic events will contribute to the /ERR flag. An overview of the diagnostic events that contribute to the /ERR flag is in Table 4. Note that in direct mode flags are not sticky and will be reset as soon as the fault situation has resolved.

Table 4 Diagnostic events

Short name	Serial communication SPI				Parallel mode	Direct mode
	Mode 0	Mode 1	Mode 2	Mode 3		
UV (undervoltage)	Yes	Yes	Yes	Yes	Yes	–
MV (missing voltage)	Yes	Yes	Yes	Yes	Yes	–
CF (channel fault)	–	–	–	–	Yes	–
TE (transmission error)	Yes	Yes	Yes	Yes	Yes	–
W4P (wait for power)	Yes	Yes	Yes	Yes	Yes	Yes
OTC (overtemperature/overcurrent	–	–	–	–	–	Yes

4.2.1 Reset of diagnostic flags after startup

As after board startup the above-mentioned diagnostic flags are set by default, the red /ERR LED will light up. Therefore, reset the diagnostic flags to switch off the /ERR LED in order that actual diagnostic events can be tracked. Provided that after startup no further diagnostic event is present (e.g. open load condition/wire-break on one of the output channels) the following actions will reset the diagnostic bits and the /ERR flag after startup:

Parallel mode:

- Issue a read to the Internal Error Register INTERR followed by a read to the Global Error Register GLERR (or vice versa)

Serial mode:

- SPI Mode 3:
  - Issue a read command to the Internal Error Register INTERR (note that in this specific case reading of INTERR is sufficient as the frame will also report the bits of the GLERR register)
- SPI Mode 2:
  - Issue a read to the Internal Error Register INTERR followed by a read to the Global Error Register GLERR (or vice versa)
- SPI Mode 1 (only WR accesses are possible):
  - Any write command will reset the /ERR flag
- SPI Mode 0 (only WR accesses are possible):
  - Any write command will reset the /ERR flag

Direct Mode:

- In direct mode, the behavior of flags on the /ERR pin are not sticky, the /ERR flag will be reset as soon as the diagnostic event has vanished. No further action has to be taken.

Diagnostic flags and the diagnostic bits are stored for tracking in the corresponding registers will only be reset if the diagnostic events have been resolved AND if the diagnostic errors have been acknowledged by the controller by reading the corresponding registers.

4.2.2 Examples for usage and hints (exemplary for SPI Mode 3)

In the following, the reset process of the diagnosis after startup and the usage of the board are explained in an exemplary way for SPI Mode 3 in conjunction with the usage of the YAT terminal software:

1. **Connect to the board**

After setting up YAT as described in Section 4.1.1, start YAT on the PC, which is connected via USB to the evaluation board and load the YAT configuration file. After the connection is established, it is signaled by the green dot on the bottom right and YAT looks as shown in Figure 7.

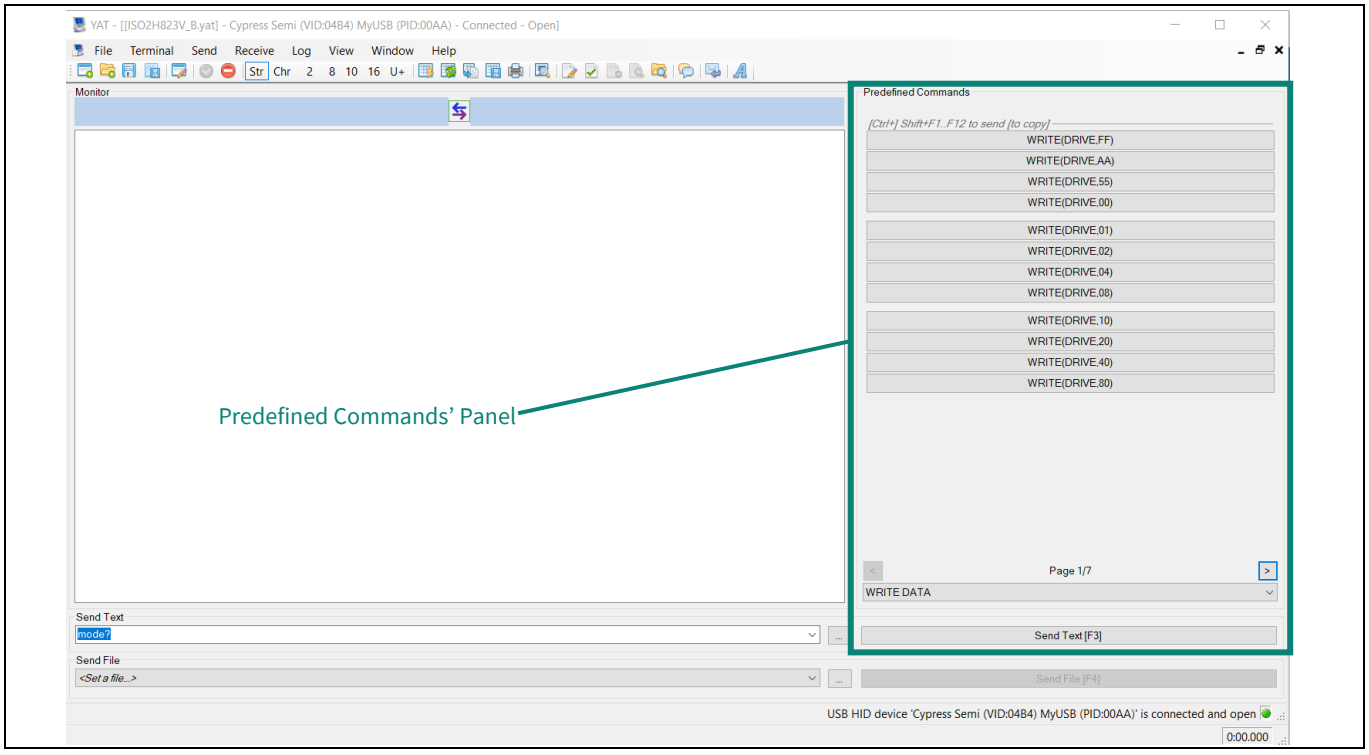

Figure 7 YAT connected to the evaluation board

2. **Reset diagnostic default bits after startup**

It is assumed that V_{BB} is inside the functional range (e.g., 24 V) and all outputs are connected to a load so that no diagnostic warnings will arise out of this. To reset the diagnostic bits that are flagged on /ERR after startup, just read the Internal Error Register (INTERR).

If you are using the provided YAT configuration file *ISO2H823V_B1v0.yat,* click on the predefined command button READ(INTERR) on page 2 of YAT's Predefined Commands panel.

- After the first read execution to the INTERR register, the /ERR led will switch off because the diagnostic bits have been reset by the read access. The answer of the first read command 0007DB shown in Figure 8 contains the diagnostic bits after startup.
- The 2nd byte of the answer 07 contains the content of the addressed register INTERR. Note that the bits “TE” (transmission error), “W4S” (wait for sense), and “ALLOFF” are set.
- The 3rd byte contains next to the CRC information also the bits UV and MV from the GLERR register. This is the reason why for SPI Mode 3, the register GLERR has not to be read explicitly after startup but reading INTERR implicitly also resets MV and UV. If another read to INTERR is issued, you can see that the UV and MV bit of the diagnosis are cleared and inside the register INTERR only the bit ALLOFF remains set. The bit ALLOFF is set because after startup all outputs are OFF by default. The presence of the bit ALLOFF has no impact on the /ERR flag. See also Figure 8 for more details.

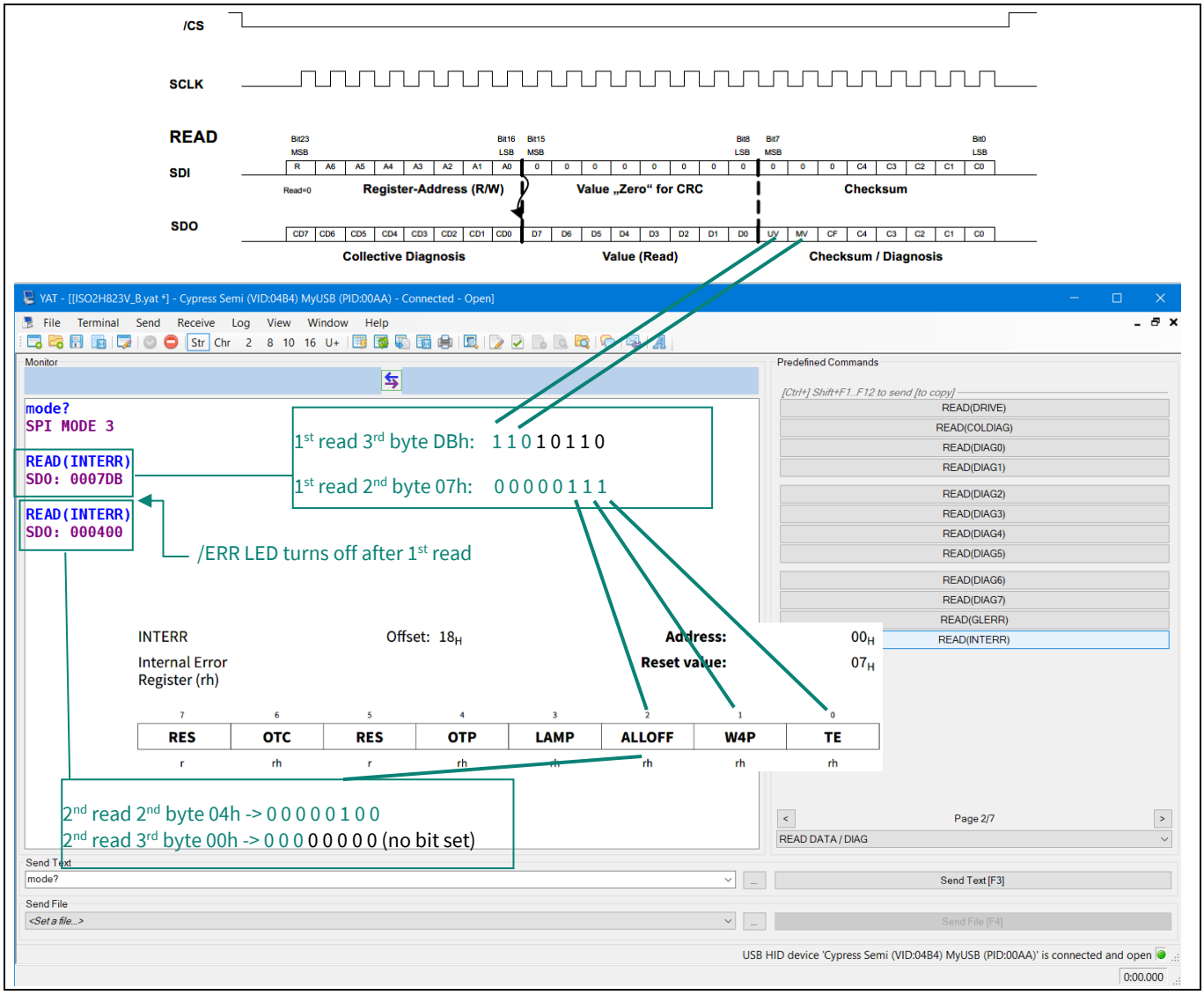

Figure 8 READ(INTERR) and response of the IC after startup

Going on with the example a bit further and switching on 4 out of the 8 channels by writing the corresponding command WRITE(DRIVE, 55) to the DRIVE register the activated switches can be identified by the green output status LEDs that are now lighting up. If you read afterwards again the INTERR register, you still get the response 000400 indicating that the ALLOFF-bit is set. This is because the bit gets cleared by the 1st read after the

diagnostic event has been resolved – so this read still shows the bit but at the same time it is clearing it in the register. This can be seen if the read command to the INTERR register is repeated once again. The response is then 000007 indicating that no bit of the INTERR register is still set. This behavior is shown in Figure 9.

The next example shows how the channel-resolved diagnosis can be obtained. Before creating the diagnostic event, first read the DRIVE register ("READ(DRIVE)") to check the actual status of the outputs. The response from the IC is 005510 meaning the outputs are in the expected state 55 and that no diagnostic bits are present. To create a diagnostic event, just disconnect the load cable of output 0. Note that the output status LED of the affected channel keeps lighting because the output driver itself is still ON but just the cable to the load is removed. If the read command to the DRIVE register is repeated after disconnecting the cable, the updated response is 015527 on SDO. The content of the 1st byte 01 translates to output channel 0 having a diagnostic event. The status of the outputs delivered in the 2nd byte 55 as expected has not changed. The 3rd byte 27 now shows the changed diagnostic bit CF, which is stored in the GLERR register. The global error bit CF stands for "Channel Fault" which is the OR-combination of all bits in the COLDIAG register. The sequence up to this point is shown in Figure 10.

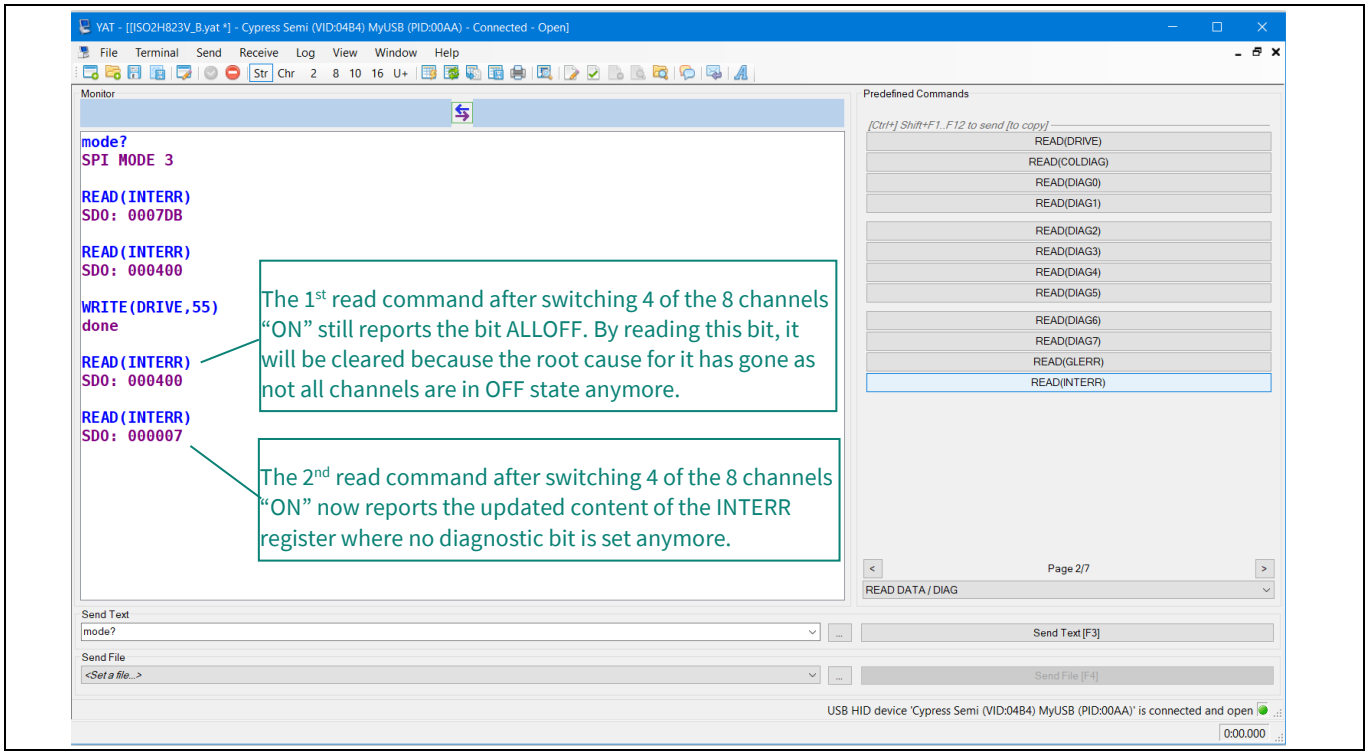

Figure 9 Repeating read access to INTERR register twice after switching on 4 output channels

To get channel-resolved information about the nature of the diagnosed problem, read first the COLDIAG register where the IC reports all channels that have diagnostic warnings. After the read command to the COLDIAG register has been issued, individual read commands to the DIAGx registers of the affected channels reported in the COLDIAG register can be sent. The content of the DIAGx registers reflects the detailed root cause of the diagnosed problem for a given channel.

In this case, the command READ(COLDIAG) reports 010126. As the 2nd byte again is the content of the addressed register (01), it becomes clear that channel 0 is the only affected output. To determine the origin of the diagnosis, the command READ(DIAG0) is sent to the IC that posts 010437 as response. The 2nd byte of the response represents the content of the DIAG0 register. The 04 signifies that the problem is open load in active state OLA0. Details to these commands are shown in Figure 11.

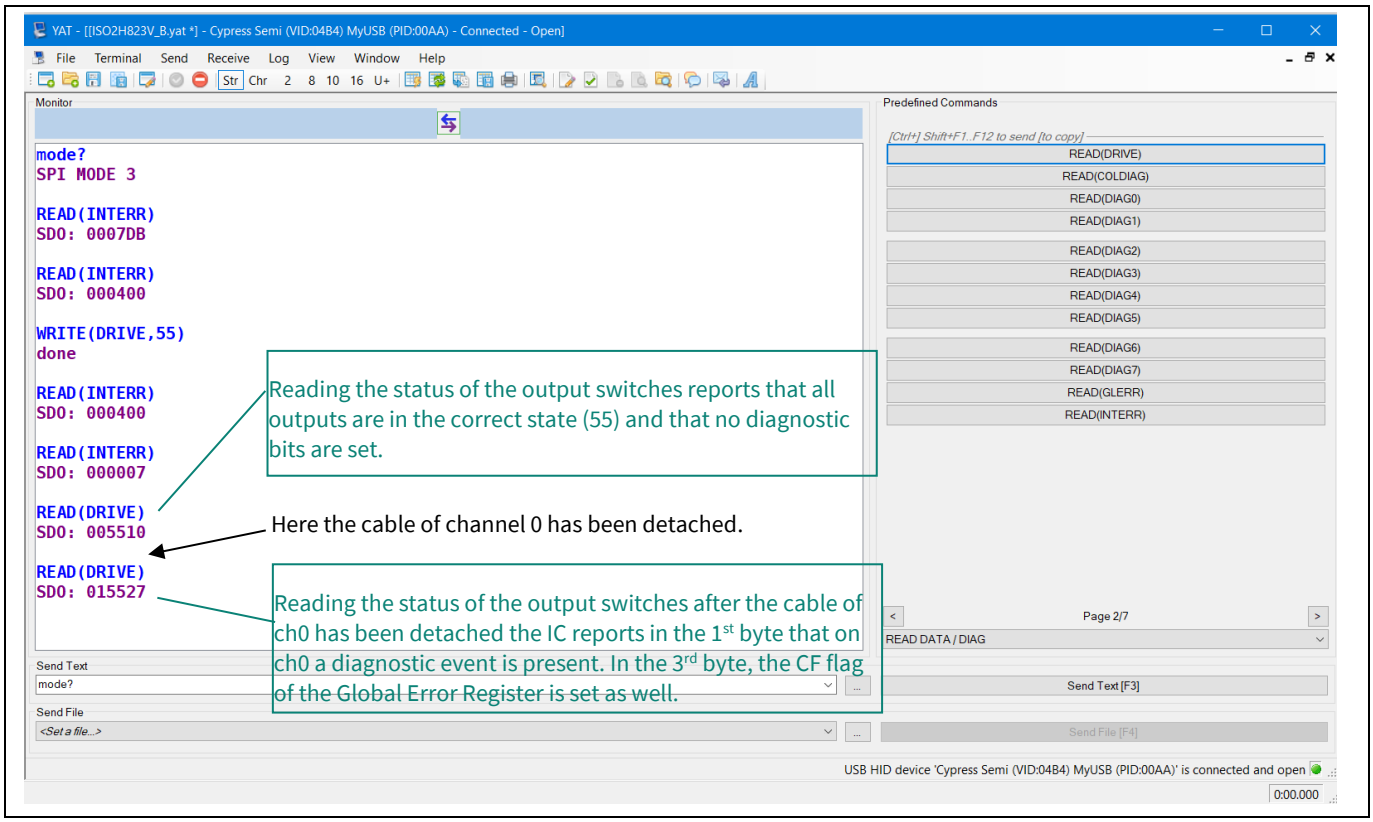

Figure 10 Reading the DRIVE register with and without diagnostic event

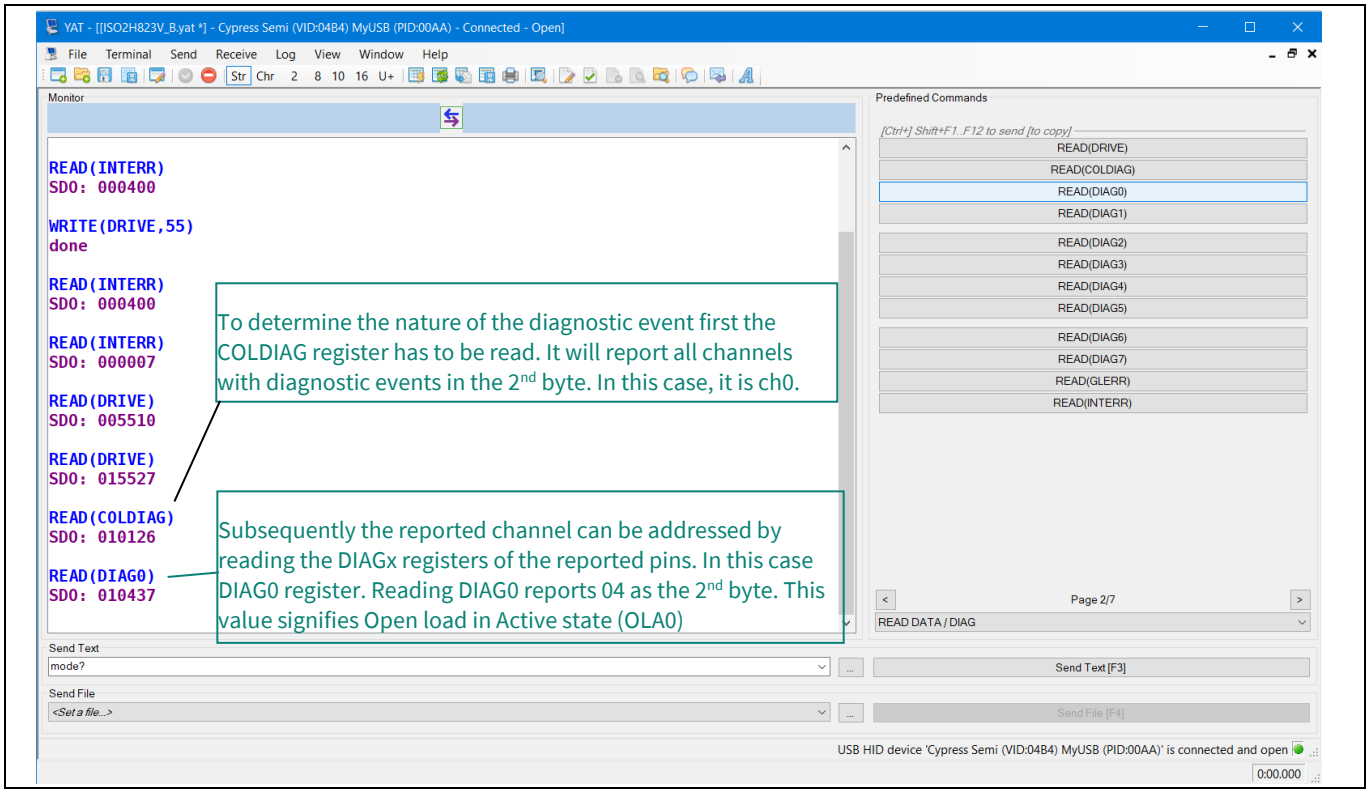

Figure 11 Determining channel resolved diagnosis (read COLDIAG register followed by a read to the corresponding DIAGx register)

4.3 Commands

Table 5 Commands

Command name	Command	Description
Status information	HW?	–
	MODE?	–
	FW?	–
	IC?	–
Pin commands	ODIS0	–
	ODIS1	–
	SYNC0	–
	SYNC1	–
	ALE/RST0	–
	ALE/RST1	–
Read commands	READ (“register”)	–
	DRIVE	Drive register
	GLERR	Global error register
	INTERR	Internal error register
	COLDIAG	Collective diagnosis
	DIAGx	Diagnosis register of channel x
	DIAGCFG	Channel diagnostics configuration register DIAGENx for channel x
	GLCFG	Global configuration register
Write commands	WRITE(“register”, “hh”)	hh denominates the binary representation of the eight output channels in hexadecimal code (hh: 00h to FFh)
	DRIVE	Drive register
	DIAGCFG	Channel diagnostics configuration register DIAGENx for channel x
	GLCFG	Global configuration register

5 Schematics

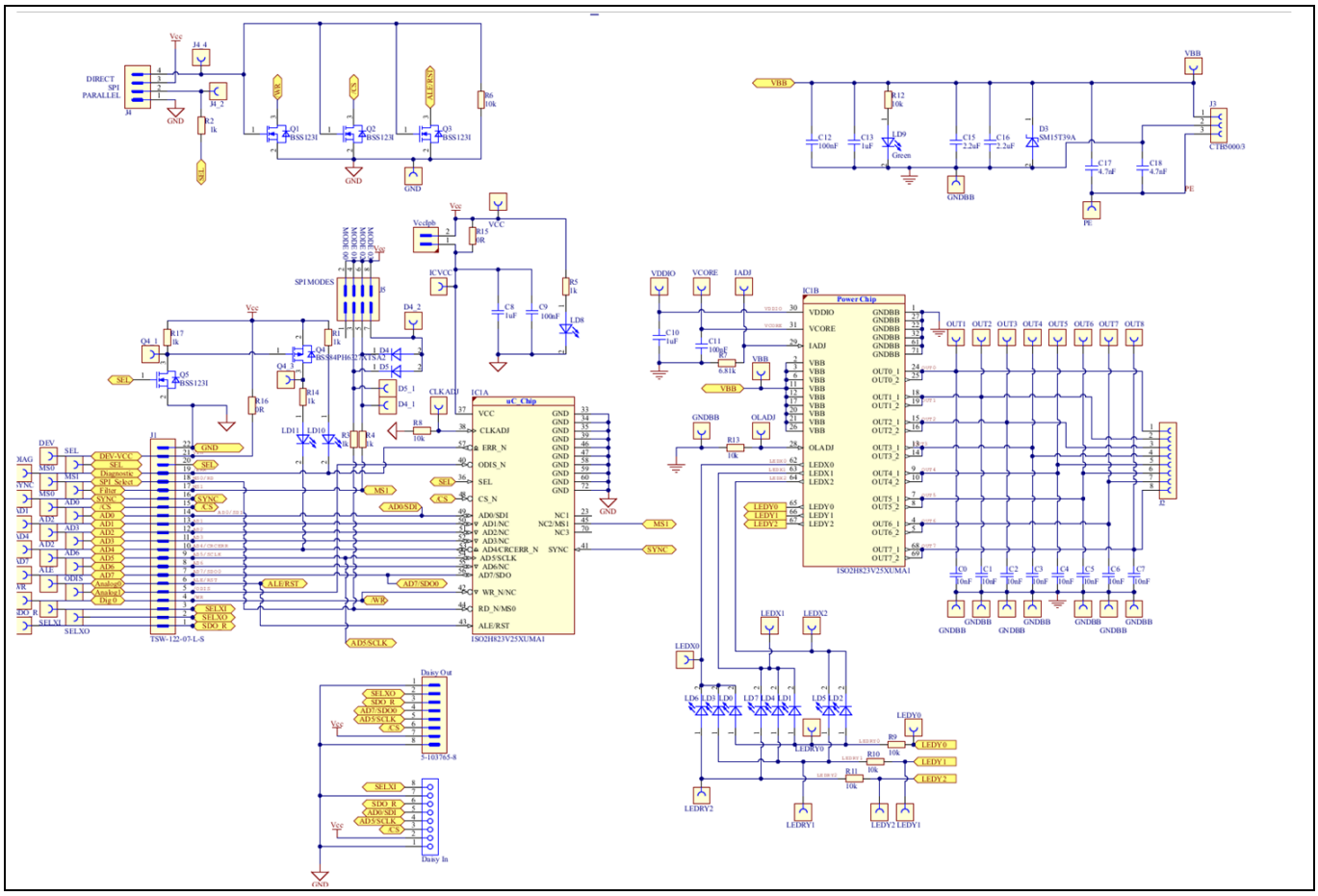

Figure 12 IC board schematics

Schematics

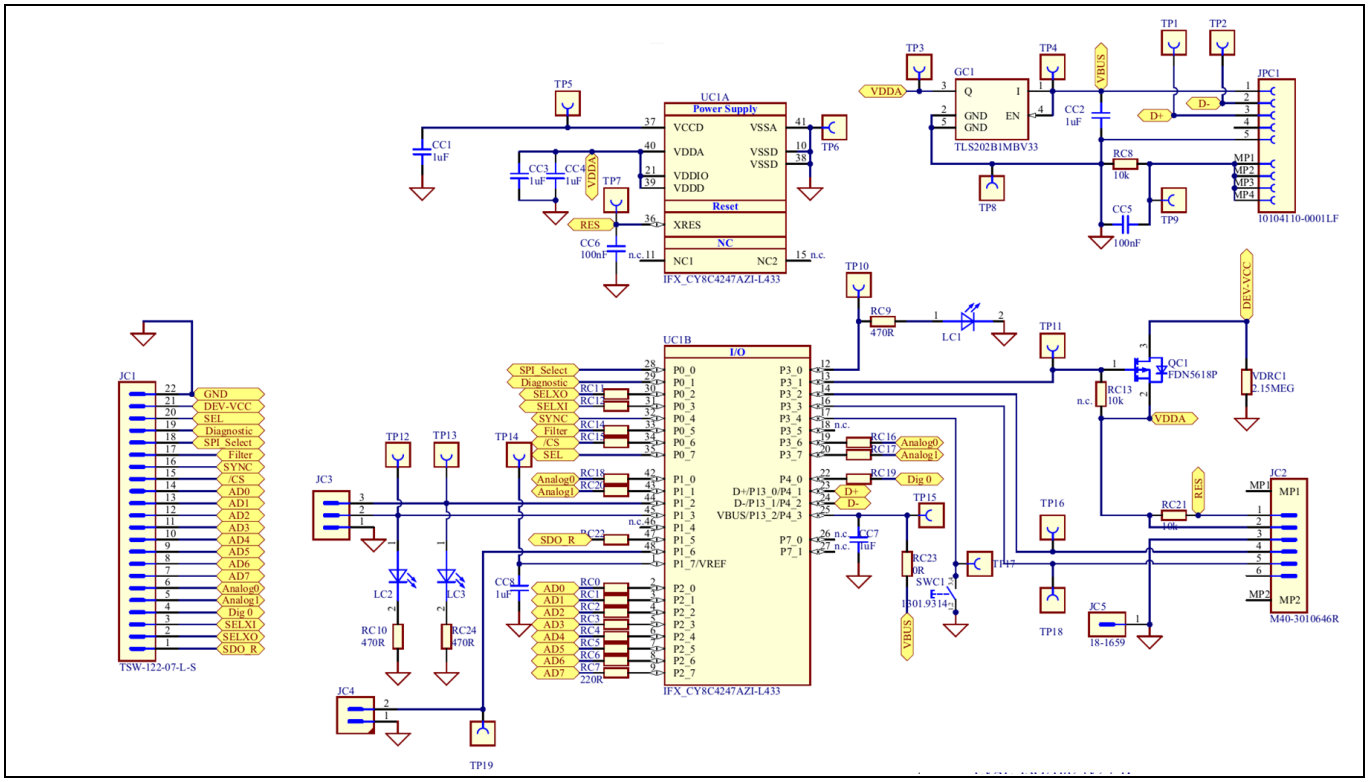

Figure 13 PSOC™ 4 controller board schematics

6 Bill of materials

Table 6 IC board bill of materials

Part	Value	Package
R1, R2, R3, R4, R5, R14, R17	1 kΩ	0805
R6, R8, R9, R10, R11, R12, R13	10 kΩ	0805
R7	6.81 kΩ	0805
R15	0 Ω	0805
R16	0 Ω	1206
C0, C1, C2, C3, C4, C5, C6, C7	10 nF 10% 100 V X7R	0805
C8, C10	1 µF 10% X5R 16 V	0805
C9, C11	100 nF 20% X7R 16 V	0805
C12	100 nF 10% X7R 100 V	0805
C13	1 µF 10% 100 V X7S	0805
C15, C16	2.2 µF 10% 100 V X7R	1812
C17, C18	4.7 nF 1 kV 5% U2J	1812
D4, D5	BAT165 [or LL4148]	SOD-80
D3	SM15T39A	SMC
LD0, LD1, LD2, LD3, LD4, LD5, LD6, LD7, LD8, LD9	LED green (KP-2012CGCK)	0805
LD10, LD11	LED red (KP-2012SRC-PRV)	0805
Q1, Q2, Q3, Q5	Transistor BSS123	SOT-23
Q4	Transistor BSS84PH6327XTSA2	SOT23
IC1	**ISO2H823V2.5**	–
J1	Header 2.54 mm 22p x 1 row straight	–
J2	Terminal Block (8 wire, 5 mm PCB, screw)	–
J3	Terminal Block (3 wire, 5 mm PCB, screw)	–
J4	Header 2.54 mm 4p x 1 row straight	–
J5	Header 2.54 mm 4p x 2 rows straight	–
Daisy in	Header 2.54 mm 8p x 1 row 90 degrees female	–
Daisy out	Header 2.54 mm 8p x 1 row 90 degrees male	–

Bill of materials

Table 7 Controller board bill of materials

Part	Value	Package
RC23	Resistor 0 R	0603
RC8, RC13, RC21	Resistor 10k 1%	0603
RC0, RC1, RC2, RC3, RC4, RC5, RC6, RC7, RC11, RC12, RC14, RC15, RC16, RC17, RC18, RC19, RC20, RC22	Resistor 220 R 1%	0603
RC9, RC10, RC24	Resistor 470 R 5%	0603
VDRC1	Resistor 2.15MEG 75 V 1%	0603
CC1, CC2, CC3, CC4, CC7, CC8	Ceramic capacitor 1 µF 16 V ±10% X5R	0805
CC5, CC6	Ceramic capacitor 0.1 µF 100 V ±10% X7R	0805
LC1, LC2, LC3	LED red (KP-2012SRC-PRV)	0805
GC1	TLS202B1MBV33 fixed LDO voltage regulator 3.3 V 150 mA	SCT-595-5
QC1	FDN5618P power MOSFET P-channel 60 V 1.2 A 0.17 Ω	Super SOT
UC1	CY8C4247AZI-L433	TQFP 48
JC1	Header male 22 positions 2.54 mm pitch	–
JC2	M40-3010646R programmer connector SIL SMT MALE 6-way	–
JC3	Header male 3 positions 2.54 mm pitch	–
JC4	Header male 2 positions 2.54 mm pitch	–
JC5	Header male 1 positions 2.54 mm pitch	–
JPC1	Connector RCPT USB2.0 MICRO B SMD R/A	–
SWC1	SWITCH TACTILE 0.05A 12 V	–

Revision history

Document revision	Date	Description of changes
V 1.0	2024-11-18	Initial release

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2024-11-18

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

UM145822

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.