IRS2890DS – Half-Bridge Gate Driver IC with Over Current Protection and Fault / Enable

IRS2890DS Technical Description

About this document
Scope and Purpose

The scope of this application note is to describe the basic features of the IRS2890DS and how to use the device within the recommended operating range. This document helps to design the necessary external circuitry for bootstrap and interfacing functions. Click to buy IRS2890DS online.

Intended Audience

Power electronics engineers who want to design reliable and efficient half-bridge gate drives with overcurrent protection.

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1 Scope

The scope of this application note is to describe the basic features of the IRS2890DS and how to use the device within the recommended operating range. This document helps to design the necessary external circuitry, such as bootstrap and interfacing. To meet the customer demands for higher power density, Infineon has developed a half-bridge gate driver with integrated overcurrent protection, a fault/enable function and a bootstrap FET for a variety of applications.

2 Product overview

2.1 Internal block diagram and features

Figure 1 illustrates the internal block diagram of the IRS2890DS.

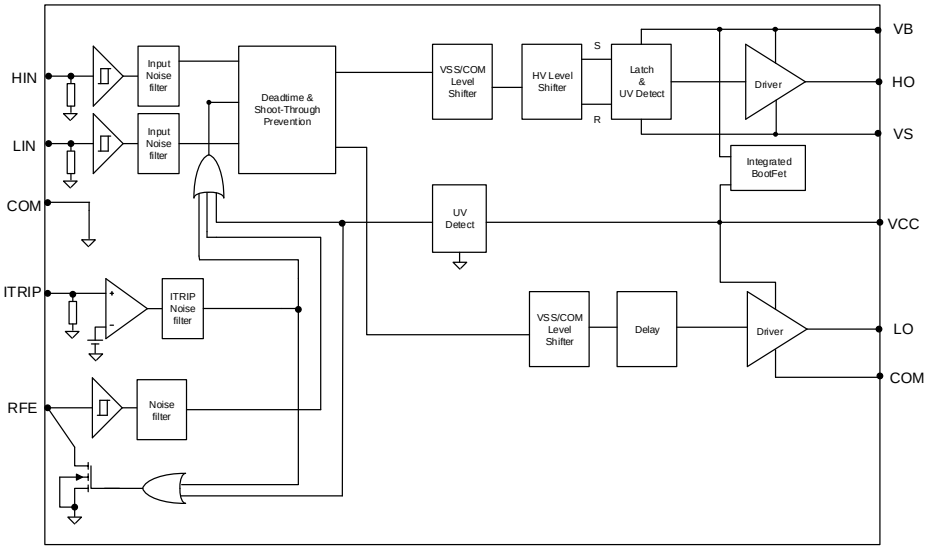

Figure 1 Internal block diagram

The detailed features and integrated functions of IRS2890DS are listed below:

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V, 5 V, and 15 V input logic-compatible
- Matched propagation delay for both channels
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs
- Integrated bootstrap FET
- Suitable for both trapezoidal and sinusoidal motor control
- Overcurrent protection, fault reporting and enable
- **Functions**
- Overcurrent shutdown
- Undervoltage lockout for both high-side and low-side
- Cross-conduction prevention
- All switches turn off during protection
- Active-high input signal logic

2.2 Maximum electrical ratings

Table 1 Detailed description of absolute maximum ratings

Symbol	Definition	Min.	Max.	Units
VB	High-side floating supply voltage	-0.3	625	V
VS	High-side floating supply offset voltage	VB - 25	VB + 0.3	
VHO	High-side floating output voltage	VS - 0.3	VB + 0.3	
VCC	Low-side and logic fixed supply voltage	-0.3	25	
VLO	Low-side output voltage	-0.3	VCC + 0.3	
VIN	Logic input voltage (LIN, HIN, RFE, ITRIP)	COM -0.3	VCC + 0.3	
dVS/dt	Allowable offset supply voltage transient	—	50	V/ns
TJ	Junction temperature	—	150	°C
TS	Storage temperature	-50	150	
TL	Lead temperature (soldering, 10 seconds)	—	300	

Table 1: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board-mounted and still-air conditions.

2.3 Description of the input and output pins

Table 2: defines the IRS2890DS input and output pins. The detailed functional descriptions are as follows:

Table 2 Pin descriptions of IRS2890DS

Pin Number	Pin Name	Pin Description
1	VCC	Low-side and logic fixed supply
2	HIN	Logic input for high-side gate driver output (HO), in phase
3	LIN	Logic input for low-side gate driver output (LO), in phase
4	ITRIP	Analog input for overcurrent shutdown. When active, ITRIP shuts down outputs and activates FAULT low. When ITRIP becomes inactive, FAULT stays active low for an externally set time T_{FLTCLR}, then automatically becomes inactive (open-drain high impedance).
5	NC	
6	COM	Low-side return
7	RFE	Integrated fault-reporting function like overcurrent (ITRIP), or low-side undervoltage lockout and the fault-clear timer. This pin has negative logic and an open-drain output. The use of overcurrent protection requires the use of external components.
8	NC	
9	LO	Low-side gate drive output
10	NC	
11	NC	
12	VS	High-side floating supply return
13	HO	High-side gate drive output
14	VB	High-side floating supply

Product overview

High-side bias voltage pins for driving the high-side device (IGBT or Mosfet)

Pins: VB – VS

- These pins provide the gate drive power to the high-side device.
- The ability to utilize a bootstrap circuit scheme for the high-side device eliminates the need of external power supplies.
- The bootstrap capacitor is charged from the VCC supply during the ON-state of the low-side device or the freewheeling state of the low-side freewheeling diode.
- In order to prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted very close to these pins.

Low-side bias voltage pin

Pin: VCC

- This is the control supply pin for the internal IC.
- In order to prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted very close to this pin and COM pins.

Low-side common supply ground pin

Pin: COM

- This pin connects the control ground for the internal IC.

Signal input pins

Pins: HIN, LIN

- These are pins to control the operation of the external device.
- They are activated by voltage input signals. The terminals are internally connected to a Schmitt trigger circuit composed of 5 V - class CMOS.
- The signal logic of these pins is active-high. The device associated with each of these pins will be turned "ON" when a sufficient logic voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the IRS2890DS against noise influences.
- To prevent signal oscillations, an RC coupling is recommended as illustrated in Figure 3.
-
- **Gate drive output pins**

Pins: HO, LO

- There pins are connected to the gate of IGBTs or Mosfets by gate resistors to turn on or turn off these power devices.
- To prevent oscillations, a gate resistor is needed to be in series with these pins and the gate of IGBT or Mosfet.

Overcurrent detection pin

Pin: ITRIP

- The current-sensing shunt resistor should be connected between the pin (emitter of low-side IGBT or source of low-side Mosfet) and the power ground to detect short-circuit current (refer to Figure 5). An RC filter should be connected between the shunt resistor and the pin ITRIP to eliminate noise.

- The integrated comparator is triggered, if the voltage V_{ITRIP} is higher than 0.5 V. The shunt resistor should be selected to meet this level for the specific application. In case of a trigger event, the voltage at pin RFE is pulled down to low.
- The connection length between the shunt resistor and ITRIP pin should be minimized.

Fault output, Fault clear timer and Enable pin

Pin: REF

- This is the fault output alarm pin. An active low output is given on this pin for a fault-state condition in the IRS2890DS. The alarm conditions are overcurrent detection and low-side bias UV (undervoltage) operation.
- The RFE output is open-drain configured. The RFE signal line should be pulled up to the logic power supply (5 V or 3.3 V) with proper resistance and capacitor between RFE and COM pins to program fault clear time.
- Externally pulling down the pin can disable the output; for normal operation, the pin needs to be pulled up.
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2.4 Outline drawings

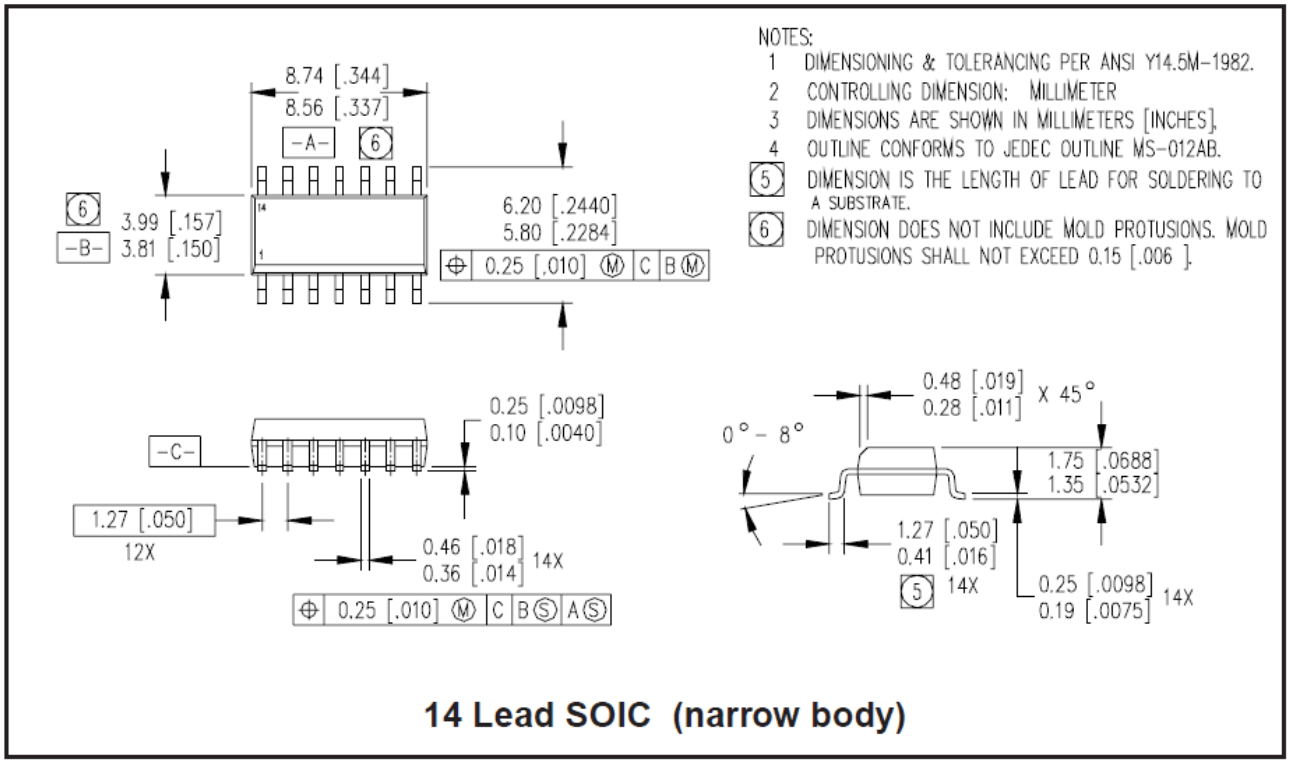


Figure 2 Package outline dimensions

3 Interface circuit and layout guide

3.1 Input/Output signal connection

Figure 3 shows the I/O interface circuit between a microcontroller and the IRS2890DS. The IRS2890DS input logic is active-high with internal pull-down resistors. The RFE output is an open-drain configuration. This signal should be pulled up to 5 V or 3.3 V by an external logic power supply with a pull-up resistor. The pull-up resistor and capacitor connected to the RFE pin should be selected according to the desired fault clear time.

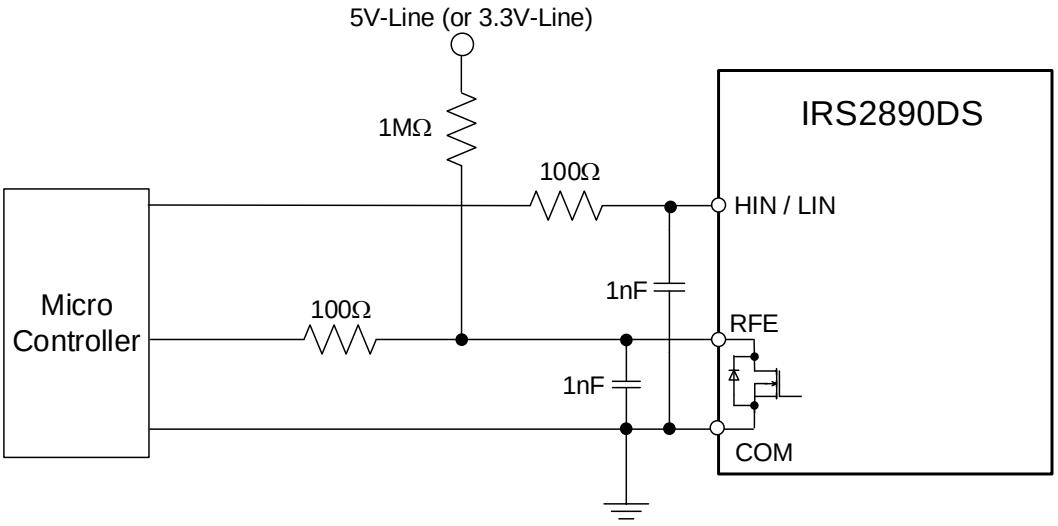


Figure 3 Recommended microcontroller I/O interface circuit

Table 3 Maximum ratings of input and RFE pins

Item	Symbol	Condition	Rating	Unit
Power supply voltage	VCC	Applied between VCC and COM	25	V
Input voltage	VIN	Applied between HIN and COM, LIN and COM	-0.3 ~ VCC+0.3	V
Fault output supply voltage	RFE	Applied between RFE and COM	-0.3 ~ VCC+0.3	V

The input and fault output maximum rating voltages are listed in Table 3. Since the fault output is open-drain configured and its rating is VCC+0.3 V, a 15 V supply interface is possible. However, it is recommended that the fault output be configured with the 5 V logic supply, which is the same as the input signals. It is also recommended to place bypass capacitors as close as possible to the RFE and COM.

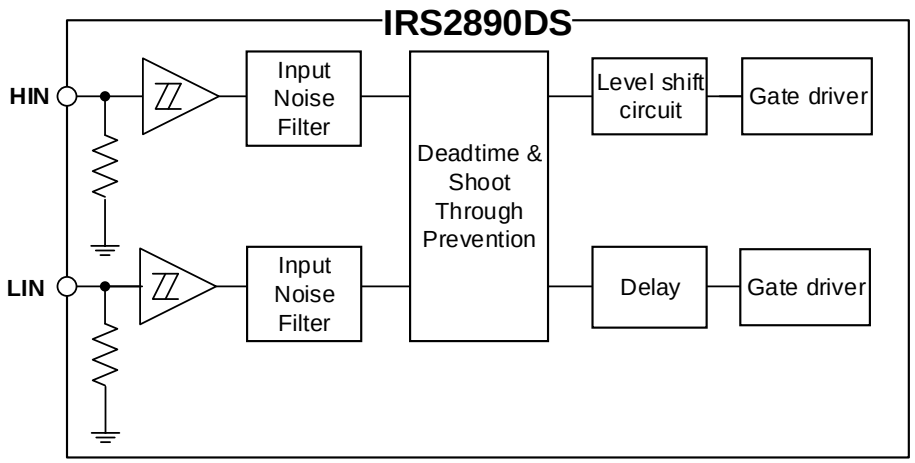


Figure 4 Simplified block diagram of IRS2890DS control IC

The IRS2890DS input pins include pull-down resistors, input Schmitt triggers, noise filters, deadtime and shoot-through prevention functions for better noise immunity. The input pins are compatible with 3.3 V microcontroller or DSP. Table 4 shows the logic input threshold.

Table 4 Input threshold voltage (at VCC = 15 V, T_J = 25 ℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic "1" input voltage (LIN, HIN)	V_{IH_TH}	HIN – COM LIN – COM	2.2	—	—	V
Logic "0" input voltage (LIN, HIN)	V_{IL_TH}		—	—	0.8	V

As shown in Figure 4, the IRS2890DS input signal section integrates a pull-down resistor. Therefore, when using an external filtering resistor between microcontroller output and IRS2890DS input, pay attention to the signal voltage drop at the IRS2890DS input terminals. It should fulfill the logic "1" input voltage requirement. For instance, R = 100 Ω and C = 1 nF for the parts shown in Figure 3.

3.2 General interface circuit example

Figure 5 shows the typical application circuit of IRS2890DS for interface schematic with control signals connected directly to a microcontroller.

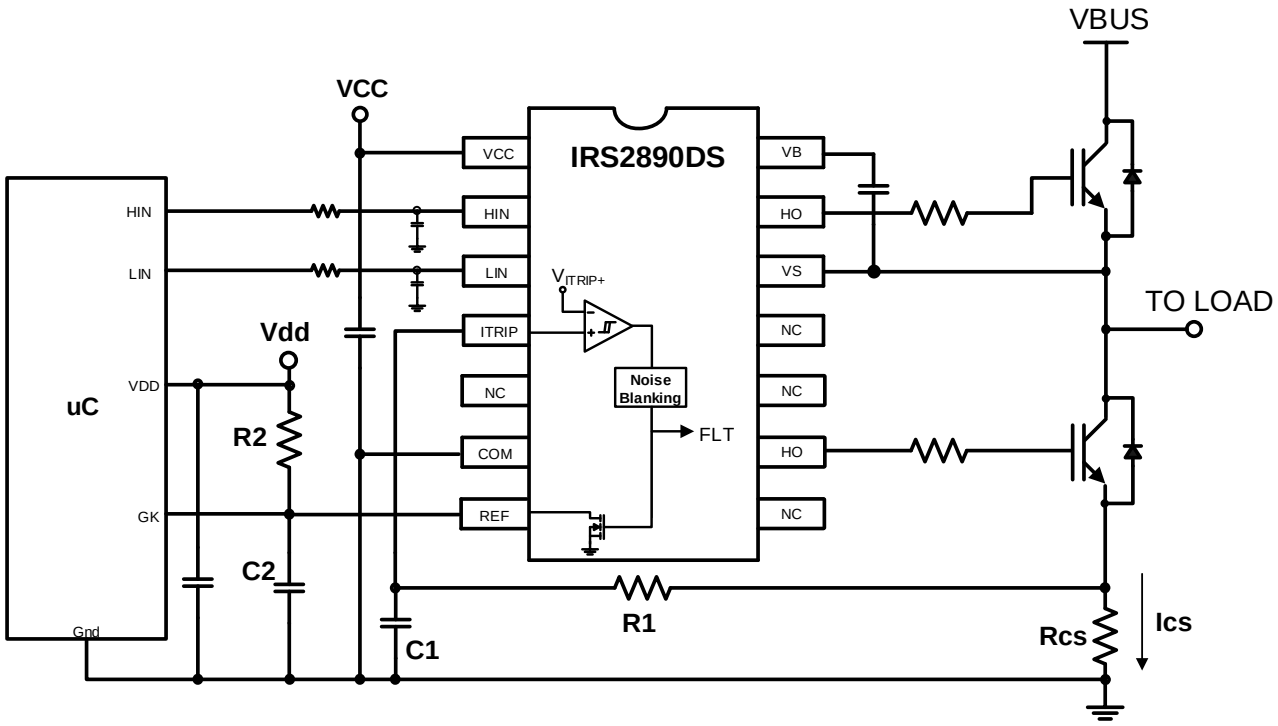


Figure 5 Application circuit example of half bridge with shunt resistor for OCP

Note:

1. *The input signals are active-high configured. There is an internal pull-down resistor from each input signal line to COM. When employing RC coupling circuits between microcontroller and IRS2890DS, the RC values should be properly selected so that the input signals are compatible with the IRS2890DS logic "1"/logic "0" input voltages.*
2. *To avoid malfunction, the wiring of each input should be as short as possible (less than 2-3 cm).*
3. *The inputs of IRS2890DS can be directly connected with microcontroller terminals without any opto-coupler or transformer isolation.*
4. *RFE output is an open-drain output. This signal line should be pulled up to the positive side of the 5 V or 3.3 V logic power supply with a pull-up resistor. When placing RC to program fault-clear time, a close location to IRS2890DS is recommended.*
5. *To prevent protection function errors, the R_1 and C_1 wiring between ITRIP and power ground should be as short as possible. C_1 wiring should be placed as close to COM pin as possible.*
6. *The short-circuit protection time constant $\tau_{ITRIP} = R_1 * C_1$ can be programmable according to the customers' requirement.*
7. *Each capacitor should be mounted as close to the pins of the IRS2890DS as possible.*
8. *VCC of 15-16 V is recommended when the integrated bootstrap circuitry only is used.*
9. *It is recommended to connect the ground pin of the microcontroller directly to the COM pin.*

3.3 Recommended layout pattern for OCP & SCP function

It is recommended that the ITRIP filter capacitor connections to the IRS2890DS pins be as short as possible. The ITRIP filter capacitor should be connected to COM pin directly without overlapped ground pattern. Connected uC ground to IRS2890DS ground, then the signal ground and power ground at shunt resistor should be as short as possible and connected at only one point via the filter capacitor of VCC line. It is also recommended to keep the current-sense loop, which is shown in Figure 6, as small as possible for better noise immunity.

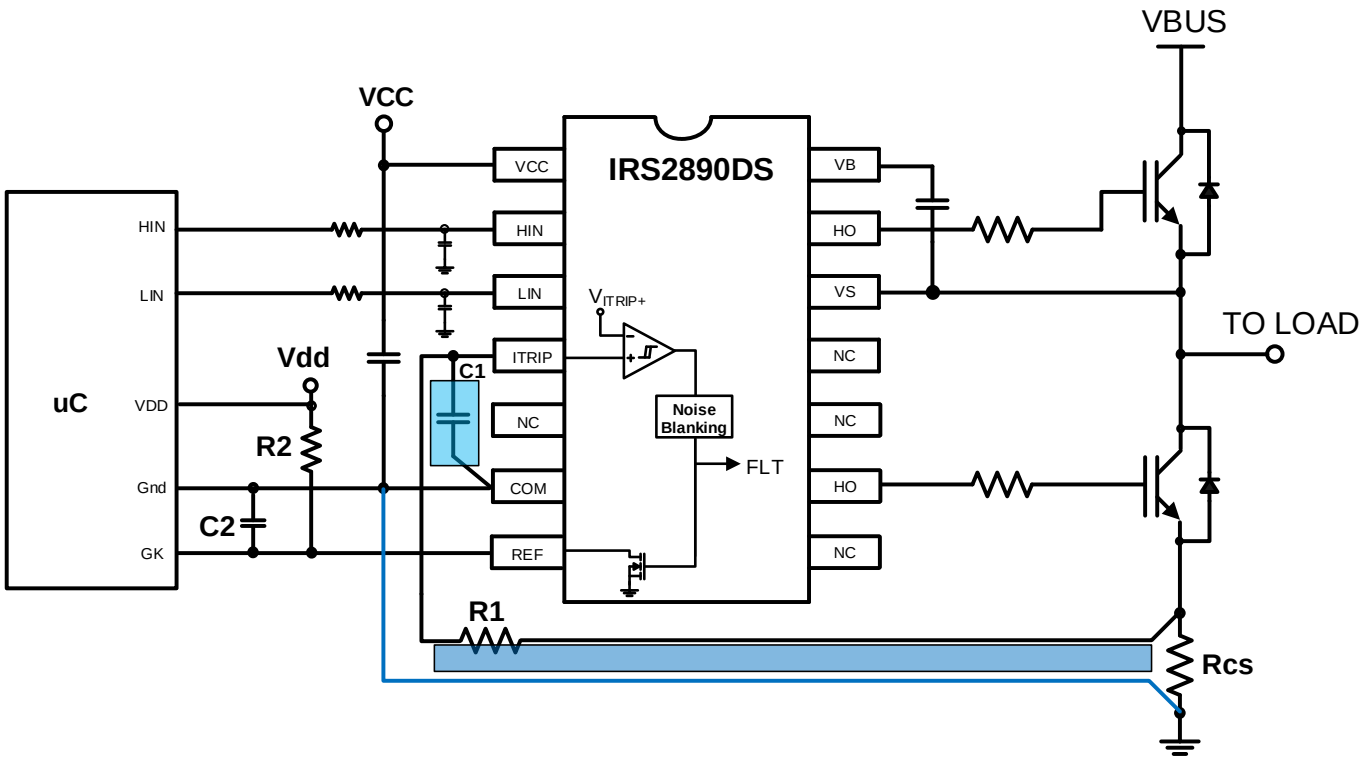


Figure 6 Recommended layout pattern for OCP & SCP function

3.4 Recommended wiring of shunt resistor and snubber capacitor

External current sensing resistors are applied to detect overcurrent. A long wiring pattern between the shunt resistors and low-side IGBT will cause excessive surges that might damage the IRS2890DS and current detection components. This may also distort the sensing signals. To decrease the parasitic inductance, the wiring between the shunt resistors and emitter of low-side IGBT should be as short as possible.

As shown in Figure 7 snubber capacitors should be installed in the right location so as to suppress surge voltages effectively. Generally a high frequency non-inductive capacitor of around 0.1-0.22 µF is recommended. If the snubber capacitor is installed in the wrong location ‘P3’ as shown in Figure 7, the snubber capacitor cannot suppress the surge voltage effectively. If the capacitor is installed in the location ‘P1’, the charging and discharging currents generated by wiring parasitic inductance and the snubber capacitor will appear on the shunt resistor. This will impact the current-sensing signal, and the SC protection level will be a little lower than the calculated design value. The ‘P1’ position surge-suppression effect is greater than the location ‘P2’ or ‘P3’. The ‘P2’ position is a reasonable compromise with better suppression than in location ‘P3’ without impacting the accuracy of the current sensing signal. For this reason, the location ‘P2’ is generally used.

Interface circuit and layout guide

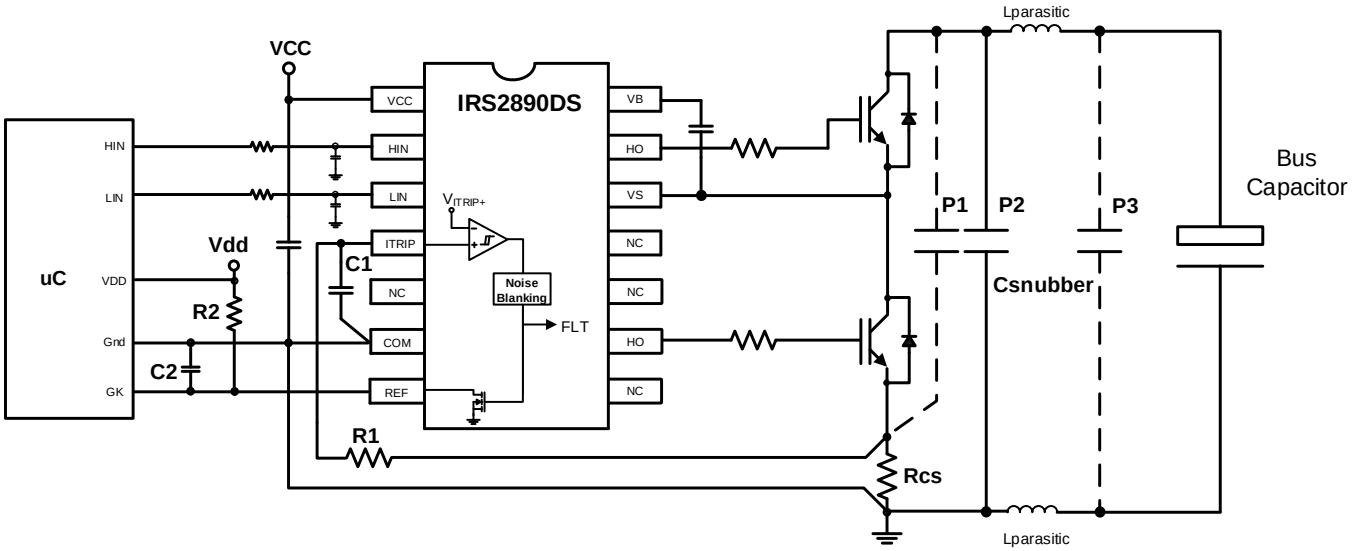


Figure 7 Recommended wiring of shunt resistor and snubber capacitor

4 Protection features

4.1 Undervoltage protection

This IC provides undervoltage lockout protection on both the VCC (logic and low-side circuitry) power supply and the VBS (high-side circuitry) power supply. Figure 8 is used to illustrate this concept; VCC (or VBS) is plotted over time, and as the waveform crosses the UVLO threshold ($V_{CCUV+/-}$ or $V_{BSUV+/-}$) the undervoltage protection is enabled or disabled.

Upon power-up, should the VCC voltage fail to reach the V_{CCUV+} threshold, the IC cannot turn on. Additionally, if the VCC voltage decreases below the V_{CCUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shut down the high- and low-side gate drive outputs, and the FAULT pin will transition to the low state to inform the controller of the fault condition.

Upon power-up, should the VBS voltage fail to reach the V_{BSUV+} threshold, the IC cannot turn on. Additionally, if the VBS voltage decreases below the V_{BSUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shut down the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power device could be driven with a low voltage, resulting in the power device conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

Control and gate drive power for the IRS2890DS is normally provided by a single 15 V supply that is connected to the VCC and COM terminals. The control supply should be well-filtered with a low impedance electrolytic capacitor and a high-frequency decoupling capacitor connected at the IRS2890DS's pins.

High-frequency noise on the supply might cause the internal control IC to malfunction and generate erroneous fault signals. To avoid these problems, the maximum ripple on the supply should be less than ±1 V. The potential at the IRS2890DS's COM terminal is different from the emitter of low-side IGBT terminal by the voltage drop across the sensing resistor. It is very important that all control circuits and power supplies be referred to this point and not to the low-side IGBT emitter terminal. If circuits are improperly connected, the additional current flowing through the sense resistor might cause improper operation of the short-circuit protection function. In general, it is best practice to make the common reference (COM) a ground plane in the PCB layout.

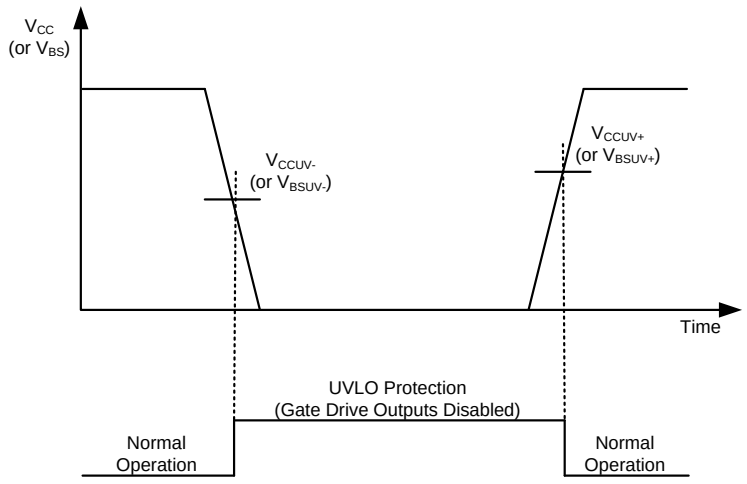


Figure 8 Timing chart of undervoltage protection function

4.2 Overcurrent protection

4.2.1 Timing chart of overcurrent (OC) protection

The IRS2890DS has an overcurrent shutdown function. Its internal comparator monitors the voltage of the ITRIP pin, and if this voltage exceeds the $V_{ITRIP+,}$ which is specified in the devices datasheets, a fault signal is activated and all channels are turned off. Typically the maximum short-circuit current magnitude is gate-voltage dependant. A higher gate voltage results in a larger short-circuit current. In order to avoid this potential problem, the maximum overcurrent trip level is generally set to below 2 times the nominal rated collector current. The overcurrent protection timing chart is shown in Figure 9.

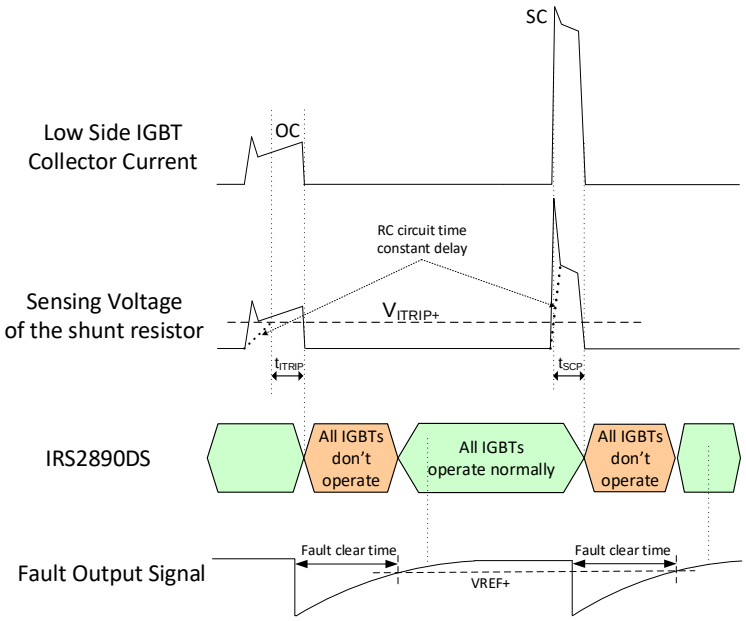


Figure 9 Timing chart of overcurrent protection function

4.2.2 Selecting current-sensing shunt resistor

The value of the current-sensing resistor is calculated by the following expression:

$$R_{SC} = \frac{V_{ITRIP+}}{I_{OC}} \qquad (1)$$

where V_{ITRIP+} is the ITRIP positive-going threshold voltage, it is typically 0.5 V. I_{OC} is the current of OC detection level.

The maximum value of OC protection level should be set lower than the repetitive peak collector current in the datasheet considering the tolerance of shunt resistor.

For example, if the overcurrent protection is 5 A, thus, the recommended value of the shunt resistor is calculated as

$$R_{SC(min)} = \frac{0.5}{5} = 0.1\ \Omega$$

For the power rating of the shunt resistor, the list below should be considered:

- Maximum load current of inverter (Irms)

Protection features

- Shunt resistor value at Tc=25 °C (R_{SC})
- Power derating ratio of shunt resistor at T_{SC}=100 °C according to the manufacturer's datasheet
- Safety margin

The shunt resistor power rating is calculated by the following equation:

$$P_{SC} = \frac{I_{rms}^2 \times R_{SC} \times \text{margin}}{\text{derating ratio}} \quad (2)$$

For example, in the case of R_{SC}=100 mΩ:

- Max. load current of the inverter : 1 A (rms)
- Power derating ratio of shunt resistor at T_{SC}=100 °C : 80%
- Safety margin : 50%

$$P_{SC} = \frac{1^2 \times 0.1 \times 1.5}{0.8} = 0.19\text{W}$$

A proper power rating of shunt resistor is over 0.19 W, e.g. 0.5 W.

Note that a proper resistance and power rating higher than the minimum value should be chosen considering the overcurrent protection level required in the application.

4.2.3 Blanking time

The internal ITRIP blanking time T_{BL}(typ.=500 ns) is necessary in the overcurrent-sensing circuit to prevent malfunction of OC protection caused by noise. If the blanking time is not enough to suppress the noise, an additional RC filter is necessary. The RC time constant is determined by considering the noise duration and the short-circuit withstand time capability of the IGBT.

When the sensing voltage on shunt resistor exceeds the ITRIP positive-going threshold (V_{ITRIP+}), this voltage is applied to the ITRIP pin of IRS2890DS via the RC filter. Table 5 shows the specification of the OC protection reference level. The filter delay time (T_{FILTER}) that the input voltage of ITRIP pin rises to the ITRIP positive threshold voltage is caused by RC filter time constant.

In addition there is a shutdown propagation delay of Itrip (T_{ITRIP}). Please refer to Table 6

Table 5 Specification of OC protection reference level' VITRIP+'

Item	Min.	Typ.	Max.	Unit
ITRIP positive-going threshold V_{ITRIP+}	0.475	0.500	0.525	V

Table 6 Specification ITRIP to output shutdown propagation delay

Item	Min.	Typ.	Max.	Unit
ITRIP to output shutdown propagation delay T_{ITRIP}	500	720	950	ns

Therefore the total time from ITRIP positive-going threshold (V_{ITRIP+}) to the shut-down of the IGBT becomes:

$$T_{TOTAL} = T_{FILTER} + T_{ITRIP} \quad (3)$$

Shut-down propagation delay is inversely proportional to the current range, therefore the T_{ITRIP} is reduced at higher current conditions. The total delay must be less than the short-circuit withstanding time (t_{SC}) of the IGBT

in the datasheet. If the t_{SC} =5 us, the RC time constant should be set in the range of 1-2 µs. Recommended values for the filter components are R=1.8 kΩ and C=1 nF.

4.3 Fault output circuit and fault-clear time setup

The IRS2890DS provides adjustable fault-clear timer. Once ITRIP pin recognizes a fault, the RFE pin is internally pulled to COM. The RFE output stays in the low state until the fault condition has been removed and the fault-clear timer expires; once the fault-clear timer expires, the voltage on the RFE pin will return to its external pull-up voltage.
The length of the fault-clear time period (T_{FLTCLR}) is determined by the exponential charging characteristics of the capacitor, where the time constant is set by R2 and C2. Figure 5 shows that R2 is connected between the external supply (Vdd) and the RFE pin, while C2 is placed between the RFE and COM pins. Figure 10 shows the timing diagram of T_{FLTCLR}. The length of the fault-clear time period can be determined by using the formula below:

$$T_{FLTCLR} = -R2 \times C2 \times \ln\left(1 - \frac{V_{REF+}}{V_{DD}}\right) \quad (4)$$

The sample of T_{FLTCLR} Setup:

R2=2 MΩ, C2=1 nF , V_{REF+} =1.9 V, Vdd=3.3 V

T_{FLTCLR} = 1.7 ms

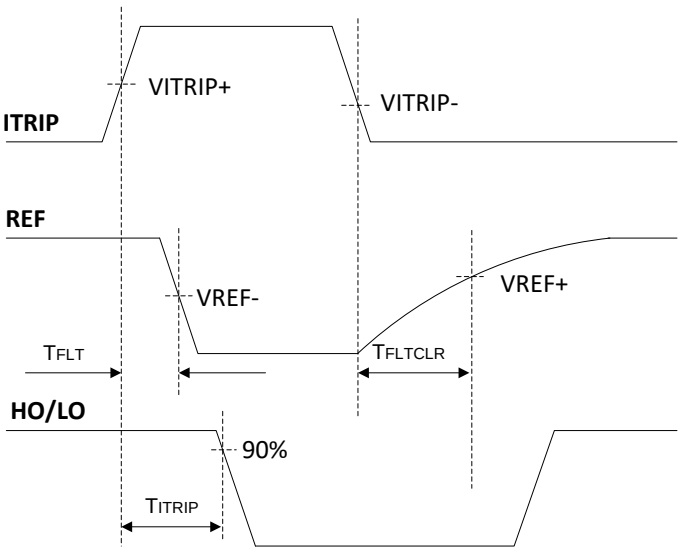


Figure 10 Timing diagram of ITRIP/REF/OUTPUT pins

Because the RFE terminal is an open-drain type, it must be pulled up to the high level via a pull-up resistor. The resistor has to be calculated according to the above specifications.

4.4 Enable input circuit

IRS2890DS provides an enable functionaltity that allows it to shutd own or enable the output. When the RFE pin is externally pulled up, the HVIC is able to operate normally (assuming no other fault condtions: undervoltage protection of VCC or overcurrent protection of ITRIP). When the RFE pin is pulled down externally, the gate

drive outputs are pulled low until the enable condtion is restored. The enable circuitry of the IRS2890DS features an input filter, the minimum input duration is specified by $t_{FLN,EN}$. Please refer to the RFE pin parameters V_{REF+}, V_{REF-} and I_{RFE} for the details of its use. Figure 11 shows the input, output and RFE pins timing diagram.

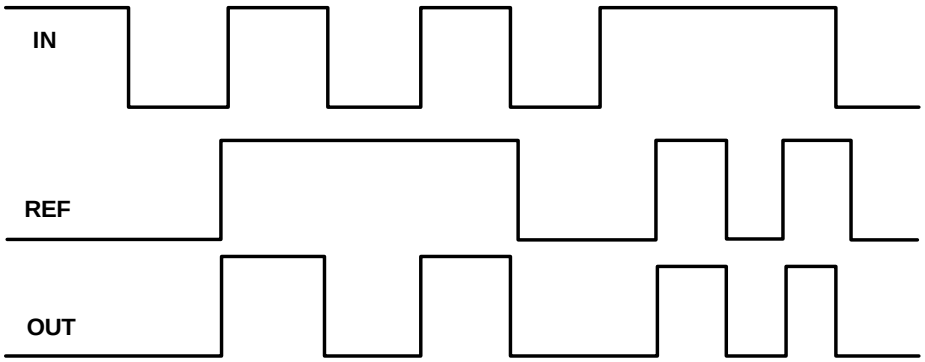


Figure 11 Input/output/enable pins timing diagram

5 Bootstrap circuit

5.1 Bootstrap circuit operation

The V_{BS} voltage, which is the voltage difference between VB and VS, provides the supply to the IC high-side section within the IRS2890DS. This supply voltage must be in the range of 10~20V to ensure that the IC can work properly. The IRS2890DS includes an undervoltage detection function for the V_{BS} to ensure that the IC does not drive the high-side device if the V_{BS} voltage drops below a specified voltage (refer to the datasheet). This function prevents the device from operating in a high dissipation mode. Please note here, that the undervoltage lockout function of the high-side section acts only on the high-side section without any feedback to the low-side section.

There are a number of ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described here. This method has the advantage of being simple and cheap. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. The IRS2890DS embeds an integrated bootstrap FET that allows an alternative drive of the bootstrap supply for a wide range of applications. The bootstrap FET is suitable for most PWM modulation schemes, including trapezoidal control, and can be used either in parallel with the external bootstrap network (diode+ resistor) or as a replacement of it. The use of the integrated bootstrap as a replacement of the external bootstrap network may have some limitations at very high PWM duty cycle due to bootstrap FET equivalent resistance (R_{BS}, see in datasheet).

The bootstrap supply is formed by a combination of the integrated bootstrap FET and external capacitor as shown in Figure 13. The current flow path of the bootstrap circuit is shown in Figure 13(a). When V_S is pulled down to ground (either through the low-side device or the load), the bootstrap capacitor (C_{BS}) is charged through the bootstrap FET and the resistor (R_{BS}) from the VCC supply.

5.2 Internal bootstrap functionality characteristics

The integrated bootstrap FET is turned on during the time when LO is ‘high’, and it has a limited source current due to RBS. The VBS voltage will be charged each cycle depending on the on-time of LO and the value of the CBS capacitor, the drain-source (collector-emitter) drop of the external IGBT (or MOSFET), and the low-side free-wheeling diode drop.

The bootstrap FET follows the state of low-side output stage (i.e., the bootstrap FET is ON when LO is high, unless the VB voltage is higher than approximately VCC. In that case, the bootstrap FET is designed to remain off until VB returns below that threshold; this concept is illustrated in Figure 12.

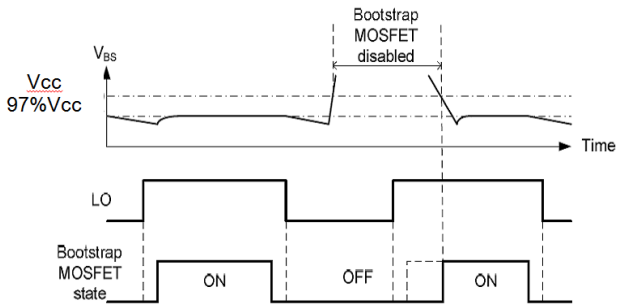


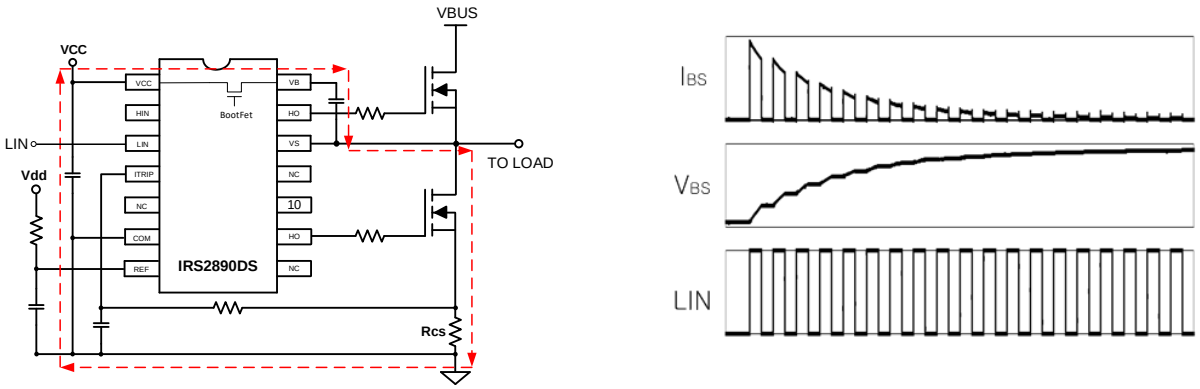
Figure 12 BootFET timing diagram

5.3 Initial charging of bootstrap capacitor

Adequate on-time duration of the low-side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated from the following equation:

$$t_{charge} \geq C_{BS} \times R_{BS} \times \frac{1}{\delta_L} \times \ln\left(\frac{V_{CC}}{V_{CC} - V_{GEmin} - V_{LS}}\right) \quad (5)$$

- R_{BS} = Bootstrap FET turn on Resistance
- V_{GEmin} = The minimum value of the bootstrap capacitor voltage, ($V_{GEmin} > V_{BSUV+}$)
- V_{LS} = Voltage drop across the low-side IGBT or Mosfet and shunt resistor
- δ_L = Duty cycle of low-side device



(a) Bootstrap circuit (b) Timing chart of initial bootstrap charging

Figure 13 Bootstrap circuit operation and initial changing

5.4 Bootstrap capacitor selection

To size the bootstrap capacitor, the first step is to establish the minimum votage drop ΔV_{BS} that we have to guarantee when the high-side IGBT or Mosfet is on. If V_{GEmin} is the minimum gate emitter voltage we want to maintain, the voltage drop must be:

$$\Delta V_{BS} \leq V_{CC} - V_{GEmin} - V_{LS} - I_C * R_{BS} \quad (6)$$

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{Q_{TOT}}{\Delta V_{BS}} \quad (7)$$

$$Q_{TOT} = Q_G + Q_{LS} + (I_{LK\_GE} + I_{LK}) \times (1 - \delta_L) \times \frac{1}{f} + (I_{QBS} + I_{LK\_CAP}) \times \frac{1}{f} \quad (8)$$

$$I_C = \frac{Q_{TOT} \times f}{\delta_L} \quad (9)$$

- Where,
- Q_{TOT} = Total needed charge
- C_{BS} = Bootstrap capacitor between VB and VS pins

Bootstrap circuit

- I_C = C_{BS} capacitor required charge current
- Q_G = Turn on required gate charge of IGBT or Mosfet
- Q_{LS} = Charge required by the internal level shifters
- I_{LK-GE} = Gate – source leakage current of IGBT or Mosfet
- I_{QBS} = Quiescent current of the high-side circuit in the IRS2890DS
- I_{LK} = Floating section leakage current
- I_{LK_CAP} = C_{BS} capacitor leakage current (ignored for non-electrolytic capacitors)
- f = Half bridge working frequency

By taking in consideration dispersion and reliability, the capacitance is generally selected to be 2~3 times higher than the calculated one. The C_{BS} is only charged when the high-side IGBT is off and the VS voltage is pulled down to ground. Therefore, the on-time of the low-side IGBT must be sufficient to ensure that the charge drawn from the C_{BS} capacitor can be fully replenished. Hence, inherently there is a minimum on-time of the low-side IGBT (or off-time of the high-side IGBT).

The bootstrap capacitor should always be placed as close to the pins of the IRS2890DS as possible. At least one low ESR capacitor should be used to provide good local de-coupling. For example, a separate ceramic capacitor close to the IRS2890DS is essential, if an electrolytic capacitor is used for the bootstrap capacitor. If the bootstrap capacitor is either a ceramic or tantalum type, it should be adequate for local decoupling.

5.5 Charging and discharging of the bootstrap capacitor during PWM-inverter operation

The bootstrap capacitor C_{BS} charges through the boot Fet according to Figure 13 from the VCC supply when the high-side IGBT is off, and the VS voltage is pulled down to ground. It discharges when the high-side IGBT or Mosfet are on.

Example:

The minimum value of the bootstrap capacitor

An example of the calculation of the minimum value of bootstrap capacitor C_{BS} is given with reference to equation (5) ~ (9).

Using a 10 A 600 V IGBT (IRGS4610D) for the example:

- Q_G = 13 nc (datasheet IRGS4610D)
- Q_{LS} = 3.8 nc
- I_{LK_GE} = 100 nA (datasheet IRGS4610D)
- I_{QBS} = 70 µA (datasheet IRS2890DS)
- I_{LK} = 50 µA (datasheet IRS2890DS)
- I_{LK_CAP} = 0 (Neglected for ceramic capacitor)
- f = 20 kHz
- δ_L = 50%

And the total charge is needed as:

Bootstrap circuit

$$Q_{TOT} = 13nc + 3.8nc + (100nA + 50\mu A) \times (1 - 50\%) \times \frac{1}{20kHz} + (70\mu A + 0) \times \frac{1}{20kHz} = 21.5nc$$

The C_{BS} capacitor required charge current is:

$$I_C = \frac{21.5nC \times 20kHz}{50\%} = 0.86mA$$

If

- V_{CC} = 15 V
- V_{LS} = 2 V
- V_{GEmin} = 12.5 V
- R_{BS} = 200 Ω

Then the voltage drop is:

$$\Delta V_{BS} \le 15V - 12.5V - 2V - 0.86mA * 200\Omega = 0.328V$$

$$C_{BS} \ge \frac{21.5nc}{0.328V} \ge 66nF$$

Then C_{BS} =220 nF ceramic capacitor is recommended.

Selection of the initial charging time

An example of the calculation of the minimum value for the initial charging time is given with reference to equation (5).

Working conditions:

- CBS = 220nF

$$t_{charge} \ge 220nF \times 200\Omega \times \frac{1}{0.5} \times \ln\left(\frac{15V}{15V - 12.5V - 2V}\right) \cong 0.3ms$$

In order to ensure safety, it is recommended that the charging time must be at least three times longer than the calculated value (eg: 1 ms).

Note that this result is only an example. It is recommended that the system design considers the actual control pattern and lifetime of the used components.

6 Thermal design

6.1 Introduction

The power loss is a key issue of IRS2890DS in high-frequency applications. In order to avoid overheating or to increase the reliability, we need to calculate the power loss and the junction temperature of IRS2890DS in the applications.

6.2 Power loss

The total losses (P_{TOT}) in the IRS2890DS result from a number of factors that can be grouped under low-voltage (static and dynamic) and high-voltage (static and dynamic) conditions.

$$P_{TOT} = P_{LSL} + P_{LDL} + P_{HSL} + P_{HDL} \quad (10)$$

Where

- Low-voltage static losses (P_{LSL})
- Low-voltage dynamic losses (P_{LDL})
- High-voltage static losses (P_{HSL})
- High-voltage dynamic losses (P_{HDL})
-

6.2.1 Low-voltage static losses

The low-voltage static losses from V_{CC} and V_{BS} are as the following:

$$\begin{aligned} P_{SVCC} &= V_{CC} \cdot I_{QCC} \\ P_{SVBS} &= V_{BS} \cdot I_{QBS} \\ P_{RBS} &= \delta \cdot R_{BS} \cdot I_C{}^2 \\ P_{IN} &= V_{IN} \cdot I_{IN} \\ P_{LSL} &= P_{SVCC} + P_{SVBS} + P_{RBS} + P_{IN} \end{aligned} \quad (11)$$

Where

- P_{SVCC} is the power loss for the quiescent current of V_{CC}
- P_{SVBS} is the power loss for the quiescent current of V_{BS}
- P_{RBS} is the conduction power loss for bootstrap Mosfet
- P_{IN} is the power loss for input (HIN/LIN) caused by INPUT current (I_{IN+})
- P_{LSL} is the total low voltage static losses from V_{CC} and V_{BS}
- I_{QCC} = Quiescent current of the low-side circuit in the IRS2890DS
- V_{IN} = Login high input voltage
- I_{IN+} = Login high input bias current

6.2.2 Low-voltage dynamic losses

The low-voltage dynamic losses are due to two different components.

1. One loss is caused by the gate drive output resistance when IRS2890DS drives IGBT or Mosfet. Wherever a capacitor equivqlent load is charged or discharged through a resistor, half of the energy that goes in

to charging the capacitance is dissipated in the resistor. The use of the external gate resistors reduces the amount of gate drive power that is dissipated inside the IRS2890DS by the ratio of the respective resistances.

The Power dissipation per gate driver is the following:

$$P_{GON} = 0.5 \cdot Q_G \cdot V_{CC} \cdot f \cdot \left(\frac{R_{GONIN}}{R_{GONIN} + R_{GONEX} + R_{GSW}}\right)$$
$$P_{GOFF} = 0.5 \cdot Q_G \cdot V_{CC} \cdot f \cdot \left(\frac{R_{GOFFIN}}{R_{GOFFIN} + R_{GOFFEX} + R_{GSW}}\right) \quad (12)$$

Where:

- P_{GON} = Power dissipation of IRS2890DS effective pull-up resistance when it turns on the IGBT
- P_{GOFF} = Power dissipation of IRS2890DS effective pull-down resistance when it turns off the IGBT
- R_{GONIN} = IRS2890DS output effective pull-up resistance (48Ω)
- R_{GOFFIN} = IRS2890DS output effective pull-down resistance (32Ω)
- R_{GONEX} = External turn-on gate resistor between IRS2890DS and IGBT
- R_{GOFFEX} = External turn-off gate resistor between IRS2890DS and IGBT
- R_{GSW} = Internal gate resistor of the IGBT

- So the total power dissipation of IRS2890DS gate drive output resistance is the following
- $P_G = 2 \cdot (P_{GON} + P_{GOFF})$ (13)
- The factor 2 in the formula is valid in the assumption that high-side and low-side are being driven, one per channel.
- The other low voltage dynamic losses associated with the switching of the internal CMOS circuitry can be approximated with the following formula:
- $P_{CMOS} = V_{CC} \cdot Q_{CMOS} \cdot f$ (14)
- where, Q_{CMOS} (7nc) is the internal CMOS essential charge for IRS2890DS at VCC.
- The total low voltage dynamic losses P_{LDL} are the following:
- $P_{LDL} = P_G + P_{CMOS}$ (15)

6.2.3 High-voltage static losses

High-voltage static losses are due to the leakage currents in the level shifting stage. They are dependent on the voltage applied to the VS pin and they are proportional to the high-side device duty cycle. But they only occur when the high-side power device is on. The losses would be zero if VS is grounded.

Therefore, depending on the high-side device duty cycle δ_H, the high-voltage static loss is the following equation (16).

$$P_{HSL} = \delta_H \cdot V_{BUS} \cdot I_{LK} \quad (16)$$

Where,

- V_{BUS} is DC link voltage
- I_{LK} is the offset leakage current of IRS2890DS at VS=V_{BUS}

6.2.4 High-voltage dynamic losses

- High-voltage dynamic losses comprise two terms, one due to the level shifting circuit and the other one due to the charging and dischargeing of the capacitance of the high-side p-well $C_{b\text{-}sub}$ within the IRS2890DS.

The IRS2890DS internal level shifting circuit loss is relative with the level shift Mosfets charge - Q_{LF} (which transfer the set and reset signal from low-side section to high-side section), the voltage of VS pin at the moment of the set and reset happening and the working frequency. In the worst case, the set and reset happen at the VS=V_{BUS} in the inductive road applications. In these applications, whenever the high-side flip-flop is set or reset, a command to turn on or turn off the high-side device causes a current to flow through the internal level-shifting circuit. This charge comes from the high voltage bus (V_{BUS}).

Thus, for a half bridge operating from a DC bus voltage (V_{BUS}), the power dissipation of internal level shifting circuit is:

$$P_{HDL} = (V_{BUS} + V_{BS}) \cdot Q_{LS} \cdot f \qquad (17)$$

Where, Q_{LS} is decided by the turn-on pulse current and turn-on pulse width for the internal level shift high voltage Mosfets.

In a high-side and low-side power circuit the well capacitance $C_{b\text{-}sub}$ is charged and discharged every time VS swings between V_{BUS} and COM.Charging current is supplied by the high voltage rail through the power device and IRS2890DS epi resistance. Discharge occurs through the low-side device and epi resistance. The losses incurred in charging or discharging a capacitor through a resistor is equal to QV/2, regardless of the value of resistance. However, much of these losses occur outside the IRS2890DS, since the epi resistance is negligible compared to the internal reistance of power devices during their switching transitions.

- So the high voltage dymanic loss is dominated by the internal level shifting circuit loss.

6.3 Junction temperature considerations and calculation example

The junction temperature (T_J) of IRS2890DS is decided by the ambient temperature (T_A), power loss (P_{TOT}) and junction to ambient thermal resistance Rth_{JA}. Here is the formula:

$$T_J = T_A + P_{TOT} \cdot Rth_{JA} \qquad (18)$$

6.3.1 IRS2890DS losses example

Here is an example of the calculation for the power loss and junction temperature for IRS2890DS with reference to equation (10) ~ (18).

Example of the application:

- Topology: Half bridge with inductive load
- Working frequency: f=20 kHz with 50% duty cycle, (δ_L= δ_H =50%)
- DC Bus Voltage : V_{BUS}=310 V
- V_{CC} and V_{BS} supply voltage: V_{CC}=15 V, V_{BS}=14 V with bootstrap power supply from V_{CC}
- Half bridge power device: IRGS4610D
- Gate resistor beween IRS2890DS and Power device: R_{GONEX} = R_{GOFFEX} = 33 Ω
- I_{VCC} = 3000 µA (datasheet IRS2890DS)

Thermal design

- I_C = 860 µA (C_{BS} charge current , see page 20)
- V_{IN} = 4 V, I_{IN} = 10 µA (datasheet IRS2890DS)

The total low-voltage static losses P_{LSL} from V_{CC} and V_{BS} are as the following:

$$P_{SVCC} = 15V \cdot 3mA = 45mW$$
$$P_{SVBS} = 14V \cdot 70\mu A = 980\mu W$$
$$P_{RBS} = 0.5 \cdot 200\Omega \cdot (0.86mA)^2 = 74\mu W$$
$$P_{IN} = 4V \cdot 10\mu A = 40\mu W$$
$$P_{LSL} = 45mW + 980\mu W + 74\mu W + 40\mu W = 46mW$$

- The total low voltage dynamic losses P_{LDL} are the following:

$$P_{GON} = 0.5 \cdot 13nc \cdot 15V \cdot 20kHz \cdot (\frac{48\Omega}{48\Omega + 33\Omega + 0\Omega}) = 1.156mW$$
$$P_{GOFF} = 0.5 \cdot 13nc \cdot 15V \cdot 20kHz \cdot (\frac{32\Omega}{32\Omega + 33\Omega + 0\Omega}) = 0.96mW$$
$$P_G = 2 \cdot (P_{GON} + P_{GOFF}) = 2 \cdot (1.156mW + 0.96mW) = 4.231mW$$
$$P_{CMOS} = V_{CC} \cdot Q_{CMOS} \cdot f = 15V \cdot 7nc \cdot 20kHz = 2.1mW$$
$$P_{LDL} = P_G + P_{CMOS} = 4.231mW + 2.1mW = 6.331mW$$

The high voltage static loss is the following:

$$P_{HSL} = 50\% \cdot 310V \cdot 50\mu A = 7.75mW$$

The high voltage dymanic loss is dominated by the internal level shifting circuit which shows the following:

$$P_{HDL} = (310V + 14V) \cdot 3.8nc \cdot 20kHz = 24.62mW$$

The total loss (P_{TOT}) in the IRS2890DS is as the following:

$$P_{TOT} = 46mW + 6.331mW + 7.75mW + 24.62mW = 84.7mW$$

6.3.2 IRS2890DS thermal resistance

The thermal resistance (Rth_{JA}) from junction to ambient of IRS2890DS is 120 °C/W for the 14-Lead SOIC package.

6.3.3 IRS2890DS junction Temperature

If the ambient temperature (T_A) is 50°C, the junction temperature of IRS2890DS is the following:

$$T_J = 50°C + 84.7mW \cdot 120°C/W = 60.1°C$$

The junction temperature (60 °C) in the applications is far below the maximum junction temperature in the datasheet (150 °C). So the IRS2890DS is safe in the application for the thermal design.

Here, Figure 14 and Figure 15 are for design engineer's reference.

Figure 14, listing the curve for IRS2890DS power loss with different working frequency and gate resistor. Figure 15, listing the curve for IRS2890DS junction temperature with different working frequency and gate resistor.

6.3.4 IRS2890DS power loss vs frequency with different gate resistor

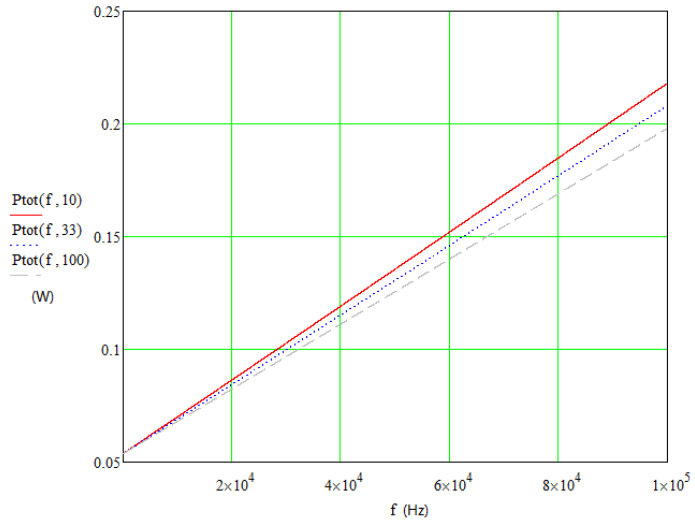


Figure 14 Power loss with Rg=10 Ω/33 Ω/100 Ω VS frequency

6.3.5 IRS2890DS junction temperature vs frequency with different gate resistor

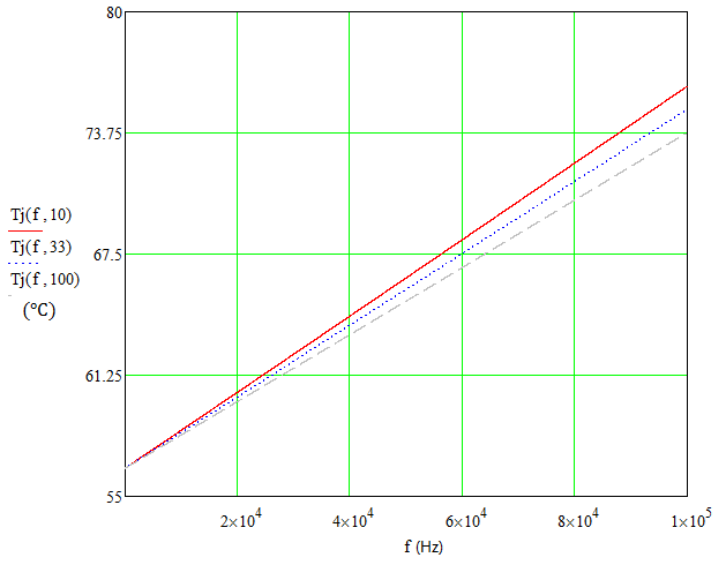


Figure 15 Junction temperature with Rg=10 Ω/33 Ω/100 Ω vs frequency at T_A =50 °C

7 References

1. [1] Datasheet of IRS2890DS, Rev 1.0, https://www.infineon.com/dgdl/Infineon-IRS2890DS-DS-v01_00-EN.pdf?fileId=5546d4625a888733015aad6fbc8a4bf4, 2017-03-02
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References

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