

# Application Note AN-1085<sub>revC</sub>

## IRS2153(1)D and IR2153(1)/IR2153(1)D Comparison

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### 1. INTRODUCTION

The new IRS2153(1)D replaces the existing IR2153(1)/IR2153(1)D HVICs advantageously by saving the need for an external bootstrap diode. It is based on the same core design and is pin-to-pin compatible, allowing minimum changes to the previous design. This application note describes the differences between the existing IR2153(1)/IR2153(1)D IC family and the new IRS2153(1)D.

### 2. BLOCK DIAGRAMS

The IR2153(1)/IR2153(1)D is not a single IC, but consists of a family of ICs (Table I).

P/N	Deadtime (typ.)	Internal Bootstrap Diode	Package Type
IR2153PbF	1.2 $\mu$ s	No	DIP8
IR2153SPbF	1.2 $\mu$ s	No	SO8
IR21531PbF	0.6 $\mu$ s	No	DIP8
IR21531SPbF	0.6 $\mu$ s	No	SO8
IR2153DPbF	1.2 $\mu$ s	Yes	DIP8
IR2153DSPbF	1.2 $\mu$ s	Yes	SO8
IR21531DPbF	0.6 $\mu$ s	Yes	DIP8
IR21531DSPbF	0.6 $\mu$ s	Yes	SO8

The functional block diagrams of each IC (Figs. 1 and 2) are exactly the same except the internal bootstrap diode.

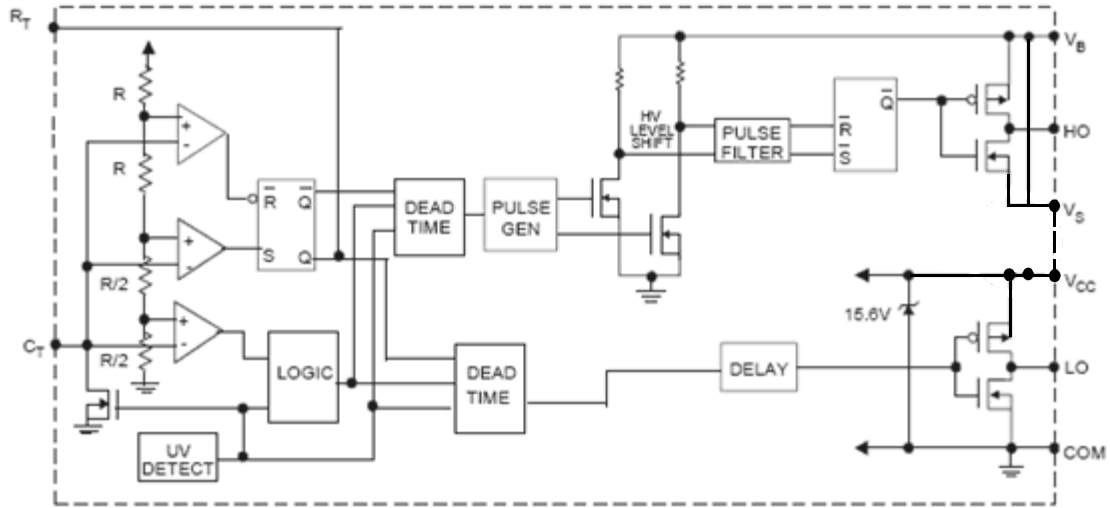
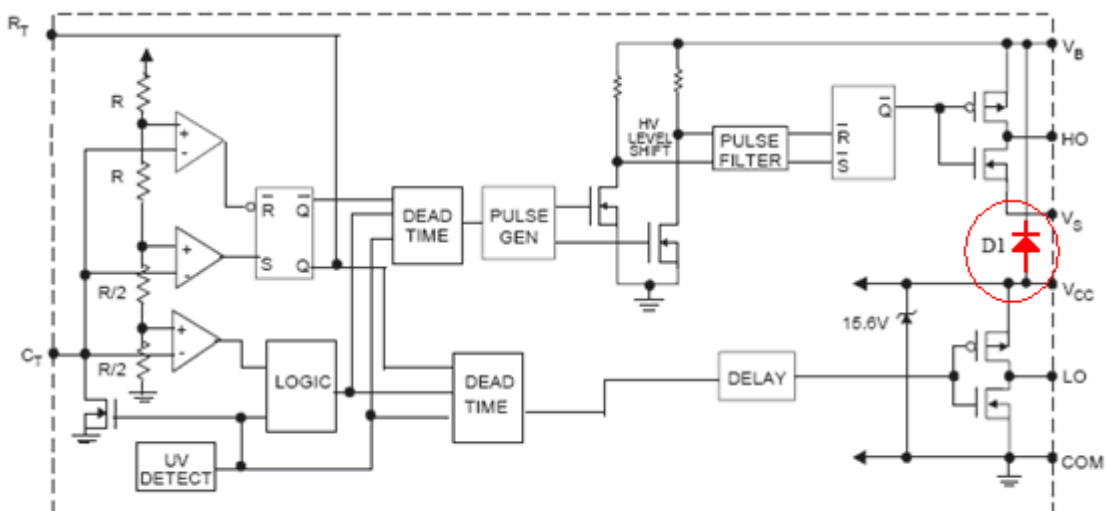


Figure 1: IR2153(1) Functional Block Diagram



NOTE: The D1 is a separate die.

Figure 2: IR2153(1)D Functional Block Diagram

In the new IRS2153(1)D IC (Fig. 3), an internal FET now replaces the internal bootstrap diode, which was previously a separate die. IRS2153(1)D has the same functionality as IR2153(1)D and the need for an additional diode has been eliminated.

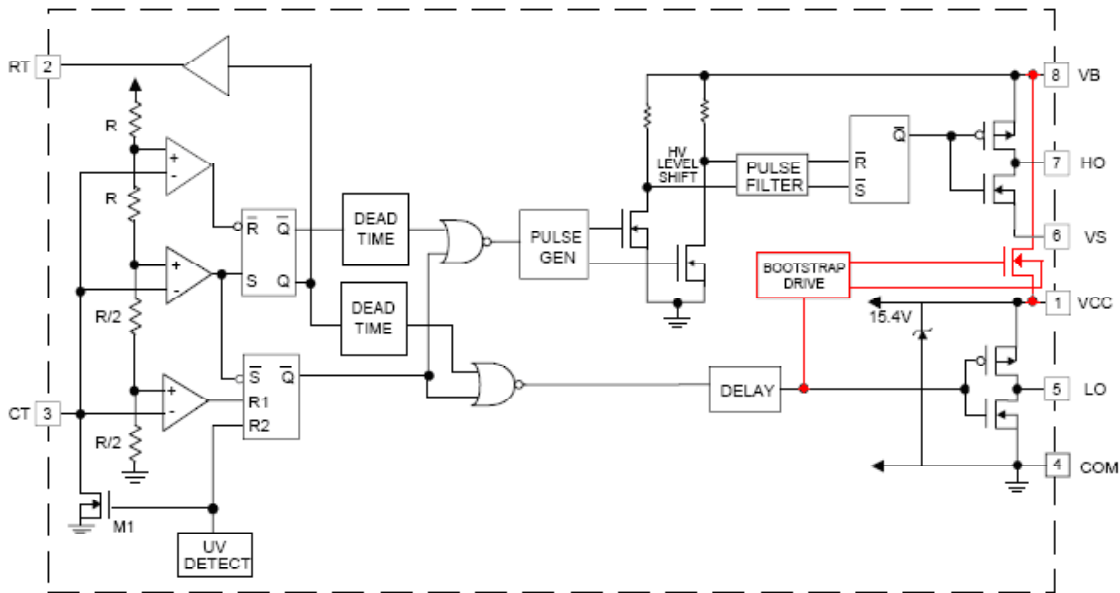


Figure 3: IRS2153(1)D Functional Block Diagram

**Consequently:** a customer using IR2153(1)/IR2153(1)D should take particular care of the bootstrap circuitry when switching to IRS2153(1)D.

### 3. IR2153(1)/IR2153(1)D vs. IRS2153(1)D ELECTRICAL CHARACTERISTICS DIFFERENCES

The following tables and comments highlight the differences between the IR2153(1)/IR2153(1)D and the new IRS2153(1)D:

#### Absolute Maximum Ratings

Parameter		IR2153(1)/IR2153(1)D		IRS2153(1)D		Units
Symbol	Definition	min	max	min	max	
V <sub>B</sub>	High side floating supply voltage	-0.3	625	-0.3	625	V
V <sub>S</sub>	High side floating supply offset voltage	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3	
V <sub>HO</sub>	High side floating output voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3	
V <sub>LO</sub>	Low side output voltage	-0.3	V <sub>CC</sub> + 0.3	-0.3	V <sub>CC</sub> + 0.3	
I <sub>RT</sub>	RT pin current	-5	5	-5	5	mA
V <sub>RT</sub>	RT pin voltage	-0.3	V <sub>CC</sub> + 0.3	-0.3	V <sub>CC</sub> + 0.3	V
V <sub>CT</sub>	CT pin voltage	-0.3	V <sub>CC</sub> + 0.3	-0.3	V <sub>CC</sub> + 0.3	
I <sub>CC</sub>	Supply current (Note 1)	---	25	---	20	mA
I <sub>O</sub> MAX	Maximum allowable current at LO and HO due to external power transistor Miller effect			-500	500	
dV <sub>S</sub> /dt	Allowable offset voltage slew rate	-50	50	-50	50	V/ns
P <sub>D</sub>	Max. power dissipation @ T <sub>A</sub> ≤ +25 °C, 8-Pin DIP	---	1.0	---	1.0	W
P <sub>D</sub>	Max. power dissipation @ T <sub>A</sub> ≤ +25 °C, 8-Pin SOIC	---	0.625	---	0.625	
R <sub>thJA</sub>	Thermal resistance, junction to ambient, 8-Pin DIP	---	125	---	85	°C/W
R <sub>thJA</sub>	Thermal resistance, junction to ambient, 8-Pin SOIC	---	200	---	128	
T <sub>J</sub>	Junction temperature	-55	150	-55	150	°C
T <sub>S</sub>	Storage temperature	-55	150	-55	150	
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	---	300	---	300	

**Comments:** All absolute maximum ratings are exactly the same except for the maximum supply current limit and the thermal resistance. The maximum supply current is rated at 20 mA for the new IRS2153(1)D versus 25 mA for the IR2153(1)/IR2153(1)D and is due to the internal zener clamp. A 20 mA maximum versus 25 mA should be a negligible amount for most applications. A lower thermal resistance will give lower temperatures on the package surface.

#### Recommended Operating Conditions

Parameter		IR2153(1)/IR2153(1)D		IRS2153(1)D		Units
Symbol	Definition	min	max	min	max	
V <sub>BS</sub>	High side floating supply voltage	V <sub>CC</sub> - 0.7	V <sub>CLAMP</sub>	V <sub>CC</sub> - 0.7	V <sub>CLAMP</sub>	V
V <sub>S</sub>	Steady state high side floating supply offset voltage	-3.0	600	-3.0	600	
V <sub>CC</sub>	Supply voltage	10	V <sub>CLAMP</sub>	V <sub>CCUV</sub> + 0.1V	V <sub>CLAMP</sub>	
I <sub>CC</sub>	Supply current		5		5	mA
T <sub>J</sub>	Junction temperature	-40	125	-40	125	°C

**Comments:** All parameters are mostly the same.

### Recommended Component Values

Parameter		IR2153(1)/IR2153(1)D		IRS2153(1)D		Units
Symbol	Definition	min	max	min	max	
R <sub>T</sub>	Timing resistor value	1	---	1	---	kΩ
C <sub>T</sub>	C <sub>T</sub> pin capacitor value	330	---	330	---	pF

**Comments:** All parameters are exactly the same.

### Electrical Characteristics

Bootstrap FET/Diode Characteristics		IR2153(1)/IR2153(1)D			IRS2153(1)D			Units	Test Conditions
Symbol	Definition	Min	Typ	Max	Min	Typ	Max		
V <sub>F</sub>	Bootstrap diode forward voltage (IR2153(1)D)	0.5	---	1.0				V	I <sub>F</sub> = 250 mA
VB_ON	VB when the bootstrap FET is on				---	13.7	---		
IB_CAP	VB source current when bootstrap FET is on				40	55	---	mA	CBS=0.1 μF
IB_10V	VB source current when bootstrap FET is on				10	12			VB=10 V

**Comments:** The IRS2153(1)D contains an integrated bootstrap MOSFET that eliminates the need for an external high-voltage bootstrap diode. The integrated bootstrap MOSFET is turned on only during the time when LO is 'high', and has a limited source current due to R<sub>DS(on)</sub>. The V<sub>BS</sub> voltage will be determined each cycle by the on-time of LO, the size of the external MOSFETs and the value of the CBS capacitor. At start-up, several cycles of LO will occur first until V<sub>BS</sub> increases above V<sub>BSUV+</sub> (see Floating Supply Characteristics) and then HO will start to oscillate. The maximum operating frequency will be determined by the MOSFET driven by IRS2153(1)D and the value of the CBS capacitor since the bootstrap MOSFET needs to maintain V<sub>BS</sub> above V<sub>BSUV-</sub> each cycle. If the frequency is too high, V<sub>BS</sub> will fall below V<sub>BSUV-</sub> and the HO output will turn off. To avoid this problem, an external high-voltage bootstrap diode can be added in parallel to maintain V<sub>BS</sub> above V<sub>BSUV-</sub> during high-frequency applications.

Low Voltage Supply Characteristics		IR2153(1)/IR2153(1)D			IRS2153(1)D			Units	Test Conditions
Symbol	Definition	Min	Typ	Max	Min	Typ	Max		
V <sub>CCUV+</sub>	Rising V <sub>CC</sub> undervoltage lockout threshold	8.1	9.0	8.1	10.0	11.0	12.0	V	
V <sub>CCUV-</sub>	Falling V <sub>CC</sub> undervoltage lockout threshold	7.2	8.0	7.2	8.0	9.0	10.0		
V <sub>CCUVHYS</sub>	V <sub>CC</sub> undervoltage lockout hysteresis	0.5	1.0	0.5	1.6	2.0	2.4		
I <sub>CCUV</sub>	Micropower startup V <sub>CC</sub> supply current	---	75	150	---	130	170	μA	V <sub>CC</sub> ≤ V <sub>CCUV-</sub>
I <sub>CC</sub>	Quiescent V <sub>CC</sub> supply current	---	500	950	---	800	1000		
I <sub>CC</sub>	V <sub>CC</sub> supply current				---	1.8	---	mA	R <sub>T</sub> =36.9 kΩ
V <sub>CLAMP</sub>	V <sub>CC</sub> zener clamp voltage	14.4	15.6	16.8	14.4	15.4	16.8	V	I <sub>CC</sub> = 5 mA

**Comments:** No major changes other than V<sub>CCUV+</sub> and V<sub>CCUV-</sub> being higher, as well as the hysteresis. The higher UVLO thresholds should not impact the application since typically V<sub>CC</sub> is regulated against its internal 15.4 V clamp voltage. The increased hysteresis should make the application more robust and prevent the IC from turning off momentarily should transient dips in the V<sub>CC</sub> voltage occur.

Floating Supply Characteristics		IR2153(1)/IR2153(1)D			IRS2153(1)D			Units	Test Conditions
Symbol	Definition	Min	Typ	Max	Min	Typ	Max		
$I_{QBS}$	Quiescent $V_{BS}$ supply current	---	30	50	---	60	80	$\mu A$	
$V_{BSUV+}$	$V_{BS}$ supply undervoltage positive going threshold				8.0	9.0	9.5	V	
$V_{BSUV-}$	$V_{BS}$ supply undervoltage negative going threshold				7.0	8.0	9.0	V	
$I_{QBSUV-}$	Micropower startup $V_{BS}$ supply current	---	0	10				$\mu A$	$V_{CC} \leq V_{CCUV-}$ , $V_{CC} = V_{BS}$
$V_{BSMIN}$	Minimum required $V_{BS}$ voltage for proper functionality from $R_T$ to $H_O$	---	4.0	5.0				V	$V_{CC} = V_{CCUV-} + 0.1 V$
$I_{LK}$	Offset supply leakage current	---	---	50	---	---	50	$\mu A$	$V_B = V_S = 600 V$

**Comments:** The new IRS2153(1)D contains an under-voltage lockout circuit. This is necessary because of the additional integrated bootstrap MOSFET. The UVLO circuit will guarantee that  $V_{BS}$  is high enough before turning on  $H_O$  and will protect the external MOSFET from being driven in the linear region should  $V_{BS}$  decrease too much.

Oscillator I/O Characteristics		IR2153(1)/IR2153(1)D			IRS2153(1)D			Units	Test Conditions
Symbol	Definition	Min	Typ	Max	Min	Typ	Max		
$f_{osc}$	Oscillator frequency	19.4	20	20.6	18.4	19.0	19.6	kHz	$R_T = 36.9/36.5 k\Omega$
		94	100	106	88	93	100		$R_T = 7.43/7.15 k\Omega$
$d$	$R_T$ pin duty cycle	48	50	52	---	50	---	%	$f_o < 100 kHz$
$I_{CT}$	$C_T$ pin current	---	0.001	1.0	---	0.02	1.0	$\mu A$	
$I_{CTUV}$	UV-mode $C_T$ pin pulldown current	0.30	0.70	1.2	0.2	0.3	0.6	mA	$V_{CC} = 7 V$
$V_{CT+}$	Upper $C_T$ ramp voltage threshold	---	8.0	---	---	9.32	---	V	
$V_{CT-}$	Lower $C_T$ ramp voltage threshold	---	4.0	---	---	4.66	---		
$V_{CTSD}$	$C_T$ voltage shutdown threshold	1.8	2.1	2.4	2.2	2.3	2.4		
$V_{RT+}$	High-level $R_T$ output voltage, $V_{CC} - V_{RT}$	---	10	50	---	10	50	mV	$I_{RT} = -100 \mu A$
		---	100	300	---	100	300		$I_{RT} = -1 mA$
$V_{RT-}$	Low-level $R_T$ output voltage	---	10	50	---	10	50		$I_{RT} = 100 \mu A$
		---	100	300	---	100	300		$I_{RT} = 1 mA$
$V_{RTUV}$	UV-mode $R_T$ output voltage	---	0	100	---	0	100		$V_{CC} \leq V_{CCUV-}$
$V_{RTSD}$	SD-mode $R_T$ output voltage, $V_{CC} - V_{RT}$	---	10	50	---	10	50		$I_{RT} = -100 \mu A$ , $V_{CT} = 0 V$
		---	100	300	---	100	300		$I_{RT} = -1 mA$ , $V_{CT} = 0 V$

**Comments:** The new IRS2153(1)D should fit into an existing design and maintain existing performance without any changes to the design with the exception of  $R_T/C_T$  value.

Gate Driver Output Characteristics		IR2153(1)/IR2153(1)D			IRS2153(1)D			Units	Test Conditions	
Symbol	Definition	Min	Typ	Max	Min	Typ	Max			
$V_{OH}$	High level output voltage	---	0	100	---	VCC	---	mV	$I_o = 0\text{ A}$	
$V_{OL}$	Low level output voltage, $V_o$	---	0	100	---	COM	---		$I_o = 0\text{ A}$	
$V_{OL\_UV}$	UV-mode output voltage, $V_o$	---	0	100	---	COM	---		$I_o = 0\text{ A}$ , $V_{CC} \leq V_{CCUV}$	
$t_r$	Output rise time	---	80	150	---	120	220	ns		
$t_f$	Output fall time	---	45	100	---	50	80			
$t_{sd}$	Shutdown propagation delay	---	660	---	---	350	---			
$t_d$	Output deadtime ( $H_o$ or $L_o$ )	2153D	0.75	1.20	1.65	0.65	1.10	1.75		$\mu\text{s}$
		21531D	0.35	0.6	0.85	0.35	0.6	0.85		
$I_{O+}$	Output source current				---	180	---	mA		
$I_{O-}$	Output sink current				---	260	---			

**Comments:** Output rise and fall times are slightly longer due to a slight decrease in the output source and sink currents. Deadtime tolerances had to be slightly downgraded, but should not impact most applications.

### 3. Conclusions

In most cases, any member for the IR2153(1)/IR2153(1)D family will be easily and advantageously replaced by the new leadfree IRS2153(1)D. The application will benefit a monolithic solution integrating a bootstrap FET, an increased UVLO hysteresis, a possibility of non-latch IC shutdown, better thermal behavior and ROHS compatibility while keeping a 3% tolerance on the frequency.