Target Applications

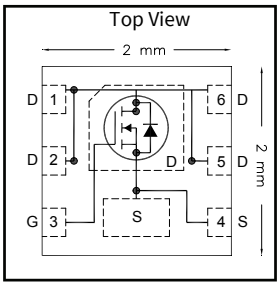
- Wireless charging
- Adapter
- Telecom

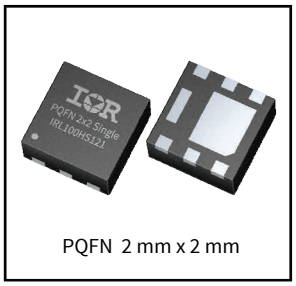
Benefits

- Higher power density designs
- Higher switching frequency
- Uses OptiMOS™5 Chip
- Reduced parts count wherever 5V supplies are available
- Driven directly from microcontrollers (slow switching)
- System cost reductions

Typical values (unless otherwise specified)

V_{DSS}	V_{GS}	$R_{DS(on)}$ (max.)
100V min.	± 20V max	42mΩ @ 10V
$Q_{g\ tot}$	Q_{gd}	$V_{gs(th)}$
3.7nC	1.6nC	1.7V





RoHS

G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRL100HS121	PQFN 2mm x 2mm	Tape and Reel	4000	IRL100HS121

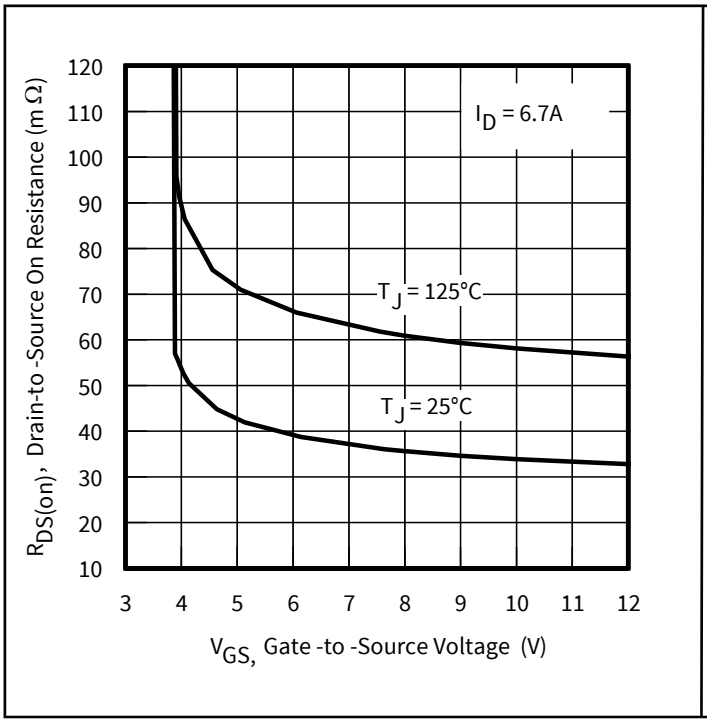


Figure 1 Typical On-Resistance vs. Gate Voltage

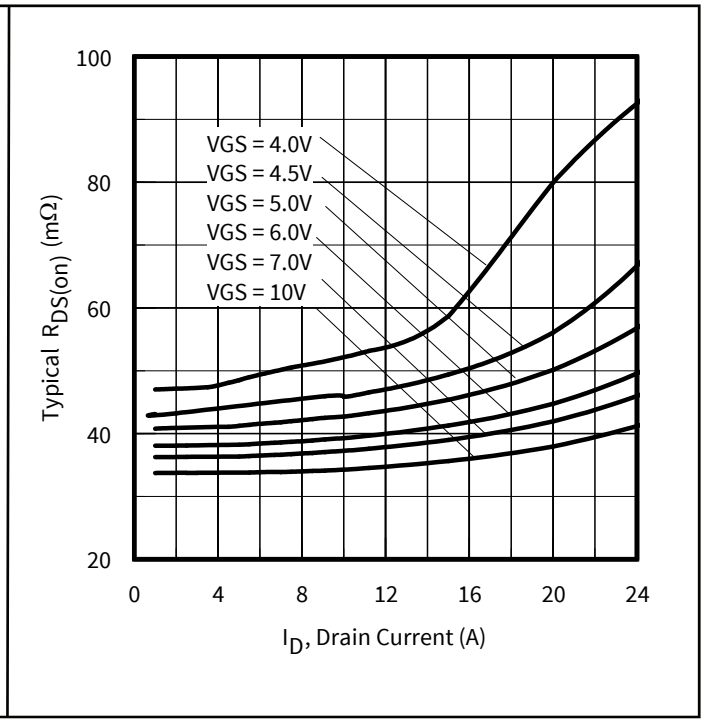


Figure 2 Typical On-Resistance vs. Drain Current

Table of Contents

1 Parameters

Table1 Key performance parameters

Parameter	Values	Units
V_{DS}	100	V
$R_{DS(on)\ max}$	42	mΩ
I_D @ T_C = 25°C	11	A
I_D @ T_A = 25°C	5.1	A

2 Maximum ratings and thermal characteristics

Table 2 Maximum ratings (at T_J = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Values	Unit
Continuous Drain Current (Silicon Limited) ⑥⑦	I_D	$T_{C\ (Bottom)}$ = 25°C, V_{GS} @ 10V	11	A
Continuous Drain Current (Silicon Limited) ⑥	I_D	$T_{C\ (Bottom)}$ = 100°C, V_{GS} @ 10V	7.8	
Continuous Drain Current (Silicon Limited) ⑦ (Source Bonding Technologies Limited)	I_D	$T_{C\ (Bottom)}$ = 25°C, V_{GS} @ 10V	10.2	
Continuous Drain Current (Silicon Limited) ⑤	I_D	T_A= 25°C, V_{GS} @ 10V	5.1	
Pulsed Drain Current ①	I_{DM}	$T_{C\ (Bottom)}$ = 25°C	41	
Maximum Power Dissipation	P_D	$T_{C\ (Bottom)}$ = 25°C	11.5	W
Maximum Power Dissipation	P_D	$T_{C\ (Bottom)}$ = 100°C	5.8	
Maximum Power Dissipation	P_D	T_A = 25°C	2.5	
Gate-to-Source Voltage	V_{GS}	-	± 20	V
Peak Soldering Temperature	T_P	-	270	°C
Operating Junction and Storage Temperature Range	T_J , T_{STG}	-	-55 to + 175	

Table 3 Thermal characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Junction-to-Case (Bottom) ④	$R_{\theta JC}$	-	-	-	13	°C/W
Junction-to-Case (Top) ④	$R_{\theta JC}$	-	-	-	90	
Junction-to-Ambient ⑤	$R_{\theta JA}$	-	-	-	60	
Junction-to-Ambient ⑤	$R_{\theta JA}$ (<10s)	-	-	-	42	

Table 4 Avalanche characteristics

Parameter	Symbol	Values	Unit
Single Pulse Avalanche Energy ②	E_{AS}	13	mJ
Avalanche Current ②	I_{AR}	5.0	A

Notes:

① *Repetitive rating; pulse width limited by max. junction temperature.*
② *Starting T_J = 25°C, L = 1.0mH, R_G = 50Ω, I_{AS} = 5.0A based on test data.*
③ *Pulse width ≤ 400µs; duty cycle ≤ 2%.*
⑧ *R_θ is measured at T_J of approximately 90°C.*
⑤ *When mounted on a 1 inch square PCB (FR-4). Please refer to AN-994 for more details.*
⑥ *Calculated continuous current based on maximum allowable junction temperature.*
⑦ *Current is limited to 10.2A by source bonding technology.*

3 Electrical characteristics

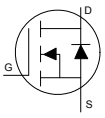
Table 5 Static characteristics

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250µA	100	-	-	V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to 25°C, I_D = 1mA	-	44	-	mV/°C
Static Drain-to-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 6.7A ③	-	34	42	mΩ
		V_{GS} = 4.5V, I_D = 3.4A ③	-	45	59	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 10µA	1.1	1.7	2.3	V
Gate Threshold Voltage Temp. Coefficient	$\Delta V_{GS(th)}/\Delta T_J$		-	-5.6	-	mV°/C
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 80V, V_{GS} = 0V	-	-	1.0	µA
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS} = 20V	-	-	100	nA
	I_{GSS}	V_{GS} = -20V	-	-	100	
Gate Resistance	R_G	-	-	0.9	-	Ω

Table 6 Dynamic characteristics

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Forward Trans conductance	gfs	V_{DS} = 25V, I_D = 6.7A	15	-	-	S
Total Gate Charge	Q_g	I_D = 6.7A V_{DS} = 50V V_{GS} = 4.5V See Fig.8	-	3.7	5.6	nC
Pre-Vth Gate-to-Source Charge	Q_{gs1}		-	0.8	-	
Post-Vth Gate-to-Source Charge	Q_{gs2}		-	0.5	-	
Gate-to-Drain Charge	Q_{gd}		-	1.6	-	
Gate Charge Overdrive	Q_{godr}		-	0.8	-	
Switch Charge (Qgs2 + Qgd)	Q_{sw}		-	2.1	-	
Output Charge	Q_{oss}	V_{DS} = 50V ,V_{GS} = 0V	-	9.5	-	nC
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50V I_D = 6.7A R_G = 2.7Ω V_{GS} = 4.5V ③	-	7.6	-	ns
Rise Time	t_r		-	21	-	
Turn-Off Delay Time	$t_{d(off)}$		-	8.7	-	
Fall Time	t_f		-	10.7	-	
Input Capacitance	C_{iss}	V_{GS} = 0V V_{DS} = 50V f = 1.0MHz	-	440	-	pF
Output Capacitance	C_{oss}		-	80	-	
Reverse Transfer Capacitance	C_{rss}		-	6.3	-	
Output Capacitance	C_{oss}	V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz	-	330	-	
Output Capacitance	C_{oss}	V_{GS} = 0V, V_{DS} = 80V, f = 1.0MHz	-	60	-	

Table 7 Reverse Diode

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Continuous Source Current (Body Diode) ⑥⑦	I_S	MOSFET symbol showing the integral reverse p-n junction diode. 	-	-	11	A
Pulsed Source Current (Body Diode) ①	I_{SM}		-	-	41	
Diode Forward Voltage	V_{SD}	T_J = 25°C, I_S = 6.7A,V_{GS} = 0V ③	-	-	1.2	V
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = 6.7A, V_{DD} = 50V di/dt = 100A/µs	-	22	-	ns
Reverse Recovery Charge	Q_{rr}		-	28	-	nC

4 Electrical characteristic diagrams

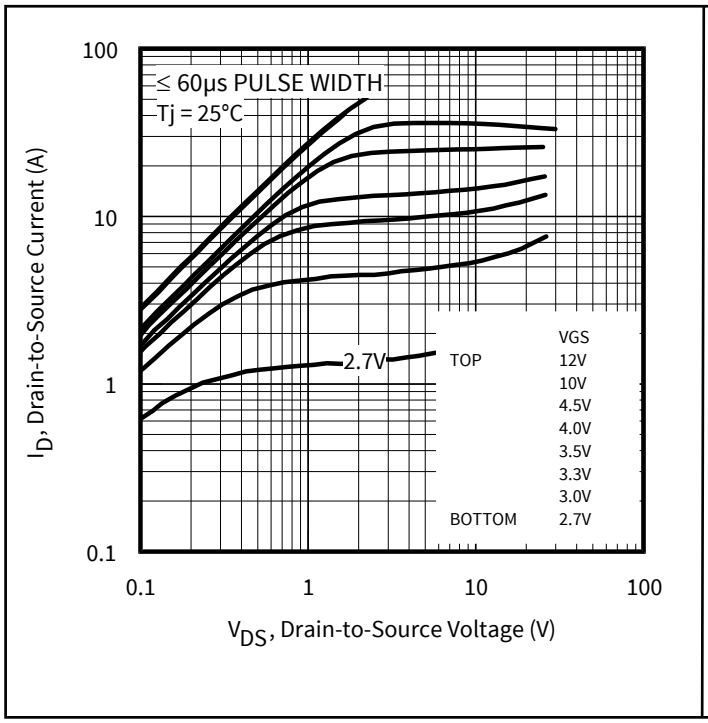


Figure 3 Typical Output Characteristics

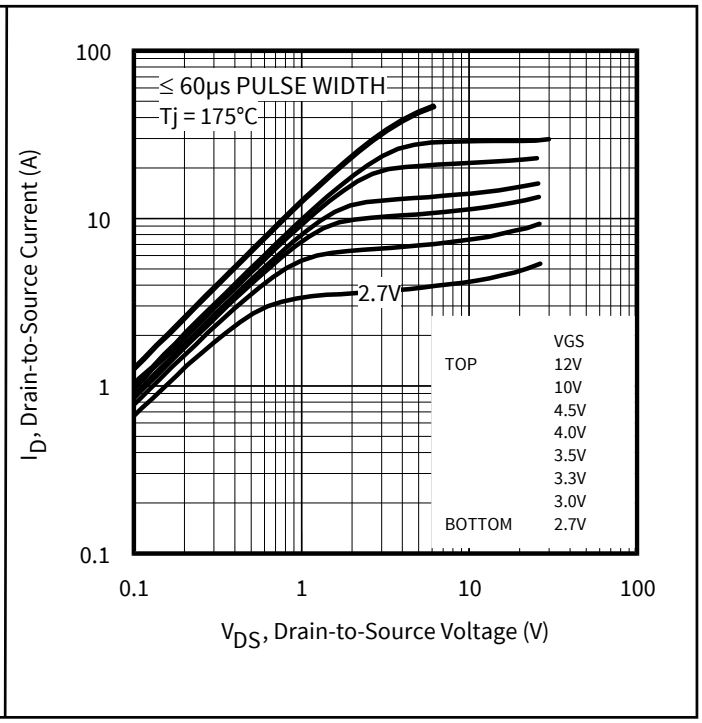


Figure 4 Typical Output Characteristics

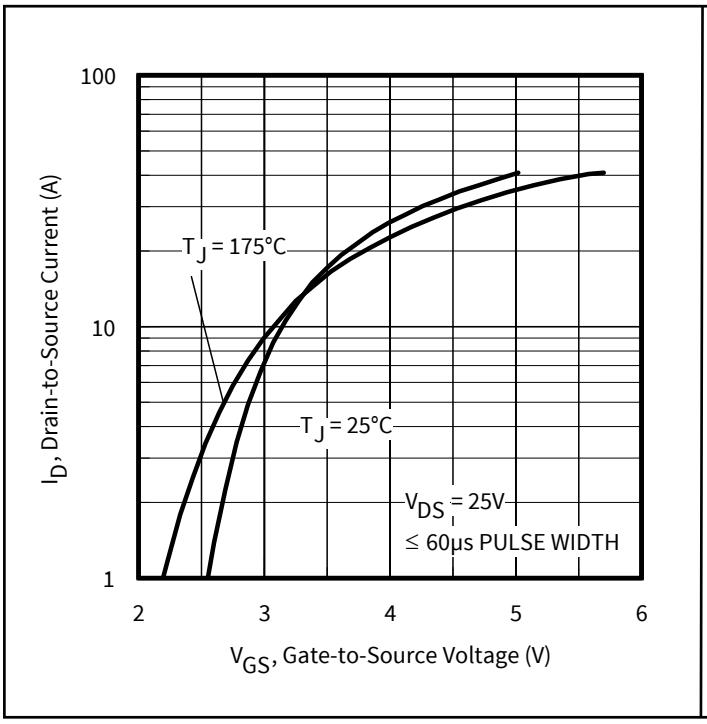


Figure 5 Typical Transfer Characteristics

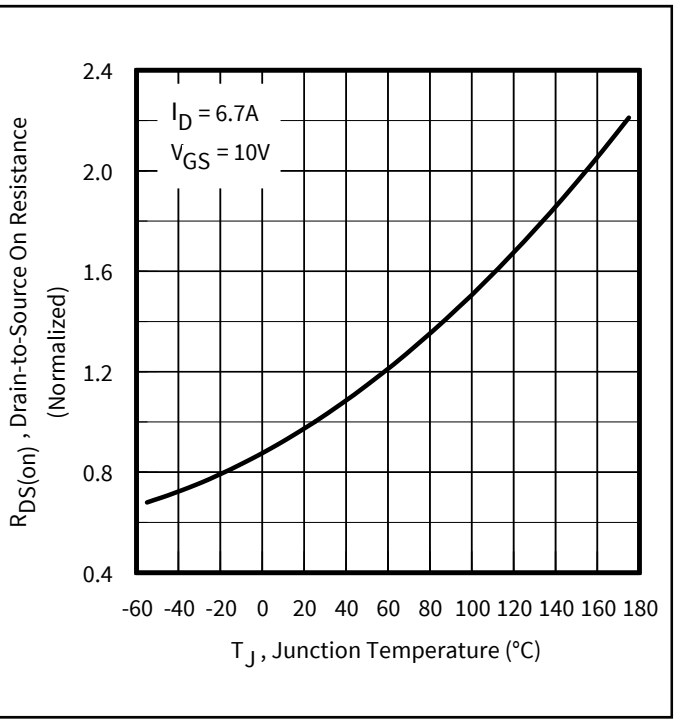


Figure 6 Normalized On-Resistance vs. Temperature

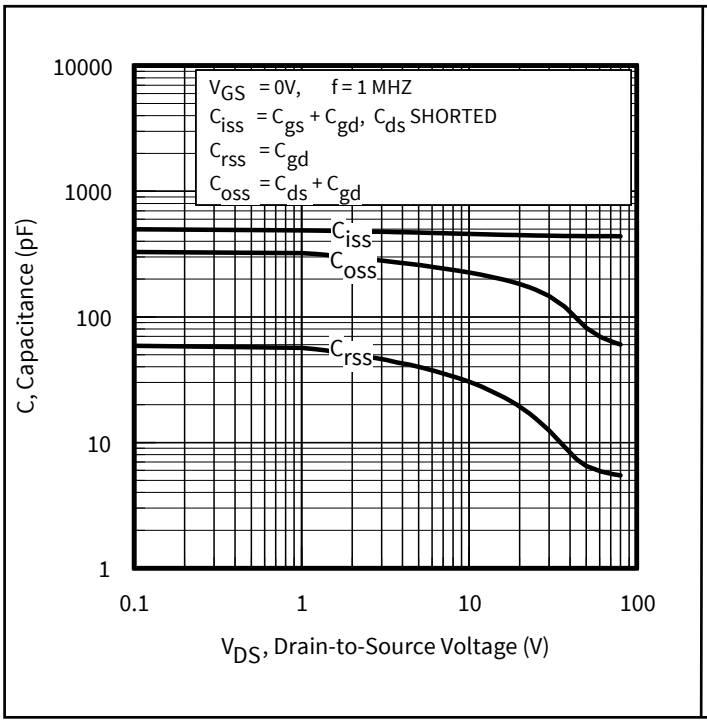


Figure 7 Typical Capacitance vs. Drain-to-Source Voltage

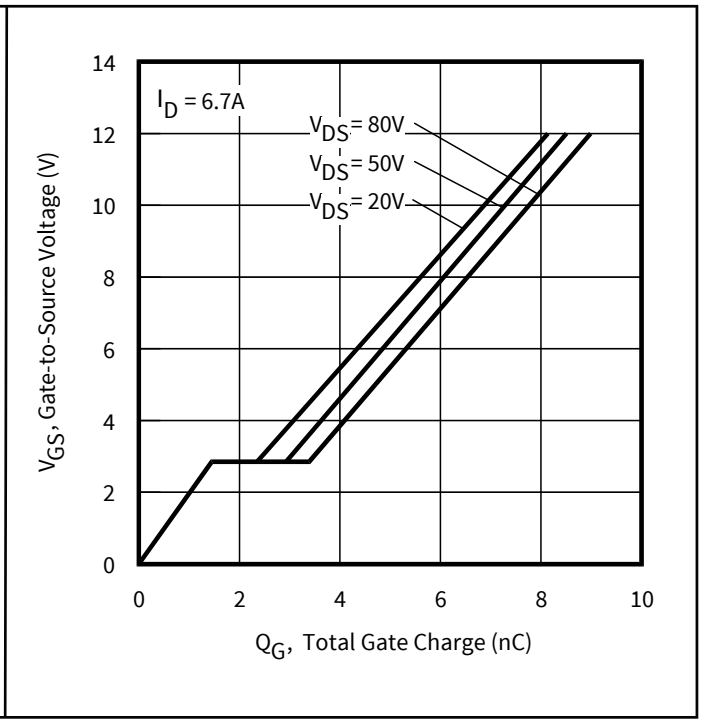


Figure 8 Typical Gate Charge vs. Gate-to-Source Voltage

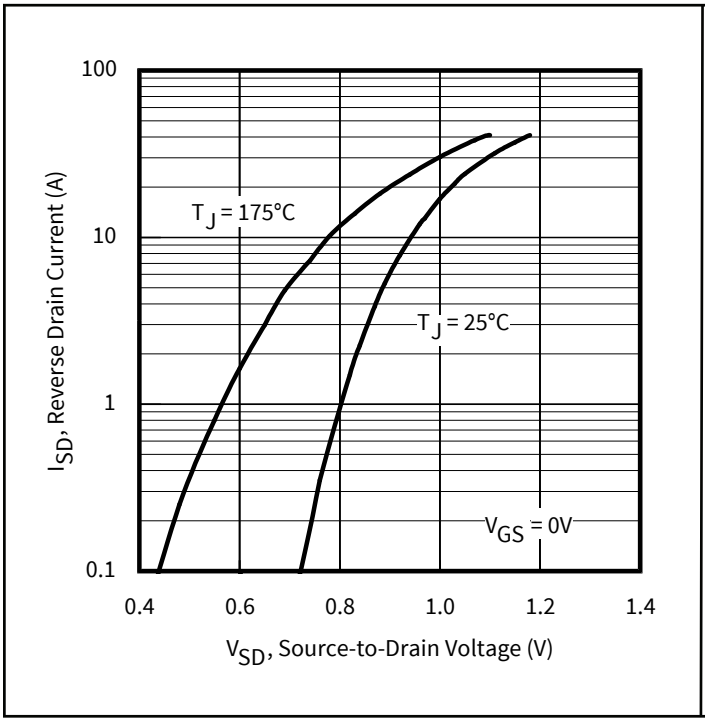


Figure 9 Typical Source-Drain Diode Forward Voltage

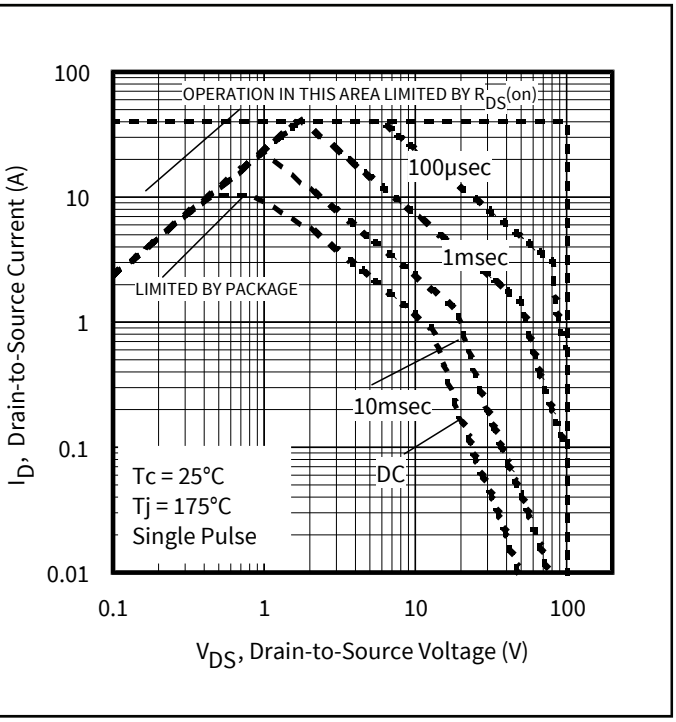


Figure 10 Maximum Safe Operating Area

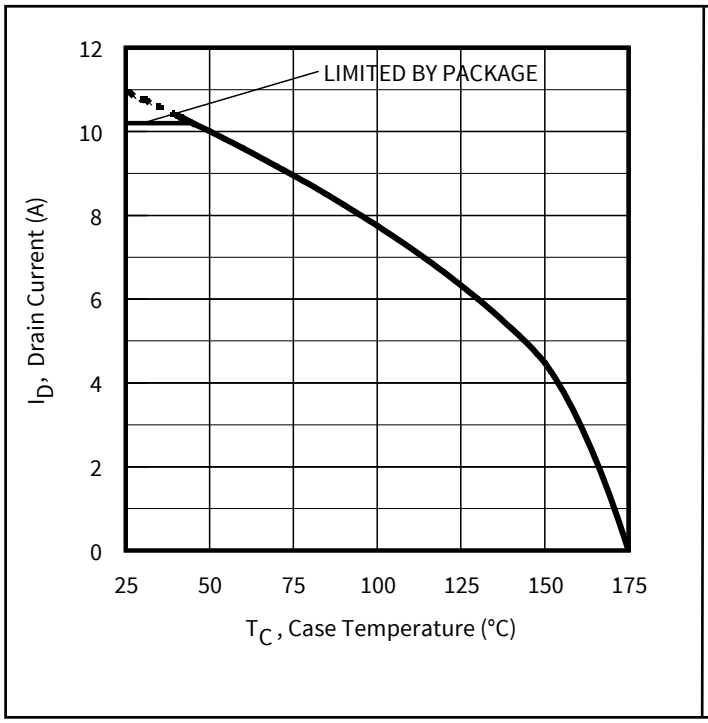


Figure 11 Maximum Drain Current vs. Case Temperature

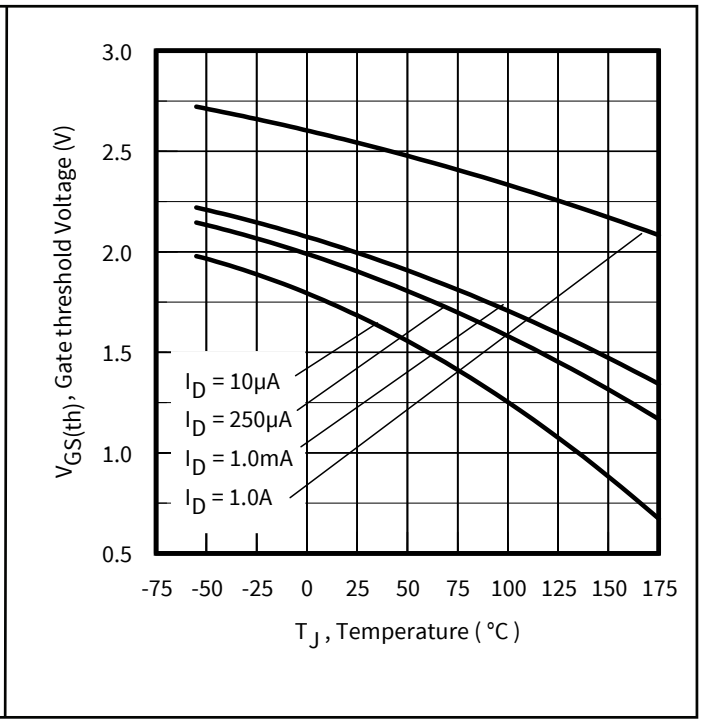


Figure 12 Typical Threshold Voltage vs. Junction Temperature

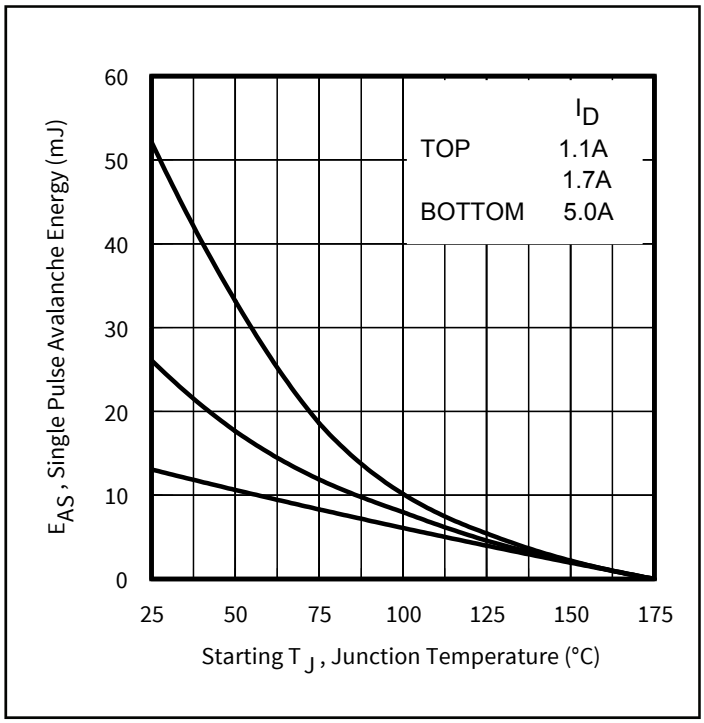


Figure 13 Maximum Avalanche Energy vs. Drain Current

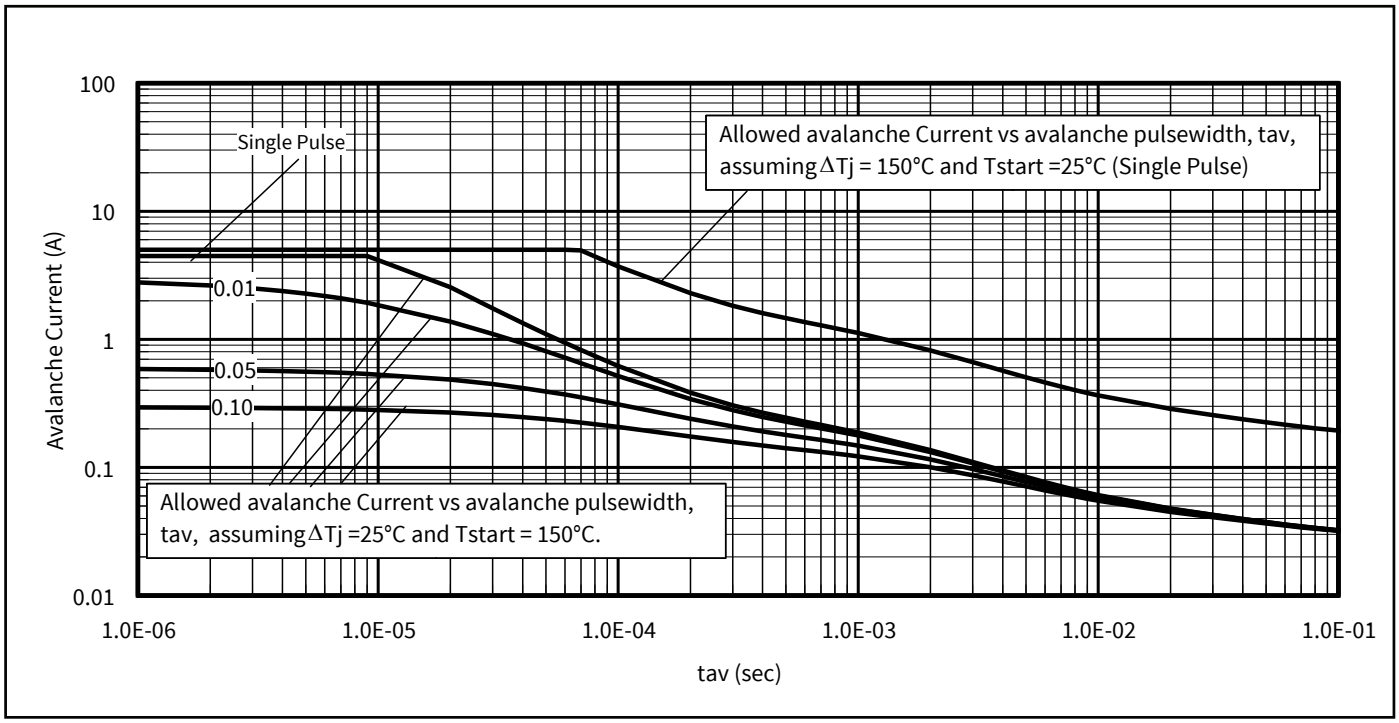


Figure 14 Typical Avalanche Current vs. Pulse Width

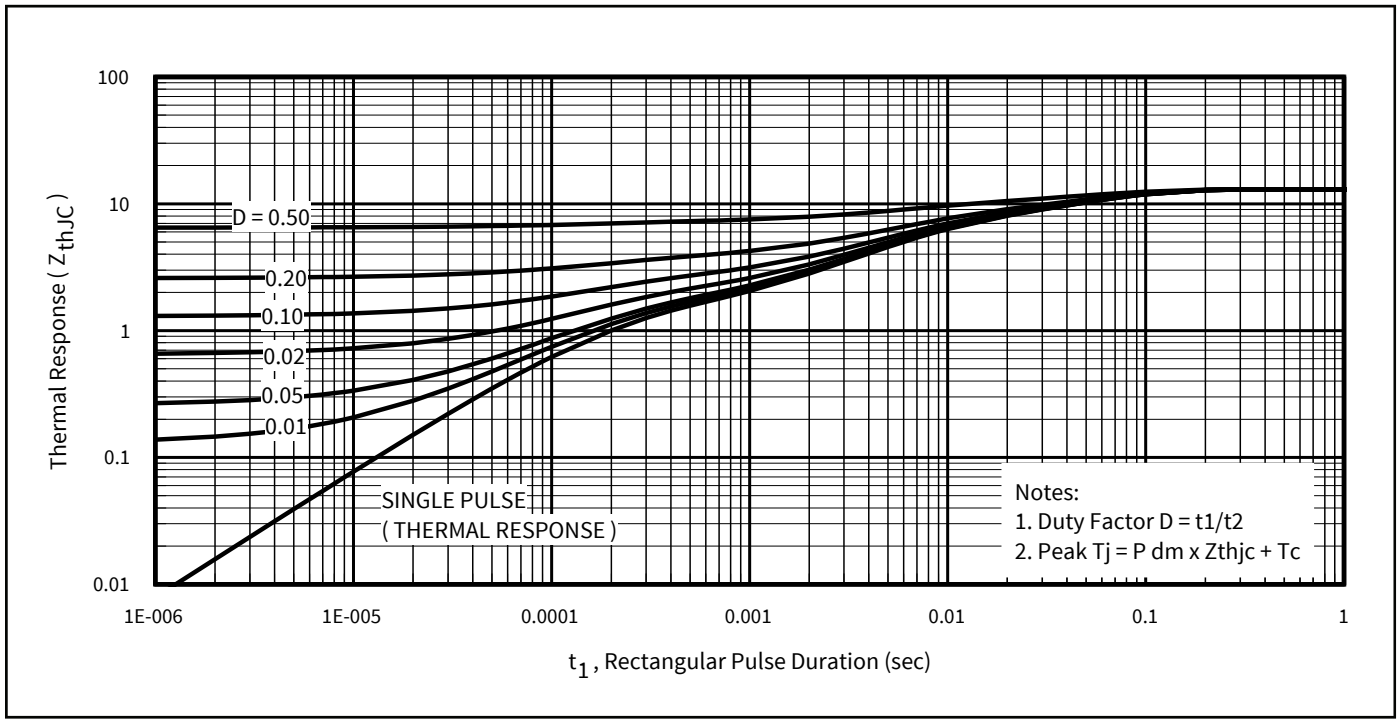


Figure 15 Maximum Effective Transient Thermal Impedance, Junction-to-Case

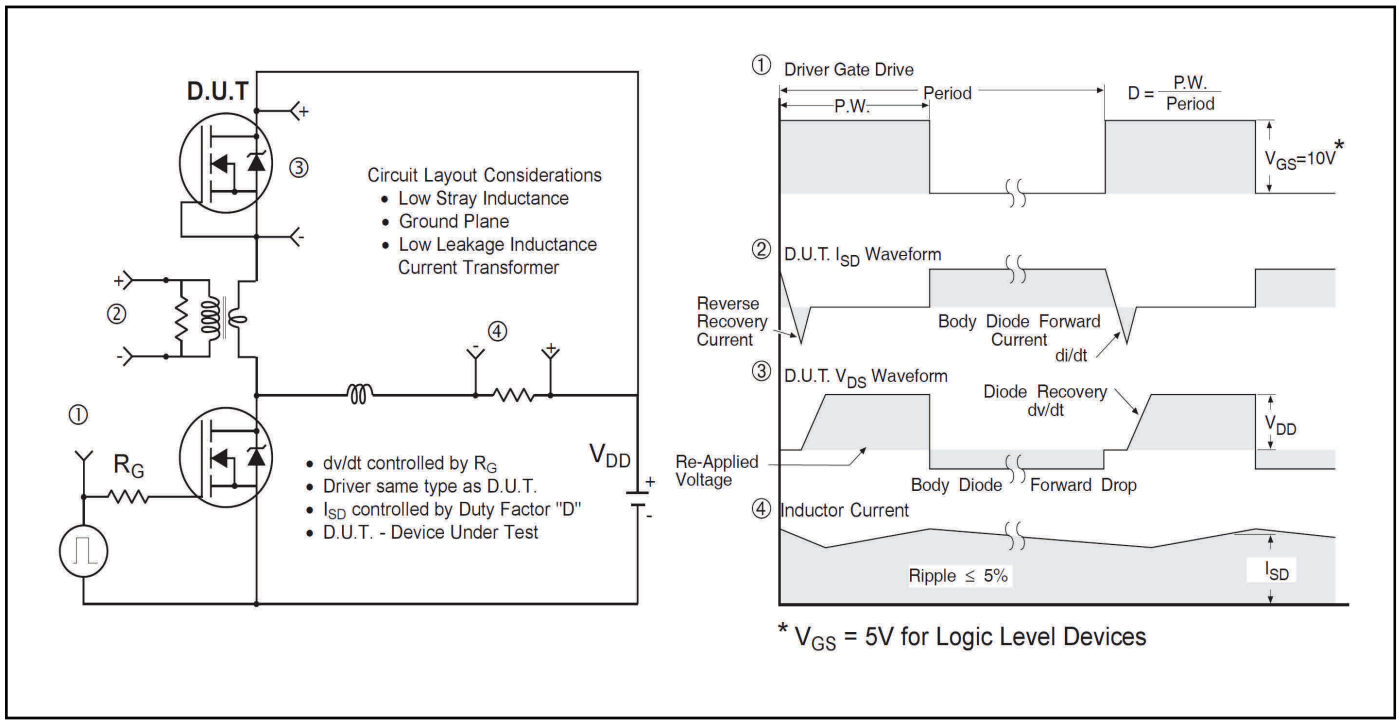


Figure 16 Peak Diode Recovery dv/dt Test Circuit for N-Channel Power MOSFETs

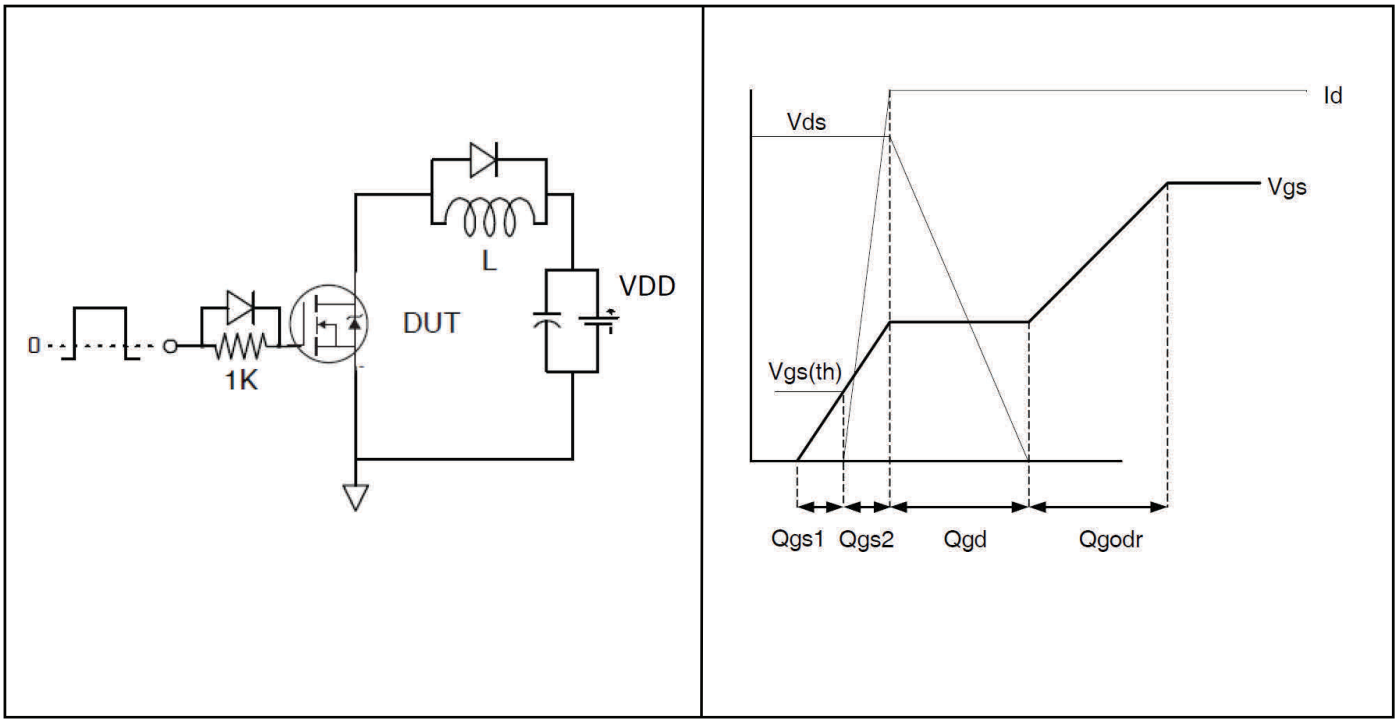


Figure 17a Gate Charge Test Circuit

Figure 17b Gate Charge Waveform

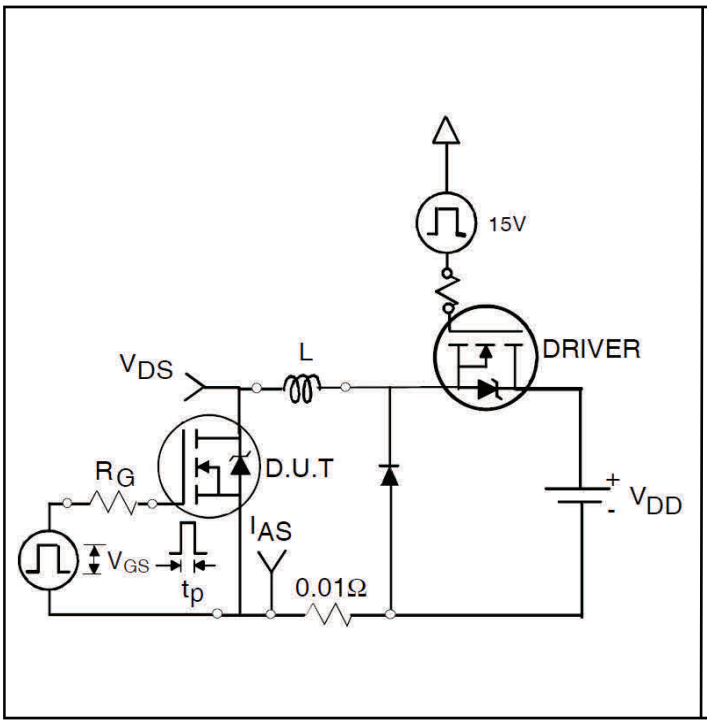


Figure 18a Unclamped Inductive Test Circuit

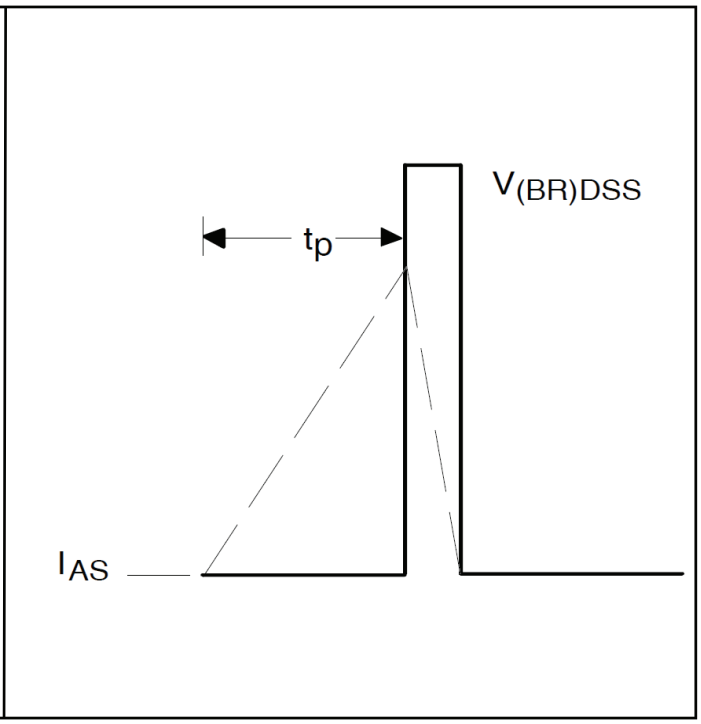


Figure 18b Unclamped Inductive Waveforms

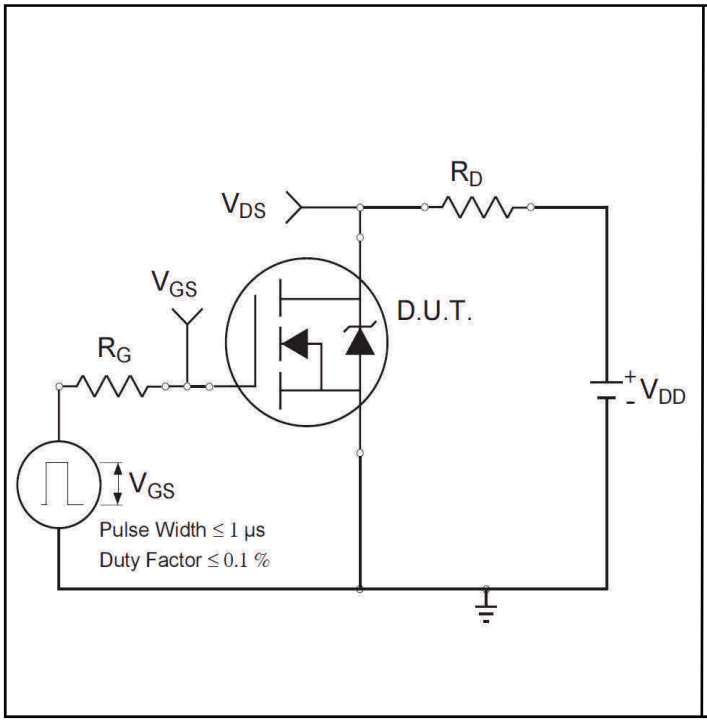


Figure 19a Switching Time Test Circuit

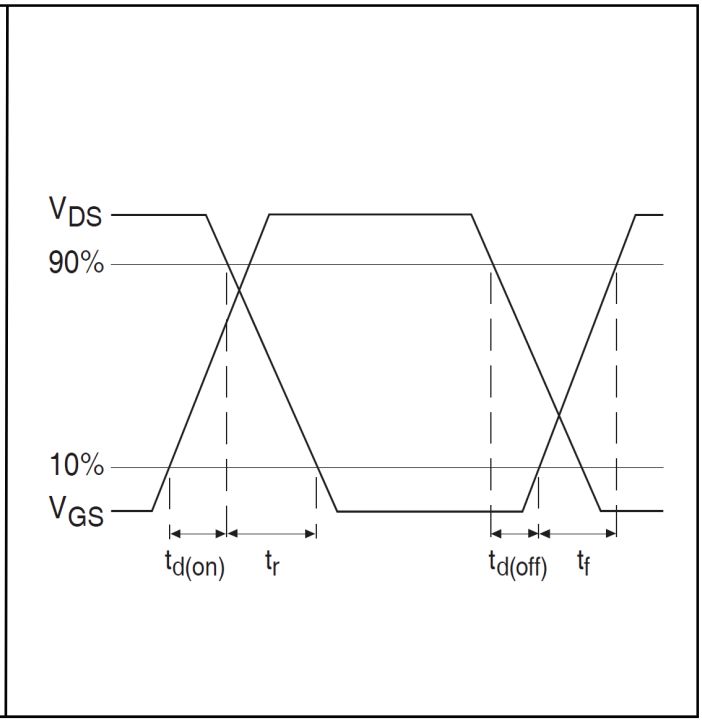
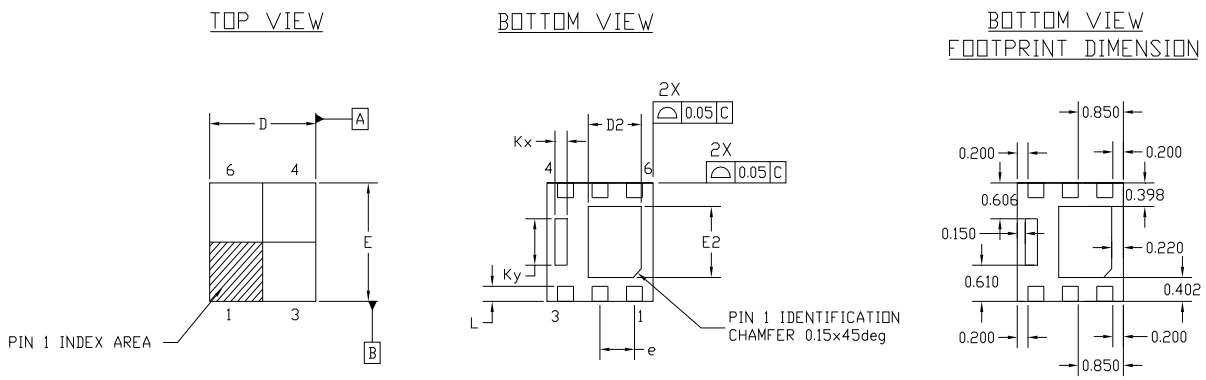


Figure 19b Switching Time Waveforms

5 Package Information

PQFN 2 x 2 Outline Package Details



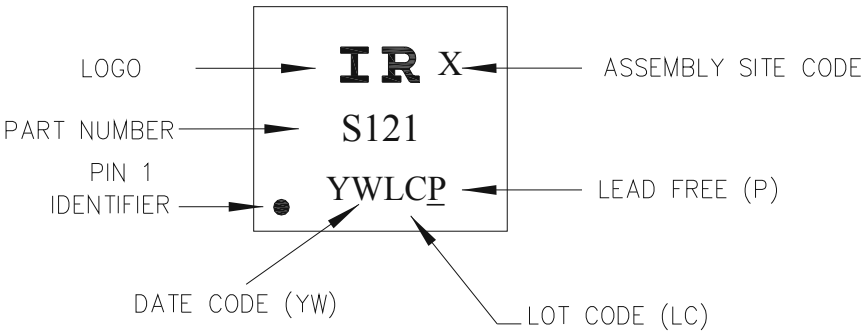
SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.032	0.036	0.040
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.203 REF			0.008 REF		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	1.90	2.00	2.10	0.075	0.079	0.083
D2	0.95	1.00	1.05	0.038	0.040	0.042
E	1.90	2.00	2.10	0.075	0.079	0.083
E2	1.15	1.20	1.25	0.046	0.048	0.050
e	0.65 BSC			0.026 BSC		
L	0.20	0.25	0.30	0.008	0.010	0.012
Kx	0.23 REF			0.010 REF		
Ky	0.785 REF			0.031 REF		

NOTES :

1. DIMENSION AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. CONTROLLING DIMENSIONS : MILLIMETER
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm. FROM TERMINAL TIP.

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: http://www.infineon.com/technical-info/appnotes/an-1136.pdf
For more information on package inspection techniques, please refer to application note AN-1154: http://www.infineon.com/technical-info/appnotes/an-1154.pdf

PQFN 2 x 2 Part Marking



Note: For the most current drawing please refer to website at : www.irf.com/package/

Package Information

PQFN 2 x 2 Tape and Reel

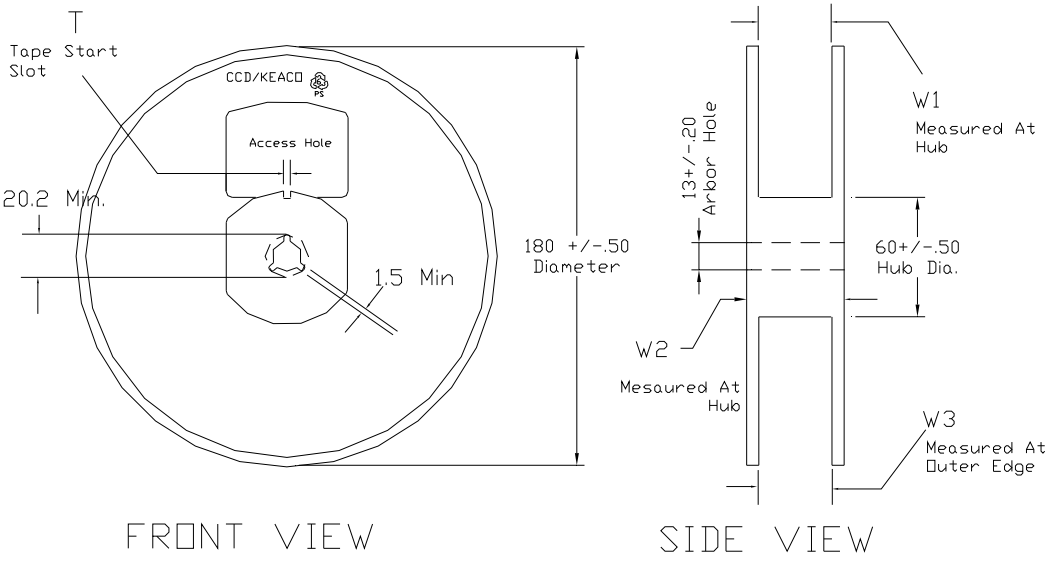
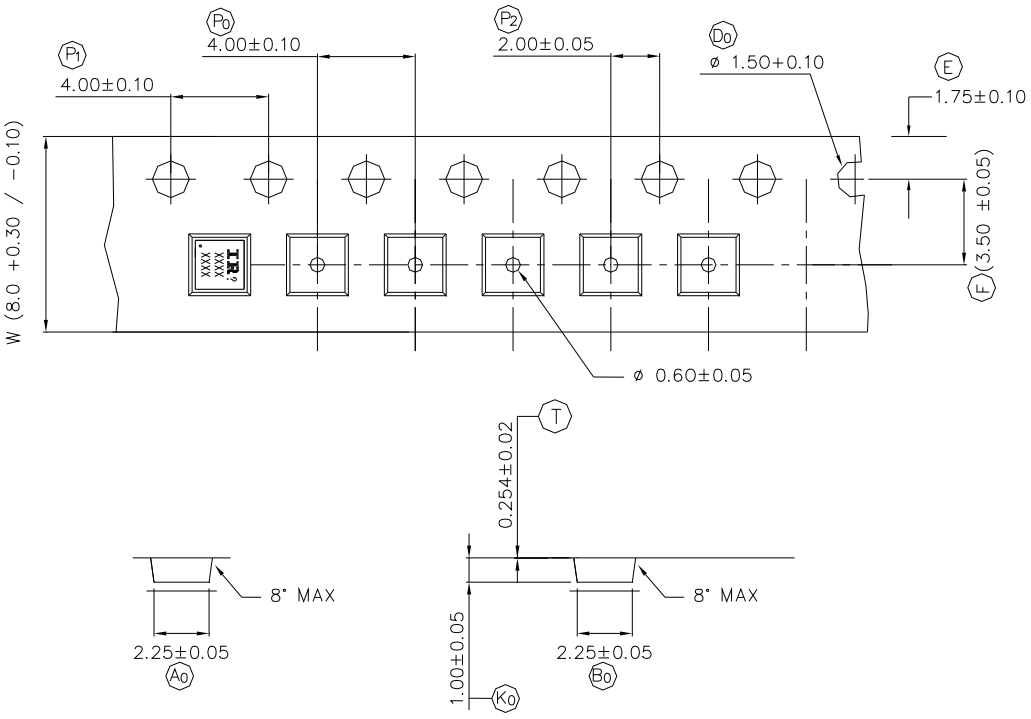


TABLE 1: REEL DETAILS

TAPE WIDTH	T	W1	W2	W3	PART NO
8 MM	3 ± 0.50	$8.4^{+1.5}_{-0.0}$	14.4 Max	7.90 Min 10.9 Max	91586-1
12 MM	5 ± 0.50	$12.4^{+2.0}_{-0.0}$	18.4 Max	11.9 Min 15.4 Max	91586-2

Note: Surface resistivity is $\geq 1\times10^{5}$ but $< 1\times10^{12}$ ohm/sq.



NOTE: The Surface Resistivity is 10^{4} – 10^{8} OHM/SQ

Note: For the most current drawing please refer to website at : www.irf.com/package/

6 Qualification Information

Qualification Information

Qualification Level	Industrial (per JEDEC JESD47F) †	
Moisture Sensitivity Level	PQFN 2 mm x 2 mm	MSL1 (per JEDEC J-STD-020D)†
RoHS Compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Revision History

Major changes since the last revision

Page or Reference	Revision	Date	Description of changes
All pages	1.0	2015-12-03	• First release data sheet as Provisional.
All page	1.1	2016-09-12	• Updated datasheet with revised package picture and outline drawings. • Datasheet is released as Provisional.
All pages	1.2	2016-10-17	• Added Switch Time test data. • Datasheet is released as Provisional.
All pages	1.3	2017-08-21	• Parts tested as Unique datasheet with revised current and all other tests • Updated ds in New Infineon Template • Added Link for Package Information—pages 12, 13 • Added IR—PQFN 2x2 Package Picture—page 1 • Datasheet completed as Approved Not Released. • Datasheet is w/o “Approved Not Released”
All pages	2.0	2017-10-06	• First release data sheet on Web.
All pages	2.1	2018-05-08	• Corrected typo on part marking from “100HS121” to “S121” to matched actual marking on the devices –page12
All pages	2.2	2019-12-13	• Features-Corrected from “IR MOSFET /OptiMOS™5” to “OptiMOS™5” to in line with the technology positioning of product –page 1.

Edition 2015-05-06
Published by
Infineon Technologies AG
81726 Munich, Germany

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Document reference

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