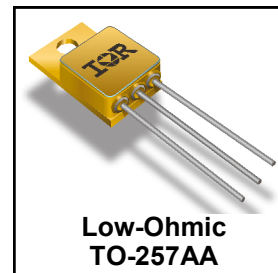


**RADIATION HARDENED  
POWER MOSFET  
THRU-HOLE (Low-Ohmic TO-257AA)**

**60V, N-CHANNEL**  
**REF: MIL-PRF-19500/775**  
**R<sub>9</sub> TECHNOLOGY**

**Product Summary**

Part Number	Radiation Level	RDS(on)	I <sub>D</sub>	QPL Part Number
IRHYS9A7034CM	100 kRads (Si)	19mΩ	30A*	JANSR2N7647T3
IRHYS9A3034CM	300 kRads (Si)	19mΩ	30A*	JANSF2N7647T3



**Description**

IR HiRel R9 technology provides superior power MOSFETs for space applications. These devices have improved immunity to Single Event Effect (SEE) and have been characterized for useful performance with Linear Energy Transfer (LET) up to 90MeV/(mg/cm<sup>2</sup>). Their combination of low RDS(on) and faster switching times reduces the power losses and increases power density in today's high speed switching applications such as DC-DC converters and motor controllers. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

**Features**

- Low RDS(on)
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Electrically Isolated
- Ceramic Eyelets
- Light Weight
- ESD Rating: Class 2 per MIL-STD-750, Method 1020

**Absolute Maximum Ratings**

**Pre-Irradiation**

Symbol	Parameter	Value	Units
I <sub>D1</sub> @ V <sub>GS</sub> = 12V, T <sub>C</sub> = 25°C	Continuous Drain Current	30*	A
I <sub>D2</sub> @ V <sub>GS</sub> = 12V, T <sub>C</sub> = 100°C	Continuous Drain Current	28	
I <sub>DM</sub> @ T <sub>C</sub> = 25°C	Pulsed Drain Current ①	120	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	75	W
	Linear Derating Factor	0.6	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	784	mJ
I <sub>AR</sub>	Avalanche Current ①	30	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	9.5	V/ns
T <sub>J</sub> T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (0.063 in./1.6mm from case for 10s)	
	Weight	4.3 (Typical)	

\* Current is limited by package

For Footnotes, refer to the page 2.

### Electrical Characteristics @ T<sub>j</sub> = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	60	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.07	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	19	mΩ	V <sub>GS</sub> = 12V, I <sub>D2</sub> = 28A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 1.0mA
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	—	-9.2	—	mV/°C	
G <sub>fs</sub>	Forward Transconductance	20	—	—	S	V <sub>DS</sub> = 15V, I <sub>D2</sub> = 28A ④
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	1.0	μA	V <sub>DS</sub> = 48V, V <sub>GS</sub> = 0V
		—	—	10		V <sub>DS</sub> = 48V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V <sub>GS</sub> = -20V
Q <sub>G</sub>	Total Gate Charge	—	—	45	nC	I <sub>D1</sub> = 30A
Q <sub>GS</sub>	Gate-to-Source Charge	—	—	14		V <sub>DS</sub> = 30V
Q <sub>GD</sub>	Gate-to-Drain ('Miller') Charge	—	—	11		V <sub>GS</sub> = 12V
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	20	ns	V <sub>DD</sub> = 30V
t <sub>r</sub>	Rise Time	—	—	40		I <sub>D1</sub> = 30A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	45		R <sub>G</sub> = 7.5Ω
t <sub>f</sub>	Fall Time	—	—	30		V <sub>GS</sub> = 12V
L <sub>s</sub> + L <sub>D</sub>	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm / 0.25 in from package)
C <sub>iss</sub>	Input Capacitance	—	1740	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	660	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	5.0	—		f = 1.0MHz
R <sub>G</sub>	Gate Resistance	—	1.2	—	Ω	f = 1.0MHz, open drain

### Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	30*	A	
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	120		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.2	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 30A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	—	130	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 30A, V <sub>DD</sub> ≤ 25V
Q <sub>rr</sub>	Reverse Recovery Charge	—	—	525	nC	di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

\* Current is limited by package

### Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	—	1.67	°C/W
R <sub>θJA</sub>	Junction-to-Ambient (Typical Socket Mount)	—	—	80	°C/W

### Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V<sub>DD</sub> = 60V, starting T<sub>J</sub> = 25°C, L = 2.0mH, Peak I<sub>L</sub> = 28A, V<sub>GS</sub> = 20V
- ③ I<sub>SD</sub> ≤ 30A, di/dt ≤ 810A/μs, V<sub>DD</sub> ≤ 60V, T<sub>J</sub> ≤ 150°C
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%
- ⑤ Total Dose Irradiation with V<sub>GS</sub> Bias. 12 volt V<sub>GS</sub> applied and V<sub>DS</sub> = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- ⑥ Total Dose Irradiation with V<sub>DS</sub> Bias. 48 volt V<sub>DS</sub> applied and V<sub>GS</sub> = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

## Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

**Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥**

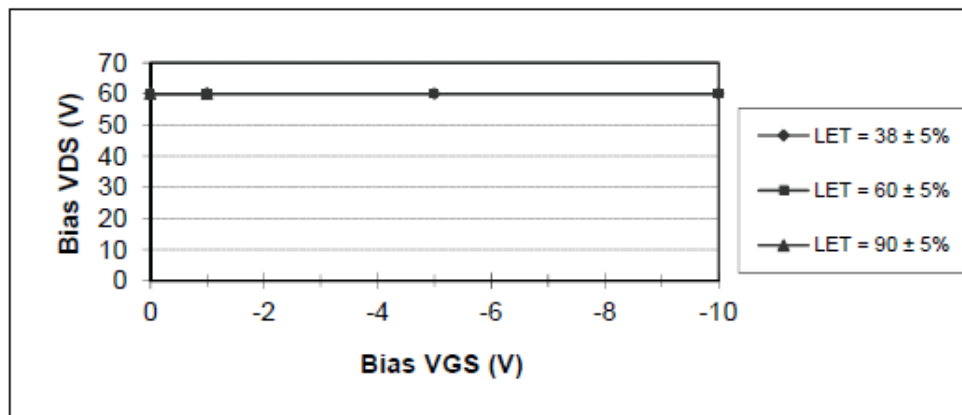
Symbol	Parameter	Up to 300 kRads (Si) <sup>1</sup>		Units	Test Conditions
		Min.	Max.		
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	60	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 1.0mA
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	100	nA	V <sub>GS</sub> = 20V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	-100	nA	V <sub>GS</sub> = -20V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	1.0	μA	V <sub>DS</sub> = 48V, V <sub>GS</sub> = 0V
R <sub>DS(on)</sub>	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	20	mΩ	V <sub>GS</sub> = 12V, I <sub>D2</sub> = 28A
R <sub>DS(on)</sub>	Static Drain-to-Source ④ On-State Resistance (Low-Ohmic TO-257AA)	—	19	mΩ	V <sub>GS</sub> = 12V, I <sub>D2</sub> = 28A
V <sub>SD</sub>	Diode Forward Voltage	—	1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 30A

1. Part numbers IRHYS9A7034CM (JANSR2N7647T3) and IRHYS9A3034CM (JANSF2N7647T3)

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

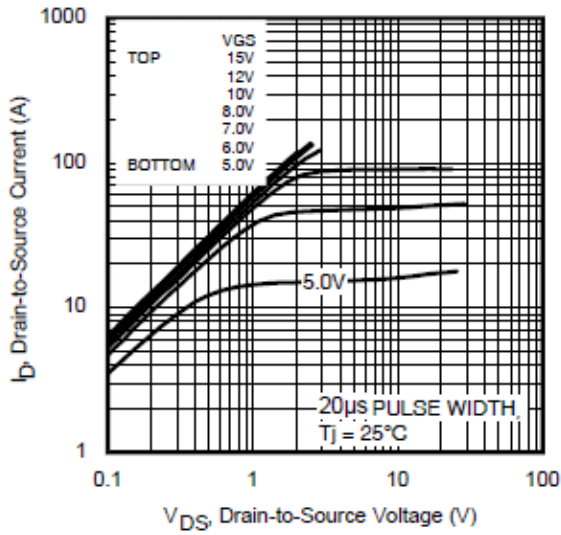
**Table 2. Typical Single Event Effect Safe Operating Area**

LET (MeV/(mg/cm <sup>2</sup> ))	Energy (MeV)	Range (μm)	VDS (V)			
			@ VGS = 0V	@ VGS = -1V	@ VGS = -5V	@ VGS = -10V
38 ± 5%	355 ± 7.5%	43 ± 7.5%	60	60	60	60
60 ± 5%	753 ± 7.5%	60 ± 10%	60	60	60	60
90 ± 5%	1515 ± 7.5%	82 ± 7.5%	60	60	—	—

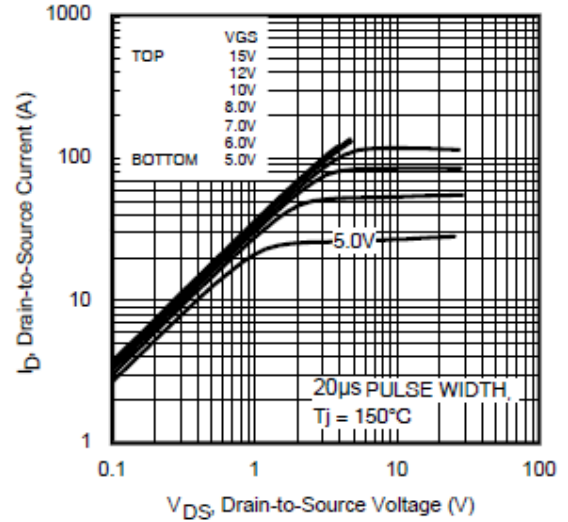


**Fig a.** Typical Single Event Effect, Safe Operating Area

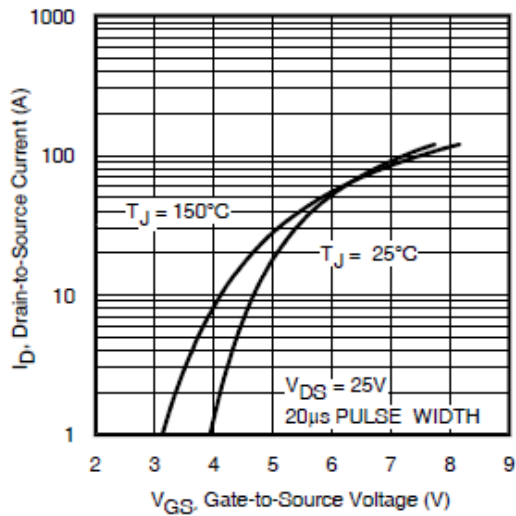
For Footnotes, refer to the page 2.



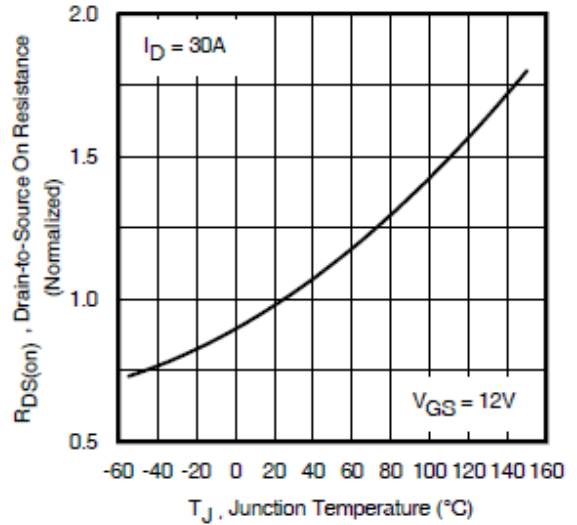
**Fig 1.** Typical Output Characteristics



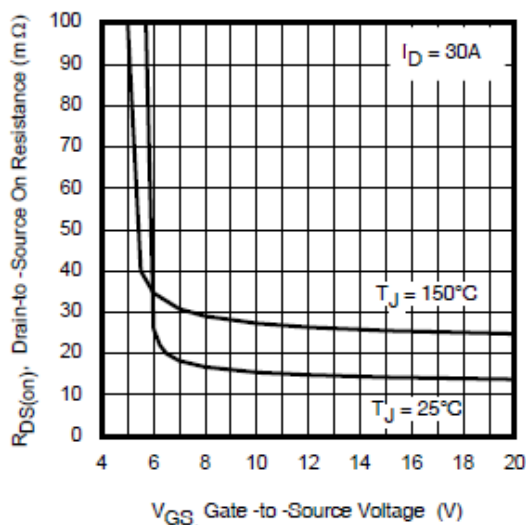
**Fig 2.** Typical Output Characteristics



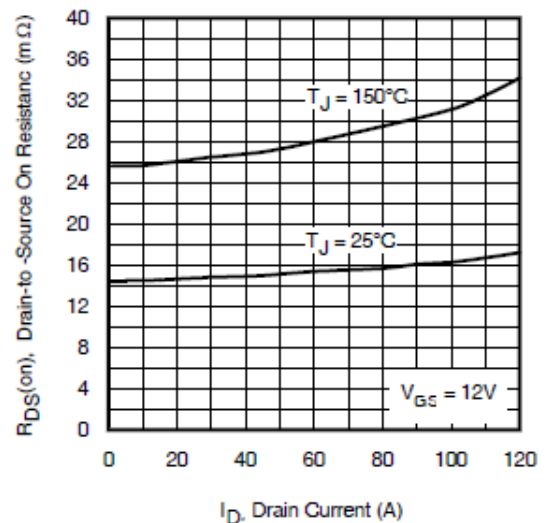
**Fig 3.** Typical Transfer Characteristics



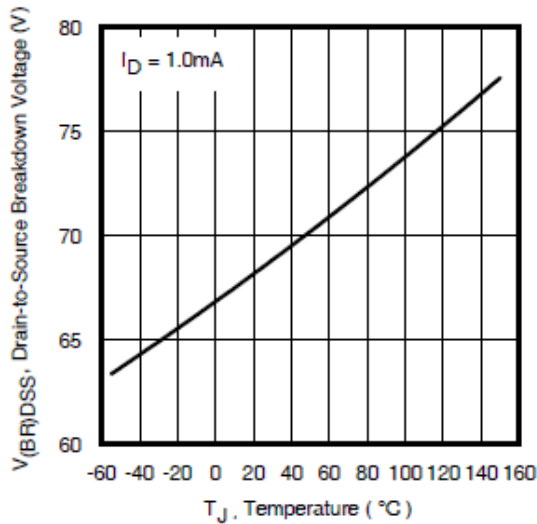
**Fig 4.** Normalized On-Resistance Vs. Temperature



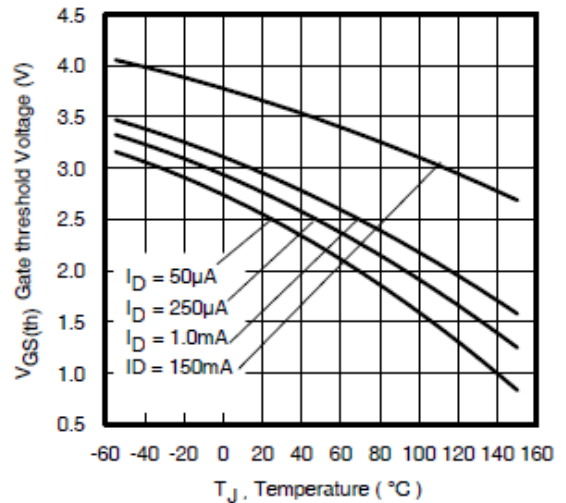
**Fig 5.** Typical On-Resistance Vs Gate Voltage



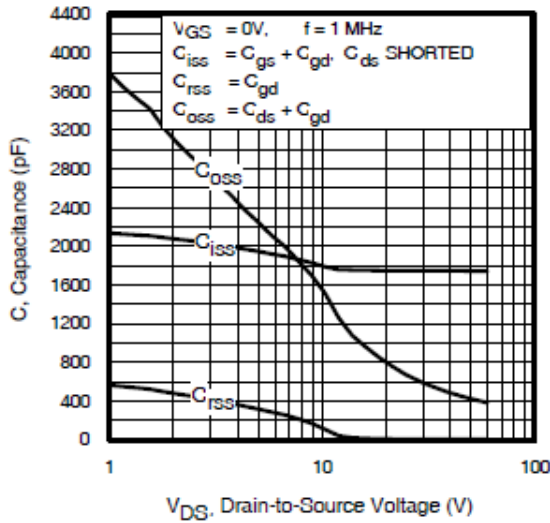
**Fig 6.** Typical On-Resistance Vs Drain Current



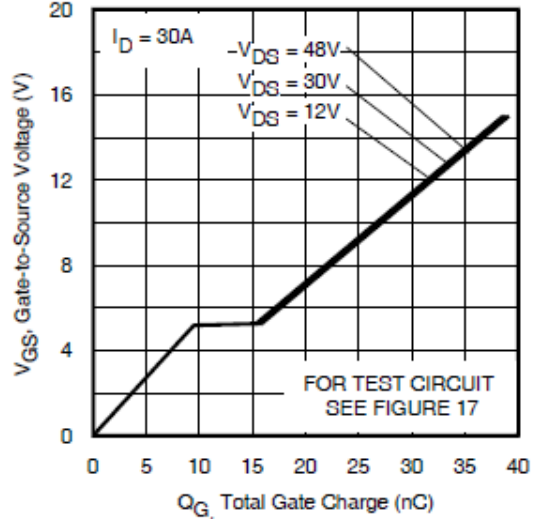
**Fig 7.** Typical Drain-to-Source Breakdown Voltage Vs Temperature



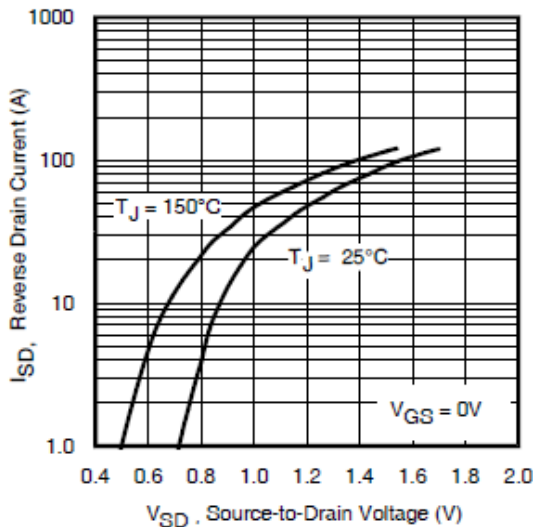
**Fig 8.** Typical Threshold Voltage Vs Temperature



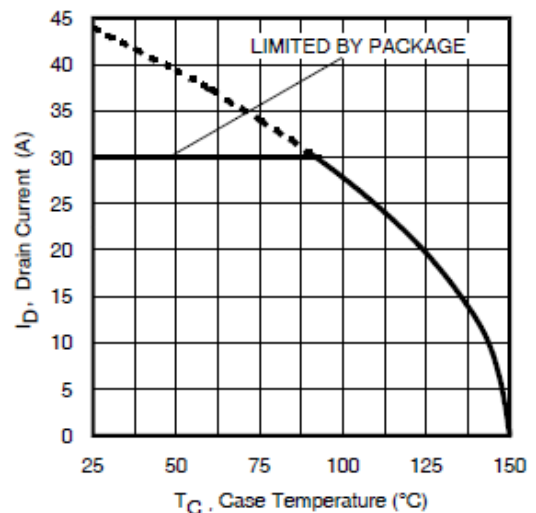
**Fig 9.** Typical Capacitance Vs. Drain-to-Source Voltage



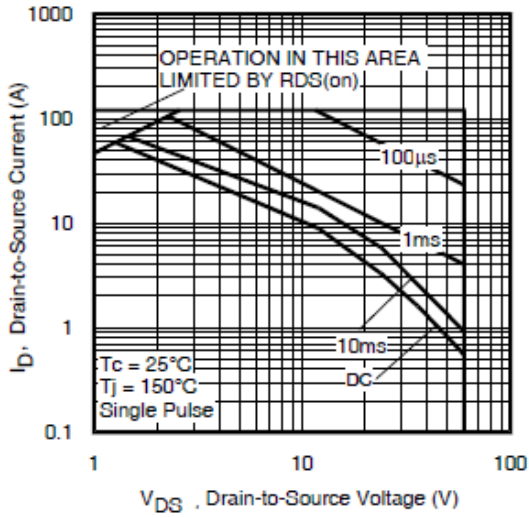
**Fig 10.** Typical Gate Charge Vs. Gate-to-Source Voltage



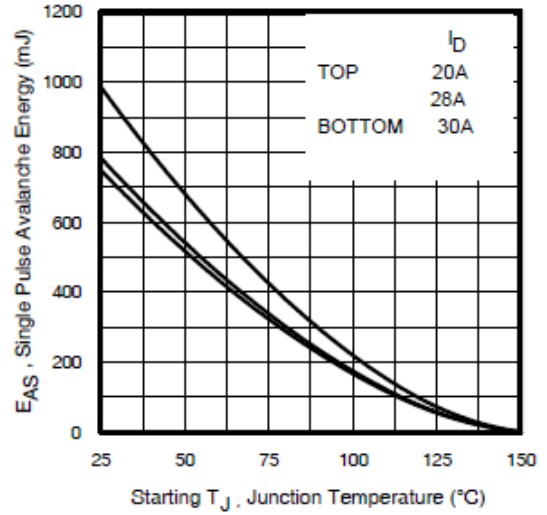
**Fig 11.** Typical Source-Drain Diode Forward Voltage



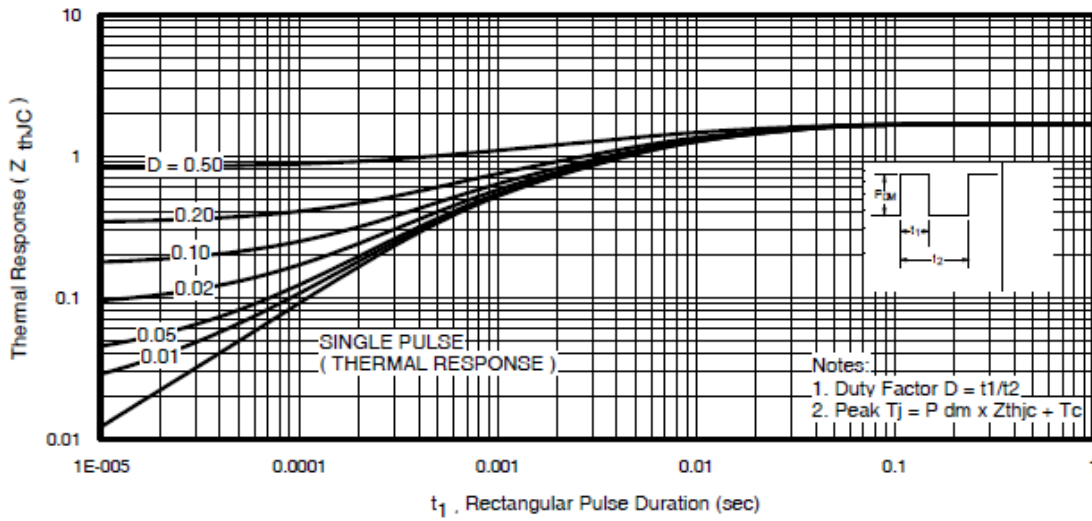
**Fig 12.** Maximum Drain Current Vs. Case Temperature



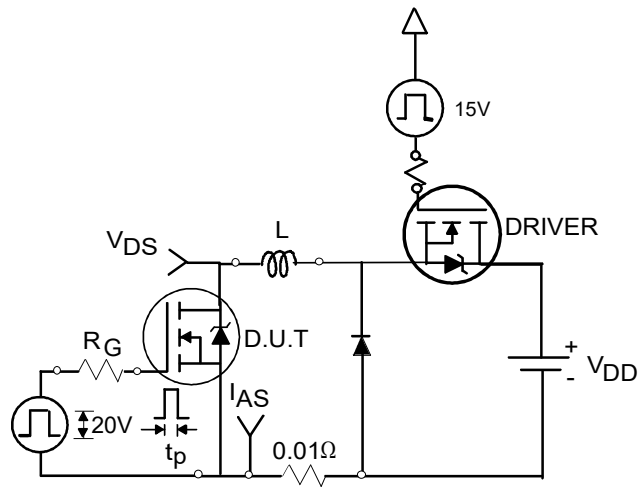
**Fig 13.** Maximum Safe Operating Area



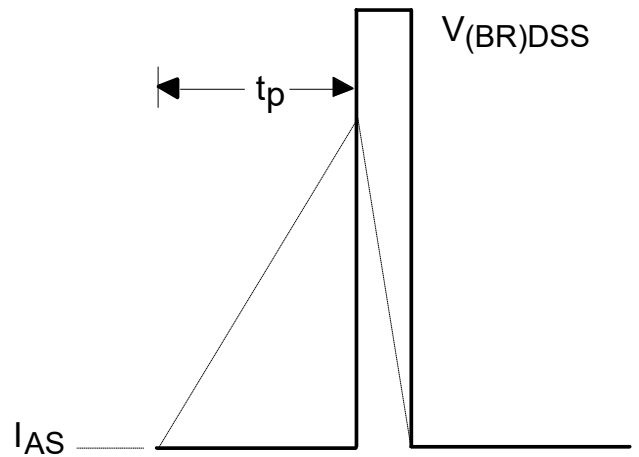
**Fig 14.** Maximum Avalanche Energy Vs. Drain Current



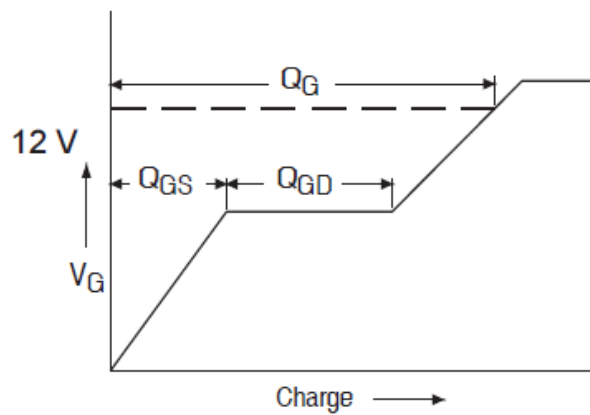
**Fig 15.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



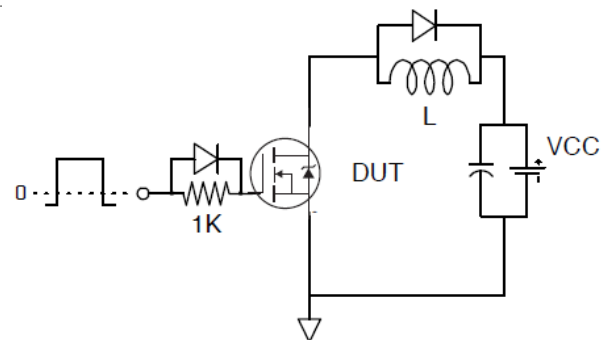
**Fig 16a.** Unclamped Inductive Test Circuit



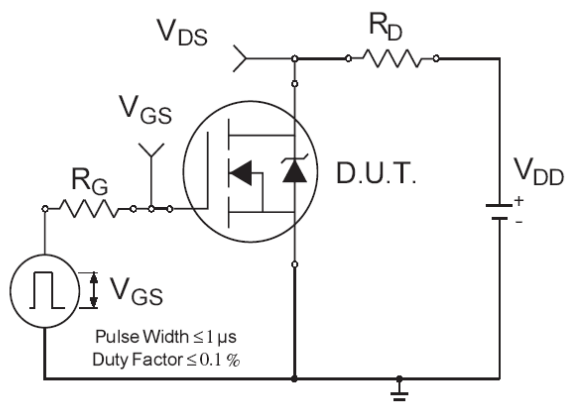
**Fig 16b.** Unclamped Inductive Wave-



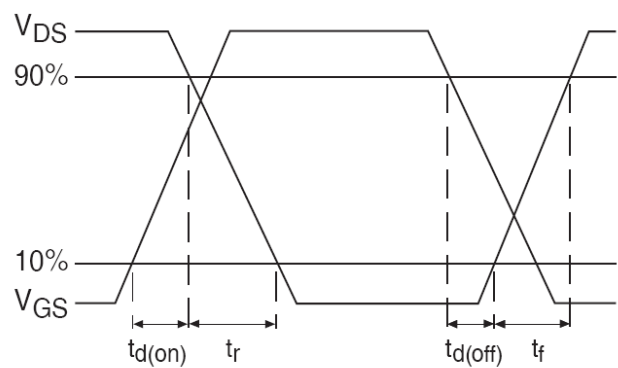
**Fig 17a.** Gate Charge Waveform



**Fig 17b.** Gate Charge Test Circuit



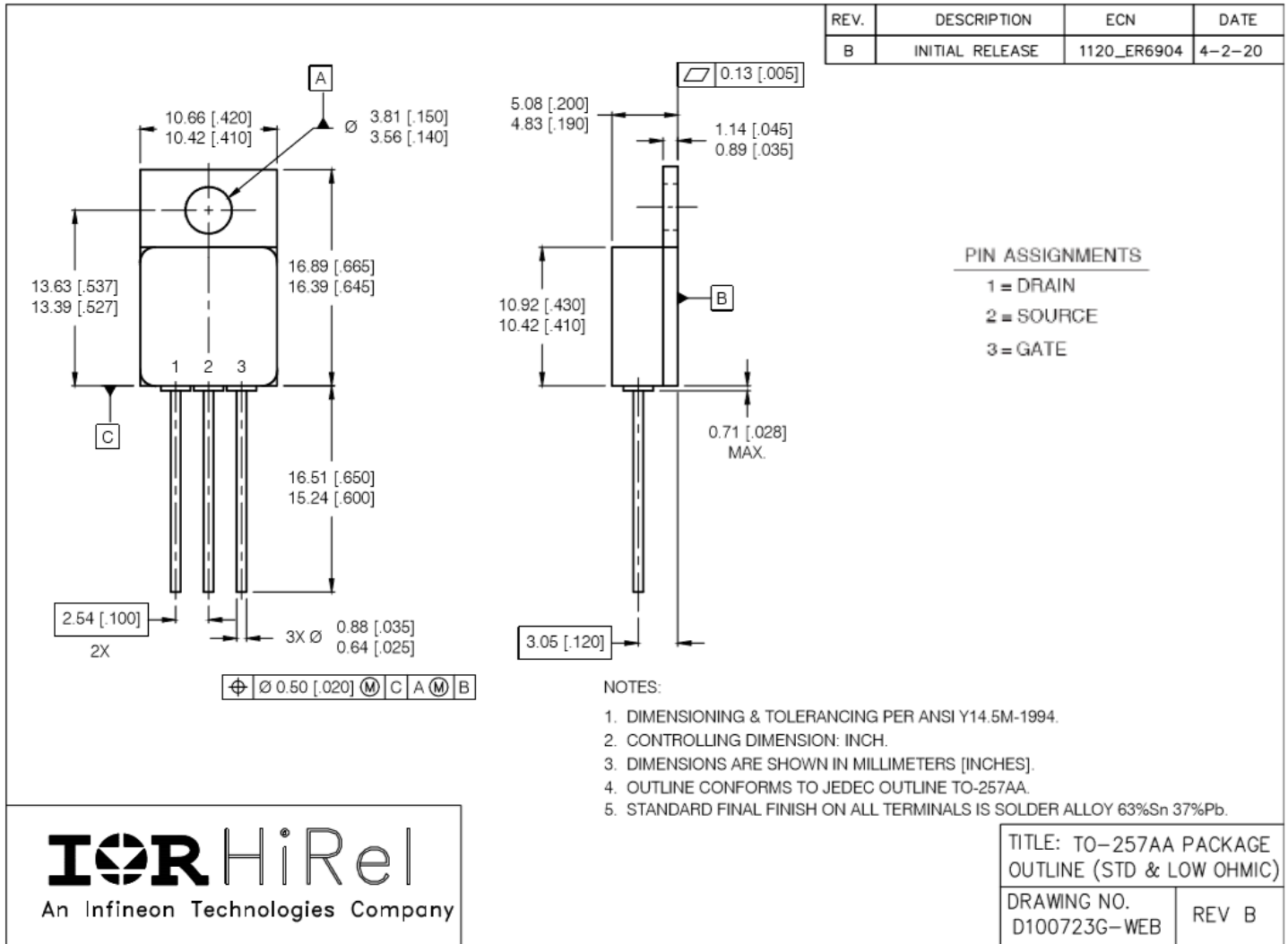
**Fig 18a.** Switching Time Test Circuit



**Fig 18b.** Switching Time Waveforms

Note: For the most updated package outline, please see the website: [TO-257AA](http://TO-257AA)

**Case Outline and Dimensions - Low-Ohmic TO-257AA**



**BERYLLIA WARNING PER MIL-PRF-19500**

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.



### **IMPORTANT NOTICE**

The information given in this document shall be in no event regarded as guarantee of conditions or characteristic. The data contained herein is a characterization of the component based on internal standards and is intended to demonstrate and provide guidance for typical part performance. It will require further evaluation, qualification and analysis to determine suitability in the application environment to confirm compliance to your system requirements.

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