

IRHYK57133CMSE

PD-96898A

Radiation Hardened Power MOSFET Surface Mount (Low-Ohmic TO-257AA) 130V, 20A, N-channel, R5 Technology

Features

- Single event effect (SEE) hardened
- Low $R_{DS(on)}$
- Fast switching
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Electrically isolated
- Ceramic eyelets
- Light Weight
- ESD rating: Class 1C per MIL-STD-750, Method 1020

Potential Applications

- DC-DC converter
- Motor drives

Product Validation

Qualified to JANS screening flow according to MIL-PRF-19500 for space applications

Description

IR HiRel R5 technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 MeV·cm²/mg. The combination of low $R_{DS(on)}$ and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well-established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHYK57133CMSE	Low-Ohmic TO-257AA	COTS	100 krad(Si)

Product Summary

- BV_{DSS} : 130V
- I_D : 20A
- $R_{DS(on),max}$: 82mΩ
- $Q_{G,max}$: 48nC



Table of contents

Table of contents

Features	1
Potential Applications.....	1
Product Validation.....	1
Description	1
Ordering Information.....	1
Table of contents.....	2
1 Absolute Maximum Ratings	3
2 Device Characteristics	4
2.1 Electrical Characteristics (Pre-Irradiation).....	4
2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)	5
2.3 Thermal Characteristics	5
2.4 Radiation Characteristics.....	5
2.4.1 Electrical Characteristics — Post Total Dose Irradiation	5
2.4.2 Single Event Effects — Safe Operating Area	6
3 Electrical Characteristics Curves (Pre-irradiation)	7
4 Test Circuits (Pre-irradiation)	10
5 Package Outline.....	11
Revision history.....	12

Absolute Maximum Ratings

1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
$I_{D1} @ V_{GS} = 12V, T_C = 25^\circ C$	Continuous Drain Current	20	A
$I_{D2} @ V_{GS} = 12V, T_C = 100^\circ C$	Continuous Drain Current	12.5	A
$I_{DM} @ T_C = 25^\circ C$	Pulsed Drain Current ¹	80	A
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	75	W
	Linear Derating Factor	0.6	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ²	73	mJ
I_{AR}	Avalanche Current ¹	20	A
E_{AR}	Repetitive Avalanche Energy ¹	7.5	mJ
dv/dt	Peak Diode Reverse Recovery ³	11.3	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (for 5s)	
	Weight	3.7 (Typical)	

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.

² $V_{DD} = 50V$, starting $T_J = 25^\circ C$, $L = 0.36mH$, Peak $I_L = 20A$, $V_{GS} = 12V$

³ $I_{SD} \leq 20A$, $di/dt \leq 690A/\mu s$, $V_{DD} \leq 130V$, $T_J \leq 150^\circ C$

Device Characteristics

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ $T_j = 25^\circ\text{C}$ (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	130	—	—	V	$V_{GS} = 0V, I_D = 1.0mA$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.09	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1.0mA$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	82	m Ω	$V_{GS} = 12V, I_{D2} = 12.5A^1$
$V_{GS(th)}$	Gate Threshold Voltage	2.5	—	4.5	V	$V_{DS} = V_{GS}, I_D = 1mA$
Gfs	Forward Transconductance	5.0	—	—	S	$V_{DS} = 15V, I_{D2} = 12.5A^1$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	10	μA	$V_{DS} = 104V, V_{GS} = 0V$
		—	—	25		$V_{DS} = 104V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Leakage Reverse	—	—	-100		$V_{GS} = -20V$
Q_G	Total Gate Charge	—	—	48	nC	$I_{D1} = 20A$
Q_{GS}	Gate-to-Source Charge	—	—	16		$V_{DS} = 65V$
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	18		$V_{GS} = 12V$
$t_{d(on)}$	Turn-On Delay Time	—	—	20	ns	$I_{D1} = 20A^{**}$
t_r	Rise Time	—	—	100		$V_{DD} = 65V$
$t_{d(off)}$	Turn-Off Delay Time	—	—	35		$R_G = 7.5\Omega$
t_f	Fall Time	—	—	40		$V_{GS} = 12V$
$L_s + L_D$	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm/ 0.25 in from package) with Source wire internally bonded from Source pin to Drain pad
C_{iss}	Input Capacitance	—	1020	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	285	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	10	—		$f = 1.0MHz$
R_G	Internal Gate Resistance	—	0.77	—	Ω	$f = 1.0MHz, \text{open drain}$

** Switching speed maximum limits are based on manufacturing test equipment and capability.

¹ Pulse width $\leq 300 \mu\text{s}$; Duty Cycle $\leq 2\%$

Device Characteristics

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	20	A	
I_{SM}	Pulsed Source Current (Body Diode) ¹	—	—	80	A	
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}$, $I_S = 20\text{A}$, $V_{GS} = 0\text{V}$ ²
t_{rr}	Reverse Recovery Time	—	—	200	ns	$T_J = 25^\circ\text{C}$, $I_F = 20\text{A}$, $V_{DD} \leq 25\text{V}$ $di/dt = 100\text{A}/\mu\text{s}$ ²
Q_{rr}	Reverse Recovery Charge	—	1.0	—	μC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	1.67	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to- Ambient (Typical socket mount)	—	—	80	

2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics — Post Total Dose Irradiation

Table 6 Electrical Characteristics @ $T_J = 25^\circ\text{C}$, Post Total Dose Irradiation^{3, 4}

Symbol	Parameter	100 krad (Si)		Unit	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	130	—	V	$V_{GS} = 0\text{V}$, $I_D = 1.0\text{mA}$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.5	V	$V_{DS} = V_{GS}$, $I_D = 1.0\text{mA}$
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Leakage Reverse	—	-100		$V_{GS} = -20\text{V}$
I_{DSS}	Zero Gate Voltage Drain Current	—	10	μA	$V_{DS} = 104\text{V}$, $V_{GS} = 0\text{V}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) ²	—	82	$\text{m}\Omega$	$V_{GS} = 12\text{V}$, $I_{D2} = 12.5\text{A}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-257AA) ²	—	82	$\text{m}\Omega$	$V_{GS} = 12\text{V}$, $I_{D2} = 12.5\text{A}$
V_{SD}	Diode Forward Voltage	—	1.2	V	$V_{GS} = 0\text{V}$, $I_F = 20\text{A}$

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.

² Pulse width $\leq 300 \mu\text{s}$; Duty Cycle $\leq 2\%$

³ Total Dose Irradiation with V_{GS} Bias. $V_{GS} = 12\text{V}$ applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

⁴ Total Dose Irradiation with V_{DS} Bias. $V_{DS} = 104\text{V}$ applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

Device Characteristics

2.4.2 Single Event Effects — Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Typical Single Event Effects Safe Operating Area

Ion	LET (MeV·cm ² /mg)	Energy (MeV)	Range (μm)	V _{DS} (V)				
				V _{GS} = 0V	V _{GS} = -5V	V _{GS} = -10V	V _{GS} = -15V	V _{GS} = -20V
Br	36.7	309	39.5	130	130	130	130	130
I	59.8	341	32.5	130	130	130	100	50
Au	82.3	350	28.4	130	120	30	—	—

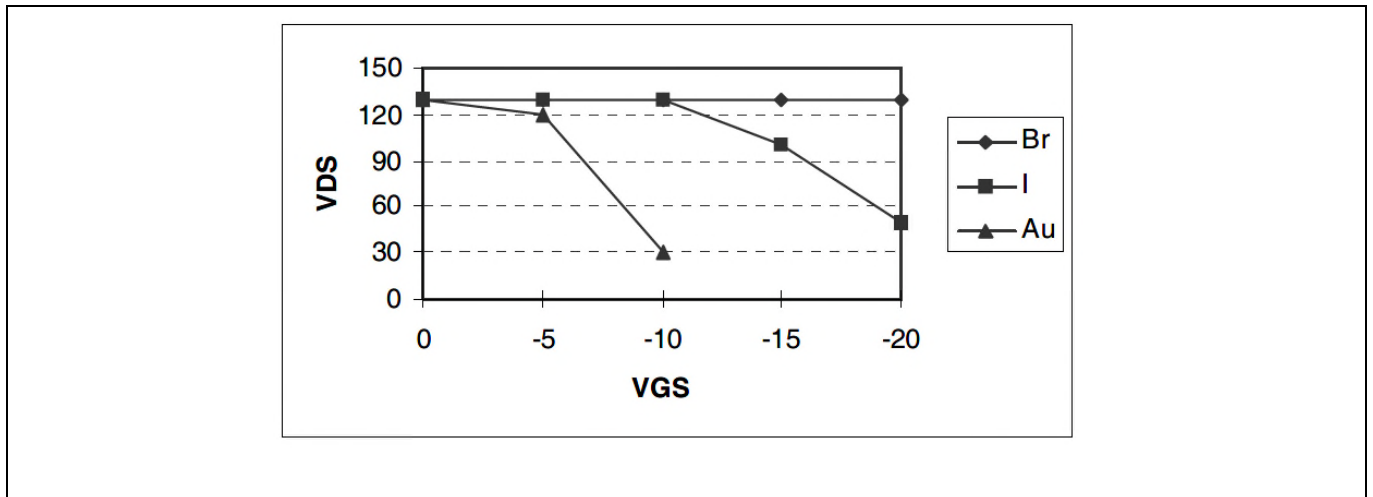


Figure 1 Typical Single Event Effect, Safe Operating Area

3 Electrical Characteristics Curves (Pre-irradiation)

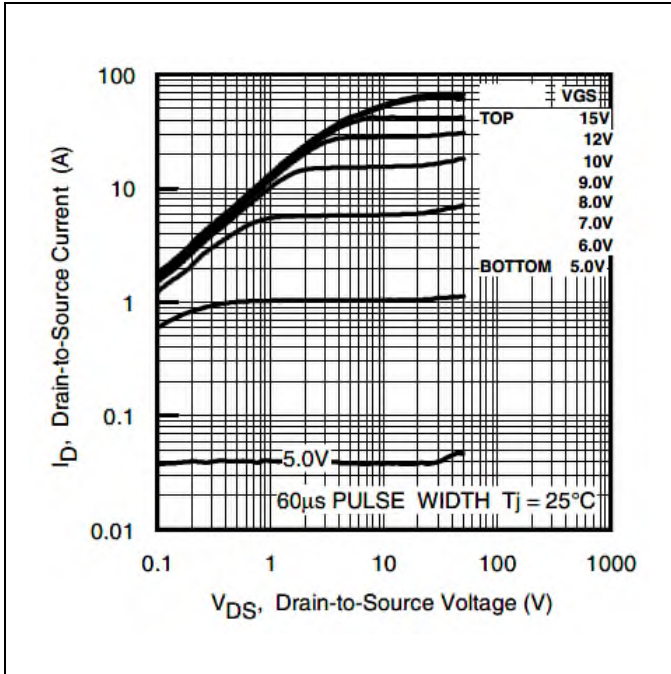


Figure 2 Typical Output Characteristics

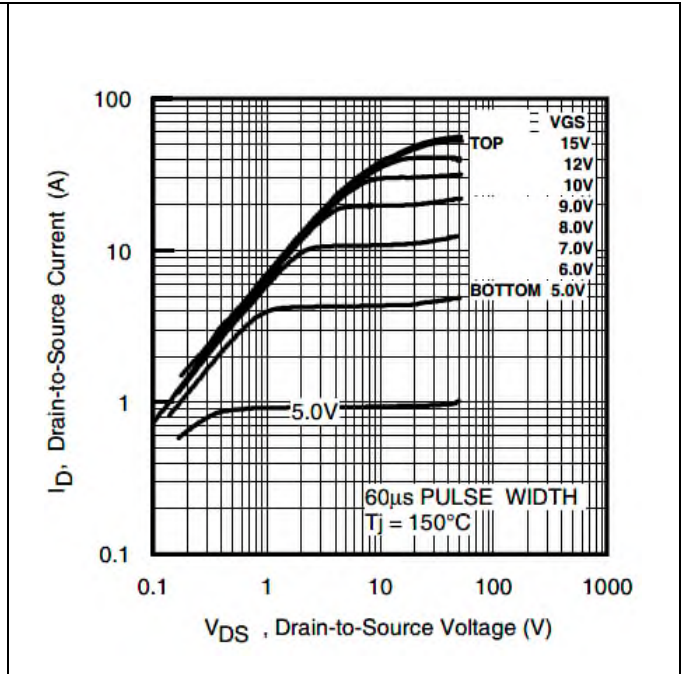


Figure 3 Typical Output Characteristics

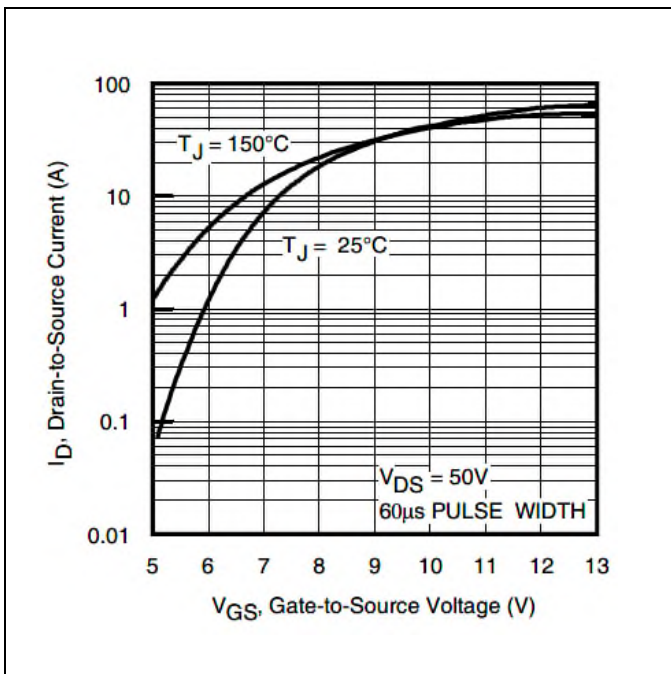


Figure 4 Typical Transfer Characteristics

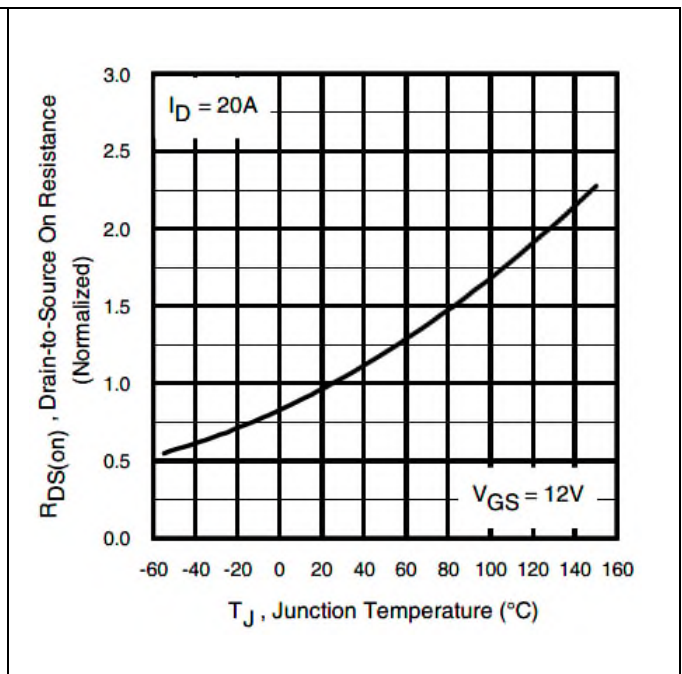


Figure 5 Normalized On-Resistance Vs. Temperature

Radiation Hardened Power MOSFET Surface Mount (Low-Ohmic TO-257AA)

Electrical Characteristics Curves (Pre-irradiation)

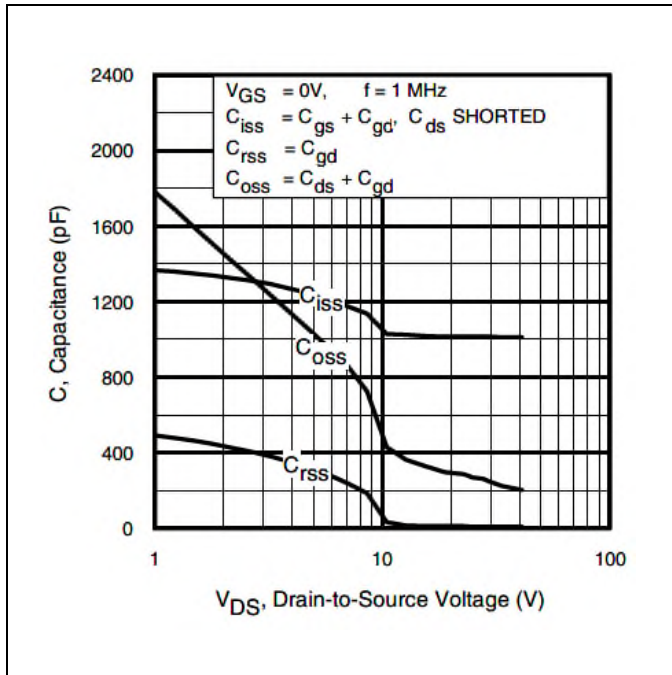


Figure 6 Typical Capacitance Vs. Drain-to-Source Voltage

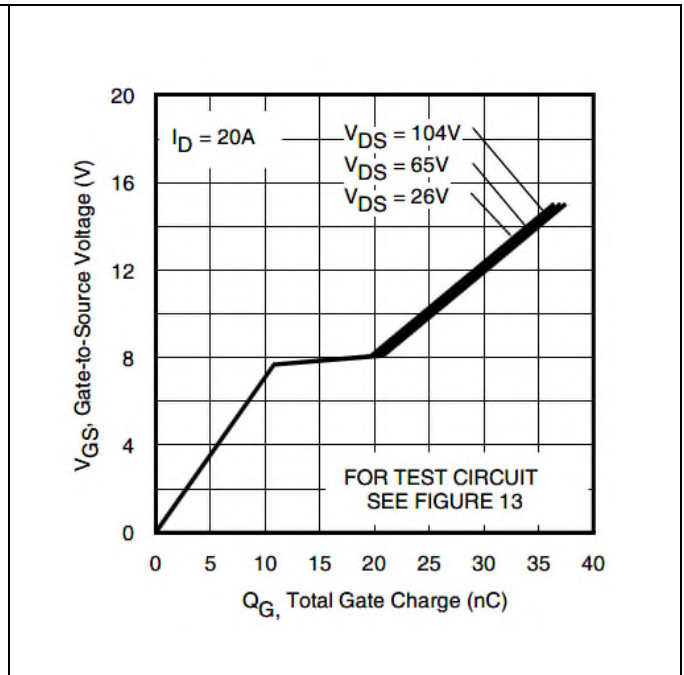


Figure 7 Typical Gate-to-Source Voltage Vs. Typical Gate Charge

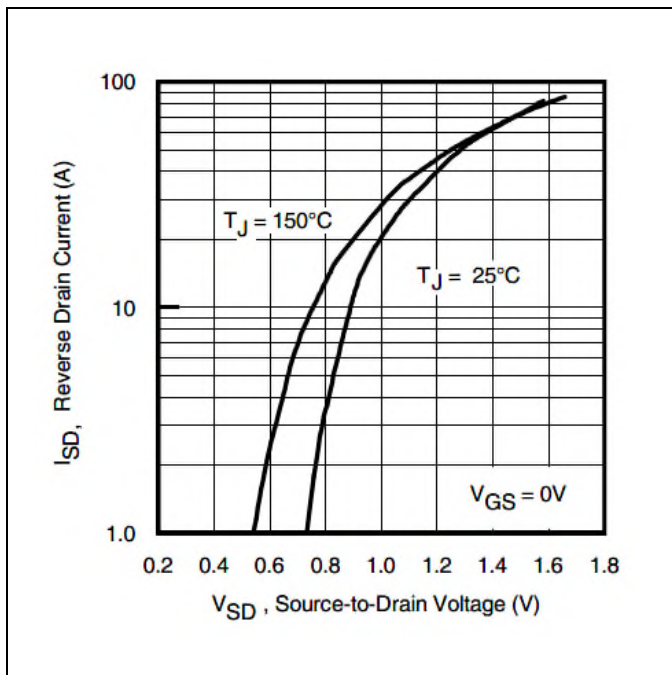


Figure 8 Typical Source-Drain Current Vs. Diode Forward Voltage

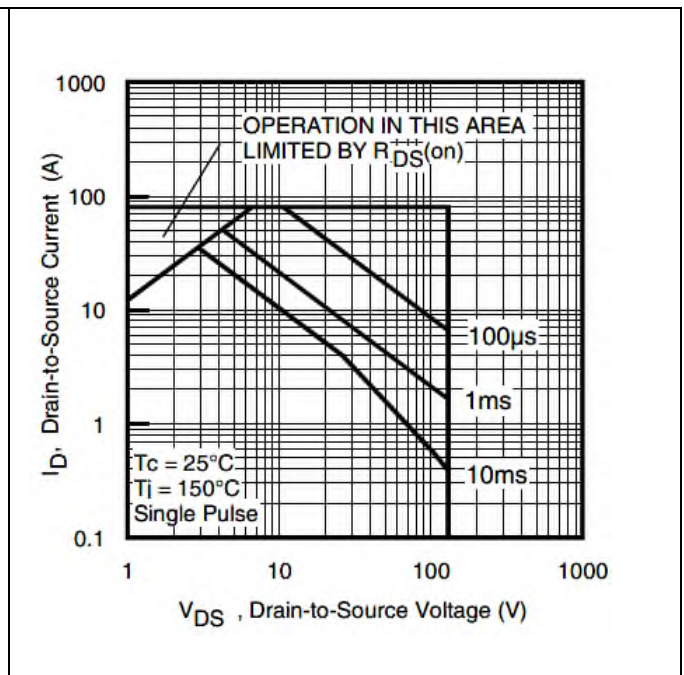


Figure 9 Maximum Safe Operating Area

IRHYK57133CMSE

Radiation Hardened Power MOSFET Surface Mount (Low-Ohmic TO-257AA)

Electrical Characteristics Curves (Pre-irradiation)

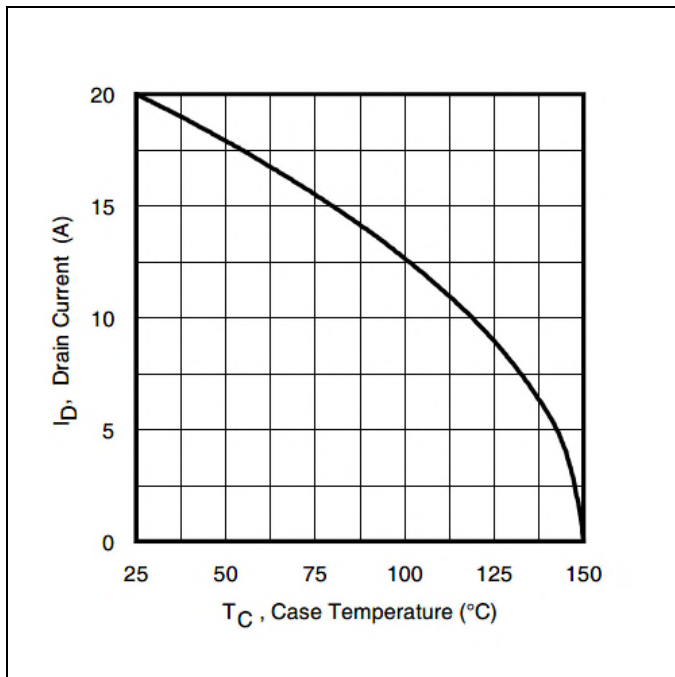


Figure 10 Maximum Drain Current Vs. Case Temperature

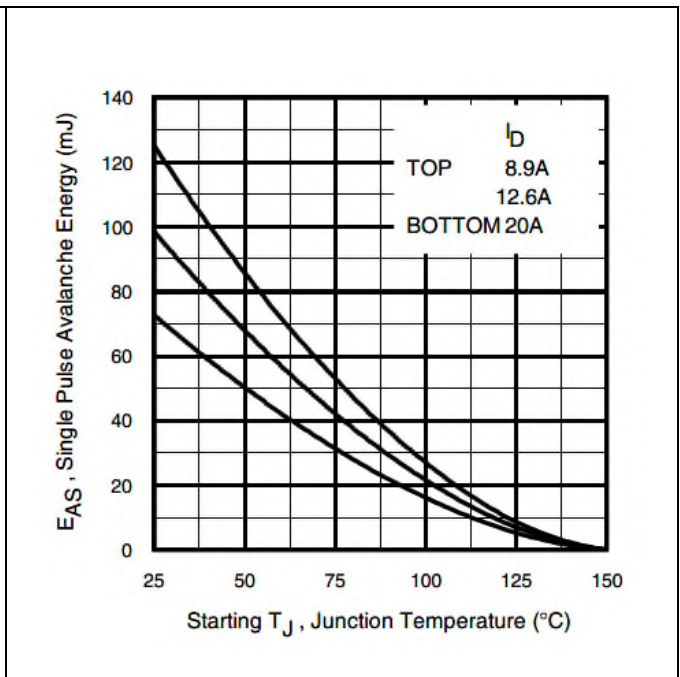


Figure 11 Maximum Avalanche Energy Vs. Junction Temperature

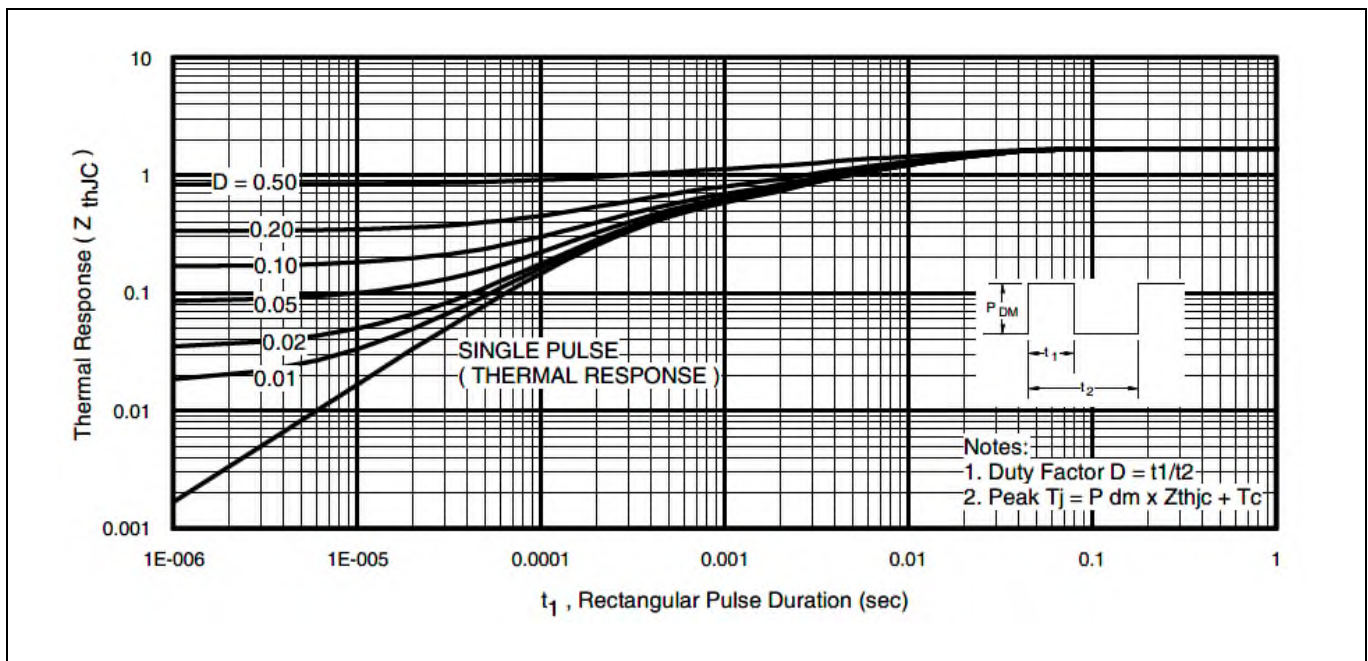


Figure 12 Maximum Effective Transient Thermal Impedance, Junction-to-Case

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Radiation Hardened Power MOSFET Surface Mount (Low-Ohmic TO-257AA)

Test Circuits (Pre-irradiation)

4 Test Circuits (Pre-irradiation)

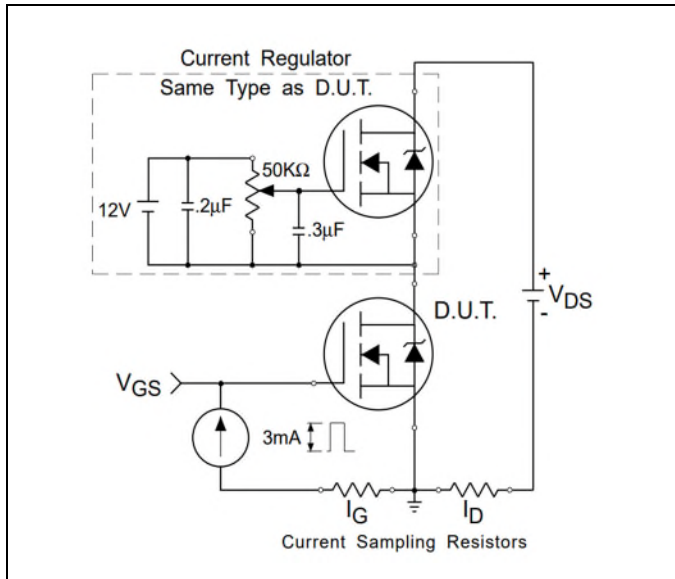


Figure 13 Gate Charge Test Circuit

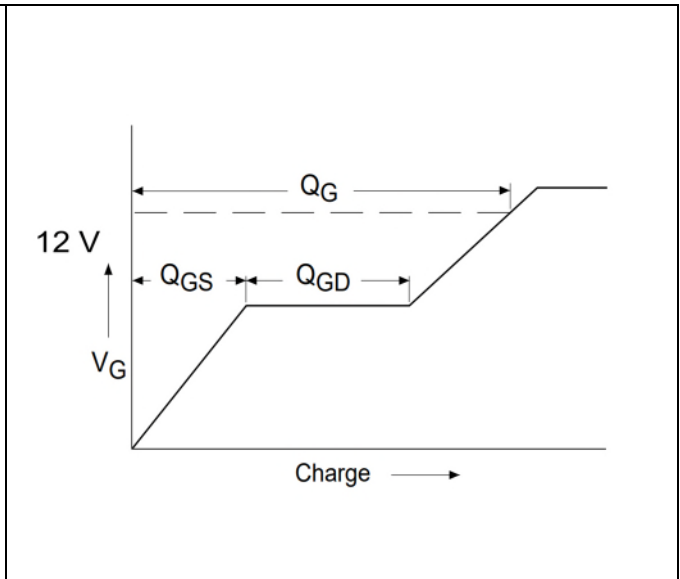


Figure 14 Gate Charge Waveform

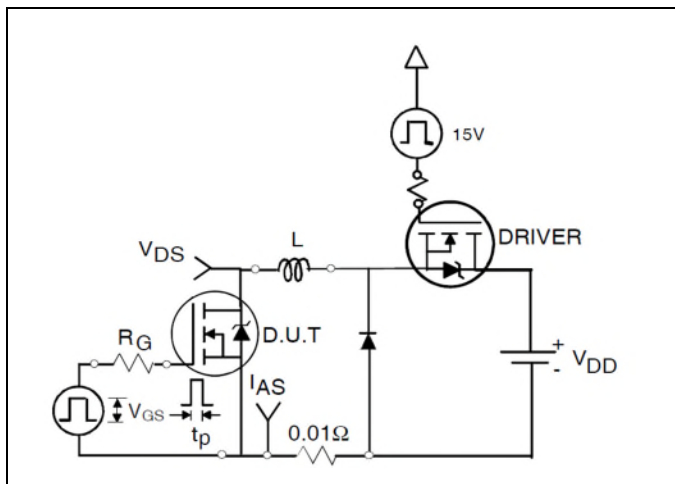


Figure 15 Unclamped Inductive Test Circuit

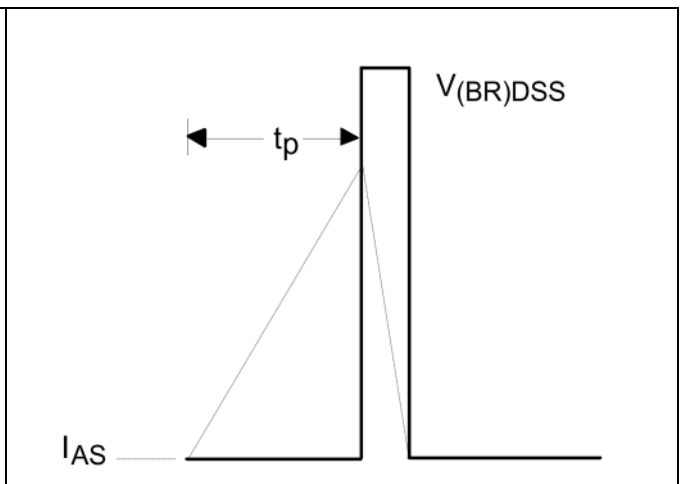


Figure 16 Unclamped Inductive Waveform

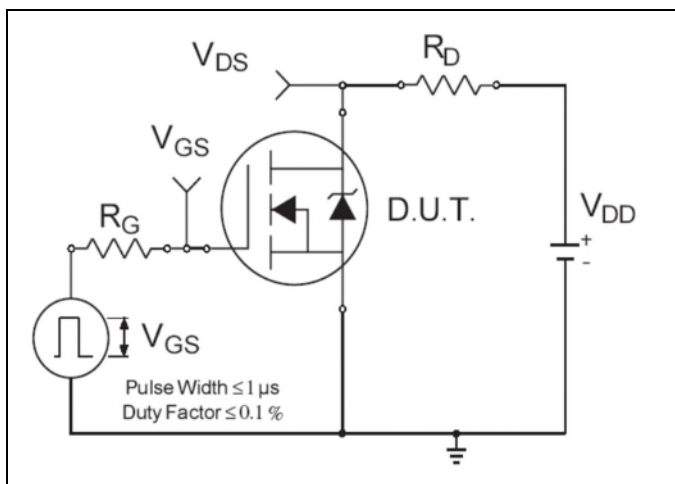


Figure 17 Switching Time Test Circuit

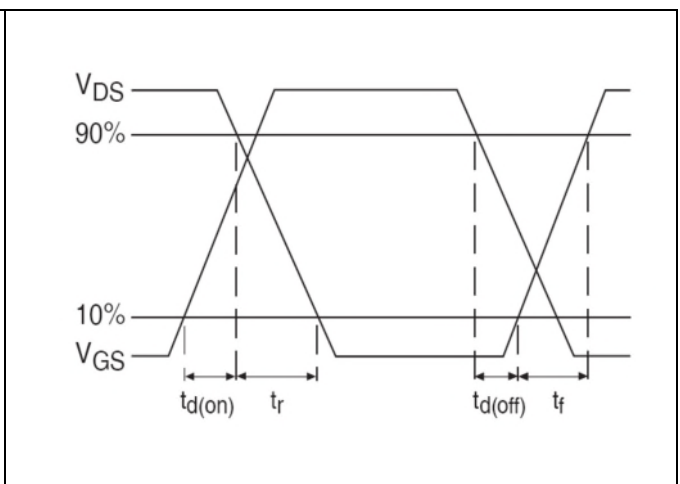
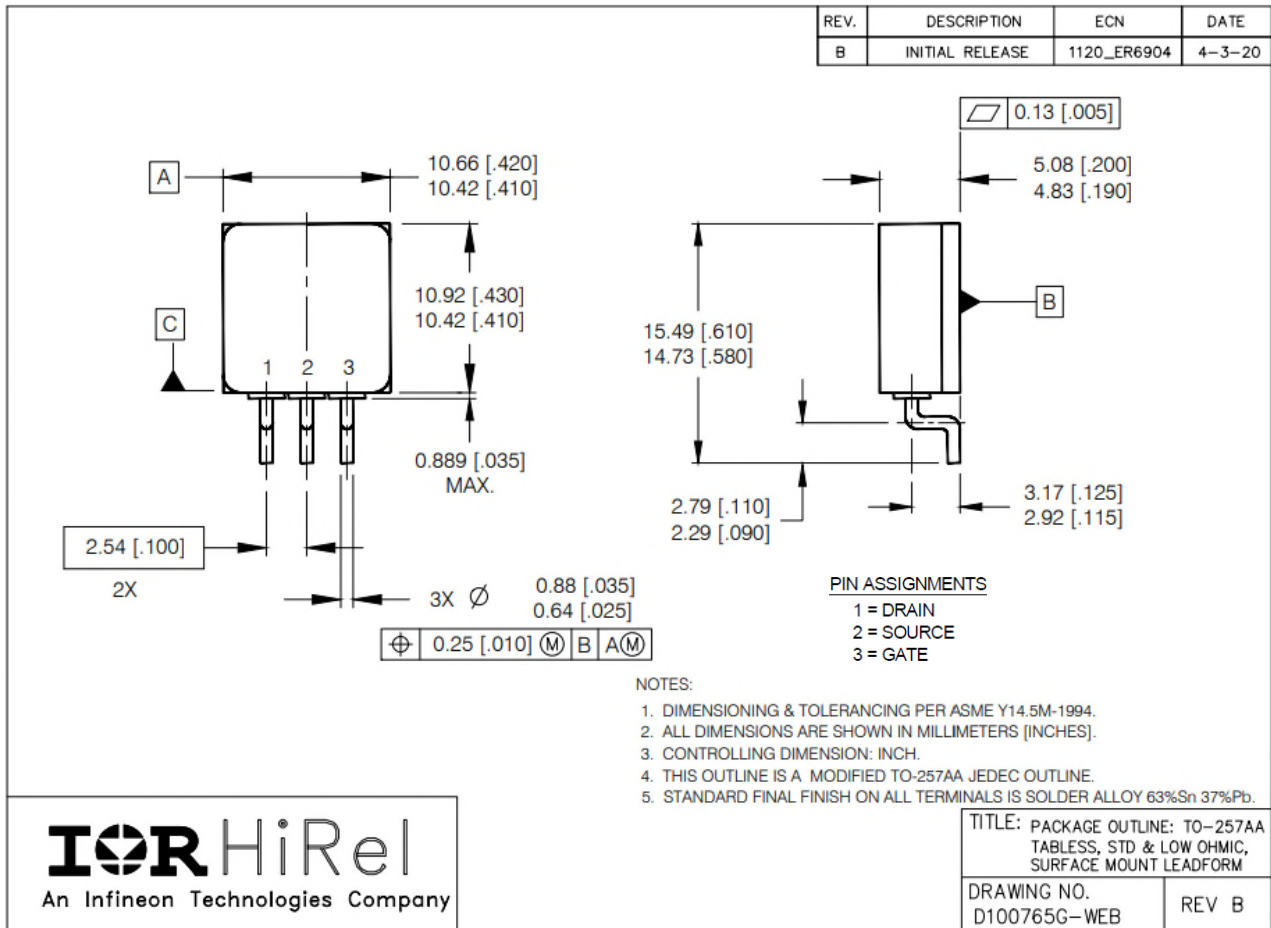


Figure 18 Switching Time Waveforms

Package Outline

5 Package Outline

Note: For the most updated package outline, please see the website: [Low-Ohmic TO-257AA](#)



Revision history

Revision history

Document version	Date of release	Description of changes
	10/28/2024	Datasheet (PD-96898)
Rev A	02/10/2023	Updated based on ECN-1120_09415

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