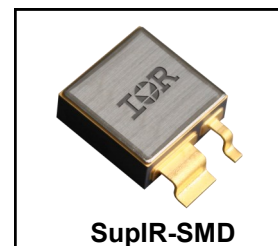


RADIATION HARDENED POWER MOSFET SURFACE MOUNT (SupIR-SMD)

100V, N-CHANNEL
REF: MIL-PRF-19500/760
R6 TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	I _D	QPL Part Number
IRHNS67160	100 kRads(Si)	0.010Ω	56A*	JANSR2N7579U2A
IRHNS63160	300 kRads(Si)	0.010Ω	56A*	JANSF2N7579U2A



Description

IR HiRel R6 technology provides high performance power MOSFETs for space applications. These devices have been characterized for both Total Dose and Single Event Effect (SEE) with useful performance up to LET of 90 (MeV/(mg/cm²)). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC-DC converters and motor controllers. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, and temperature stability of electrical parameters.

Features

- Single Event Effect (SEE) Hardened
- Low RDS(on)
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Ceramic Package
- Light Weight
- Surface Mount
- ESD Rating: Class 3A per MIL-STD-750, Method 1020

Absolute Maximum Ratings

Pre-Irradiation

Symbol	Parameter	Value	Units
I _{D1} @ V _{GS} = 12V, T _C = 25°C	Continuous Drain Current	56*	A
I _{D2} @ V _{GS} = 12V, T _C = 100°C	Continuous Drain Current	56*	
I _{DM} @ T _C = 25°C	Pulsed Drain Current ①	224	
P _D @ T _C = 25°C	Maximum Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
V _{GS}	Gate-to-Source Voltage	±20	V
E _{AS}	Single Pulse Avalanche Energy ②	462	mJ
I _{AR}	Avalanche Current ①	56	A
E _{AR}	Repetitive Avalanche Energy ①	25	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (for 5s)	
	Weight	3.3 (Typical)	

* Current is limited by package

For Footnotes, refer to the page 2.

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.010	Ω	V _{GS} = 12V, I _{D2} = 56A* ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 1.0mA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	—	-10.12	—	mV/°C	
g _{fs}	Forward Transconductance	60	—	—	S	V _{DS} = 15V, I _{D2} = 56A* ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	10	μA	V _{DS} = 80V, V _{GS} = 0V
		—	—	25		V _{DS} = 80V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _G	Total Gate Charge	—	—	170	nC	I _{D1} = 56A*
Q _{GS}	Gate-to-Source Charge	—	—	60		V _{DS} = 50V
Q _{GD}	Gate-to-Drain ('Miller') Charge	—	—	80		V _{GS} = 12V
t _{d(on)}	Turn-On Delay Time	—	—	50	ns	V _{DD} = 50V
t _r	Rise Time	—	—	150		I _{D1} = 56A*
t _{d(off)}	Turn-Off Delay Time	—	—	100		R _G = 2.35Ω
t _f	Fall Time	—	—	50		V _{GS} = 12V
L _S + L _D	Total Inductance	—	2.8	—	nH	Measured from center of Drain pad to center of Source pad
C _{iss}	Input Capacitance	—	8690	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	1600	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	20	—		f = 1.0MHz
R _G	Gate Resistance	—	0.45	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	56*	A	
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	224		
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _J = 25°C, I _S = 56A*, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	500	ns	T _J = 25°C, I _F = 56A*, V _{DD} ≤ 25V
Q _{rr}	Reverse Recovery Charge	—	—	5.5	μC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S + L _D)				

* Current is limited by package

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	—	0.5	°C/W
R _{θJ-PCB}	Junction-to-PC Board (Soldered to 2" sq copper clad board)	—	1.6	—	

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V_{DD} = 25V, starting T_J = 25°C, L = 0.29mH, Peak I_L = 56A, V_{GS} = 12V
- ③ I_{SD} ≤ 56A, di/dt ≤ 640A/μs, V_{DD} ≤ 100V, T_J ≤ 150°C
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%
- ⑤ Total Dose Irradiation with V_{GS} Bias. 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- ⑥ Total Dose Irradiation with V_{DS} Bias. 80 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

Symbol	Parameter	Up to 300 kRads (Si) ¹		Units	Test Conditions
		Min.	Max.		
BV _{DSS}	Drain-to-Source Breakdown Voltage	100	—	V	V _{GS} = 0V, I _D = 1.0mA
V _{GS(th)}	Gate Threshold Voltage	2.0	4.0	V	V _{DS} = V _{GS} , I _D = 1.0mA
I _{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	-100	nA	V _{GS} = -20V
I _{DSS}	Zero Gate Voltage Drain Current	—	10	μA	V _{DS} = 80V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.011	Ω	V _{GS} = 12V, I _{D2} = 56A *
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (SupIR-SMD)	—	0.010	Ω	V _{GS} = 12V, I _{D2} = 56A*
V _{SD}	Diode Forward Voltage ④	—	1.3	V	V _{GS} = 0V, I _S = 56A*

1. Part numbers IRHNS67160 (JANSR2N7579U2A) and IRHNS63160 (JANSF2N7579U2A)

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	VDS (V)					
			@ VGS = 0V	@ VGS = -5V	@ VGS = -10V	@ VGS = -15V	@ VGS = -19V	@ VGS = -20V
39 ± 5%	315 ± 7.5%	40 ± 7.5%	100	100	100	100	100	40
61 ± 5%	345 ± 7.5%	32 ± 7.5%	100	100	100	30	—	—
90 ± 5%	375 ± 7.5%	29 ± 7.5%	100	100	—	—	—	—

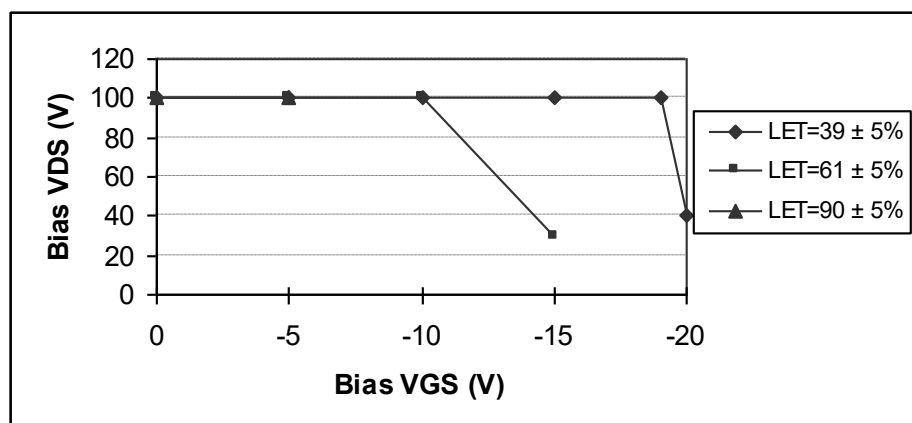


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

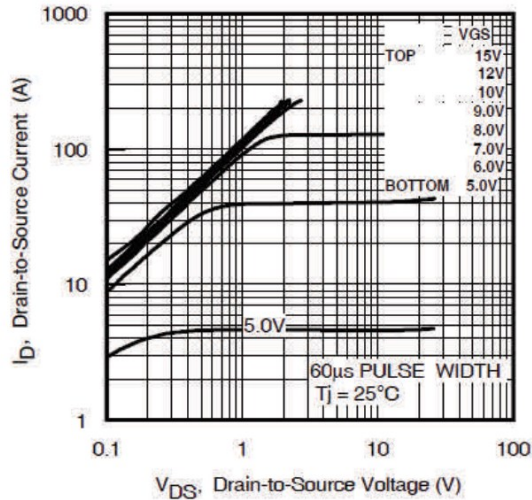


Fig 1. Typical Output Characteristics

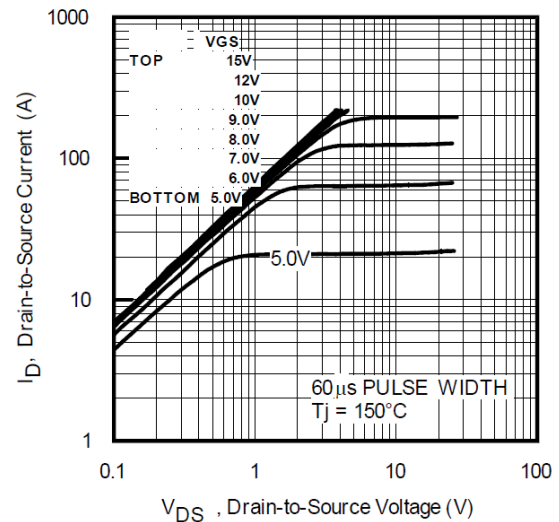


Fig 2. Typical Output Characteristics

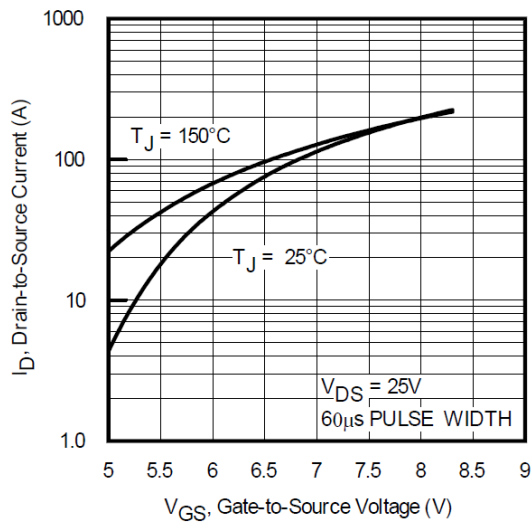


Fig 3. Typical Transfer Characteristics

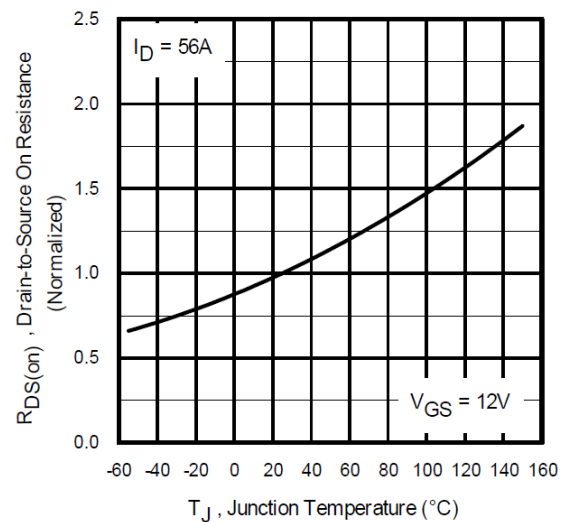


Fig 4. Normalized On-Resistance Vs. Temperature

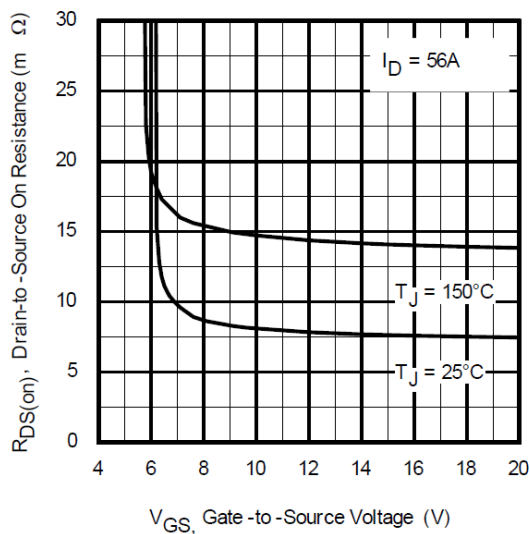


Fig 5. Typical On-Resistance Vs Gate Voltage

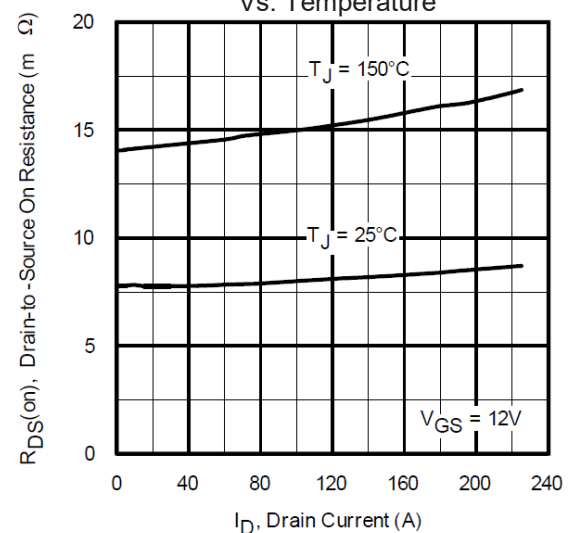


Fig 6. Typical On-Resistance Vs Drain Current

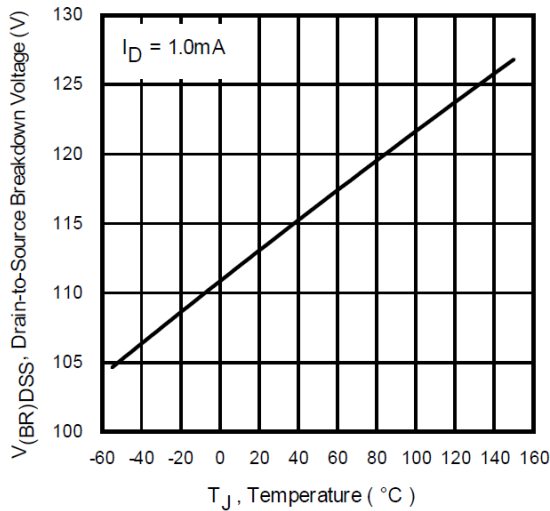


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

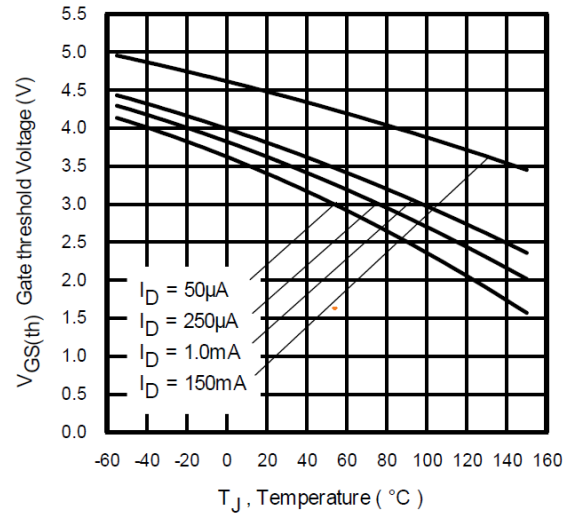


Fig 8. Typical Threshold Voltage Vs Temperature

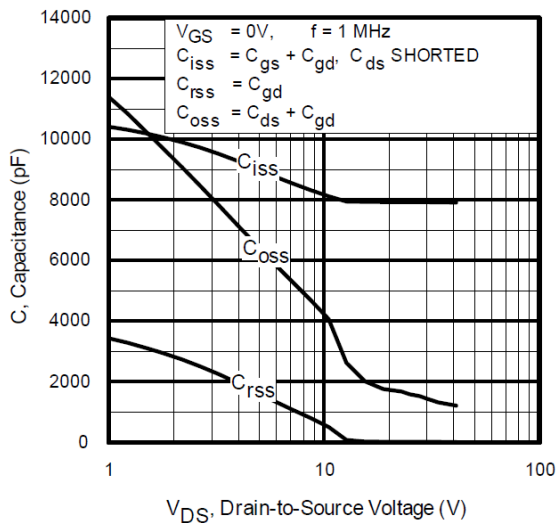


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

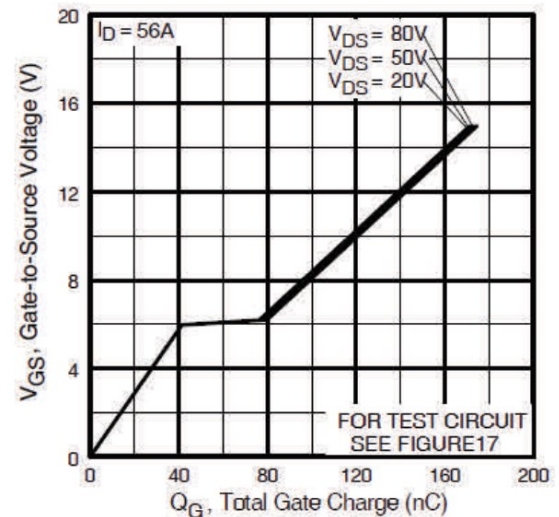


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

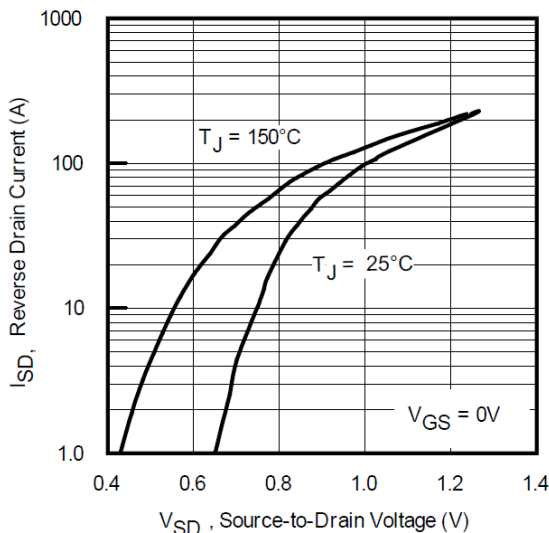


Fig 11. Typical Source-Drain Diode Forward Voltage

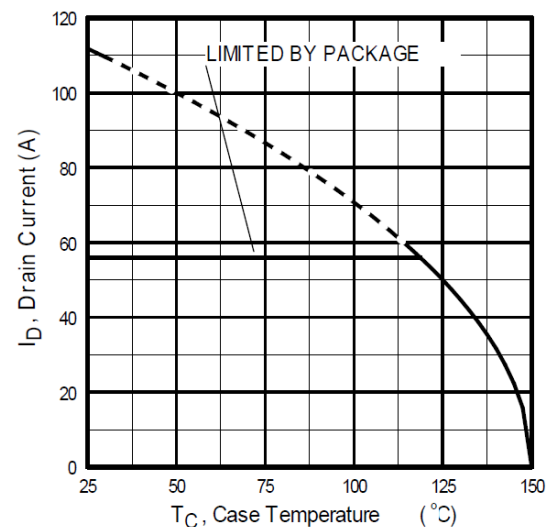


Fig 12. Maximum Drain Current Vs. Case Temperature

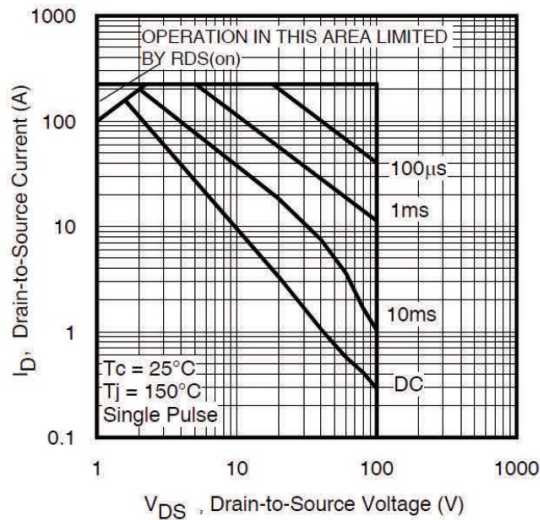


Fig 13. Maximum Safe Operating Area

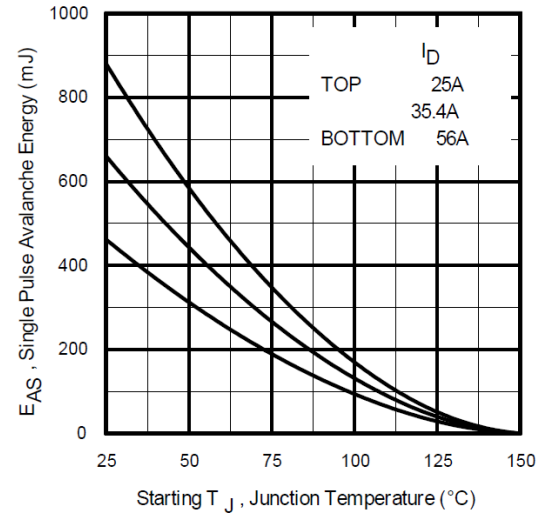


Fig 14. Maximum Avalanche Energy Vs. Drain Current

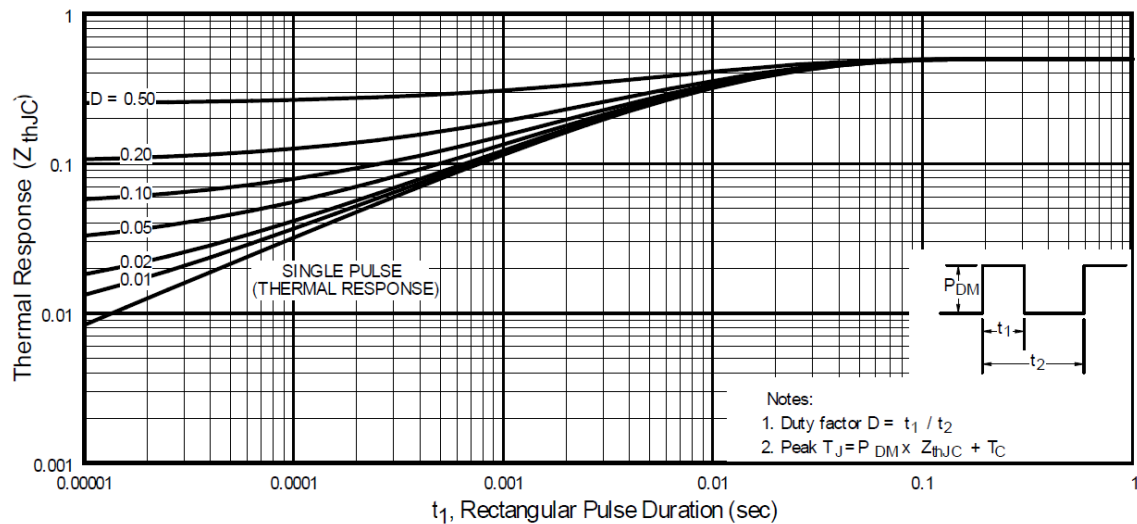


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

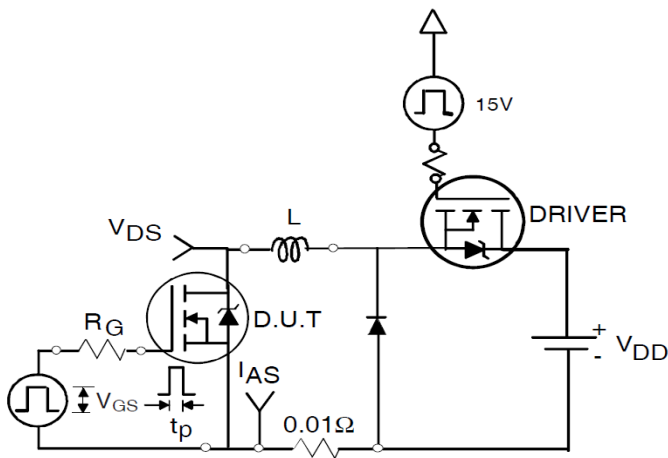


Fig 16a. Unclamped Inductive Test Circuit

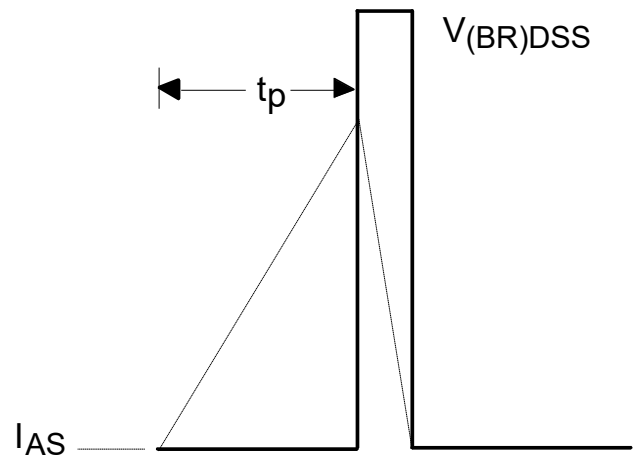


Fig 16b. Unclamped Inductive Wave-

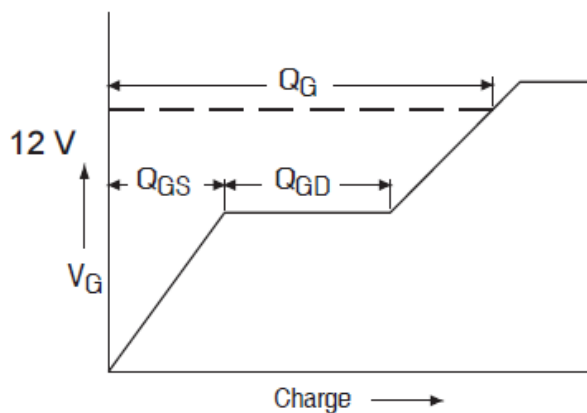


Fig 17a. Gate Charge Waveform

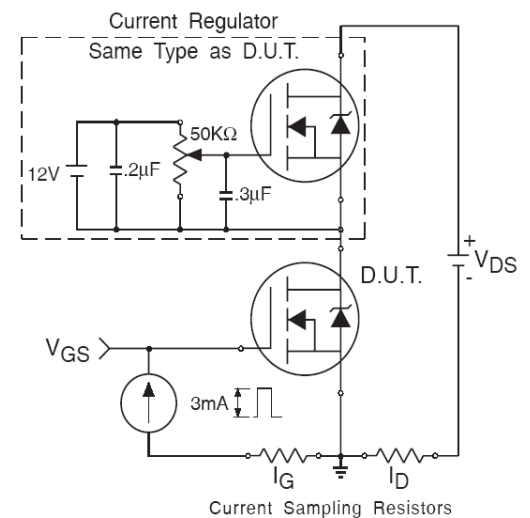


Fig 17b. Gate Charge Test Circuit

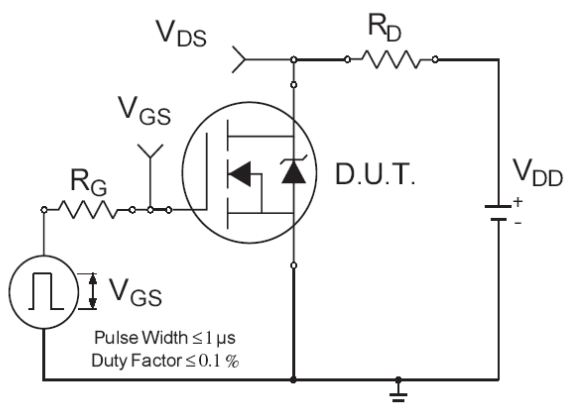


Fig 18a. Switching Time Test Circuit

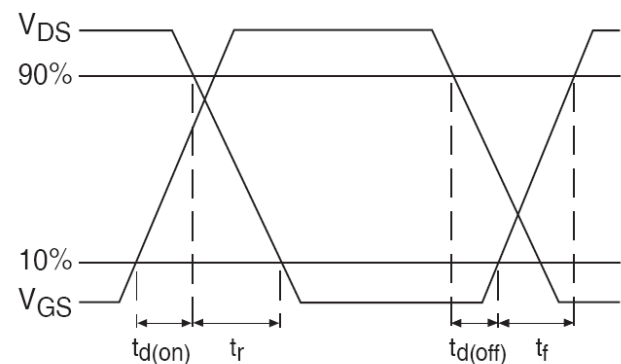
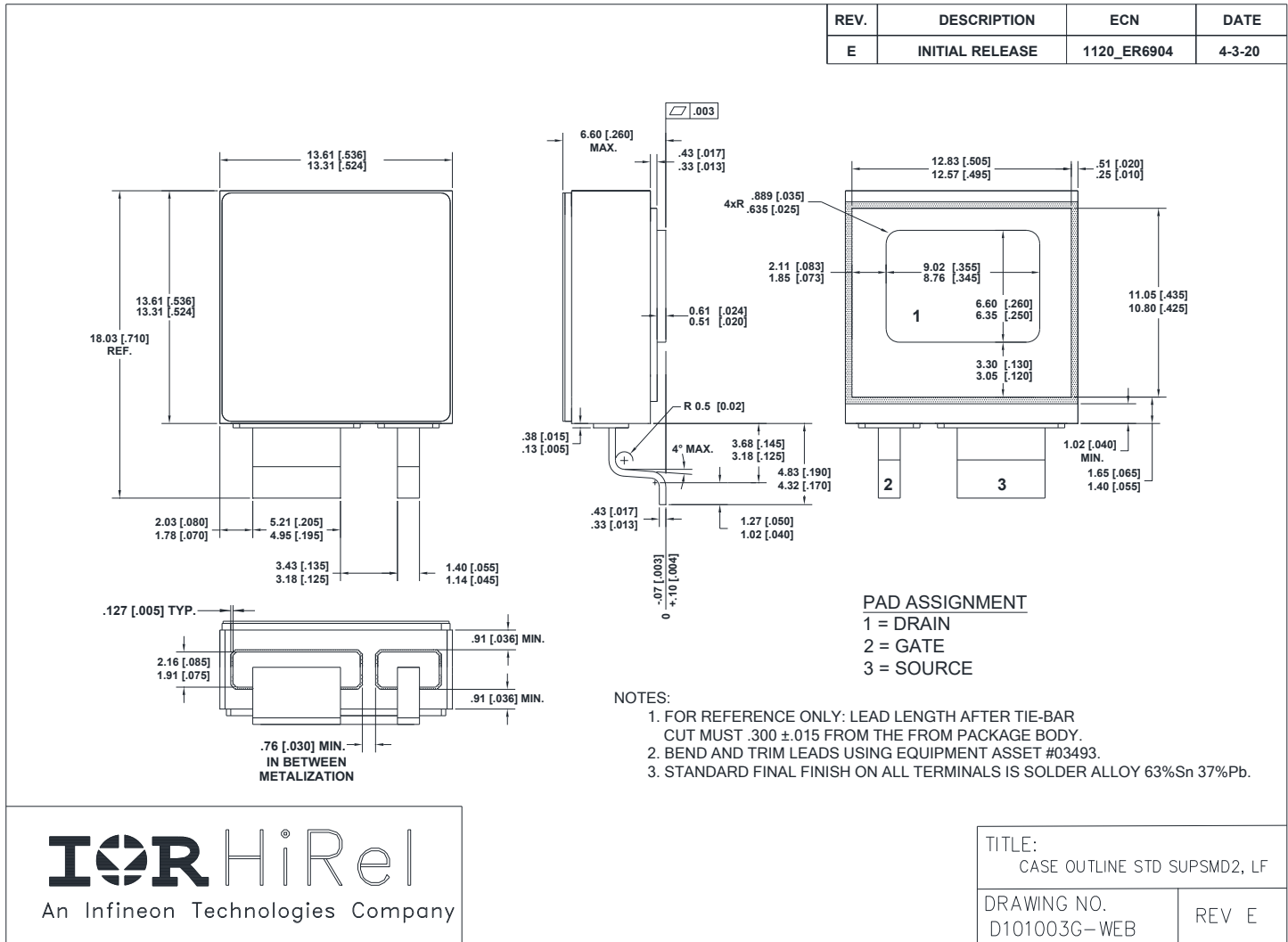


Fig 18b. Switching Time Waveforms

Note: For the most updated package outline, please see the website: [SupIR-SMD](http://www.infineon.com/supir-smd)

Case Outline and Dimensions - SupIR-SMD



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