IR HiRel
An Infineon Technologies Company

IRHNM57214SE, IRHNMC57214SE

PD-97818D

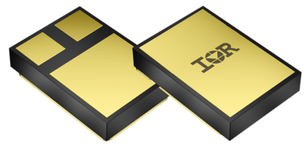
Radiation Hardened Power MOSFET
Surface Mount (SMD-0.2)
250V, 3.7A, N-channel, R5 Technology

Features

- Single event effect (SEE) hardened
- Low $R_{DS(on)}$
- Low total gate charge
- Simple drive requirements
- Low total gate charge
- Hermetically sealed
- Surface mount
- Ceramic package
- Light weight
- ESD rating: Class 1B per MIL-STD-750, Method 1020

Product Summary

- **BV_{DSS}**: 250V
- **I_D**: 3.7A
- **$R_{DS(on), max}$**: 1.7Ω
- **$Q_{G, max}$**: 9.1nC



SMD-0.2

Potential Applications

- DC-DC converter
- Motor drives

Product Validation

Qualified to IR HiRel's S-level screening flow which is equivalent to MIL-PRF-19500

Description

IR HiRel R5 technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80MeV·cm^2/mg. The combination of low $R_{DS(on)}$ and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well-established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parametersswitching and temperature stability of electrical parameters.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHNM57214SE	SMD-0.2	COTS	100 krad(Si)
IRHNM57214SESCS	SMD-0.2	S-level	100 krad(Si)
IRHNMC57214SE	SMD-0.2 ceramic lid	COTS	100 krad(Si)
IRHNMC57214SESCS	SMD-0.2 ceramic lid	S-level	100 krad(Si)

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1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
I_{D1} @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	3.7	A
I_{D2} @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	2.4	A
I_{DM} @ T_C = 25°C	Pulsed Drain Current [1]	14.8	A
P_D @ T_C = 25°C	Maximum Power Dissipation	40	W
	Linear Derating Factor	0.32	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy [2]	34	mJ
I_{AR}	Avalanche Current [1]	3.7	A
E_{AR}	Repetitive Avalanche Energy [1]	4.0	mJ
dv/dt	Peak Diode Reverse Recovery [3]	3.7	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (for 5s)	°C
	Weight	0.25 (Typical)	g

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.

[2] V_{DD} = 50V, starting T_J = 25°C, L = 5.0mH, Peak I_L = 3.7A, V_{GS} = 12V

[3] $I_{SD} \leq$ 3.7A, di/dt $\leq$ 1018A/µs, $V_{DD} \leq$ 250V, $T_J \leq$ 150°C

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	250	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.27	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	1.7	Ω	V_{GS} = 12V, I_{D2} = 2.4A [1]
$V_{GS(th)}$	Gate Threshold Voltage	2.5	—	4.5	V	V_{DS} = V_{GS}, I_D = 1.0mA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-9.1	—	mV/°C	
Gfs	Forward Transconductance	2.0	—	—	S	V_{DS} = 15V, I_{D2} = 2.4A [1]
I_{DSS}	Zero Gate Voltage Drain Current	—	—	10	µA	V_{DS} = 200V, V_{GS} = 0V
		—	—	25		V_{DS} = 200V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_G	Total Gate Charge	—	—	9.1	nC	I_{D1} = 3.7A V_{DS} = 125V V_{GS} = 12V
Q_{GS}	Gate-to-Source Charge	—	—	2.9		
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	4.3		
$t_{d(on)}$	Turn-On Delay Time	—	—	7.5	ns	I_{D1} = 3.7A ** V_{DD} = 125V R_G = 7.5Ω V_{GS} = 12V
t_r	Rise Time	—	—	6.6		
$t_{d(off)}$	Turn-Off Delay Time	—	—	16.8		
t_f	Fall Time	—	—	14		
$L_s + L_D$	Total Inductance	—	6.8	—	nH	Measured from center of Drain pad to center of Source pad
C_{iss}	Input Capacitance	—	308	—	pF	V_{GS} = 0V V_{DS} = 20V f = 1.0MHz
C_{oss}	Output Capacitance	—	51	—		
C_{rss}	Reverse Transfer Capacitance	—	1.2	—		
R_G	Gate Resistance	—	6.6	—	Ω	f = 1.0MHz, open drain

** Switching speed maximum limits are based on manufacturing test equipment and capability.

[1] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	3.7	A	
I_{SM}	Pulsed Source Current (Body Diode) [1]	—	—	14.8	A	
V_{SD}	Diode Forward Voltage	—	—	1.0	V	T_J = 25°C, I_S = 3.7A, V_{GS} = 0V [2]
t_{rr}	Reverse Recovery Time	—	—	145	ns	T_J = 25°C, I_F = 3.7A, V_{DD} ≤ 25V di/dt = 100A/µs [2]
Q_{rr}	Reverse Recovery Charge	—	—	857	nC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	3.12	°C/W

2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics — Post Total Dose Irradiation

Table 6 Electrical Characteristics @ T_J = 25°C, Post Total Dose Irradiation [3, 4]

Symbol	Parameter	Up to 100 krad (Si)		Unit	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	250	—	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.5	V	V_{DS} = V_{GS}, I_D = 1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	—	-100		V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	—	10	µA	V_{DS} = 200V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) [2]	—	1.7	Ω	V_{GS} = 12V, I_{D2} = 2.4A
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (SMD-0.2) [2]	—	1.7	Ω	V_{GS} = 12V, I_{D2} = 2.4A
V_{SD}	Diode Forward Voltage	—	1.0	V	V_{GS} = 0V, I_F = 3.7A

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.
[2] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%
[3] Total Dose Irradiation with V_{GS} Bias. V_{GS} = 12V applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
[4] Total Dose Irradiation with V_{DS} Bias. V_{DS} = 200V applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

2.4.2 Single Event Effects — Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Worst Case Single Event Effects Safe Operating Area

Ion	LET (MeV·cm²/mg)	Energy (MeV)	Range (µm)	V_{DS} (V)				
				V_{GS} = 0V	V_{GS} = -5V	V_{GS} = -10V	V_{GS} = -15V	V_{GS} = -20V
Br	36.7	309	39.5	250	250	250	250	250
I	59.8	341	32.5	250	250	250	250	240
Au	82.3	350	28.4	250	250	225	175	50

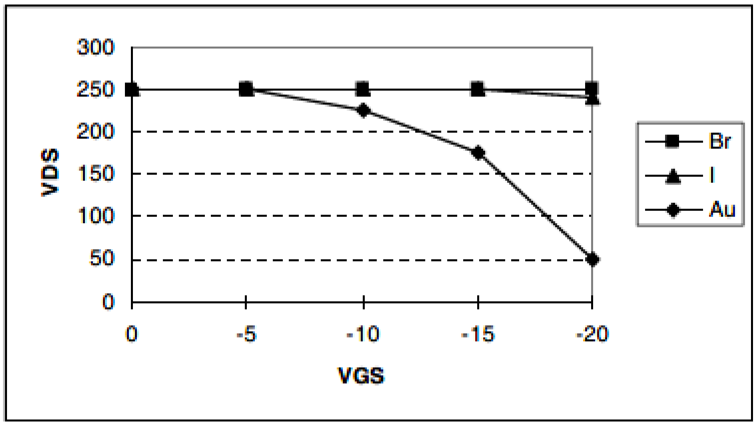


Figure 1 Worst Case Single Event Effect, Safe Operating Area

3 Electrical Characteristics Curves (Pre-irradiation)

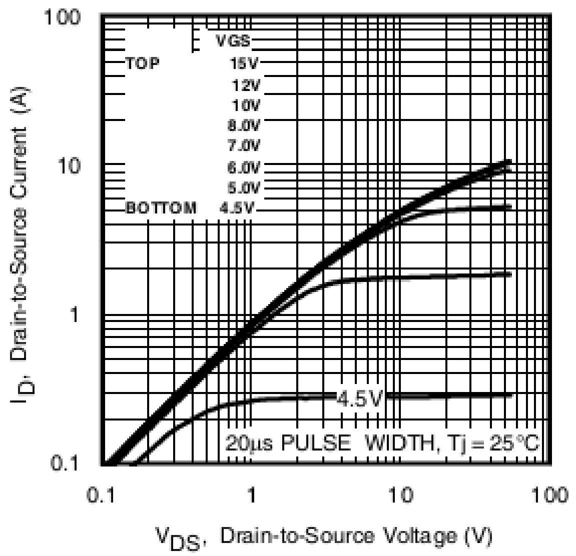


Figure 2 Typical Output Characteristics

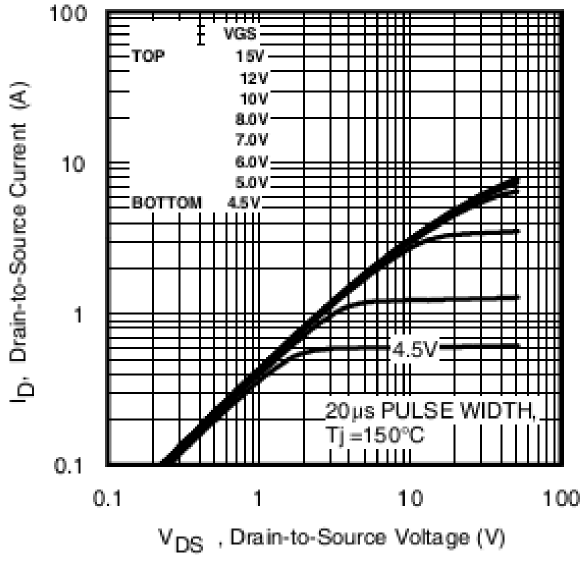


Figure 3 Typical Output Characteristics

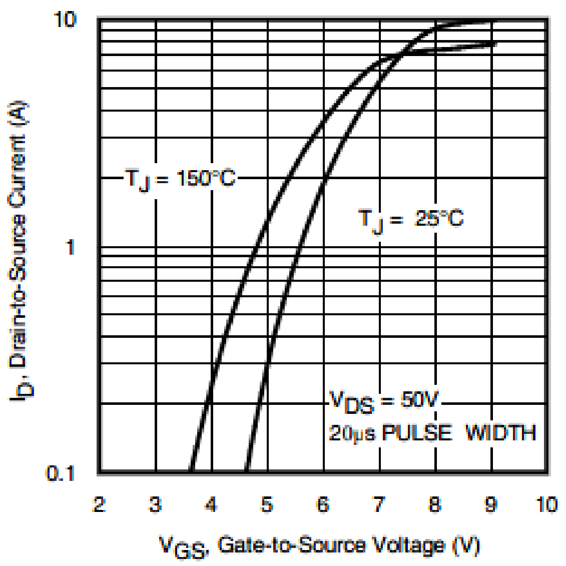


Figure 4 Typical Transfer Characteristics

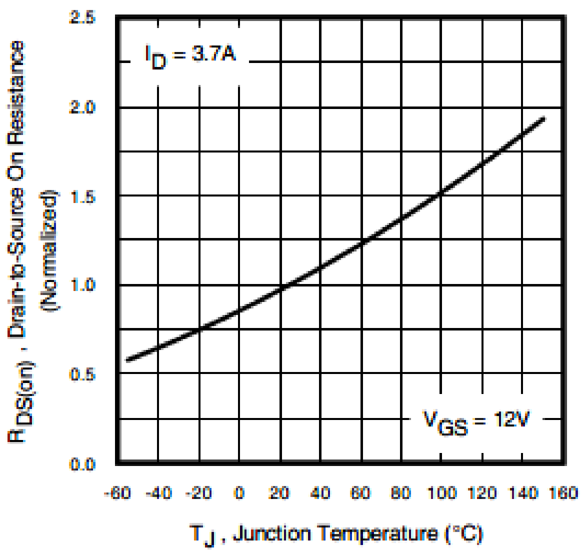


Figure 5 Normalized On-Resistance Vs. Temperature

Electrical Characteristics Curves (Pre-irradiation)

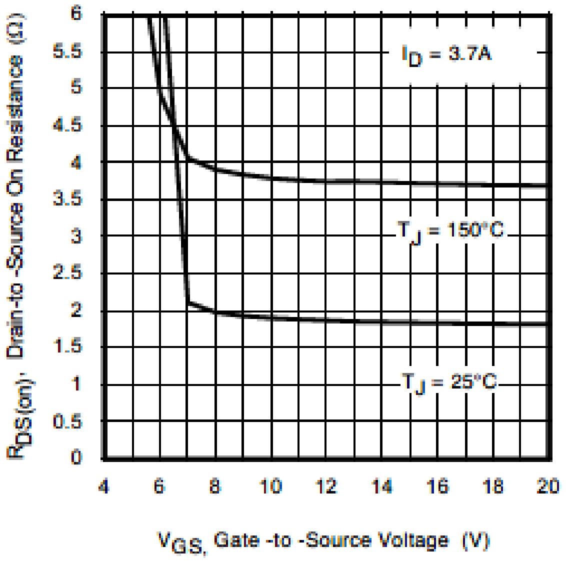


Figure 6 **Typical On-Resistance Vs. Gate Voltage**

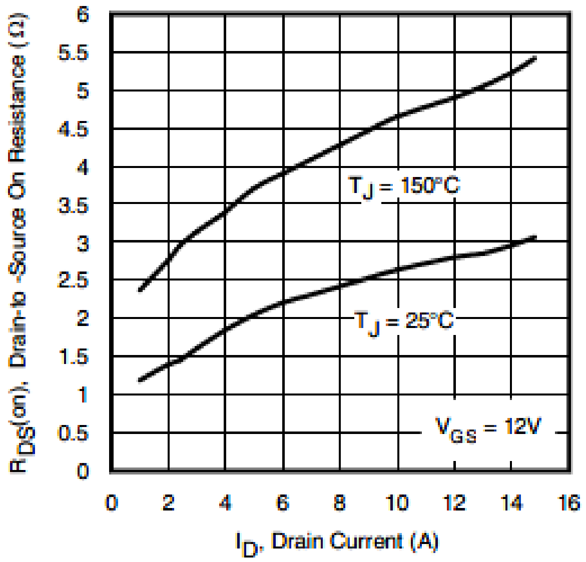


Figure 7 **Typical On-Resistance Vs. Drain Current**

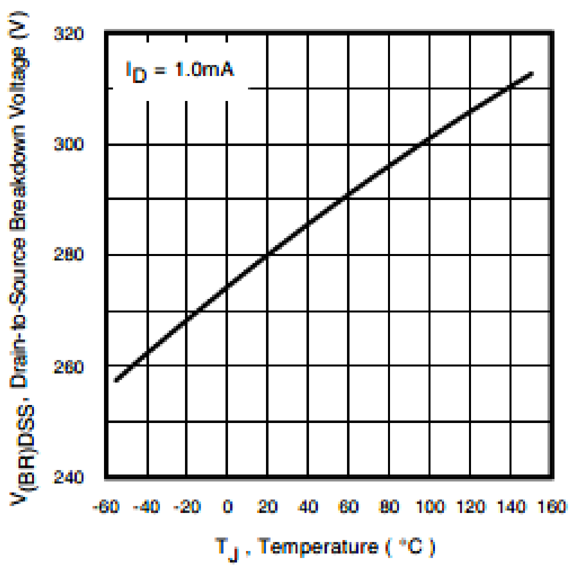


Figure 8 **Typical Drain-to-Source Breakdown Voltage Vs. Temperature**

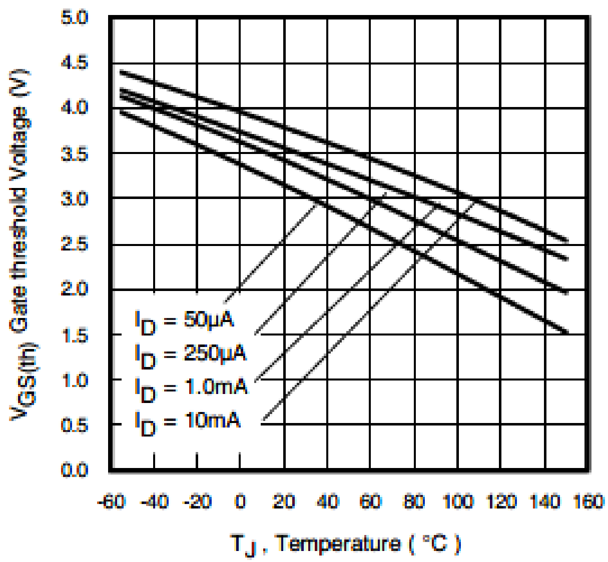


Figure 9 **Typical Threshold Voltage Vs. Temperature**

Electrical Characteristics Curves (Pre-irradiation)

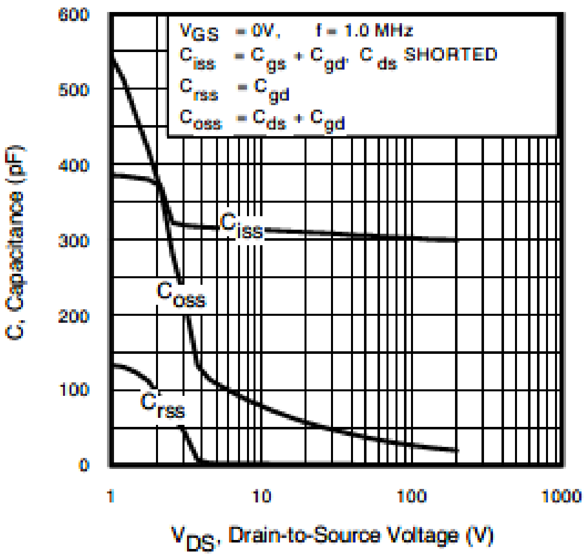


Figure 10 Typical Capacitance Vs. Drain-to-Source Voltage

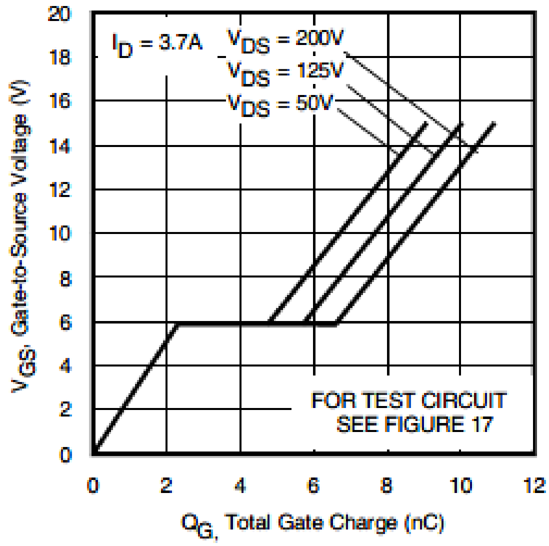


Figure 11 Gate-to-Source Voltage Vs. Typical Gate Charge

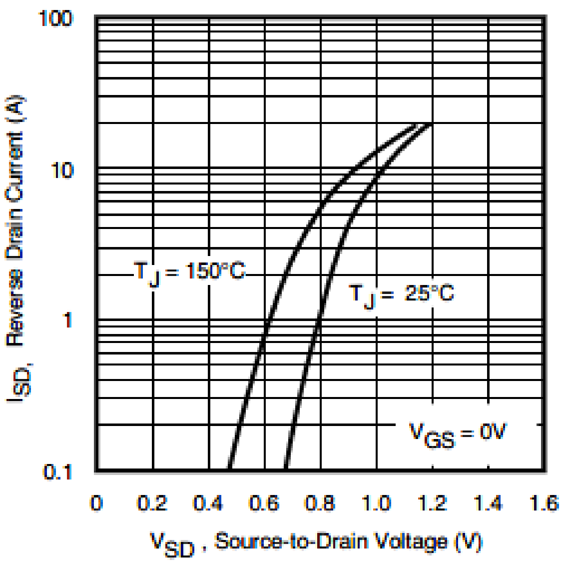


Figure 12 Typical Source-Drain Current Vs. Diode Forward Voltage

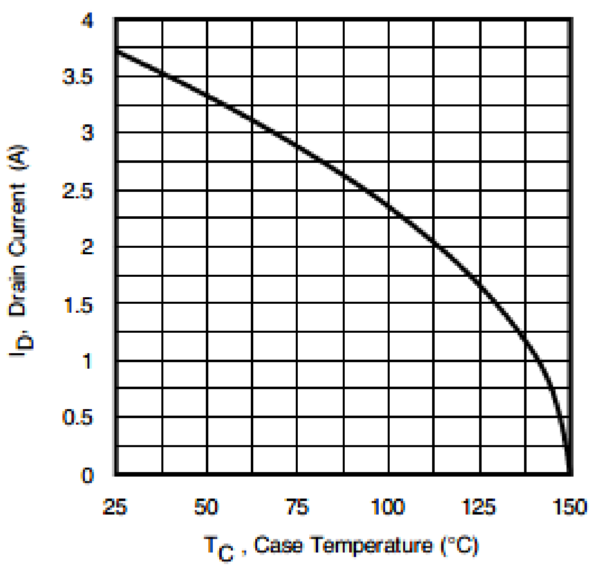


Figure 13 Maximum Drain Current Vs. Case Temperature

Electrical Characteristics Curves (Pre-irradiation)

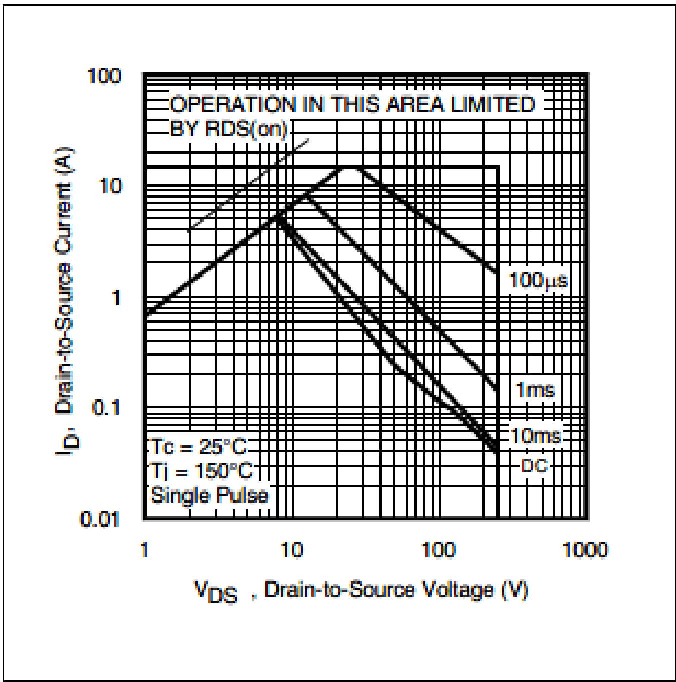


Figure 14 Maximum Safe Operating Area

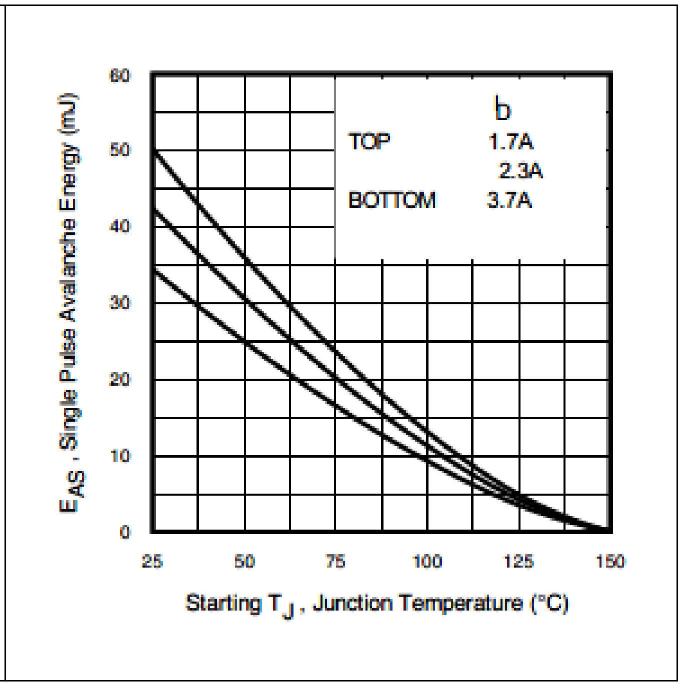


Figure 15 Maximum Avalanche Energy Vs. Junction Temperature

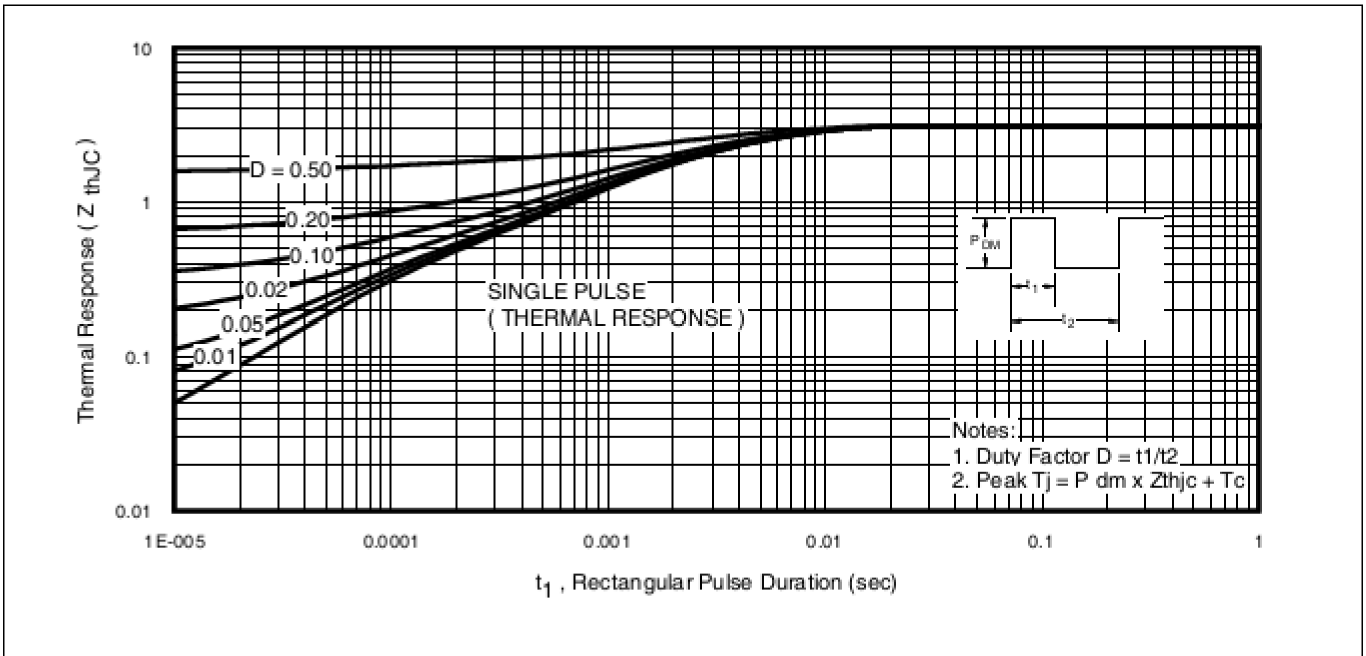


Figure 16 Maximum Effective Transient Thermal Impedance, Junction-to-Case

4 Test Circuits (Pre-irradiation)

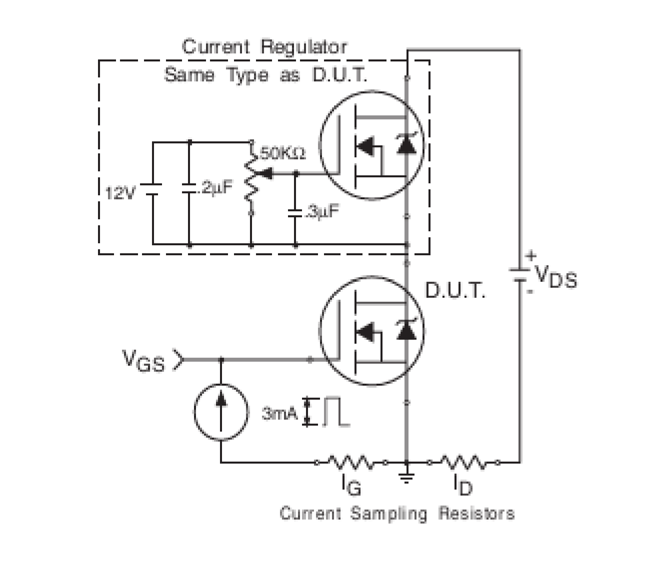


Figure 17 Gate Charge Test Circuit

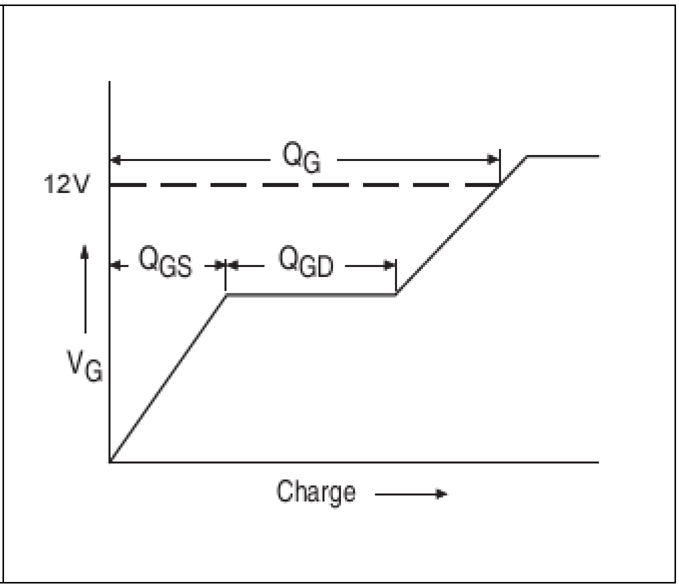


Figure 18 Gate Charge Waveform

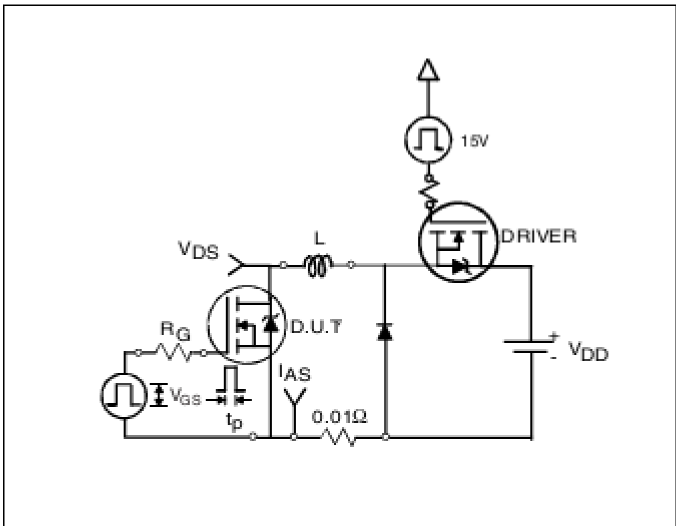


Figure 19 Unclamped Inductive Test Circuit

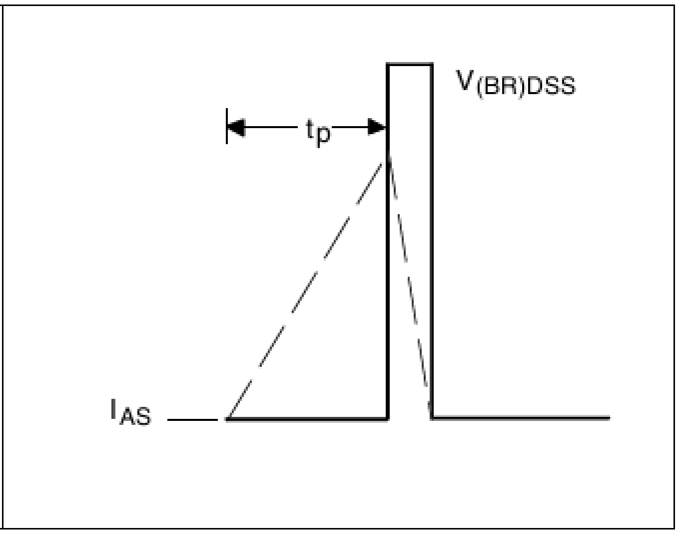


Figure 20 Unclamped Inductive Waveform

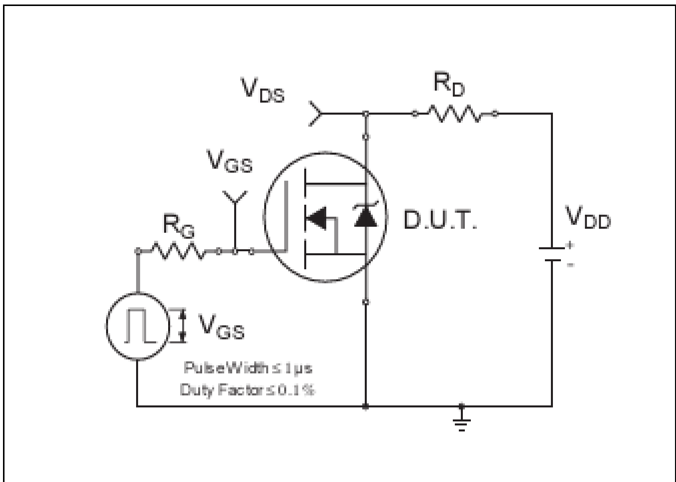


Figure 21 Switching Time Test Circuit

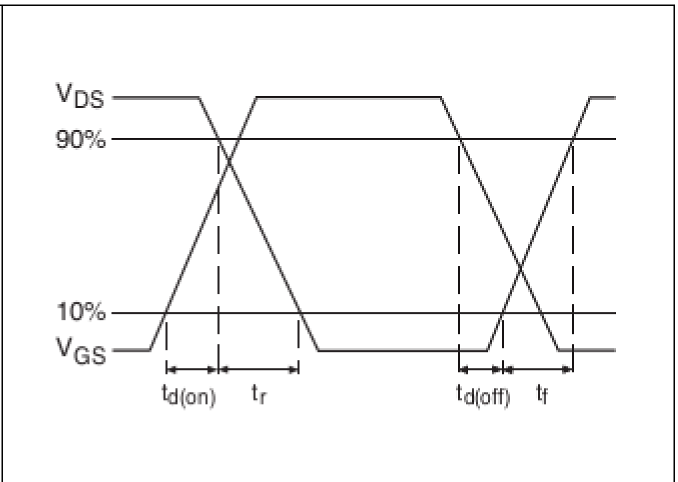
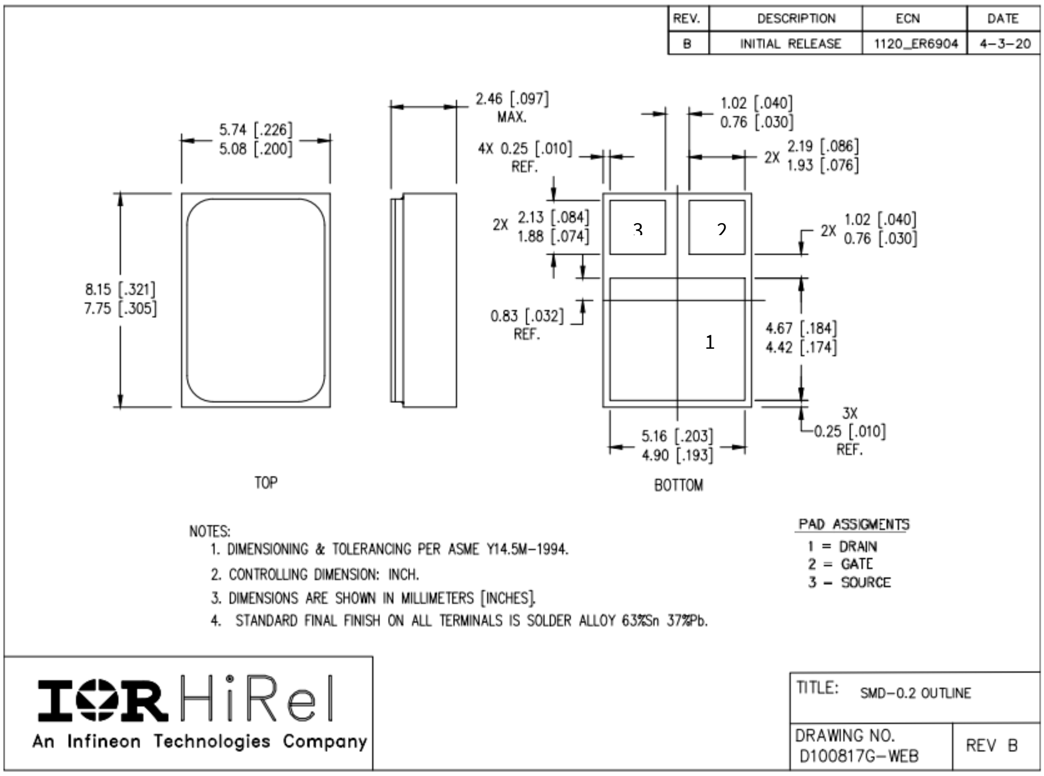


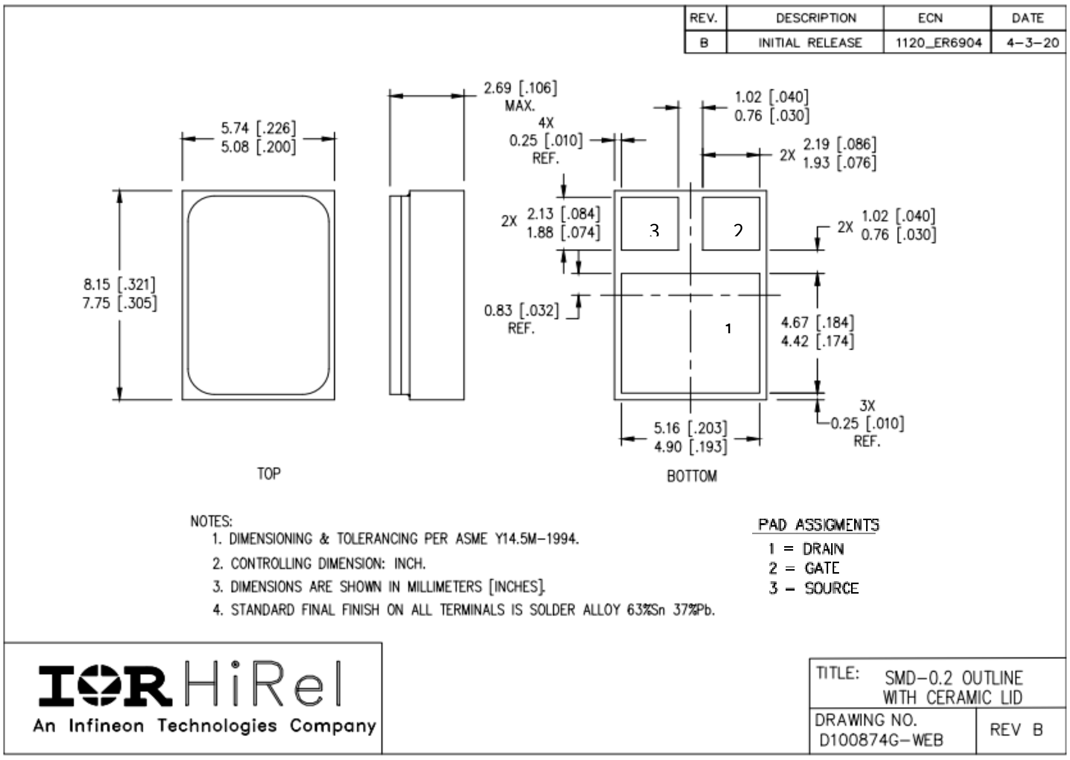
Figure 22 Switching Time Waveforms

5 Package Outline

Note: For the most updated package outline, please see the website: [SMD-0.2 (Metal Lid)]



Note: For the most updated package outline, please see the website: [SMD-0.2 (Ceramic Lid)]



Revision history

Document version	Date of release	Description of changes
	02/12/2014	Datasheet (PD-97818)
Rev A	10/7/2016	Updated based on ECN-1120_04671
Rev B	06/16/2017	Updated based on ECN-1120_05233
Rev C	11/13/2019	Updated based on ECN-1120_07618
Rev D	05/23/2022	Updated based on ECN-1120_08905

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