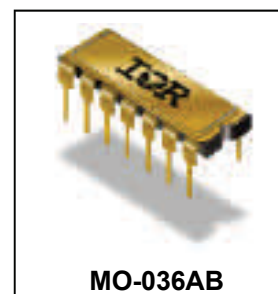


**RADIATION HARDENED
LOGIC LEVEL POWER MOSFET
THRU-HOLE (MO-036AB)**

100V, QUAD N-CHANNEL
R₇ TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	I _D
IRHLG7S7110	100 kRads(Si)	0.33Ω	1.8A
IRHLG7S3110	300 kRads(Si)	0.33Ω	1.8A



Description

IRHLG7S7110 is part of the International Rectifier HiRel family of products. IR HiRel R7 S-line Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available.

Features

- 5V CMOS and TTL Compatible
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Light Weight
- ESD Rating: Class 1B per MIL-STD-750, Method 1020

Absolute Maximum Ratings (Per Die)

Pre-Irradiation

	Parameter		Units
I _D @ V _{GS} = 4.5V, T _C = 25°C	Continuous Drain Current	1.8	A
I _D @ V _{GS} = 4.5V, T _C = 100°C	Continuous Drain Current	1.1	
I _{DM}	Pulsed Drain Current ①	7.2	
P _D @ T _C = 25°C	Maximum Power Dissipation	1.4	W
	Linear Derating Factor	0.01	W/°C
V _{GS}	Gate-to-Source Voltage	± 10	V
E _{AS}	Single Pulse Avalanche Energy ②	97	mJ
I _{AR}	Avalanche Current ①	1.8	A
E _{AR}	Repetitive Avalanche Energy ①	0.14	mJ
dv/dt	Peak Diode Recovery dv/dt ③	11	V/ns
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	1.3 (Typical)	

For Footnotes, refer to the page 2.

Pre-Irradiation

Electrical Characteristics For Each N-Channel Device @ T_J = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.33	Ω	V _{GS} = 4.5V, I _D = 1.1A ④
V _{GS(th)}	Gate Threshold Voltage	1.0	—	2.0	V	V _{DS} = V _{GS} , I _D = 250μA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	—	-4.4	—	mV/°C	
G _{fs}	Forward Transconductance	2.8	—	—	S	V _{DS} = 15V, I _D = 1.1A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	μA	V _{DS} = 80V, V _{GS} = 0V
		—	—	10		V _{DS} = 80V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 10V
	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -10V
Q _G	Total Gate Charge	—	—	11	nC	I _D = 1.8A
Q _{GS}	Gate-to-Source Charge	—	—	4.0		V _{DS} = 50V
Q _{GD}	Gate-to-Drain ('Miller') Charge	—	—	6.0		V _{GS} = 4.5V
t _{d(on)}	Turn-On Delay Time	—	—	20	ns	V _{DD} = 50V
t _r	Rise Time	—	—	35		I _D = 1.8A
t _{d(off)}	Turn-Off Delay Time	—	—	65		R _G = 7.5Ω
t _f	Fall Time	—	—	20		V _{GS} = 5.0V
L _S + L _D	Total Inductance	—	10	—	nH	Measured from Drain lead (6mm / 0.025 in from package) to Source lead (6mm / 0.025 in from pack) with Source wire internally bonded from Source pin to Drain pin
C _{iss}	Input Capacitance	—	653	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	119	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	2.7	—		f = 1.0MHz
R _G	Gate Resistance	—	10	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics (Per Die)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	1.8	A	
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	7.2		
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _J = 25°C, I _S = 1.8A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	100	ns	T _J = 25°C, I _F = 1.8A, V _{DD} ≤ 25V
Q _{rr}	Reverse Recovery Charge	—	—	223	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Thermal Resistance for Each N-Channel Device

	Parameter	Min.	Typ.	Max.	Units
R _{θJA}	Junction-to-Ambient (Typical socket mount)	—	—	90	°C/W
R _{θJC}	Junction-to-Case *	—	7.5	—	°C/W
R _{θJ-LEAD}	Junction-to-Lead (Measured at shoulder of the Lead) *	—	29	—	°C/W
R _{θJ-LID}	Junction-to-Lid *	—	17	—	°C/W

* Values established by Thermal Modeling

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V_{DD} = 50V, starting T_J = 25°C, L = 60mH, Peak I_L = 1.8A, V_{GS} = 10V
- ③ I_{SD} ≤ 1.8A, di/dt ≤ 497A/μs, V_{DD} ≤ 100V, T_J ≤ 150°C
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%
- ⑤ **Total Dose Irradiation with V_{GS} Bias.** 10 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- ⑥ **Total Dose Irradiation with V_{DS} Bias.** 80 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation (Per Die) ⑤⑥

	Parameter	Up to 300 kRads (Si) ¹		Units	Test Conditions
		Min.	Max.		
BV _{DSS}	Drain-to-Source Breakdown Voltage	100	—	V	V _{GS} = 0V, I _D = 250μA
V _{GS(th)}	Gate Threshold Voltage	1.0	2.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V _{GS} = 10V
I _{GSS}	Gate-to-Source Leakage Reverse	—	-100	nA	V _{GS} = -10V
I _{DSS}	Zero Gate Voltage Drain Current	—	1.0	μA	V _{DS} = 80V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source ^④ On-State Resistance (TO-3)	—	0.29	Ω	V _{GS} = 4.5V, I _D = 1.1A
R _{DS(on)}	Static Drain-to-Source ^④ On-State Resistance (MO-036AB)	—	0.33	Ω	V _{GS} = 4.5V, I _D = 1.1A
V _{SD}	Diode Forward Voltage	—	1.2	V	V _{GS} = 0V, I _D = 1.8A

1. Part numbers IRHLG7S7110 and IRHLG7S3110

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	VDS (V)					
			@ VGS = 0V	@ VGS = -1V	@ VGS = -2V	@ VGS = -5V	@ VGS = -6V	@ VGS = -7V
36.3	451	54.6	100	100	100	100	100	100
59.2	808	64.7	100	100	100	100	—	—

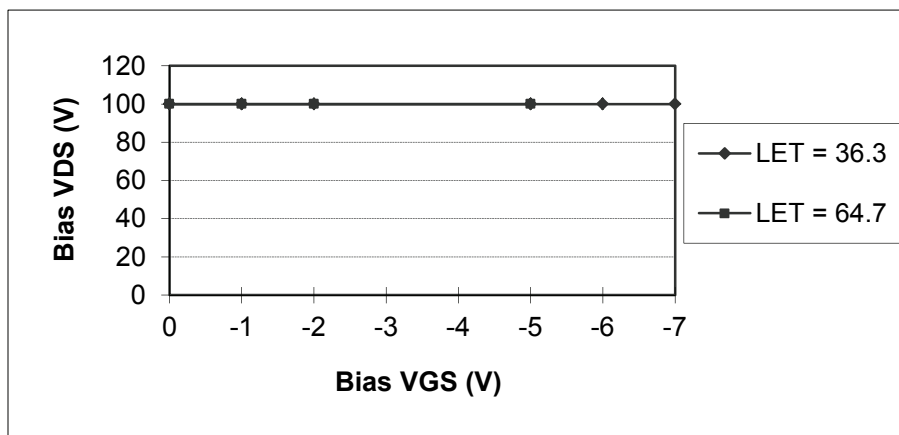


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

Pre-Irradiation

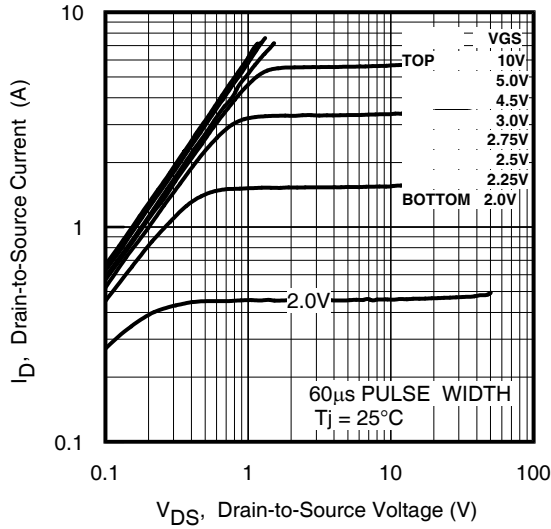


Fig 1. Typical Output Characteristics

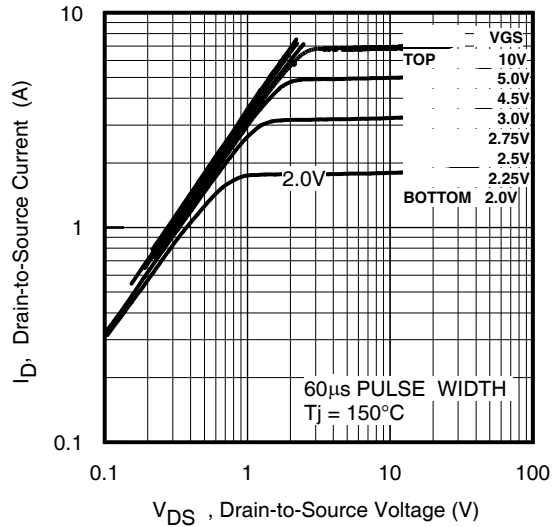


Fig 2. Typical Output Characteristics

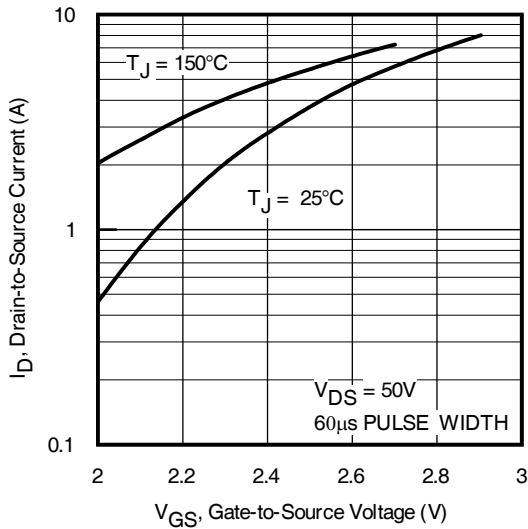


Fig 3. Typical Transfer Characteristics

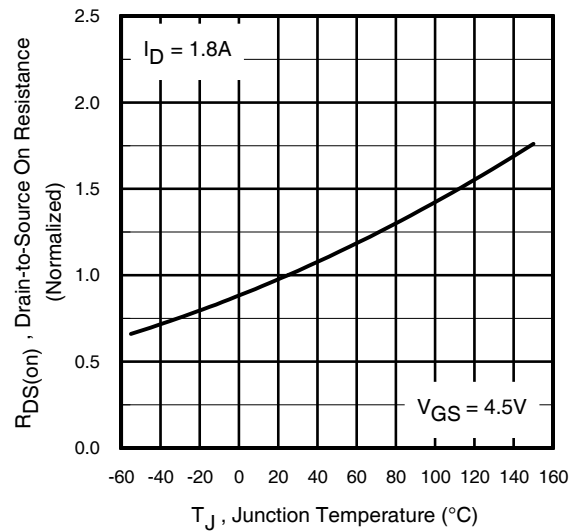


Fig 4. Normalized On-Resistance Vs. Temperature

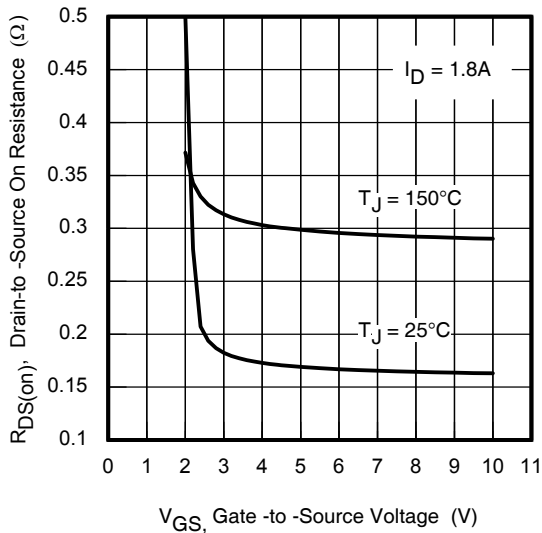


Fig 5. Typical On-Resistance Vs Gate Voltage

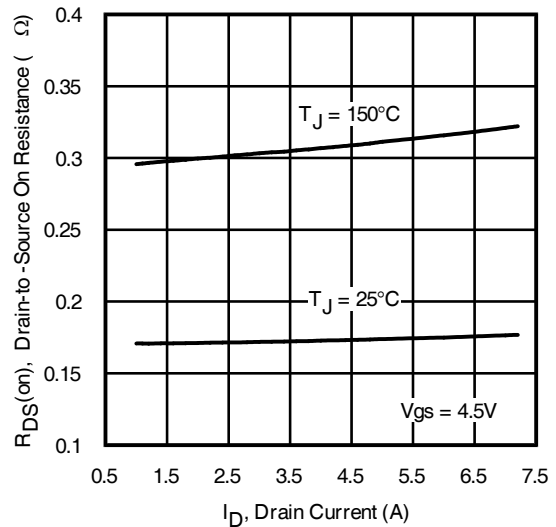


Fig 6. Typical On-Resistance Vs Drain Current

Pre-Irradiation

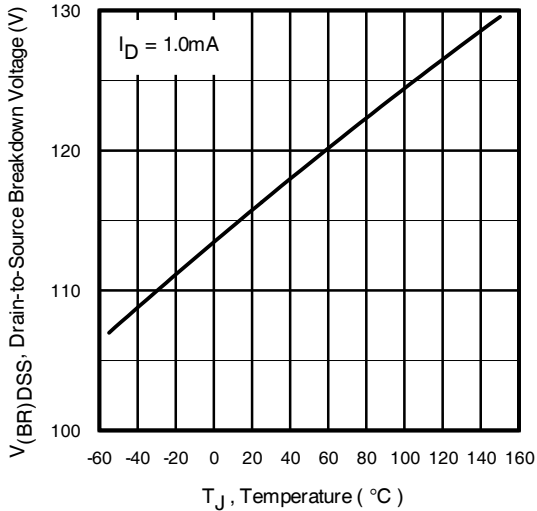


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

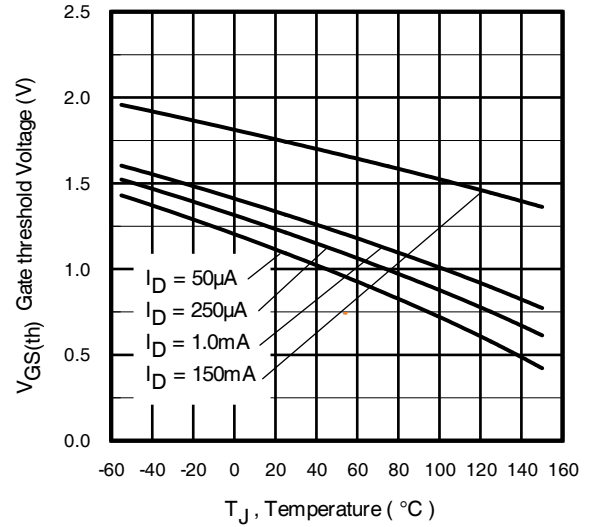


Fig 8. Typical Threshold Voltage Vs Temperature

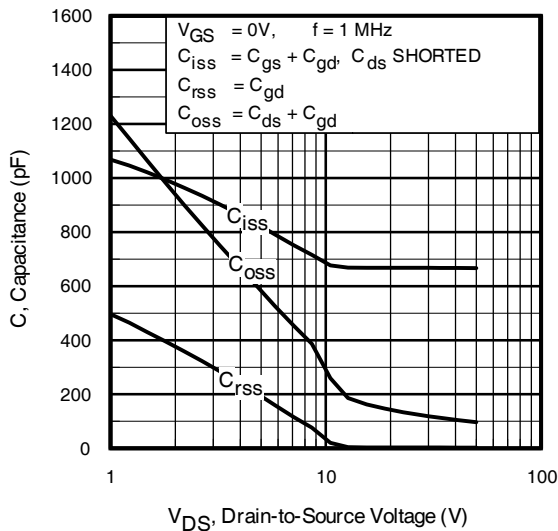


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

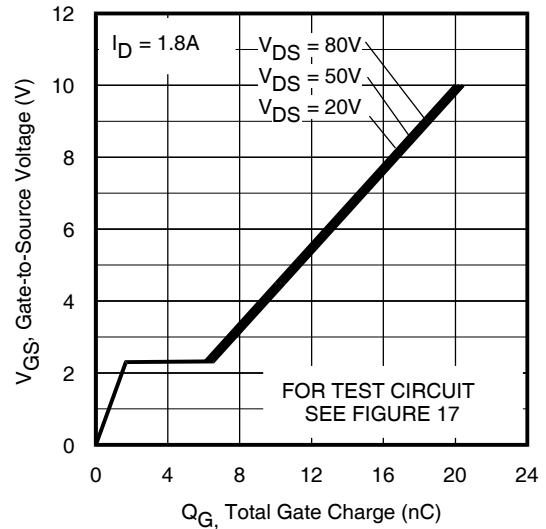


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

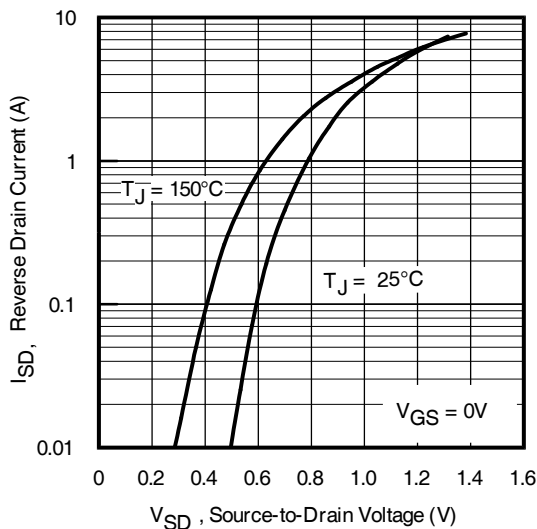


Fig 11. Typical Source-Drain Diode Forward Voltage

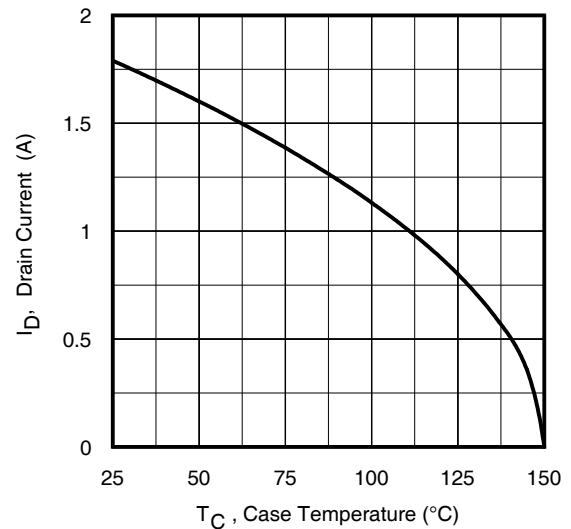


Fig 12. Maximum Drain Current Vs. Case Temperature

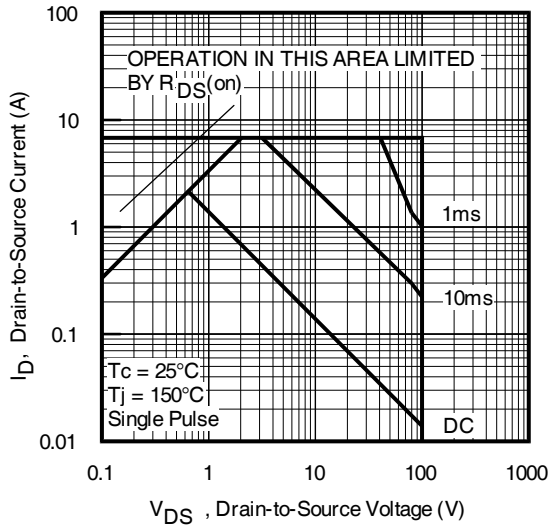


Fig 13. Maximum Safe Operating Area

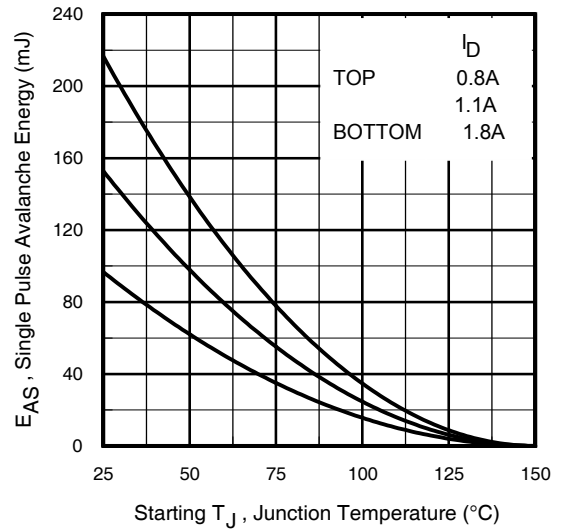


Fig 14. Maximum Avalanche Energy Vs. Drain Current

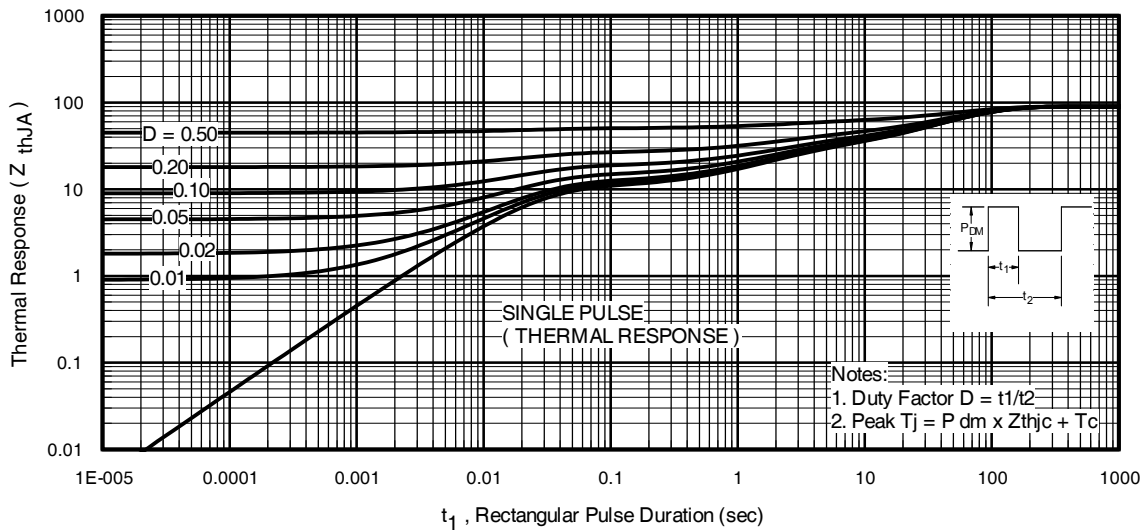


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

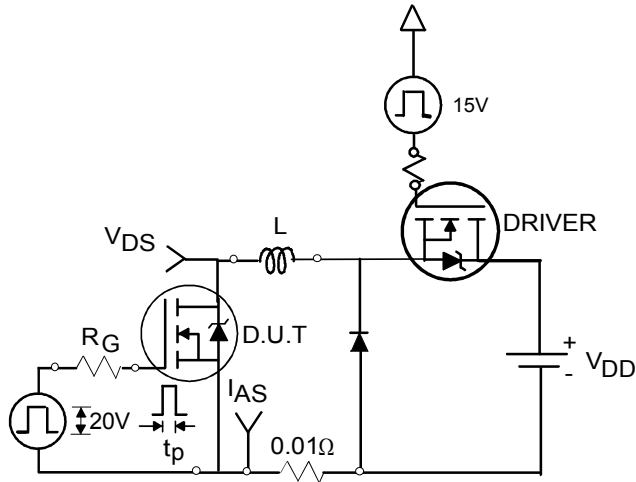


Fig 16a. Unclamped Inductive Test Circuit

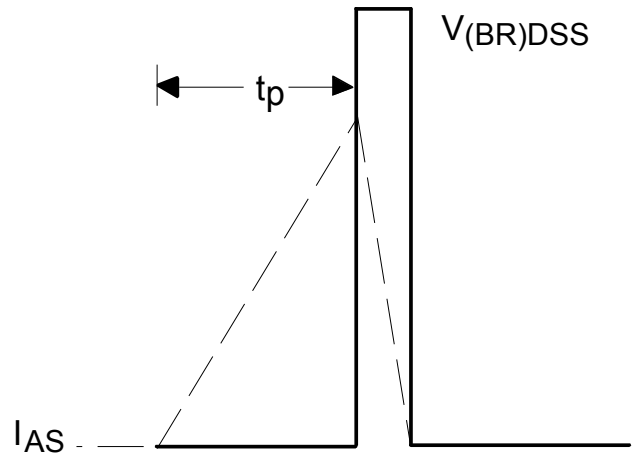


Fig 16b. Unclamped Inductive Waveforms

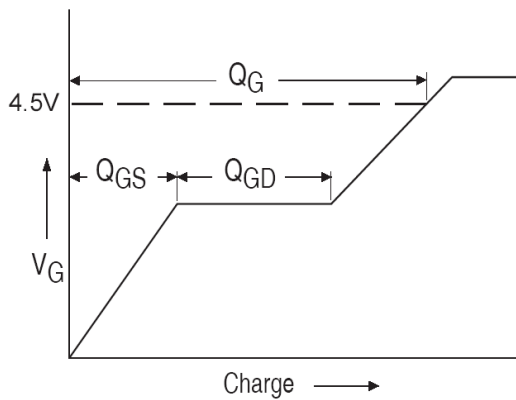


Fig 17a. Gate Charge Waveform

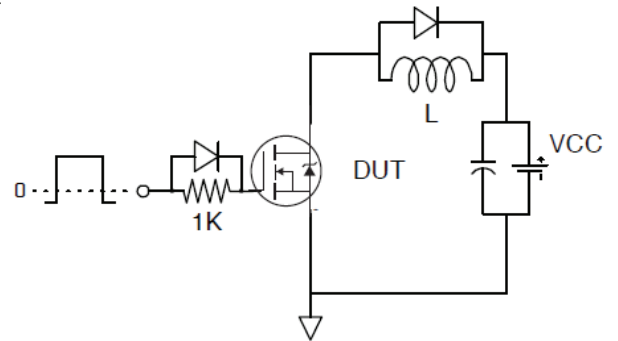


Fig 17b. Gate Charge Test Circuit

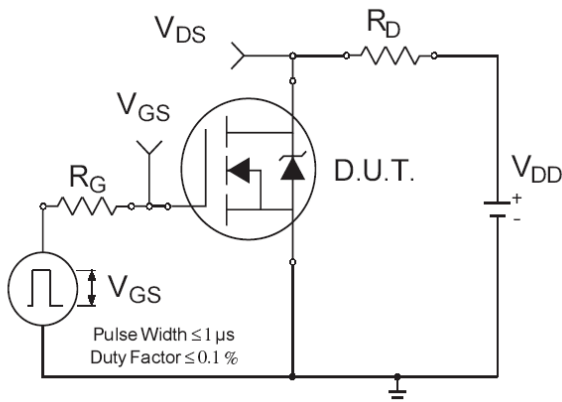


Fig 18a. Switching Time Test Circuit

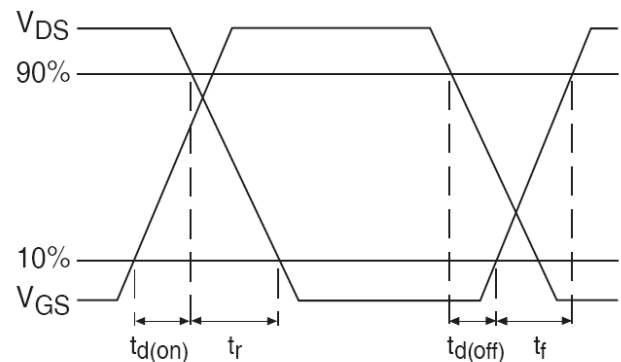
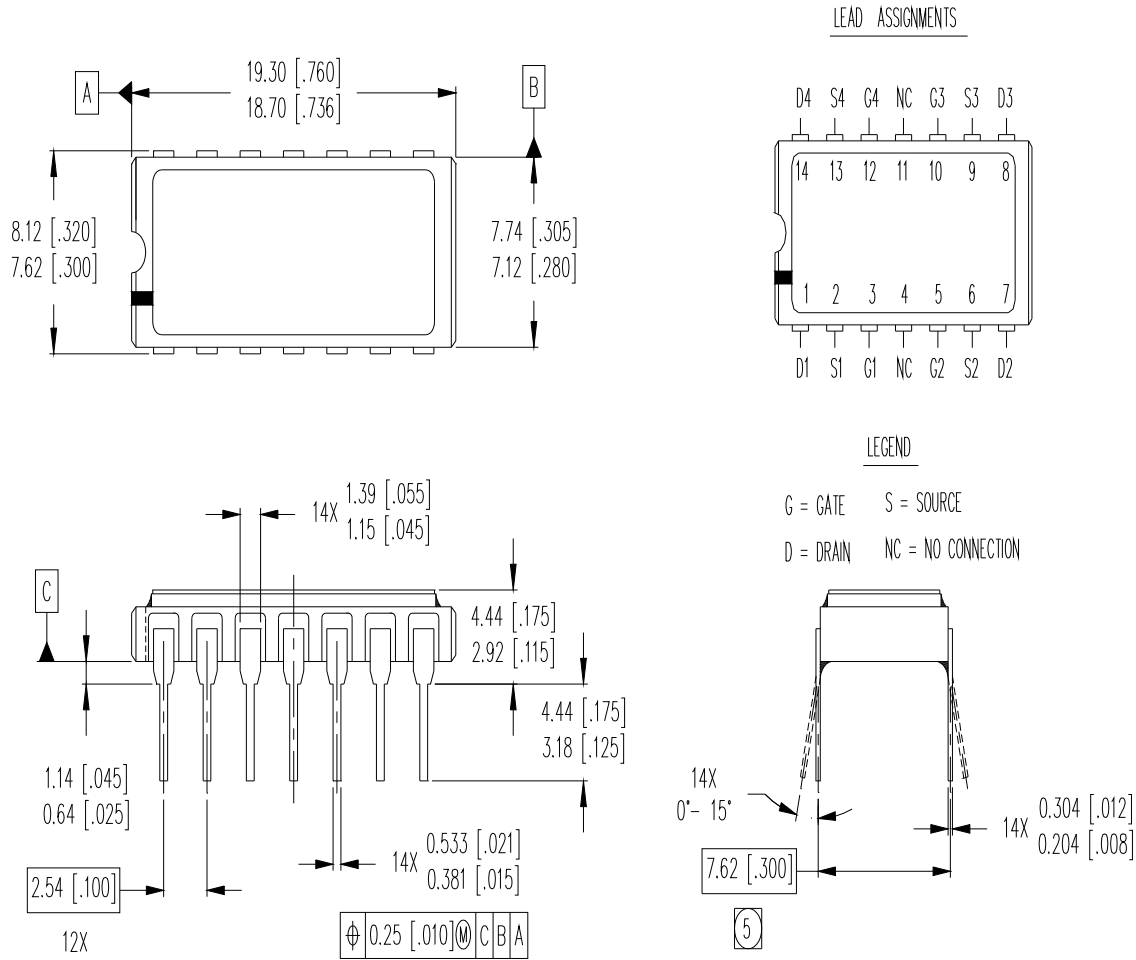


Fig 18b. Switching Time Waveforms

Case Outline and Dimensions - MO-036AB



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MO-036AB.
- ⑤ MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

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