Features
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free

Description
This HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>ID @ Tc = 25°C</td>
<td>A</td>
</tr>
<tr>
<td>ID @ Tc = 100°C</td>
<td>A</td>
</tr>
<tr>
<td>ID @ Tc = 25°C</td>
<td>A</td>
</tr>
<tr>
<td>IDM</td>
<td>A</td>
</tr>
<tr>
<td>PD</td>
<td>W</td>
</tr>
<tr>
<td>VGS</td>
<td>V</td>
</tr>
<tr>
<td>EAS</td>
<td>mJ</td>
</tr>
<tr>
<td>EAS (tested)</td>
<td>mJ</td>
</tr>
<tr>
<td>IAR</td>
<td>A</td>
</tr>
<tr>
<td>EAR</td>
<td>mJ</td>
</tr>
<tr>
<td>TJ</td>
<td>°C</td>
</tr>
<tr>
<td>TSTG</td>
<td>°C</td>
</tr>
<tr>
<td>Mounting torque, 6-32 or M3 screw</td>
<td>10 lbf•in (1.1N•m)</td>
</tr>
</tbody>
</table>

Thermal Resistance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rjce</td>
<td>°C/W</td>
</tr>
<tr>
<td>Rja</td>
<td>°C/W</td>
</tr>
<tr>
<td>Rja (PCB Mount, steady state)</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

HEXFET® is a registered trademark of International Rectifier.
www.irf.com
R = 2.5 \Omega

Limited by TJmax, see Fig. 12a, 12b, 15, 16 for typical repetitive avalanche performance.

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Limited by Tjmax, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
**Fig 1.** Typical Output Characteristics

**Fig 2.** Typical Output Characteristics

**Fig 3.** Typical Transfer Characteristics

**Fig 4.** Typical Forward Transconductance vs. Drain Current
**IRF2907Z/S/LPbF**

**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage

**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

**Fig 7.** Typical Source-Drain Diode Forward Voltage

**Fig 8.** Maximum Safe Operating Area
Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Normalized On-Resistance vs. Temperature

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case
Fig 12a. Unclamped Inductive Test Circuit

Fig 12b. Unclamped Inductive Waveforms

Fig 12c. Maximum Avalanche Energy vs. Drain Current

Fig 13a. Basic Gate Charge Waveform

Fig 13b. Gate Charge Test Circuit

Fig 14. Threshold Voltage vs. Temperature
Notes on Repetitive Avalanche Curves, Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)
1. Avalanche failures assumption:
   1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of $T_{j\text{max}}$. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as $T_{j\text{max}}$ is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_D(\text{ave}) = \frac{1}{2} (1.3 \cdot BV \cdot I_{av})$
5. $BV =$ Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. $I_{av} =$ Allowable avalanche current.
7. $\Delta T =$ Allowable rise in junction temperature, not to exceed $T_{j\text{max}}$ (assumed as 25°C in Figure 15, 16).
8. $t_{av} =$ Average time in avalanche.
9. $D =$ Duty cycle in avalanche = $t_{av}/f$
10. $Z_{thJC}(D, t_{av}) =$ Transient thermal resistance, see Figure 11)

$$P_D(\text{ave}) = \frac{1}{2} (1.3 \cdot BV \cdot I_{av}) = \frac{\Delta T}{Z_{thJC}}$$
$$I_{av} = \frac{2 \cdot \Delta T}{(1.3 \cdot BV \cdot Z_{th})}$$
$$E_{AS(AR)} = P_D(\text{ave}) t_{av}$$

Fig 15. Typical Avalanche Current Vs. Pulsewidth

Fig 16. Maximum Avalanche Energy vs. Temperature
Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

Fig 18a. Switching Time Test Circuit

Fig 18b. Switching Time Waveforms
TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

TO-220AB Part Marking Information

EXAMPLE:  THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Notes: "P" in assembly line position indicates "Lead- Free"

Notes:
1. For an Automotive Qualified version of this part please see http://www.irf.com/product-info/auto/
2. For the most current drawing please refer to IR website at http://www.irf.com/package/

www.irf.com
**IRF2907Z/S/LPbF**

**D²Pak (TO-263AB) Package Outline**

Dimensions are shown in millimeters (inches)

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**Notes:**

1. For an Automotive Qualified version of this part please see [http://www.irf.com/product-info/auto/](http://www.irf.com/product-info/auto/)
2. For the most current drawing please refer to IR website at [http://www.irf.com/package/](http://www.irf.com/package/)

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D²Pak (TO-263AB) Part Marking Information

**Example:** This is an IRF530S with LOT CODE 8024 ASSEMBLED ON WW02, 2000 IN THE ASSEMBLY LINE "L"

Note: "F" in assembly line position indicates "Lead - Free"
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"

International Rectifier

Notes:
1. For an Automotive Qualified version of this part please see http://www.irf.com/product-info/auto/
2. For the most current drawing please refer to IR website at http://www.irf.com/package/

www.irf.com
IRF2907Z/S/LPbF

D²Pak Tape & Reel Information
Dimensions are shown in millimeters (inches)

NOTES:
1. CONFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.
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