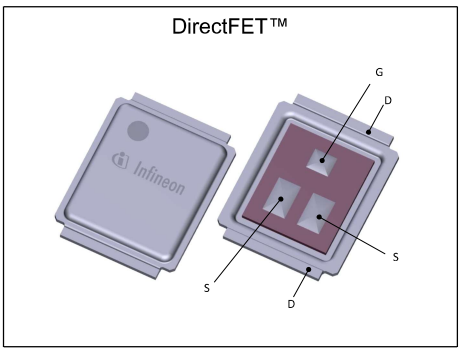
MOSFET

OptiMOS™ 5, 150 V

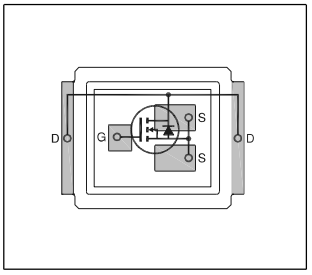


Features

- Lead free, ultra thin double sided cooling package
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on -resistance $R_{DS(on)}$
- N-channel normal level
- 100% avalanche tested

Applications

- Brushed Motor drive, Synchronous rectifier and BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters



Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	150	V
$R_{DS(on),max}$	11.3	mΩ
I_D	60	A
Q_{oss}	87	nC
Q_G (0V..10V)	33	nC

Type / Ordering Code	Package	Marking	Related Links
IRF150DM115	MG-WDSON-5	M115	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - -	- - -	60 38 11	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{THJA}=45 °C/W[2]
Pulsed drain current[3]	$I_{D,pulse}$	-	-	240	A	T_A=25 °C
Avalanche energy, single pulse[4]	E_{AS}	-	-	72	mJ	I_D=45 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	78 2.8	W	T_C=25 °C T_A=25 °C, R_{THJA}=45 °C/W[2]
Operating and storage temperature	T_j, T_{stg}	-40	-	150	°C	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.6	°C/W	-
Thermal resistance, junction - ambient, double sided cooling	R_{thJA}[5]	-	12.5	-	°C/W	-
Thermal resistance, junction - ambient, mounted on minimum foot print	R_{thJA}[6]	-	20	-	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}[2]	-	-	45	°C/W	-
Device on PCB	$R_{thJ\text{-}PCB}$	-	0.75	-	°C/W	-
Soldering temperature, wave andreflow soldering are allowed	T_{sold}	-	-	260	°C	reflow MSL3

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information
[5] Used double sided cooling, mounting pad with large heat sink
[6] Mouted on minimum footprint full size board with metalized back with small clip heat sink

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	3	3.8	4.6	V	V_{DS}=V_{GS}, I_D=106 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=120 V, V_{GS}=0 V, T_j=25 °C V_{DS}=120 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	8.5	11.3	mΩ	V_{GS}=10 V, I_D=45 A
Gate resistance	R_G	-	0.7	-	Ω	-
Transconductance[1]	g_{fs}	33	66	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=45 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1]	C_{iss}	-	2300	3000	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Output capacitance[1]	C_{oss}	-	580	780	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Reverse transfer capacitance[1]	C_{rss}	-	41	70	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	11	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=45 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	21	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=45 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	14	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=45 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	14	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=45 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[2]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	13.2	-	nC	V_{DD}=75 V, I_D=45 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	8.7	-	nC	V_{DD}=75 V, I_D=45 A, V_{GS}=0 to 10 V
Gate to drain charge[1]	Q_{gd}	-	8.0	12	nC	V_{DD}=75 V, I_D=45 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	12.5	-	nC	V_{DD}=75 V, I_D=45 A, V_{GS}=0 to 10 V
Gate charge total[1]	Q_g	-	33	50	nC	V_{DD}=75 V, I_D=45 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	5.7	-	V	V_{DD}=75 V, I_D=45 A, V_{GS}=0 to 10 V
Output charge[1]	Q_{oss}	-	87	115	nC	V_{DS}=75 V, V_{GS}=0 V

[1] Defined by design. Not subject to production test.
[2] See "Gate charge waveforms" for parameter definition

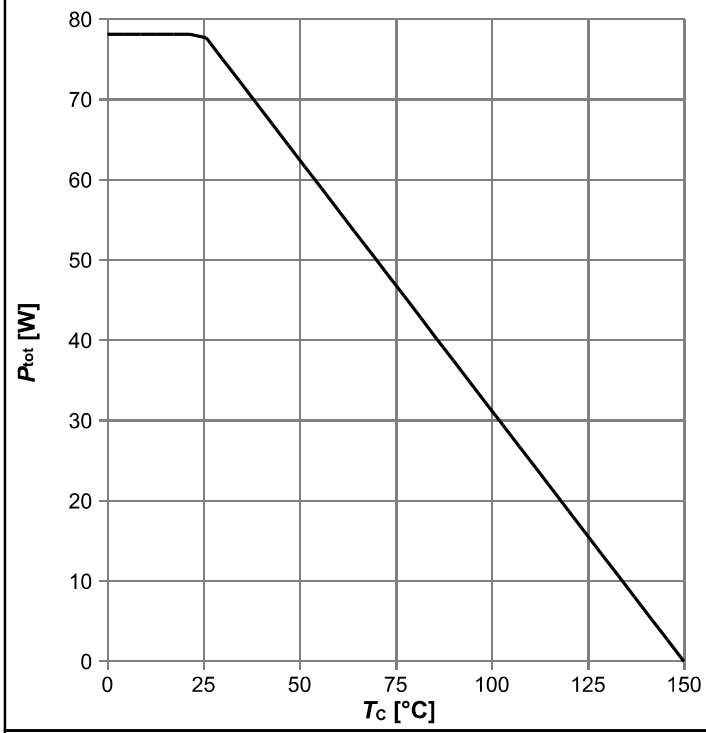
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	60	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	240	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.9	1.2	V	V_{GS}=0 V, I_F=45 A, T_j=25 °C
Reverse recovery time[1)]	t_{rr}	-	39	78	ns	V_R=75 V, I_F=45 A, di_F/dt=100 A/µs
Reverse recovery charge[1)]	Q_{rr}	-	47	94	nC	V_R=75 V, I_F=45 A, di_F/dt=100 A/µs

[1)] Defined by design. Not subject to production test.

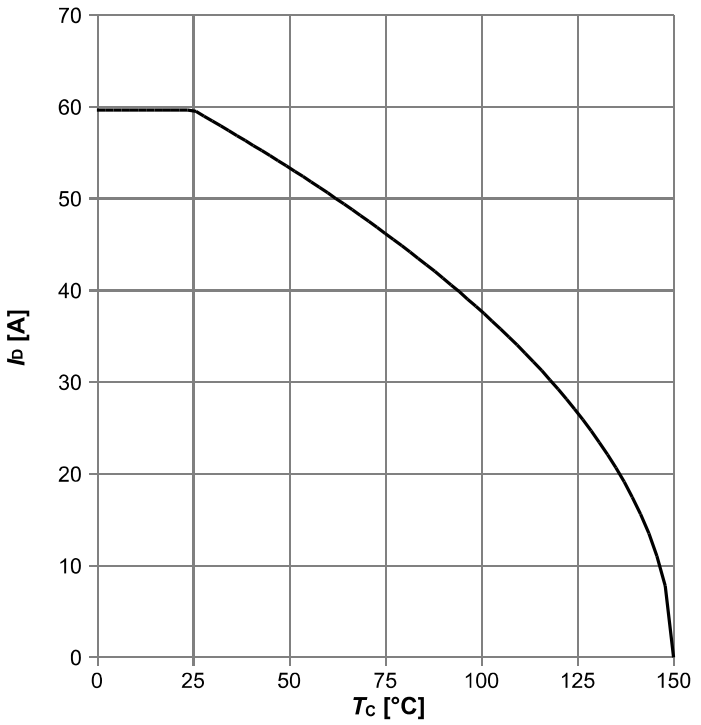
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



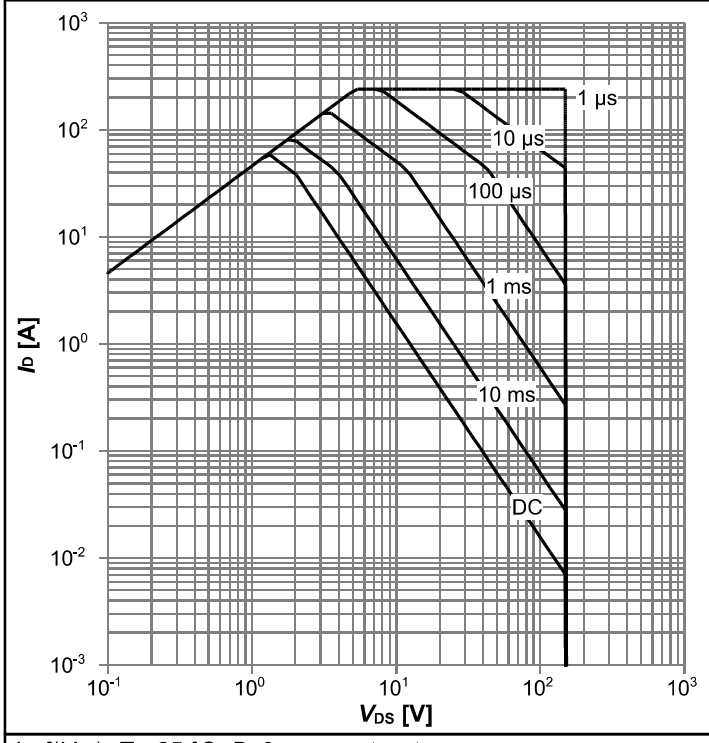
$P_{tot}=f(T_C)$

Diagram 2: Drain current



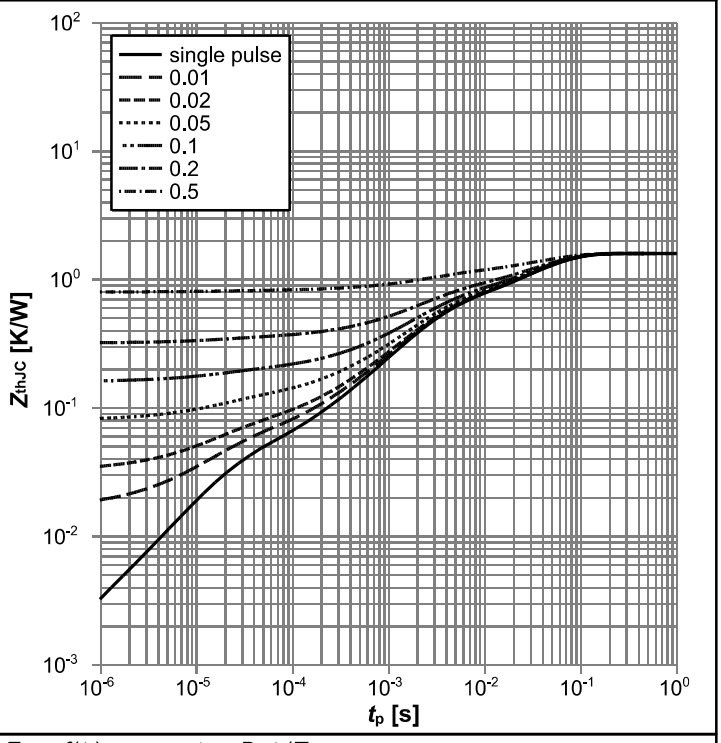
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



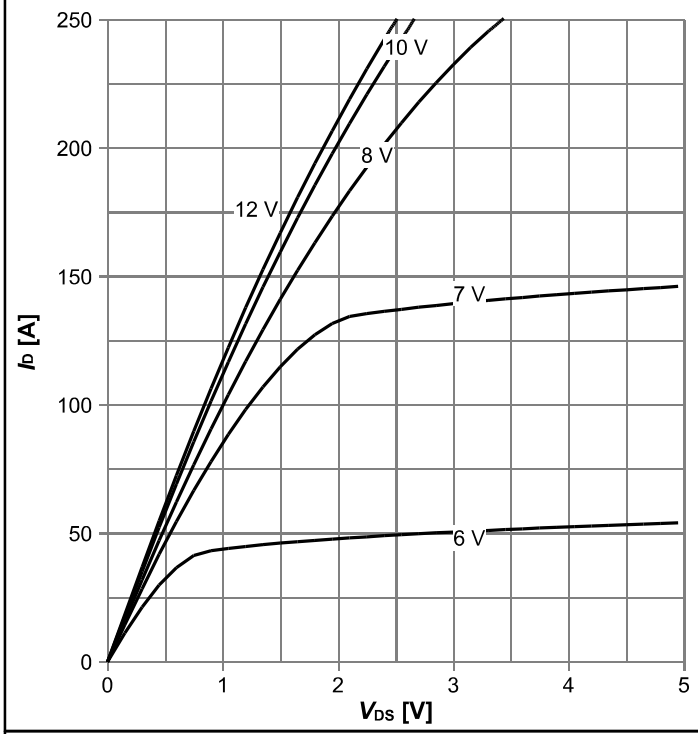
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



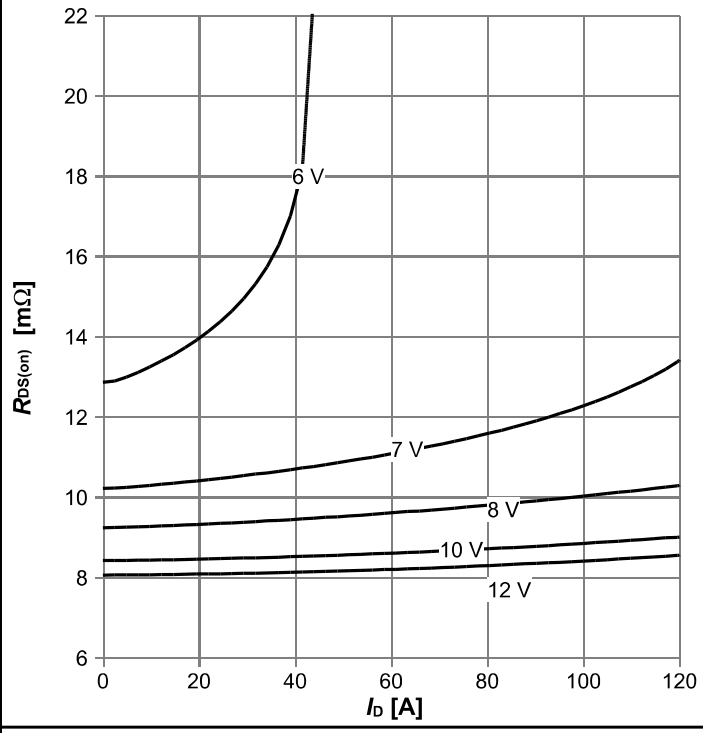
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



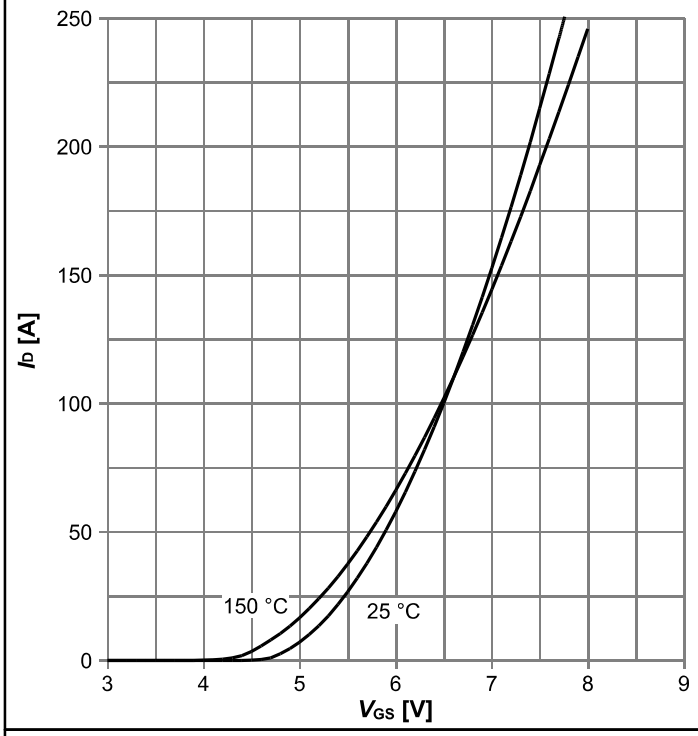
$I_D=f(V_{DS})$, $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



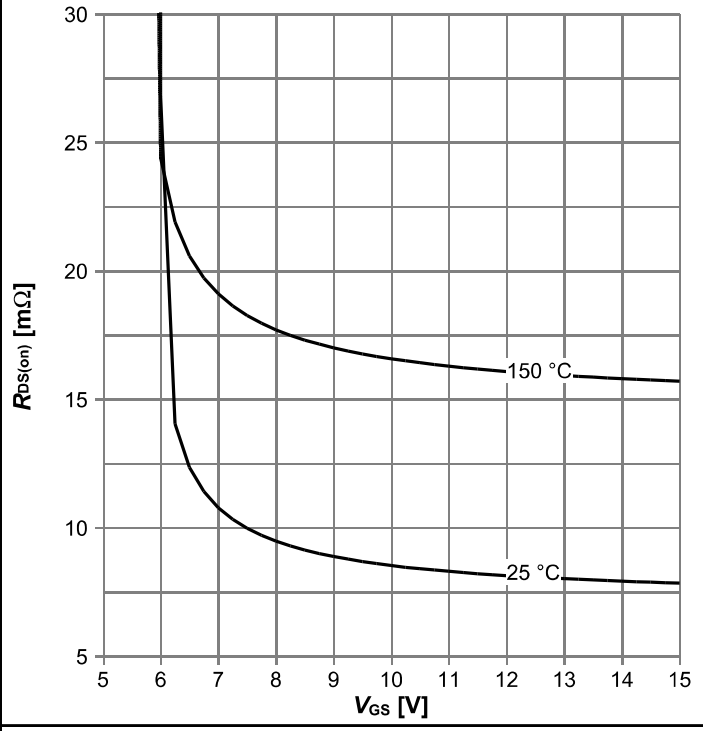
$R_{DS(on)}=f(I_D)$, $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



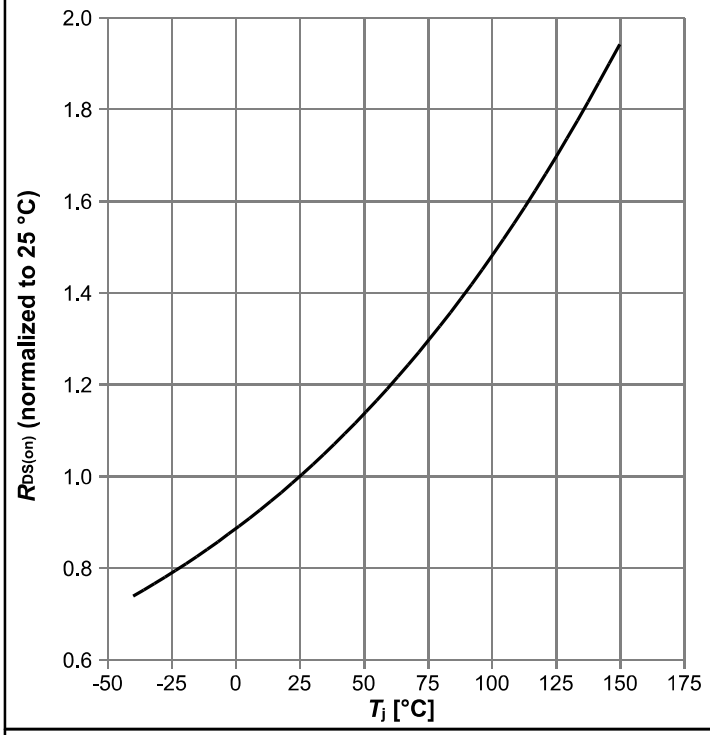
$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



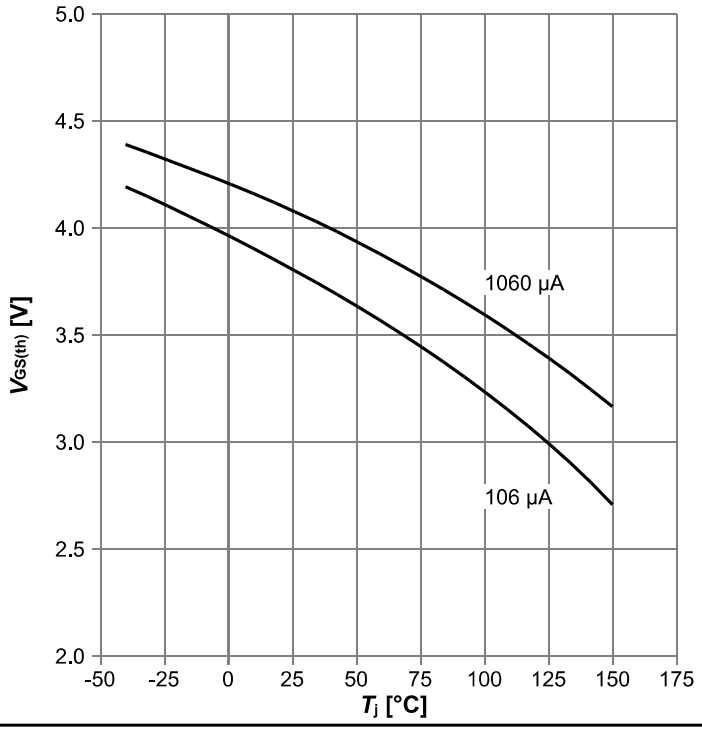
$R_{DS(on)}=f(V_{GS})$, $I_D=45$ A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



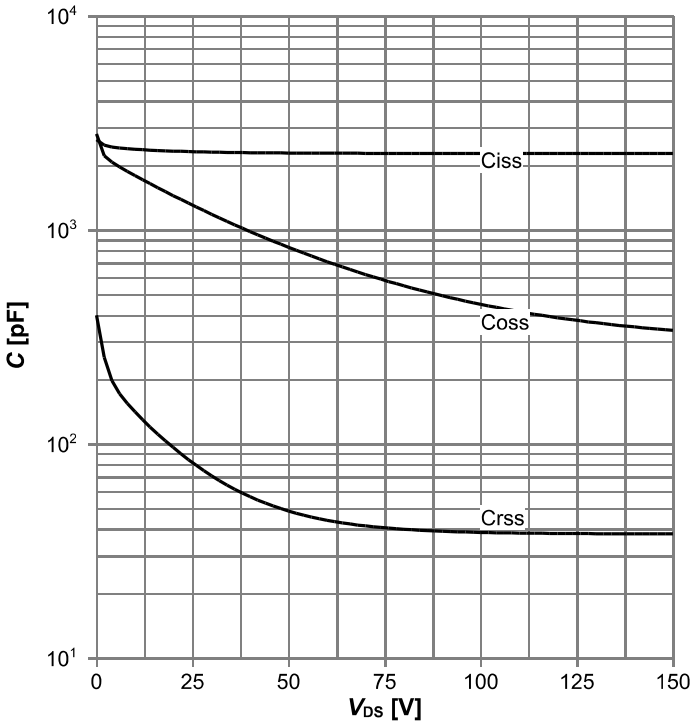
$R_{DS(on)}$=f(T_j), I_D=45 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



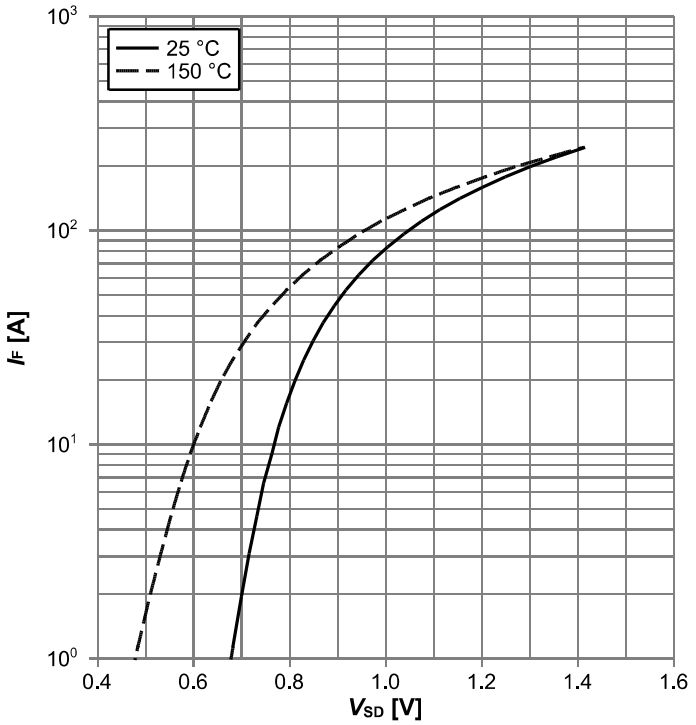
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



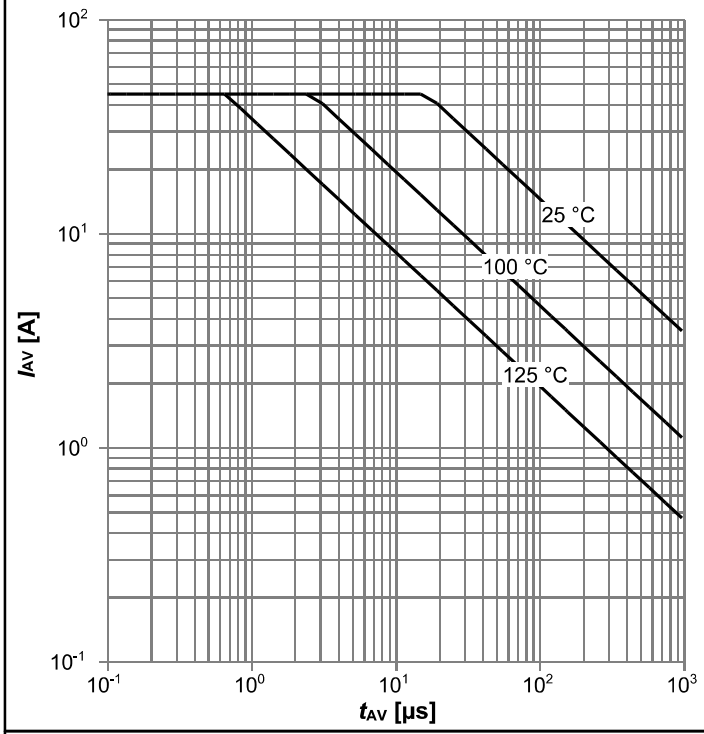
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Typ. forward characteristics of reverse diode



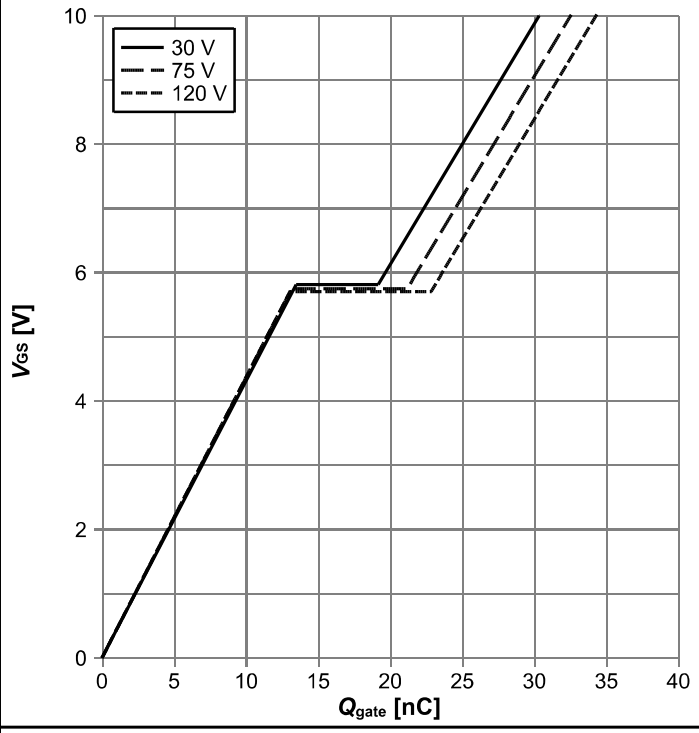
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



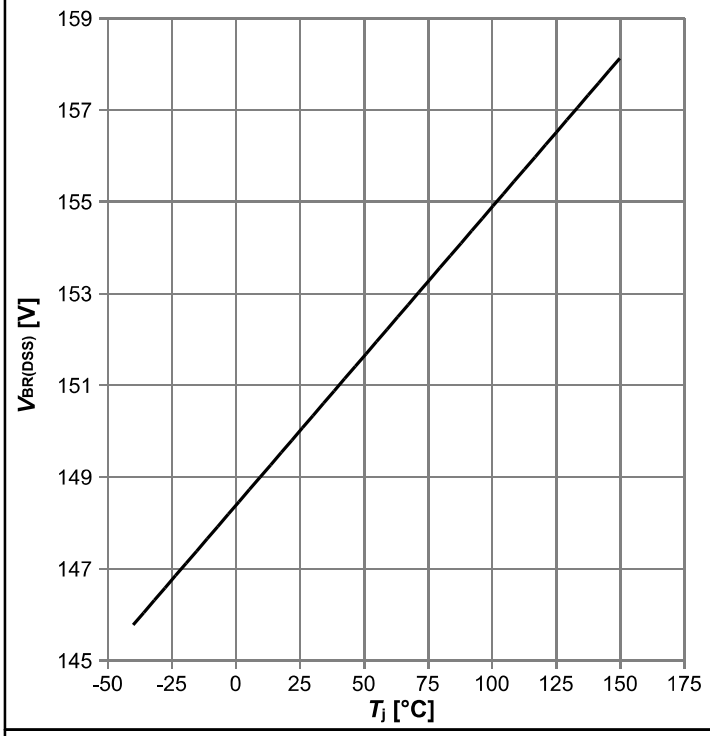
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



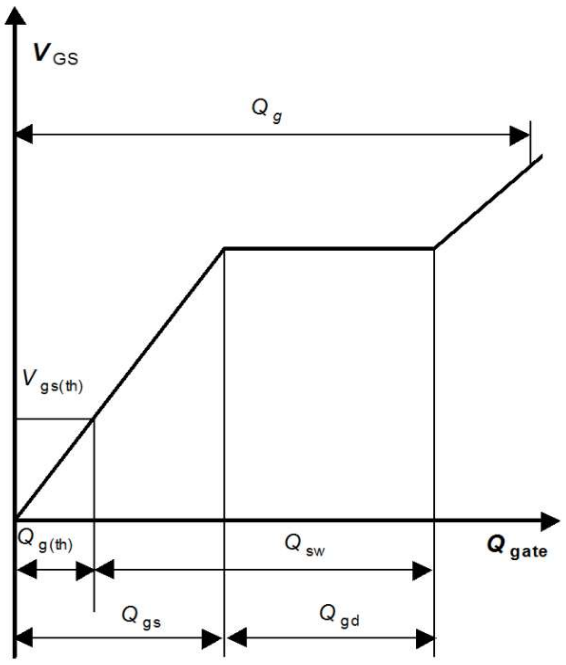
V_{GS}=f(Q_{gate}), I_D=45 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage



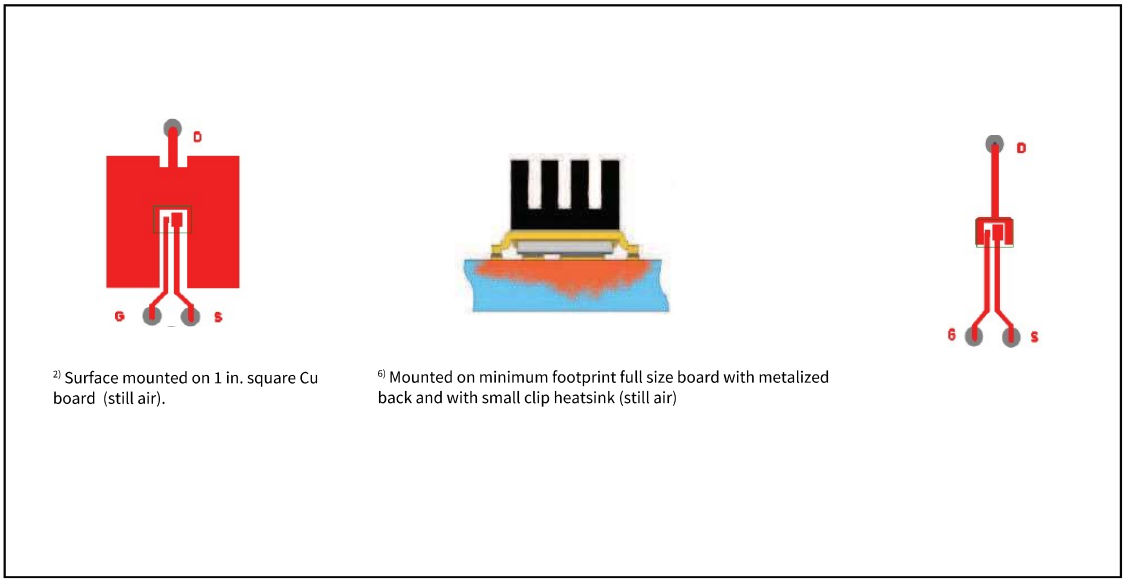
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms



5 Test Circuits

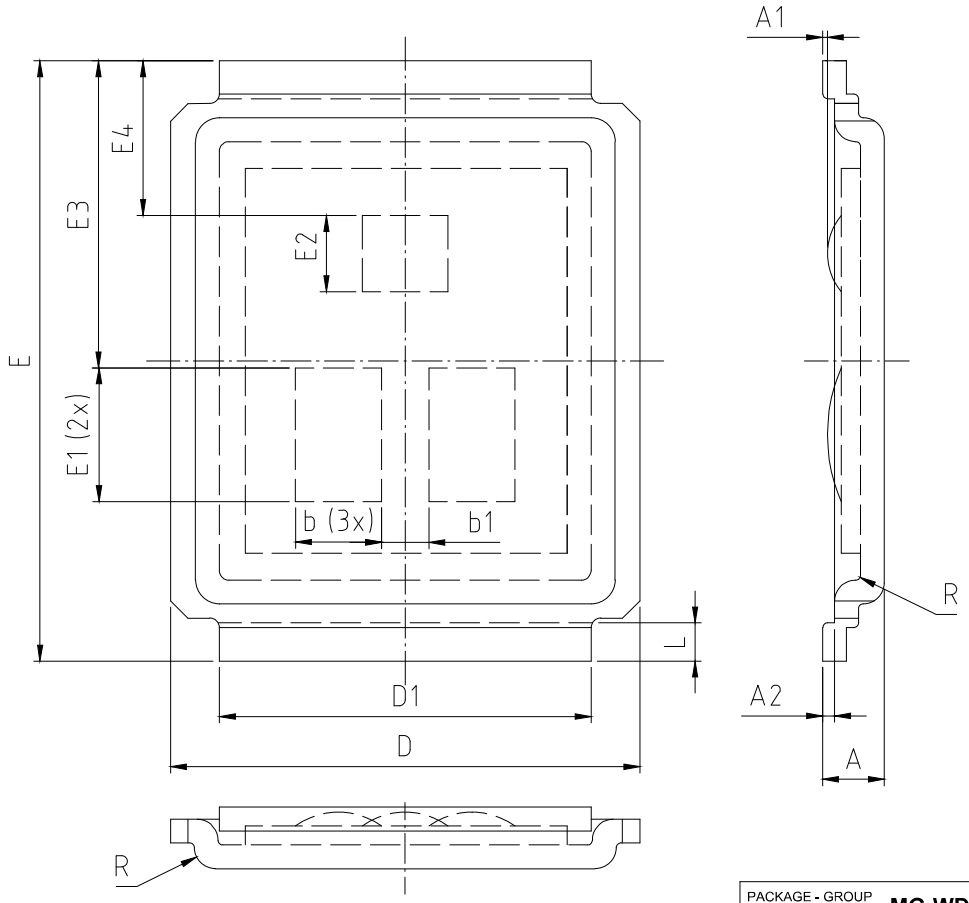
Table 8 Rth/Zth measurement diagrams



[2] Surface mounted on 1 in. square Cu board (still air).

[6] Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)

6 Package Outlines



PACKAGE - GROUP NUMBER:	MG-WDSON-5-U02	
DIMENSIONS	**MILLIMETERS**	
	MIN.	MAX.
A	0.59	0.70
A1	0.00	0.10
A2	0.08	0.17
b	0.88	0.92
b1	0.48	0.52
D	4.80	5.05
D1	3.85	3.95
E	6.25	6.35
E1	1.38	1.42
E2	0.78	0.82
E3	3.125	3.33
E4	1.525	1.73
L	0.35	0.45
R	---	0.10
N	5	

Figure 1 Outline MG-WDSON-5, dimensions in mm

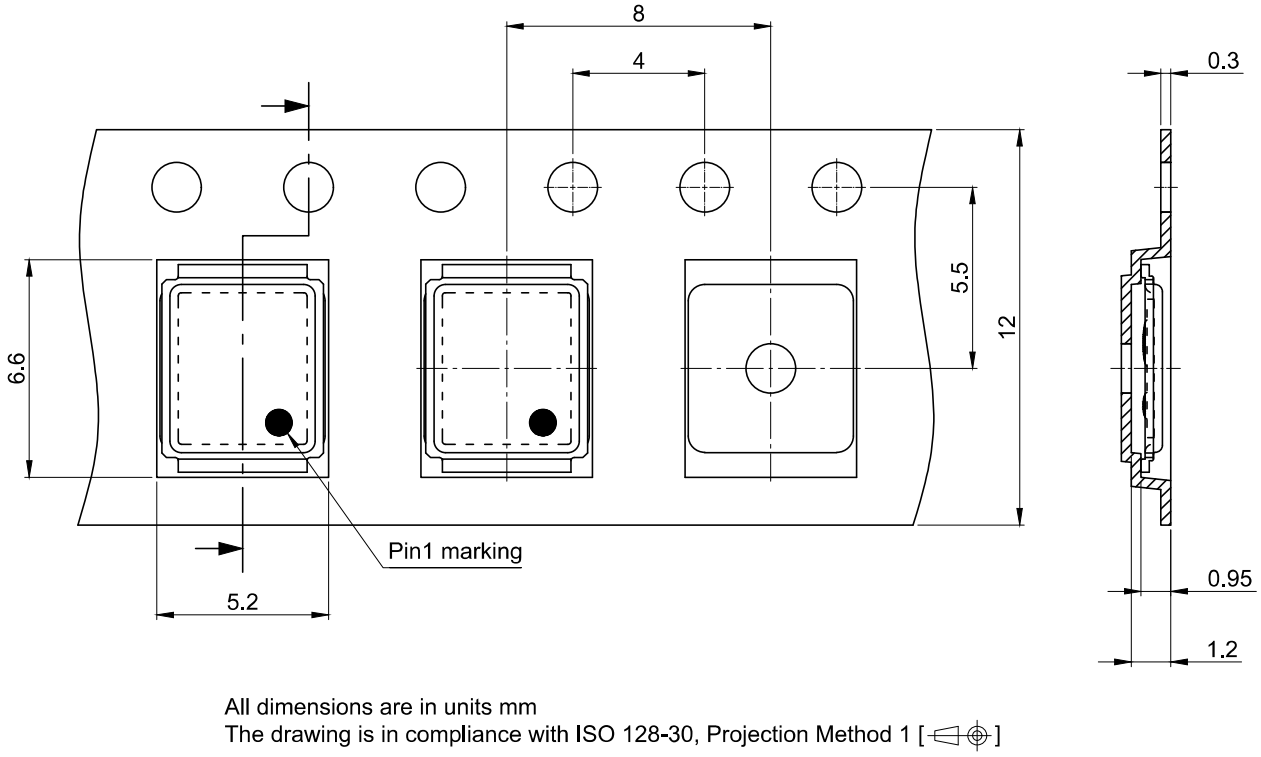


Figure 2 Outline Tape (MG-WDSON-5), dimensions in mm

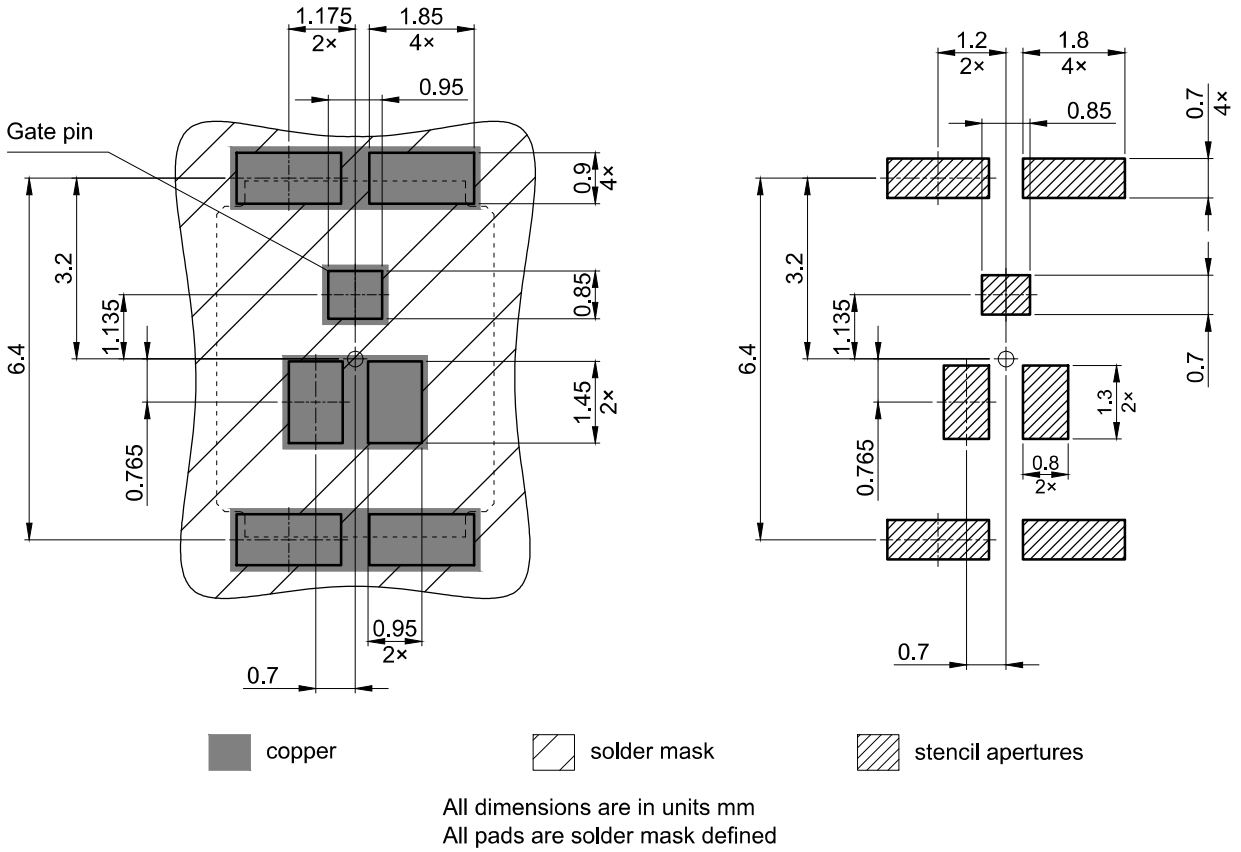


Figure 3 Outline Footprint (MG-WDSON-5), dimensions in mm

Revision History

IRF150DM115

Revision: 2023-08-29, Rev. 2.1

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2022-04-08	Release of final version
2.1	2023-08-29	Updated Rg, and outline_tape_footprint drawings

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