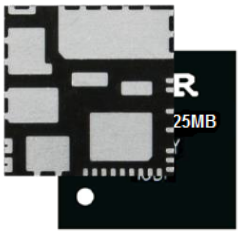
Reference Manual

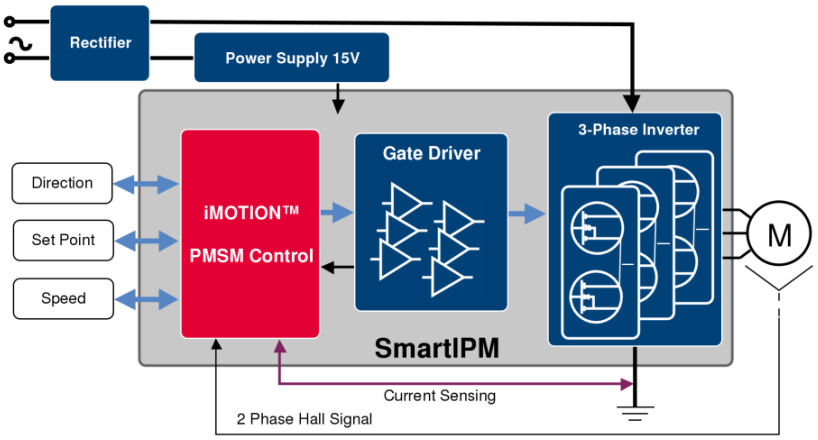
iMOTION™ Motion Controller Module for PM AC Fan

Quality Requirement Category: Industry

Features

- Complete 250V - 500V 3-phase inverter system in one chip
- Permanent Magnet Sinusoidal Motors Control by Hall sensors
  Only two low cost Hall elements required
- High efficiency control by quadratic phase advance curve
- Internal clock based on external RC
- 15V single power supply
  3.3V Integrated Voltage Regulator
- Integrated protection features:
  Dynamic overcurrent , Overtemperature ,
  Overspeed, Rotor lock, Undervoltage lockout
- Full Three Phase Gate Driver
- Integrated Bootstrap Diodes
- No heatsink required
- 12x12 mm² PQFN package





Applications

- PM fan motor control

Description

IRDM983-025MB, IRDM983-035MB are the complete PM motor controller including six power MOSFET, high voltage integrated circuit, high precision analog circuit and integrated digital control algorithm. The controller implements a Hall sensor based control algorithm for 3-phase sinusoidal permanent magnet motor fan applications.

Other than the IRDM982 the IRDM983 only requires two hall sensors.

The integrated digital controller does not require any programming.
Instead there are 16 load curves stored in the internal ROM that can be selected via two resistor pairs.

The IRDM983 is packaged in the 12 x 12 PQFN package and designed to dissipate the power loss through a PCB without the use of an external heatsink.

There are two products available depending on the power rating of the internal high voltage MOSFETs:

1) IRDM983-025MB – employs six MOSFETs 500V 2A and 600V high voltage IC

2) IRDM983-035MB – employs six MOSFETs 500V 3A and 600V high voltage IC

International
IOR Rectifier

IRDM983-025/035MB Reference Manual

Complete Motion Controller Module for PM AC fan

Features

- Complete 500V 3-phase inverter system in one chip
- No heat-sink required
- Permanent Magnet Sinusoidal Motors Control by two Hall sensors
- Internal clock based on external RC
- High efficiency control by quadratic phase advance curve
- 15V single power supply
- 3.3V Integrated Voltage Regulator
- Selectable 4 or 12 pulse output per revolution
- Low standby power
- Dynamic overcurrent limit per temperature
- Over-temperature control
- Over-speed protection
- Rotor lock detection/protection
- Full Three Phase Gate Driver
- Integrated Bootstrap Diodes
- Under-voltage lockout

Typical Applications

- Fan motor control

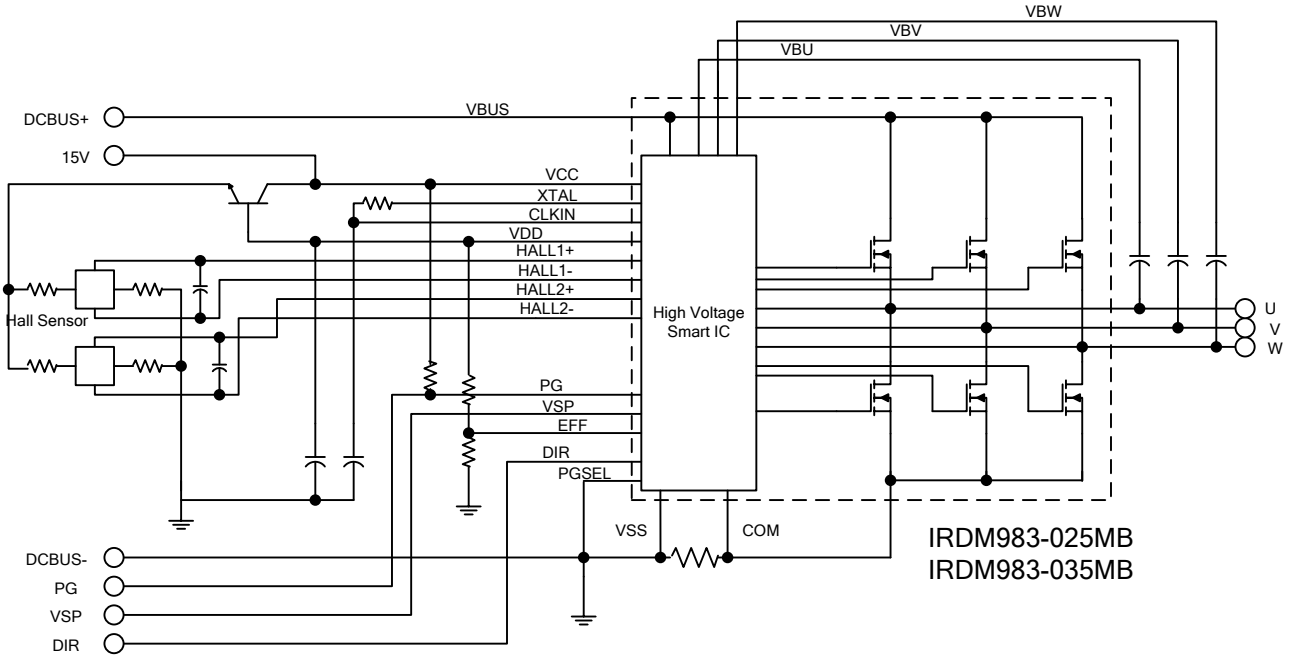
Product Summary

Topology	3 Phase AC
V_{OFFSET}	≤ 500 V
Control	Current phase & CEMF shift control
Feedback	DC bus shunt, 2 Hall sensor
Temperature sensor	Integrated

Package

12 mm x 12mm PQFN

Typical Connection Diagram



Revision History

1) IRDM983 DATASHEET REVISION 1 (MAY 5, 2015)

2) INITIAL RELEASE – AUGUST 8, 2015

3) IRDM983 REFERENCE MANUAL REVISION 2 (MARCH 22, 2015)

Table of Contents

1.0 Introduction

IRDM983-025MB, IRDM983-035MB are the complete PM motor controller including six power MOSFET, high voltage integrated circuit, high precision analog circuit and digital control algorithm. There are two products depending on power rating of internal high voltage MOSFET listed below:

1) IRDM983-025MB – employs six MOSFET 500V/Rdson=4ohms and 600V high voltage IC
2) IRDM983-035MB – employs six MOSFET 500V/Rdson=2ohms and 600V high voltage IC

All two products are packaged in the 12 x 12 PQFN package and designed to dissipate the power loss through a mating PCB without an external heatsink. All two products contain exactly same control algorithm and analog functions. The controller implements a two Hall sensor based control algorithm for 3-phase sinusoidal permanent magnet motor fan applications. The control also employs high efficiency PM motor control algorithm based on a quadratic load curve stored in internal ROM. 16 possible curves are selectable.

The IRDM983-025MB, IRDM983-035MB have an on-chip voltage regulator to derive the 3.3V, required by the digital logic, from the 15V (VCC15) supply. The 3.3VDC regulated voltage pin is available externally for connection to Hall-effect sensors. The IC provides low power standby (less than 7mW) mode of operation that 3.3V power is cut off when VSP (Voltage Set Point) becomes less than 1.15V to provide further power efficient operation.

An integrated A/D Converter is used to acquire EFF Parameters, temperature (internal temperature sensing), and the VSP input that sets the motor duty command. An internal temperature sensor is interfaced to the ADC and resulting digital conversion data is used to control the dynamic over-current set-points as well as max over-temperature limit.

The IRDM983-025MB, IRDM983-035MB protections include a supply under-voltage lockout (3.3V and 15VDC), over-speed protection, over-temperature limit and Over-current limitation protections. The reset circuitry includes a Power-On reset block and a reset input.

All devices do not require any programming. Default coefficients and system parameters are stored in internal ROM. The EFF input pin, used to adapt to specific motor and load to improve efficiency, can be used by means of two resistor pairs to choose one of 16 pre-stored load curves in ROM. DIR is a digital input pins which specify the motor direction command (CW or CCW). The PGSEL and DIR are digital input pins which specify speed feedback type (1 or 3 pulses per electrical revolution) and the motor direction command.

The IRDM983-025MB, IRDM983-035MB has an on-chip PLL to generate internal clocks. The PLL requires an external low frequency reference clock (32768 Hz). The clock can be provided through an RC or a low-cost crystal (typically used in wrist-watches).

The IRDM983-025MB, IRDM983-035MB integrates high and low side gate drivers for applications up to 500V, it includes integrated Bootstrap diodes, and six power MOSFETs. The simplified block diagram is shown in Figure 1.1 in terms of hardware elements while the control elements are depicted in Figure 1.2 in the following pages.

Simplified Block Diagram

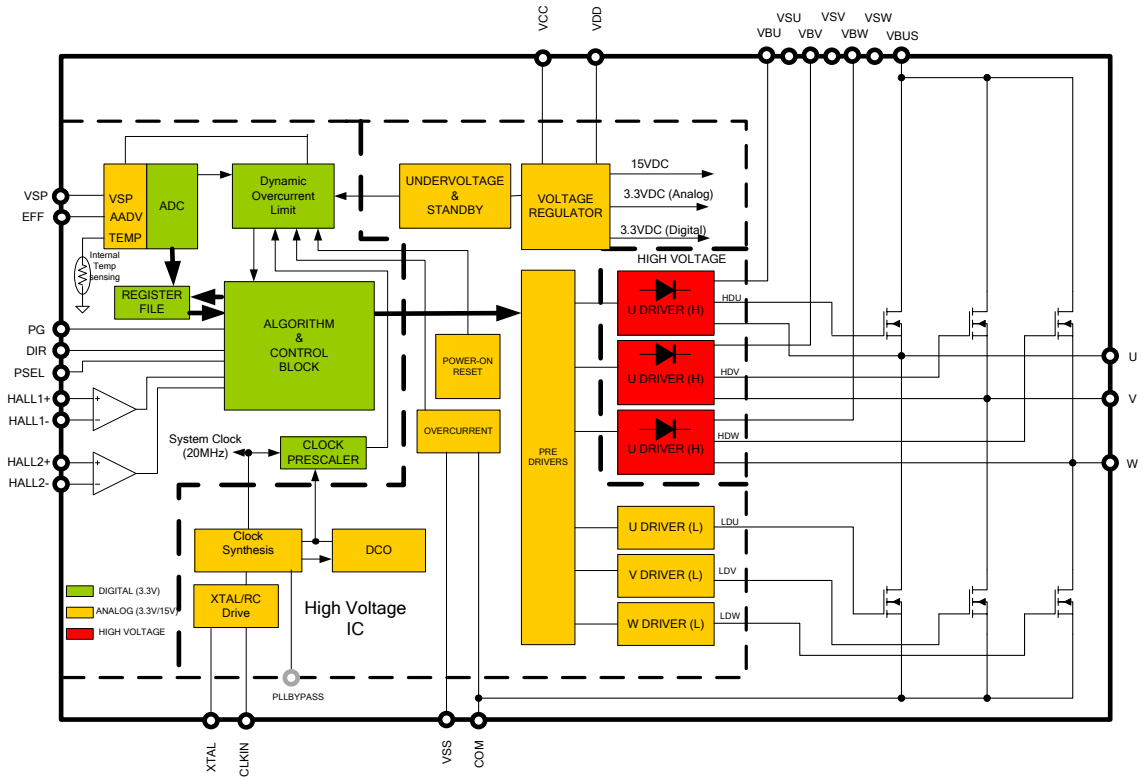


Figure 1.1 Simplified Block Diagram

Control Block Diagram

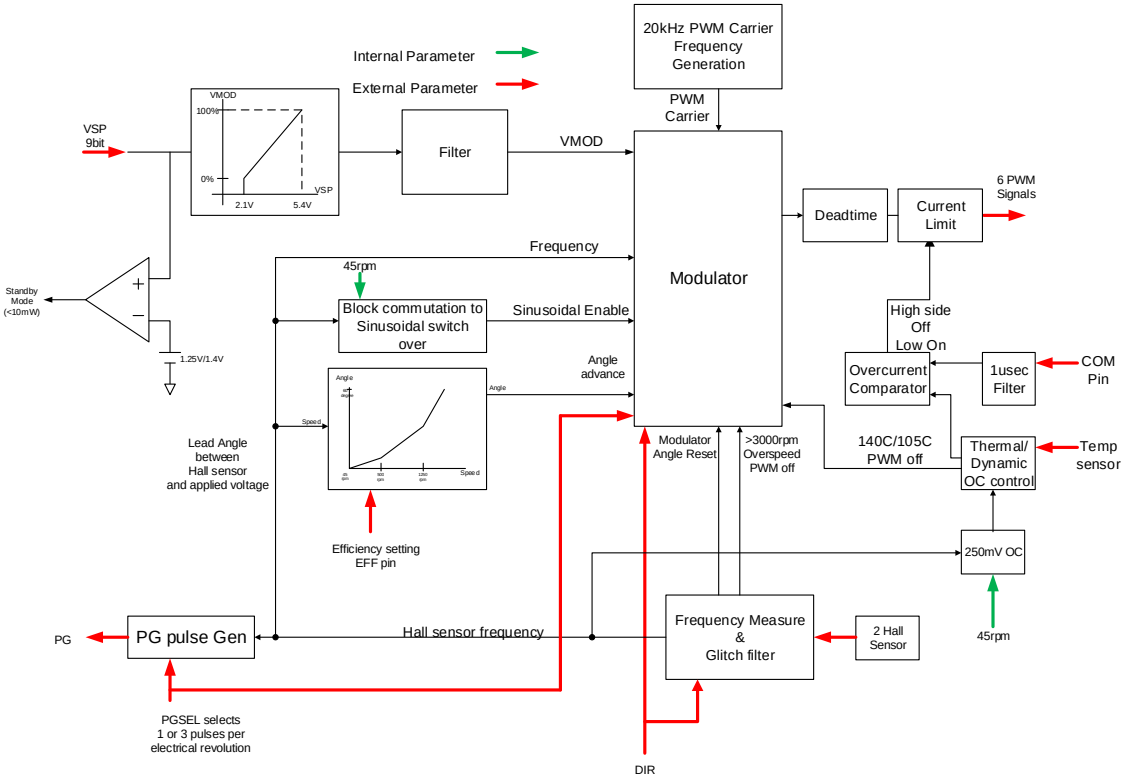
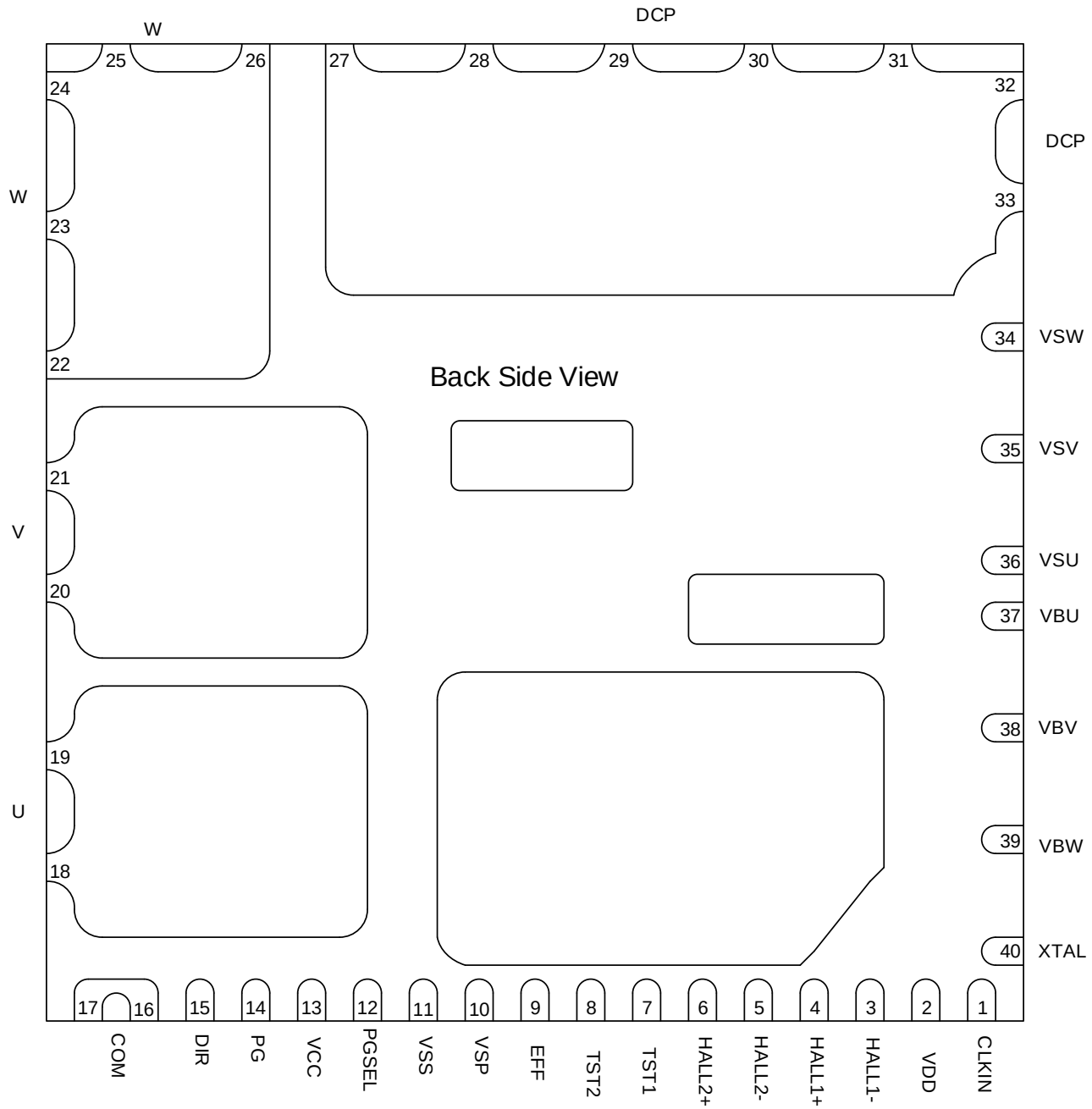


Figure 1.2 Control Block Diagram

2.0 Lead Definitions

Symbol	Pin #	Description
VSP	10	Voltage Set Point analog input. Provides the value of the PWM modulation index to the controller.
PG	14	Provides speed feedback to through pulsed per revolution. It is an open drain output 15V tolerant.
DIR	15	Motor Direction Input (internally pulled up high = U→V→W)
EFF	9	VoltageCurveGain Parameter Input
XTAL	40	Clock buffer output
CLKIN	1	Clock buffer input
VSS	11	Logic ground
COM	16,17	Analog input ITRIP and power ground and low side MOSFET source
VCC	13	15V Supply Voltage
PGSEL	12	Pulses per revolution select (Internally pulled up high = 12 pulses per revolution on a 8 poles motor)
HALL1+	4	Hall sensor U positive input
HALL1-	3	Hall sensor U negative input
HALL2+	6	Hall sensor V positive input
HALL2-	5	Hall sensor V negative input
TST1	8	Pin for factory testing – connect to VDD in normal application
TST2	7	Pin for factory testing – connect to VSS in normal application
VDD	2	3.3V output
U	18,19	U phase output
V	20,21	V phase output
W	22,23,24, 25,26	W phase output
VBU	37	Phase U High side Bootstrap capacitor positive
VBV	38	Phase V High side Bootstrap capacitor positive
VBW	39	Phase W High side Bootstrap capacitor positive
VSU	36	Phase U High side Bootstrap capacitor negative
VSV	35	Phase V High side Bootstrap capacitor negative
VSW	34	Phase W High side Bootstrap capacitor negative
DCP	27,28,29, 30,31,32, 33	DC Bus voltage

Lead Assignments



3.0 Peripherals and Inputs/Outputs

The IRDM983-025MB, IRDM983-035MB have several on-chip peripherals including: A/D Converter (for conversion of the analog inputs: VSP, internal temperature and EFF. This section provides the description of the main features and each pin functions.

3.1 VSP Analog Input pin

The VSP input has a triple purpose. One is the analog input representing the amount of duty of PWM output signal which is a part of the Host Processor Interface that includes the signals VSP and PG and DIR. The 2nd mode is a standby mode to reduce power consumption where VSP is less than 1.15V/1.40V (hysteresis). The 3rd mode is a Trap test mode recognition which transfers the system operation to six step modulation mode only for a final motor assembly testing purpose. There are two parallel input paths to the ADC. The VSP input structure is also shown in Figure 3.1.

In the normal operating mode, the VSP input ranges from 0 to 5.0V and converted into 0-511 value range. The converted value (0-511) represents a point in the duty curve. At VSP=1.9V which corresponds 0% duty and internal ADC value=199.

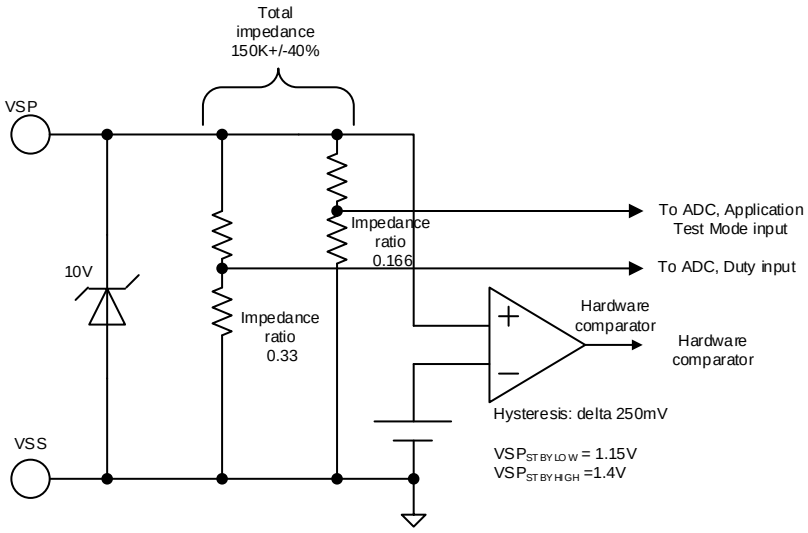


Figure 3.1 VSP Input structure

A motor start/stop command is issued based upon the value of the VSP input. The converted value is compared against a fixed threshold. The threshold is set to 1.9 V. For any values of VSP below the threshold the PWM modulation will be 0% and all gate drivers are off.

The motor will run with VSP above the threshold 1.9 V and the duty saturates beyond 5.0V.

When VSP <1.15V, then the system goes into a standby mode where all internal circuitry is basically shut off.

The VSP pin has a typical input impedance of 150K ohm. With an external 1kohm series resistor, the VSP input may sustain the voltage exceeding a 10.0V with a condition that the input current is within 10mA. However, the exceeding amount voltage beyond 10.0V is not guaranteed under any conditions.

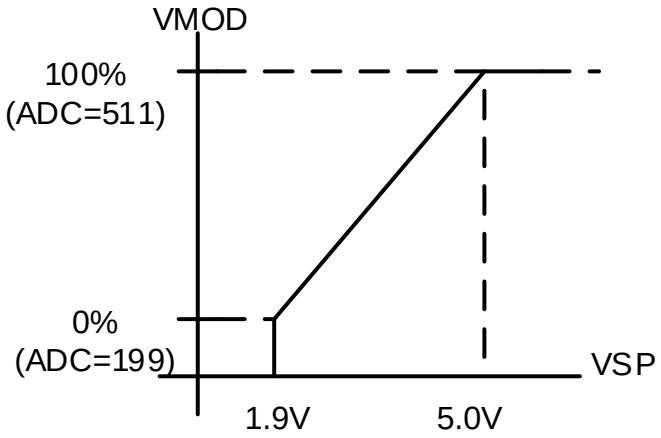


Figure 3.2 VSP Range and Thresholds

VSP standby description

When VSP becomes less than 1.15V, the system goes into the standby mode and all circuit except a few analog circuits are powered off. Basically it disengages internal and external 3.3V power supply and wait for the system to become active.

When VSP becomes less than 1.15V, the system waits for 5 seconds before entering the standby mode. (See Figure 3.4)

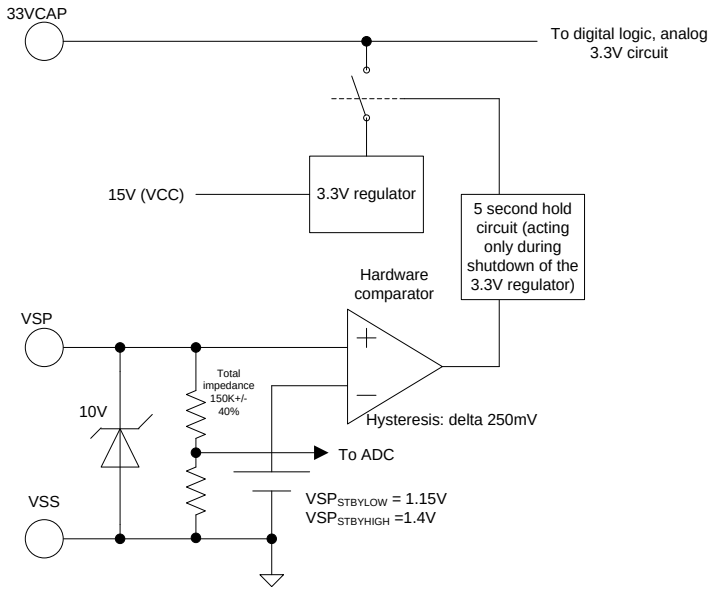


Figure 3.3 VSP standby and simplified analog circuit

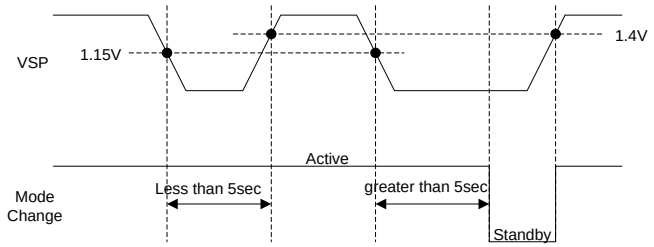


Figure 3.4 VSP stand by to active mode example

Once the system goes into a standby mode, all digital power and 3.3V analog power are shut off and only comparator circuit to monitor VSP analog input voltage is activated. In this standby mode, typical power consumption will be at around 7mW. Once VSP becomes above 1.4V, then the system becomes active as all digital and 3.3V analog circuits are activated.

VSP Trapezoidal (6 steps) Test Mode

VSP input can change the normal operating mode to the Trap Test Mode. As per Figure 3.1, there are 2 channels to monitor Vsp input signal. The mapping of the 2 Vsp channels is as follow:

- One channel is mapped as [0V 5.0V] to [0 511] and it is used for normal operating mode voltage set point.
- The other channel is mapped as [0V 9,9V] to [0 511] and it is used to detect the request to enter in specific trapezoidal (trap) test mode.

The used threshold to enter the trap test mode is 8.8V converted to digital number 454.
The algorithm is described in the following steps:

1. To enter or exit the trap test mode, a counter is used to count ADC conversions where Vsp is greater or lower than the threshold of 8.8V (454).
2. When in normal mode, if 1376 consecutive ADC conversions are greater than 8.8V (454) then the system enters in trap test mode
3. When in normal mode, if at least 1 conversion is below the 8.8V (454) threshold then the counter to enter test mode is reset and the system stays in normal mode
4. When in Trap test mode, if 551 consecutive conversions will be lower than 8.8V (454) then the system exits test mode and reverts back to normal operating mode
5. When in Trap test mode, if at least 1 conversion is above the 8,8V threshold then the counter to exit test mode is reset and the system stays in trap test mode

Here are some remarks regarding the algorithm to enter the trap test mode:

1. During Trap test mode entering the DcBus should be properly set to 0V. Because the system is in normal mode and will react to Vsp maximum value.
2. 1376 scans mean 500 ms. In fact each scan of the ADC takes 363.3 us. So to enter trap test mode, Vsp must be greater than 8.8V for more than 500 ms.
3. 551 scans mean 200 ms. This means that to exit trap test mode Vsp must be lower than 8.8V more than 200 ms.
4. The reference voltage of the ADC is the most important source for the threshold accuracy that is roughly +/-10%. Example Threshold at 8,8V (= 454 raw number) is min 8,0V and max 9,68V

These following numbers have been put to the metal option area (described in the appendix) so they could be changed by changing one metal layer only:

a. threshold (454)
b. timing thresholds (1376 and 551)
c. possibility to disable completely this function

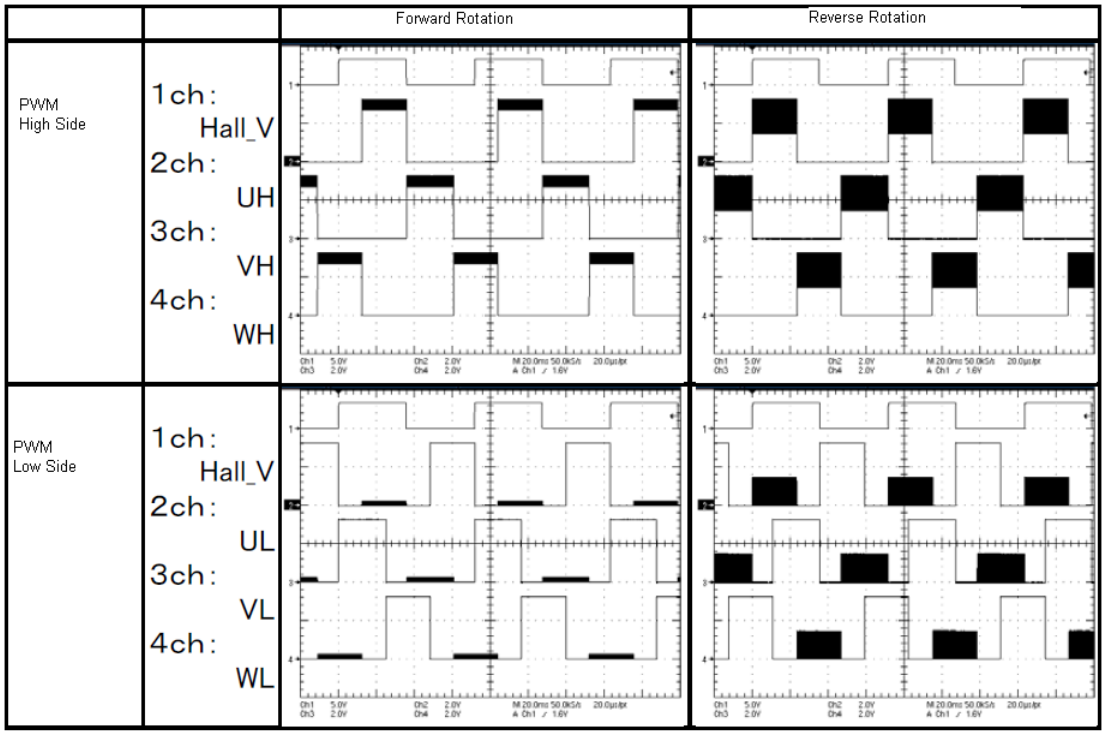


Figure 3.5 Trap test mode modulation

The modulation in trap test mode is shown in figure 3.5 where DIR = 1. In the figure both forward direction and reverse rotating direction cases are shown.

The modulation depends on the speed in the forward direction and depends on motor poles number.

- Modulation initially is 80% (effective 78% considering the dead time)
- Modulation changes from 80% (effective 78% considering the dead time) to 95% (effective 93% considering the dead time) when motor speed becomes bigger than 45 rpm in forward direction (according to DIR pin setting)
- For 8 poles motor, modulation changes back from 95% to 80% when motor speed becomes lower than 24 rpm in forward direction (according to DIR pin setting)
- In reverse direction, modulation is always 80%

In Figure 3.6 an example of duty depending on the speed is shown for DIR=1.

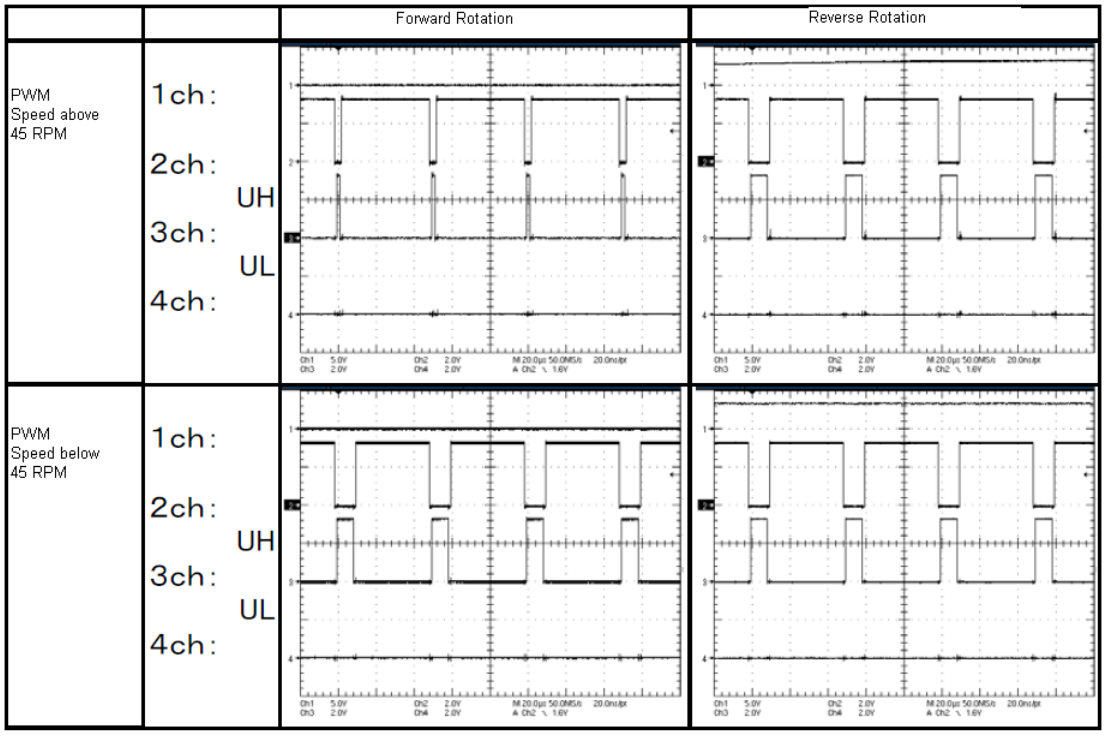


Figure 3.6 Duty in trap test mode depends on forward speed

VSP signal path to PWM

The detailed signal path of VSP is shown in Figure below. VSP starts with analog input to ADC block followed by filtering and averaging process, and final PWM block. The data range and each function units are described in this Figure.

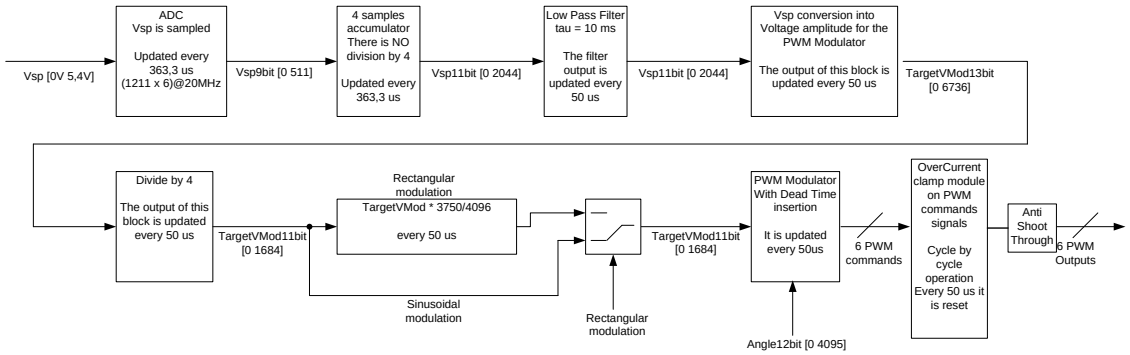


Figure 3.7 VSP signal path

Between the ADC and PWM block, there are two filtering blocks as shown in the following Figure. The 4 times moving average filtering eliminates a potential PWM blanking due to internal stop action followed by start when internal filtered VSP becomes less than a digital corresponding value of 199 to analog VSP=1.9V and immediately recover to start condition. Four registers are updated at each 363.3usec conversion of VSP input which is a part of consecutive six channels conversion by 20MHz clock (each conversion takes 1211 clock cycles). At each VSP register

update, synchronization to ADC section takes place with two filtering blocks, namely 4 times averaging and 10msec filter block, by 20 kHz clock domain. The start and stop internal command is issue at the output of 10msec digital filter based on the certain digital value.

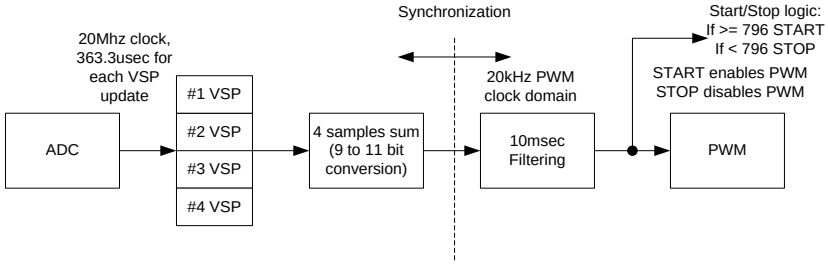


Figure 3.8 VSP digital filtering

There is a functional block named “VSP conversion into Voltage amplitude for the PWM modulator”. This block converts VSP 11 bit value into usable digital form of Voltage command for PWM modulator at every 50us update rate. The detailed signal flow inside of this functional block is shown in Figure 3.9. The output signal of this functional block is called TargetVMod and 13bit data range.

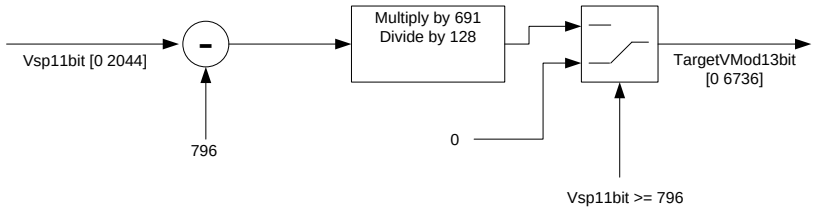


Figure 3.9 VSP conversion to PWM voltage command

PWM modulator

Figure 3.10 shows the PWM modulator which receives the voltage command and angle command from the previous functional blocks. The modulator is based on the Space vector modulation scheme with a two phase modulation. This module employs one Cordic rotator (multiplexed and used twice per cycle) to perform trigonometric function of sinusoid followed by the TimeCalculator which produces two active vectors time period amplitude aligned with a given 60 degree quadrant, namely HalfTa and HalfTb. These two active vector time periods, HalfTa and HalfTb, summed to HalfT0 give half of the PWM cycle period (25 microseconds). HalfTa, HalfTb and HalfT0 are fed to Compare Generator block which generates time instance of the gate signal event as a result of carrier frequency up/down counter comparison. The deadtime is inserted also by this functional block. The final element of PWM modulator is Minimum Pulse Width on High Side Limiter which eliminates the high side pulse width smaller than 400 nanoseconds.

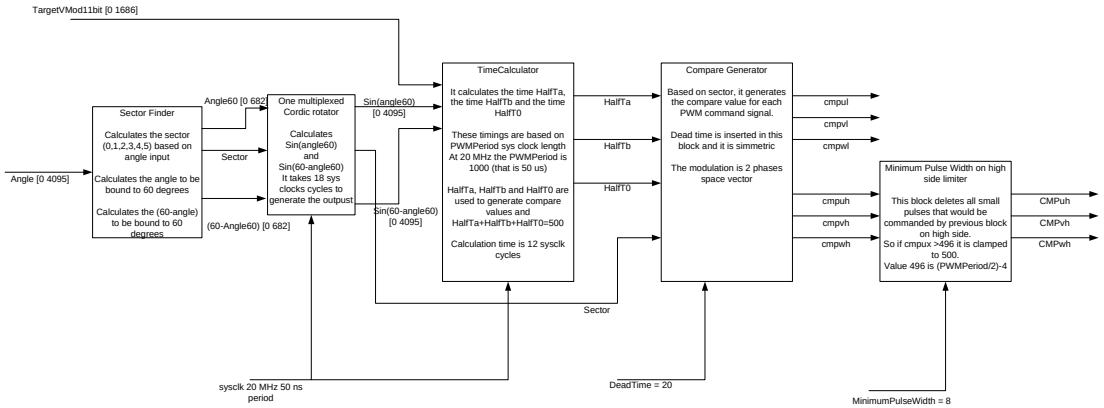


Figure 3.10 PWM modulator detailed block diagram

3.2 Temperature Sensing

The IRDM983-025MB, IRDM983-035MB have an internal temperature sensor. It updates at every 363,3usec and selects appropriate overcurrent threshold value which goes into the hardware over-current limit comparator (see below Figure).
This logic described below is the over-temperature limit control at a temperature below 100C degree. The conversion equations from temperature to digital ADC value are:

$$ADC_{OUT} = 0.532 \times (T_C + 273.15)$$
$$T_C = (ADC_{OUT} / 0.532) - 273.15$$

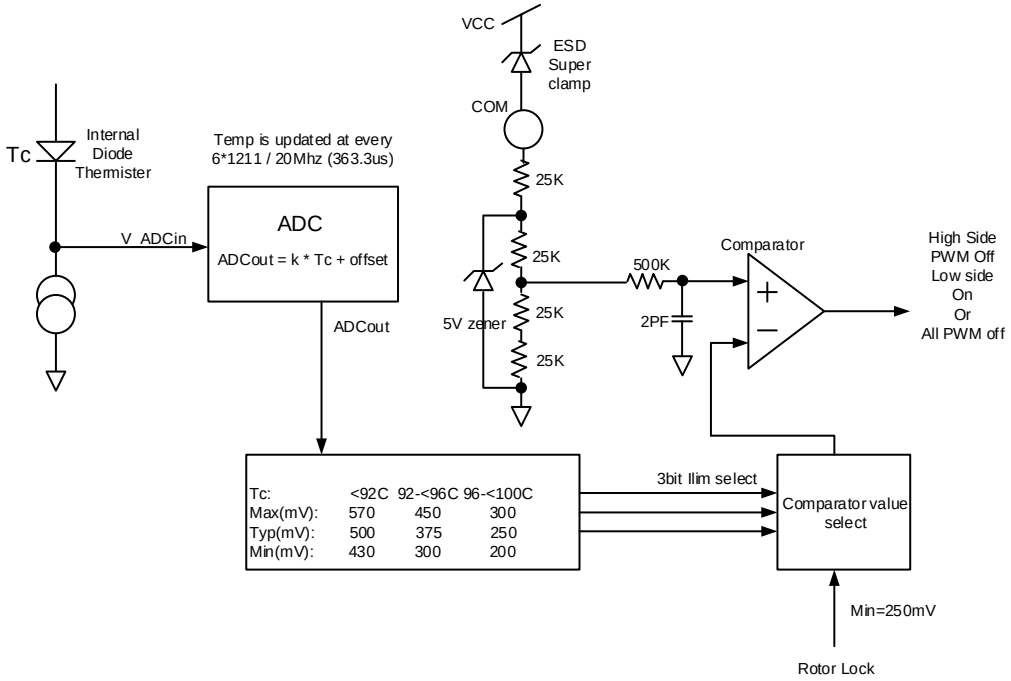


Figure 3.11 Internal Temperature Sensing Structure and Current Limit

Tc	<92C	between 92-96	between 96-100
Min (mV)	570	450	300
Typ (mV)	500	375	250
Max (mV)	430	300	200

Figure 3.12 Internal Temperature Sensing Structure and Current Limit IRDM983

Over-temperature processing

Over-temperature fault turns off PWM completely so long as the sensed temperature exceeds 100C Celsius degrees. When over-temperature is engaged, there is a hysteresis to disengage over-temperature at 80C degree. Temperature acquisition to ADC is updated every 363,3 usec at 20MHz as a part of six channel ADC conversion. Once converted to ADC value, it is checked against a window limiter and if exceeds its limit which are 160C and -40C boundary, the converted value is discarded and do not pass to the next registers. Once passed the limit-rejecter, the value is transferred to four FIFO registers and passed on to the preceding digital control algorithm section by synchronization logic. In the algorithm section, four TEMP values are averaged followed by a 10msec digital filter by 20kHz clock operation. Then it is passed to eight consecutive PWM periods to further qualify the over-temperature condition. All this process is described in the following Figure.

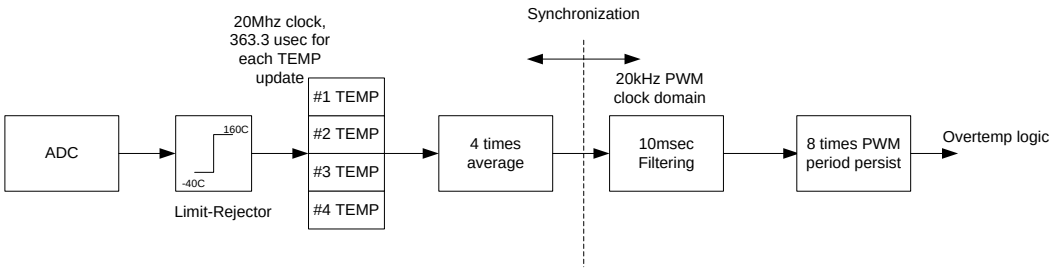


Figure 3.13 Overtemperature processing

3.3 Hall sensor interface pins, Commutation and PWM

The IRDM983-025MB, IRDM983-035MB has direct interface pins for two Hall sensors. The Hall sensors are non-buffered type and have a differential output. The IRDM983-025MB, IRDM983-035MB are designed to work with particularly HW-101A by Asahi Kasei Microdevices. Each differential Hall signals are buffered by high gain operational amplifier with a preceding 1.5usec analog filter shown in Figure below. The third Hall sensor signal Hall 3 (or Hall W) is virtually generated.

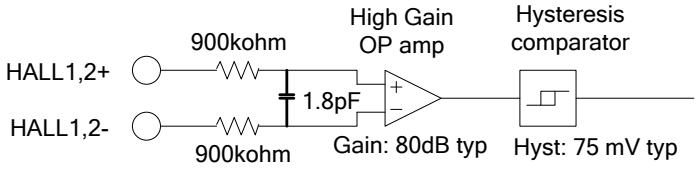


Figure 3.14 Hall sensor input circuit

Two Hall sensor input signals go through multiple stage of digital filtering shown in Figure 3.15. The first stage of digital filter is based on the 20MHz counter to continuously count up to 60 counts to qualify the signal. The U', V', and W' are the filtered signals in Figure below. Then this signal is fed to the qualification filter (Figure 3.16) which further qualifies the Hall input signal by eliminating noise and multiple bouncing signals at a transition. The signal U", V", W" are the qualified signal in Figure and used for sinusoidal two phase SVPWM and speed information generation.

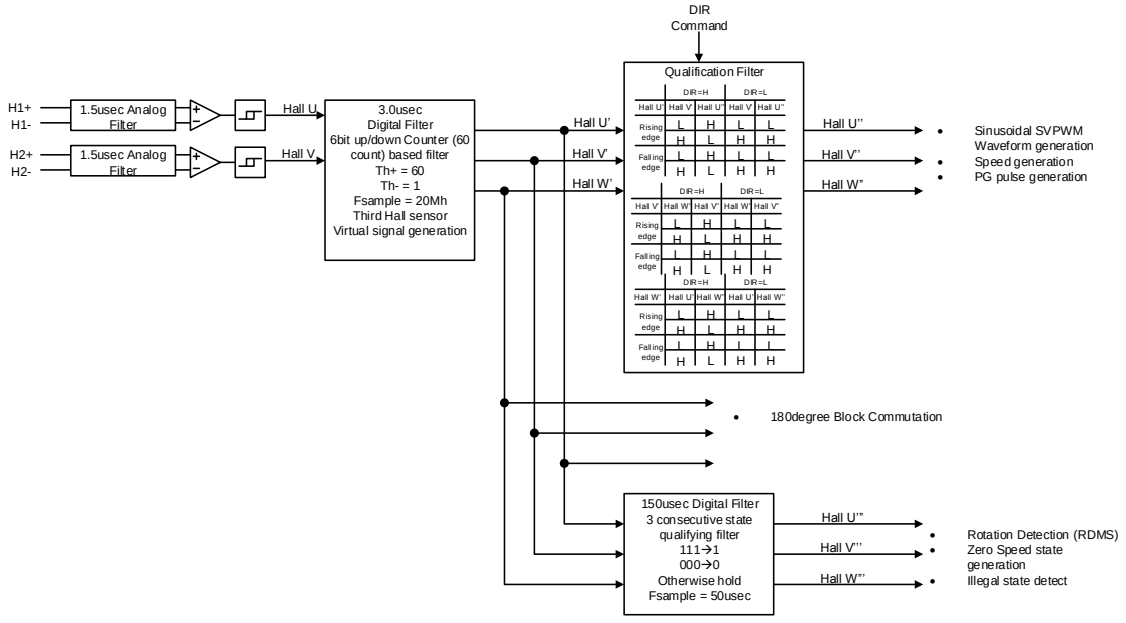


Figure 3.15 Hall sensor input filtering

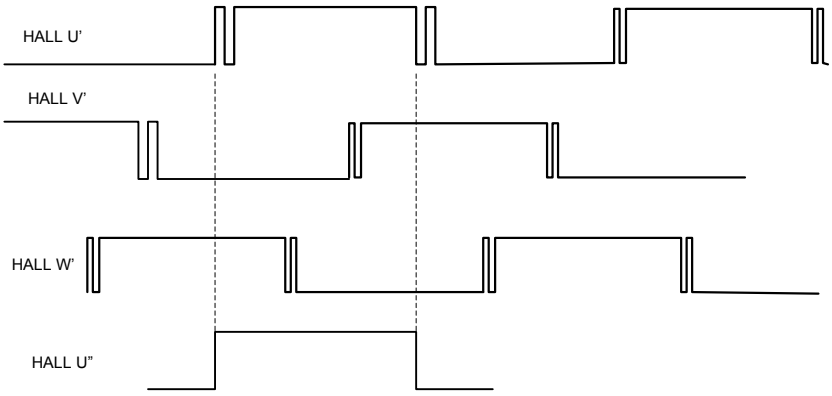


Figure 3.16 Hall sensor input qualification filter

3.4 Block commutation within +/-45rpm

At starting a motor, up to 45rpm toward the same direction of DIR pin state, the IRDM983-025MB, IRDM983-035MB operates by a block commutation mode based on the Hall signal U', V', and W'. When motor rotates reverse and opposite direction of DIR pin state, then regardless of the motor speed, the PWM operation is based on a block commutation. Figure 3.17 shows the speed range where a block commutation applies as indicated arrow lines depending on a DIR state. These signals are filtered by 150usec digital filter with 50usec sampling as shown in Figure. These signals are also used for identifying an illegal state such as (000) or (111) Hall state and rotation detection. The block commutation signal waveform are shown in Figure 5.3.3 and Figure 5.3.4 and based on half cycle PWM while positive voltage (180degree) applied to a motor with 30 degree phase leading to the CEMF phase to neutral signal.

The PWM duty of block commutation is always 80% of commanded VSP.

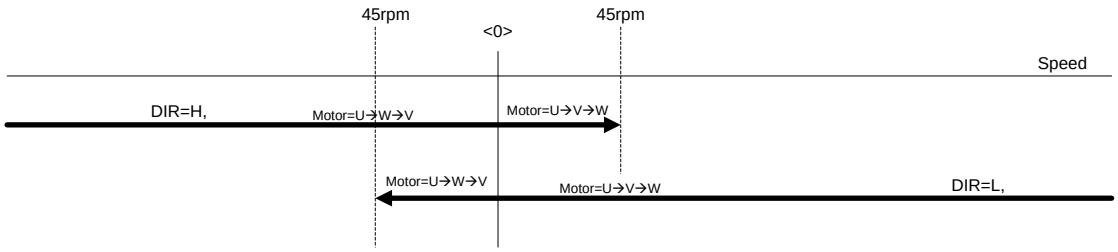


Figure 3.17 Block commutation speed range

Transition to/from Block commutation

When the speed, measured by hall sensor V (H2) falling edge to falling edge, reaches above 45rpm, a transition occurs and it switches to a two phase SVPWM. This transition is based on the speed measurement by the Hall V" falling edge to falling edge (one electrical revolution) and occurs if speed measurement becomes above 45 rpm by one speed measurement. When the period between 2 adjacent Hall sensors edge changes, that is 60 degrees sector period becomes bigger than 102,7 ms, thus indicating a speed lower than 24,3 rpm for 8 poles motor and 19,5 rpm for 10 poles motor, a transition from 2-phase SVPWM to block commutation occurs.

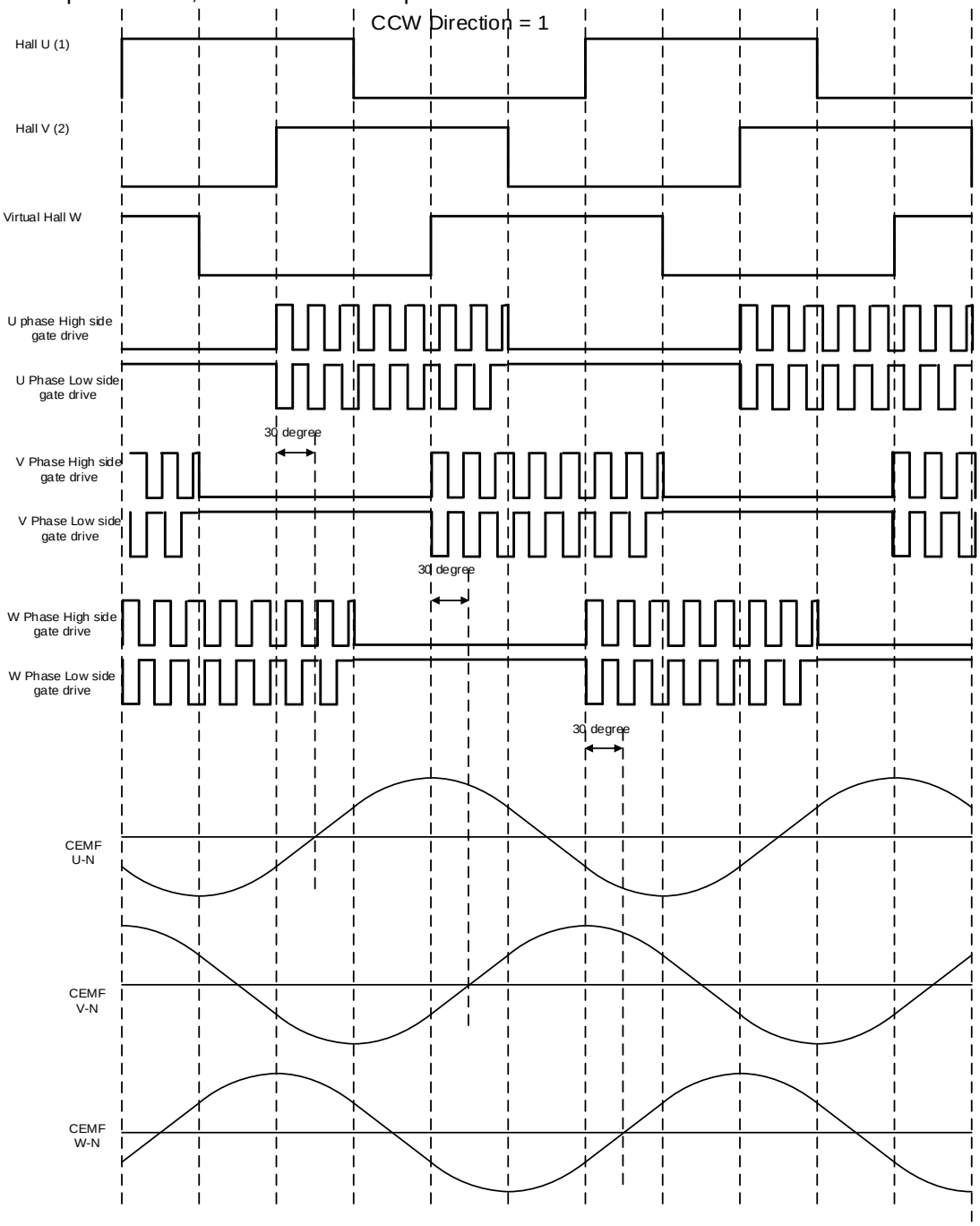


Figure 3.18 Block Commutation – CCW, DIR=high

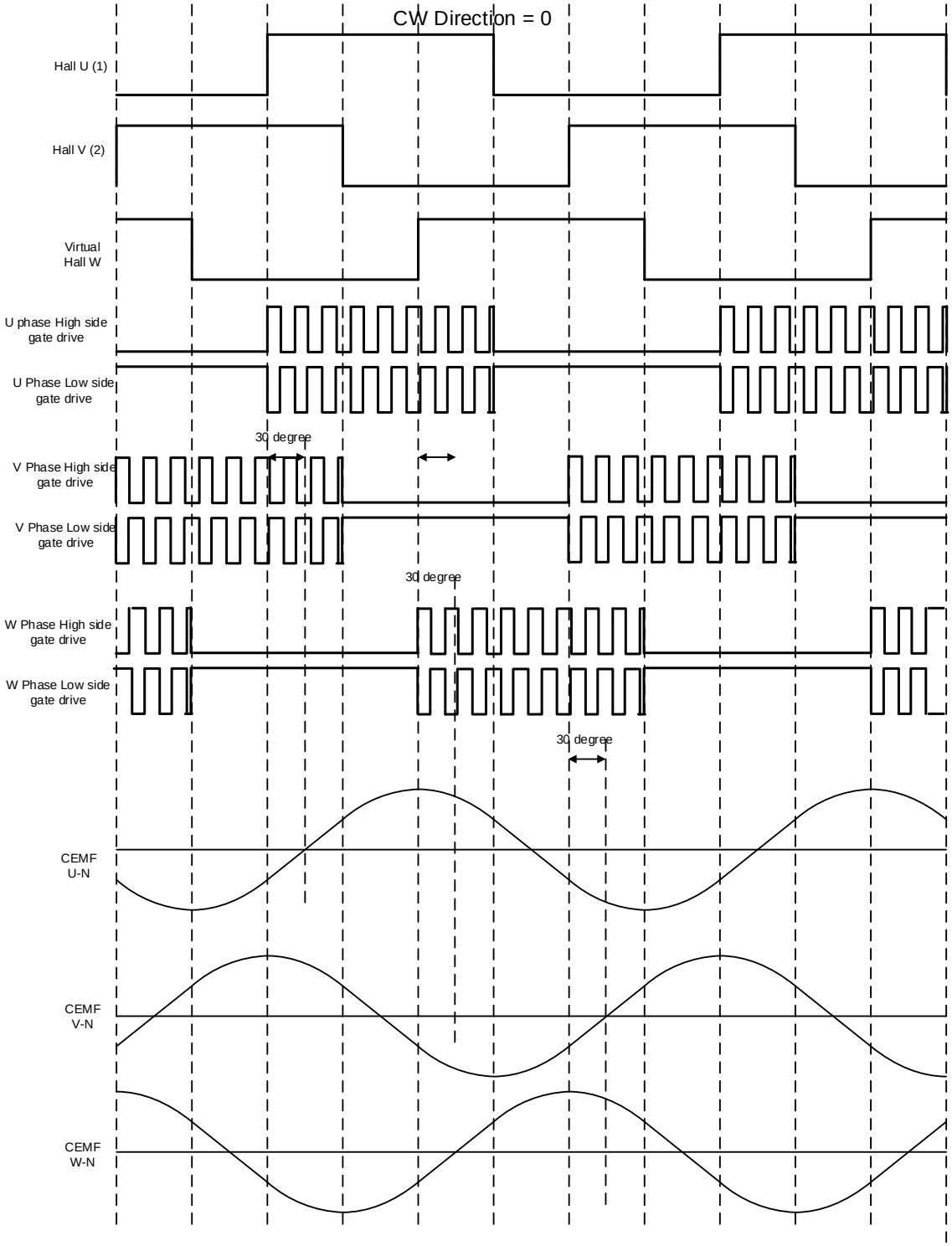


Figure 3.19 Block Commutation – CW, DIR=low

3.5 Sinusoidal two phase SVPWM

Above 45rpm, PWM modulation becomes a sinusoidal two phase SVPWM. In the two phase SVPWM modulation, commutation update occurs every 60 degree quadrant based on the Hall signal input, more specifically Hall signal filtered by a qualification filter described in the section 5.3.
If the current 60 degree period is longer than the previous period, the current commutation and duty is placed on hold beyond the previous period. On the opposite side, if the current 60 degree period is shorter than the previous period, then the commutation and duty update occurs at exact event time of the 60 degree quadrant before reaching to the previous 60 degree period. (see Figure 3.21)

Each 60 degree period measurement is performed by 16-bit timer/register clocked by 625kHz and 20kHz PWM carrier frequency period is clocked by a 20MHz internal clock yielding 1000 count resolution per carrier frequency period.

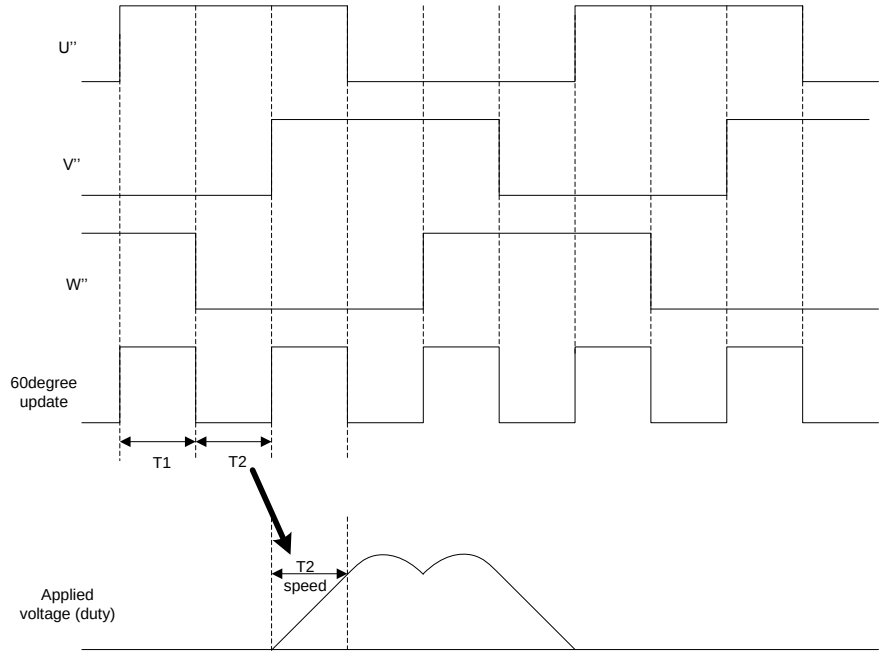


Figure 3.20 60 degree commutation update

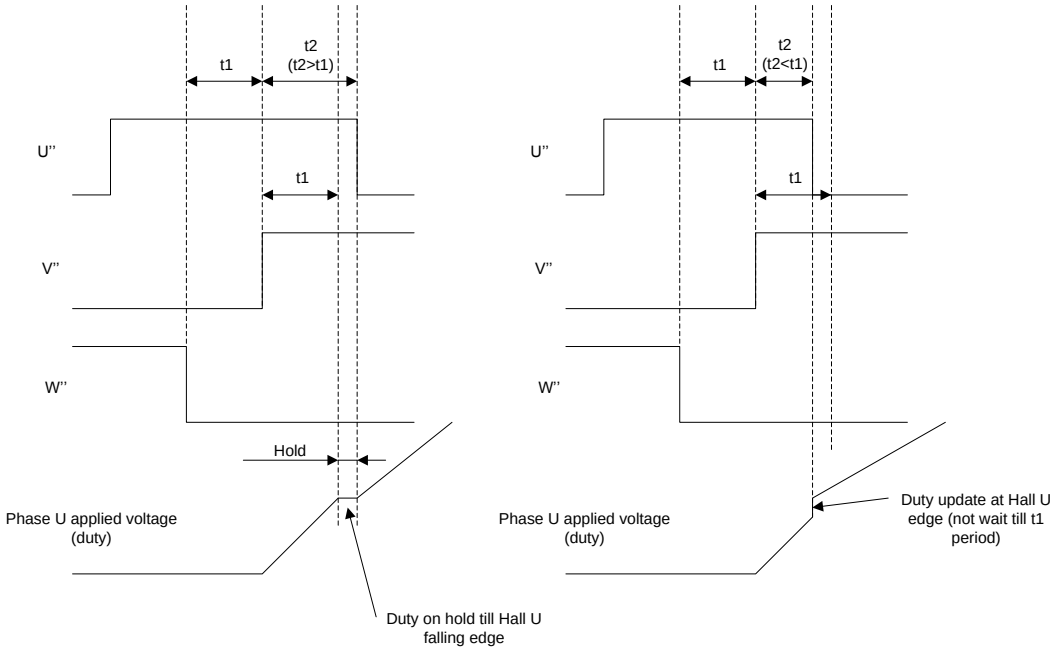


Figure 3.21 60 degree commutation update

The RPM speed measurement is done by the phase V Hall (2) sensor falling edge to falling edge based on the qualified filtered Hall V (2) signal (V"). The period is measured with a 20bit register at 625kHz. This speed information is used by the following areas and functions:

- Speed information to switch from square wave commutation to sinusoidal commutation after 1 measure above 45 rpm.
- Speed information to use VSP attenuated at maximum 80% when below 45 rpm.
- Speed information to determine over-speed > 3000 rpm (on a 8 poles motor).
- Speed information used in the stored look up table based on EFF parameter.

3.6 Rotation Detect

When the motor rotation changes, the rotation detect logic ensures a smooth rotation change including zero speed detection. In particular, when the motor shaft is locked and it vibrates around zero speed between forward and reverse rotation, it is essential that the motor control logic asserts proper zero speed states to alleviate any oscillation during a locked rotor condition.

Figure 3.22 shows the basic block diagram of rotation detect logic. In the qualification filter, it uses the 3-prime signals (U"', V"', W"') which are filtered by 3 x 50usec time constant based on the U', V' and W' signals (see Figure 3.12). The state machine logic is described by the truth tables shown in Table 3.1, Table 3.2, and Table 3.3 and each tables generates RDM signals at the transition edge depending on the state of other 3-prime signals (U"', V"', W"') and DIR signal. RDM and RDMM are the signals used for generating zero speed state as well as forward/rewind state as shown in Figure 3.23, 3.25, 3.26 and 3.27.

RDM (Rotation Direction Monitor) is the signal which logic state is generated by AND of RDM-U, RDM-V and RDM-W. RDM changes its state if persisting two consecutive samples at each U"',

V’’’, W’’’ edges. For example, if it persists H and H twice in row, then RDM = H, or if it persists L and L twice in row, then RDM = L. Otherwise it holds the previous state. The meaning of RDM logic states are “L”= Rotate same direction of command / “H”=Rotate opposite direction of command.

RDMS (Rotation Direction Monitor Status) is a tri-state logic signal that “1”= Rotate same direction of command/”0”=Stop/ “-1”= Rotate opposite direction of command. When RDM changes its state, its state becomes STOP state (speed=zero). While STOP state, if persisting three consecutive samples of HHJ or LLL at each Hall U’’, Hall V’’ transition, it becomes 1 (HHH) or -1 (LLL).
When sampling AND signal of each RDM to qualify that there is no change in two consecutive samplings, care must be taken not to sample the before transition of each RDM since RDM changes. Example is shown in Figure 3.28 to avoid false sampling of a wrong state just before transition change of AND signal.

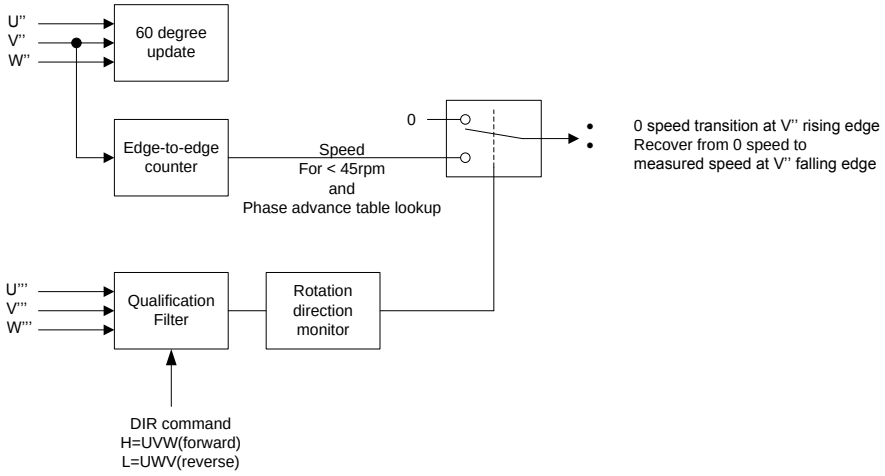


Figure 3.22 RDM signal and rotation detect

Hall U’’’ edge	HALL2’’’	RDM-U	
		DIR=H	DIR=L
Rise	L	L	H
	H	H	L
Fall	L	H	L
	H	L	H

Table 3.1 RDM U signal generation

Hall V’’’ edge	HallW’’’	RDM-V	
		DIR=H	DIR=L
Rise	L	L	H
	H	H	L
Fall	L	H	L
	H	L	H

Table 3.2 RDM V signal generation

Hall W''' edge	HALL1'''	RDM-W	
		DIR=H	DIR=L
Rise	L	L	H
	H	H	L
Fall	L	H	L
	H	L	H

Table 3.3 RDM W signal generation

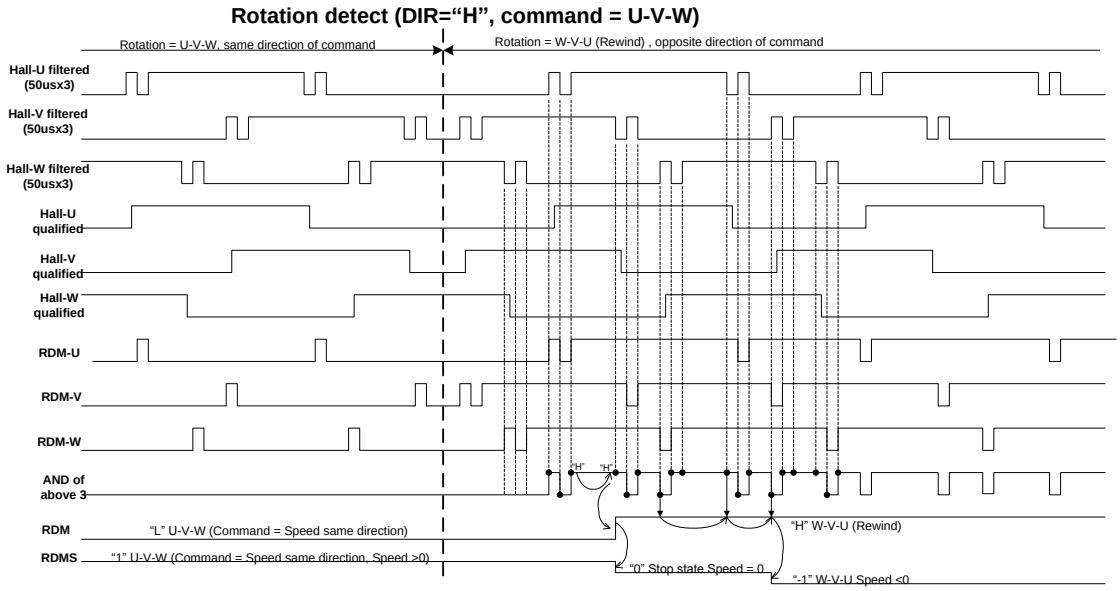


Figure 3.23 Rotation detect (DIR=H, Forward to Reverse)

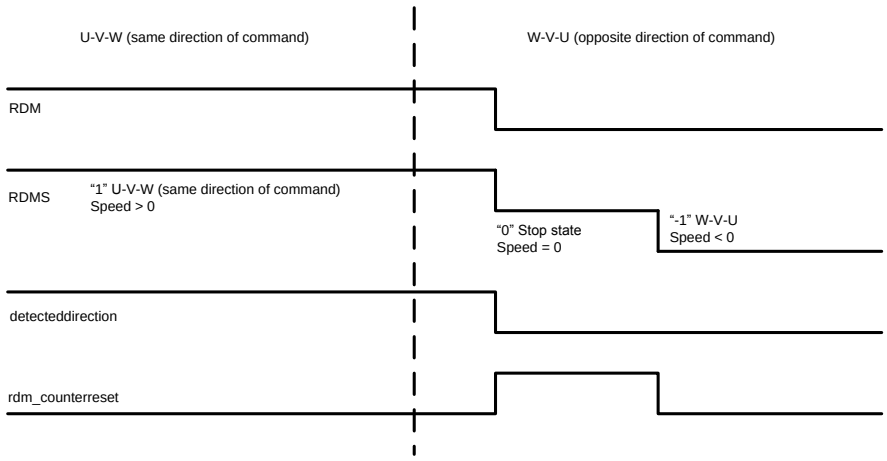


Figure 3.24 Rotation Detect internal signals (DIR=H, Forward to Reverse)

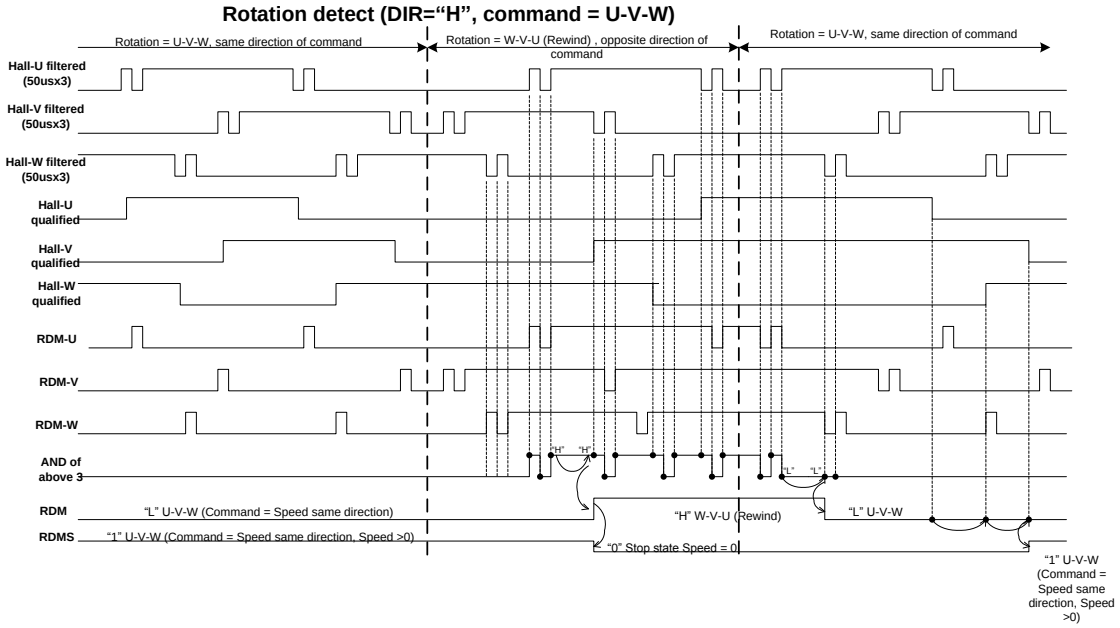


Figure 3.25 Rotation detect (DIR=H, Forward to Reverse to Forward)

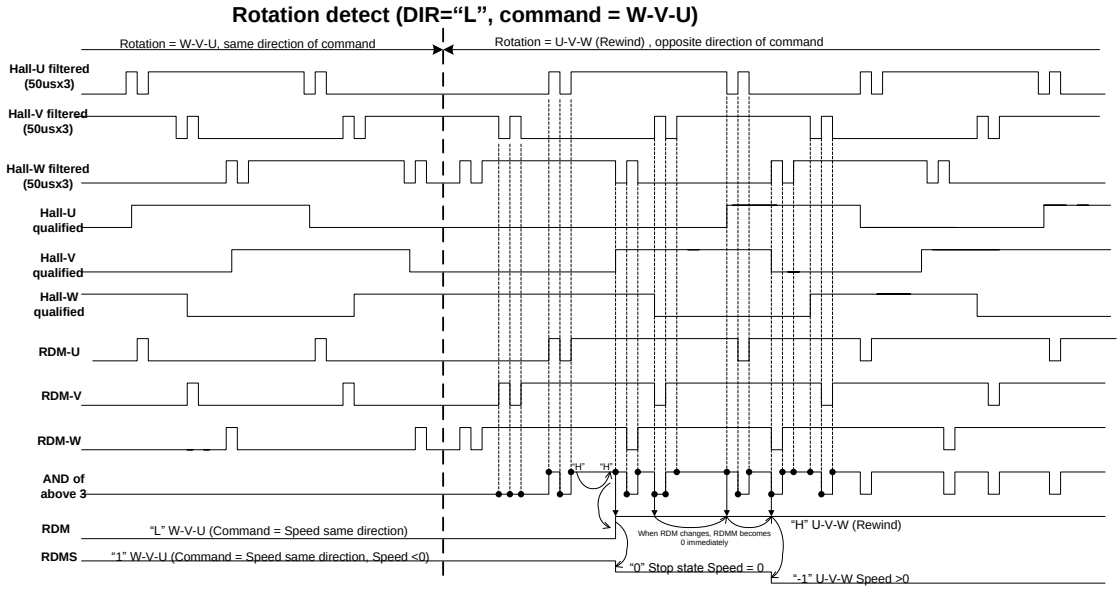


Figure 3.26 Rotation detect (DIR=L, Forward to Reverse)

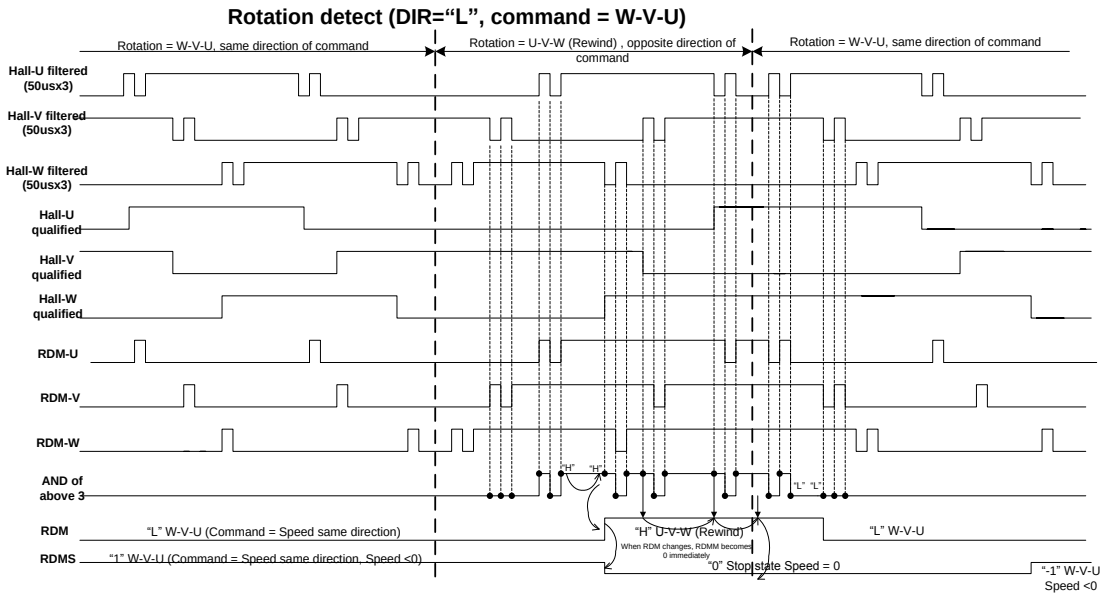


Figure 3.27 Rotation detect (DIR=L, Forward to Reverse to Forward)

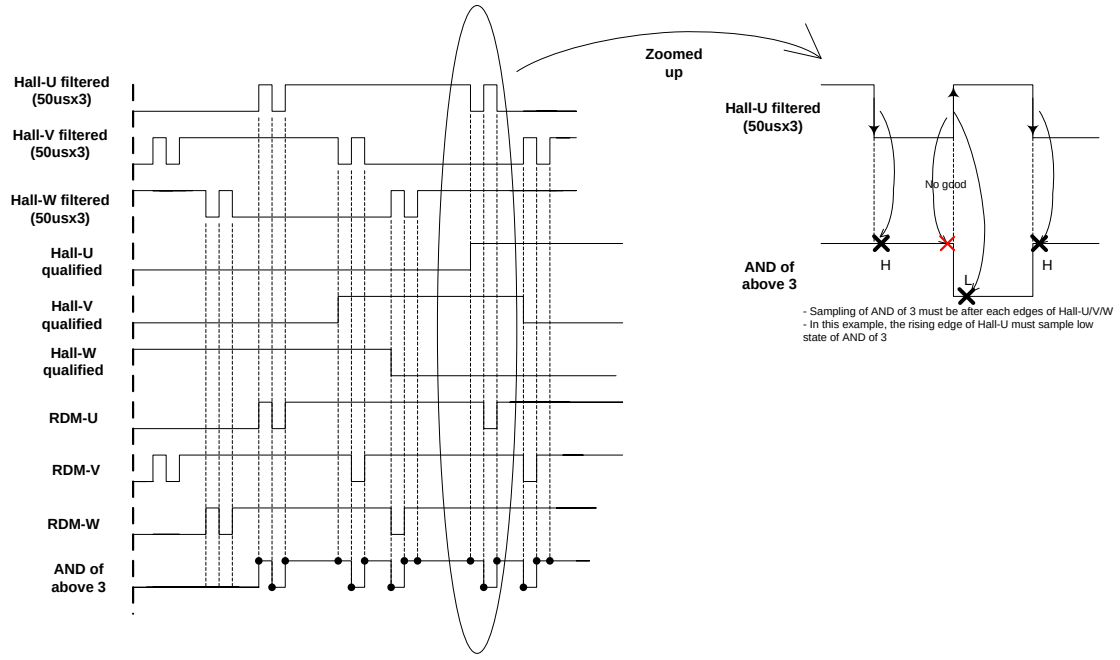


Figure 3.28 Creation of AND signal of RDM-U, RDM-V, and RDM-W

Dynamic DIR change and Rotation detection

A motor needs to stop when changing DIR input. In Figure 3.24 it is shown how physically the signal RDMS is represented inside the digital logic. The RDMS signal is split into 2 digital signals that represent 2 distinct type of information:

- detecteddirection: it represents the direction detected from the Hall signal conditioning and it is obtained as per figure 3.29. The detecteddirection signal is used in the block that manages the transitions between block commutation mode and sinusoidal mode. The same signal is also used in the current limit modules.
- rdm_counterreset: it is a pulse that is used to re-initialize at maximum period the following counters and registers that are used for speed information:
    - Hall V falling edge to falling edge period counter is reset to maximum period (hence speed signal become clamped down to zero)
    - Hall 60 degrees every edge from every edge period counter is reset to maximum period (hence speed signal become clamped down to zero)
    - Reset the Hall V falling to falling edge number of period counter and the cascaded Flip Flop in the block that manages the transitions between block commutation mode and sinusoidal mode.

So the overall effect of these signals is:

- if direction is not equal to detecteddirection, modulation becomes block commutation and the current limit method is different from when the motor is normally rotating in the desired rotation (please refer to over current description)

- if rdm_counterreset is set at 1, all speed information are reset to 0 and the counter and Flip Flop that keep information of actual commutation mode are re-initialised to block commutation mode.

The following figure shows the used algorithm to change from block to sinusoidal (and vice versa) based on speed and on detecteddirection and rdm_counterreset signals.

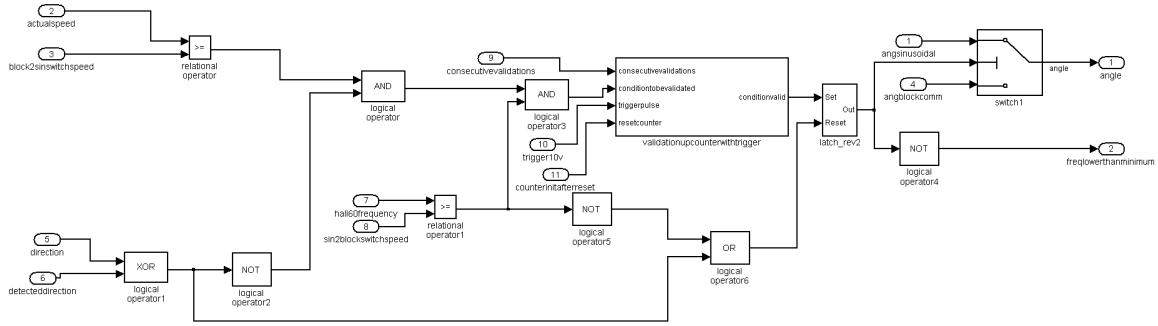


Figure 3.29 Block to Sinusoidal Commutation Validator

As per figure 3.29 in the event of DIR change while motor is running at sinusoidal operation, there will be some delay in RDMS to reflect a change in DIR which causes generation of distorted sinusoidal waveform for a short period of time. This is due to the method that has been used to generate the detecteddirection signal that was designed not considering dynamic DIR changes. An example of the detecteddirection signal is shown in following scope picture where DIR is changing from 1 to 0. In this case an anomalous spike is appearing in the detecteddirection signal causing a wrong modulation for short time period (modulation should be block commutation). To change the direction, the motor must be stopped and then re-started so that the new direction command is latched.

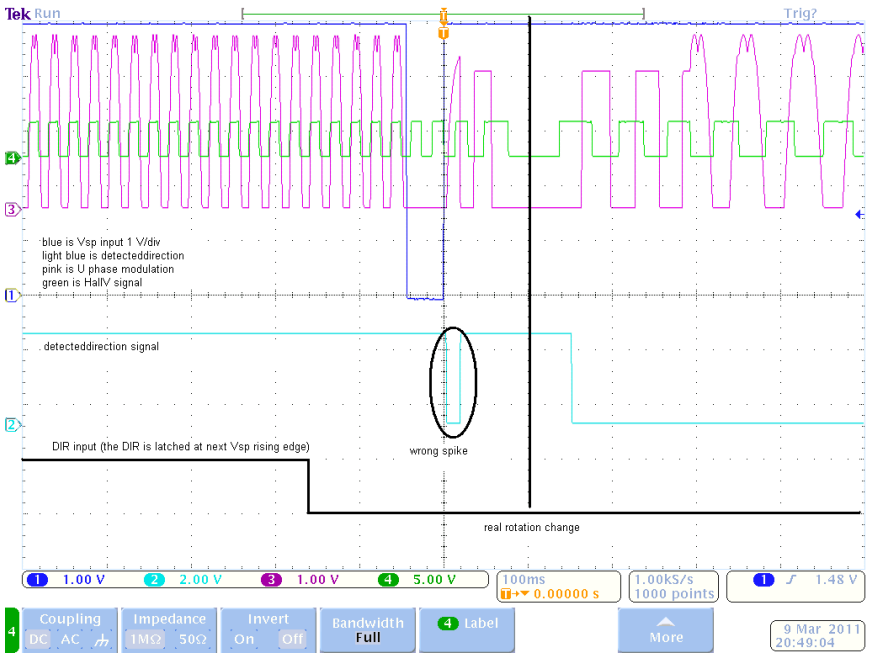


Figure 3.30 Dynamic DIR change

Same applies to next scope picture where DIR is changing from 0 to 1. The anomalous spike in this case is longer, since detecteddirection changes its state before real change of the motor rotation.

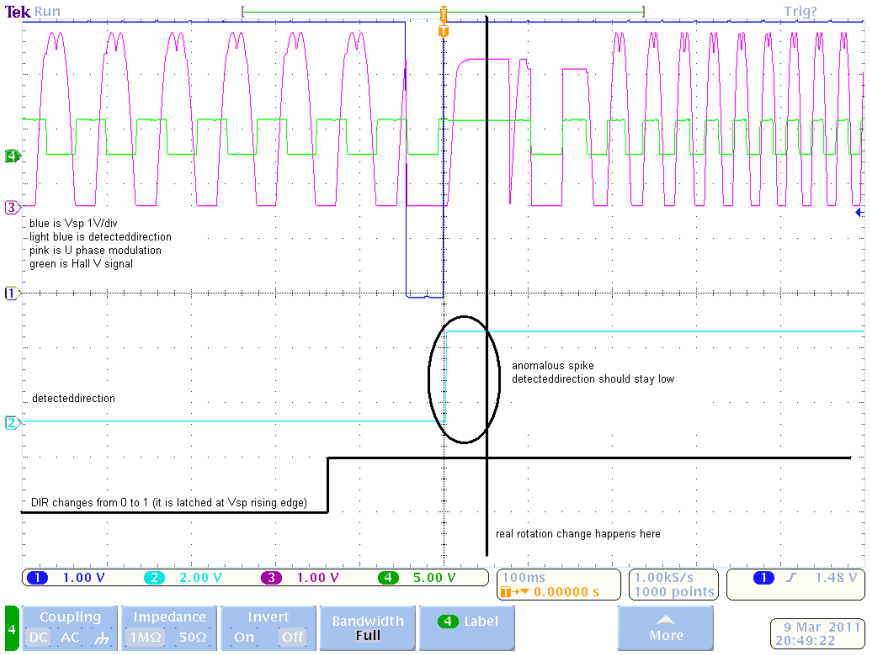


Figure 3.31 Dynamic DIR change

This behavior is known and it is mainly due to the rotation detection logic shown in the next Figure.

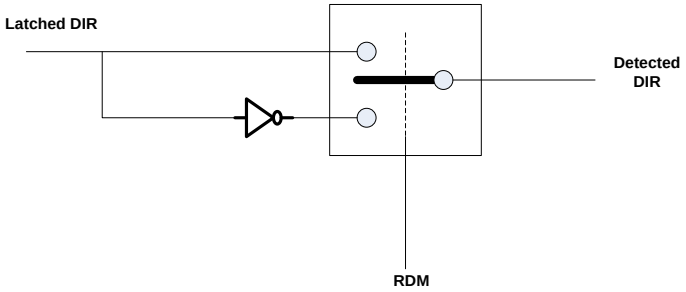


Figure 3.32 Detected DIR

In the event of dynamic change of DIR input, with subsequent new DIR latch due to motor stop and start events, in the moment where detecteddirection is not reflecting the real direction, some distorted sinusoidal modulation waveform may appear (see Figure below). So as a result, to change the direction, the motor must be stopped and then re-started so that the new direction command is latched.

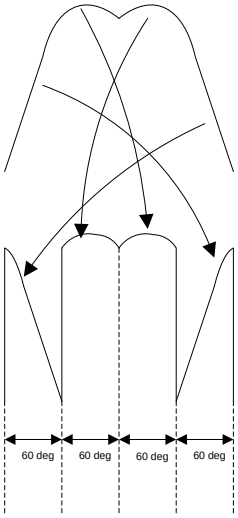


Figure 3.33 Distorted sinusoidal waveform

3.7 COM/VSS pin and Overcurrent limit circuit

COM pin is provided for an external shunt resistor for sensing a motor current on the DC bus. An internal analog filter has 1usec time constant in order to eliminate spike noise appearing on the DC bus current associated with diode recovery of main switches at commutation.

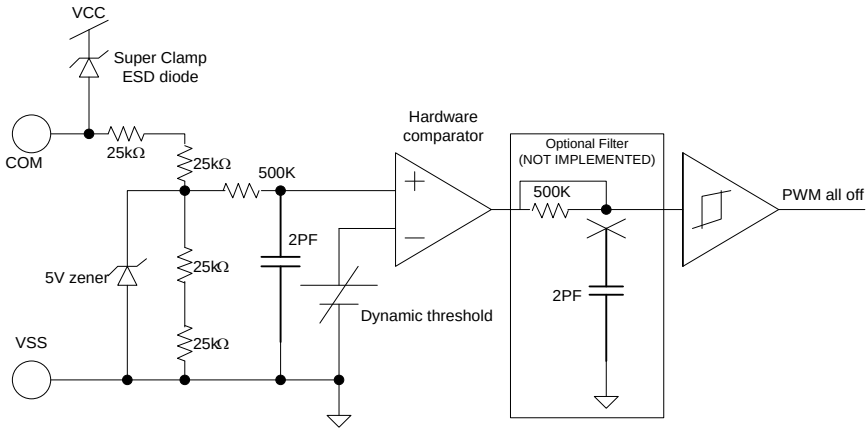


Figure 3.34 - COM pin current limit comparator and analog filter

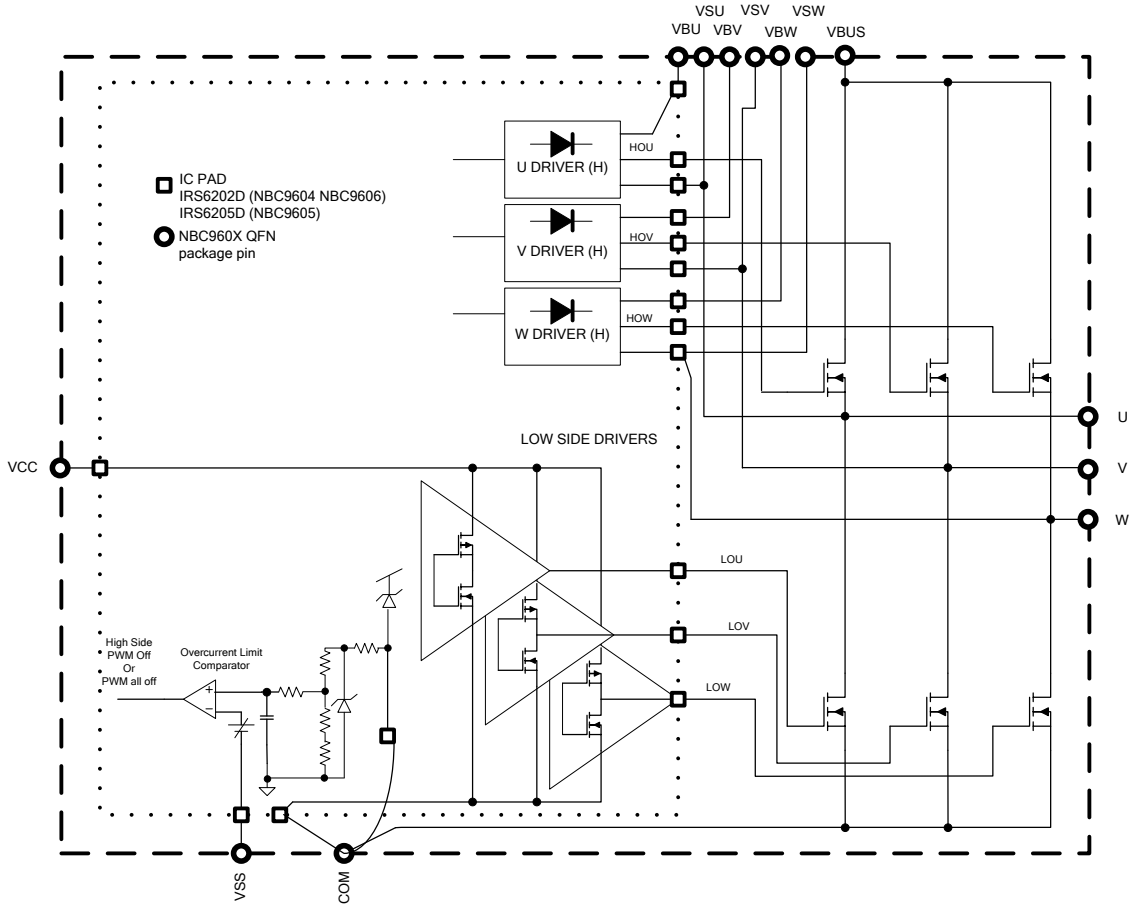


Figure 3.35 COM/VSS connection between IC and QFN package pins

COM/VSS pins and the IC pads inside of IRDM983-025MB, IRDM983-035MB are connected by the bonding wires and shown in Figure 3.35. In the application circuit, a shunt resistor is connected between VSS and COM pins. Therefore a main motor current flow from COM pin to VSS pin. In the IC there are three IC pads for the logic ground, the low side gate drivers return, and the overcurrent sensing circuit input. The overcurrent sensing pad and the low side gate drivers return pad are connected to COM pin by two wires bonding inside of the QFN 12x12 package. The logic ground (VSS) pad is connected to VSS pin.

3.8 EFF – Phase angle advancement parameter input pin

There is one motor parameter called EFF in the system. This pin defines the phase angle advancement between the applied voltage and the BEMF (or Hall sensor). The curve is a quadratic function and 16 (sixteen) selection with a different gain. The definition of each curve is based on degree/rpm, more specifically degree at 50Hz. For IRDM983-025MB and IRDM983-035MB, the default curve passes at 5,37degree/50Hz and with the maximum possible gain is 25,9degree/50Hz
There is a phase angle advancement limit which is 45degree.
Above 100 Hz the phase advancement is kept constant.
Figure 3.36a,b and c show the look up tables of EFF for IRDM983-025MB and IRDM983-035MB.

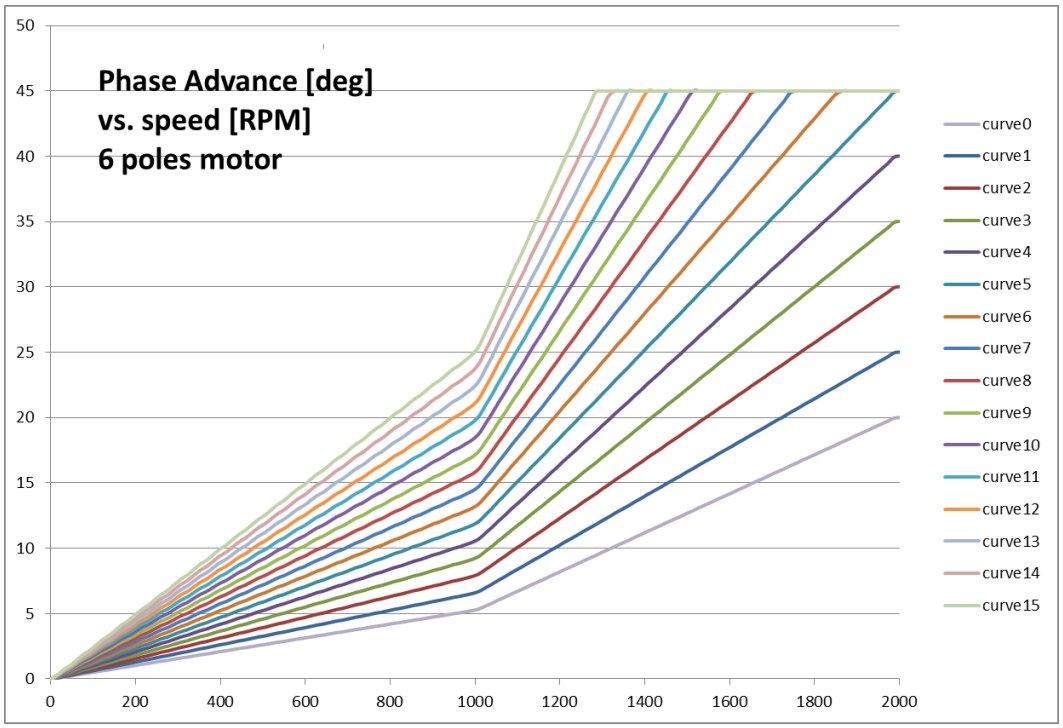


Figure 3.36a Phase Gain Parameters (EFF) Selection Scheme – 8 poles motor

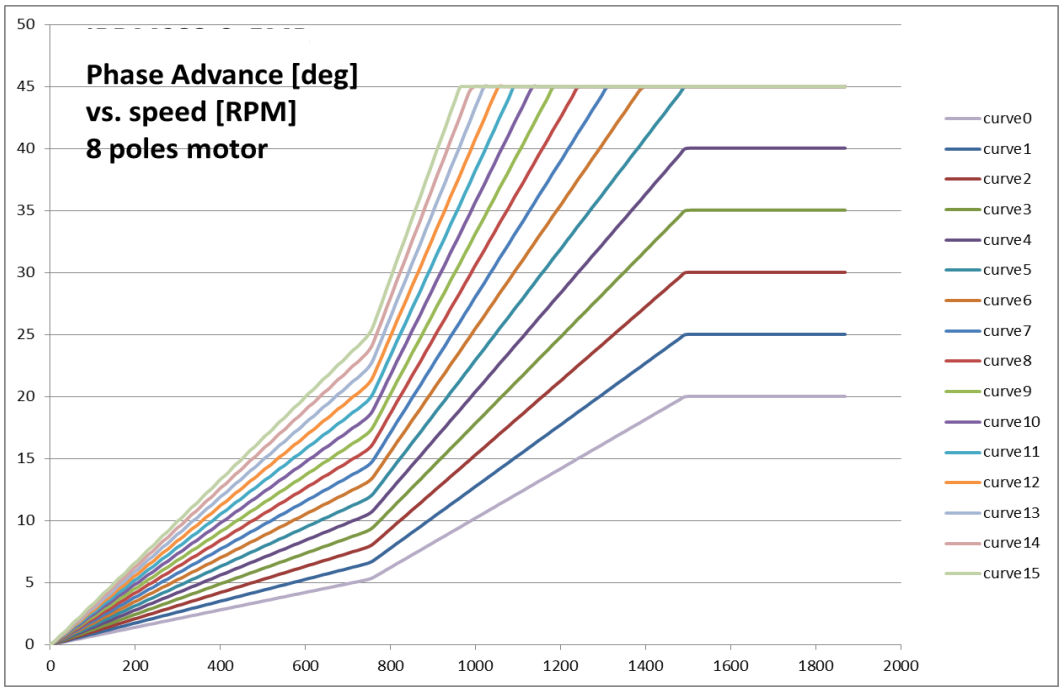


Figure 3.36b Phase Gain Parameters (EFF) Selection Scheme – 6 poles motor

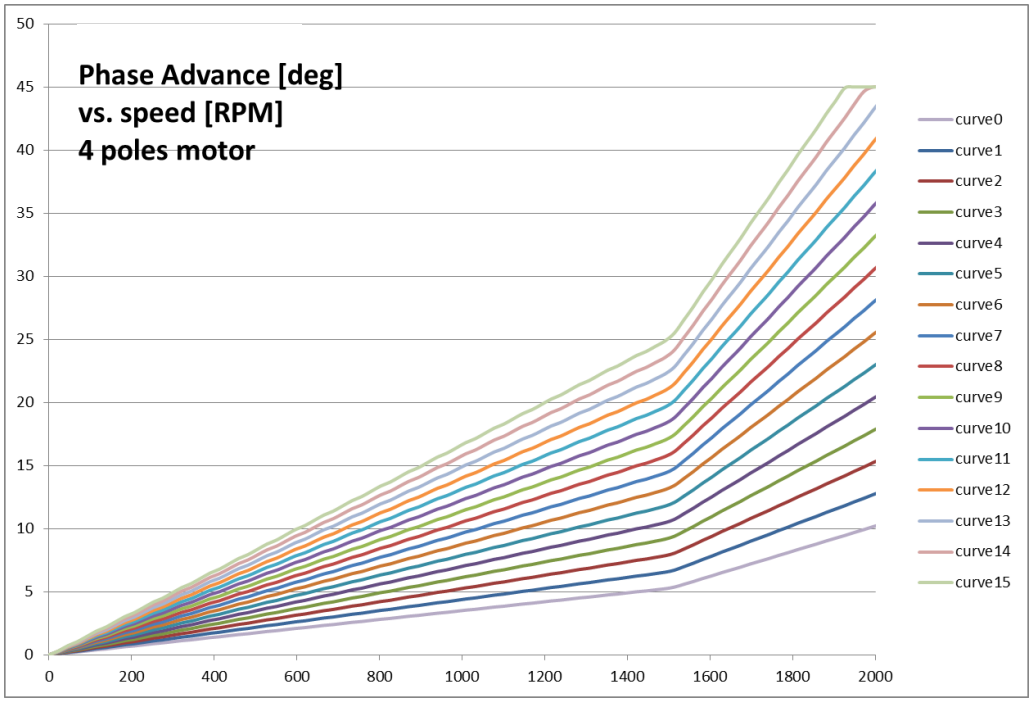


Figure 3.36c Phase Gain Parameters (EFF) Selection Scheme – 4 poles motor

The above curves depend on effective value of the PWM frequency, given the RC network on CLKIN and XTAL pins, since the values in the table below are calculated at nominal PWM frequency of 20 kHz.

The following table shows the parameters selections and defaults.

Table 3.4a – Parameters Selection for IRDM983

Select	Degree/50Hz	Frequency [Hz] @ advance=45deg	EFF input	EFF digital input
15	25.49	64.22	3.094V – 3.300V	152
14	24.15	65.75	2.888V – 3.087V	144
13	22.81	68.04	2.681V – 2.881V	136
12	21.47	70.34	2.475V – 2.675V	128
11	20.12	72.63	2.269V – 2.469V	120
10	18.78	75.69	2.063V – 2.262V	112
9	17.44	78.75	1.856V – 2.056V	104
8	16.10	81.80	1.650V – 1.850V	96
7	14.76	87.16	1.444V – 1.644V	88
6	13.42	92.51	1.238V – 1.437V	80
5	12.07	99.39	1.031V – 1.231V	72
4	10.73	Advance=40deg above 100Hz	0.825V – 1.025V	64
3	9.39	Advance=35deg above 100Hz	0.619V – 0.819V	56
2	8.05	Advance=30deg above 100Hz	0.413V – 0.612V	48
1	6.71	Advance=25deg above 100Hz	0.206V – 0.406V	40
Default = 0	5.37	Advance=20deg above 100Hz	0.000V – 0.200V	32

Notes:

1) EFF input is sampled/latched at reset/power-on and takes four times averaging.

3.9 Motor Direction (DIR) pin

The direction pin allows the user to set the rotation sense of the motor. The status of this pin is latched at the motor start command and any change will not take effect until the motor is halted and then started again. In normal operation the 11 bit Vsp value after 4 samples sum and after 10ms Low Pass Filter is used to issue the start command (that is PWM enable) and to issue the stop command (that is PWM disable). So if Vsp11bit >=796 it is considered as start command and the PWM is enabled and the DIR pin is latched. If Vsp11bit < 796 it is considered as stop command and the PWM is disabled. The motor direction is set by the DIR pin as follows

DIR pin = LOW; Motor Direction (phases sequence) V, U, W
DIR pin = HIGH; Motor Direction (phases sequence) U, V, W (Default value)

The logic state of this input sets the motor direction only if the MOTOR_START command is generated through the VSP input. While if the MOTOR_START command is issued through the UART by writing to the specific register, the motor direction is set by the specific register in the register file and the status of the DIR pin ignored.

This pin is internally pulled-up, and its level will be high if left unconnected.

3.10 Motor Speed Feedback (PG pin) and Feedback Select (PGSEL)

The PG pin is an output that indicates the mechanical speed of motor. The speed is expressed in the form of pulses/mechanical rotation. This output pin is an open drain with an on-resistance of 50 ohm. The default rate is 3 pulses per electrical revolution, hence for a 8 poles motor the rate is 12PPR. The PGSEL pin determines the feedback frequency, if pulled low, the pulses per electrical revolution become 1, hence 4 PPR for a 8 poles motor. PGSEL=high is a default condition with internal pull up resistor, which corresponds to 12PPR on 8 poles motor.

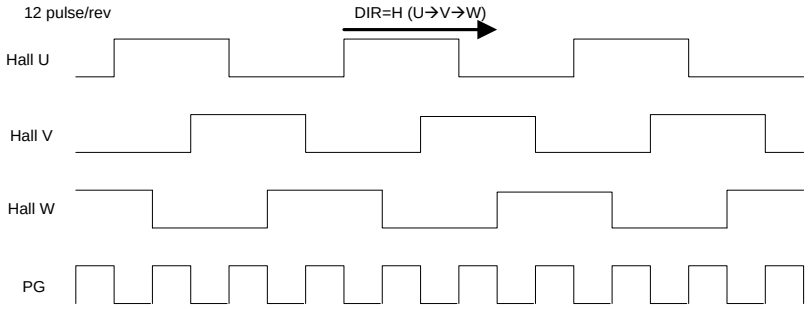


Figure 3.37 PG output

3.11 Power MOSFET Options

Two types of high voltage MOSFET are equipped with each of IRDM983-025MB, IRDM983-035MB depending on the voltage rating and Rds(on) at 25C.

Table 3.5 MOSFET option

MOSFET type	Voltage	Rds(on)
IRDM983-025MB	500V	4Ω
IRDM983-035MB	500V	2.2Ω

3.12 Supply Inputs and Grounds

The IRDM983-025MB, IRDM983-035MB require one single 15VDC supply. The internal circuitry operating at 3.3VDC is powered through an internal voltage regulator. The regulator's output is available externally to a pin for connection to a capacitor. The regulator's output is also available for powering external devices (maximum output capability is 2mA). Both the 15VDC and 3.3VDC are monitored by an on-chip under-voltage detection circuitry that triggers a system shut-down in case the lower thresholds are crossed.

The IRDM983-025MB, IRDM983-035MB has a common ground for the analog and digital circuitry (VSS) and for the MOSFET's gate drivers return (COM) which also interconnects to the current sensing input.

3.13 Analog to Digital Converter

The IRDM983-025MB, IRDM983-035MB integrate a 9-bit dual-slope A/D Converter to acquire Ground connection voltage for offset compensation of all the other 5 channels, VSP, internal Temperature sensor, EFF, internal voltage reference and Vsp input for 6 step special test mode which totals of six channels. The ADC does not require any external components. Figure 3.42 shows a simplified block diagram of the A/D converter.
The ADC state machine controls the operations of the analog input multiplexer, the integrator and the latching of the converted value from the counter into the relevant ADC conversion register.

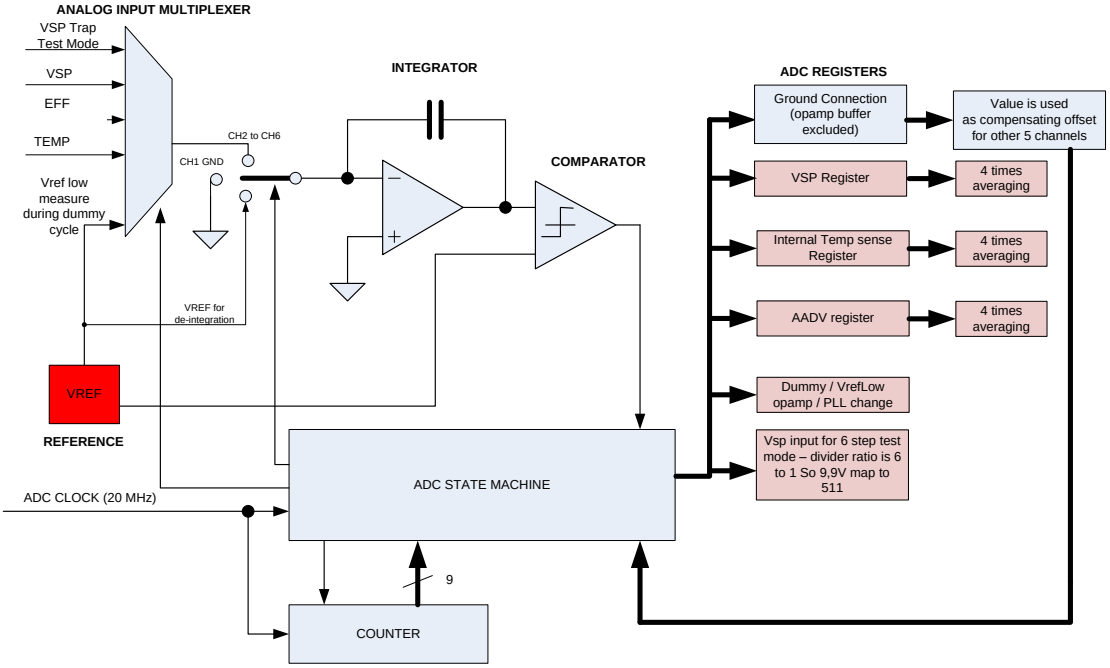


Figure 3.42 A/D Converter Simplified Block Diagram

The basic operations of the dual-ramp ADC are the followings: the input signal (Vinput) is applied to the integrator (in the form Vref – Vin). At the same time the counter is started, counting clock pulses (ADC clock 20MHz). After a predetermined number of 512 counts (hence a fixed integration interval of time T) a reference voltage having opposite polarity is applied to the integrator. At this instant, the accumulate charge on the integrating capacitor is proportional to the average value of the input over the interval T. One AD conversion takes 1211 cycles based on a 20MHz clock which is 60.55usec.
The integral of the reference is an opposite-going ramp, this phase is called de-integration. At the same time, the counter is again counting from zero. When the integrator output reaches the low threshold, the count is stopped and the analog circuit is reset (Zeroing phase). Since the charge gained (integration phase) is proportional to Vin * T, and the equal amount of charge lost (de-integration phase) is proportional to Vref *ΔT, then the number of counts relative to the full count is proportional to Δt/T or Vin/Vref. The counter therefore is the binary representation of the input voltage.

The dual-slope A/D Converter is independent of both capacitance and the clock frequency, because they affect both the integration and de-integration in the same ratio.

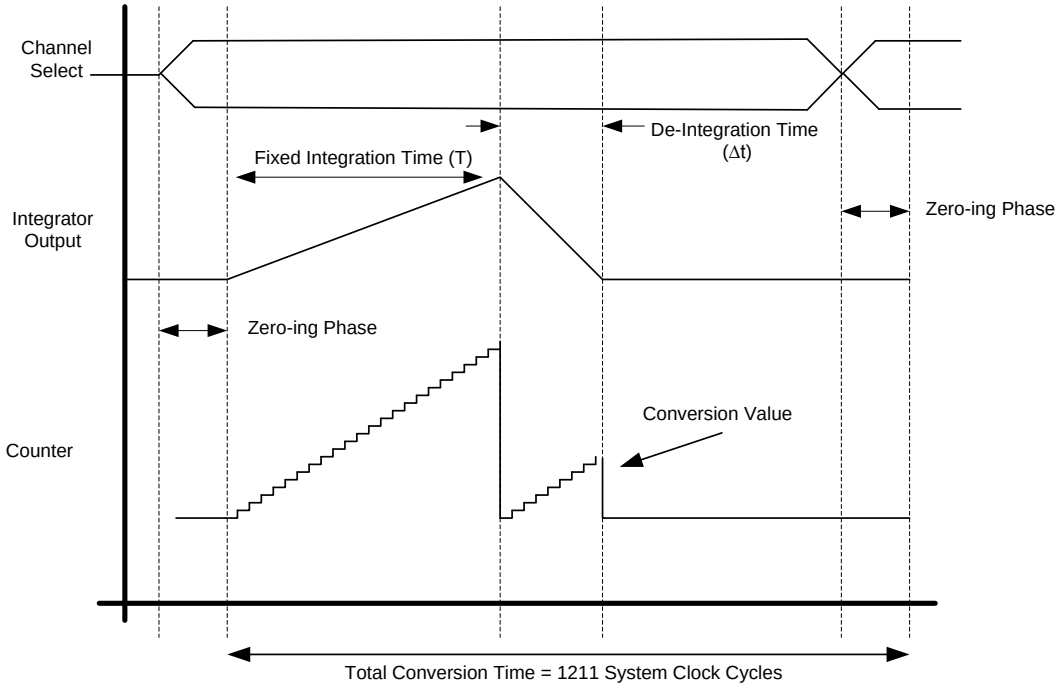


Figure 3.43 A/D Converter Conversion Sequence

The six A/D Channels are converted in the following sequence shown in Figure 3.44;

1) Ground connection to calculate offset compensation. Ground connection bypasses the multiplexer.
2) VSP input
3) Internal temperature sensing
4) the EFF pin input
5) dummy conversion – low level saturation of the opamp buffer. During this cycle the PLL may change the clock
6) Vsp input to enter in 6 step Trap test mode. The resistor divider is 6 to 1 ratio. 9,9V is mapped to 511.

One scan of the above eight channel conversion takes 363,3usec which is derived from a rate = 6 * 1211 * ADC Clock (20MHz). Figure 3.44 shows the conversion sequence. EFF is continuously converted in the sequence but their value is latched once to the secondary register after 4 consecutive samples and averaged. Then the only latched value is used when the IC becomes active either from standby or power up. Therefore continuous EFF conversion will not affect any algorithm execution.
The internal voltage references are acquired and used to compensate the drift of the voltage reference (compensation logic is embedded in the A/D Converter state-machine).
The internal temperature sensing is the one that affects a dynamic overcurrent threshold and maximum overtemperature limit. Every scan cycle includes the conversion of 6 channels. The converted value of the first channel that is directly connected to Ground is used to compensate the offset in the other 5 channels. The value read in the first channel should be ideally zero, however the channel is able to read both positive and negative values. The offset coming from

the first channel is clamped to be in the range of [-30 to +30]. The other 5 channels (Vsp, Temperature, EFF, dummy ref. low and Vsp for test mode are then automatically compensated by the measured offset in the first channel.

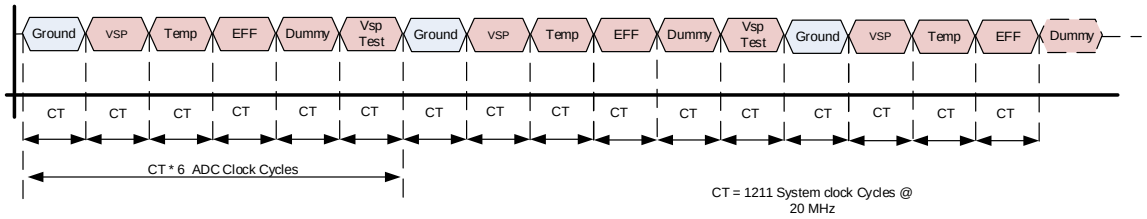


Figure 3.44 A/D Converter Channels Conversion Sequence

The A/D converter in the IRDM983-025MB, IRDM983-035MB has an embedded filtering function due to its Dual Slope structure and the fixed period integration performed on input signal.
The input is not instantaneously sampled, but integrated for a time that lasts 512 * t (where t is the ADC clock period: 50nS).
The frequency response of this filter is similar to the one with a single pole RC filter with a -3dB frequency of:

$$\frac{1}{2 \cdot 511 \cdot t} \cong 19.53KHz$$

In addition the filter has multiple transmission zeroes at 1/256*t frequency and his harmonics.
The following picture is a simulated frequency response of this kind of filter.
The simulated filter has a -3 dB point that is half (10 KHz instead of 20 KHz) of the IRDM983-025MB, IRDM983-035MB Converter filter.
The shape of the amplitude is the same, frequency not in scale.

Offset cancellation in the ADC circuit

The A/D converter circuit contains the offset cancellation circuit. In Figure 3.42, one channel is connected to the ground at an operational amplifier. Ideally the de-integration phase should last 512 cycles, thus producing zero (the complement of 512) as the result of the integral action of ADC.
If the offset results, it is clamped to +/-30.

1) Case of negative offset

In this case the de-integration ramp is shifted above the ideal de-integration ramp (while keeping the same slope). As an example, in case of a negative offset of -10 counts would consist in 522 cycle de-integration time for the channel 1 ground. As a net result it is a conversion 10 cycles longer. The offset in this case is computed as
Offset=512-522=-10
This means that all other channels would experience a longer de-integration time of 10 counts thus giving uncompensated result 10 counts smaller (note: remember that ADC result is 512 complement of de-integration time). So by subtracting the offset, that in this case is negative, has a net result of adding 10 counts to all the other 5 channel readings.

2) Case of positive offset

In this case the de-integration ramp is shifted below the ideal de-integration ramp (while keeping the same slope). As an example, in case of a positive offset of 10 counts would consist in 502

cycle de-integration time for the channel 1 ground. As a net result it is a conversion 10 cycles shorter. The offset in this case is computed as
Offset=512-502=10
This means that all other channels would experience a shorter de-integration time of 10 counts thus giving uncompensated result 10 counts bigger (note: remember that ADC result is 512 complement of de-integration time). So by subtracting the offset, that in this case is positive, has a net result of subtracting 10 counts to all the other 5 channel readings.

3) Maximum offset clamp

Offset is always clamped between -30 and 30. Every 6 channels scan has a new offset reading. The operation of subtracting the offset with its sign is conducted by taking care of the lower and upper saturation of the final results, this means that for channels from 2 to 6 the ADC result is always kept in the range [0 511].
Example) if Vsp reads 4 and offset is 10, compensated result is 0.

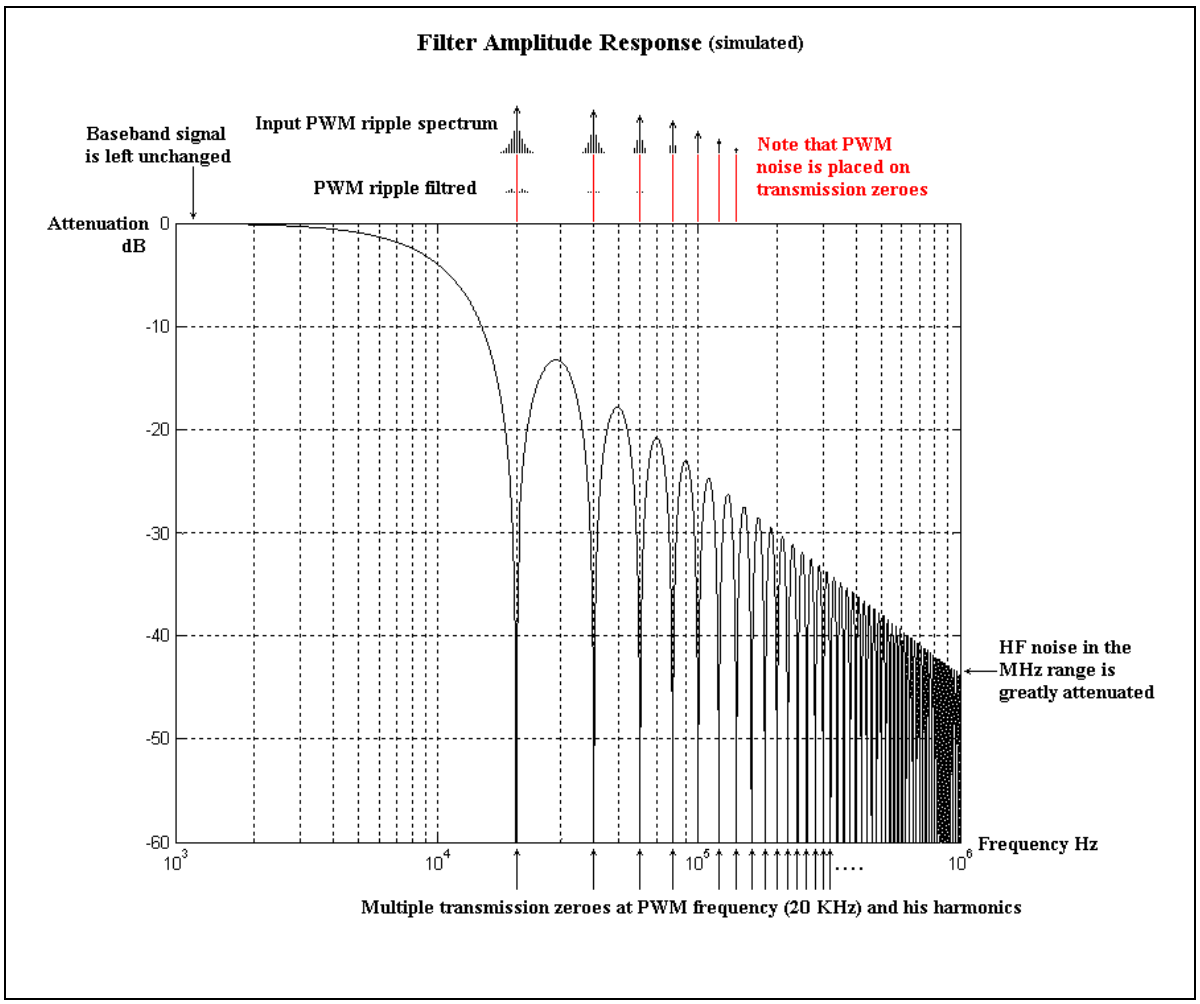


Figure 3.45 Filtering Introduced by the Dual-Slope Converter

3.14 Clock Generation (XTAL, CLKIN)

The IRDM983-025B and IRDM983-035MB have an on-chip PLL (Phase-Locked Loop) to generate the internal system clock. The PLL relies on an internal DCO (Digital Controlled Oscillator) and on and external low-frequency reference input clock of 32.768kHz (32768Hz) to synthesize the internal main clock. The PLL has a fixed multiplication factor of 1220, to provide a 40MHz clock (at the DCO output) from the 32,768Hz of the reference clock. The DCO output is then divided through a prescaler to obtain the 20MHz system clock.
The following Figure 3.46 shows the PLL block diagram.

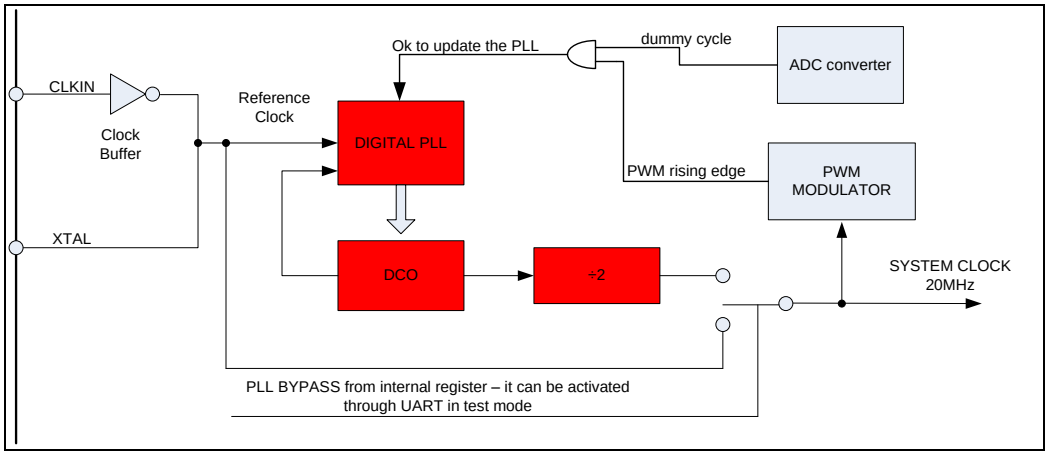


Figure 3.46 PLL Block Diagram

The input clock can be provided by either a 32,768KHz crystal or ceramic resonator (typically the low-cost type of quartz used in watches) or an oscillator. An RC, with time-constant properly sized to generate the required 32KHz can also be used (connections are shown in the Figure below).

Note: The IRDM983-025MB, IRDM983-035MB have an on-chip UART interface. In order to operate correctly with other devices, the UART standard requires the reference clock input to have a tolerance within 5%.
The PLL can accept reference clock frequency within +/-15% from its target frequency (32768Hz).

The system clock (DCO output clock/2), is used in all the system's peripherals including ADC, and PWM modulator.
A variation of the reference clock directly reflects on the system clock on the same percentage amount. For example a 10% change on the Fref will reflect on a 10% variation on the system clock.
An intentional variation of the Fref from its nominal frequency can be introduced by the customer to modify the PWM modulator carrier frequency from the nominal value.

Example: If the nominal carrier frequency selected is 20KHz at 32768Hz reference clock, the carrier frequency could be modified to 21 KHz (5% increase) by changing the reference clock to its value can be modified by modifying the reference clock to 34406Hz.

A loss of external clock does not cause the system to stall. The external clock is used as reference only. Upon an external clock loss the internal clock (DCO) will still be running although not regulated, it allows the system function and protections to operate.

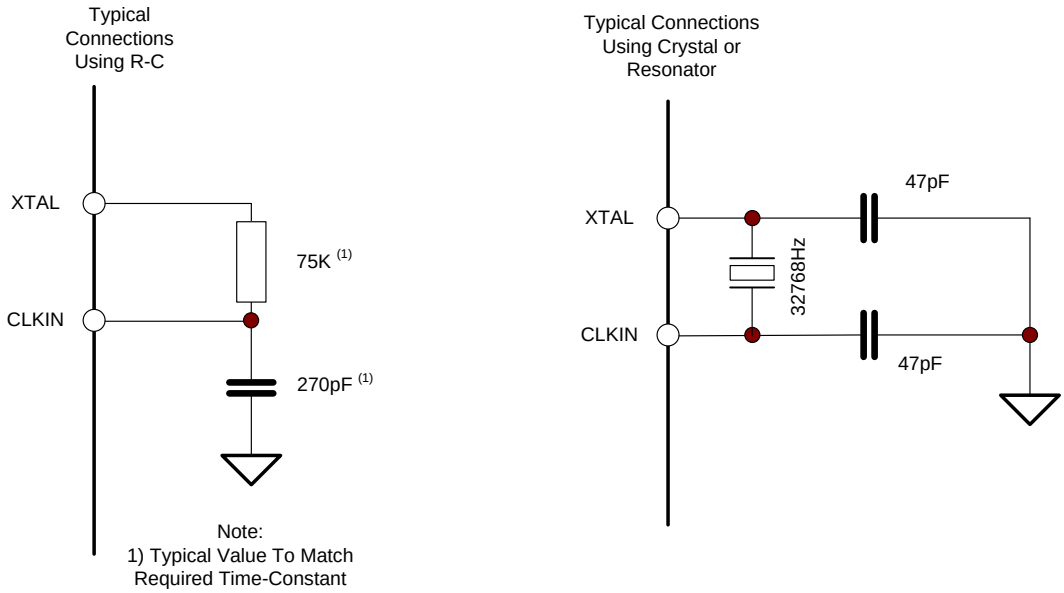


Figure 3.47 Typical Required External Circuitry for Clock Generation

$$F_{PWM} = \frac{1}{\left[\left(R_{EXT} + R_{IC}\right) * \left(C_{EXT} + C_{IC} + C_{PCB}\right) + t_{DEL}\right] * K}$$

K=2.466; scale factor (engineering unit conversion)

t_{DEL} = 900 ns; internal delay time of clock circuit in nanoseconds

The following combination of each RC will yield Fpwm=18.5kHz

R_{EXT} = 75kohm
R_{IC} = 50ohm
C_{EXT}=270pF
C_{IC}=5pF
C_{PCB}=5pF

The following combination of each RC will yield Fpwm=20.5kHz

R_{EXT} = 39.2kohm
R_{IC} = 50ohm
C_{EXT}=470pF
C_{IC}=5pF
C_{PCB}=5pF

3.15 PLL control algorithm

The IRDM983-025MB and RIDM983-035MB have a special PLL control algorithm that is optimized and has the following features:

- PLL is updated only during the dummy channel scan so clock variation does not affect the ADC channel conversion
- PLL is updated only at rising edge of PWM cycle so that the PWM pulse is not affected by the instantaneous clock change due to PLL change
- There is a specific guard band on the number of fast clock cycles (i.e. 20 MHz clock) inside the external reference clock period. The allowed number of clock cycles is 1220 +/- 30. This specific guard band reduces the jittering of the main DCO clock hence it reduces the jittering of the PWM output
- There is a specific guard band used within every ADC 6 channels scan period (1211 x 6 clock cycles). Every 6 channels scan the difference between the used DCO control word and the desired DCO control word is computed. The used DCO control word is updated only if the difference between the used and the desired control word is bigger than 3 in absolute value
- Every ADC 6 channels scan the difference between used and desired DCO control word is reset, that means: either used DCO control word is updated or the desired control word is reset to be equal to the used control word
- Every ADC 6 channel scan start in the measure of how many fast clock cycles (i.e. 20 MHz) inside the external reference clock period are reset for the next 2 periods
- The control algorithm uses always the average of 2 samples of fast clock cycles counts inside 2 external reference frequency periods

The block diagram that explains the algorithm is shown in figure 3.48.

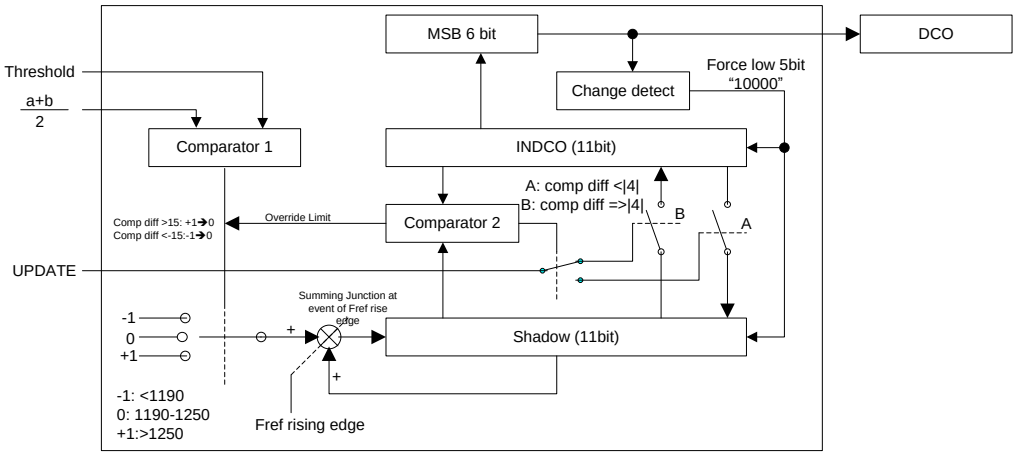


Figure 3.48 PLL control algorithm block diagram

In figure 3.48 the signal indicated with ‘Fref rise’ is a pulse that is generated every time the external reference frequency signal exhibits a rising edge.

The ‘UPDATE’ signal is a pulse generated when the following condition is met:
ADC is in dummy channel conversion (that lasts 1211 fast clock cycles) AND a rising edge of PWM clock occurred.
The average indicated as ‘(a+b)/2’ indicates the fast clock cycles (i.e. 20 MHz) counts inside 2 adjacent periods of the external reference clock.
The comparator 1 generates a +1, a 0 or a -1 output depending on the value of the (a+b)/2 average. In the event that the Comparator 2 output exceeds more than 15 or less than -15, then the value to the summing junction is forced to be zero and the Comparator 2 output stays within +/-15 as a maximum value limit. This means that the Shadow register is always kept in the range [INDCO-15 INDCO+15].
In the event of 2 PWM rising edges within a dummy cycle, the first rising edge is updating either the INDCO or the Shadow, the second is repeating the same operation without any effect(i.e. the Comparator 2 out is 0) and the non-usable Comparator 1 output data becomes four Fref cycles as opposed to two Fref cycles.

In figure 3.49 it is shown a timing diagram that demonstrates how the computation is done in the algorithm.

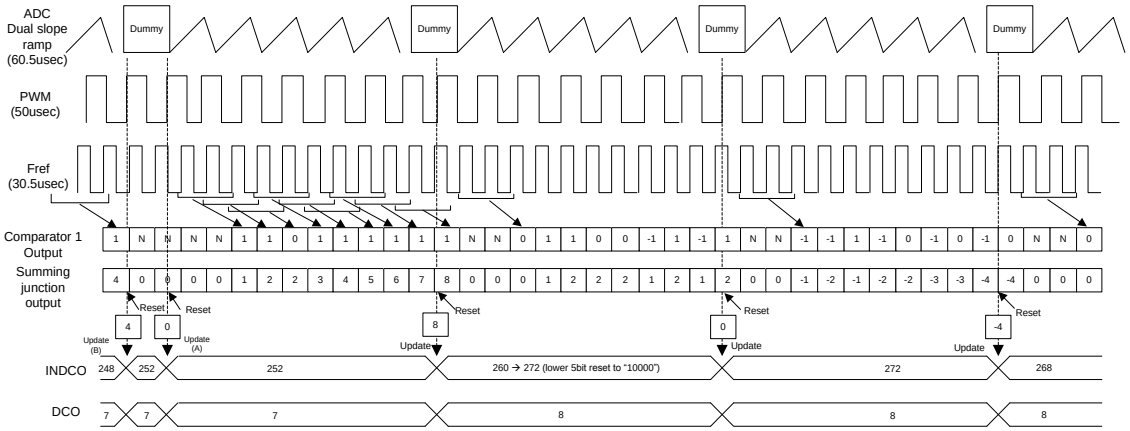


Figure 3.49 PLL control algorithm block diagram

In Figure 3.49 it is shown the ADC sequence made of 6 channels scan. The channel sequence of the ADC in IRDM983-025MB, IRDM983-035MB is composed of 6 channels, as per previous paragraph description. One of these 6 channels in each sequence is called ‘dummy’ channel and its conversion is discarded and not used in normal operating mode function.

When the dummy channel is converted, in conjunction with a rising edge of the PWM clock, a pulse to change the INDCO control word is generated. The effect of this ‘change’ pulse signal is either copying Shadow register (fig 3.47) in to INDCO register or vice versa.

The output of the comparator (-1, 0 or +1) is always reset to 0 in the next 2 cycles after a ‘change’ pulse signal.

The copy from the shadow register to the INDCO register is executed whenever the ‘add result’ is bigger than 3 in absolute value.

If the INDCO 11 bit control word is modified and this modification affects the 6 MSB of the control word, then the DCO clock is really changed. In this case, to avoid further jittering also the lower 5 LSB of the INDCO and the Shadow 11 bit control word are modified to become “10000”$_b$.

4.0 Power up sequence and Faults

4.1 Power up sequence and standby state

The IRDM983-025MB and IRMD983-035MB can be forced into RESET State by the on-chip power-on reset block (POR), by the on-chip supply monitor block (following a 15VDC or 3.3VDC supplies under-voltage). The device is forced into RESET state until all the sources of the reset have become inactive, thus starting the BOOT Sequence. The IRDM983-025MB and IRMD983-035MB also have internal standby mode based on VSP input voltage. When VSP becomes less than 1.15V while VCC is 15V then the system goes into a standby mode where all PWM output becomes off, VDD is disengaged and internal digital circuit becomes inactive including ADC conversion. Once a power up starts or transition to active state starts from the standby mode (VSP > 1.4V) VDD is first activated followed by POR (Power On Reset) release. The PLL reset is then released to active and establishes the system clock internally. Once the system clock is established, the ADC starts its function. After 41 ADC scans, the 4 samples average of EFF input value is stored for internal angle advancement value use. Although the EFF is continuously converted while VCC is on and VSP > 1.4V, its converted value is no longer used in the system until the next reset or standby event. PGSEL digital input is latched after 3 consecutive sampling which are 10microsecond apart, and determined by a majority voting. The PGSEL latch starts at Logic Reset release. DIR is sampled three times and based on the majority voting, and latched at a motor RUN command and the value is determined and stored in the system to be used for algorithm computation. Once sampling of EFF and PGSEL is completed, these values are stored and used until next Reset regardless of the ADC update. DIR setting is sampled after every motor start command to allow change of direction.

Figure 4.1 shows the Power up Sequence timing and states.

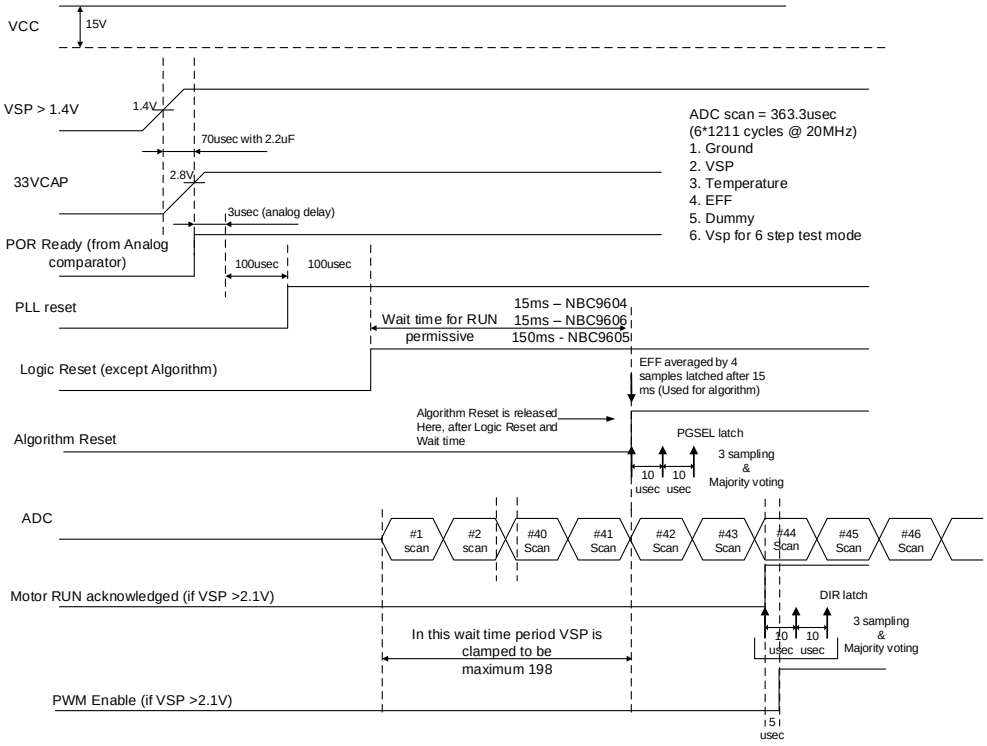


Figure 4.1 Power up Sequence Timing

4.1.1 VDD voltage in standby

In standby state, VDD pin may still exhibit some voltage (usually <100mV). This is normal because the internal digital circuits may not be able to discharge VDD pin to 0V.

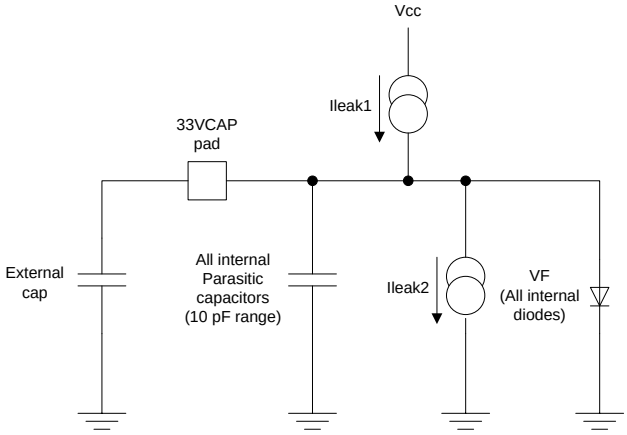


Figure 4.2 Equivalent circuit of VDD pin in standby

4.2 Protection

The IRDM983-025MB, IRDM983-035MB have several on-chip protections to ensure proper operations and avoid damage to motor and motor drive. The table summarizes the faults and associated actions.

Fault	Value	Action
UVCC	8.2V	Reset
UVBS	8.2V	Associated high side off for a PWM cycle
VSP standby	1.15V	All digital circuit powered off. Will cause reset
Overcurrent	dynamic	High side off/low side all on OR All PWM off
Over-temperature	Above 100C	All PWM off
Over-temperature	Below 100C	Set dynamic current limit of 520mV/375mV/250mV
Rotor Lock	VSP>1.9V and less than 45rpm for more than 5 seconds	Change current limit to 250mV
Over-speed	Above 3000rpm	All PWM off

Table 4.1 Fault and Protection

4.2.1 Over-Current Limit

The over current limit function never causes a trip or reset. It sustains motor running operation PWM cycle by PWM cycle while only engages its functionality. The comparator to determine whether overcurrent or not has a dynamic/variable threshold (four values including rotor lock) depending on the temperature.
Once the overcurrent limit is triggered by a comparator, the overcurrent limit action persists within a pending PWM cycle. In the other word, the overcurrent action cannot aborted within a pending PWM and its action is latched till the end of PWM cycle.

The over current functionality is described below.
There are 3 current limit modules, one per each phase U, V and W.
The current limit module, placed after the deadtime insertion logic block, takes the high side and the low side PWM commands coming from modulator as input (e.g. uhin ulin) and generates PWM commands (e.g. uhout ulout).

In normal operation (no overcurrent) the current limit module behaves as this:

1- high side command: the high side command is passed through the current limit module (e.g. uhout=uhin)
2- low side command: the low side command is passed through the current limit module (e.g. ulout=ulin)

During overcurrent:

There are two overcurrent limit actions depending on the state of speed and the combination of motor direction and DIR signal (RDM). The speed condition is based on the Hall V edge to edge measurement. The combination of motor direction and DIR signal is specified:

RDM signal = 0 (DIR=forward and motor rotation=forward, or DIR=reverse and motor rotation=reverse)
RDM signal = 1 (DIR=reverse and motor rotation = forward, or DIR=forward and motor rotation=reverse)

1) Overcurrent limit action 1
    a. PWM action: High side off and Low side all on
    b. Condition: any speed and RDM=0, and speed within negative 45rpm and RDM=1

2) Overcurrent limit action 2
    a. PWM action: All off
    b. Condition: speed beyond negative 45rpm and RDM=1

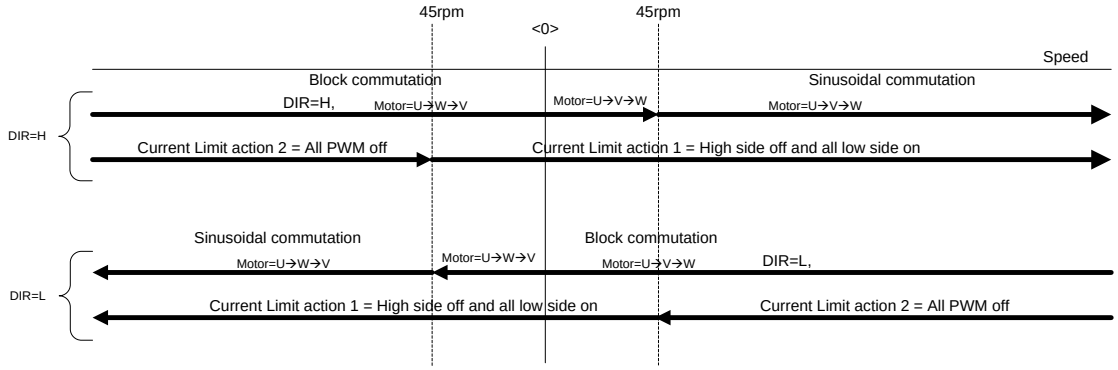


Figure 4.3 Overcurrent Limit action and condition

The deadtime within the overcurrent limit block is inserted under the following condition.
If low side command in input is zero (e.g. ulin=0) then the deadtime is inserted and during deadtime low side command is kept to 0 (ulout=0) and only after deadtime the low side command is raised to one (ulout=1 after dead time).

4.2.2 Power Supply Under-Voltage Protection

The IRDM983 is equipped with power supply monitor circuitry. If the external 15VDC drop below the minimum threshold an internal reset is generated. The device is held in fault condition until the voltage levels return above the minimum threshold. Once the supplies value return above the minimum level, a reset sequence is initiated and the system can resume normal operations.

4.2.3 Over-Temperature Protection above 100C

Over-temperature is activated when reaching to 100C or above. Once over-temperature is activated, it remains in fault state until temperature is reduced to 80C. This is a hysteresis so that it prevents the system goes back and forth between active and inactive.

4.2.4 Rotor Lock Detection

The rotor lock condition (or under-speed condition) is detected by two conditions that:

- VSP > 1.9V
- Speed is less than +/-45rpm
- 5 seconds timer elapsed (5 seconds is at 20 kHz PWM nominal frequency. Otherwise it is 5 seconds x 20 kHz / PWM freq [kHz])

The following Figure illustrates the mode of Rotor Lock and normal run mode.

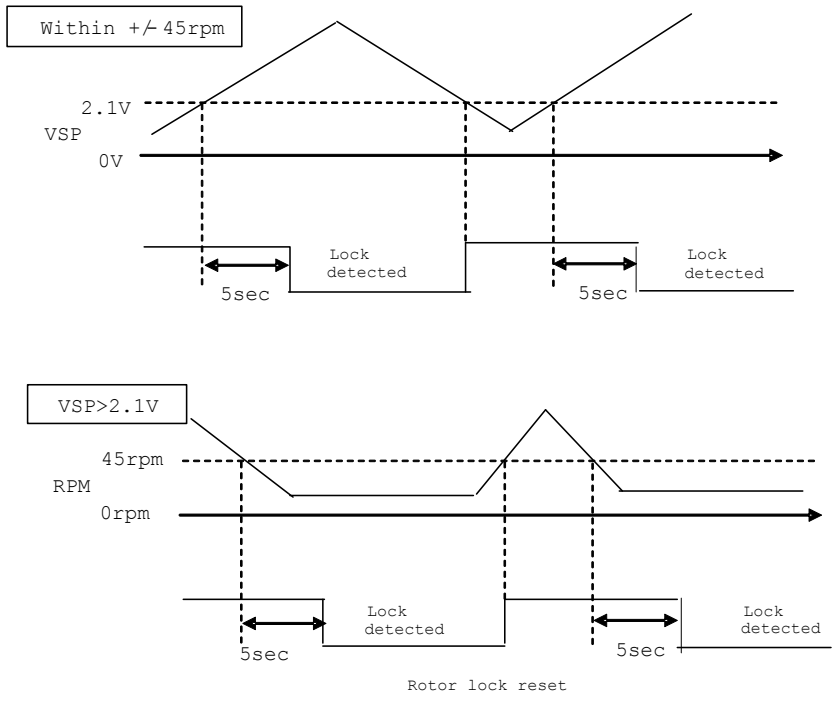


Figure 4.4 Rotor Lock

4.2.5 Over-speed protection

When the speed exceeds 3000rpm (on a 8 poles motor), all PWM becomes off. There is no hysteresis on over-speed. 3000 rpm is based on 20 kHz PWM nominal frequency. If different PWM frequency is used the threshold becomes; over-speed = 3000 RPM x PWMfreq [kHz] / 20kHz.

Appendix A. Register File

Registers Map

The IRDM983-025MB, IRDM983-035MB have a set of register that are loaded at power-on or reset with default values stored in the internal ROM. In test mode, a Personal Computer or host processor can modify the value of the registers to control the IRDM983-025MB, IRDM983-035MB device using a standard RS-232 port in test mode. Control/status registers are mapped into a 128-byte address space.

.

Address (L) decimal	Address (H) decimal	Name	Width	Type	Decimal Value Default at Reset
02	03	testmodereg	4	WR	0
04	05	hw_mode_bits*	7	WR	12 if not in test mode – 2 if test mode
06	07	pg_source	5	WR	0 if not in test mode – 1 if test mode
08	09	dir_source	5	WR	0
10	11	test_adc_chsel	3	WR	0
12	13	reset_control*	2	WR	0
14	15	uart_controls*	6	WR	0
16	17	baudrate	16	WR	1041
18	19	Vsp_UART	11	WR	1000
20	21	directtomodulatordata	11	WR	0
22	23	directtomodulatorcmd	1	WR	0
24	25	directangleadvance	10	WR	0
26	27	enabledirectangleadvance	1	WR	0
28	29	EFF_UART	9	WR	128
30	31	debug0	6	WR	0
32	33	dco_uartcontrolword	6	WR	32
34	35	DIR_UART	1	WR	1
36	37	Currentlimitthrset	3	WR	0
38	39	Start/Stop_UART	1	WR	0
40	41	Enable6StepTestMode	2	WR	1

Table A-1 IRDM983-025MB, IRDM983-035MB Write Register Map

Notes:

1) Registers marked with asterisk have different function for each of their bits. They are accessed as byte. To set a specific bit to logic 1 perform a read before (to know other bits value) then write new value with the proper bit set. Similar operation if a bit needs to be cleared.

Address (L) decimal	Address (H) decimal	Name	Width	Type
42	43	raw unfiltered Vsp from ADC	9	RD
44	45	raw unfiltered temperature from ADC	9	RD
46	47	mechanical speed	16	RD
48	49	vsp11bit used in the algorithm	11	RD
50	51	modulation	11	RD
52	53	ground connection ADC readback	9	RD
54	55	EFF ADC readback	9	RD
56	57	filtered vsp11bit from ADC	11	RD
58	59	Filtered temperature from ADC	9	RD
60	61	dbg_temp_ranges*	6	RD
62	63	dbg_wires*	7	RD
64	65	motorrunacknowledged	1	RD
66	67	pana_state*	16	RD
68	69	Rawvspfor6steptestmode	9	RD
70	71	indco 11 bit	11	RD
72	73	raw ref-low from ADC	9	RD
74	75	currentlimit_rotor_lock*	4	RD

Table A-2 IRDM983-025MB, IRDM983-035MB Read Register Map

Write Registers description

Once the device enters the test mode, the UART is enabled at default 19200 bps @ 20 MHz clock input fed to CLKIN input. Through UART it is possible to read register values (this applies to all registers) and to write new values to those registers that are read/write type.
The registers that show an asterisk are control bit registers (each bit is responsible of a different function).
The same registers are shown here with each bit definition

hw_mode_bits – address 2 – normal mode default 0001100 – test mode default 0000010						
6	5	4	3	2	1	0
rxdselectpadpgseli	dco_directcontrol	ileak_33_disable	ndco_bypass	dco_enable	activate_pad	uart_pgsel

rxdselectpadpgseli – active high: set to 1 if UART rxd is connected to PSEL. Set 0 (default) to have UART rxd is connected to TST1.
dco_directcontrol – active high: set to 1 to control directly DCO by feeding control word from register called dco_uartcontrolword
ileak_33_disable – active high: set to 1 to disable analog circuits working on VDD
ndco_bypass – active low: set to 0 to bypass the internal DPLL controller of the DCO. When controller is bypassed, clock must be fed from CLKIN pin.
dco_enable – active high: set to 1 to enable the internal DCO
activate_pad – active high: set to 1 to activate the digital function in test mode in Hall inputs
uart_pgsel – active high: only when bypassed by UART (see uart_controls register), set to 1 to have pgsel=1 or set to 0 to have pgsel=0

reset_control – address 6 – default 00	
1	0
force_reset	disable_reset_counters

force_reset – active high: set to 1 to initiate internal reset
disable_reset_counters – active high: set to 1 to disable all counters (e.g. 5 seconds before stand by).

uart_controls - address 7 – default 000000					
5	4	3	2	1	0
motorstartstop	direction	vsp	pgsel	angleadvance	adc_chsel

motorstartstop – active high: set to 1 to have the start/stop function bypassed by UART.
If bypassed the command comes from motorstartstopuart register.
direction – active high: set to 1 to have the direction command bypassed by UART
If bypassed the DIR command comes from directioncmd register.
vsp – active high: set to 1 to have the Vsp input bypassed by UART
If bypassed the command comes from targetvoltagesp register.
pgsel – active high: set to 1 to have the pgsel input bypassed by UART
If bypassed the command comes from hw_mode_bits[0] register.
angleadvance – active high: set to 1 to have the angleadvance setting bypassed by UART
If bypassed the command comes from angleadvance register.
adc_chsel – active high: set to 1 to have the ADC channel selection bypassed by UART
If bypassed the command comes from test_adc_chsel register.

Following table shows the possible values for pg_source register.

pg_source	**value**
pgo	0 default in normal mode
txd	1 default in test mode
padmotordiri	2
adctimedvalue	3
sysclkdiv4	4
ncurrentlimit	5
HALL1	6
HALL2	7
hallw	8
pwm_clk	9
padpgseli	10
0	11
1	12
endofconversion	13
convstartpulse	14

Following table shows the possible values for dir_source register

dir_source	value
DIR pad	0 default - input
txd	1 – output
	2 – output
adctimedvalue	3 – output
sysclkdiv4	4 – output
ncurrentlimit	5 – output
HALL1	6 – output
HALL2	7 – output
hallw	8 – output
pwm_clk	9 – output
padpgseli	10 – output
0	11 – output
1	12 – output
endofconversion	13 – output
convstartpulse	14 – output
sysclk2x	15 – output

testmodereg – this register is used in test mode and defines specific test mode function:

testmodereg = 0 is the default uart communication test mode

testmodereg = 1 enables factory scan mode

testmodereg = 2 enables gate drivers test mode. During this test mode the 6 Hall inputs drive directly and independently each of the 6 MOS

testmodereg = 8 enables over current threshold test mode. During this test the register currentlimitthrset is used to drive directly the over current comparator

testmodereg =10 enables Hall digital input mode for use with buffered hall sensors. Hall U comes from H1+, Hall V comes from H2+. The other two Hall inputs are not used.

test_adc_chsel – this register is used with uart_controls[0]=1 and controls directly the ADC channel MUX selector.

baudrate – this register defines the baudrate for uart communication. Formula is:

baudrate = (clockfrequency [Hz] / desired bps [bps]) -1

1041 is default and it is used for 19.2 kbps at 20 MHz clock input.

targetvoltagesp – this register is used to set Vsp when uart_controls[3]=1. Range is [0 to 2044]. Note that when commanded in UART test mode the start/stop command is decoupled from vsp.

directtomodulatordata – this register is used to feed directly the modulator if directtomodulatorcmd =1 . Range is from [0 to 1686] that is [0% to 100%].

directtomodulatorcmd – if set to 1 the modulator is fed directly from directtomodulatordata register.

directangladvance – this register is used to feed directly the angle advance in the modulator if enabledirectangleadvance =1 . Range is from [0 to 682] that is [0deg to 60deg].

enabledirectangleadvance - if set to 1 the modulator angle advance is fed directly from directangleadvance register.

angleadvance – if uart_controls[1]=1 this register is used to set the EFF equivalent input value. Mapping is [0 511] and emulates EFF input [0V 3.3V].

debug0_host_register – this register is used to drive the internal debug0 pad. It is used only at wafer level factory test.

dco_uartcontrolword – this register is used in conjunction with hw_mode_bits[5]=1 and controls directly the DCO ring oscillator.

directioncmd – this register is used in conjunction with uart_controls[4]=1 to select the direction bypassing DIR pin setting. This register works in real time and does not need latching at rising Vsp as DIR input pin.

currentlimitthrset – when testmodereg=8 this register is used to force a specific current threshold to the over current comparator.

motorstartstopuart – when uart_controls[5]=1 this register is used to issue the start (1) and the stop (0) motor command.

enablepanatestmode – this register is composed of 2 bits. Default value is 01.

Bit 0 (default=1) if set to 1 enables the trap test mode if Vsp>8,8V. If it is set to 0 the trap test mode is disabled completely.

Bit 1 (default=0) if set to 1 forces the trap test mode independently from Vsp > 8,8V threshold.

Read Registers description

Once the device enters the test mode, the UART is enabled at default 19200 bps @ 20 MHz and it is possible to read registers to observe some specific internal values.

adcconvregrawvsp – this is the raw 9 bit ADC conversion of the VSP analog input channel for PWM duty modulation before 4 samples sum and 10 ms filter.

adcconvregrawvbe – this is the raw 9 bit ADC conversion of the internal temperature analog input channel before 4 samples average and 10 ms filter.

internalfrequency – this is 16 bit values and represents the internal speed information based on HALL2 falling edge to falling edge. Mapping is 100 RPM mechanical = 436.

vsp11bit – this is the 11 bit Vsp input value used for PWM modulation. It may come either from ADC or directly from UART.

duty_cycle_adj – this is the modulator amplitude used to generate PWM. Mapping is [0 1686] to [0% to 100%].

adcconvregreflo – this value reflects the direct ground connection read by the ADC. This value is also used (with proper sign) to compensate the other 5 ADC channels. Note that ideally this value should be 0. The ADC is able to read both positive and negative offset, however this register reflects only the absolute value. If this register displays a value bigger than 30, the used value for other 5 channels compensation is always clamped to maximum 30.

adcangleadvancement – this is the 9 bit value as read by ADC of EFF input pin mapping is [0 511] to [0V 3,3V].

adcconvregvspout – this is the 11 bit Vsp input value from ADC after 4 samples sum and 10 ms filter. This is used for PWM modulation if not bypassed by UART.

adcconvregvbe - this is the 9 bit ADC conversion of the internal temperature analog input channel after 4 samples average and 10 ms filter.

dbg_temp_ranges – this is a register that reflects internal signals for factory test.

dbg_wires – this is a register that reflects internal signals for factory test.

motorrunacknowledged – if the motor is in run mode this register is set to 1. Otherwise it is 0.

pana_state – this register is composed of [pana_testmode_state[1:0], panacounter[12:0]]. The panacounter is the counter used to decide if entering or not in trap test mode. The pana_testmode_state reflects the state of the state machine that executes the validation algorithm to enter the trap testmode.

adcconvregrawvspfortestmode – this is the raw 9 bit ADC conversion of the VSP analog input channel for trap test mode enter. Mapping is [0 511] to [0V 9,9V].

indco – This the 11 bit register generated by PLL controller. The 6 MSB are used to control DCO.

adcconvregrawoldreflow – This is the register that reflects the reading of the low saturation of the buffer opamp inside the ADC circuitry. Please note that this value is compensated by adcconvregreflo register value. Ideally this register should have 0 value.

currentlimit_rotor_lock – this register is composed by following bits: [cl2,cl1,cl0,rotorlock]. So bit 0 reflects rotor lock condition (if set to 1 it means that rotor lock has been detected). While bit from 3 to 1 reflect the current limit threshold set in the system.

Appendix B. Test mode and UART Communication Protocol

The IRDM983-025MB, IRDM983-035MB contains digital circuitry to perform in house end of production line tests. When this circuitry is activated, the IRDM983-025MB, IRDM983-035MB is said to be operating in ‘test mode’.
The procedure to enter in test mode has been specifically designed to avoid the IC entering in test mode during normal operation.

The test mode entry procedure is described in this paragraph. And some basic description of the available test modes is given.

The test mode uses the following specific pins depending for each purpose.

Entering the test mode:

Pin	Function
CLKIN	20MHz clock input and Entering Test mode
XTAL	Entering test mode only

UART communication pins after entering the test mode:

Pin	Function
TST1	RX, receive data from the host
PG	TX, send data to the host

B.1 Test mode entering mechanism

The test mode can be activated only at IC startup. So, if test mode entry is needed, the IC needs to be power cycled. To ensure successful enter in test mode, these steps must be followed:

1- Start with VCC=0V and VSP=0V
2- Do not apply any signal to the IC when it is switched off otherwise a biasing condition with ESD structure may cause interference
3- [1)]Connect externally (by a relay as an example) XTAL to CLKIN to VDD.
4- Apply VCC=15V
5- Apply VSP=2.0V
6- Wait for minimum 500microseconds
7- Remove the short between CLKIN and XTAL and VDD
8- Connect 20MHz crystal oscillator (50% duty of square waveform) to CLKIN
9- Connect TST1 to the Host UART TX (transmit)
10- [2)]Connect PG pin to the Host UART RX (receive)

[1)]: External 3.3V supply can be used to guarantee 100% test mode entering.
[2)]: PG output needs a pull up resistor.

At this point the test mode is operative and a specific test may be chosen by programming proper values in the proper write registers as per APPENDIX A.
To exit the test mode, simply remove the voltage applied to the IC.

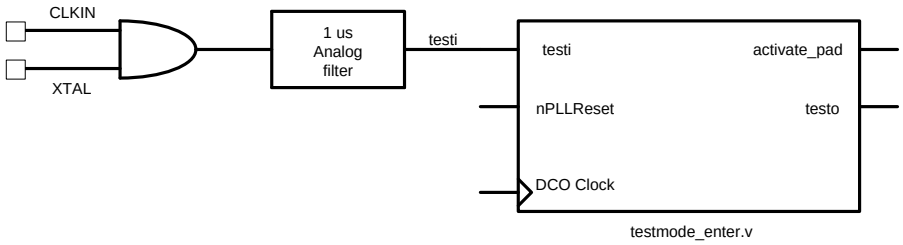


Figure B-1 Test mode entry

The block diagram of the test mode enter circuitry is shown in Fig. B-1. The timing diagram that refers to the same circuit is shown in Fig. B-2.

As voltage is applied to the IC, the nPOReset is released and after 100 us also the nPLLReset signal is released.
The testi signal is sampled twice, at rising edge of nPLLReset and after 1000 clock cycles of the internal DCO (that is roughly after 100 us). If both testi samples are at 1, then the IC enters in test mode.
When entering in the test mode the 6 Hall digital inputs become activated, hence IC consumption may increase.
If the IC does not enter in test mode the digital pads connected to the Hall input pads are completely disabled.

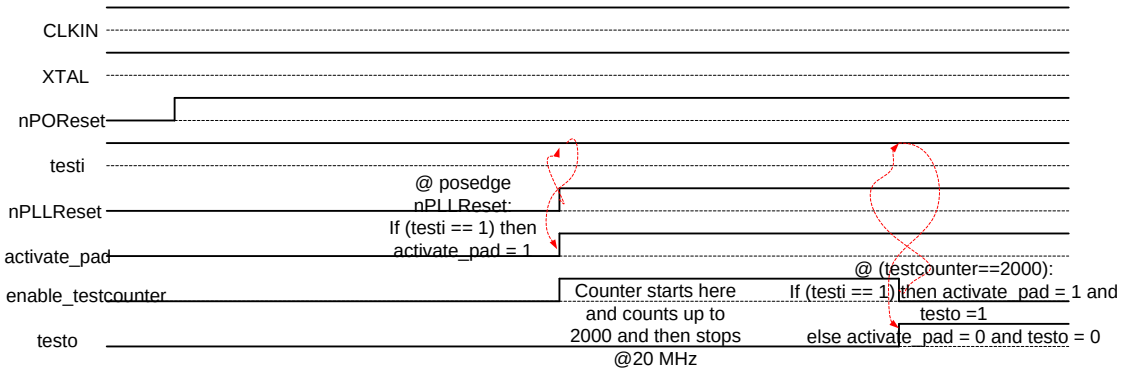


Figure B-2 Test Mode enter timing diagram

There are specific test modes available and they depend on testmodereg register value. The test modes are shown in Table B-1. All other test may be performed with testmodereg=0.

testmodereg	Test Mode
0	All tests except the following rows
1	Factory Scan Test
2	Gate Driver Test (refer to Appendix A for more details)
8	Over Current Threshold test
10	Digital Hall functionality for buffered hall inputs

Table B-1 Test Mode Functions

B.2 Test mode description

SCAN test (testmodereg=1)
This mode enables the in house JTAG scan test.

Gate Drivers test (testmodereg=2)

testmodereg=2 allows testing the gate drives output functionality. On this test mode, the 6 Hall inputs are used to control only the corresponding output as shown is the table below.

Input Hall pin	Corresponding MOS operation
H1+ = 1 H1+ = 0	MOS UH ON MOS UH OFF
H1- = 1 H1- = 0	MOS UL ON MOS UL OFF

H2+ = 1 H2+ = 0	MOS VH ON MOS VH OFF
H2- = 1 H2- = 0	MOS VL ON MOS VL OFF
TST2 = 1 TST2 = 0	MOS WH ON MOS WH OFF
TST1 = 1 TST1 = 0	MOS WL ON MOS WL OFF

Table B-3 Gate Drive Output Test

Notes:

1) By default the TST1 in test mode is also used as RX UART input.

OverCurrent/Current Limit Test (testmodereg = 8)

The IRDM983-025MB, IRDM983-035MB has an on-chip multi-threshold comparator whose eight levels are selected based on the die temperature. testmodereg=8 allows the selection of the thresholds by the currentlimitthrset register accordingly with the following Table.

Selection	Threshold (mV)	currentlimitthrset[2]	currentlimitthrset[1]	currentlimitthrset[0]
0	250	0	0	0
1	250	0	0	1
2	375	0	1	0
3	500	0	1	1
4	625	1	0	0
5	700	1	0	1
6	875	1	1	0
7	1000	1	1	1

Table B-4 Overcurrent/Current Limit Test

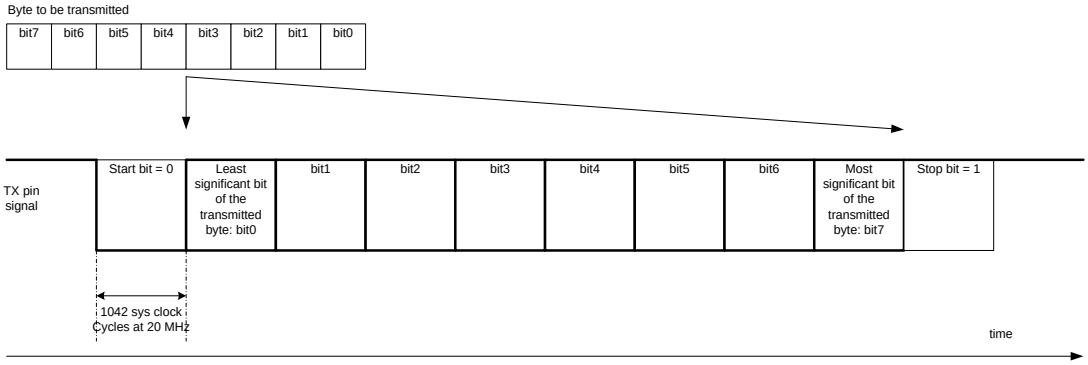
The overcurrent comparator output is observable through the pin PG (direct status of the comparator) or through the PWM outputs (disabled when the comparator is active).

UART behavior during test mode

In the IRDM983-025MB, IRDM983-035MB, a UART is embedded in the design to add visibility and testability to the device. A simple protocol is implemented and specified in the next paragraph. In UART mode the pin TST1 is the UART RX pin while the pin PG is the UART TX signal. During this test the device must be clocked using 20MHz. Bits are sent in the channel following the Rs232 protocol.

CLKIN frequency	**20MHz**
Baud rate	**19200**
Parity	**None**
Start bit	**1**
Stop bit	**1**
Delimiters	**None**

Table B-5 UART setting for Test Mode



When used in test mode, the IRDM983-025MB, IRDM983-035MB IC includes an RS-232 interface channel that provides a direct connection to the host PC or processor. The software interface combines a basic "register map" control method with a simple communication protocol to accommodate potential communication errors.

B.3 RS-232 Register Write Access

A Register write operation consists of a command/address byte, byte count, register data and checksum. When the IRDM983-025MB, IRDM983-035MB receives the register data, it validates the checksum, writes the register data, and transmits and acknowledgement to the host.

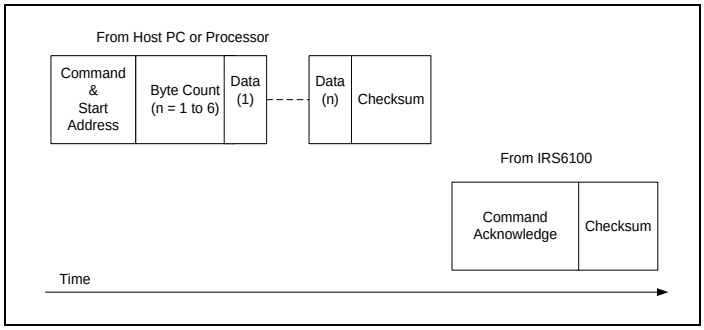


Figure B6 Write Command and Acknowledge Sequence

Command & Start Address Format

Bit Position							
7	6	5	4	3	2	1	0
Command 0 = Write 1 = Read	Register Start Addr Bit 6	Register Start Addr Bit 5	Register Start Addr Bit 4	Register Start Addr Bit 3	Register Start Addr Bit 2	Register Start Addr Bit 1	Register Start Addr Bit 0

Command Acknowledge Format

Bit Position							
7	6	5	4	3	2	1	0
0 = OK 1 = Error	Register Start Addr Bit 6	Register Start Addr Bit 5	Register Start Addr Bit 4	Register Start Addr Bit 3	Register Start Addr Bit 2	Register Start Addr Bit 1	Register Start Addr Bit 0

B.4 Command Acknowledgement Byte Format

The following example shows a command sequence sent from the host to the IRDM983-025MB, IRDM983-035MB requesting a two-byte register write operation:

0x2F Write operation beginning at offset 0x2F
0x02 Byte count of register data is 2
0x00 Data byte 1
0x04 Data byte 2
0x35 Checksum (sum of preceding bytes, overflow discarded)

A good reply from the IRDM983-025MB, IRDM983-035MB would appear as follows:

0x2F Write completed OK at offset 0x2F
0x2F Checksum

An error reply to the command would have the following format:

0xAF Write at offset 0x2F completed in error
0xAF Checksum

B.5 RS-232 Register Read Access

A register read operation consists of a command/address byte, byte count and checksum. When the IRDM983-025MB, IRDM983-035MB receives the command, it validates the checksum and transmits the register data to the host.

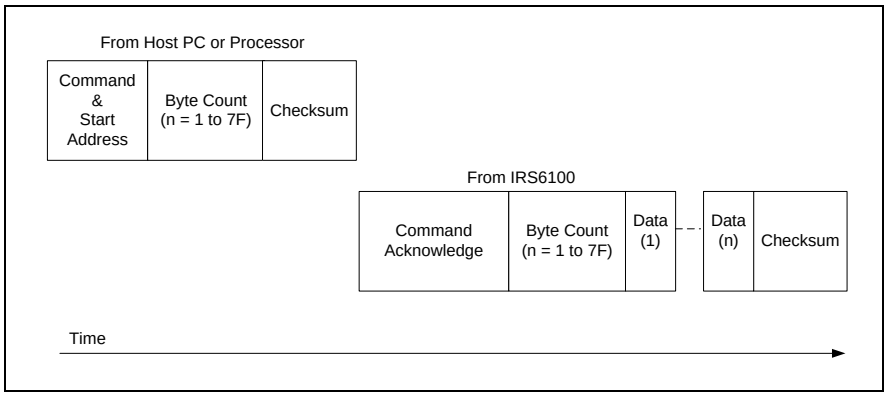


Figure B-7 Read Command and Acknowledge Sequence

The following example shows a command sequence sent from the host to the IRDM983-025MB, IRDM983-035MB requesting four bytes of read register data:
0xA0 Read operation beginning at offset 0x20 (high-order bit selects read operation)
0x04 Requested data byte count is 4
0xA4 Checksum

A good reply from the IRDM983-025MB, IRDM983-035MB might appear as follows:

0x20 Read completed OK at offset 0x20
0x11 Data byte 1
0x22 Data byte 2
0x33 Data byte 3
0x44 Data byte 4
0xCA Checksum

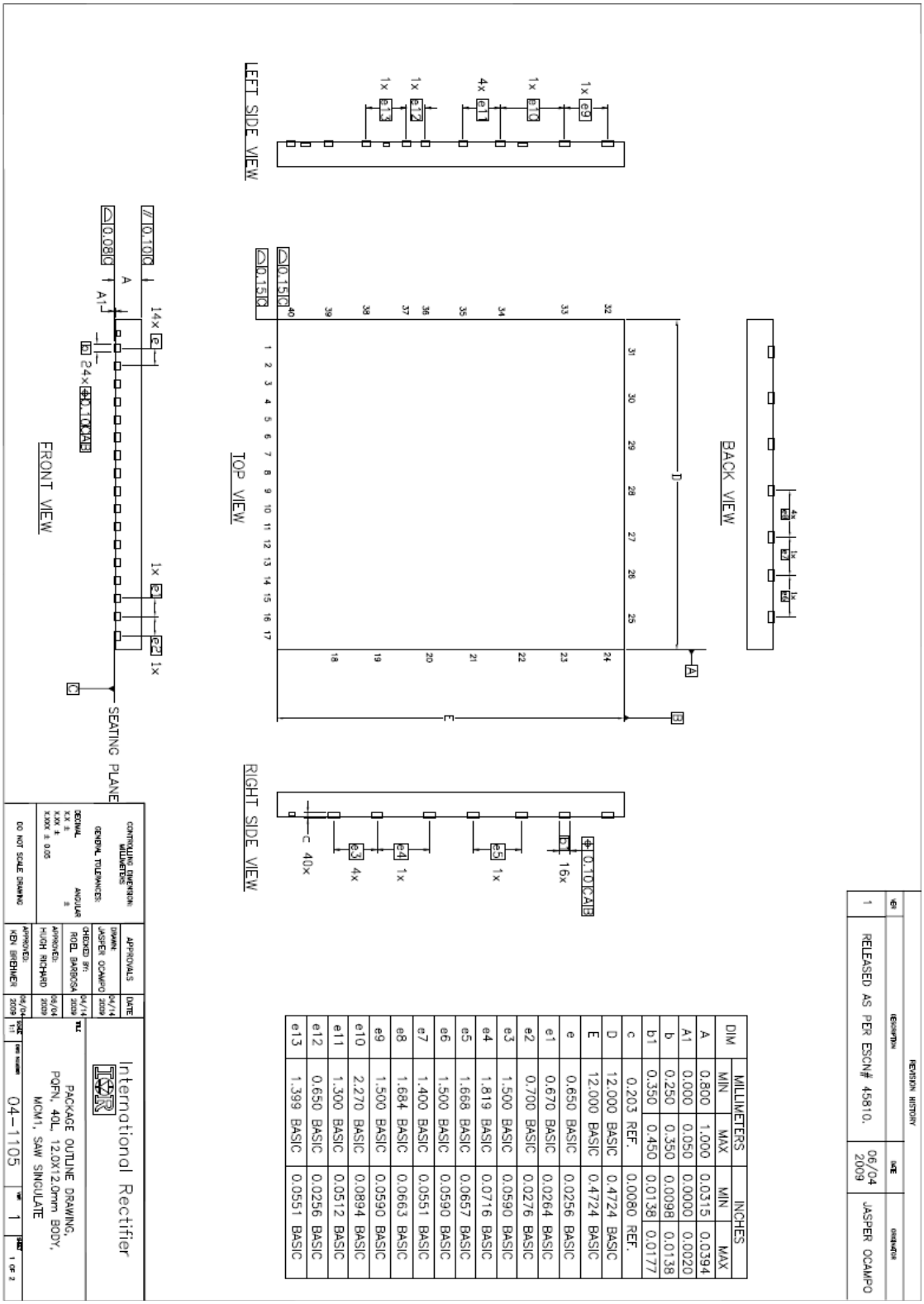
An error reply to the command would have the following format:

0xA0 Read at offset 0x20 completed in error
0xA0 Checksum

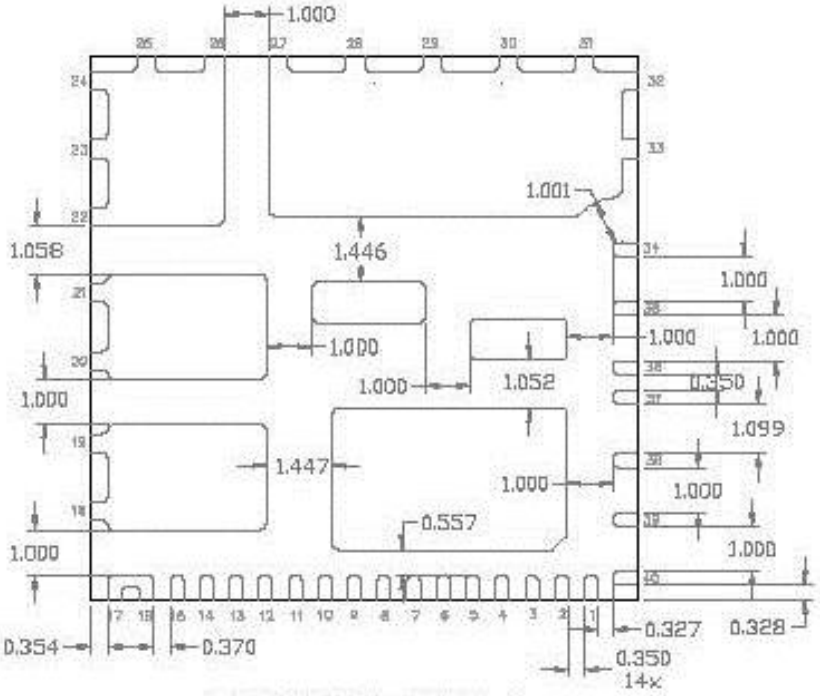
B.6 RS-232 Timeout

The IRDM983-025MB, IRDM983-035MB receiver includes a timer that automatically terminates transfers from the host to the IRDM983-025MB, IRDM983-035MB after a period of 26,214 msec. The timeout applies to an entire command sequence.

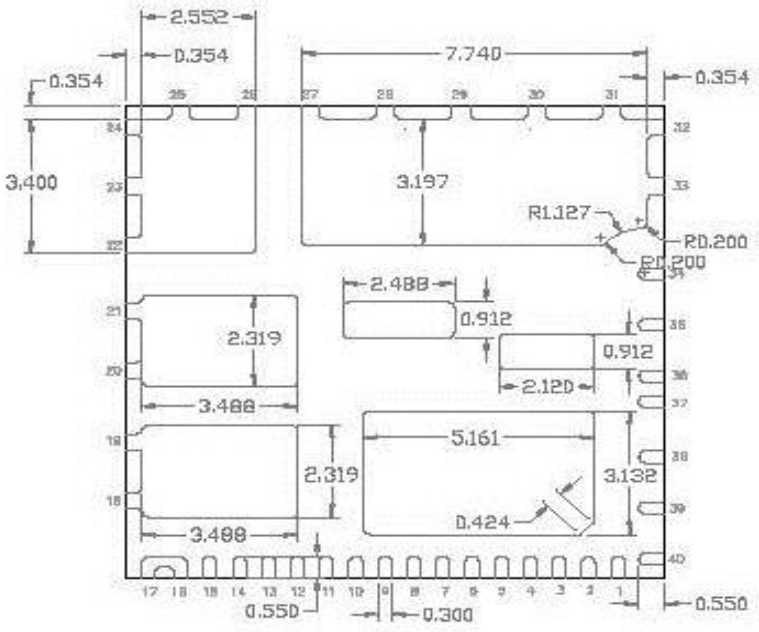
Appendix C. Package Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.800	1.000	0.0315	0.0394
A1	0.000	0.050	0.0000	0.0020
b	0.250	0.350	0.0098	0.0138
b1	0.350	0.450	0.0138	0.0177
c	0.203 REF.		0.0080 REF.	
D	12.000 BASIC		0.4724 BASIC	
E	12.000 BASIC		0.4724 BASIC	
e	0.650 BASIC		0.0256 BASIC	
e1	0.670 BASIC		0.0264 BASIC	
e2	0.700 BASIC		0.0276 BASIC	
e3	1.500 BASIC		0.0590 BASIC	
e4	1.819 BASIC		0.0716 BASIC	
e5	1.668 BASIC		0.0657 BASIC	
e6	1.500 BASIC		0.0590 BASIC	
e7	1.400 BASIC		0.0551 BASIC	
e8	1.684 BASIC		0.0663 BASIC	
e9	1.500 BASIC		0.0590 BASIC	
e10	2.270 BASIC		0.0894 BASIC	
e11	1.300 BASIC		0.0512 BASIC	
e12	0.650 BASIC		0.0256 BASIC	
e13	1.399 BASIC		0.0551 BASIC	

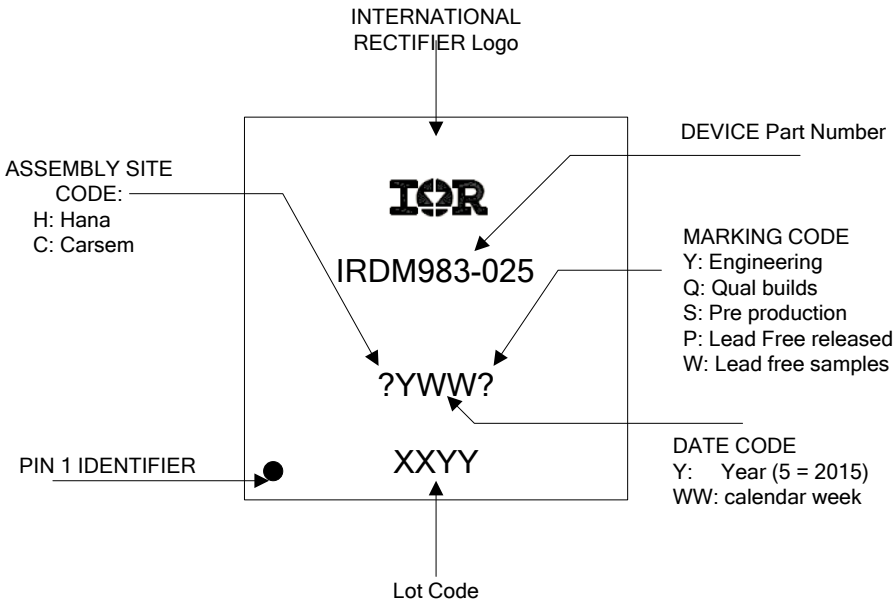


BOTTOM VIEW– DETAIL 1



BOTTOM VIEW– DETAIL 2

Appendix D. Package Marking



Part number	Internal MOSFET
IRDM983-025MB	500V 2A
IRDM983-035MB	500V 3A

Part number location:
Center top

Appendix E. Soldering temperature profile

The following soldering temperature profile is recommended. Any temperature which may exceed those indicated below is not recommended and may cause a permanent damage to the physical component such as deformation.

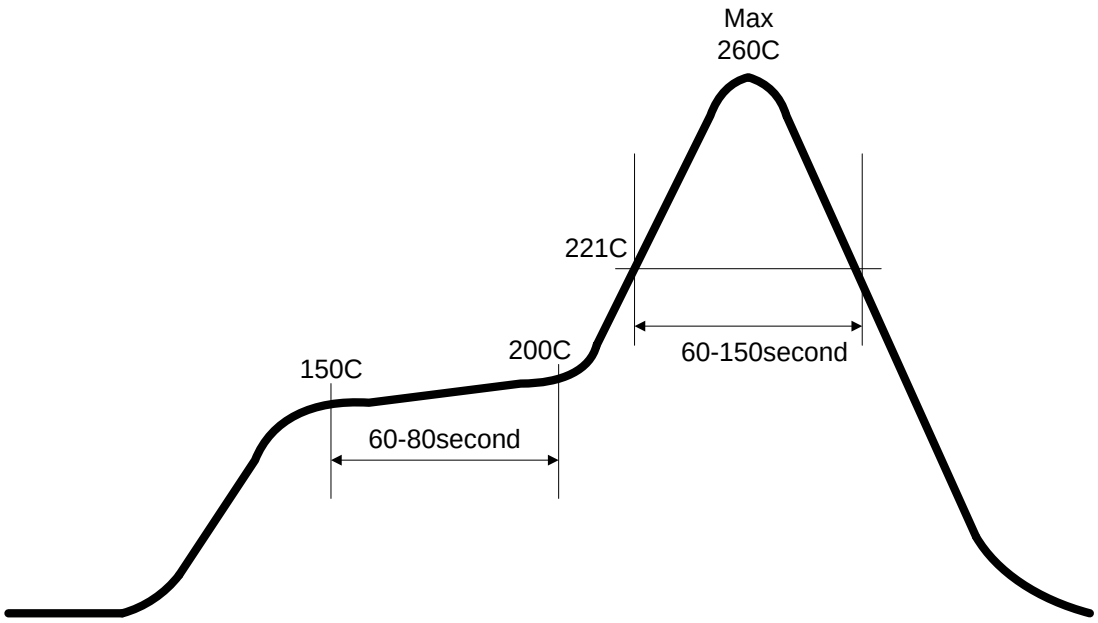


Figure F.1 Recommended soldering temperature profile

Condition	Value	Remark
Temperature rise rate	3°C	
Temperature fall rate	6°C	
Number of reflow	2	
Manual soldering temperature	260°C	
Manual soldering time	10 second	

Table 1 Recommended soldering reflow condition

Edition 2015-03-22

Published by

Infineon Technologies AG

81726 München, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”) .

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer’s compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer’s products and any use of the product of Infineon Technologies in customer’s applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer’s technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (www.infineon.com).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies’ products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.