IR3825

20A Highly Integrated Single-Input Synchronous Sup*IR*Buck® Regulator

Datasheet

Rev 3.7, 03/24/2016

Power Management & Multimarket

1 Product Overview

Features

- Single 5V to 21V application
- Wide Input Voltage Range from 1.0V to 21V with external Vcc
- Output Voltage Range: 0.6V to 0.86×Vin
- Enhanced Line/Load Regulation with Feed-Forward
- Programmable Switching Frequency up to 1.5MHz
- Internal Digital Soft-Start
- Three selectable current limits
- Enable input with Voltage Monitoring Capability
- Thermally Compensated Internal Over-Current Protection with Three selectable settings
- Enhanced Pre-Bias Start-Up
- Precision Reference Voltage (0.6V+/-0.6%)
- Integrated MOSFET drivers and Bootstrap Diode
- Thermal Shut Down
- Programmable Power Good Output
- Monotonic Start-Up
- Operating temp: -40°C < Tj < 125°C
- Small Size: PQFN 5 mm x 6 mm
- Lead-free, Halogen-free and RoHS Compliant

Description

The IR3825 SupIRBuck® is an easy-to-use, fully integrated and highly efficient DC/DC regulator. The onboard PWM controller and MOSFETs make IR3825 a space-efficient solution, providing accurate power delivery.

IR3825 is a versatile regulator, operating with wide input and output voltage range, which offers programmable switching frequency from 300kHz to 1.5MHz, and three selectable current limits.

It features important protection functions, such as Pre-Bias startup, thermally compensated current limit, over voltage protection and thermal shutdown to give required system level security in the event of fault conditions.

Applications

- Server Applications
- Netcom Applications
- Storage Applications
- Telecom Applications
- Distributed Point of Load Power Architectures

Table 1-1 Enterprise Controller Offerings

Part Number	Package Type	Standard Pack		Part Number
		Form	Quantity	
IR3825	PQFN 5 mm x 6 mm	Tape and Reel	4000	IR3825MTRPBF

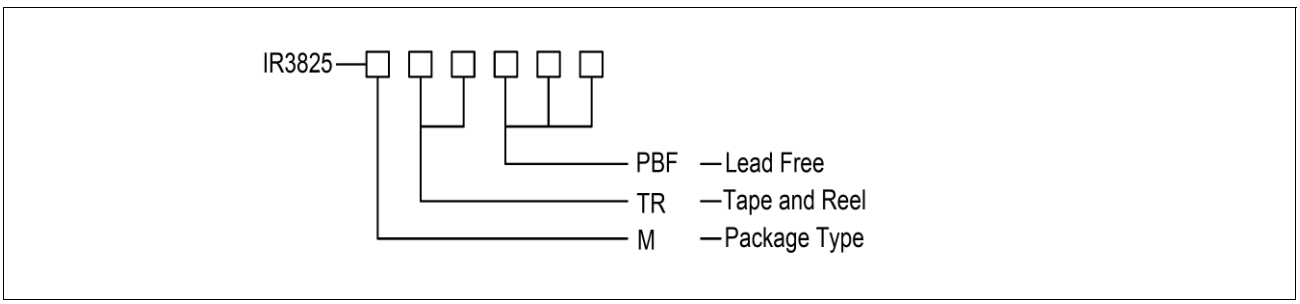


Figure 1-1 IR3825 Part Number Configuration Code

2 Basic Application

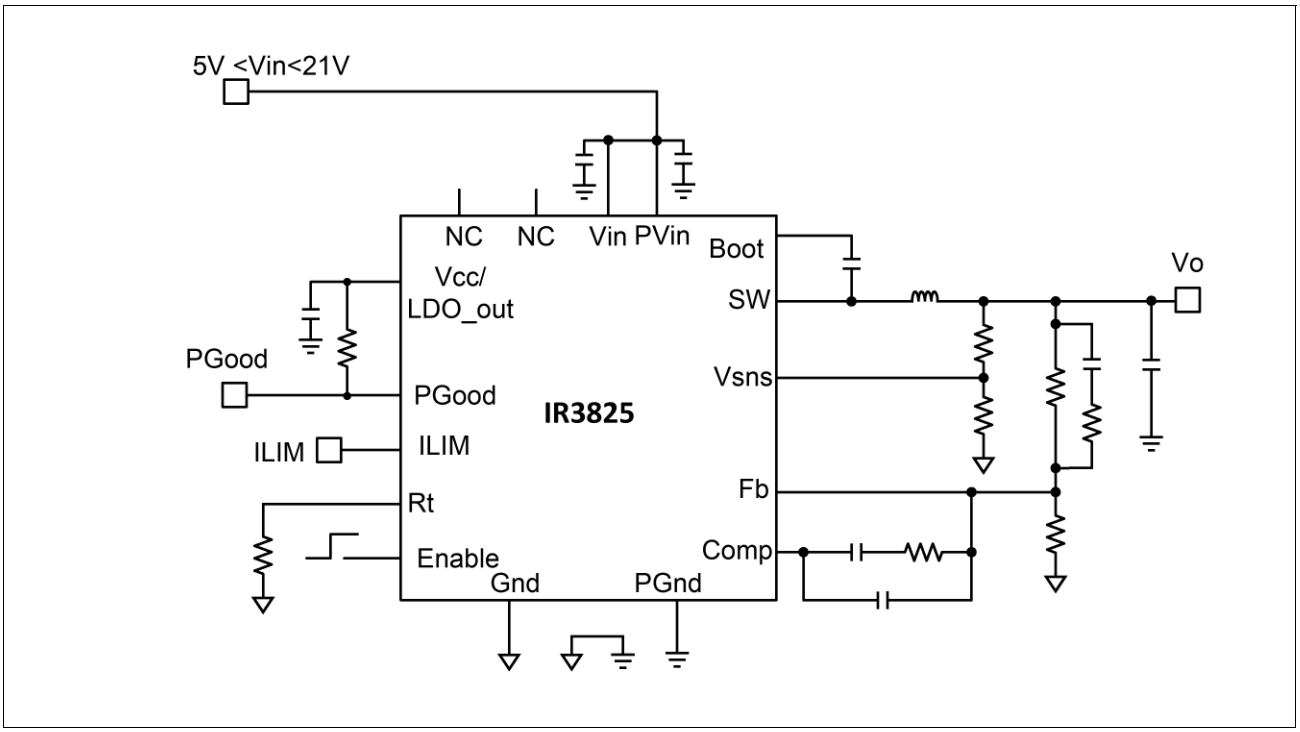


Figure 2-1 IR3825 Basic Application Circuit

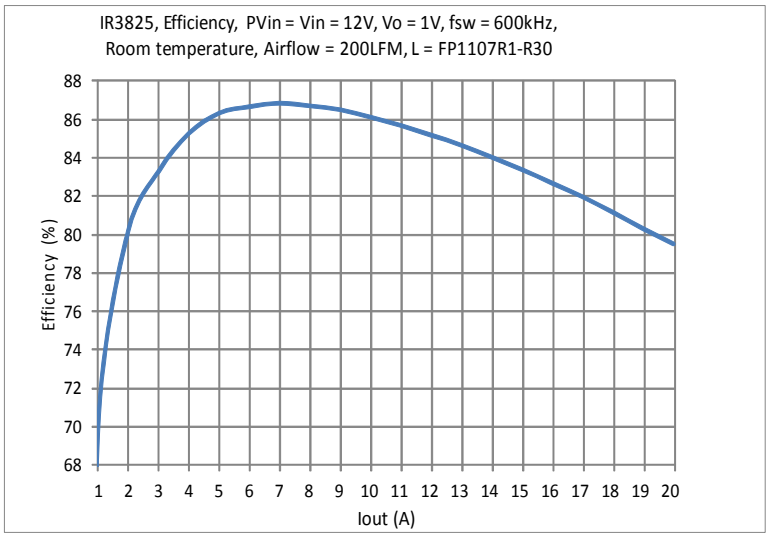


Figure 2-2 IR3825 Efficiency

3 Block Diagram

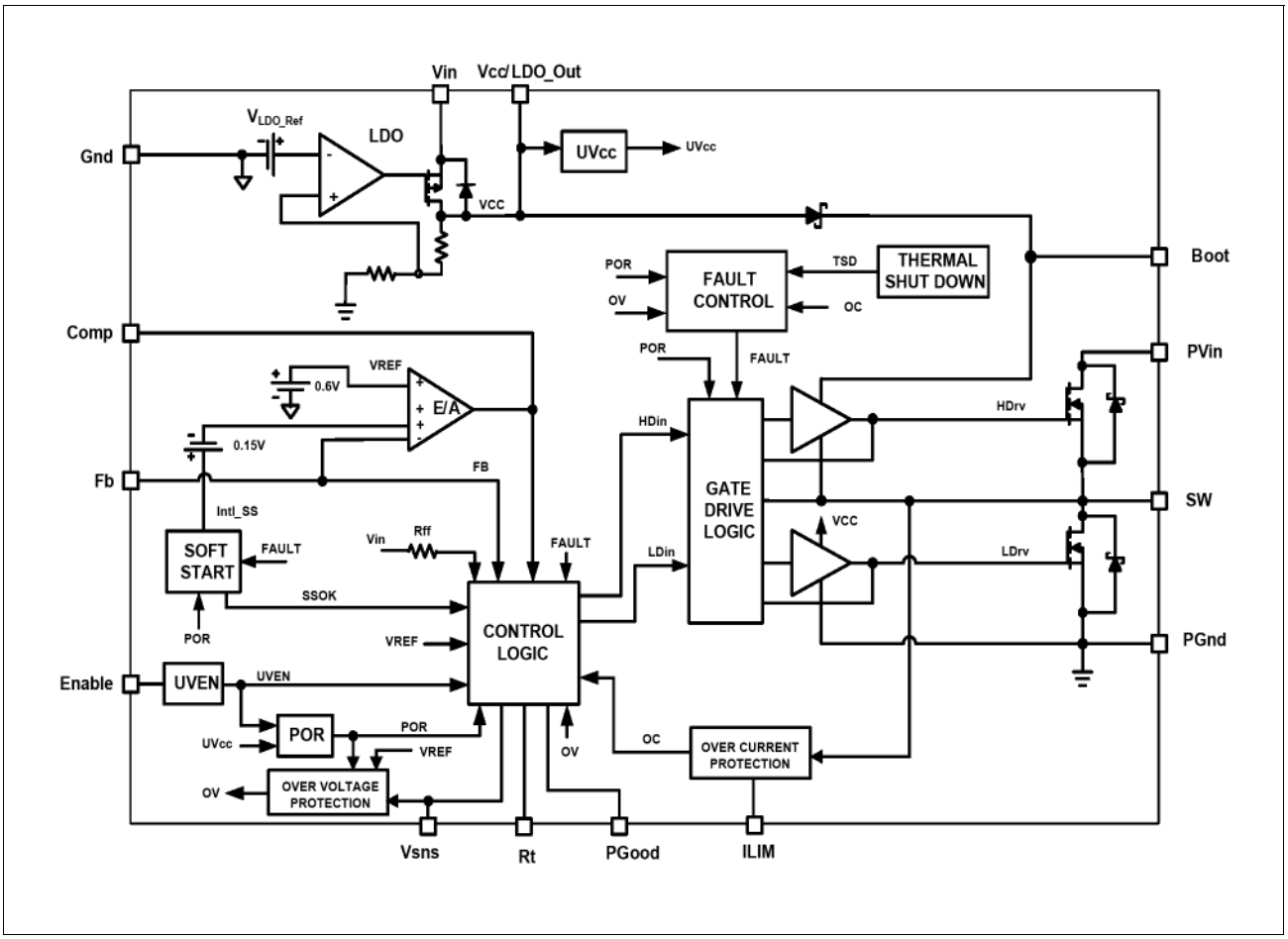


Figure 3-1 Simplified block diagram

4 Pinout Diagram and Pin Description

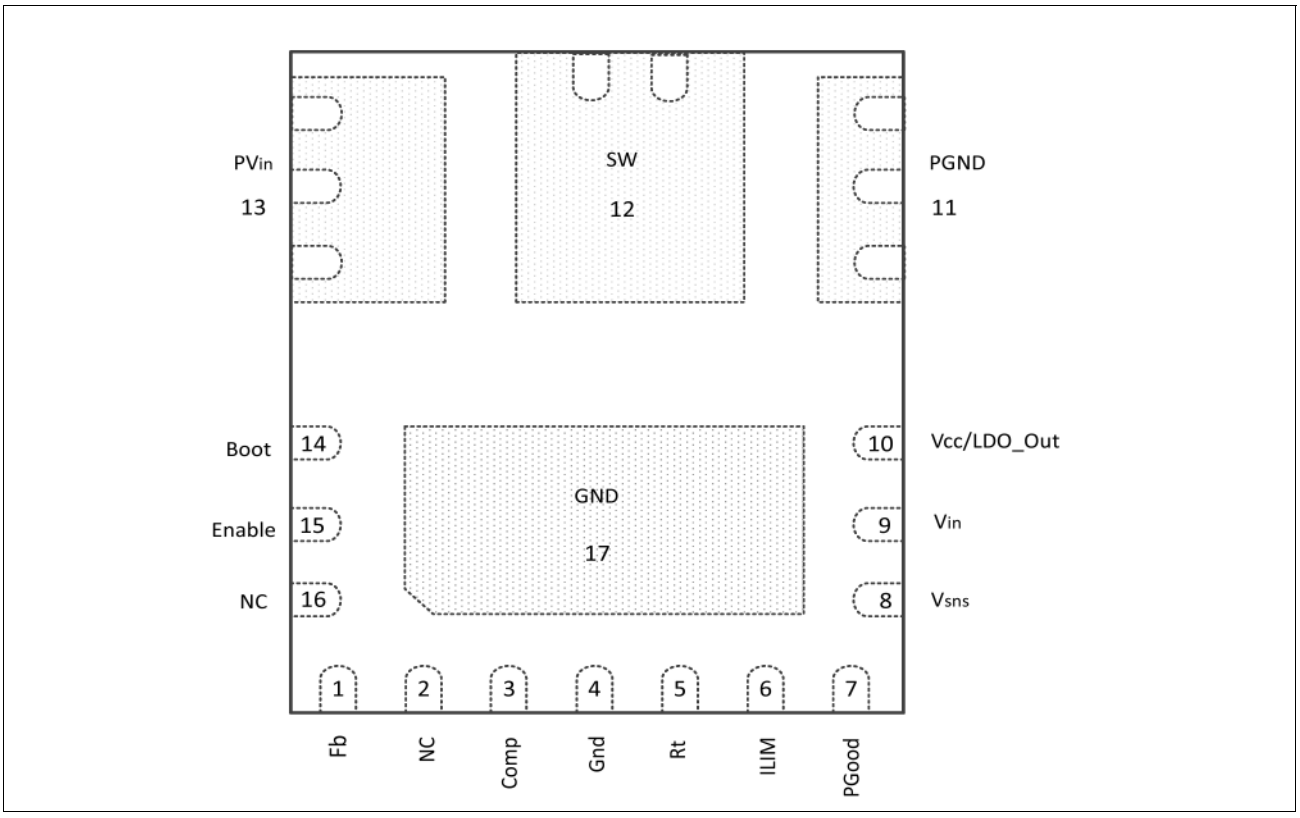


Figure 4-1 Pinout Diagram: PQFN 5 mm x 6 mm (Top View)

Table 4-1 Pin Description

Pin No.	Name	Pin Type	Function
1	Fb	I	Inverting input to the error amplifier. This pin is connected directly to the output of the regulator via resistor divider to set the output voltage and provide feedback to the error amplifier.
2	NC	-	Do Not Connect. Must be left floating.
3	Comp	O	Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to Fb to provide loop compensation.
4	Gnd	S	Signal ground for internal reference and control circuitry.
5	Rt	I	Set switching frequency. Use an external resistor from this pin to Gnd to set the free-running switching frequency.
6	ILIM	I	Current Limit set point. This pin allows the trip point to be set to one of three possible settings by either floating this pin, connecting it to VCC or connecting it to PGnd.
7	PGood	O	Power Good status output pin is open drain. Connect a pull up resistor from this pin to the voltage lower than or equal to the Vcc.
8	Vsns	I	Sense pin for over-voltage protection and PGood.

Table 4-1 Pin Description

Pin No.	Name	Pin Type	Function
9	Vin	S	Input voltage for Internal LDO. A 1.0µF capacitor should be connected between this pin and PGnd. If external supply is connected to Vcc/LDO_out pin, this pin should be shorted to Vcc/LDO_out pin.
10	Vcc/LDO_Out	I/O	Input Bias for external Vcc Voltage/ output of internal LDO. Place a minimum 2.2µF cap from this pin to PGnd
11	PGnd	S	Power Ground. This pin serves as a separated ground for the MOSFET drivers and should be connected to the system's power ground plane.
12	SW	O	Switch node. This pin is connected to the output inductor.
13	PVin	S	Input voltage for power stage.
14	Boot	I	Supply voltage for high side driver, a 100nF capacitor should be connected between this pin and SW pin.
15	Enable	I	Enable pin to turn on and off the device, if this pin is connected to PVin pin through a resistor divider, input voltage UVLO can be implemented.
16	NC	-	Do Not Connect. Must be left floating.
17	GND	S	Signal ground for internal reference and control circuitry.

5 Specifications

5.1 Absolute Maximum Ratings

Stresses beyond those listed in **Table 5-1** may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

Table 5-1 Absolute Maximum Ratings

Parameter	Min	Max	Units	Conditions
PVin, Vin	-0.3	25	V	
Vcc / LDO_Out	-0.3	8.0	V	**Note 1**
Boot	-0.3	33	V	
SW	-0.3	25	V	(DC)
	-4.0	25	V	(AC, 100ns)
Boot to SW	-0.3	VCC + 0.3	V	**Note 2**
ILIM, PGood	-0.3	VCC + 0.3	V	**Note 2**
Other Input/Output Pins	-0.3	3.9	V	
PGnd to Gnd	-0.3	0.3	V	
Junction Temperature Range	-40	150	^{o}C	**Note 1**
Storage Temperature Range	-55	150	^{o}C	

Note 1: Vcc must not exceed 7.5V for Junction Temperature between -10°C and -40°C

Note 2: Must not exceed 8V

Table 5-2 Thermal Information

Parameter	Value / Units	Condition
Junction-to-ambient thermal resistance θ_{JA}	30 ^{o}C/W	**Note 3**
Junction to PCB thermal resistance $\theta_{J\text{-}PCB}$	2 ^{o}C/W	

Note 3: θ_{JA} is measured with components mounted on a high effective thermal conductivity test board in free air.

5.2 Recommended Operating Conditions

Table 5-3 Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units	Condition
PVin	Power Stage Input Voltage Range	1	21	V	**Note 4**
Vin	Input Voltage Range	5	21	V	**Note 5**
Vcc	Supply Voltage Range	4.5	7.5	V	**Note 6**
Boot to SW	Boot to Switch Node Voltage Range	4.5	7.5	V	
V_O	Output Voltage Range	0.6	0.86xVin	V	**Note 9**
I_O	Output Current Range	0	20	A	
F_S	Switching Frequency	0.3	1.5	MHz	
T_J	Operating Junction Temperature	-40	125	°C	

Note 4: Maximum SW node voltage should not exceed 25V.

Note 5: For internally biased single rail operation. When Vin drops below 7.5V, the internal LDO enters dropout mode. Please refer to LDO section and Over Current Protection for detailed application information.

Note 6: Vcc/LDO_out can be connected to an external regulated supply. If so, the Vin input should be connected to Vcc/LDO_out pin.

Note 9: For applications with high duty ratio, such as 12V to 5V conversion, sufficient cooling should be applied to help thermal dissipation such as using airflow, large copper area on PCB etc. Reducing switching frequency also helps reduce power losses.

5.3 Electrical Characteristics

Unless otherwise specified, these specifications apply over, 7.5V < Vin = PVin < 21V, 0°C < T_J < 125°C.

Typical values are specified at Ta = 25°C.

Table 5-4 Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Power Stage						
P_{LOSS}	Power Losses	Vin = 12V, V_O = 1.0V, I_O = 20A, Fs = 600kHz, L = 0.3uH, 200LFM,Vcc = 6.9V (internal LDO), **Note 7**	-	5	-	W
$R_{ds(on)\_Top}$	Top Switch	VBoot - Vsw= 6.9V, I_O = 20A, Tj =25°C	-	8.4	10.5	mΩ
$R_{ds(on)\_Bot}$	Bottom Switch	Vcc = 6.9V, I_O = 20A Tj =25°C	-	3.8	4.9	mΩ
	Bootstrap Diode Forward Voltage	I(Boot) = 15mA	200	300	500	mV
I_{SW}	SW Leakage Current	SW = 0V, Enable = 0V	-	-	1	µA
		SW = 0V, Enable = high, No Switching	-	-	1	
T_{db}	Dead Band Time	**Note 7**	-	20	-	ns
Supply Current						

Table 5-4 Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$I_{in(Standby)}$	Vin Supply Current (standby)	EN = Low, No Switching	-	100	150	µA
$I_{in(Dyn)}$	Vin Supply Current (dynamic)	EN = High, Fs = 600kHz, Vin = PVin = 21V	-	20	25	mA
VCC LDO Output						
V_{CC}	Output Voltage	Vin(min) = 7.5V, Icc = 0-50mA, Cload = 2.2uF	6.5	6.9	7.2	V
V_{CC_drop}	VCC Dropout	Icc=50mA,Cload=2.2uF	-	-	0.88	V
Oscillator						
V_{Rt}	Rt Voltage		-	1.0	-	V
F_S	Frequency Range	Rt = 80.6K	270	300	330	kHz
		Rt = 39.2K	540	600	660	
		Rt = 15.0K	1350	1500	1650	
V_{ramp}	Ramp Amplitude	Vin = 7.5V, Vin slew rate max = 1V/µs, **Note 7**	-	1.125	-	Vp-p
		Vin = 12V, Vin slew rate max = 1V/µs, **Note 7**	-	1.80	-	
		Vin = 21V, Vin slew rate max = 1V/µs, **Note 7**	-	3.15	-	
		Vcc = Vin = 5V, For external Vcc operation, **Note 7**	-	0.75	-	
$Ramp_{(OS)}$	Ramp Offset	**Note 7**	-	0.16	-	V
$T_{min(ctrl)}$	Minimum Pulse Width	**Note 7**	-	-	60	ns
D_{max}	Maximum Duty Cycle	Fs = 300kHz, PVin = Vin = 12V	86	-	-	%
T_{off}	Minimum Off Time	**Note 7**	-	200	250	ns
Error Amplifier						
I_{fb} (E/A)	Input Bias Current		-1	-	1	µA
GBWP	Gain-Bandwidth Product	**Note 7**	20	30	40	MHz
Gain	DC Gain	**Note 7**	100	110	120	dB
V_{max} (E/A)	Maximum Output Voltage		1.7	2.0	2.3	V
V_{min} (E/A)	Minimum Output Voltage		-	-	100	mV
Reference Voltage (VREF)						
V_{fb}	Feedback Voltage		-	0.6	-	V
	Accuracy	25°C < Tj < 85°C	-0.6	-	0.6	%
		-40°C < Tj < 125°C, **Note 8**	-1.2	-	1.2	%
Soft Start						
Ramp S-Start	Soft Start Ramp Rate		0.16	0.2	0.24	mV/µs
Power Good						
VPG(on)	Pgood Turn on Threshold	Vsns Rising	85	90	95	% Vref

Table 5-4 Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
VPG (lower)	Pgood Lower Turn off Threshold	Vsns Falling	80	85	90	% Vref
VPG (on)_Dly	Pgood Turn on Delay	Vsns Rising, see VPG(on)	-	2.5	-	ms
VPG (Upper)	Pgood Upper Turn off Threshold	Vsns Rising	115	120	125	% Vref
VPG (comp)_Dly	Pgood Comparator Delay	Vsns < VPG(lower) or Vsns > VPG(upper)	1	2	3.5	µs
PG (voltage)	Pgood Voltage Low	Ipgood = -5mA	-	-	0.5	V
Under Voltage Lockout						
Vcc_UVLO_Start	Vcc-Start Threshold	Vcc Rising Trip Level	3.9	4.1	4.3	V
Vcc_UVLO_Stop	Vcc-Stop Threshold	Vcc Falling Trip Level	3.6	3.8	4.0	V
Enable_UVLO_Start	Enable-Start-Threshold	Supply ramping up	1.14	1.2	1.26	V
Enable_UVLO_Stop	Enable-Stop-Threshold	Supply ramping down	0.95	1	1.05	V
I_{en}	Enable Leakage Current	Enable = 3.3V	-	-	1	µA
Over Voltage Protection						
OVP_Vth	OVP Trip Threshold	Vsns Rising	115	120	125	% Vref
OVP_Tdly	OVP Comparator Delay		1	2	3.5	µs
Over Current Protection						
I_{LIMIT}	Current Limit	ILIM = VCC, VCC = 6.9V, Tj = 25°C	22.5	26	30.4	A
		ILIM = f loating, VCC = 6.9V, Tj = 25°C	17.8	21.5	25.2	
		ILIM = PGnd, VCC = 6.9V, Tj = 25°C	13.9	16.8	19.7	
T_{blk_Hiccup}	Hiccup Blanking Time		-	20.48	-	ms
Over Temperature Protection						
T_{tsd}	Thermal Shutdown Threshold	**Note 7**	-	145	-	°C
T_{tsd_hys}	Hysteresis	**Note 7**	-	20	-	°C

Note 7: Ensured by design but not tested in production.

Note 8: Hot and Cold temperature performance is assured via correlation using statistical quality control. Not tested in production.

5.4 Typical Efficiency and Power Loss Curves

PV_{in} = V_{in} = 12V, V_{CC} = Internal LDO, I_O = 0A - 20A, Room Temperature, 200LFM Air Flow. Note that the efficiency and power loss curves include the losses of IR3825, the inductor losses and the losses of the input and output capacitors. The table shows the inductors used for each of the output voltages in the efficiency measurement.

Table 5-5 Inductor List for IR3825 Efficiency Measurement: PV_{in} = V_{in} = 12V

VOUT (V)	F_S (kHz)	LOUT (µH)	P/N	DCR (mΩ)	Size (mm)
1.0	600	0.3	FP1107R1-R30-R (Coiltronics)	0.29	11.0 x 7.2 x 7.5
1.2	600	0.3	FP1107R1-R30-R (Coiltronics)	0.29	11.0 x 7.2 x 7.5
1.8	600	0.3	FP1107R1-R30-R (Coiltronics)	0.29	11.0 x 7.2 x 7.5
3.3	600	0.56	IHLP-5050FD-A1 (Vishay)	1.2	13.26 x 12.9 x 6.4

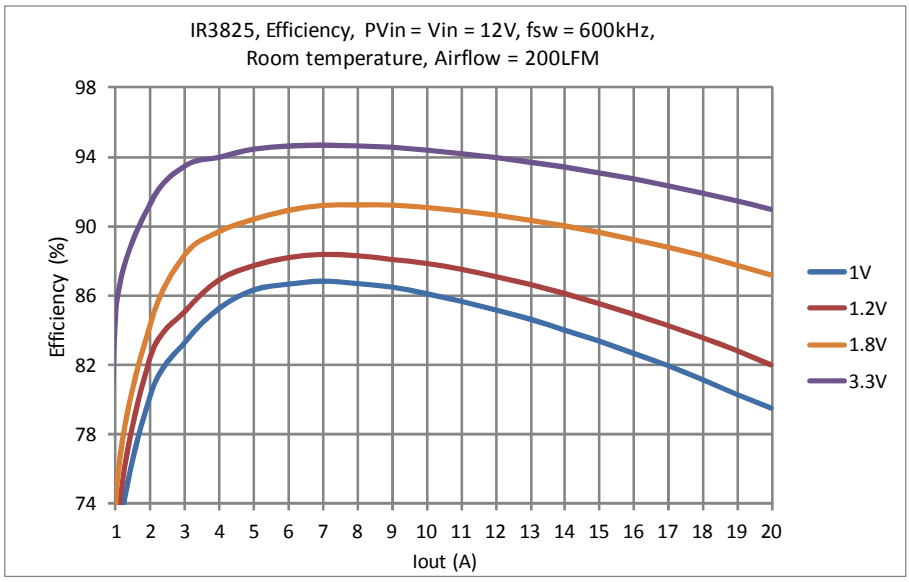


Figure 5-1 IR3825 Efficiency Curves - PV_{in} = V_{in} = 12V, V_{CC} = Internal LDO

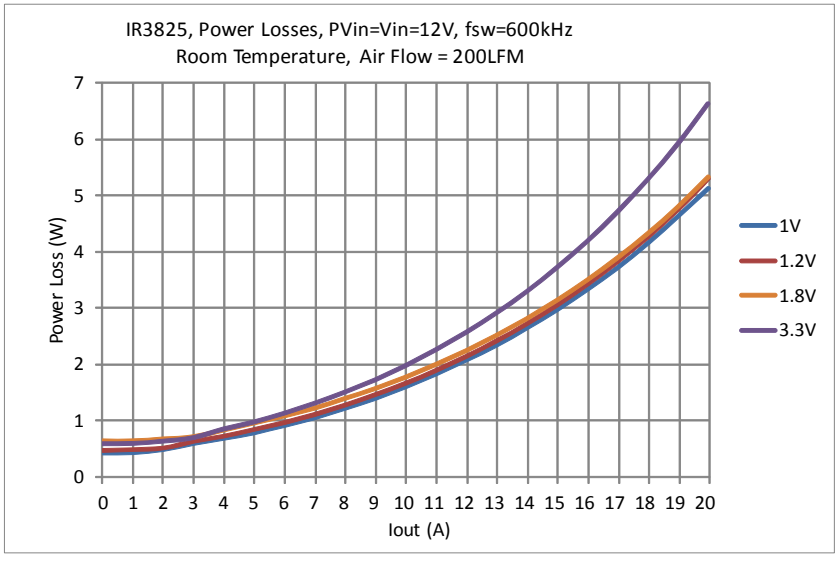


Figure 5-2 IR3825 Power Loss Curves- PV_{in} = V_{in} = 12V, V_{CC} = Internal LDO

PV_{in} = V_{in} = V_{CC} = 5V, I_O = 0A-20A, Room Temperature, 200LFM Air Flow. Note that the efficiency and power loss curves include the losses of IR3825, the inductor losses and the losses of the input and output capacitors. The table shows the inductors used for each of the output voltages in the efficiency measurement.

Table 5-6 Inductor List for IR3825 Efficiency Measurement: PV_{in} = V_{in} = V_{CC} = 5V

VOUT (V)	F_S (kHz)	LOUT (µH)	P/N	DCR (mΩ)	Size (mm)
1.0	600	0.23	FP1107R1-R23-R (Coiltronics)	0.29	11.0 x 7.2 x 7.5
1.2	600	0.23	FP1107R1-R23-R (Coiltronics)	0.29	11.0 x 7.2 x 7.5
1.8	600	0.3	FP1107R1-R30-R (Coiltronics)	0.29	11.0 x 7.2 x 7.5

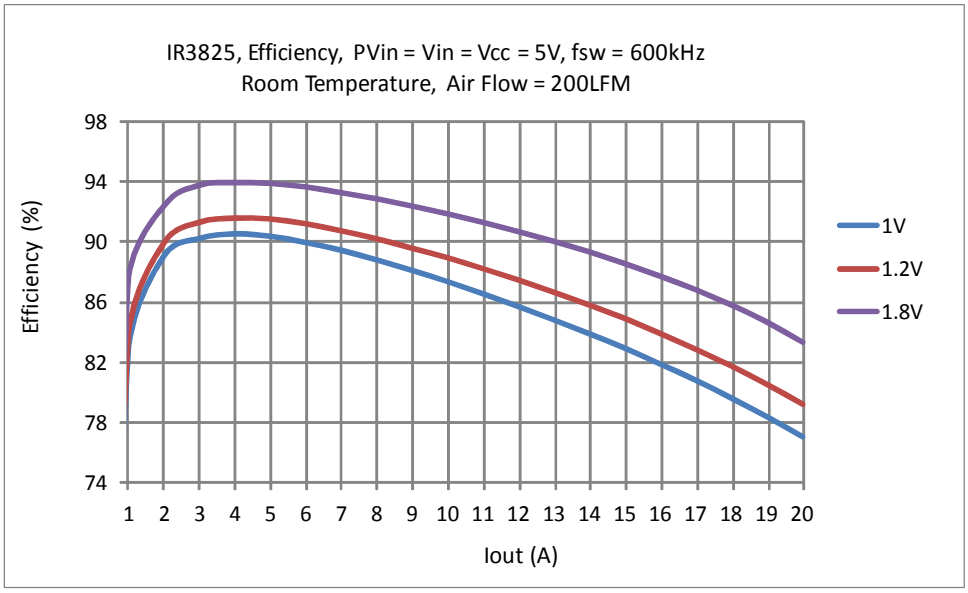


Figure 5-3 IR3825: Efficiency Curves - PV_{in} = V_{in} = V_{CC} = 5V

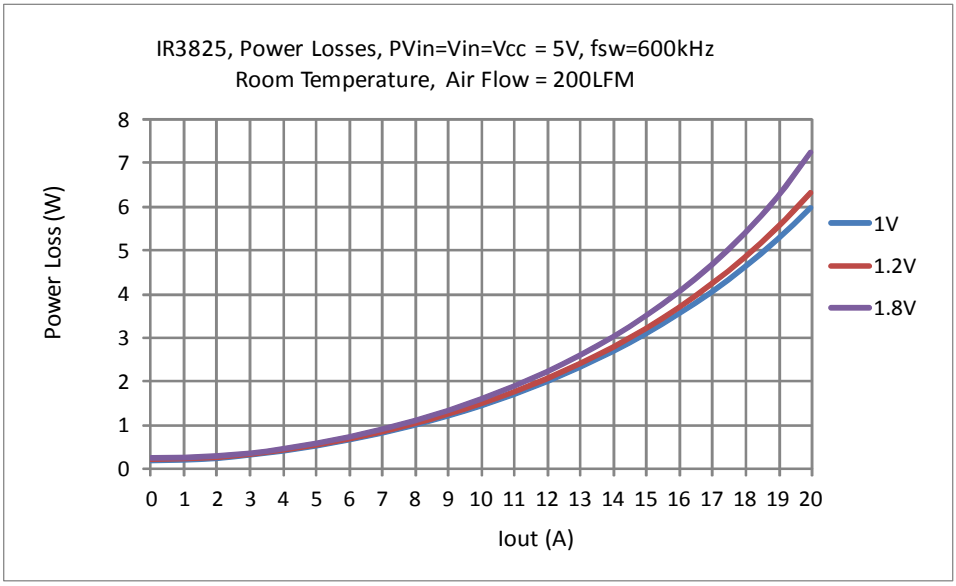


Figure 5-4 IR3825: Power Loss Curves- PV_{in} = V_{in} = V_{CC} = 5V

5.5 $R_{DS(ON)}$ of MOSFETs over Temperature

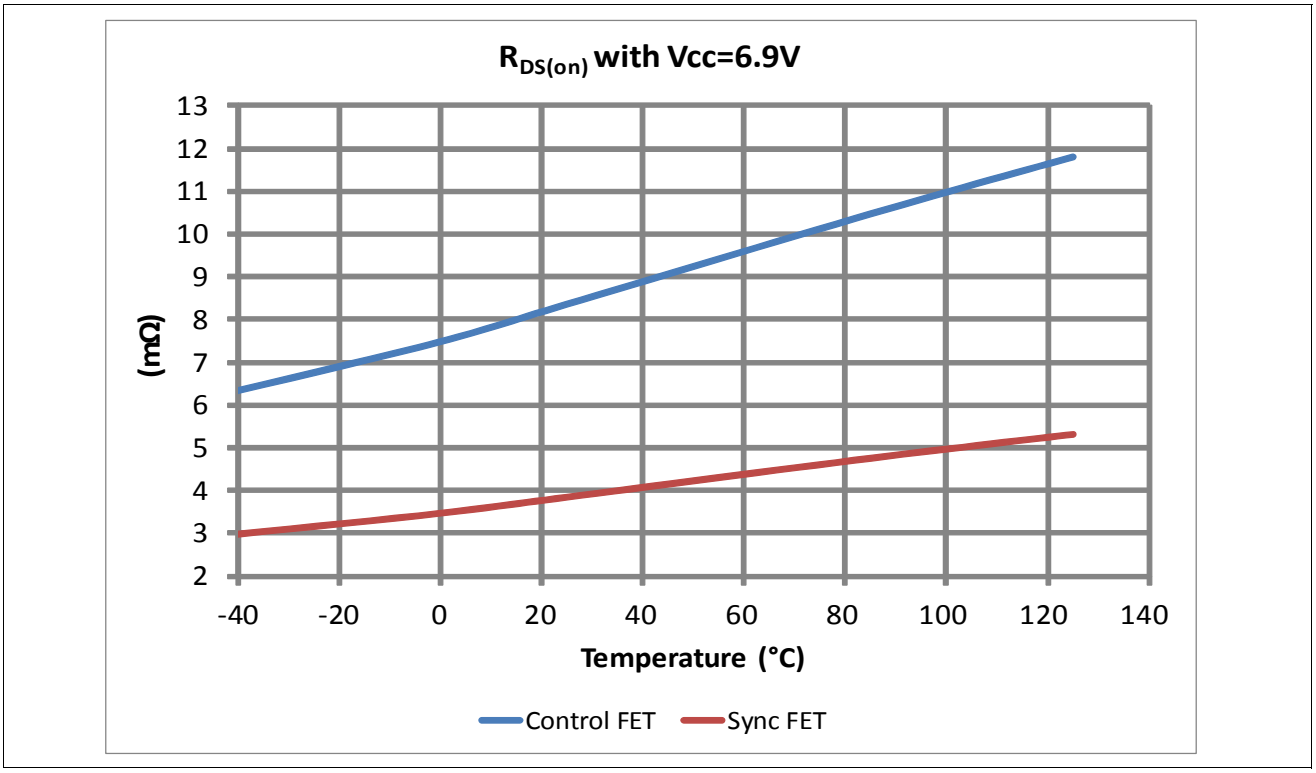


Figure 5-5 $R_{DS(ON)}$ with V_{CC} = 6.9V Over Temperature

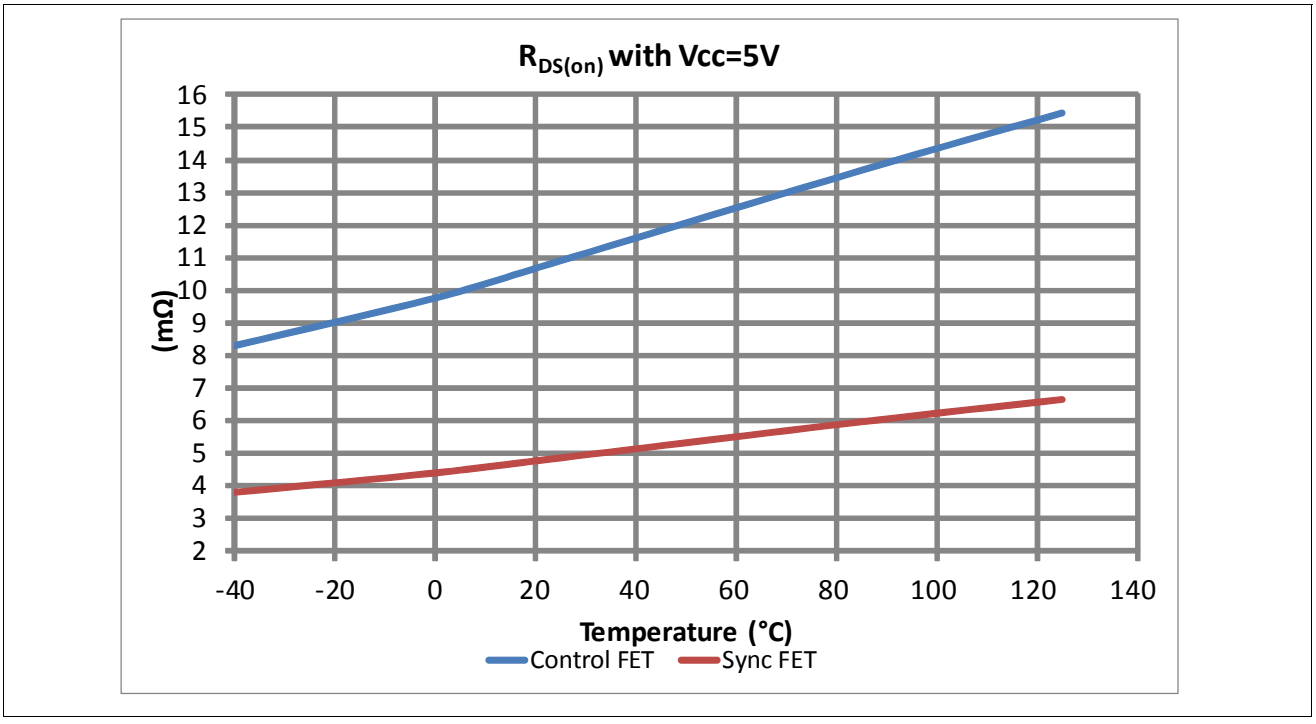


Figure 5-6 $R_{DS(ON)}$ with V_{CC} = 5.0V Over Temperature

5.6 Typical Operating Characteristics -40°C To +125°C

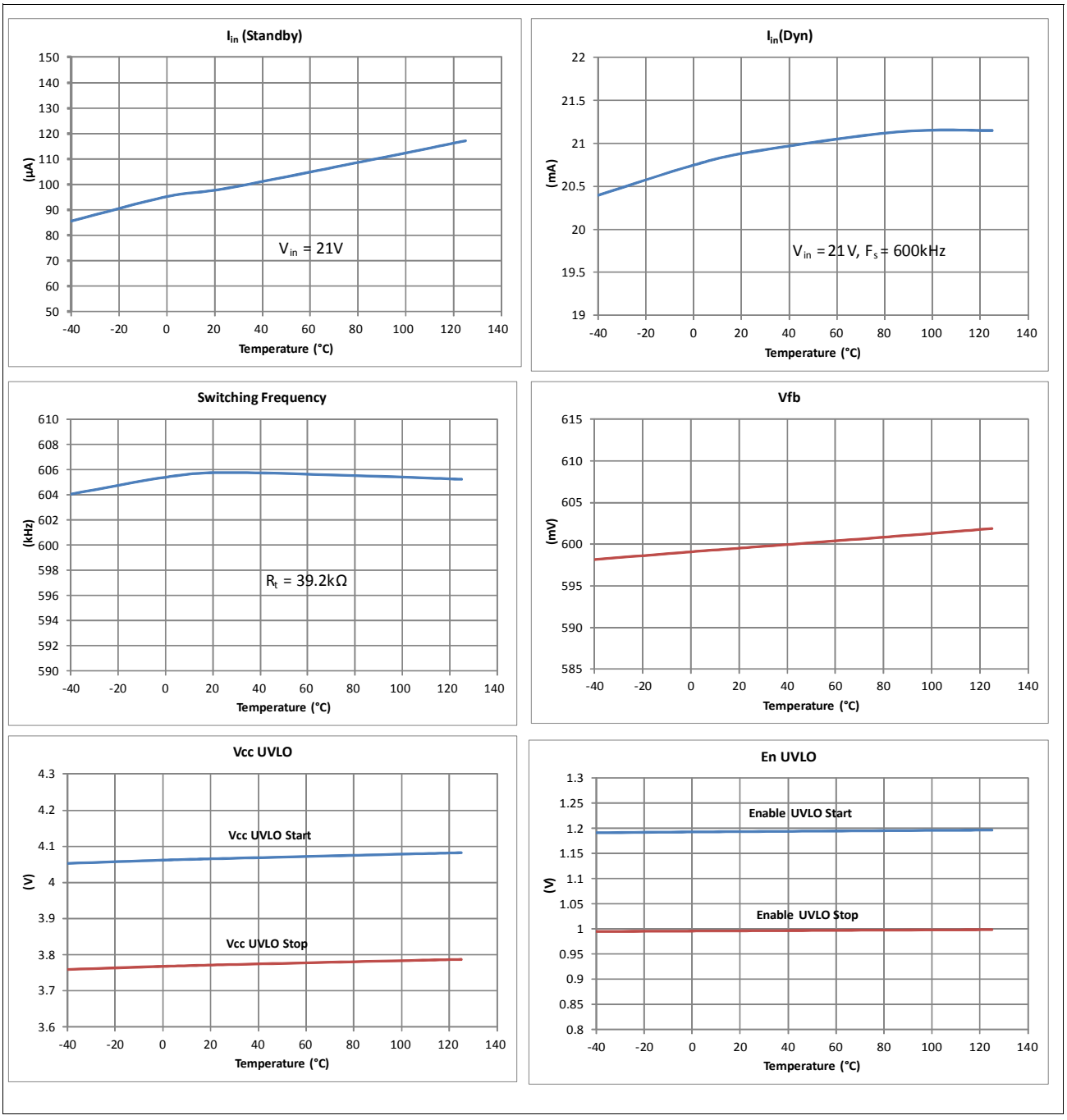


Figure 5-7 Typical Operation Characteristics (Set 1 of 2)

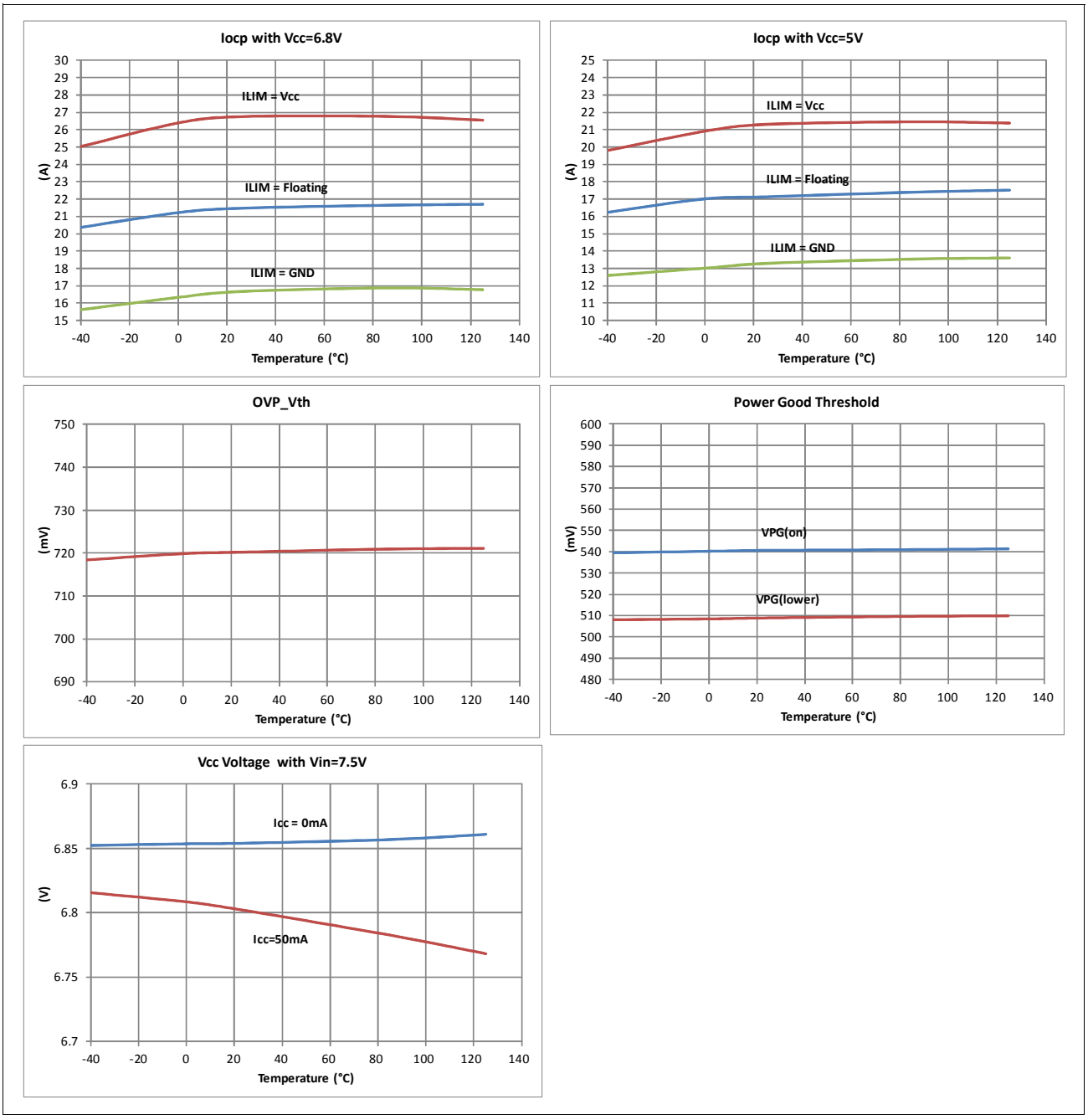


Figure 5-8 Typical Operation Characteristics (Set 2 of 2)

6 Theory of Operation

The IR3825 uses a PWM voltage mode control scheme with external compensation to provide good noise immunity and maximum flexibility in selecting inductor values and capacitor types.

The switching frequency is programmable from 300 kHz to 1.5MHz and provides the capability of optimizing the design in terms of size and performance. IR3825 provides precisely regulated output voltage programmed via two external resistors from 0.6V to 0.86*Vin.

The IR3825 operates with an internal bias supply (LDO) which is connected to the Vcc/LDO_out pin. This allows operation with single supply. The IC can also be operated with an external supply from 4.5 to 7.5V, allowing an extended operating input voltage (PVin) range from 1.0V to 21V. For using the internal LDO supply, the Vin pin should be connected to PVin pin. If an external supply is used, it should be connected to Vcc/LDO_Out pin and the Vin pin should be shorted to Vcc/LDO_Out pin.

The device utilizes the on-resistance of the low side MOSFET (sync FET) for over current protection. This method enhances the converter's efficiency and reduces cost by eliminating the need for external current sense resistor. IR3825 includes two low $R_{ds(on)}$ MOSFETs using Infineon's HEXFET technology. These are specifically designed for high efficiency applications.

6.1 Voltage Loop Compensation Design

The IR3825 uses PWM voltage mode control. The output voltage of the POL, sensed by a resistor divider, is fed into an internal Error Amplifier (E/A). The output of the E/R is then compared to an internal ramp voltage to determine the pulse width of the gate signal for the control FET. The amplitude of the ramp voltage is proportional to V_{in} so that the bandwidth of the voltage loop remains almost constant for different input voltages. This feature is called input voltage feedfoward. It allows the feedback loop design independent of the input voltage. Please refer to the feedforward section for more information.

A RC network has to be connected between the FB pin and the COMP pin to form a feedback compensator. The goal of the compensator design is to achieve a high control bandwidth with a phase margin of 45° or above. The high control bandwidth is beneficial for the loop dynamic response, which helps to reduce the number of output capacitors, the PCB size and the cost. A phase margin of 45° or higher is desired to ensure the system stability. The proprietary PWM modulator in IR3825 significantly reduces the PWM jittering, allowing the control bandwidth in the range of $1/10^{th}$ to $1/5^{th}$ of the switching frequency.

Two types of compensators, Type II (PI) and Type III (PID), are commonly used. The selection of the compensation type is dependent on the ESR of the output capacitors. Electrolytic capacitors have relatively higher ESR. If the ESR pole is located at the frequency lower than the cross-over frequency, F_C, the ESR pole will help to boost the phase margin. Thus a type II compensator can be used. For the output capacitors with lower ESR such as ceramic capacitors, type III compensation is often desired.

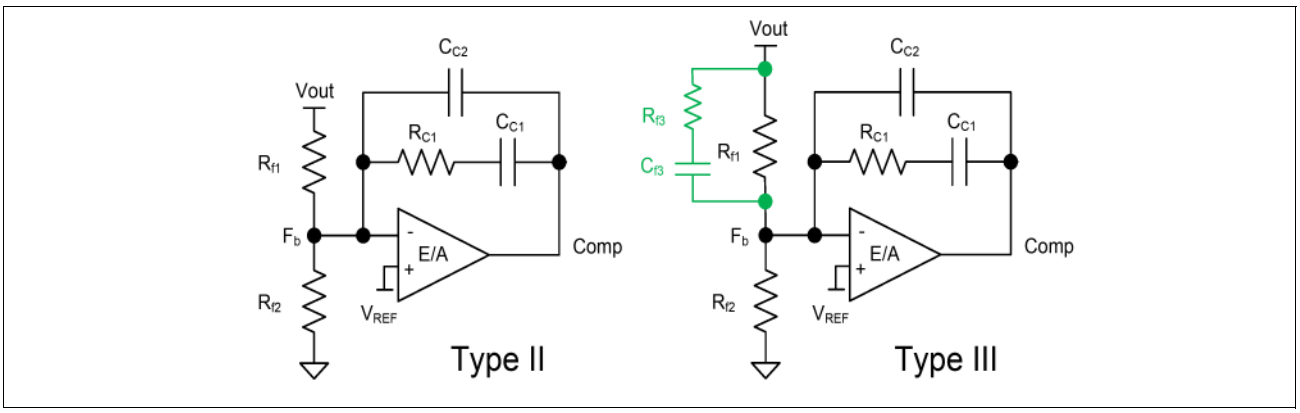


Figure 6-1 Loop Compensators

Table 6-1 lists the compensation selection for different types of output capacitors.

For more detailed design guideline of voltage loop compensation, please refer to the application note AN-1162, “Compensation Design Procedure for Buck Converter with Voltage-Mode Error-Amplifier”. SupBuck design tool is also available at (**www.infineon.com**) providing the reference design based on user’s design requirements.

Table 6-1 Recommended Compensation Type

Compensator	Location of Cross-Over Frequency	Type of Output Capacitors
Type II (PI)	$F_{LC} < F_{ESR} < F_O < F_S / 2$	Electrolytic, POS-CAP, SP-CAP
Type III-A (PID)	$F_{LC} < F_O < F_{ESR} < F_S / 2$	POS-CAP, SP-CAP
Type III-B (PID)	$F_{LC} < F_O < F_S / 2 < F_{ESR}$	Ceramic

F_{LC} is the resonant frequency of the output LC filter. It is often referred to as double pole.

F_{ESR} is the ESR zero of the output capacitor.

F_O is the cross-over frequency of the control loop and F_S is the switching frequency.

$$F_{LC} = \frac{1}{2 \times \pi \sqrt{L_o \times C_o}} \qquad F_{ESR} = \frac{1}{2\pi \times ESR \times C_o}$$

6.2 Under-Voltage Lockout and Power On Ready

The under-voltage lockout circuit monitors the voltage of Vcc/LDO_Out pin and the Enable input. It assures that the MOSFET driver outputs remain in the off state whenever either of these two signals drop below the set thresholds. Normal operation resumes once Vcc/LDO_Out and Enable rise above their thresholds.

The POR (Power On Ready) signal is generated when all these signals reach the valid logic level (see system block diagram). The soft start sequence starts when the POR is asserted.

6.3 Enable

The Enable features another level of flexibility for startup. The Enable has precise threshold, which is internally monitored by Under-Voltage Lockout (UVLO) circuit. Therefore, the IR3825 will turn on only when the voltage at the Enable pin exceeds this threshold, typically, 1.2V.

If the input to the Enable pin is derived from the bus voltage by a suitably programmed resistive divider, it can be ensured that the IR3825 does not turn on until the bus voltage reaches the desired level (**Figure 6-2**). Only after the bus voltage reaches or exceeds this level and voltage at the Enable pin exceeds its threshold, IR3825 will be enabled. Therefore, in addition to being a logic input pin to enable the IR3825, the Enable feature, with its precise threshold, also allows the user to implement an Under-Voltage Lockout for the bus voltage (PVin). This is desirable particularly for high output voltage applications, where we might want the IR3825 to be disabled until PVin exceeds the desired output voltage level.

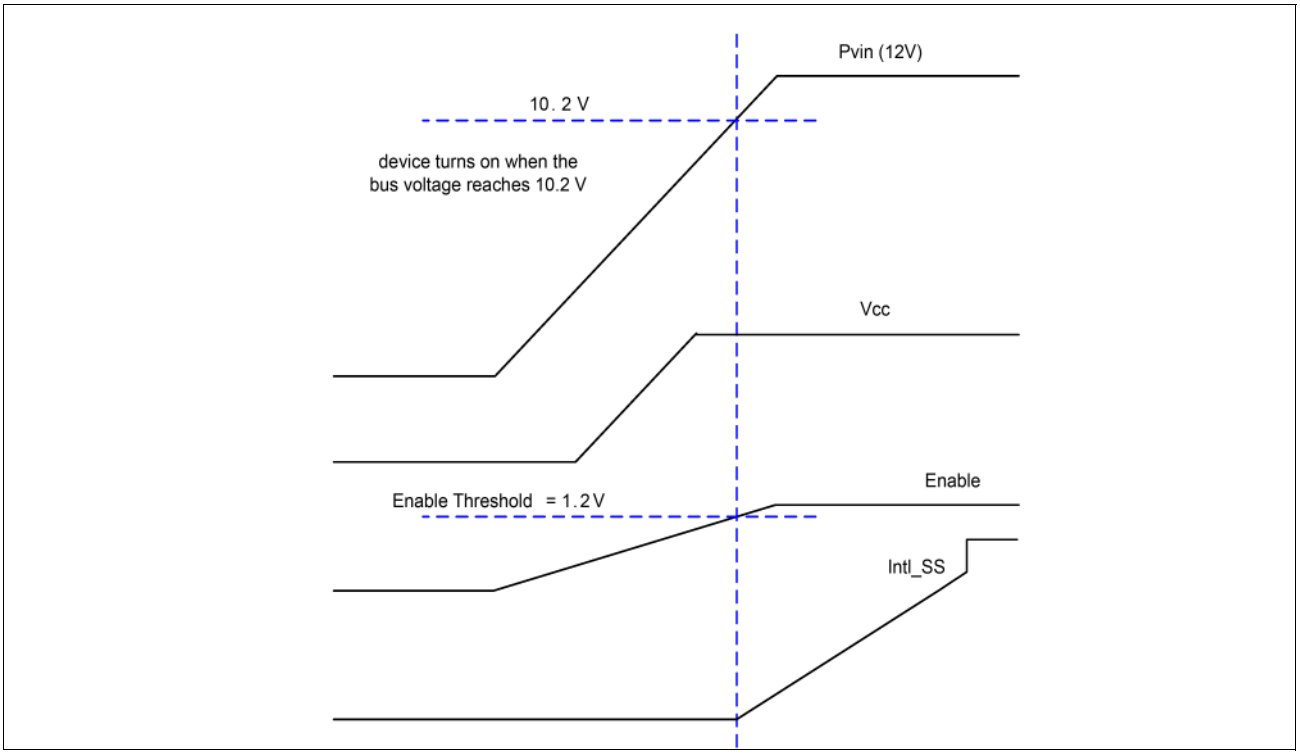


Figure 6-2 Normal start-up with Enable connected to PVin through a resistor divider at 10.2V

When Enable is used as a logic input, the recommended start-up sequence for the normal operation of IR3825 is shown in **Figure 6-3**.

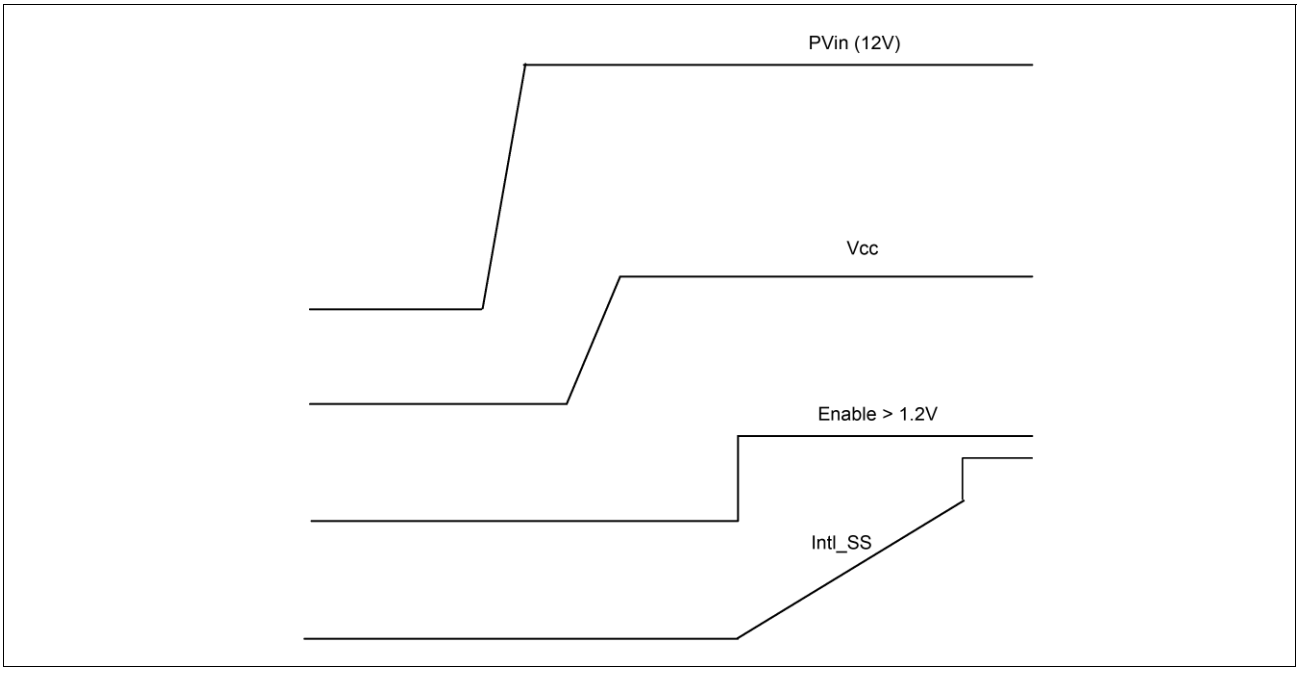


Figure 6-3 Normal start-up with a logic input for Enable signal

It is recommended to add a 1kΩ resistor in series with the Enable pin to limit the current flowing into the Enable pin. In addition, the Enable pin should not be left floating. A pull-down resistor in the range of several kilo ohms is recommended to connect between the Enable Pin and Gnd.

6.4 Pre-bias Startup

IR3825 is able to start up into pre-charged output, without oscillations and disturbances of the output voltage. The output starts in asynchronous fashion and keeps the synchronous MOSFET (Sync FET) off until the first gate signal for control MOSFET (Ctrl FET) is generated. **Figure 6-4** shows a typical pre-bias condition at startup.

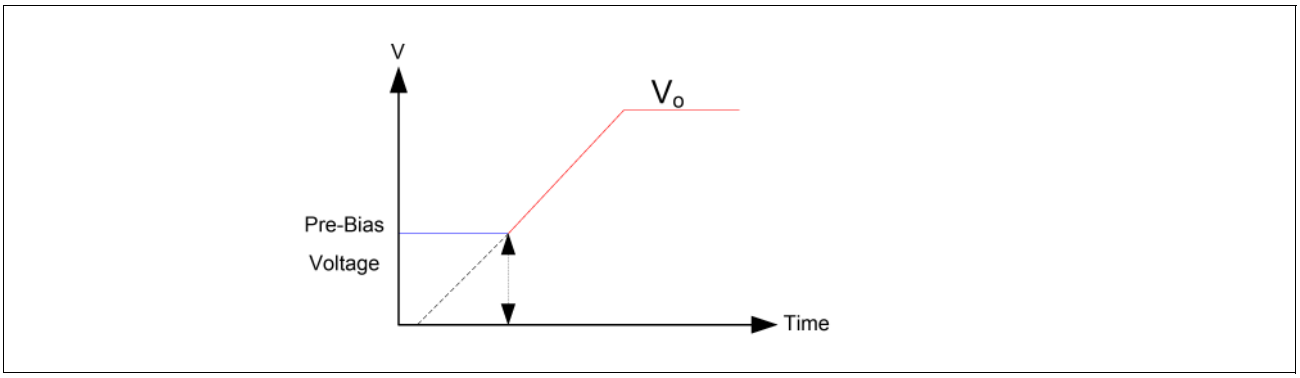


Figure 6-4 Pre-Bias Startup

The sync FET always starts with a narrow pulse width (12.5% of a switching period) and gradually increases its duty cycle with a step of 12.5% until it reaches the steady state value. The number of these startup pulses for each step is 16 and it's internally programmed. **Figure 6-5** shows the series of 16x8 startup pulses.

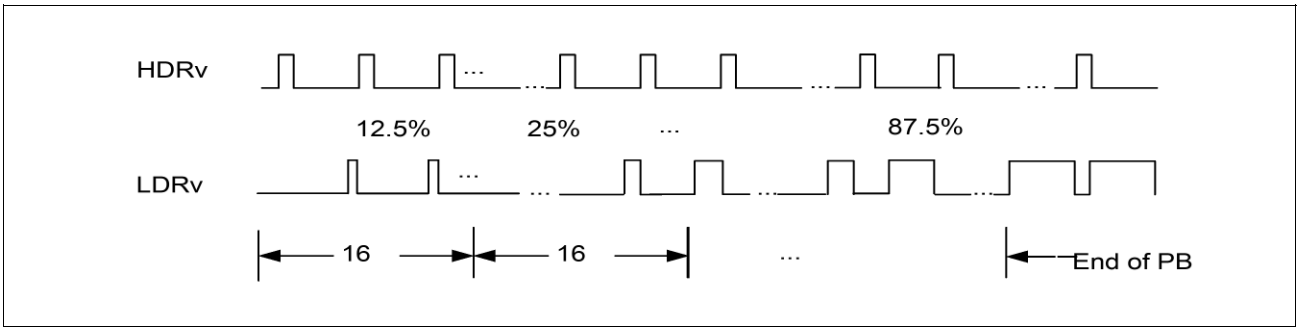


Figure 6-5 Pre-bias Startup Pulses

6.5 Soft Start

IR3825 has an internal digital soft-start to control the output voltage rise and to limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Enable and Vcc rise above their UVLO thresholds and generate the Power On Ready (POR) signal. The internal soft-start (Intl_SS) signal linearly rises with the rate of 0.2mV/µs from 0V to 1.5V. **Figure 6-6** shows the waveforms during the soft-start. The normal Vout start-up time is fixed, and is equal to:

$$T_{start} = \frac{0.75\text{V} - 0.15\text{V}}{0.2\text{mV/us}} = 3.0\text{ms}$$

During the soft-start, the over-current protection (OCP) and over-voltage protection (OVP) are enabled to protect the device for any short circuit or over voltage condition.

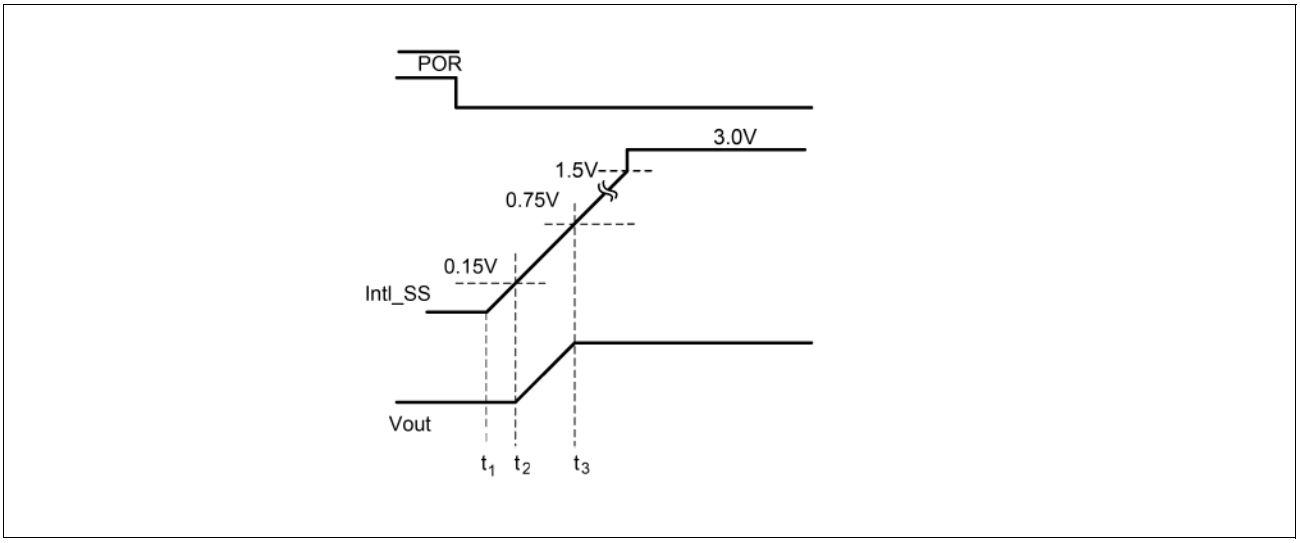


Figure 6-6 Theoretical Waveforms during Soft-Start

6.6 Operating Frequency

The switching frequency can be programmed between 300 kHz – 1.5 MHz by connecting an external resistor from R_t pin to Gnd. Table 2 lists the R_t with each corresponding switching frequency.

Table 6-2 Switching Frequency (F_s) vs. External Resistor (R_t)

R_t (KΩ)	F_S (kHz)
80.6	300
60.4	400
48.7	500
39.2	600
34.0	700
29.4	800
26.1	900
23.2	1000
21.0	1100
19.1	1200
17.4	1300
16.2	1400
15.0	1500

6.7 Shutdown

IR3825 can be shut down by pulling the Enable pin below its 1.0V threshold. This will put both the high side and the low side driver in a tri-state.

6.8 Over Current Protection

The over current (OC) protection is performed by sensing current through the $R_{DS(on)}$ of the Synchronous MOSFET. This method enhances the converter's efficiency, reduces cost by eliminating a current sense resistor and any layout related noise issues. The over current (OC) limit can be set to one of three possible settings by

floating the ILIM pin, by pulling up the ILIM pin to VCC, or pulling down the ILIM pin to PGnd. The current limit is internally compensated according to the IC temperature. So at different ambient temperature, the over-current trip threshold remains almost constant.

Note that the over current limit is affected by the Vcc voltage. In general, a lower Vcc voltage increases the $R_{DS(on)}$ of the Synchronous MOSFET and hence results in a lower OCP limit. Please refer to the typical performance curves of the OCP current limit with different Vcc voltages.

To prevent false tripping induced by noise and transients, the current near the valley of the inductor current is sensed by the Over Current Protection circuit. More precisely, the inductor current is sampled for about 40ns on the downward inductor current slope approximately 12.5% of the switching period before the inductor current valley. When the current exceeds the OCP limit, an over current condition is detected.

When an Over Current event is detected, PGood signal is pulled low and the device enters hiccup mode. Hiccup mode is performed by latching an internal OC signal, which keeps both Control FET and Synchronous FET off for 20.48ms (typical) blanking time. OC signal clears after the completion of blanking time and the device attempts to recover to the nominal output voltage with a soft-start, as shown in **Figure 6-7**. The device will repeat hiccup mode and attempt to recover until the overload or short circuit conditions is removed.

Since the current sensing point is near the valley of the inductor current, the actual DC output current limit point will be greater than the valley point by approximately one half of peak to peak inductor ripple current. The DC current limit point can be calculated by the following equation. It should be pointed out that the OCP limits specified in the Electrical Table refer to the over current limit valley point.

$$I_{OCP} = I_{LIMIT} + \frac{\Delta I}{2}$$

I_{OCP} = DC current limit hiccup point

I_{LIMIT} = Over Current limit (valley of inductor current)

ΔI = Inductor ripple current

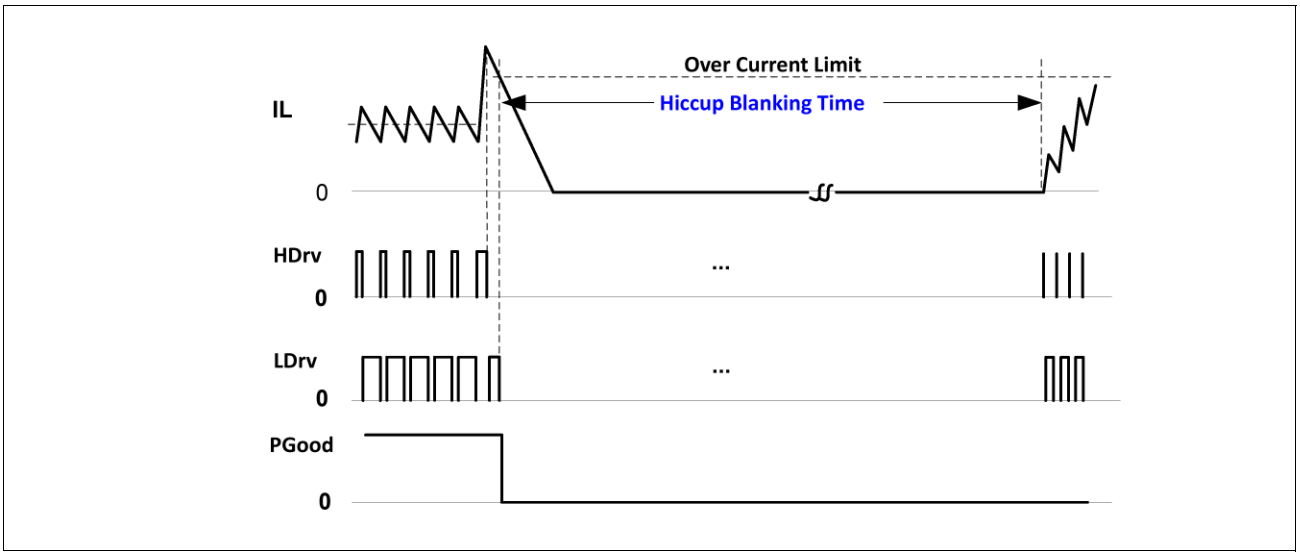


Figure 6-7 Timing Diagram for Current Limit Hiccup

6.9 Thermal Shutdown

Temperature sensing is provided inside IR3825. The trip threshold is typically set to 145°C. When trip threshold is exceeded, thermal shutdown turns off both MOSFETs and resets the internal soft start.

Automatic restart is initiated when the sensed temperature drops within the operating range. There is a 20°C hysteresis in the thermal shutdown threshold.

6.10 Feed-Forward

Feed-Forward is an important feature, because it can keep the converter stable and preserve its load transient performance when Vin varies in a large range. In IR3825, Feed-Forward function is enabled when Vin pin is connected to PVin pin. In this case, the internal low dropout (LDO) regulator is used. The PWM ramp amplitude (Vramp) is proportionally changed with Vin to maintain Vin/Vramp almost constant throughout Vin variation range as shown in the timing diagram. Thus, the control loop bandwidth and phase margin can be maintained constant. Feed-forward function can also minimize impact on output voltage from fast Vin change. The maximum Vin slew rate is within 1V/µs.

If an external bias voltage is used as Vcc, Vin pin should be connected to Vcc/LDO_out pin instead of PVin pin. Then the Feed-Forward function is disabled. A re-calculation of loop compensation parameters is needed.

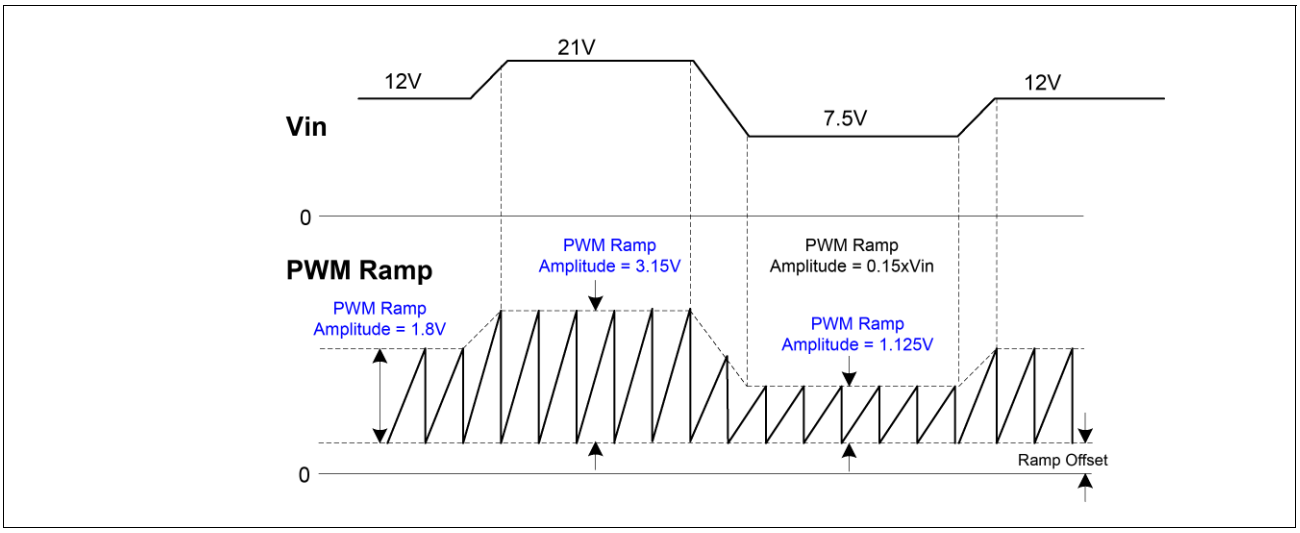


Figure 6-8 Timing diagram for Feed-Forward function

6.11 Low Dropout Regulator (LDO)

IR3825 has an integrated low dropout (LDO) regulator which can provide gate drive voltage for both drivers.

For internally biased single rail operation, Vin pin should be connected to PVin pin. If external bias voltage is used, Vin pin should be connected to Vcc/LDO_Out pin as shown in the figure.

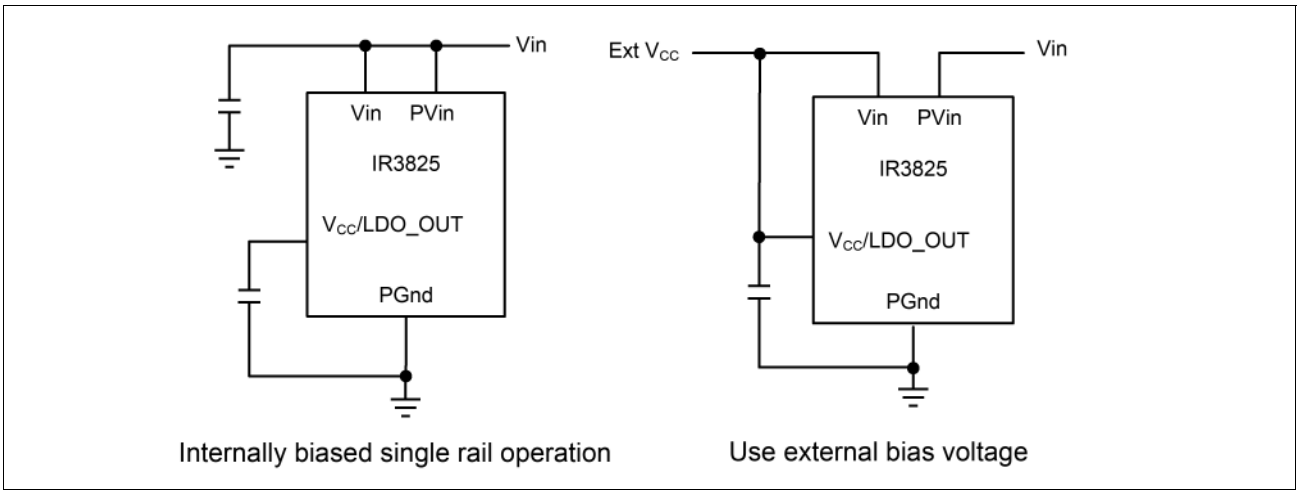


Figure 6-9 Internal LDO or External V_{CC} Configurations

When the Vin voltage is below 7.5V, the internal LDO may enter the dropout mode. The dropout voltage increases with the switching frequency. The figure shows the LDO voltage for 600kHz and 1000kHz respectively.

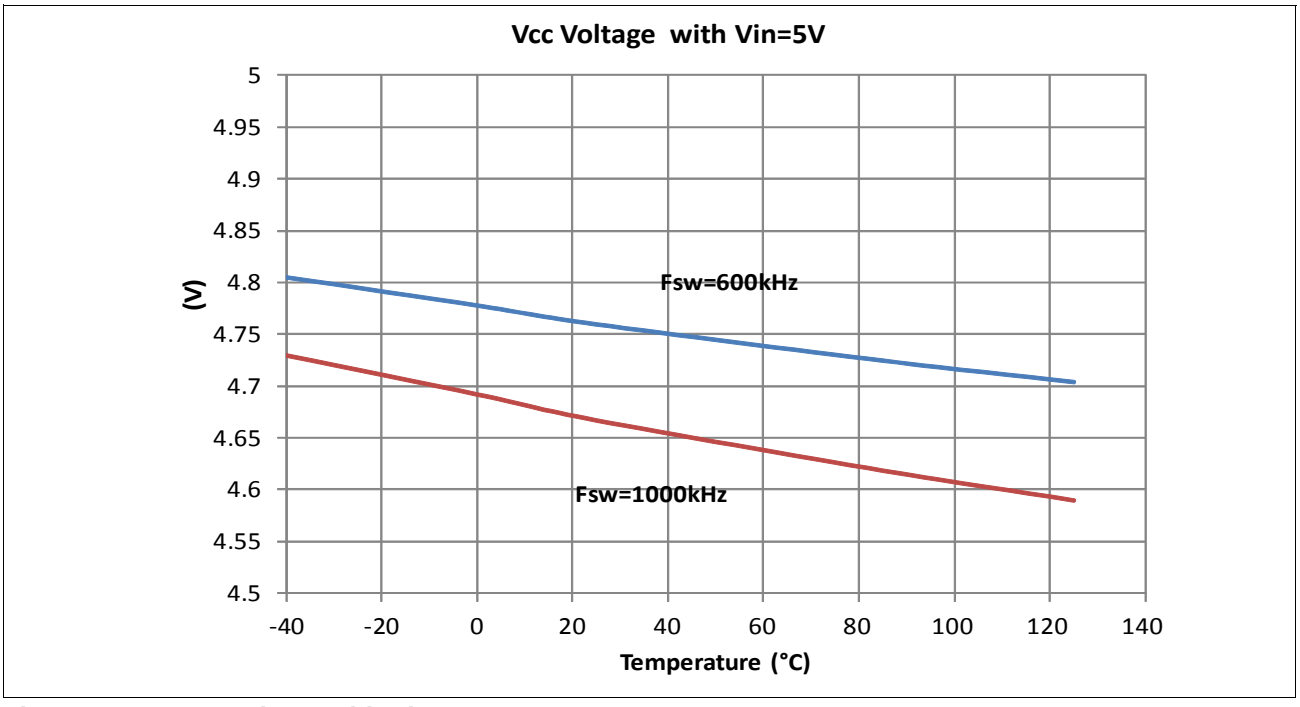


Figure 6-10 LDO Voltage with Vin = 5V

6.12 Power Good Output

IR3825 continually monitors the output voltage via the sense pin (Vsns) voltage. The Vsns voltage is an input to the window comparator with upper and lower turn-off threshold of 120% and 85% of the reference voltage respectively. PGood signal is high whenever Vsns voltage is within the PGood comparator window thresholds. The PGood is an open drain output. Hence, a pull-up resistor is needed to limit the current flowing into the PGood pin

less than 5mA when the output voltage is not in regulation. A typical value used is 49.9kΩ. High state indicates that output is in regulation. **Figure 6-11** shows the timing diagram of the PGood signal. Vsns signal is also used by OVP comparator for detecting output over voltage condition.

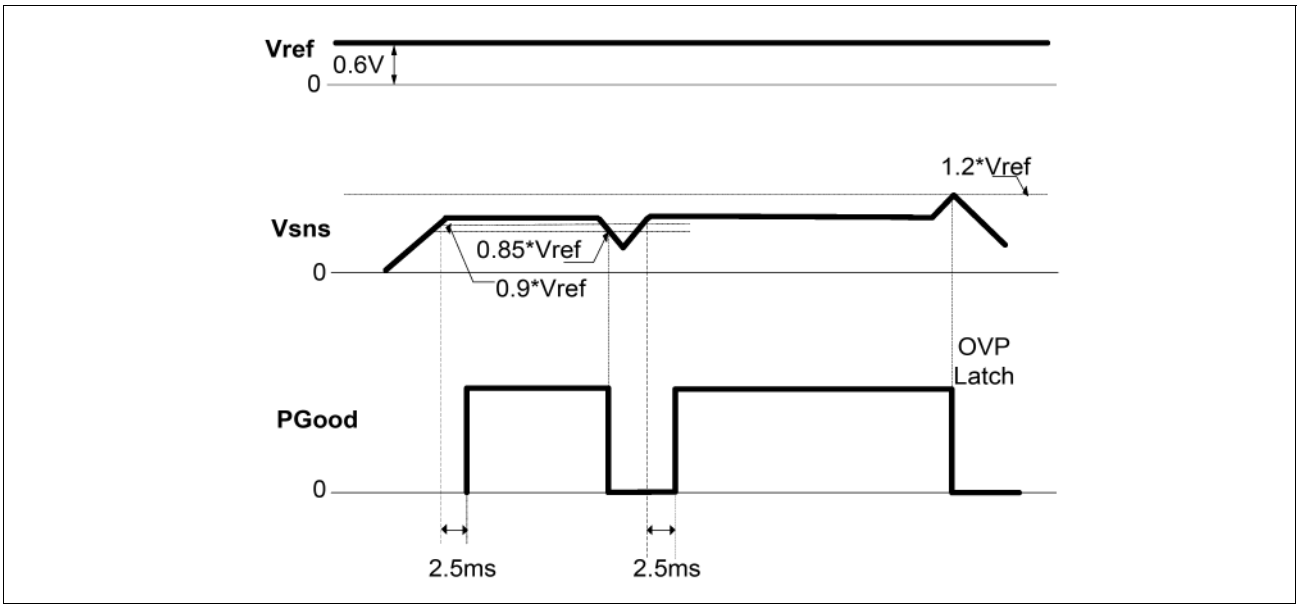


Figure 6-11 Vsns vs. PGood Relationship Timing Diagram

6.13 Over-Voltage Protection (OVP)

OVP is achieved by comparing Vsns voltage to an OVP threshold voltage, 1.2 x Vref. When Vsns exceeds the OVP threshold, an over voltage trip signal asserts after 2us typical delay. Then the control FET is latched off immediately, PGood flags low. The sync FET remains on to discharge the output capacitor. When the Vsns voltage drops below the threshold, the sync FET turns off to prevent the complete depletion of the output capacitor. The control FET remains latched off until either Vcc or Enable signal is re-cycled.

OVP comparator becomes active when the enable signal exceeds the start threshold. Vsns voltage is set by the voltage divider connected to the output and it can be programmed externally.

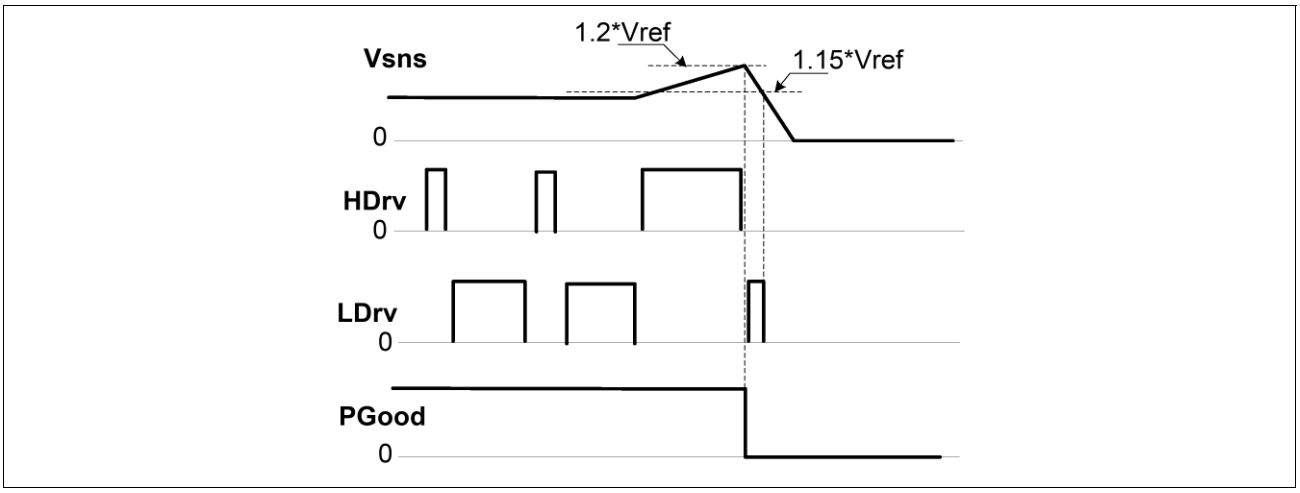


Figure 6-12 OVP Timing Diagram

6.14 Minimum On Time Considerations

The minimum ON time is the shortest amount of time for Control FET to be reliably turned on. This is a very critical parameter for low duty cycle, high frequency applications. Conventional approach limits the pulse width to prevent noise, jitter and pulse skipping. This results in lower closed loop bandwidth.

Infineon has developed a proprietary scheme to improve and enhance minimum pulse width that utilizes the benefits of voltage mode control scheme with higher switching frequency, wider conversion ratio and higher closed loop bandwidth, the latter results in reduction of output capacitors. Any design or application using IR3825 must ensure operation with a pulse width that is higher than this minimum on-time. This is necessary for the circuit to operate without jitter and pulse-skipping, which can cause high inductor current ripple and high output voltage ripple.

$$t_{on} = \frac{D}{F_s} = \frac{V_{out}}{V_{in} \times F_s}$$

In any application that uses IR3825, the following conditions must be satisfied:

$$t_{on(\min)} \le t_{on}$$

$$t_{on(\min)} \le \frac{V_{out}}{V_{in} \times F_s}$$

$$V_{in} \times F_s \le \frac{V_{out}}{t_{on(\min)}}$$

The minimum output voltage is limited by the reference voltage and hence Vout(min) = 0.6 V. Therefore, for Vout(min) = 0.6 V,

$$V_{in} \times F_s \le \frac{V_{out}}{t_{on(\min)}} = \frac{0.6V}{60\,ns} = 10\,\mathrm{V}/\mu\mathrm{s}$$

Therefore, at the maximum recommended input voltage of 21V and minimum output voltage, the converter should be designed at a switching frequency that does not exceed 476 kHz. Conversely, for operation at the maximum recommended operating frequency (1.5MHz) and minimum output voltage (0.6V), the input voltage (PVin) should not exceed 6.6V. Else pulse skipping will happen.

6.15 Maximum Duty Ratio

IR3825 is designed to have a maximum duty ratio of 0.86 for most applications. In addition, there are two other factors to limit the maximum duty ratio. One is the minimum off-time, which is more dominant at high switching frequency. The other factor is the maximum output voltage of the error amplifier. Due to the built-in input voltage feedforward, the ramp voltage of the internal PWM modulator increases with Vin. However the output of the error amplifier is clamped at the maximum voltage as specified in the electrical table, which can result in a max duty ratio smaller than 0.86 at high Vin. The figure shows a plot of the maximum duty ratio vs. the switching frequency with built in input voltage feedforward.

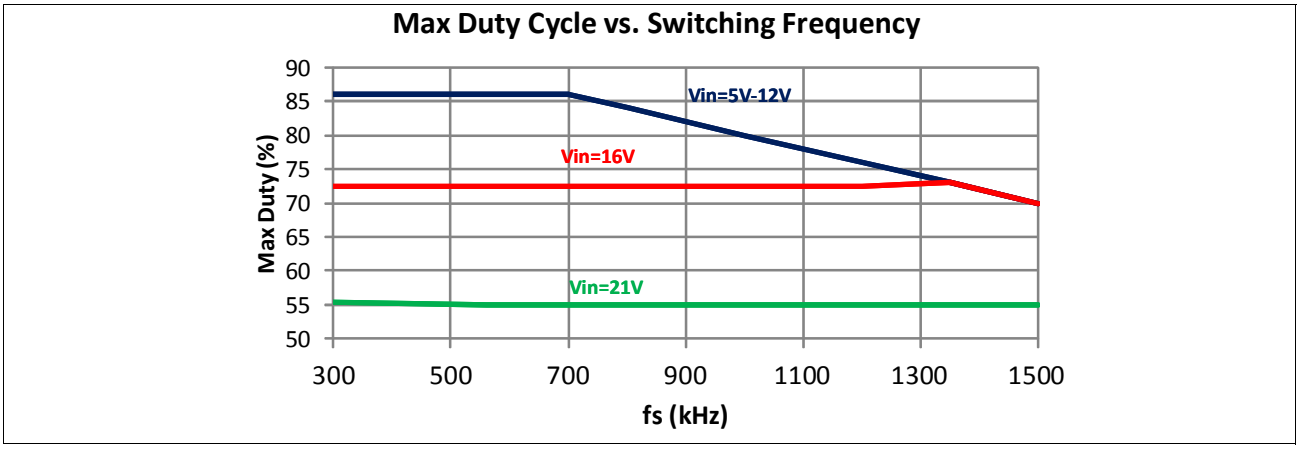


Figure 6-13 Maximum Duty Cycle vs. Switching Frequency with Vin Feedforward

7 Applications Design Example

The following key parameters shall be used as an example for typical IR3825 applications. The application circuit is shown in **Section 7.9**.

- $PV_{in} = V_{in}$ = 12V (±10%)
- V_O = 1.0V
- I_O = 20A
- Peak-to-Peak Ripple Voltage = 1% of V_O
- ΔVo = ± 4% of V_O (for 30% Load Transient)
- F_S = 600kHz

7.1 Enabling The IR3825

As explained earlier, the precise threshold of the Enable lends itself well to implementation of a UVLO for the Bus Voltage shown by the resistor divider network.

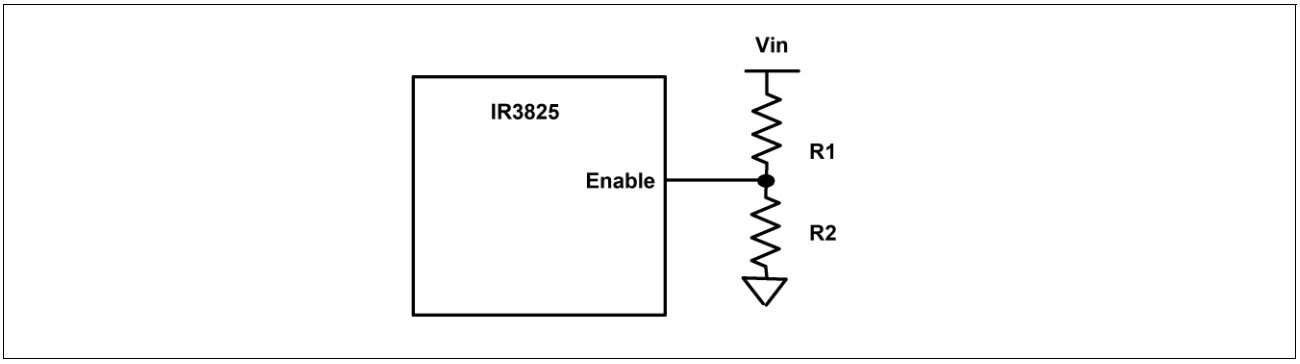


Figure 7-1 Using Enable pin for UVLO implementation for a typical Enable threshold of V_{EN} = 1.2 V

$$V_{in(\min)} \times \frac{R_2}{R_1 + R_2} = V_{EN} = 1.2\text{V}$$

$$R_2 = R_1 \times \frac{V_{EN}}{V_{in(\min)} - V_{EN}}$$

For V_{in} (min)= 9.2V, R1= 49.9kΩ and R2 = 7.5kΩ is a good choice.

7.2 Programming the Frequency

For F_S = 600kHz, select R_t = 39.2kΩ, using **Table 6-2**.

7.3 Output Voltage Programming

Output voltage is programmed by reference voltage and external voltage divider. The Fb pin is the inverting input of the error amplifier, which is internally referenced to 0.6V. The divider ratio is set to provide 0.6V at the Fb pin when the output is at its desired value. The output voltage and the external resistor dividers connected to the output are defined by using the equations:

$$V_o = V_{ref} \times (1 + \frac{R_{F1}}{R_{F2}})$$

$$R_{F2} = R_{F1} \times \left(\frac{V_{ref}}{V_o - V_{ref}} \right)$$

For the calculated values of R_{F1} and R_{F2}, see feedback compensation section.

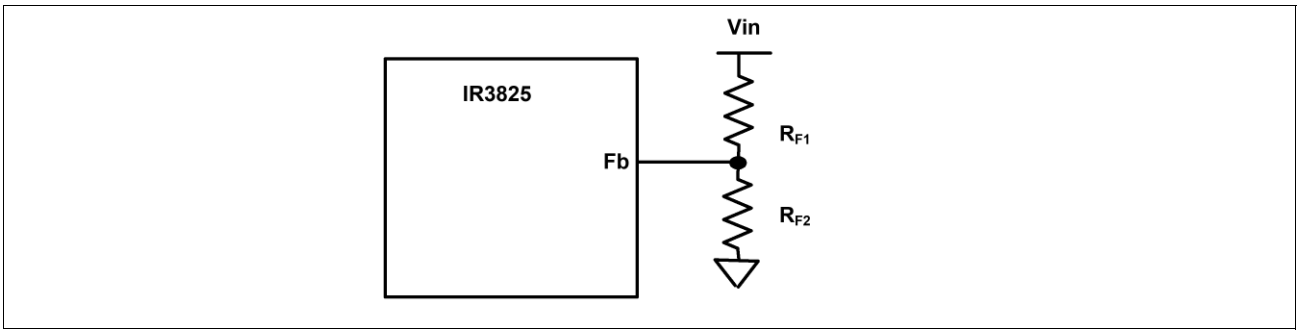


Figure 7-2 Output Voltage Programming for Typical Applications of IR3825

7.4 Bootstrap Capacitor Selection

To drive the Control FET, it is necessary to supply a gate voltage at least 4V greater than the voltage at the SW pin, which is connected to the source of the Control FET. This is achieved by using a bootstrap configuration, which comprises the internal bootstrap diode and an external bootstrap capacitor (C1).

When the sync FET is turned on, the capacitor node connected to SW is pulled down to ground. The capacitor charges towards Vcc through the internal bootstrap diode, which has a forward voltage drop V_D. The voltage Vc across the bootstrap capacitor C1 is approximately given as:

$$V_C = V_{CC} - V_D$$

When the control FET turns on in the next cycle, the capacitor node connected to SW rises to the bus voltage Vin. However, if the value of C1 is appropriately chosen, the voltage Vc across C1 remains approximately unchanged and the voltage at the Boot pin becomes:

$$V_{BOOT} = V_{in} + V_{CC} - V_D$$

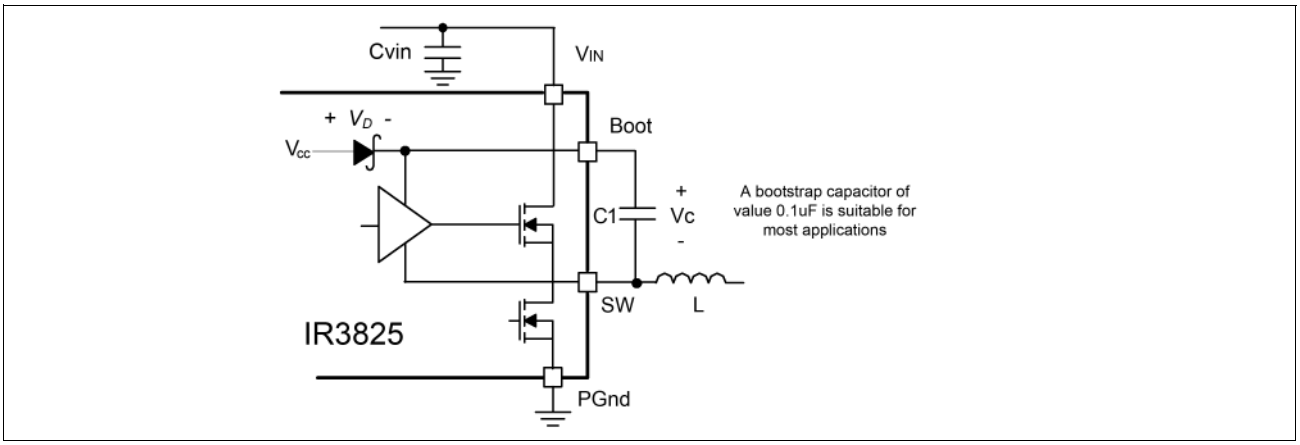


Figure 7-3 Bootstrap Circuit to Generate Vc Voltage.

7.5 Input Capacitor Selection

The ripple current generated during the on time of the control FET should be provided by the input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_o \times \sqrt{D \times (1-D)}$$

$$D = \frac{V_o}{V_{in}}$$

Where:

D is the Duty Cycle

I_{RMS} is the RMS value of the input capacitor current. Io is the output current.

For I_O = 20A and D = 0.0833, the I_{RMS} = 5.52A.

Ceramic capacitors are recommended due to their peak current capabilities. They also feature low ESR and ESL at higher frequency which enables better efficiency. For this application, it is advisable to have 5x10µF, 25V ceramic capacitors, C3216X5R1E106M from TDK. In addition to these, although not mandatory, a 1x330µF, 25V SMD capacitor EEV-FK1E331P from Panasonic may also be used as a bulk capacitor and is recommended if the input power supply is not located close to the converter.

7.6 Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value causes large ripple current, resulting in the smaller size, faster response to a load transient but poor efficiency and high output noise. Generally, the selection of the inductor value can be reduced to the desired maximum ripple current in the inductor (ΔiL). The optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for the desired operating ripple current can be determined using the following relations:

$$V_{in\max} - V_o = L \times \frac{\Delta i_L}{\Delta t} \qquad \Delta t = \frac{D}{F_s}$$

$$L = (V_{in\max} - V_o) \times \frac{V_o}{V_{in\max} \times \Delta i_L \times F_s}$$

Where:

V_{inmax} = Maximum input voltage

V_O = Output Voltage

Δi_L = Inductor Peak-to-Peak Ripple Current

F_S= Switching Frequency

Δt = On time for Control FET

D = Duty Cycle

If $\Delta i_L \approx 25\%*Io$, then the output inductor is calculated to be 0.31µH. Select L=0.30µH, FP1107R1-R30-R, from Coiltronics which provides an inductor suitable for this application.

7.7 Output Capacitor Selection

The voltage ripple and transient requirements determine the output capacitors type and values. The criterion is normally based on the value of the Effective Series Resistance (ESR). However the actual capacitance value and

the Equivalent Series Inductance (ESL) are other contributing components. These components can be described as:

$$\Delta V_o = \Delta V_{o(ESR)} + \Delta V_{o(ESL)} + \Delta V_{o(C)}$$

$$\Delta V_{o(ESR)} = \Delta I_L \times ESR$$

$$\Delta V_{o(ESL)} = (\frac{V_{in} - V_o}{L}) \times ESL$$

$$\Delta V_{o(C)} = \frac{\Delta I_L}{8 \times C_o \times F_s}$$

Where:

ΔV_O = Output Voltage Ripple

ΔI_L = Inductor Ripple Current

Since the output capacitor has a major role in the overall performance of the converter and determines the result of transient response, selection of the capacitor is critical. The IR3825 can perform well with all types of capacitors.

As a rule, the capacitor must have low enough ESR to meet output ripple and load transient requirements.

The goal for this design is to meet the voltage ripple requirement in the smallest possible capacitor size. Therefore it is advisable to select ceramic capacitors due to their low ESR and ESL and small size. In this case a good choice is eight 47µF ceramic capacitors, C2012X5R0J476M from TDK. The ESR of this type of capacitor is around 3mΩ each. The de-rated capacitance value with 1.0VDC bias and 10mVAC voltage is around 29µF each.

It is also recommended to use a 0.1µF ceramic capacitor at the output for high frequency filtering.

7.8 Feedback Compensation

For this design, the resonant frequency of the output LC filter, F_{LC}, is:

$$F_{LC} = \frac{1}{2 \times \pi \sqrt{L_o \times C_o}}$$

$$= \frac{1}{2 \times \pi \sqrt{0.3 \times 10^{-6} \times 8 \times 29 \times 10^{-6}}}$$

$$= 19.1\text{kHz}$$

The equivalent ESR zero of the output capacitors, F_{ESR}, is:

$$F_{ESR} = \frac{1}{2\pi \times ESR \times C_o}$$

$$= \frac{1}{2\pi \times 3 \times 10^{-3} \times 29 \times 10^{-6}}$$

$$= 1.8\text{MHz}$$

Designing crossover frequency around 1/7th of switching frequency gives F_O =80 kHz.

According to **Table 6-1**, Type III B compensation is selected for $F_{LC} < F_O < F_{S/2} < F_{ESR}$. Type III compensator is shown in **Figure 7-4** for easy reference.

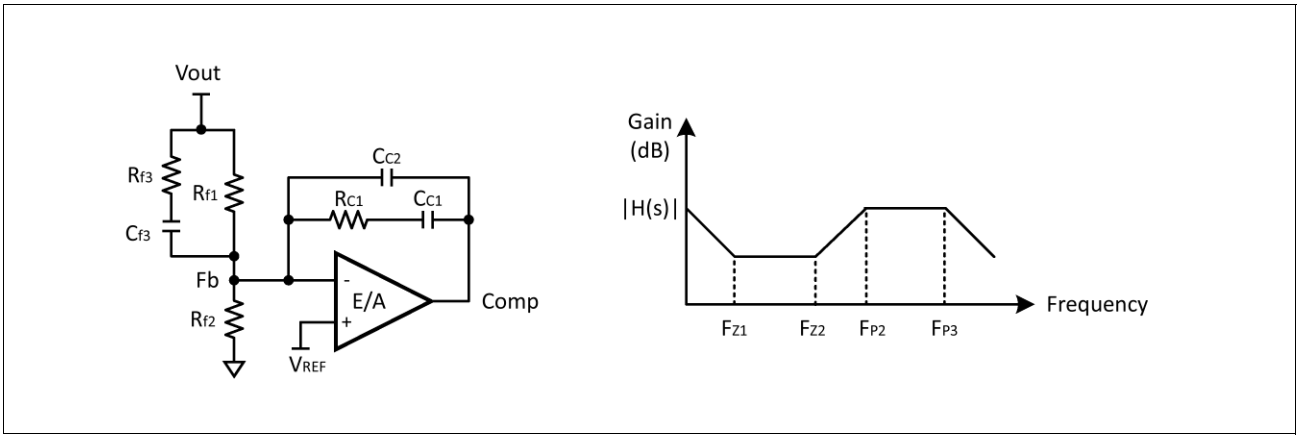


Figure 7-4 Type III compensation and its Asymptotic Gain Plot

As shown in **Figure 7-4**, Type III compensator contains two zeros and three poles.

The zeros are:

$$F_{Z1} = \frac{1}{2\pi \times R_{C1} \times C_{C1}}$$

$$F_{Z2} = \frac{1}{2\pi \times C_{F3} \times (R_{F3} + R_{F1})}$$

The poles are:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R_{F3} \times C_{F3}}$$

$$F_{P3} = \frac{1}{2\pi \times R_{C1} \times C_{C2}}$$

To archive the sufficient phase boost near the cross-over frequency, it is desired to place one zero and one pole as follows:

$$F_{Z2} = F_0 \sqrt{\frac{1-\sin\theta}{1+\sin\theta}} = 80 \times 10^3 \sqrt{\frac{1-\sin 70}{1+\sin 70}} = 14.1\text{kHz}$$

$$F_{P2} = F_0 \sqrt{\frac{1+\sin\theta}{1-\sin\theta}} = 80 \times 10^3 \sqrt{\frac{1+\sin 70}{1-\sin 70}} = 454.0\text{kHz}$$

To compensate the phase lag of the pole at the origin and to provide extra phase boost, the other zero could be placed at one half of the first zero, i.e. F_{Z1} = 7.05 kHz. The third pole is usually placed at one half of the switching frequency to damp the switching noise. i.e. F_{p3} = 300 kHz.

Please note that the zeros and poles locations do not necessarily follow the general design guides above and could vary with the design preference. The selected compensation parameters are: R_{F1}=4.02kΩ, R_{F2}=6.04kΩ, R_{F3}=100Ω, C_{F3}=3300pF, R_{C1}=1.5kΩ, C_{C1}=10nF, C_{C2}=220pF. Finally, select the Vsns resistors (R7 / R8 in **Section 7.9**) to the same ratio of R_{F1} / R_{F2} to ensure the proper OVP and Pgood operations.

7.9 Application Diagram and Bill of Materials

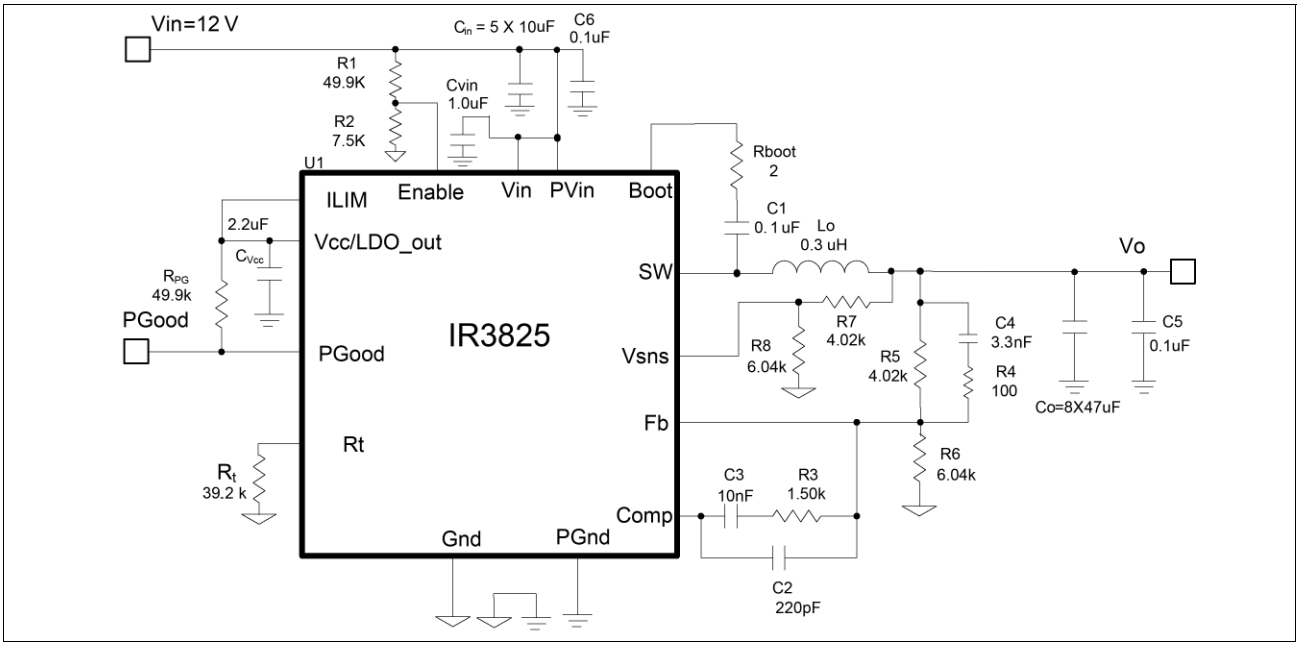


Figure 7-5 Application Circuit for a 12V to 1.0V, 20A Point of Load Converter

Table 7-1 Suggested Bill of Materials for the Application Circuit

Part Reference	Qty	Value	Description	Manufacturer	Part Number
Cin	1	330µF	SMD Electrolytic F size 25V 20%	Panasonic	EEV-FK1E331P
	5	10µF	1206, 25V, X5R, 20%	TDK	C3216X5R1E106M
C1 C5 C6	3	0.1µF	0402, 25V, X7R, 10%	Murata	GRM155R71E104KE14J
C4	1	3300pF	0402, 50V, X7R, 10%	Murata	GRM155R71H332KA01D
C2	1	220pF	0402, 50V, NP0, 5%	Murata	GRM1555C1H221JA01D
C_0	8	47µF	0805, 6.3V, X5R, 20%	TDK	C2012X5R0J476M
CV_{CC}	1	2.2µF	0603, 16V, X5R, 20%	TDK	C1608X5R1C225M
C3	1	10nF	0402, 25V, X7R, 10%	Murata	GRM155R71E103KA01D
C_{VIN}	1	1.0µF	0402, 25V, X5R, 10%	Murata	GRM155R61E105KA12D
L_0	1	0.3uH	SMD 11.0x7.2x7.5mm,0.29mΩ	Coiltronics	FP1107R1-R30-R
R3	1	1.5KΩ	Thick Film, 0402, 1/10W, 1%	Panasonic	ERJ-2RKF1501X
R5 R7	2	4.02KΩ	Thick Film, 0402, 1/10W, 1%	Panasonic	ERJ-2RKF4021X
R6 R8	2	6.04KΩ	Thick Film, 0402, 1/10W, 1%	Panasonic	ERJ-2RKF6041X
R4	1	100Ω	Thick Film, 0402, 1/10W, 1%	Panasonic	ERJ-2RKF1000X
R_t	1	39.2kΩ	Thick Film, 0402, 1/10W, 1%	Panasonic	ERJ-2RKF3922X
R_{boot}	1	2Ω	Thick Film, 0402, 1/16W, 1%	Vishay	CRCW04022R00FKED
R1 R_{pg}	2	49.9KΩ	Thick Film, 0402, 1/10W, 1%	Panasonic	ERJ-2RKF4992X
R2	1	7.5KΩ	Thick Film, 0402, 1/10W, 1%	Panasonic	ERJ-2RKF7501X
U1	1	IR3825	PQFN 5 mm x 6 mm	Infineon	IR3825MPBF

7.10 Typical Operating Waveforms

Vin=12.0V, Vout=1.0V, Iout=0-20A, room temperature, 200LFM Air Flow.

Figure 7-6 Startup at 20A Load (Ch_1:Vin, Ch_2:Vout, Ch_3: PGood, Ch_4:Enable)

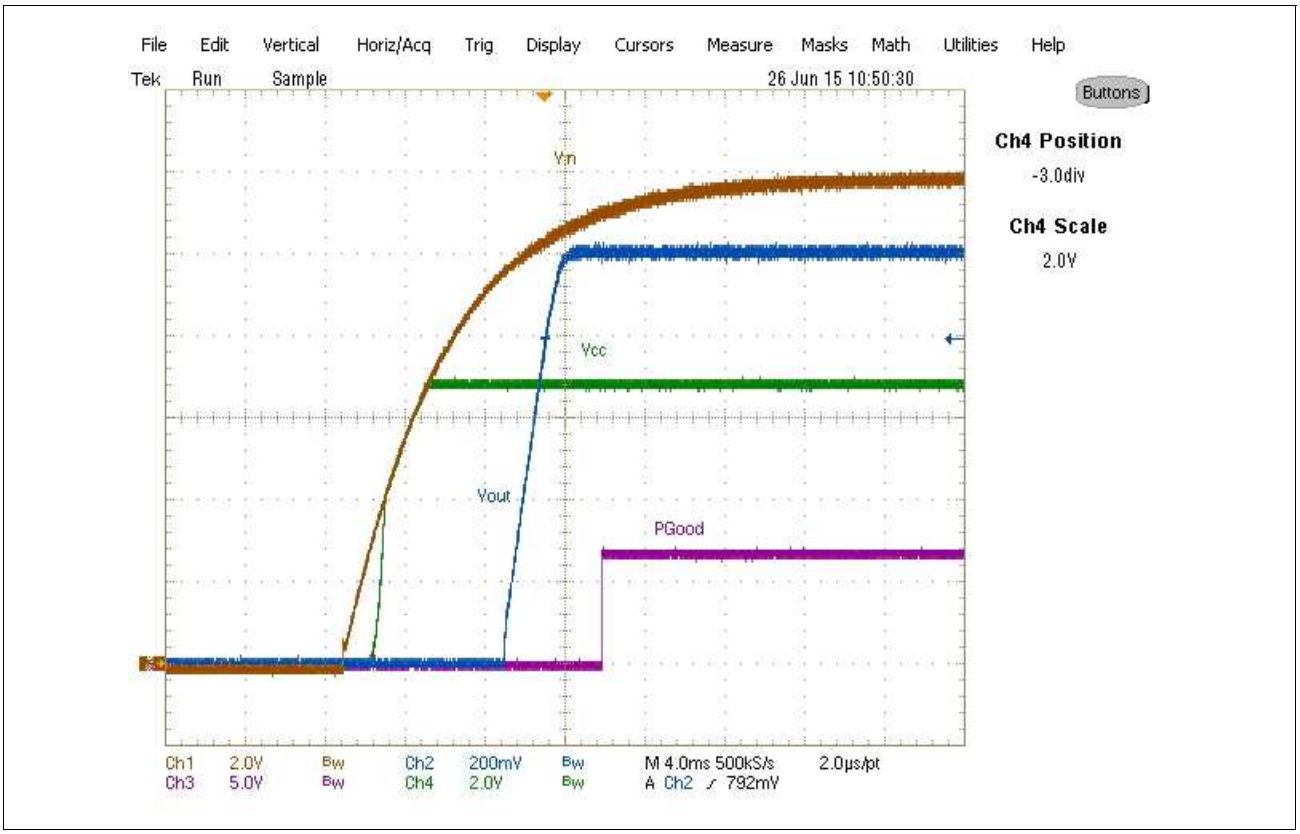


Figure 7-7 Startup at 20A Load (Ch_1:Vin, Ch_2:Vout, Ch_3: PGood, Ch_4:V_{CC})

Vin=12.0V, Vout=1.0V, Iout=0-20A, room temperature, 200LFM Air Flow.

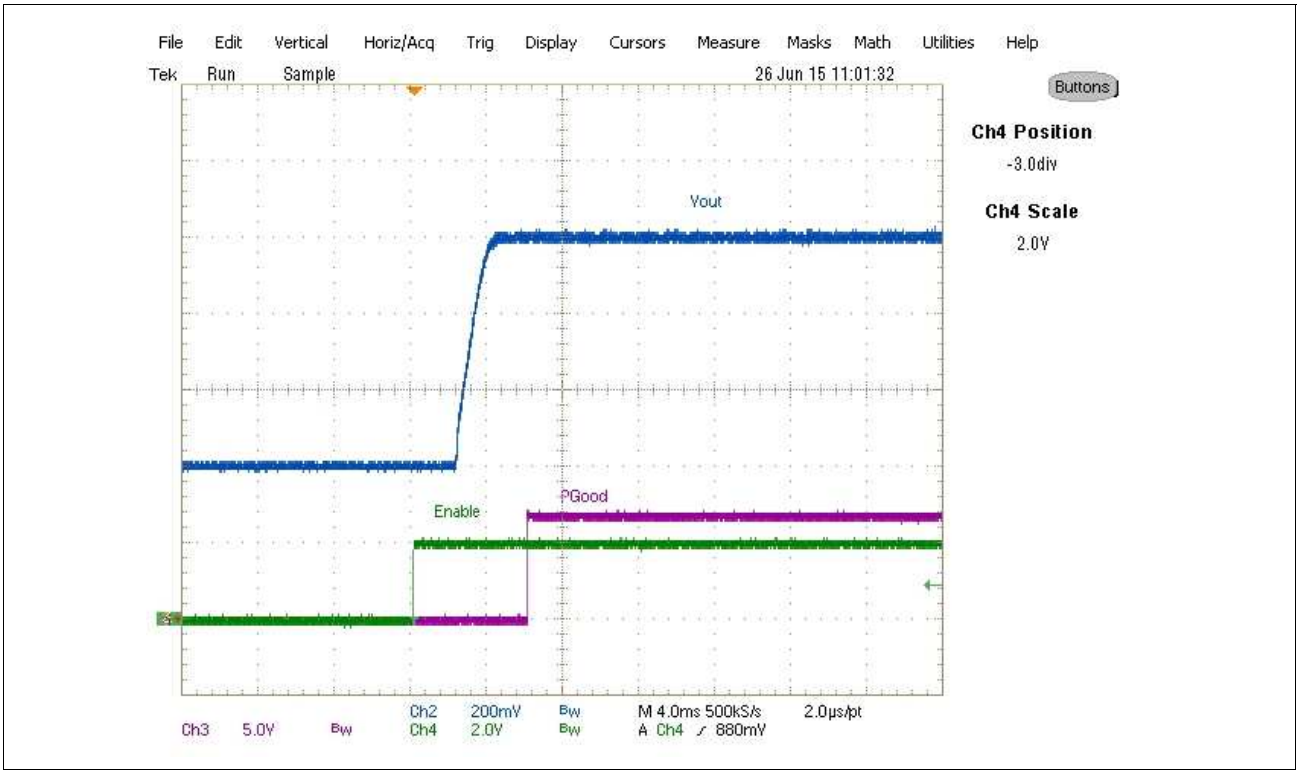


Figure 7-8 Start up with pre bias, 0A Load (Ch_2:Vout, Ch_3: PGood, Ch_4:Enable)

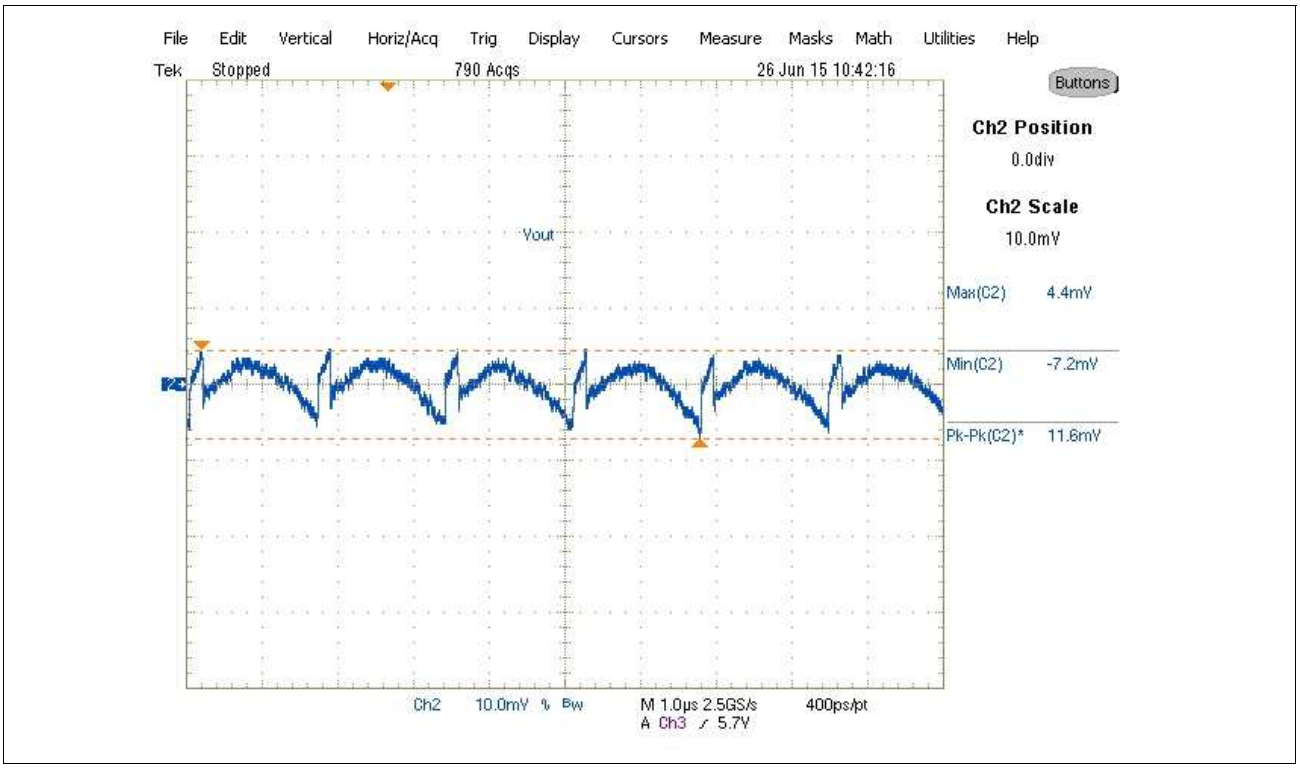


Figure 7-9 Output voltage ripple, 20A load (Ch_2:Vout)

Vin=12.0V, Vout=1.0V, Iout=0-20A, room temperature, 200LFM Air Flow.

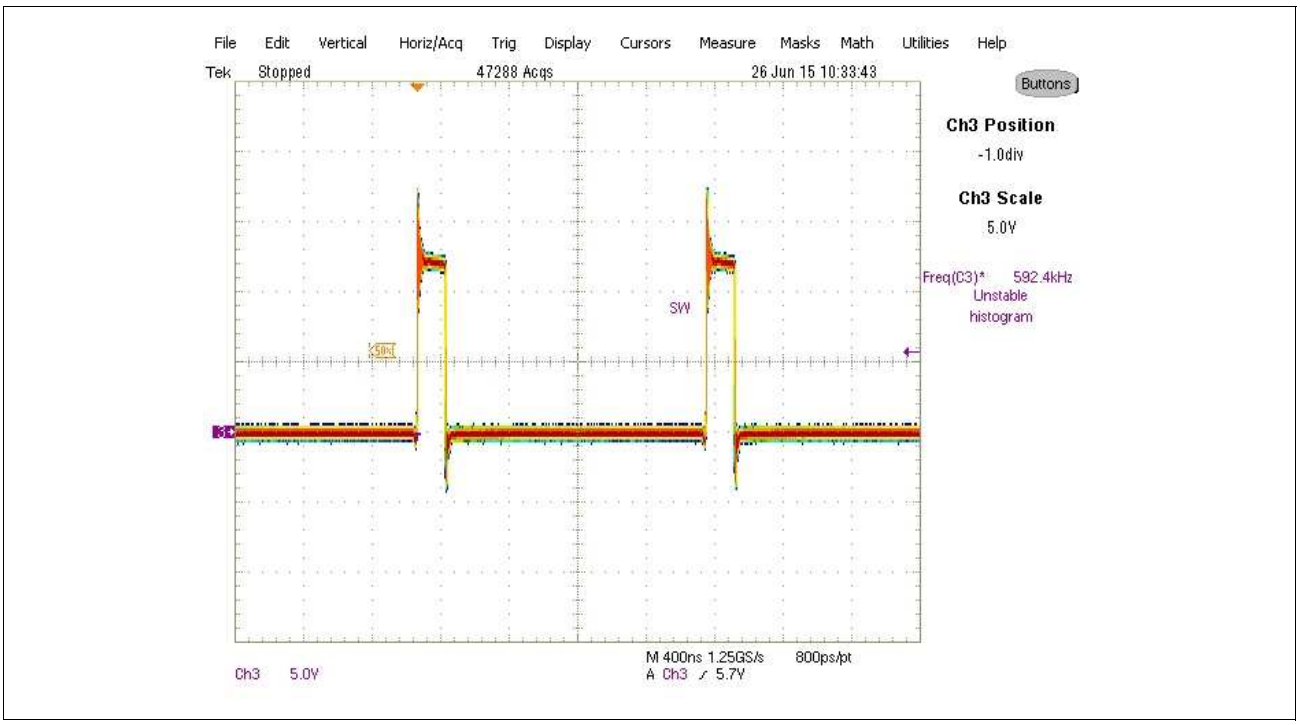


Figure 7-10 Inductor node at 20A load (Ch_3: Switch Node)

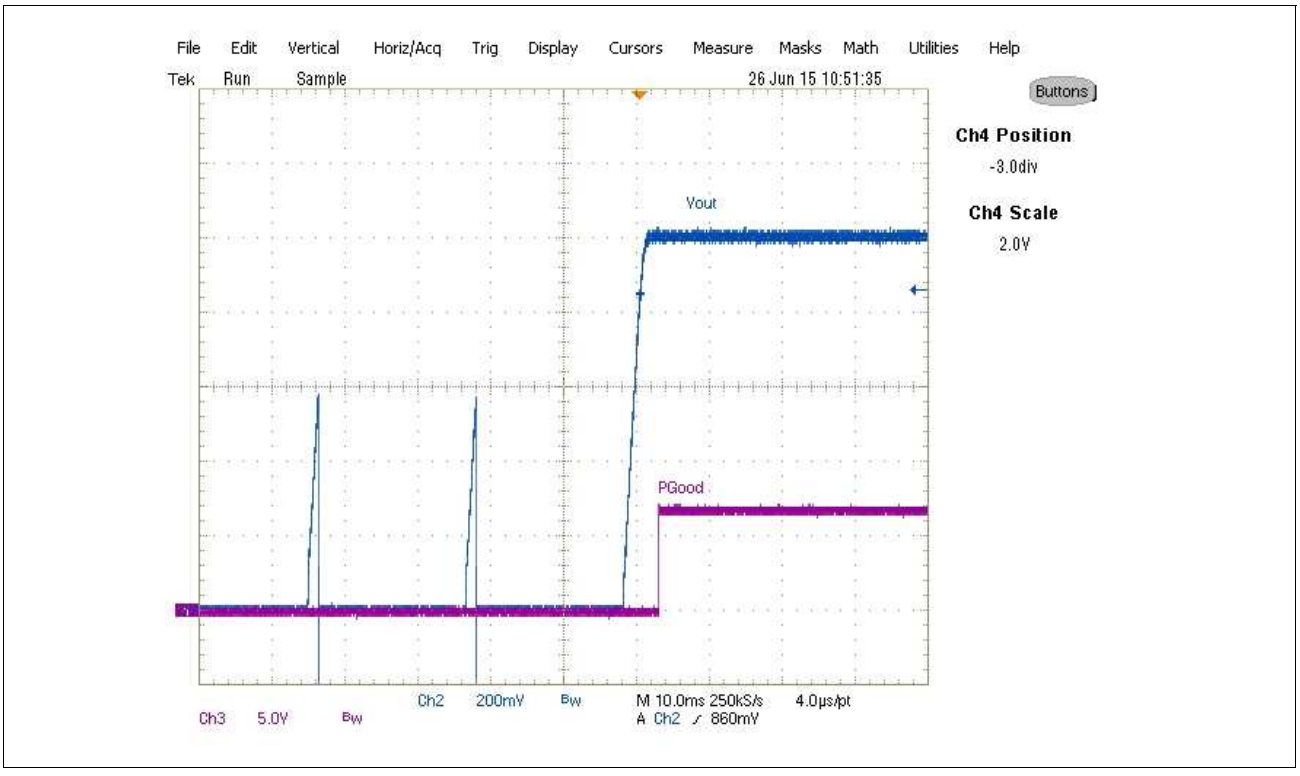
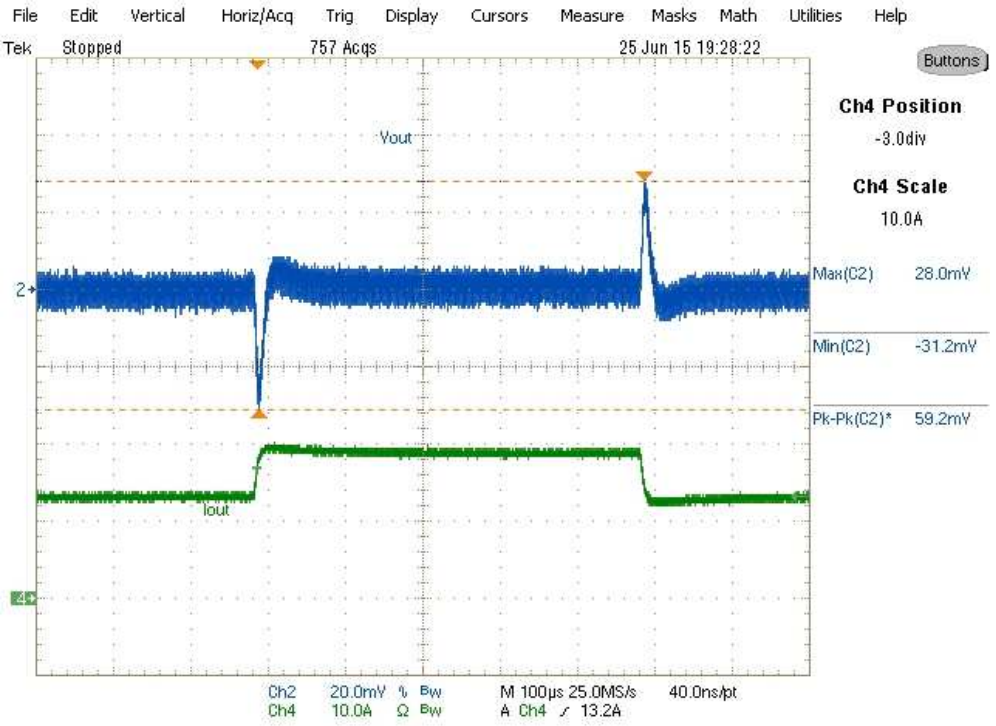


Figure 7-11 Short circuit (hiccup) recovery (Ch_2:Vout, Ch_3: PGood)

Vin=12.0V, Vout=1.0V, Iout=0-20A, room temperature, 200LFM Air Flow.

(a) I_{out} = 2A to 8A



(b) I_{out} = 14A to 20A

Figure 7-12 Transient response at 6A steps @2.5A/us slew rate. Ch_2:V_{out}, Ch_4:I_{out}

Vin=12.0V, Vout=1.0V, Iout=0-20A, room temperature, 200LFM Air Flow.

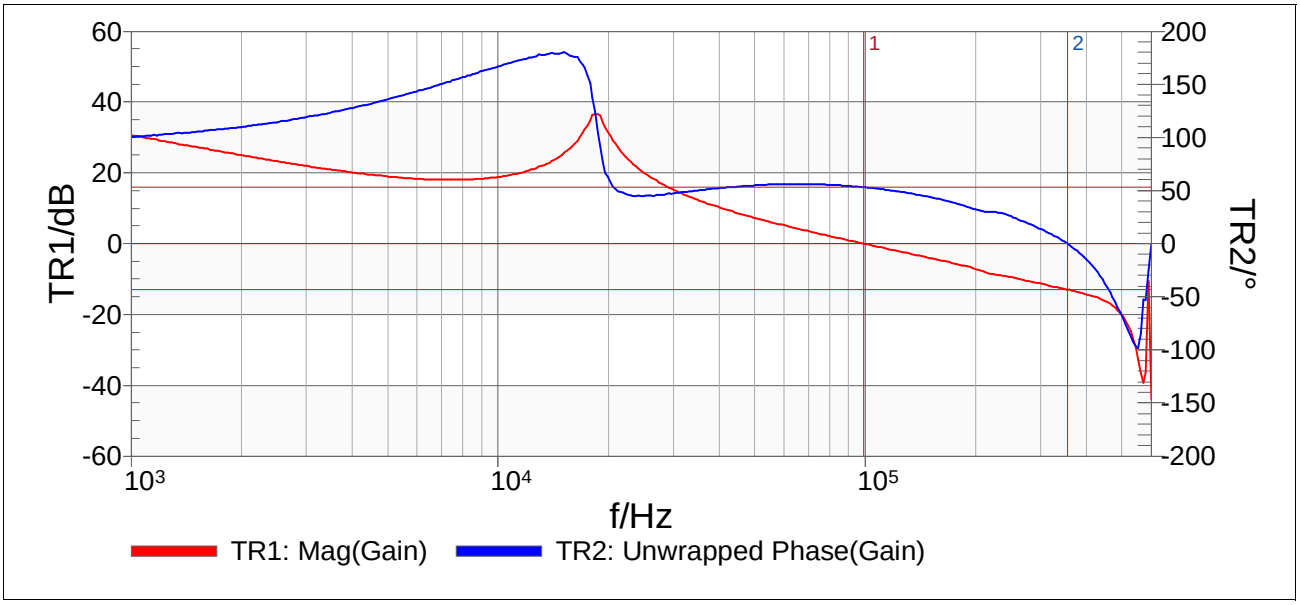


Figure 7-13 Bode plot at 20A load shows a bandwidth of 99.1kHz and phase margin of 53º

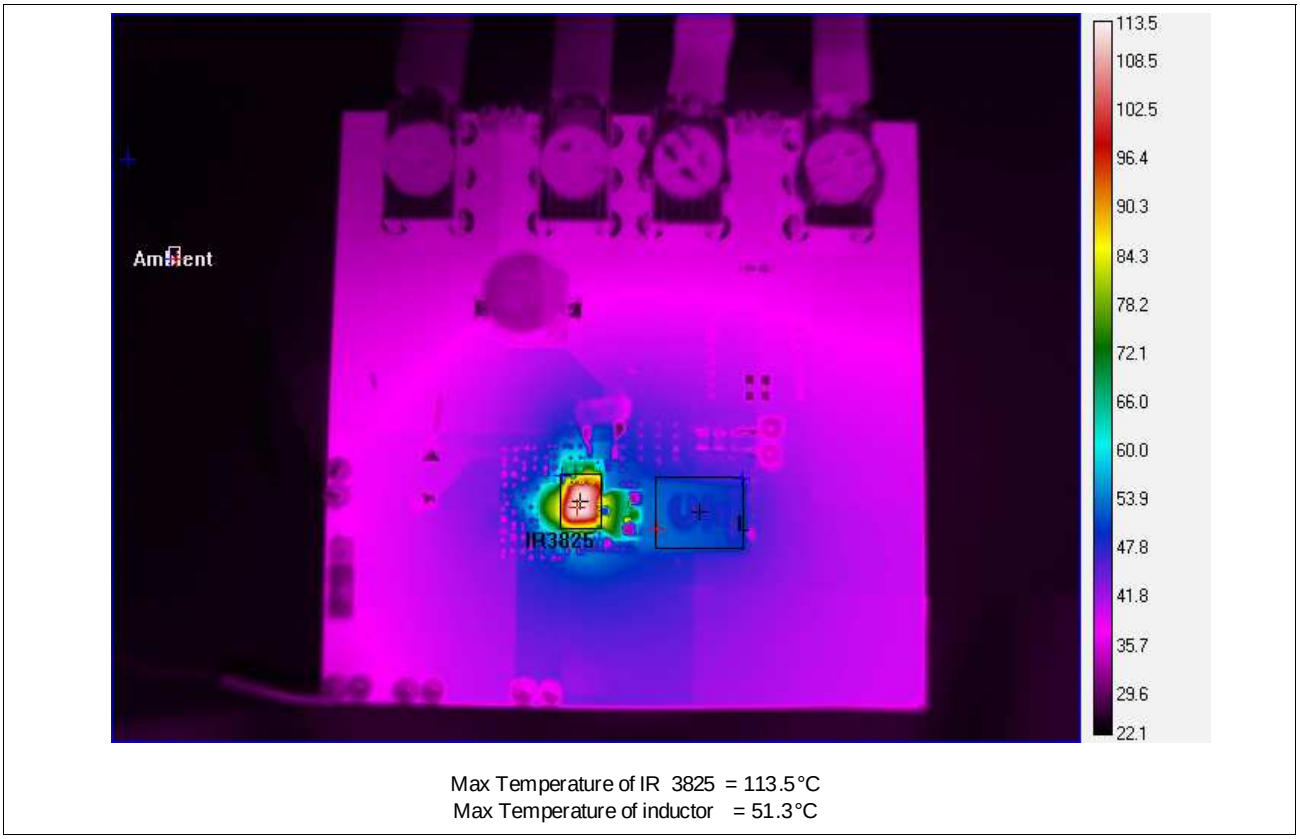


Figure 7-14 Thermal Image of the Board at 20A Load

8 Layout Considerations

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Make the connections for the power components on the top layer with wide, copper filled areas or polygons. In general, it is desirable to make proper use of power planes and polygons for power distribution and heat dissipation.

The inductor, output capacitors and the IR3825 should be as close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place the input capacitor directly at the PVin pin of IR3825. The critical bypass components such as capacitors for Vin, Vcc and Vref should be close to their respective pins. The feedback part of the system should be kept away from the inductor and other noise sources. It is important to place the feedback components including feedback resistors and compensation components close to Fb and Comp pins.

In a multilayer PCB use one layer as a power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point. It is recommended to place all the compensation parts over the analog ground plane on top layer.

The Power QFN is a thermally enhanced package. Based on thermal performance it is recommended to use at least a 4-layers PCB. To effectively remove heat from the device the exposed pad should be connected to the ground plane using vias. The figures illustrate the implementation of the layout guidelines outlined above, on the IRDC3825 4-layer demo board.

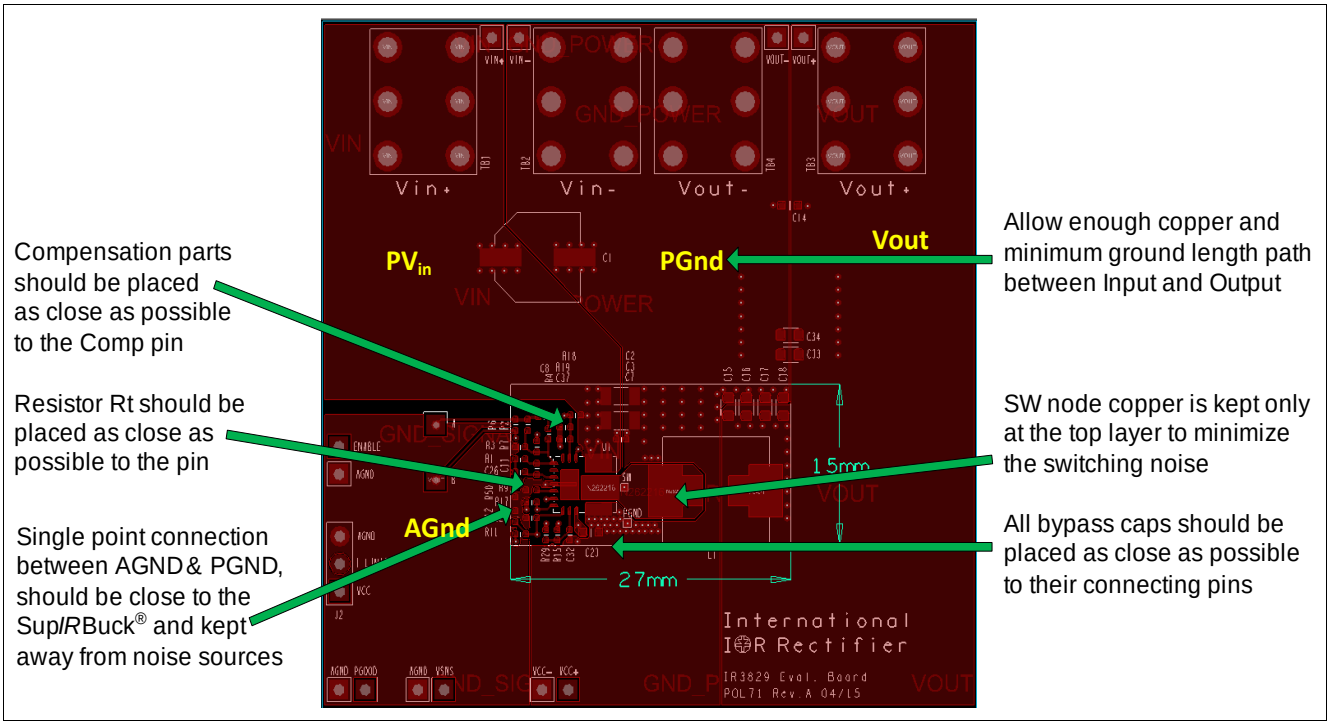


Figure 8-1 IRDC3825 Demo Board – Top Layer

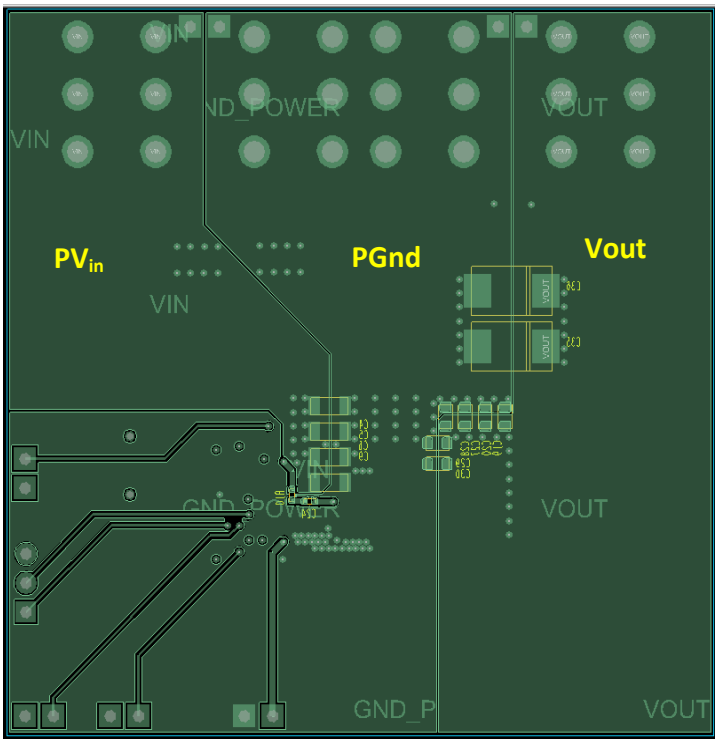


Figure 8-2 IRDC3825 Demo Board – Bottom Layer

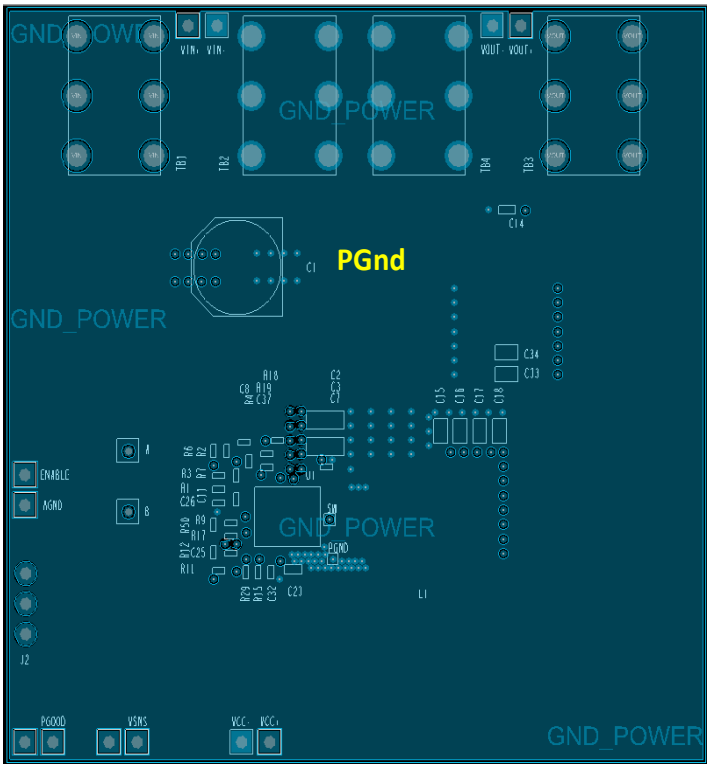


Figure 8-3 IRDC3825 Demo Board – Middle Layer 1

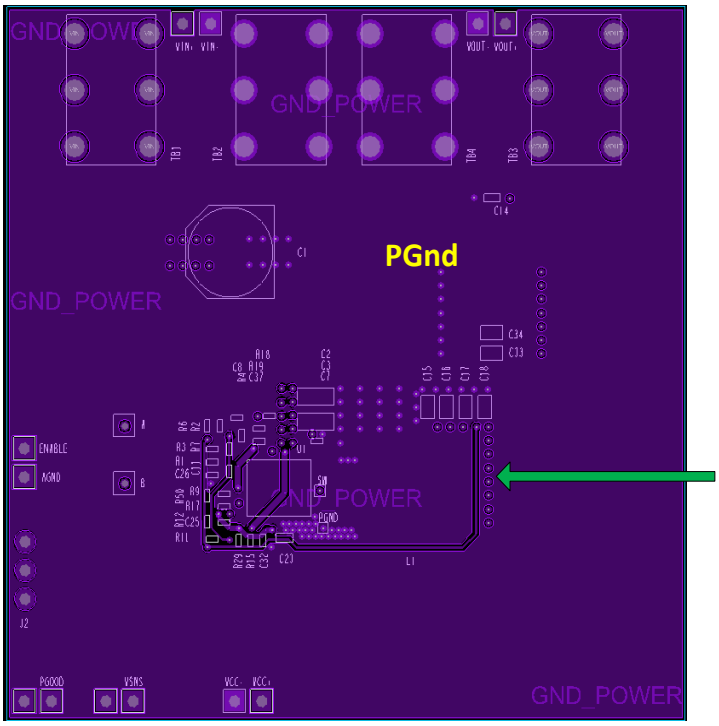


Figure 8-4 IRDC3825 Demo Board – Middle Layer 2

8.1 PCB Metal and Component Placement

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout as shown in following Figures. PQFN devices should be placed to an accuracy of 0.050mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes and experiments should be run to confirm the limits of self-centering on specific processes.

For further information, please refer to “SupIRBuck® Multi-Chip Module (MCM) Power Quad Flat No-Lead (PQFN) Board Mounting Application Note.” (AN1132)

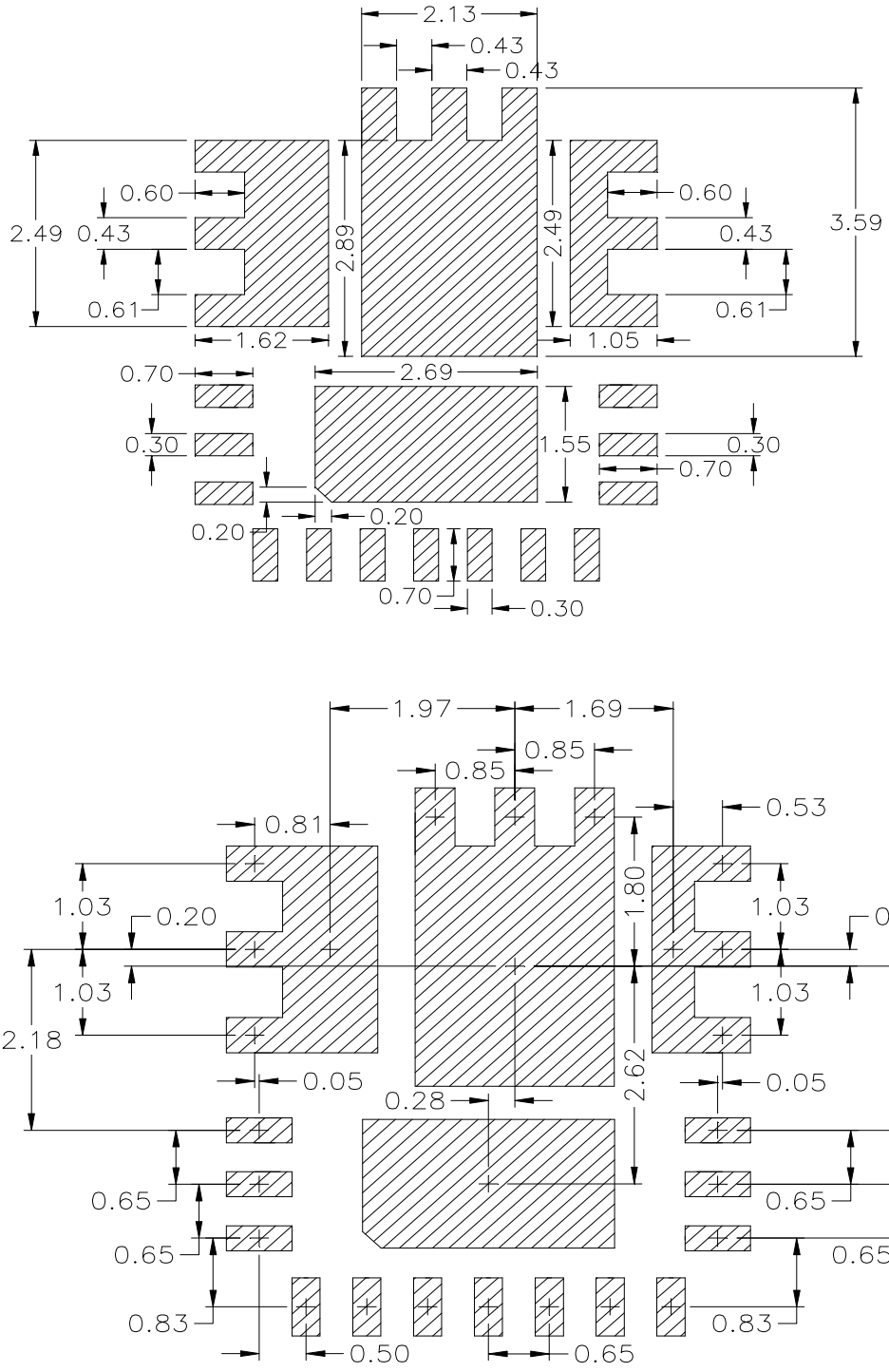


Figure 8-5 PCB metal pad sizing and spacing (all dimensions in mm)

8.2 Solder Resist

- It is recommended that the larger Power or Land Area pads are Solder Mask Defined (SMD.)
  - This allows the underlying Copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability.
- When using SMD pads, the underlying copper traces should be at least 0.05mm larger (on each edge) than the Solder Mask window, in order to accommodate any layer to layer misalignment. (i.e. 0.1mm in X & Y.)
- However, for the smaller signal type leads around the edge of the device, it is recommended that these are Non Solder Mask Defined or Copper Defined.
- When using NSMD pads, the Solder Resist Window should be larger than the Copper Pad by at least 0.025mm on each edge, (i.e. 0.05mm in X&Y,) in order to accommodate any layer to layer misalignment.
- Ensure that the solder resist in-between the smaller signal lead areas are at least 0.15mm wide, due to the high x/y aspect ratio of the solder mask strip.

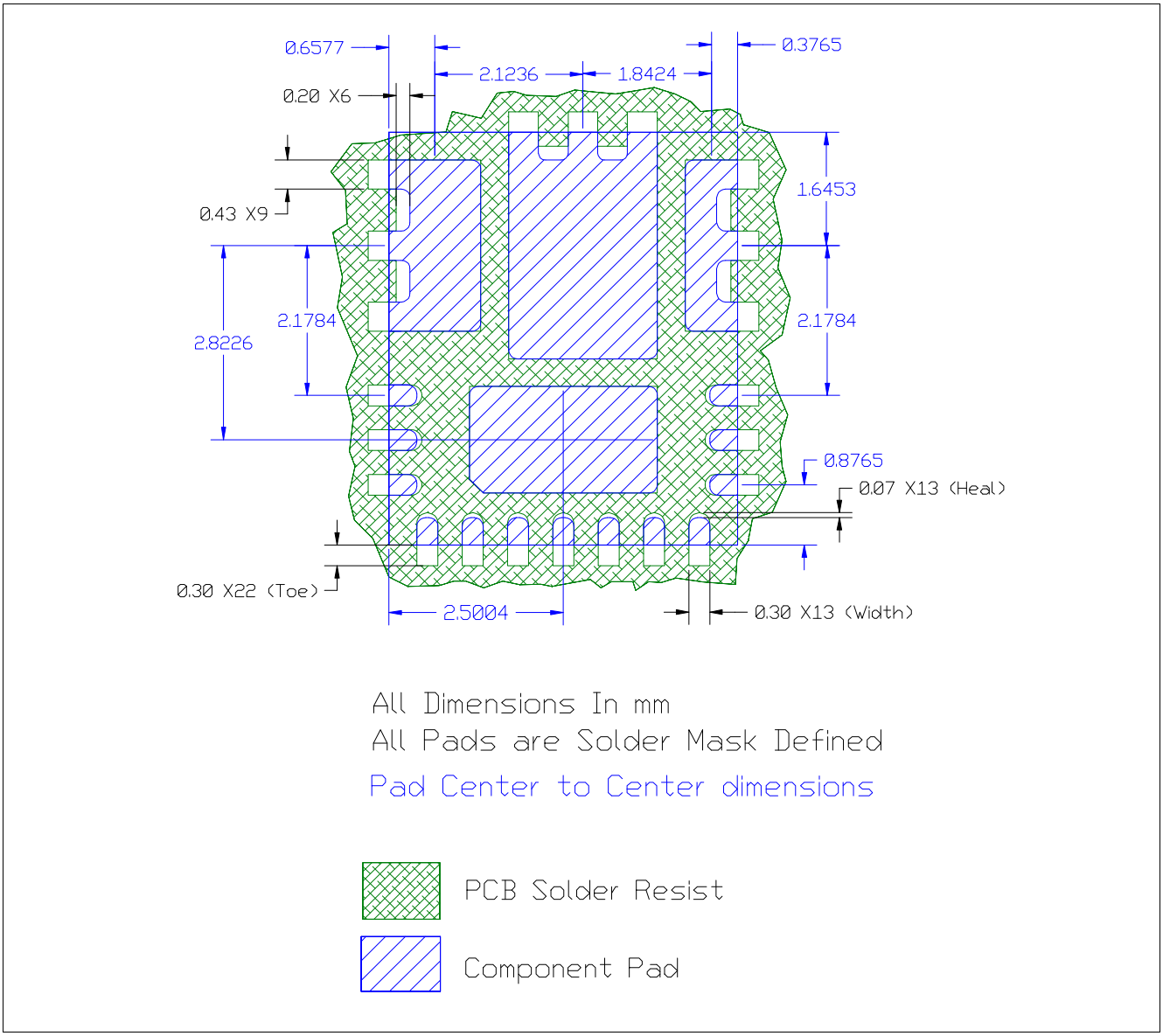


Figure 8-6 Solder Resist

8.3 Stencil Design

- Stencils for PQFN can be used with thicknesses of 0.100-0.250mm (0.004-0.010"). Stencils thinner than 0.100mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground pad; high reductions sometimes create similar problems. Stencils in the range of 0.125mm-0.200mm (0.005-0.008"), with suitable reductions, give the best results.
- Evaluations have shown that the best overall performance is achieved using the stencil design shown in following Figure. This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.

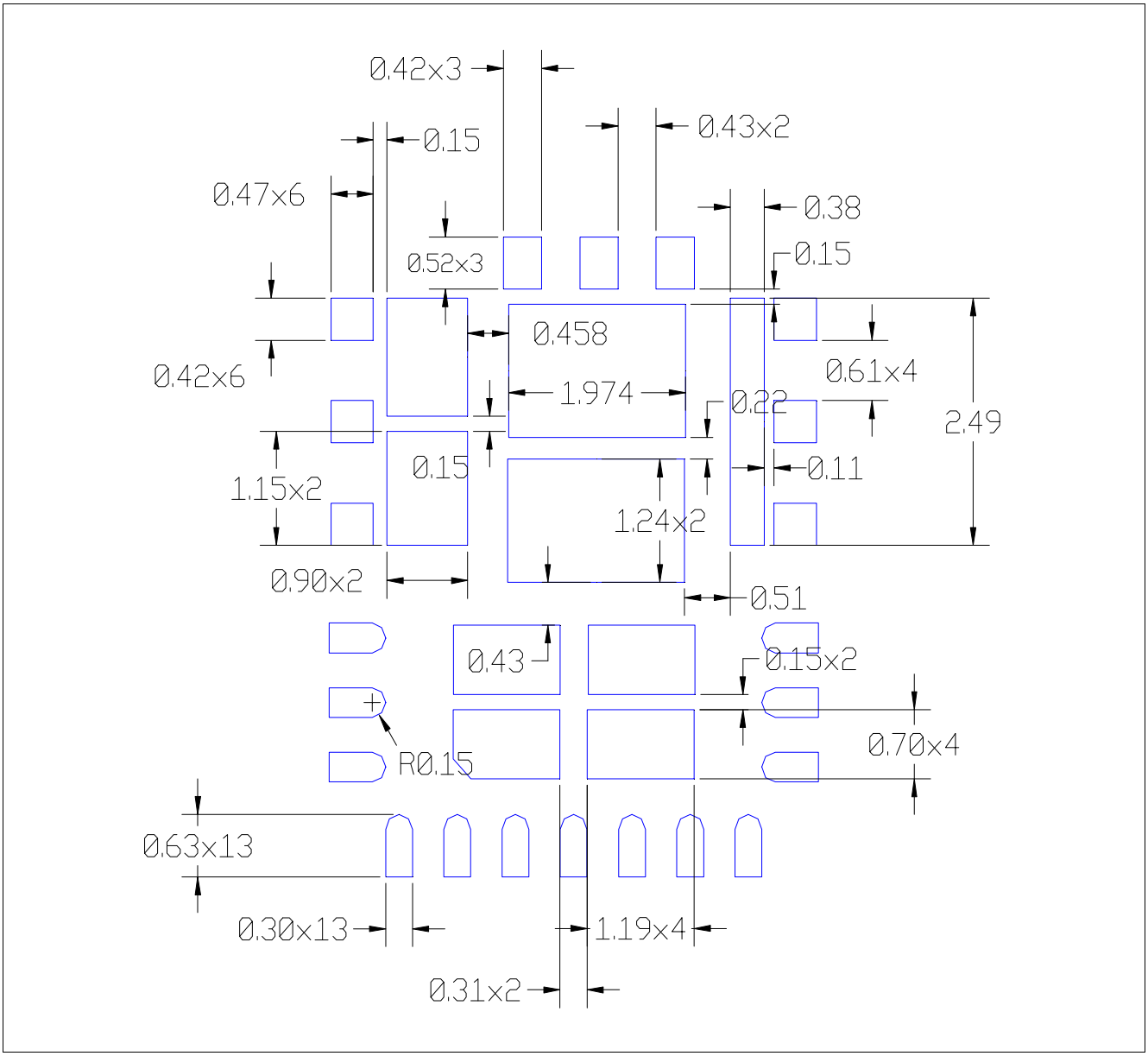


Figure 8-7 Stencil pad spacing (all dimensions in mm)

8.4 Marking Information

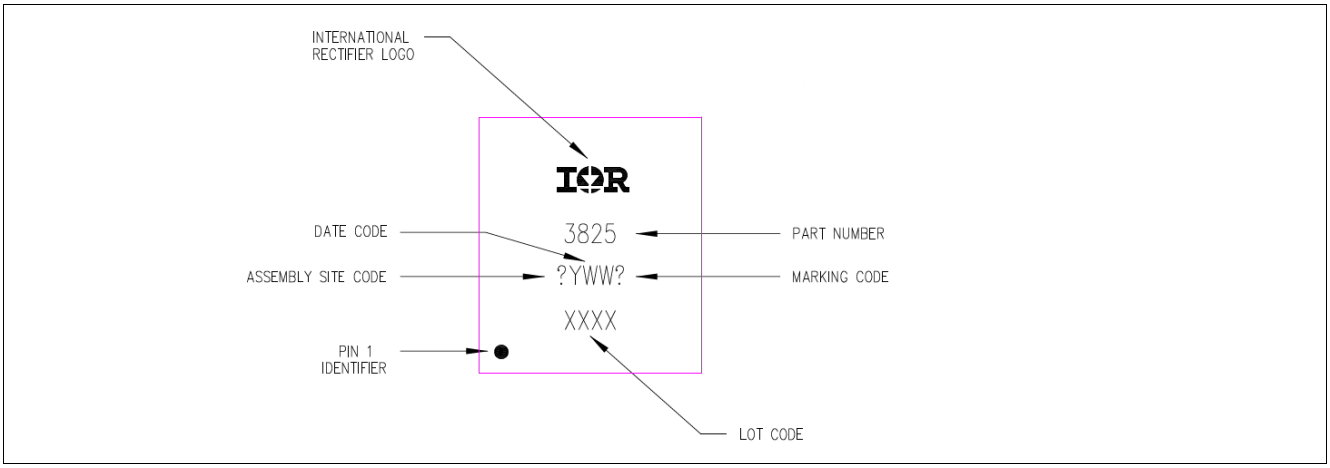


Figure 8-8 Marking information

8.5 Package Information

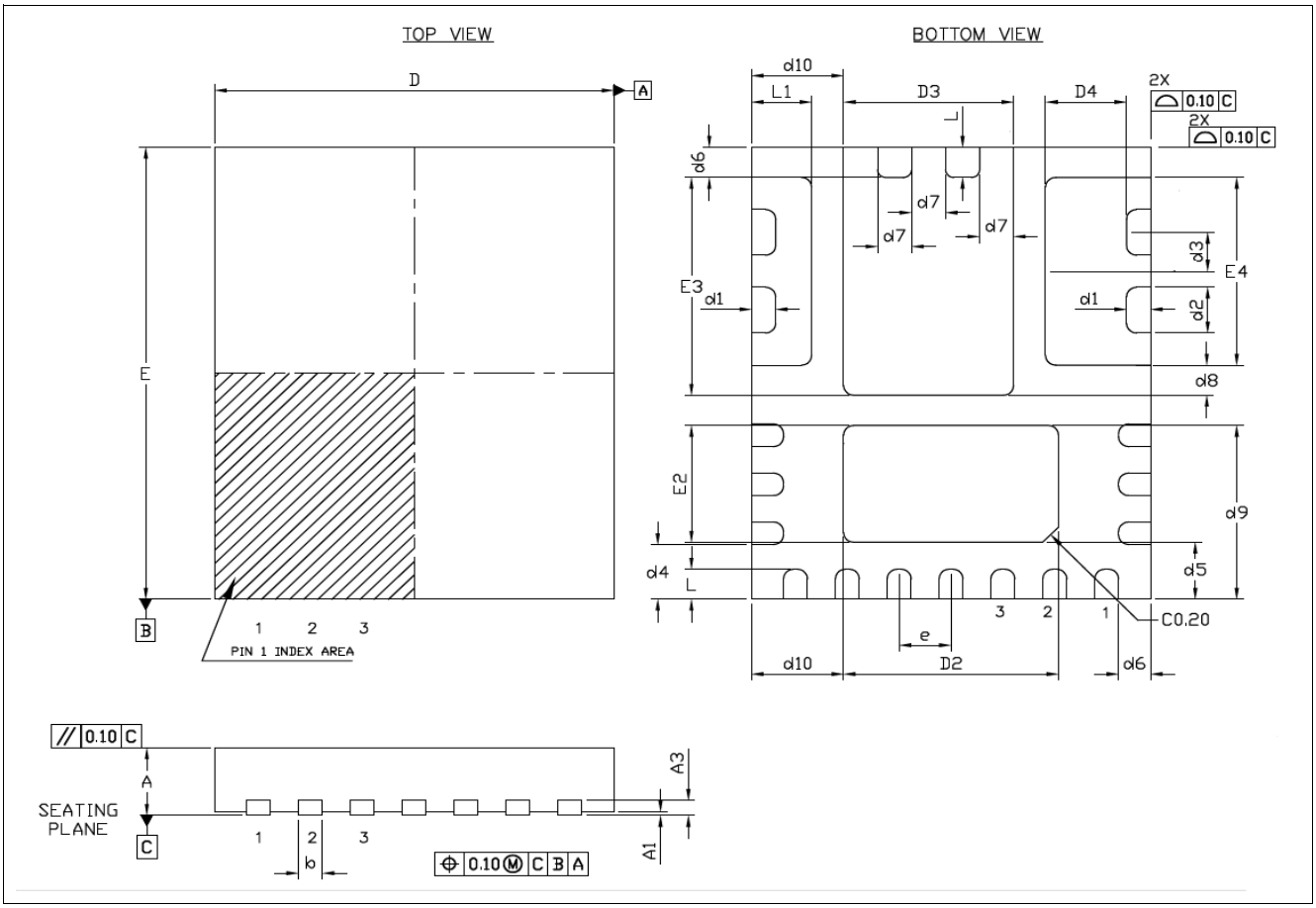


Figure 8-9 Package Dimensions

SYMBOL	Common					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.85	0.90	0.95	0.034	0.036	0.038
A3	0.203 REF.			0.008 REF.		
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
D	4.90	5.00	5.10	0.193	0.197	0.201
D2	2.64	2.69	2.74	0.104	0.106	0.108
D3	2.08	2.13	2.18	0.082	0.084	0.086
D4	0.97	1.02	1.07	0.039	0.041	0.043
E	5.90	6.00	6.10	0.233	0.237	0.241
E2	1.50	1.55	1.60	0.060	0.062	0.063
E3	2.84	2.89	2.94	0.112	0.114	0.116
E4	2.44	2.49	2.54	0.097	0.099	0.100
e	0.65 BSC			0.026 BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.70	0.75	0.80	0.028	0.030	0.031
d1	0.30 REF.			0.012 REF.		
d2	0.61 REF.			0.024 REF.		
d3	0.52 REF.			0.020 REF.		
d4	0.73 REF.			0.029 REF.		
d5	0.76 REF.			0.030 REF.		
d6	0.40 REF.			0.016 REF.		
d7	0.43 REF.			0.017 REF.		
d8	0.40 REF.			0.016 REF.		
d9	2.31 REF.			0.091 REF.		
d10	1.15 REF.			0.045 REF.		

Figure 8-10 Package Dimensions Table

8.6 Environmental Qualifications

Table 8-1 Environmental Qualifications†

Qualification Level		Industrial	
Moisture Sensitivity Level		**PQFN 5 mm x 6 mm**	JEDEC Level 2 @ 260°C
ESD	Machine Model (JESD22-A115A)	Class A	
		< 200V	
	Human Body Model (JESD22-A114F)	Class 2	
		≥ 2000V to < 4000V	
	Charged Device Model (JESD22-C101D)	Class III	
		≥ 500V to ≤1000V	
RoHS Compliant		Yes	

† Qualification standards can be found at Infineon web site: **www.irf.com**

Revision History:	
Revision / Date	**Subjects (major changes since previous revision)**
IR3825 Rev 3.7, 03/24/2016	
3.7 03-24-16 S476	Initial web release.

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