XMC1000 System

XMC™ microcontrollers

September 2016

Agenda

1. XMC1000 and ARM® Cortex®-M0
2. Memories
3. Bus system
4. Interrupt system
5. Clock
6. Reset
7. Power
8. Ports

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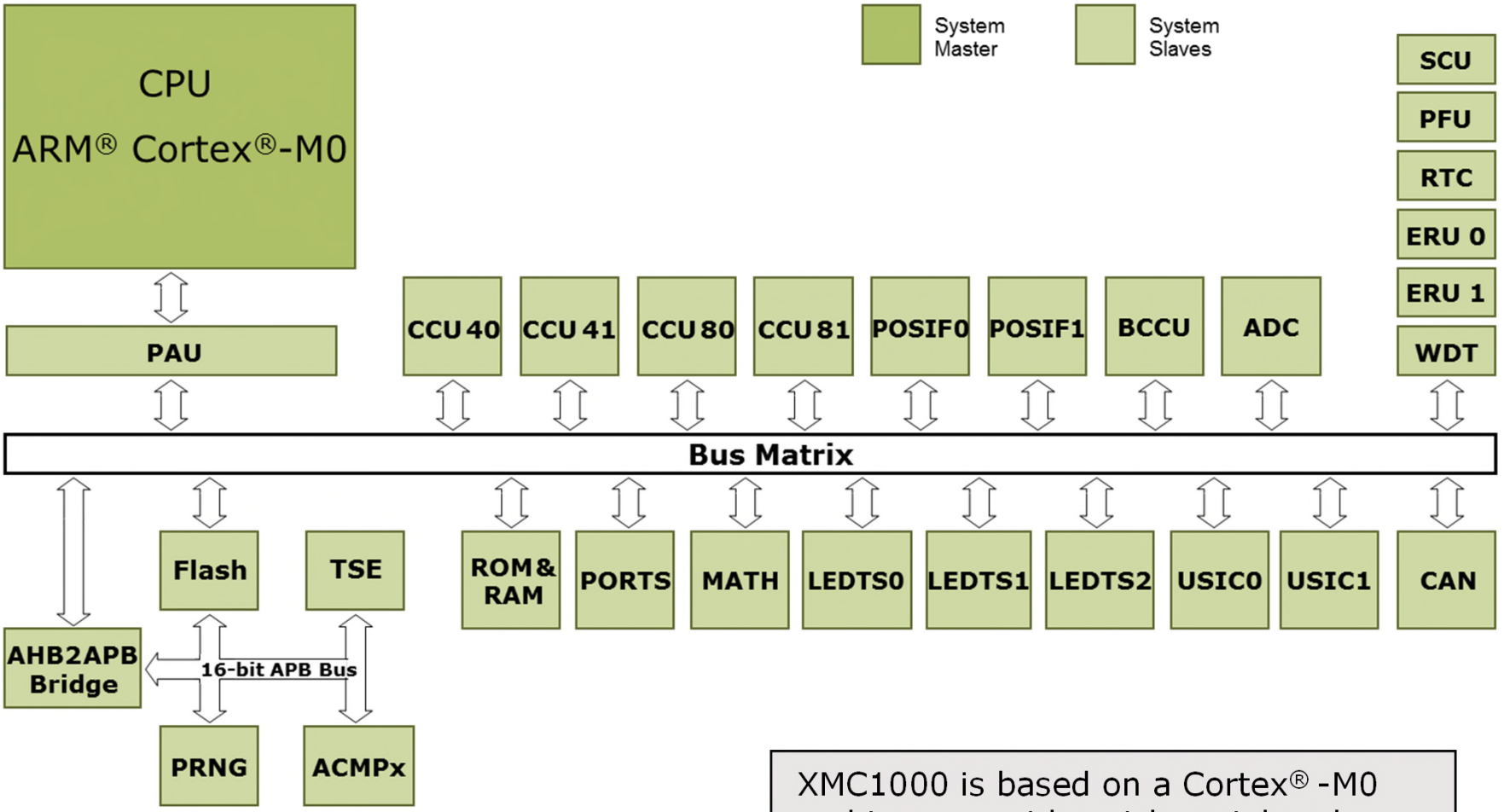
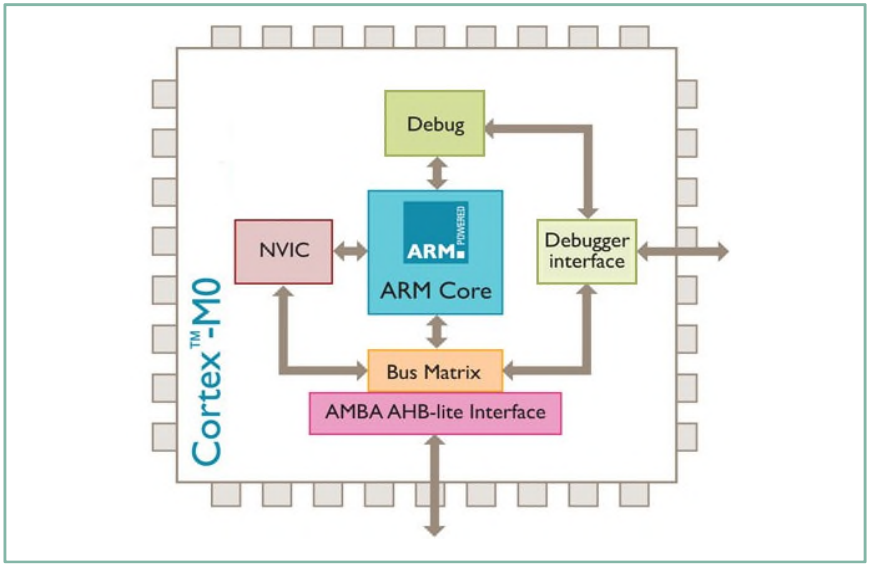
XMC1000 block diagram



XMC1000 is based on a Cortex® -M0 architecture with a rich peripheral set for sensor/actuator applications.

Architecture of Cortex®-M0



Highlights

Cortex®-M0 is a lean 32-bit processor core with 0.84 DMIPS/MHz. It allows modern programming style in C-language to reduce development time.
Its optimized interrupt controller allows use in hard real-time applications.
Widespread standard core offers a broad variety of software tools and components.

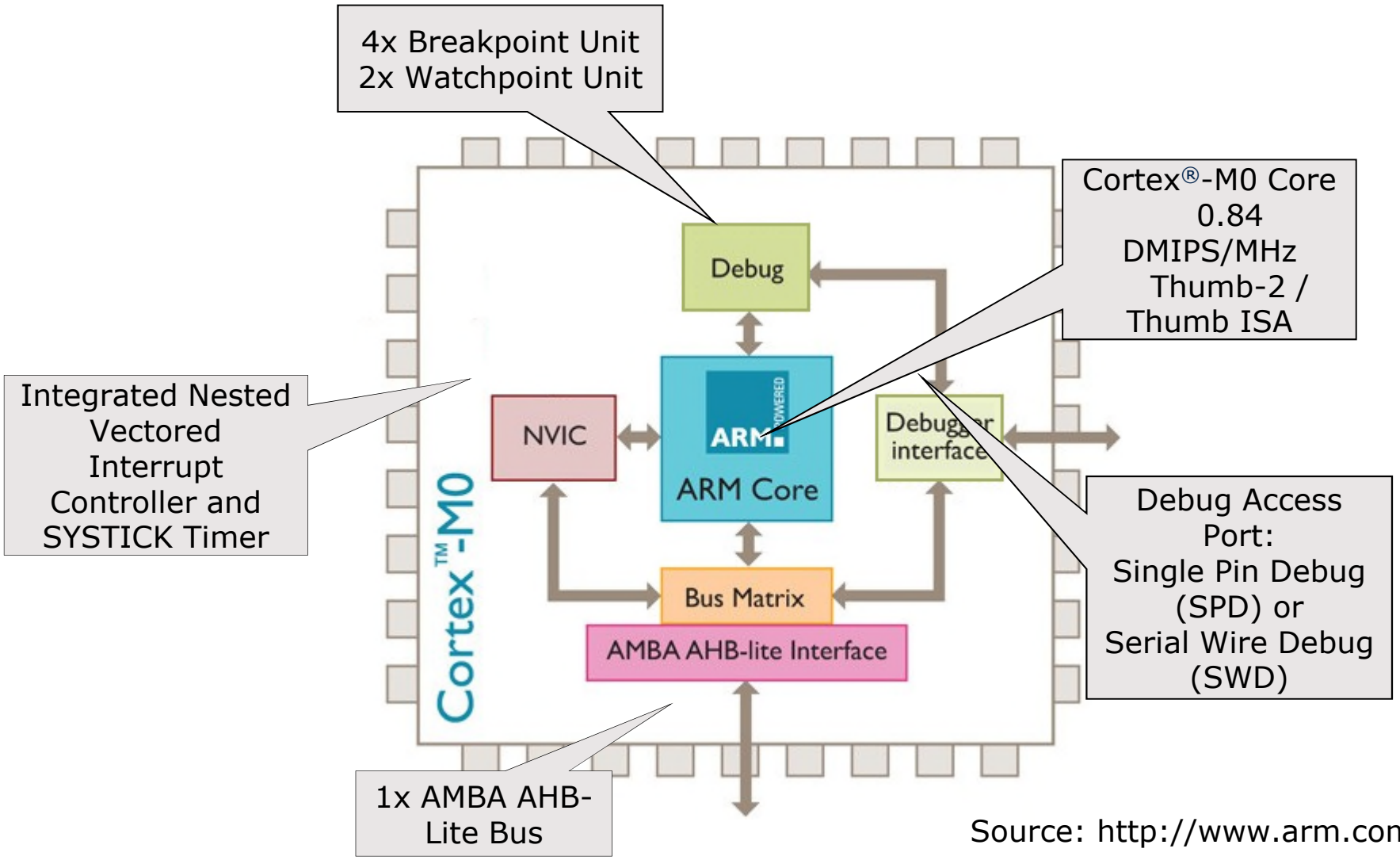
Key features

- Standard core
- Modern 32-bit instruction set
- Upwards compatible to Cortex® M3/M4

Customer benefits

- Availability of third party tools, software libraries and engineering force
- Using C language reduces development time and maintenance cost
- Offers high scalability with reusing software components

Architecture of Cortex®-M0 Standard core (1/2)



Source: http://www.arm.com

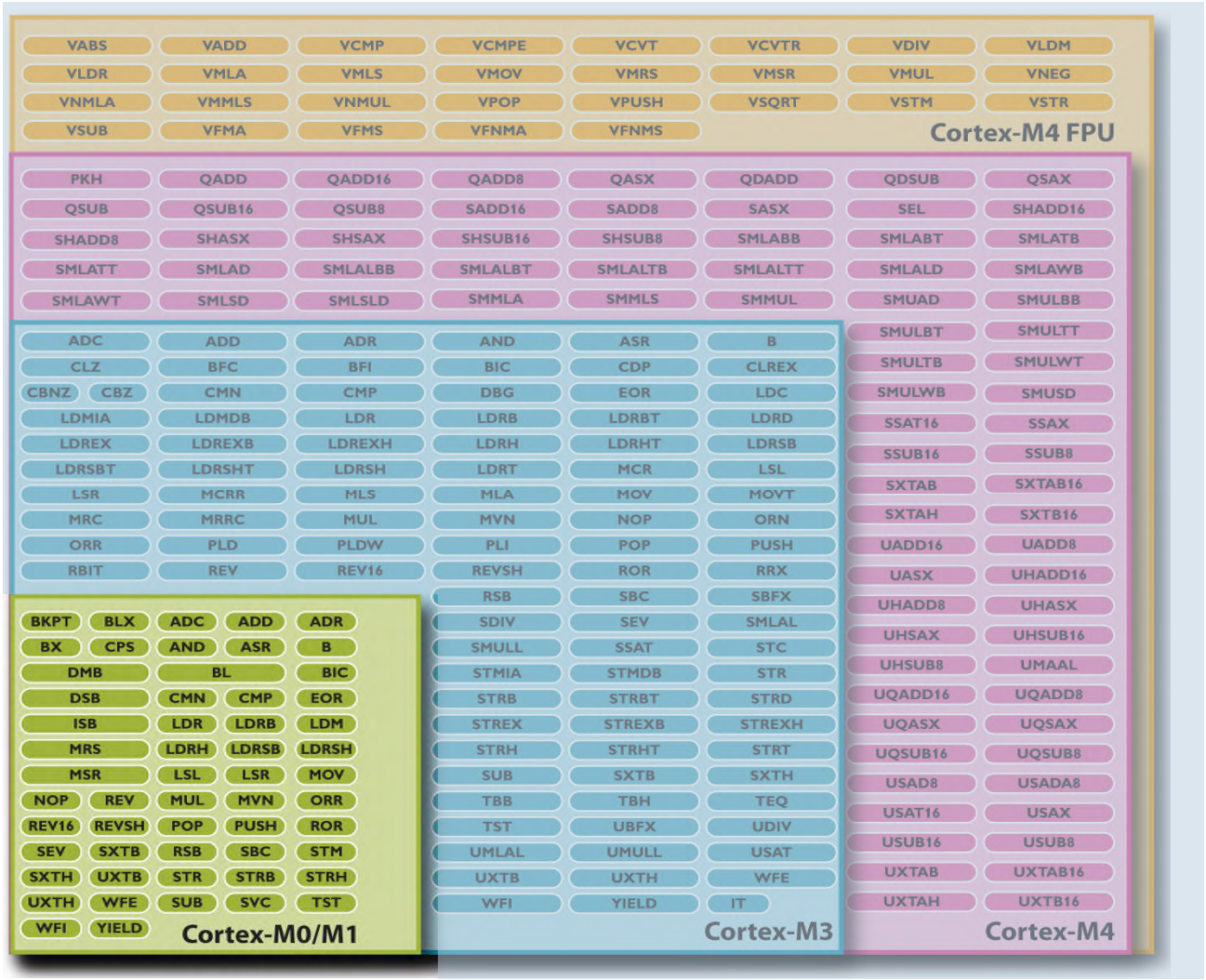
Architecture of Cortex®-M0 Standard core (2/2)

ARM® Cortex®-M	Thumb	Thumb-2	ARM® architecture	Core architecture
Cortex®-M0	Most	Subset	ARMv6-M	Von Neumann
Cortex®-M3	Entire	Entire	ARMv7-M	Harvard
Cortex®-M4	Entire	Entire	ARMv7E-M	Harvard

ARM® Cortex®-M	Hardware multiply	Hardware divide	Saturated math	DSP extensions	Floating-point
Cortex®-M0	1 or 32 cycle	No	No	No	No
Cortex®-M3	1 cycle	Yes	Yes	No	No
Cortex®-M4	1 cycle	Yes	Yes	Yes	Optional

Source: Wikipedia

Architecture of Cortex®-M0
Modern 32-bit instruction set



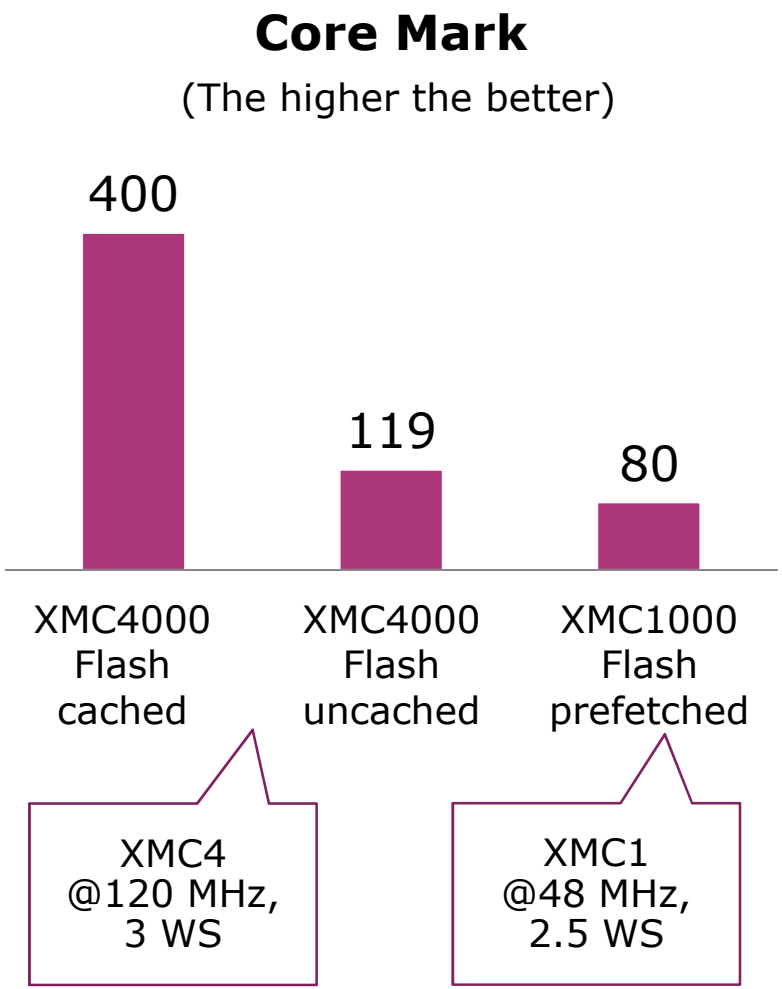
Cortex®-M0 is an ARMv6-M architecture.

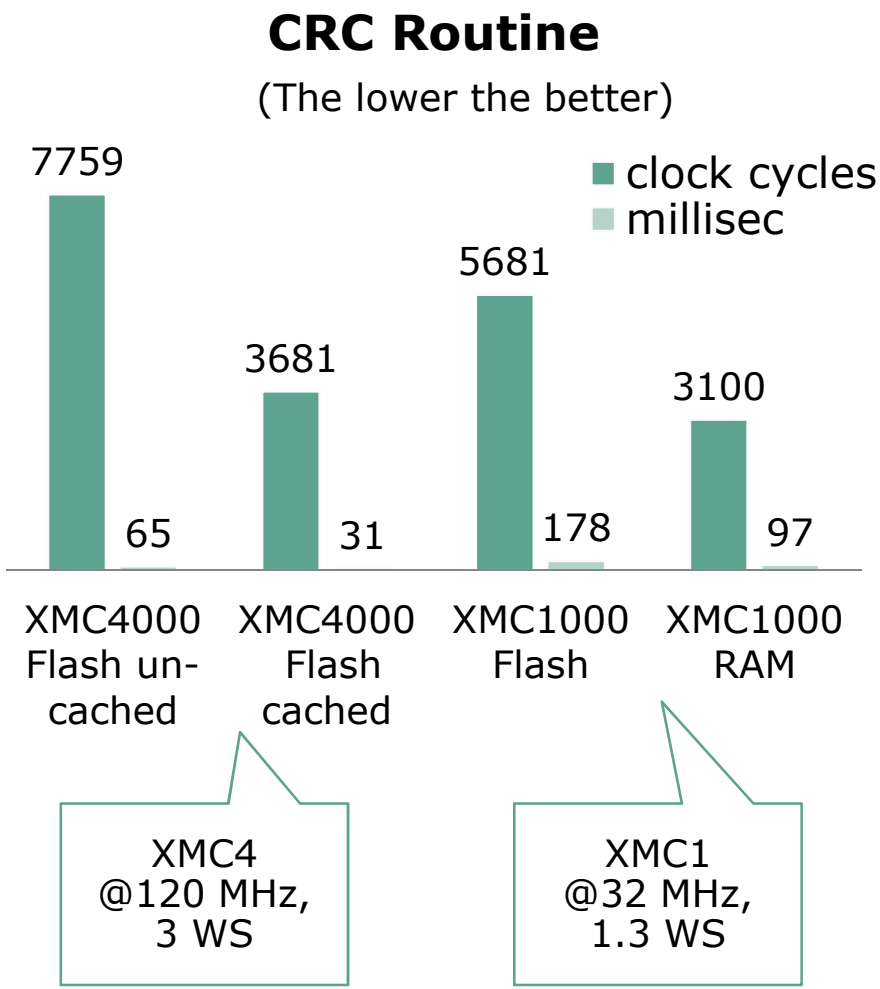
It has a subset of Thumb and Thumb-2 instruction sets.

Cortex® M0 is fully upwards compatible to Cortex®-M4

Source: http://www.arm.com

Architecture of Cortex®-M0
CPU performance benchmark





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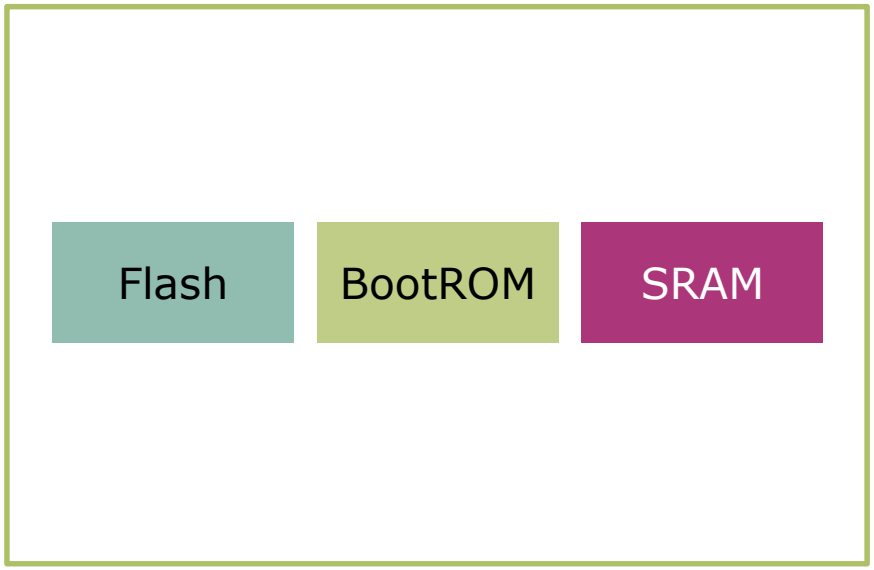
Memories



Highlights

The memory map is based on standard ARM® Cortex®-M0 system memory map.

The linear address space of the 32-bit architecture provides full access to all code, memory and peripheral addresses.

Key feature

- Parity protected RAM and ECC protected flash
- Memory and IP protection
- Excellent program/erase timing with high endurance

Customer benefits

- High code/data integrity due to hardware error detection and correction mechanism
- Protected against unauthorized read-out of memory content
- No need for external EEPROM, reduced system cost

Memories
Parity protected RAM and ECC protected flash

- RAM supports parity bit generation and error detection
  - Parity bit can be inverted to force an error for test purposes
  - Hardware support for ClassB Library saves CPU load for volatile memory test
- Flash supports ECC with:
  - Single bit error correction
  - Partial double bit error detection
- Flash supports automatic verification of programmed data
- Flash supports configurable erase and write protection
- Flash provides a low power sleep mode
  - Enabled/disabled through NVMCONF.NVM_ON bit
- Zero-wait-state access to RAM @48 MHz
  - 8-bit, 16-bit and 32-bit write access
  - 32-bit read access

Memories
Memory and IP protection (1/2)

- IP protection
  - Unauthorized external access to Flash is blocked
    - Boot options to download and execute external code are blocked
    - Unauthorized read out of critical data and user IP from Flash is prevented
    - Only user code originating from the Flash can be executed
  - Blocking mechanism
    - After user code is programmed into Flash, the Boot Mode Index (BMI) is expected to be switched to “user productive mode”
    - Entry to other boot modes is blocked
    - User code can trigger a change in BMI but that will first erase the complete user Flash

Memories
Memory and IP protection (2/2)

- Access protection during run-time
  - Flash write and erase protection
    - A range of Flash sectors starting from sector 0 can be user-configured to be erase- and write-protected
  - SFR Bit protection scheme
    - Specific system-critical SFR bits (e.g. CLKCR.PCLKSEL) require a special software write sequence
  - Privilege access control scheme
    - Each memory address range (or sub-block) that supports this scheme has a disable bit
    - When the bit is set, the corresponding memory address range is rendered invalid
    - Any access to such an invalid address causes a bus error
    - The same bit can be cleared to enable access again

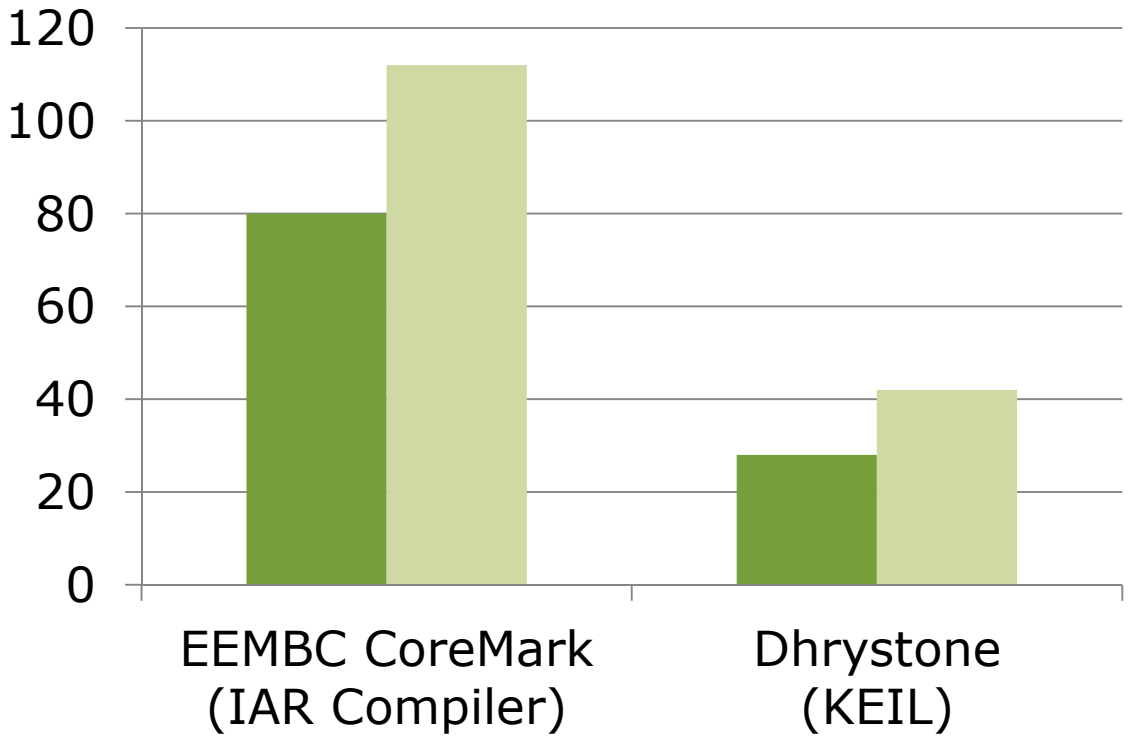
Memories
Excellent timings with high endurance

Parameter	Min.	Typical	Max.	Unit	Note
Voltage range	1.8	-	5.5	V	
Erase time per page	6.8	7.1	7.6	ms	Page = 256 bytes
Erase all	-	-	8	s	At 200 Kbytes
Write time per block	102	152	204	µs	Block = 16 bytes
Data retention	20	-	-	years	Ta = 85°C, 100 cycles @ 200 Kbyte data
	10	-	-	years	Ta = 85°C, 10k cycles @ 16 Kbyte data
Flash wait states	0	0	0	cycles	f_{MCLK} = 8 MHz
	0	1	1	cycles	f_{MCLK} = 16 MHz
	1	1.3	2	cycles	f_{MCLK} = 32 MHz
	2	2.5	3	cycles	f_{MCLK} = 48 MHz
Erase cycles per page	-	-	$5*10^4$	cycles	
Total erase cycles	-	-	$2*10^6$	cycles	

› Note: When Flash is busy, any access to Flash memory or write access to Flash SFRs will be stalled

Memories
Flash and SRAM performance

- Performance of Cortex®-M0 @48 MHz
  - Based on XMC1400



Flash (perfected)

Flash + SRAM

Note: SRAM is too small to run the entire benchmark codes

Note: Additional performance can be gathered using the MATH Co-processor

Note: higher numbers are better

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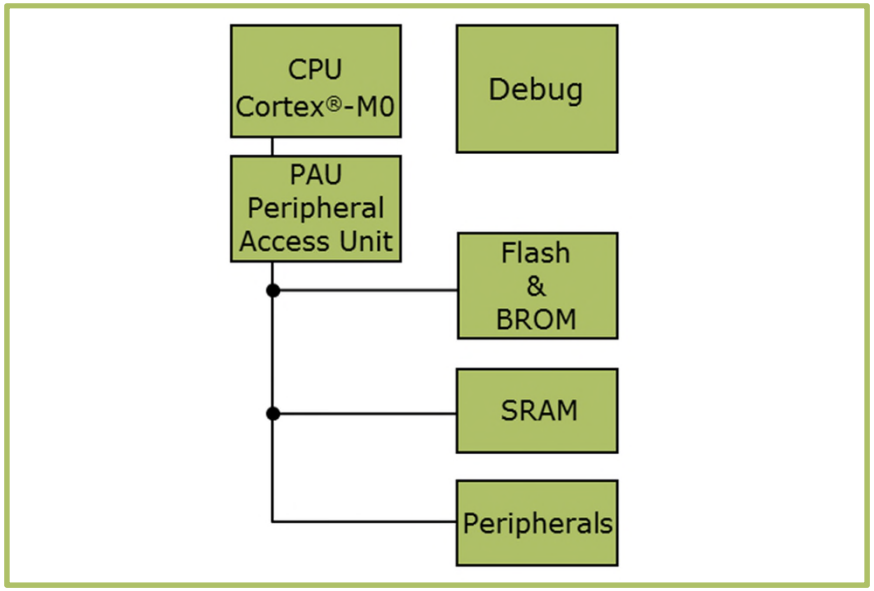
Bus system
Peripheral Access Unit (PAU)



Highlights

Allows user application to enable/ disable the access to programmable memory locations.

Generates a Hard Fault exception when there is an access to a disabled or unassigned address location.

Key features

- Protect against unintencional memory access
- Hard fault exception for invalid access

Customer benefits

- Safety mechanism for runaway code
- Enter safe state in case of runaway code

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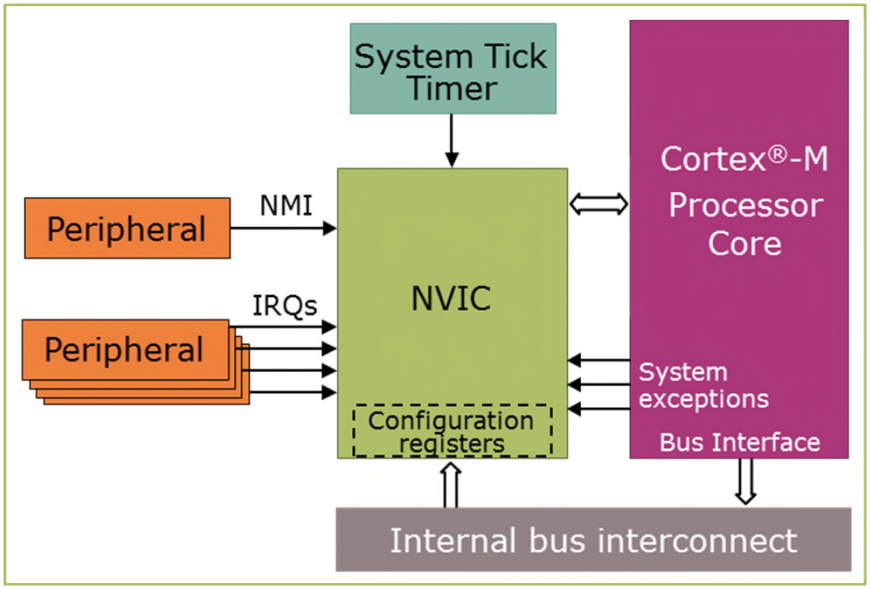
Interrupt system



Highlights

The interrupt system consists of the Nested Vectored Interrupt Controller (NVIC) and the interrupt generation blocks in the individual modules.

Events from peripherals can be routed via the connection matrix directly to other peripherals and can trigger interrupt requests.

Key features

- 4 programmable priority levels
- Interrupt tail-chaining
- Automatic state saving and restoring

Customer benefits

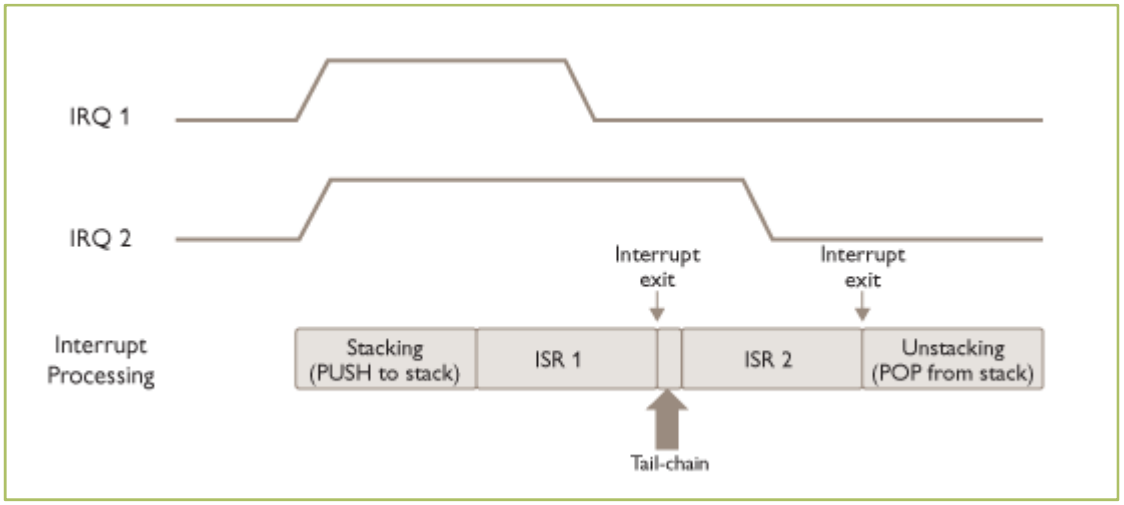
- Flexible priority control
- Speed-up interrupt servicing
- Low latency exception handling

Interrupt system
4 programmable priority levels

- NVIC supports 32 interrupt nodes
- Each interrupt node has an 8-bit priority field (only 2 MSBs are writable) in IPRn (Interrupt Priority Register)
- A priority level is assigned to an interrupt node by writing to its corresponding priority field
- The lower the value written to the priority field, the higher the priority
- A higher priority interrupt can interrupt an existing lower priority interrupt, resulting in nested interrupts
- When multiple interrupts have the same priority level, the pending interrupt with the lower node ID takes precedence

Interrupt system
Interrupt tail-chaining

- When a current ISR is completed and there is a pending interrupt, stack pop is skipped and control is transferred to the new ISR
- Allows interrupt servicing to speed up



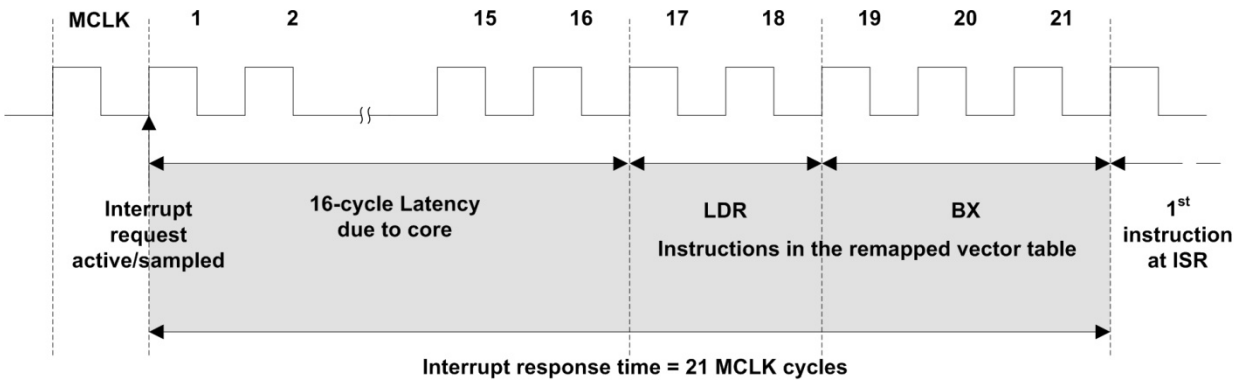
Tail-chaining
Source: http://www.arm.com

Interrupt system
Automatic state saving and restoring

- Automatic state saving and restoring are done without any instruction overhead:
  - State registers are pushed onto the stack before entering the ISR
  - Reading of vector table entry is done after the state saving
  - State registers are popped after exiting the ISR

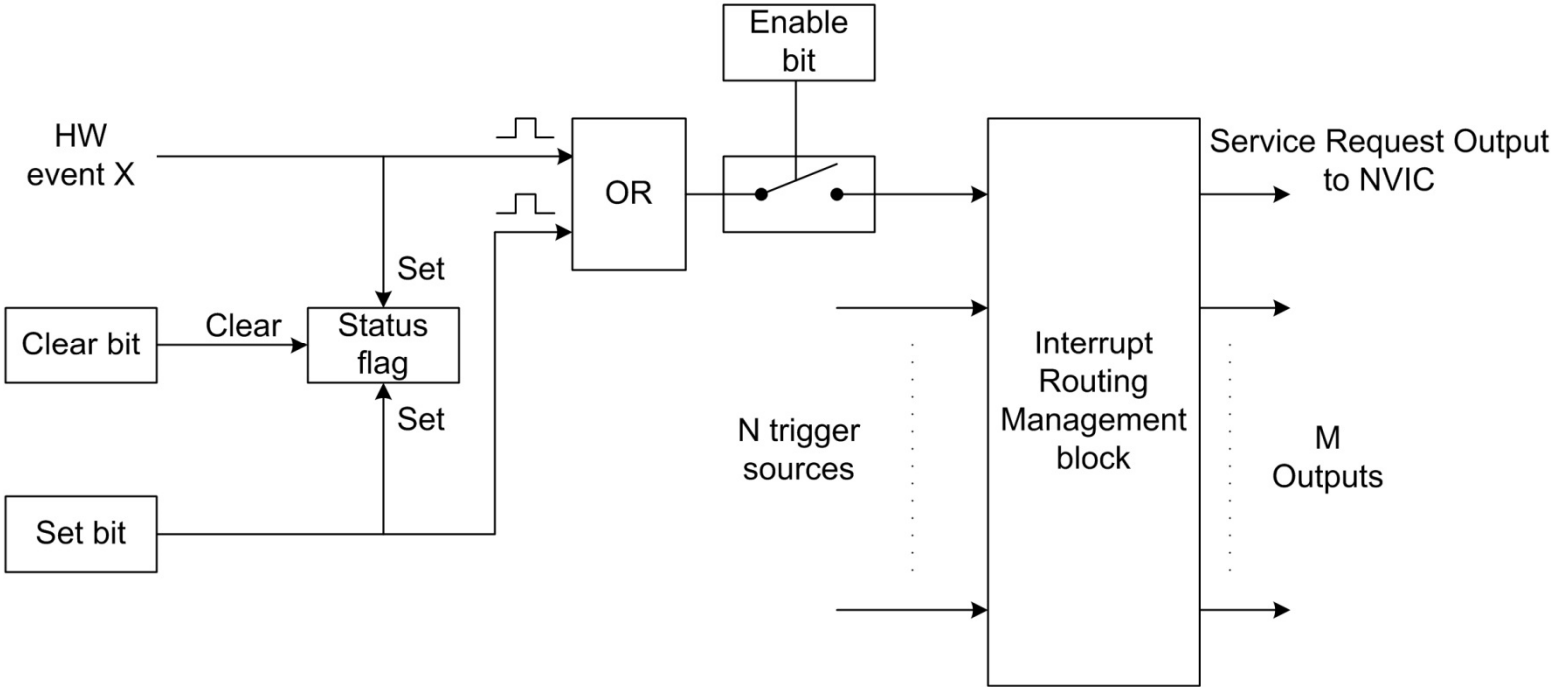
Interrupt system
Interrupt latency

- Defined as the time from detection of interrupt pulse and latching of interrupt by NVIC, to execution of first instruction in ISR
- Typically 21 MCLK cycles



- *Note: Flash wait states are not considered*

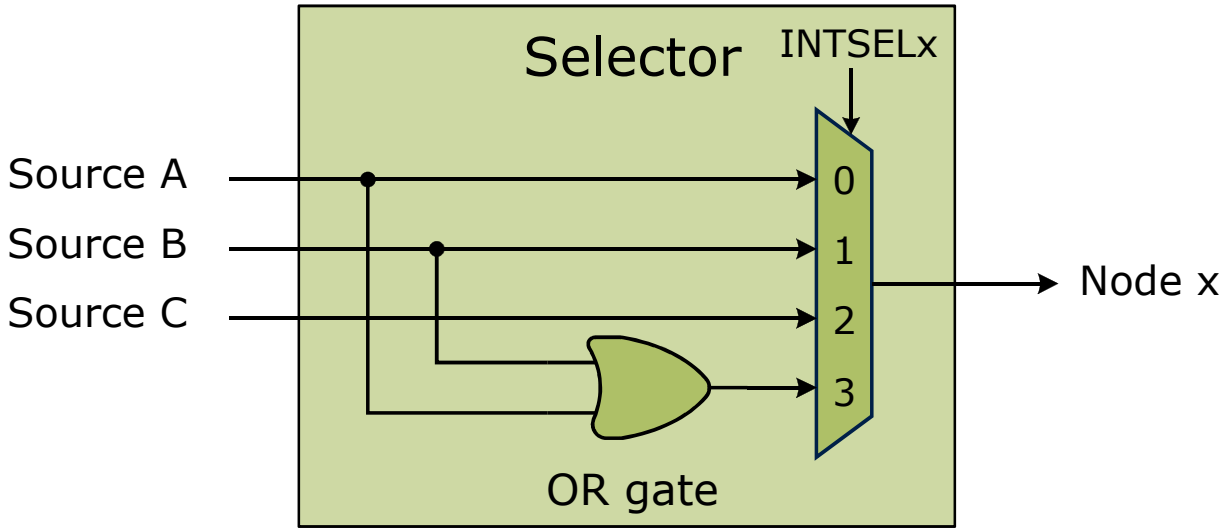
Interrupt system
General module interrupt structure



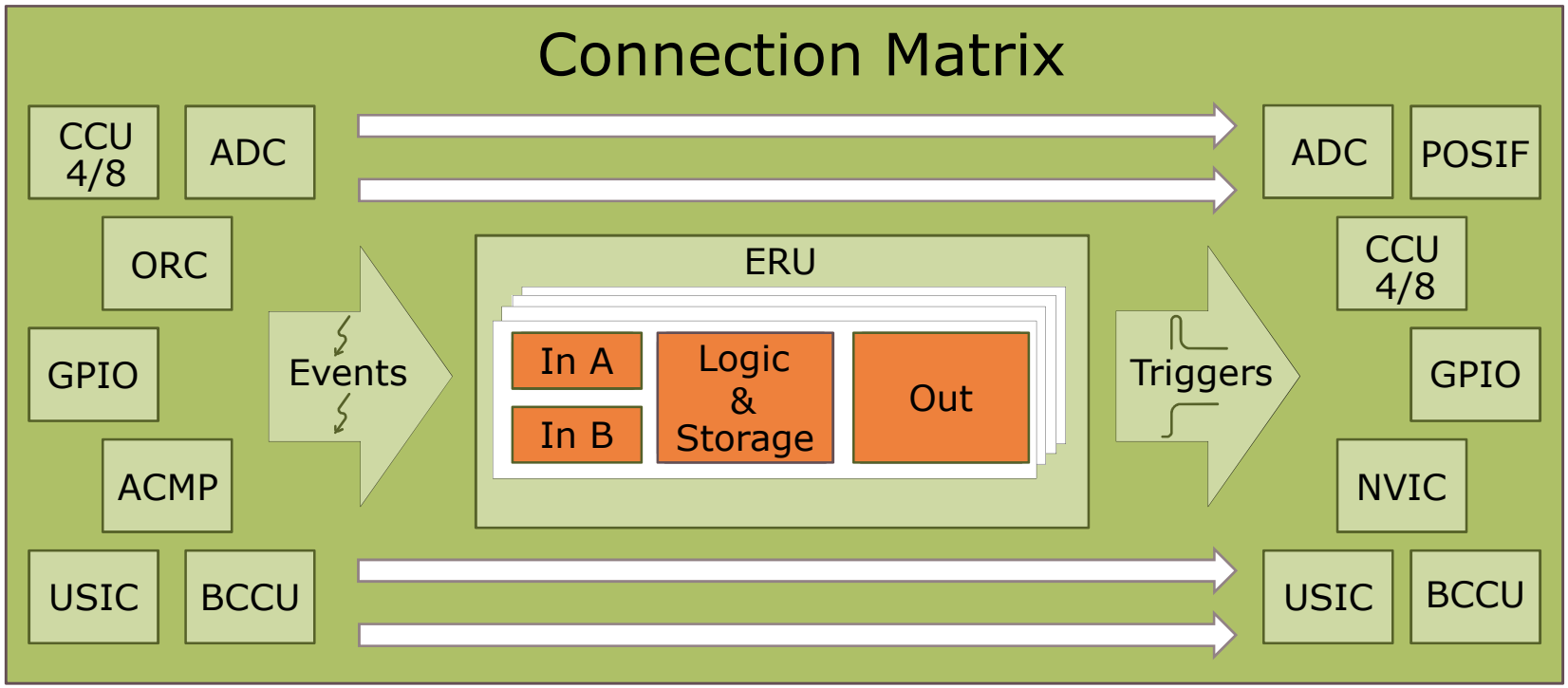
- Generates interrupt pulses to NVIC
- Independent of status flag level

Interrupt system
Interrupt node source extension

- XMC1400 only
- For additional flexibility
- Each interrupt node can select out of 3 service request sources



Interrupt system
Connection matrix



- Peripheral outputs can trigger events which are routed to peripheral inputs or to the NVIC
- Additional event routing is possible via the Event Request Unit ERU which can store events and logically combine two events
- This allows very flexible and powerful system design

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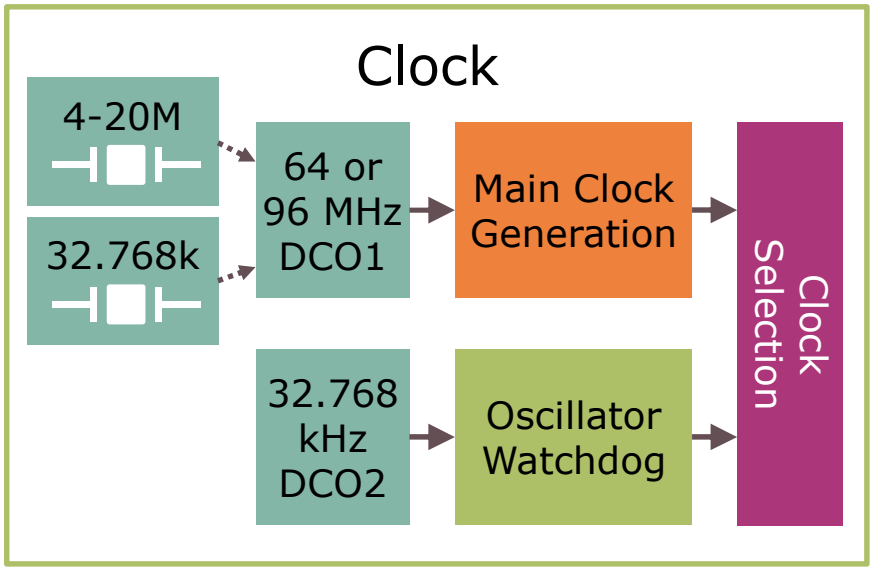
Clock



Highlights

The main function of the clock system is to generate clock for the CPU and the on-chip peripherals.

An oscillator watchdog monitors the frequencies of the two on-chip oscillators.

Peripheral clock can run at twice the speed of CPU clock.

Key features

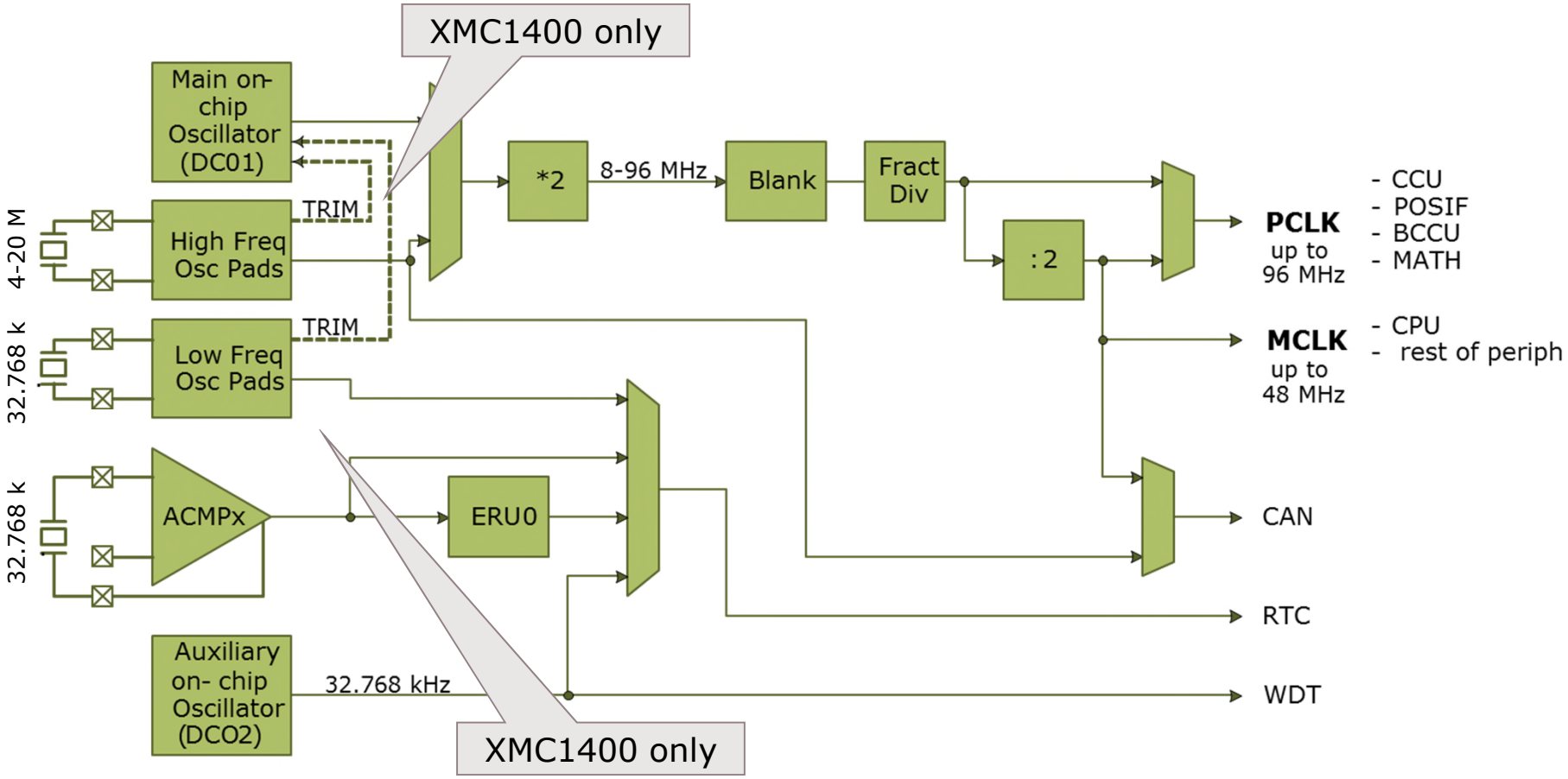
- Oscillator watchdog
- Individual peripheral clock gating
- Oscillator frequency calibration by hardware/software

Customer benefits

- Safely shut down system during loss of clock
- Optimized overall current consumption
- Improved clock accuracy

Clock
Clock generation

- Up to 96 MHz peripheral clock
- Up to 48 MHz CPU clock



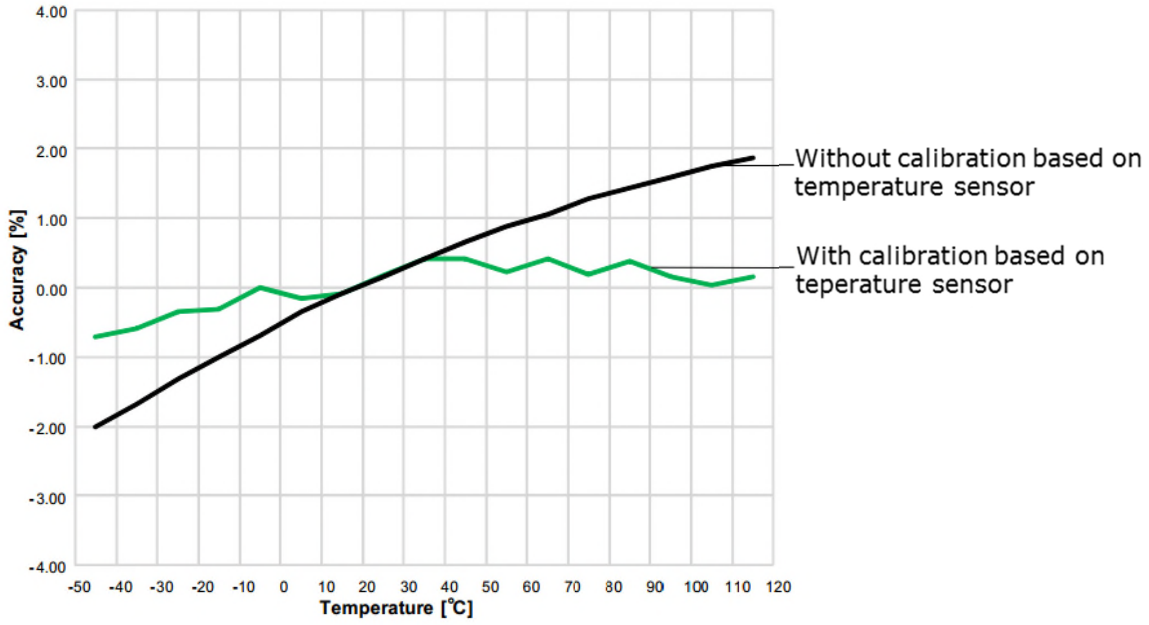
Clock
Oscillator frequency calibration (1/3)

- XMC1400 only
- **Accurate peripheral and main clock achieved by calibrating DCO1 with external crystal**
  - This is an automatic process

- Low-frequency pads (32.768 kHz)
  - RTC
  - Automatic DCO1 calibration
- High-frequency pads (4-20 MHz)
  - Direct jitter-free clock for CAN
  - Automatic DCO1 calibration

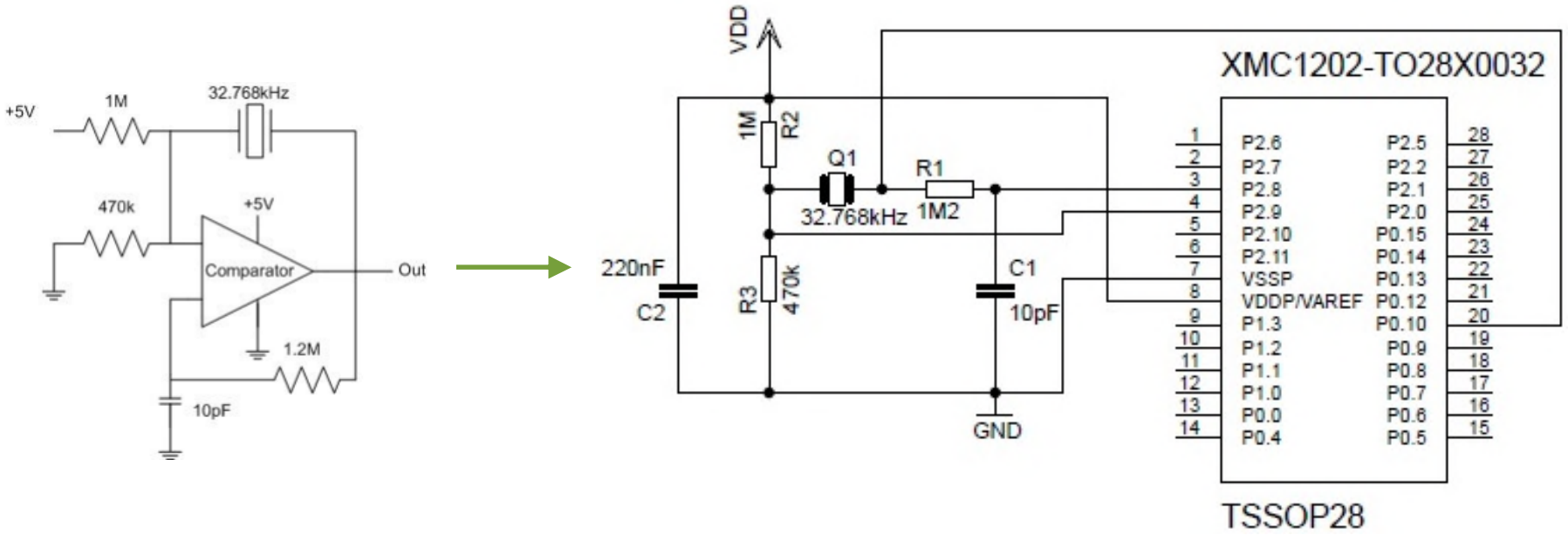
Clock
Oscillator frequency calibration (2/3)

- Software adjustment based on die temperature (DCO1)
  - Runtime calibration with on-chip die temperature sensor (DTS)
  - The offset is calculated using formulae and values stored in the flash configuration sector
  - Improved clock accuracy



Clock
Oscillator frequency calibration (3/3)

- Fractional divider adjustment based on external reference
  - External frequency captured by Capture Compare Unit 4 (CCU4)
  - Discrete oscillator circuit with on-chip comparator



Clock
Clock blanking (1/2)

- XMC1000 microcontrollers don't require a V_{DDC} buffer capacitor
- Stable core voltage during load changes is guaranteed by clock blanking
- During clock blanking, main clock (MCLK) and peripheral clock (PCLK) freeze for a few clock cycles to guarantee system stability and avoid brown-out reset

- Clock blanking may occur if there is a significant load increase (more than ~300 %)
  - Several peripherals are enabled at the same time (typically at startup)
  - Sudden significant increase in main and peripheral clock frequency (typically at startup)
  - Wakeup from deep sleep
  - Does not occur during normal runtime operation

Clock
Clock blanking (2/2)

- Clock blanking can be avoided if
  - Peripherals are enabled one at a time
  - Clock frequency is increased in steps (e.g. 2 MHz → 8 MHz → 32 MHz)
  - Clock frequency is decreased to 125 kHz and all peripherals are disabled before entering sleep
- If clock blanking happens
  - Wait 15 usec before increasing the load again to prevent further drop in the core voltage
    - Status bit CLKCR.V_{DDC}2LOW indicates stabilized core voltage
- Clock blanking can be monitored externally on P0.1

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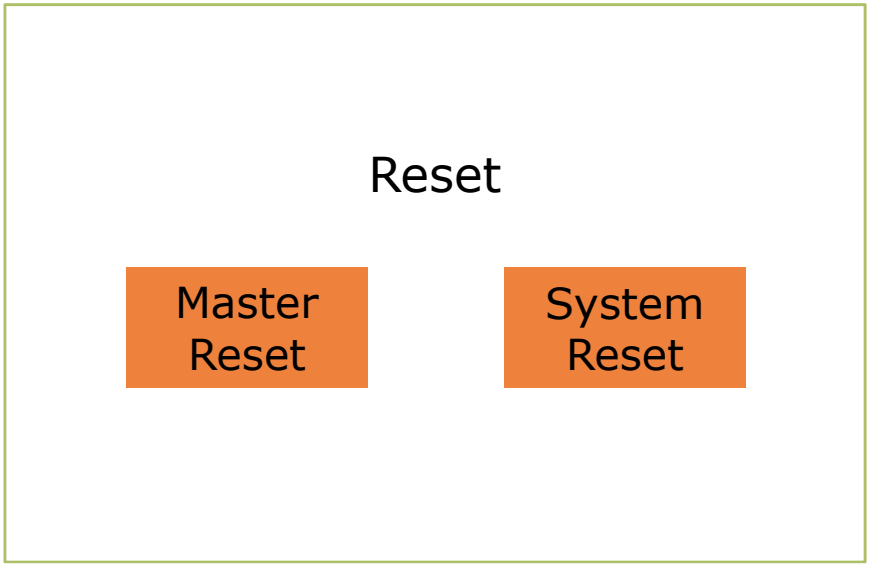
Reset



Highlights

Always ensure safe application state via on-chip reset generation.

Full user control via reset event signals and software control.

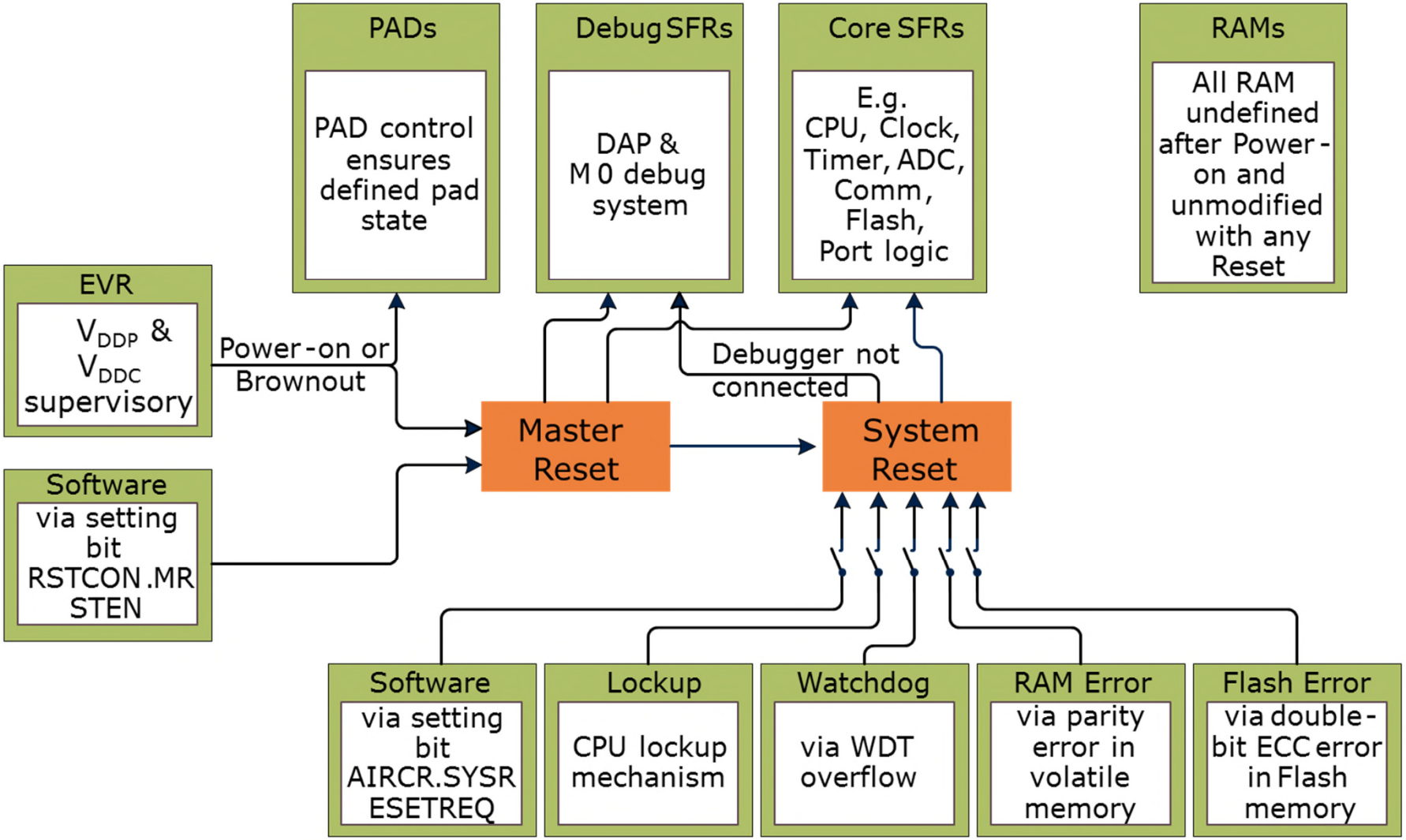
Key features

- Master reset
- Fail safe mechanisms

Customer benefits

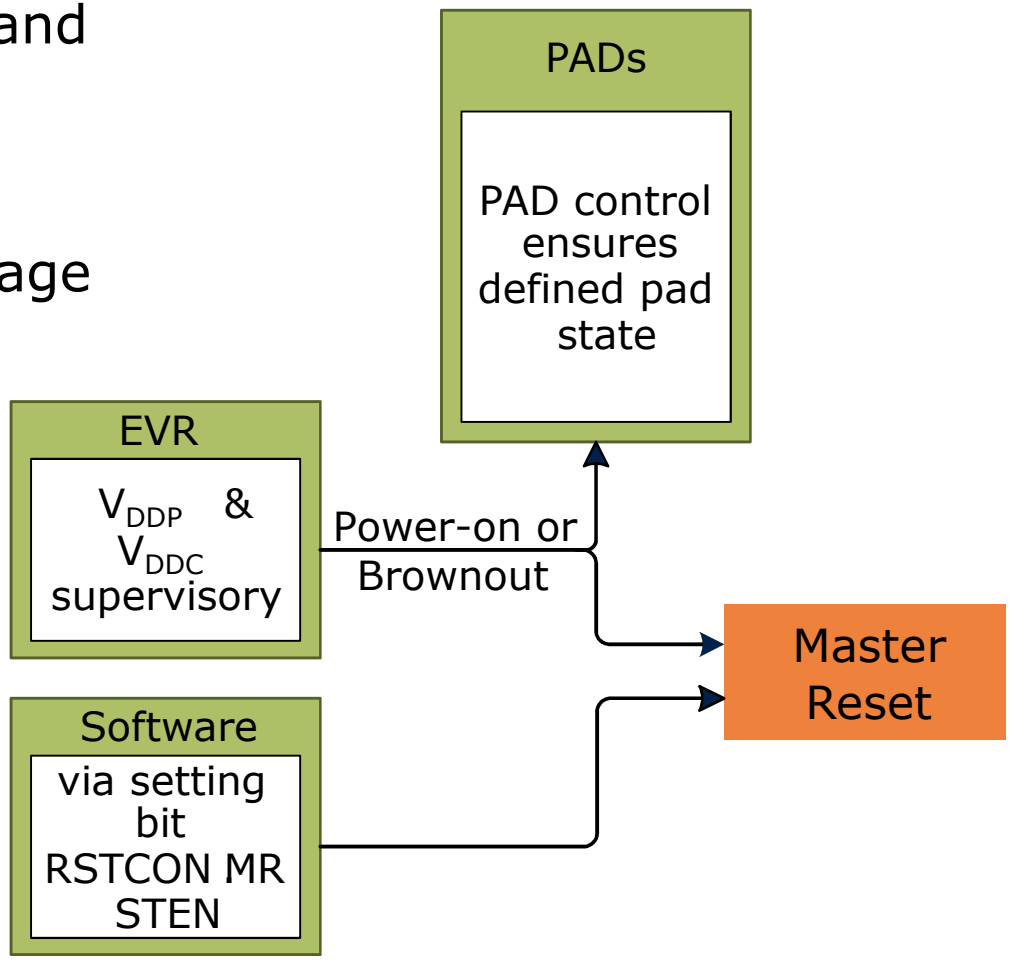
- Safe operating conditions and defined system state after power-on/brownout
- Reset brings the system into safe operation

Reset
Reset overview



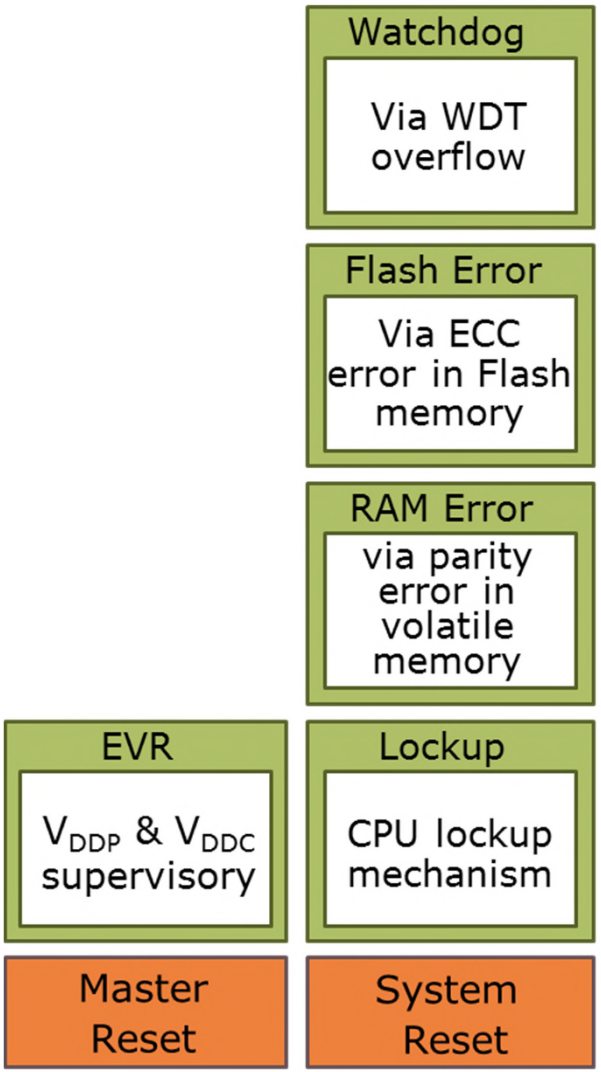
Reset
Master reset

- Supply voltage (1.8-5.5 V) and core voltage monitoring
  - Upon power-on
  - Upon V_{DDP}/V_{DDC} undervoltage (brownout)
- Or triggered by software
- Complete device reset



Reset
Fail safe mechanisms

- RAM parity error detection
  - Optional system reset in case of parity error
- Flash ECC error detection
  - Optional system reset in case of double-bit ECC error
- Lockup reset
  - Standard ARM® CPU feature
  - Optional reset in case of unrecoverable CPU states
- Watchdog timer reset
  - Watchdog reset generated if CPU is not responsive
  - Watchdog reset can be avoided with optional pre-warning
- V_{DDP} or V_{DDC} low pre-warning interrupts
  - Prepare system for clock blanking or imminent brownout reset



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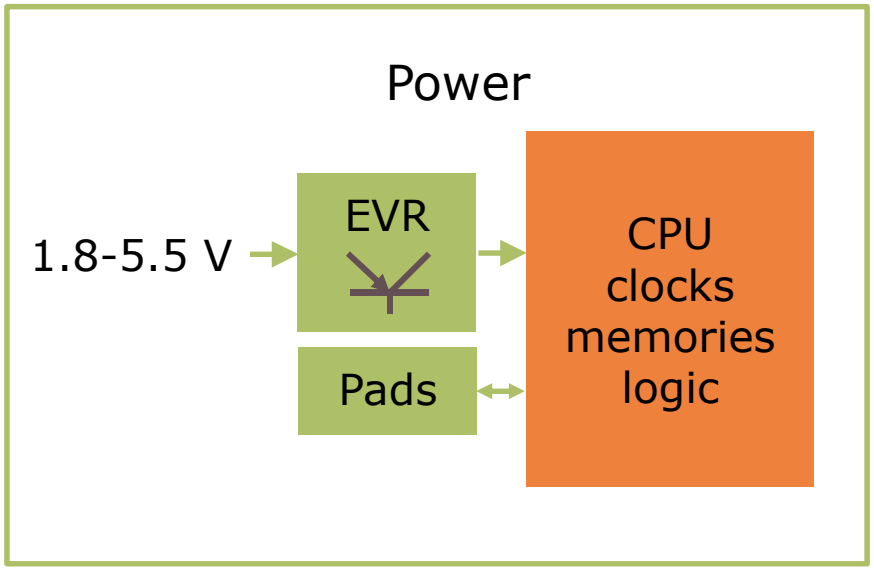


Highlights

A power supply of 1.8 V to 5.5 V is needed via the power supply pin pair (VDD, VSS).

The core supply for the CPU, memories and most of the peripherals is generated by the EVR.

Key features

- Different power saving modes
- Power monitoring and validation
- Very wide supply voltage range of 1.8-5.5 V

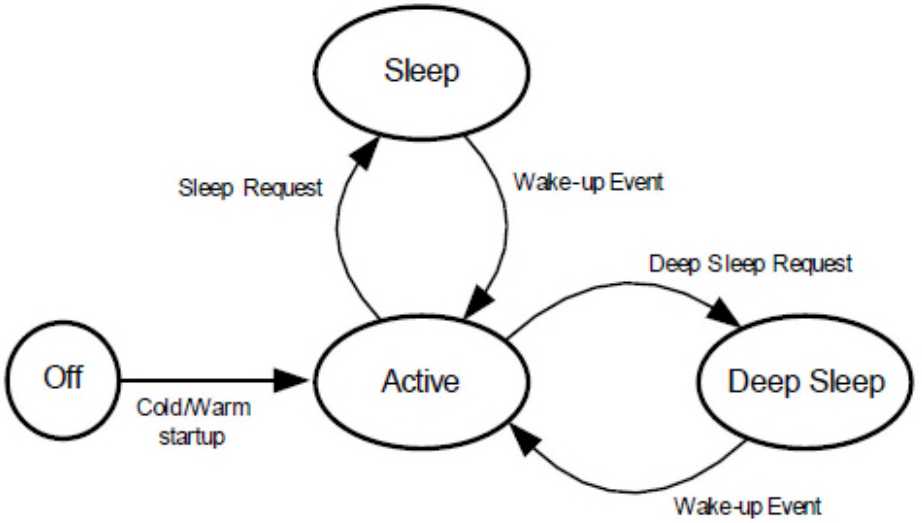
Customer benefits

- Scalable power consumption according to application use case
- Fail safe functionality
- Can be used in a wide range of designs with a wide range of components

Power
Different power saving modes (1/2)

Simple transition scheme

- Both power saving states entered from Active state
  - Active – Sleep
  - Active – Deep Sleep
- Power saving states entered with a single request
  - Sleep and Deep Sleep entered via CPU instruction
- Flexible Wake-up trigger
  - One wake-up trigger source can serve different power saving modes

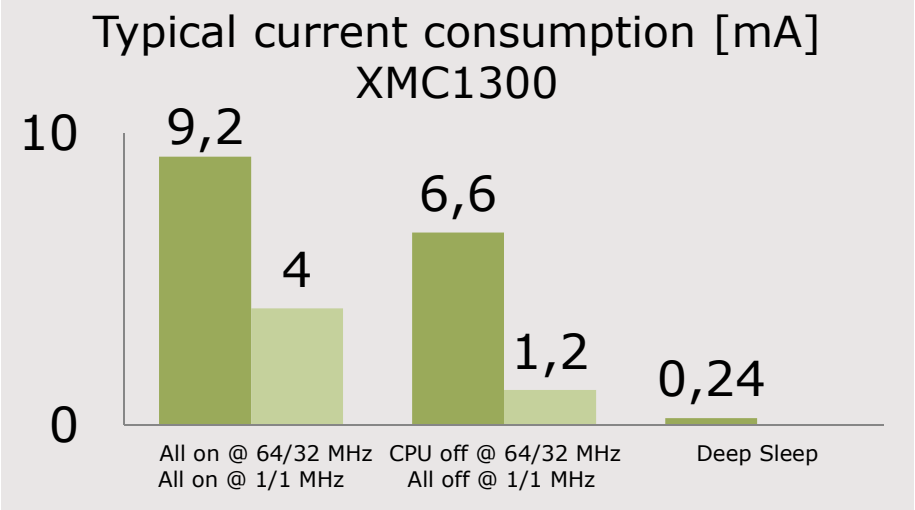


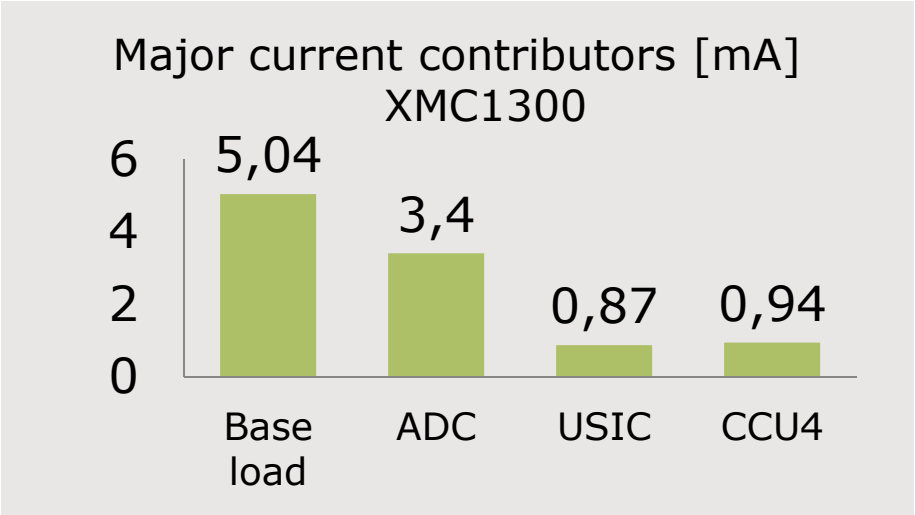
Mode	Power Saving	Recovery
Active	- Clock scaling - Disable selected peripherals by clock gating - Flash on/off	- Full SW control
Sleep	- CPU stopped	- Wakeup via interrupt - Automatic restoration
Deep Sleep	- CPU stopped - Main oscillator (DCO1) stopped	- Wakeup via interrupt - Automatic restoration

Power
Different power saving modes (2/2)

- Low active current
- Current consumption depends on clock frequency and enabled peripherals

XMC™ Family	Typical [mA]	Worst case [mA]
XMC1100	8.4	11
XMC1200	8.8	11.5
XMC1300	9.2	12
XMC1400	23	25

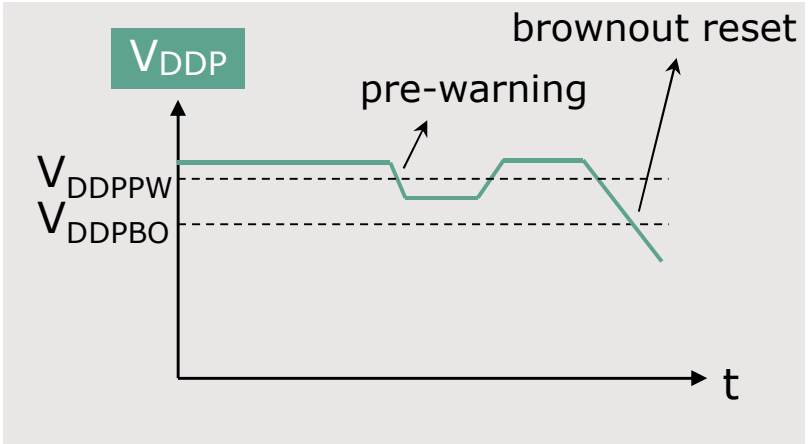


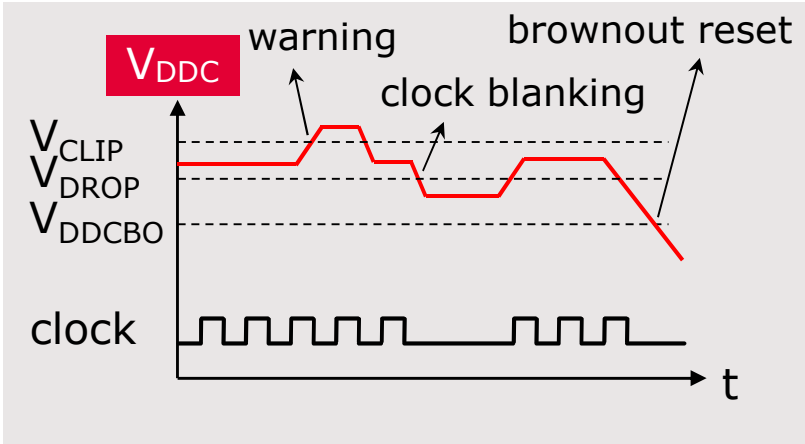


Power
Power monitoring and validation

- Pad domain power monitoring
  - Supply voltage V_{DDP}
  - Pre-warning when $V_{DDP} < V_{DDPPW}$
  - Brownout reset when $V_{DDP} < V_{DDPBO}$
- Core domain power validation
  - Core voltage V_{DDC}
  - Warning when $V_{DDC} > V_{CLIP}$
  - Warning & clock blanking when $V_{DDC} < V_{DROP}$
  - Brownout reset when $V_{DDC} < V_{DDCBO}$

Safe power up and down with automatic internal reset handling (release & issue)

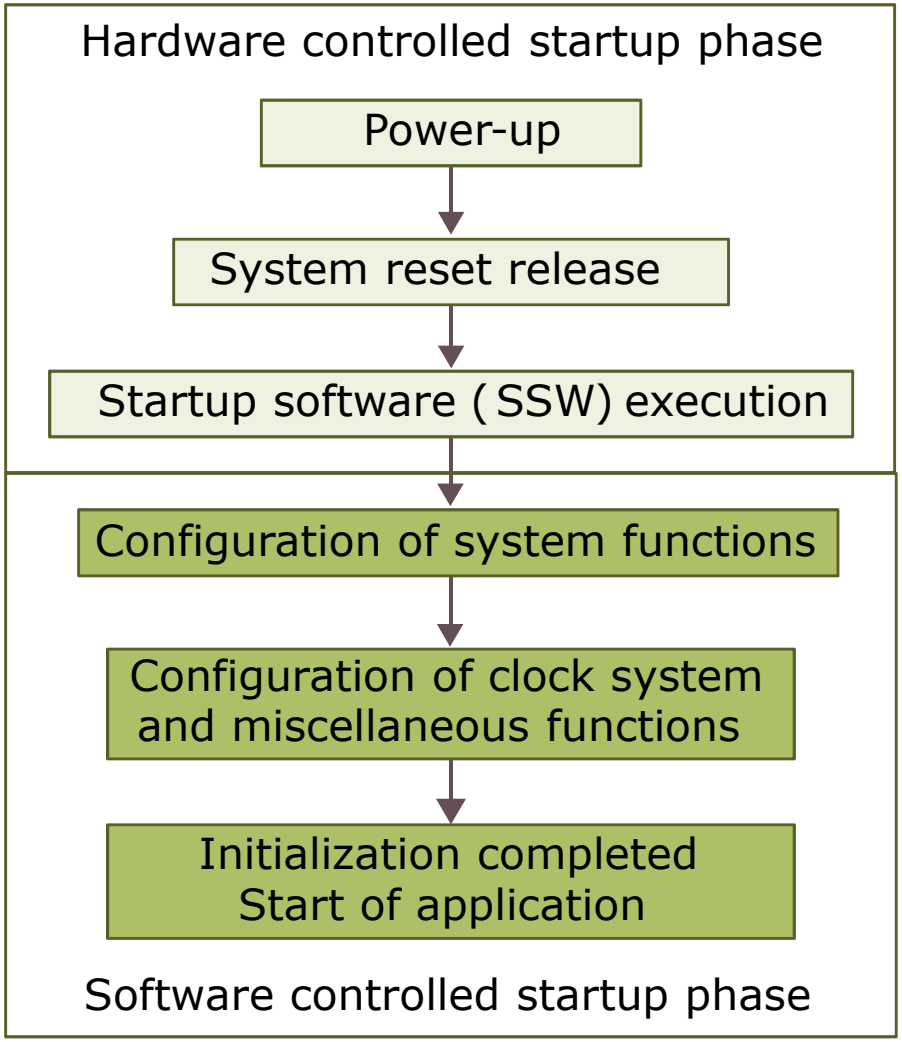




Power
Voltage detectors

- Supply Voltage (V_{DDP}) Monitoring
  - External voltage detector, V_{DEL}
  - External brownout detector, BDE
- Core voltage (V_{DDC}) Monitoring
  - V_{DDC} brownout detector
  - V_{DROP} detector
    - Monitor lower limits of the core voltage
  - V_{CLIP} detector
    - Monitor upper limits of the core voltage

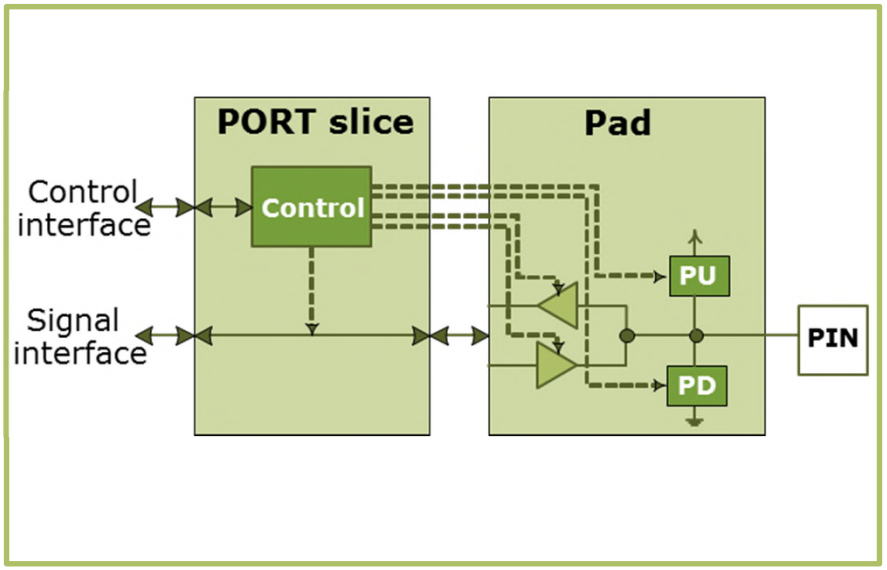
Power, reset and clock
Start-up sequence



Agenda

1. XMC1000 and ARM® Cortex®-M0
2. Memories
3. Bus system
4. Interrupt system
5. Clock
6. Reset
7. Power
8. Ports

Ports



Highlights

The Ports module provides a generic and flexible interface to the microcontroller.

Key features

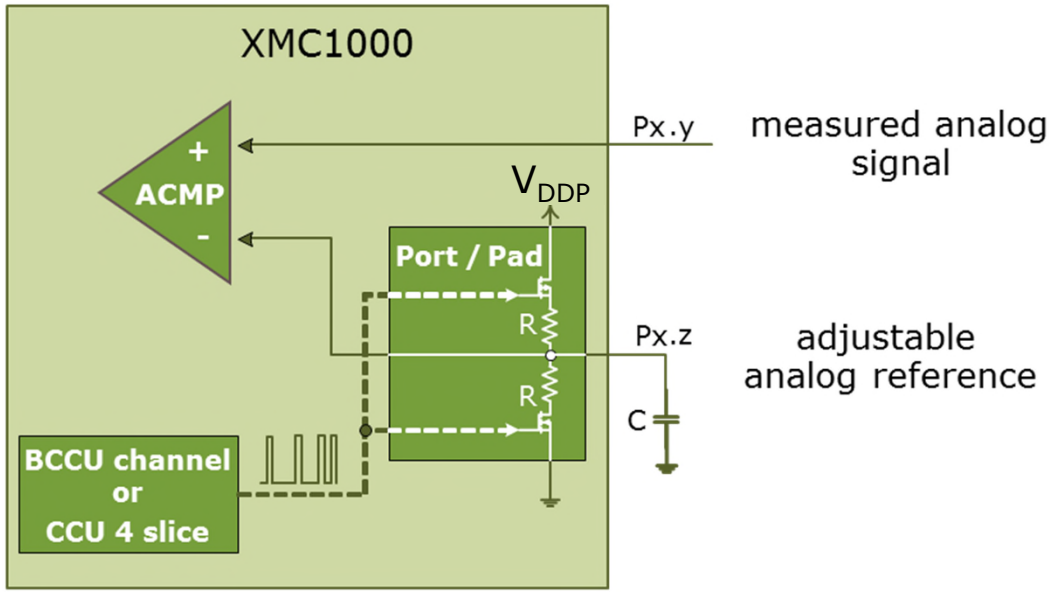
- Flexible function mapping
- High-current pins
- Very wide supply voltage range of 1.8-5.5 V

Customer benefits

- Up to 13 input / 11 output functions per pin, special functions (e.g. DAC)
- Driverless MOSFET switching, signaling LED control without external transistor
- Can be used in a wide range of designs with a wide range of components

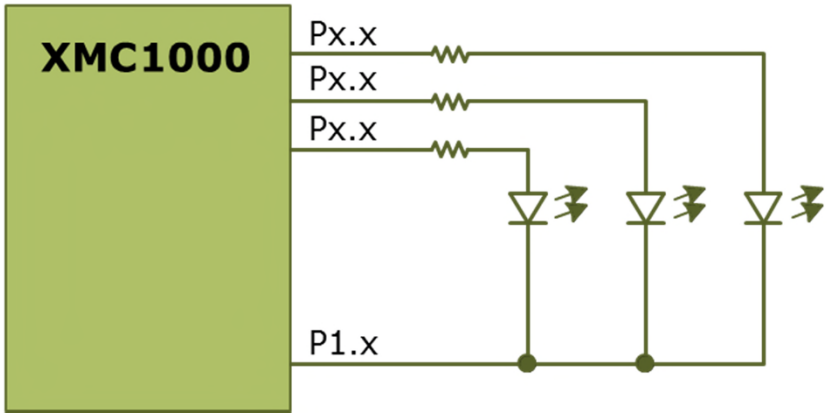
Ports
Flexible function mapping

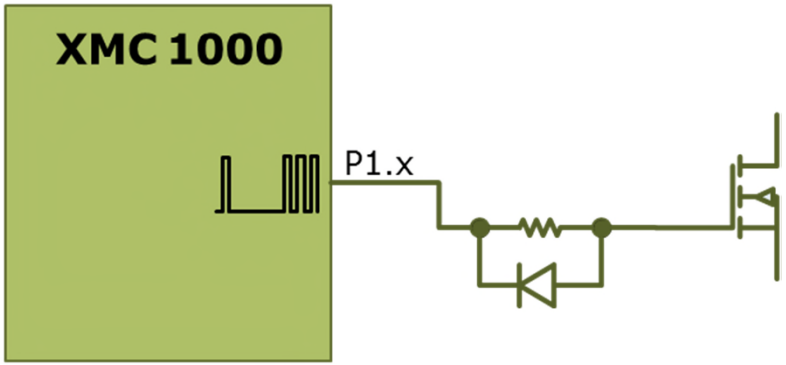
- Up to 12 input / 9 output functions per pin
- Adjustable pad properties
  - Input / output
  - Push-pull / open drain
  - Pull-up / pull-down / tristate
  - Power save
  - Adjustable pad hysteresis
- Direct control by peripherals
  - Analog reference generation by
    - pull-up/pull-down control
    - using a switching signal
  - Quad SPI functionality without
    - software overhead
  - LED matrix control without
    - software overhead



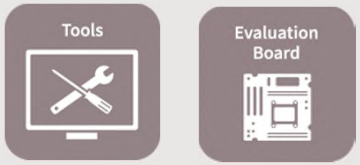
Ports
High-current pins

- Certain P1.x pins only
- Sink up to 50 mA
- Direct drive multiple LEDs in a common cathode configuration
- Fast MOSFET turn-off without external driver





Support material

Collaterals and brochures 	› Product briefs › Selection guides › Application brochures › Presentations › Press releases, ads	› www.infineon.com/XMC
Technical material 	› Application notes › Technical articles › Simulation models › Datasheets, MCDS files › PCB design data	› www.infineon.com/XMC › Kits and Boards › DAVE™ › Software and Tool Ecosystem
Videos 	› Technical videos › Product information Videos	› Infineon Media Center › XMC™ Mediathek
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