

Hibernate

XMC™ microcontrollers
September 2016



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Overview

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Key feature: real time clock and retention memory

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Key feature: low power analog comparator

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Key feature: flexible wake-up configuration

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Software view

Hibernate

RTC + alarm

Analog Wake-Up Input Detection

Digital Wake-Up Input Detection

Retention Memory

Highlights

XMC™4000 provides a very low power hibernate mode allowing power saving while real time keeping and system context retention in sixteen 32-bit registers, at current consumption below 10 μ A.

Key feature

- › Real time clock and retention memory
- › Low Power Analog Comparator (LPAC)
- › Flexible wake-up configuration

Customer benefits

- › Real time and context keeping while the rest of the system is powered off
- › Support for wake-up on analog event
- › Diversity of wake-up trigger options from external and internal sources

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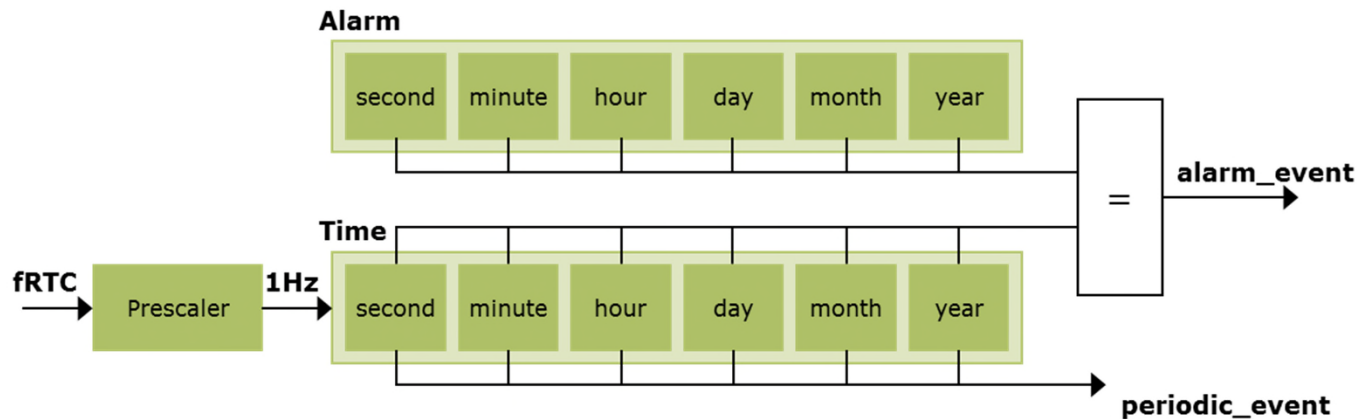
Software view

Hibernate

Real time clock and retention memory

› RTC features

- Clock and calendar function
- Generation of alarms and periodic events including wake-up events
- Time keeping during system power off



› 16 x 32-bit registers for data storage

- Context storage for wake-up from hibernate

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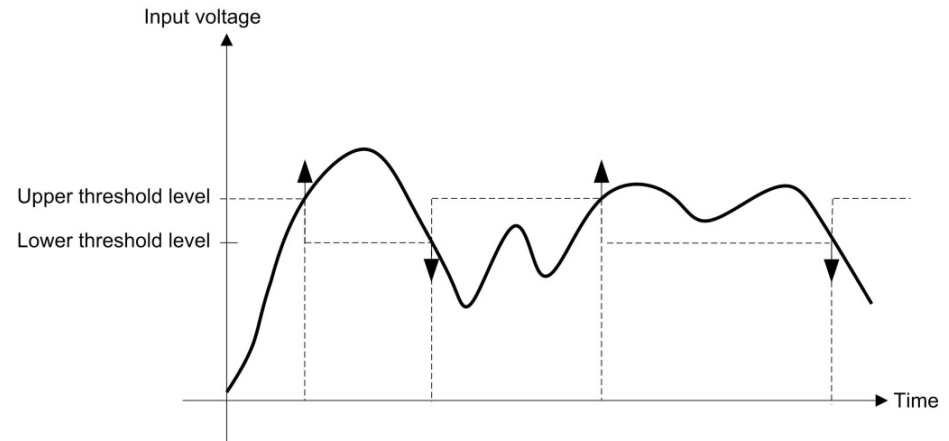
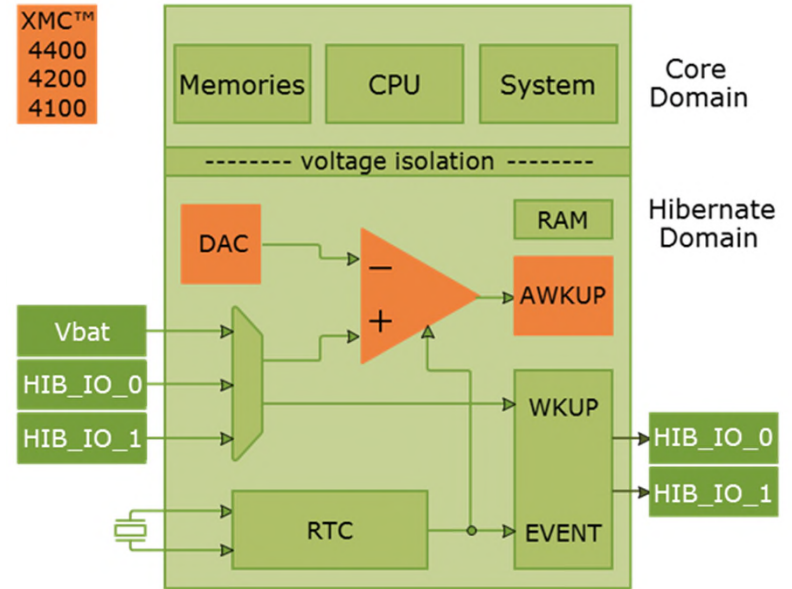
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Software view

Hibernate

Low power analog comparator (LPAC)

- › Supports wake-up from hibernate on analog events
- › 3 independent analog input channels: battery supply pin V_{BAT} , HIB_IO_0, HIB_IO_1
- › Compare triggered by RTC, digital HIB_IO event, software or continuous mode
- › Upper and lower threshold programmable with 6-bit resolution (64 level)



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Hibernate

Flexible wake-up configuration



- › Wake-up from hibernate on
 - Digital input signals at HIB_IO pins
 - RTC events
 - Single alarm
 - Periodic event
 - Low Power Analog Comparator (LPAC) event on the analog input signal
 - Analog sensor input
 - Threshold crossing on V_{BAT} pin

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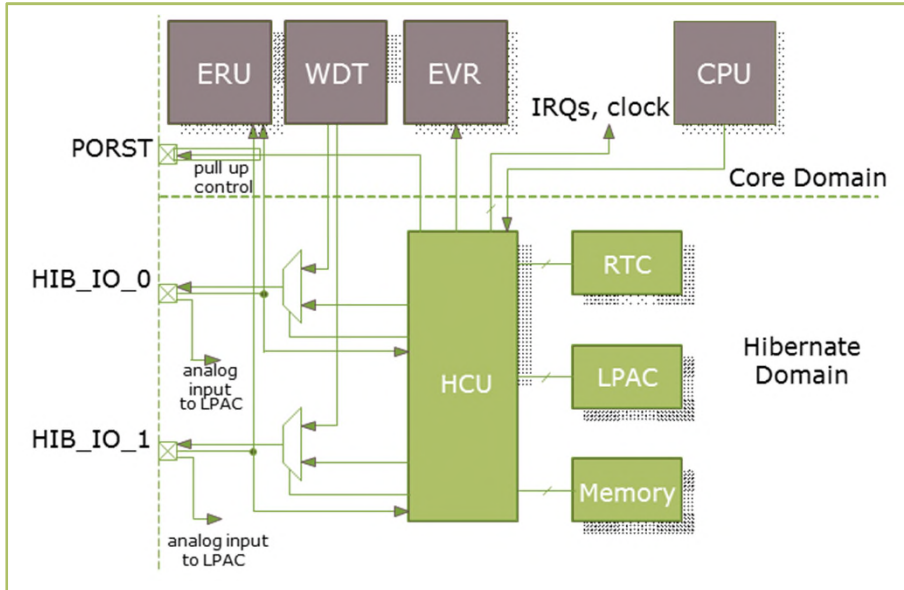
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Software view

Hibernate System integration



XMC™4500	XMC™4400	XMC™4200
●	●	●

LPAC module is available on XMC™4400 and XMC™4200 only.

The hibernate domain consists of several functional modules that can be used in hibernate mode and also in active mode.

User software can access hibernate domain registers and memory while in active mode.

- › Target applications
 - Human machine interface
 - General purpose

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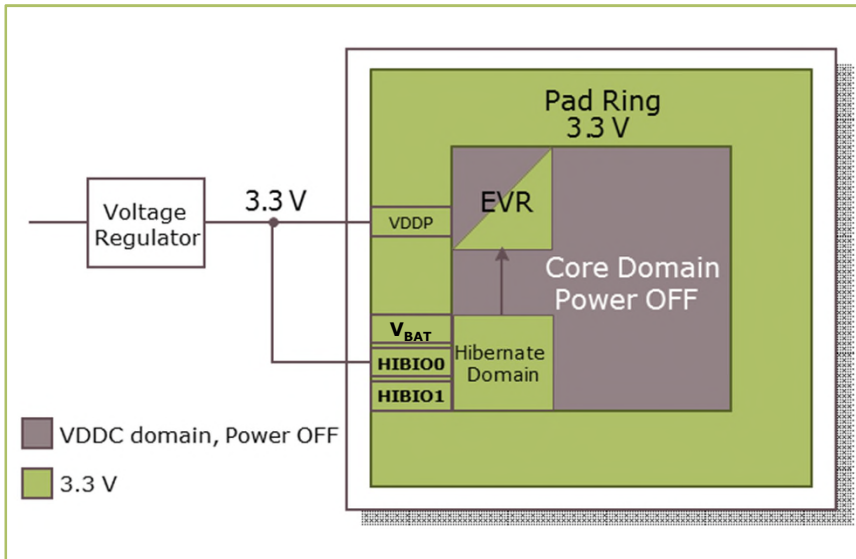
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Software view

Application example

Internally controlled hibernate mode



Overview

The main chip supply voltage is present during hibernate mode. Embedded voltage regulator (EVR) is controlled by hibernate domain. Core domain of the chip is powered off.

Current consumption of $\sim 25 \mu\text{A}$ can be achieved while RTC is active.

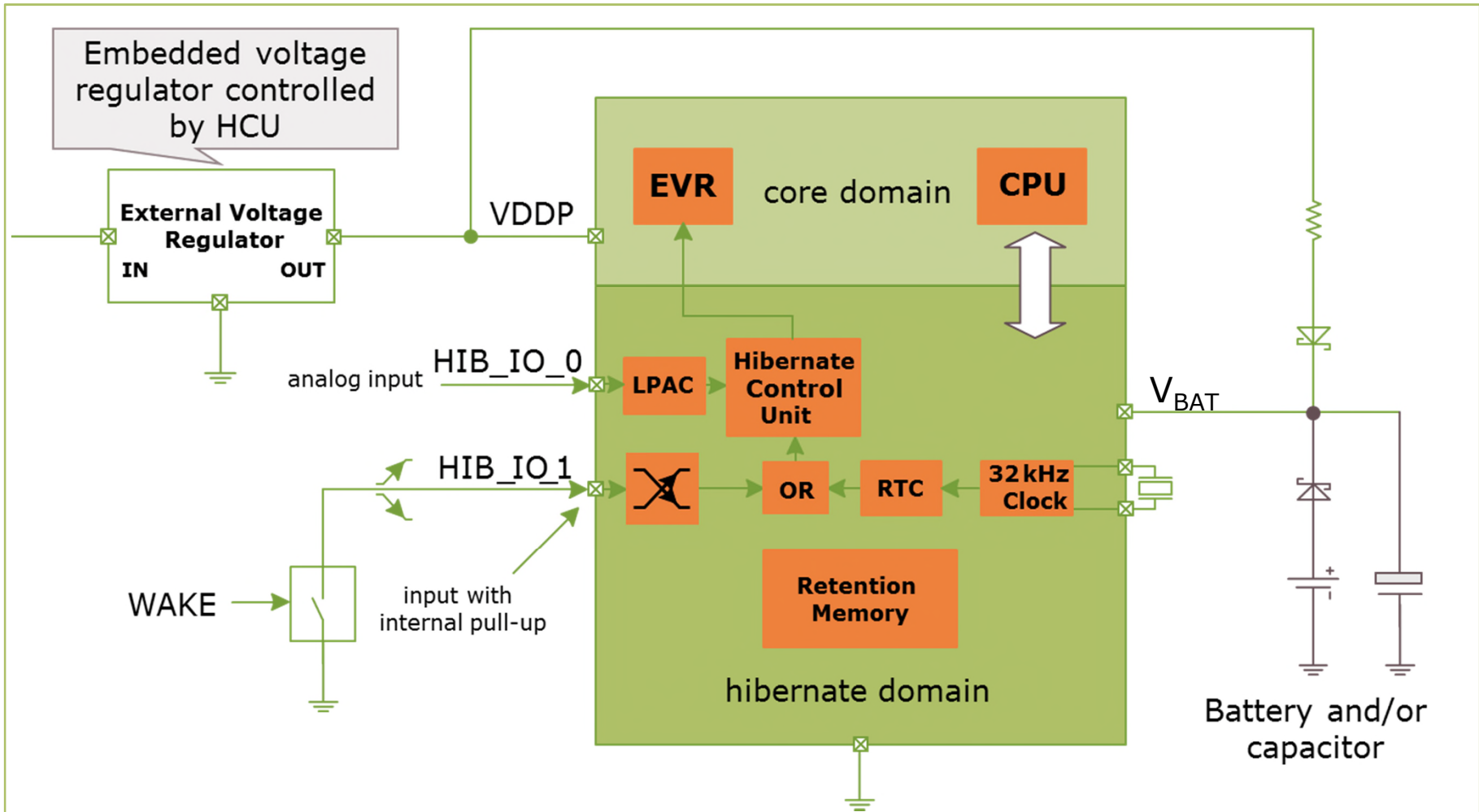
In brief

The lowest BoM. Valid supply voltage present while in hibernate mode.

Supported on XMC™4400 and XMC™4200 only.

Application example

Internally controlled hibernate mode



Application example – Internally controlled hibernate mode: detailed block diagram