GPDMA
General Purposes DMA

XMC™ microcontrollers
September 2016

Agenda

1. Overview
2. Key feature: multi-block transfers through linked list
3. Key feature: scatter or gather transfer mode
4. Key feature: software or hardware triggered DMA
5. System integration
6. Application example

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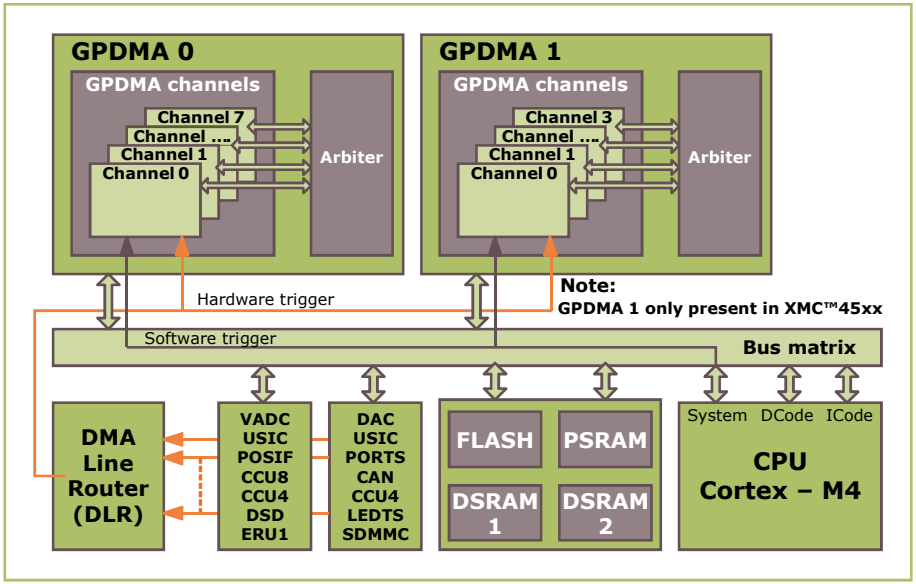

Highlights

The GPDMA is a highly configurable DMA controller, that allows low latency data transfers between peripherals and memories. Complex data transfers can be done with minimal intervention of the processor, keeping this way the CPU resources free for other operations. DMA line router also provides flexible peripheral connection to different DMA channels.

Key feature

- Multi-block transfers achieved through linked list
- Scatter or gather transfer mode
- Software or hardware triggered DMA

Customer benefits

- Can achieve greater flexibility for complex data transfer from source to destination
- Source or destination address increment or decrement and address offset
- Hardware trigger allows integrated system solution with minimal CPU loading

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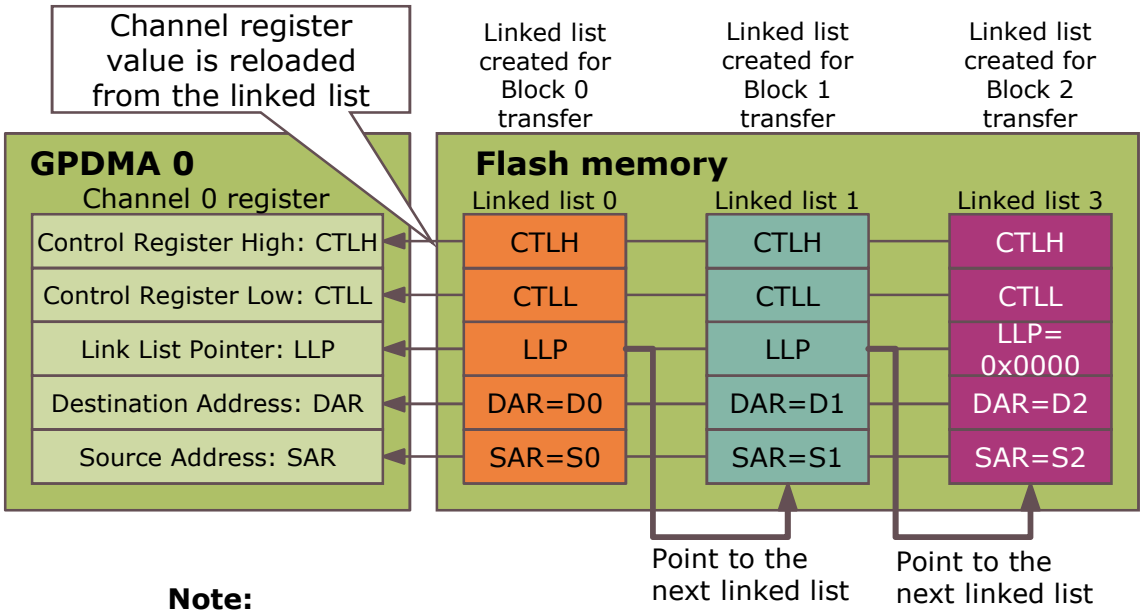
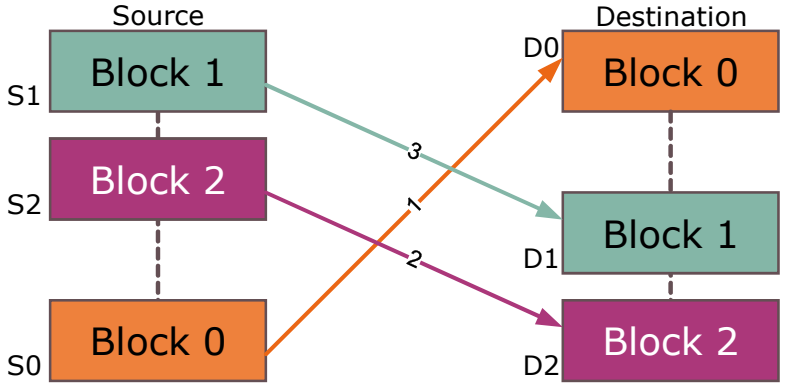
GPDMA: Multi-block transfers achieved through linked list

- The linked list method offers greater flexibility for source and destination address control during multi block transfer
- The GPDMA reprograms the channel registers prior to the start of each block by fetching the linked list for that block from system memory
- GPDMA block chaining uses a **Linked List Pointer register (LLP)** that stores the address in memory of the next linked list item



Note:
S0, S1, S2 are the base address for source
D0, D1, D2 are the base address for destination



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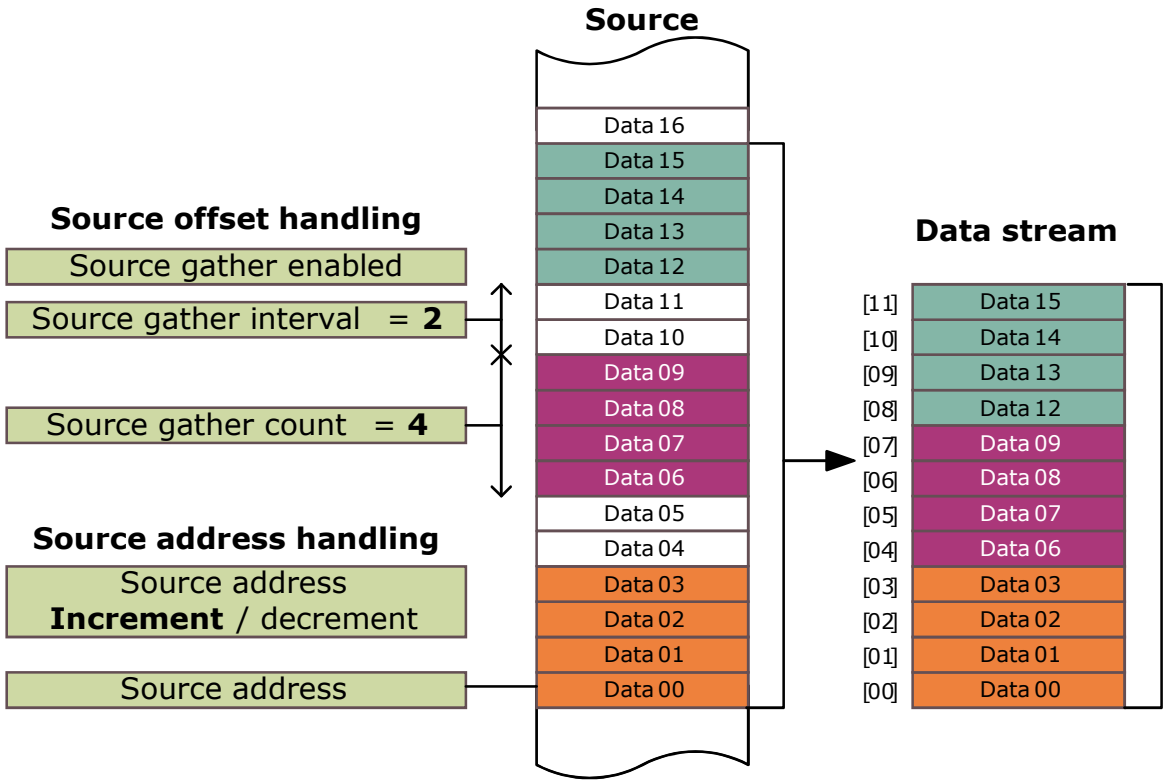
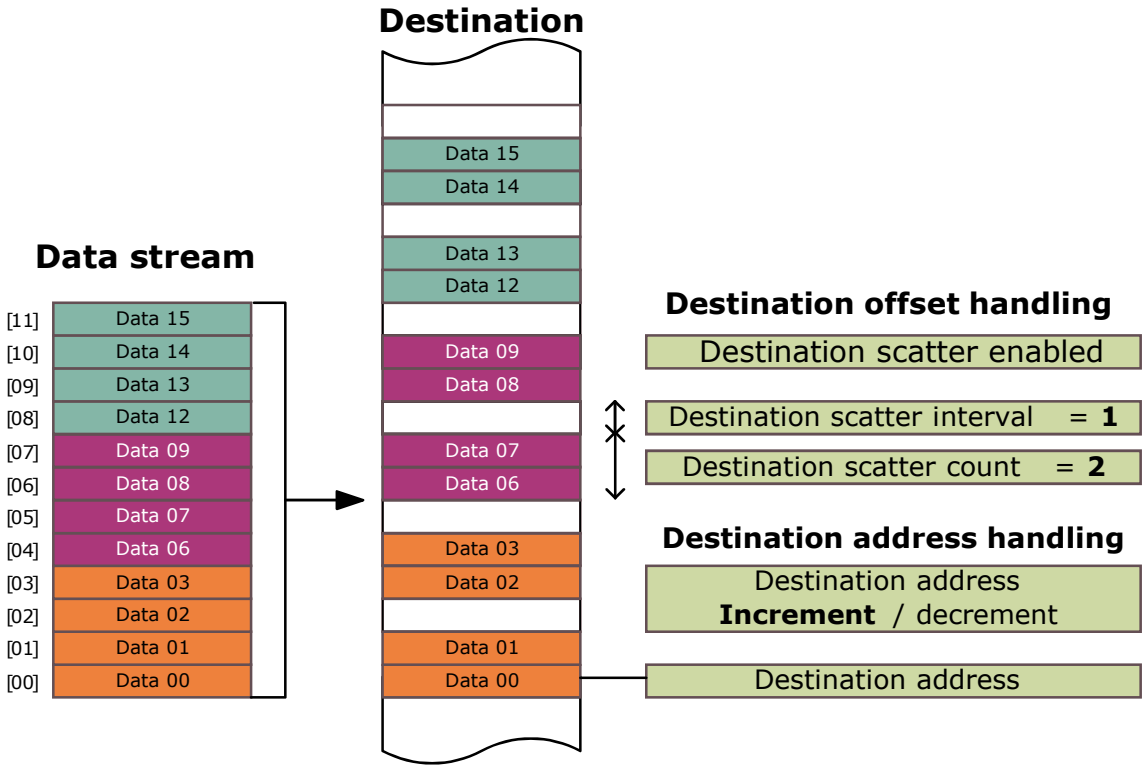
GPDMA
Scatter or gather transfer mode (1/2)



- To perform a source address offset within a transfer block, we can make use of the **gather transfer mode**
- The source address is incremented or decremented by a programmed amount (source gather interval) when a gather boundary (source gather count) is reached

GPDMA
Scatter or gather transfer mode (2/2)



- To perform a destination address offset within a transfer block, we can make use of the **scatter transfer mode**
- The destination address is incremented or decremented by a programmed amount (destination scatter interval) when a scatter boundary (destination scatter count) is reached

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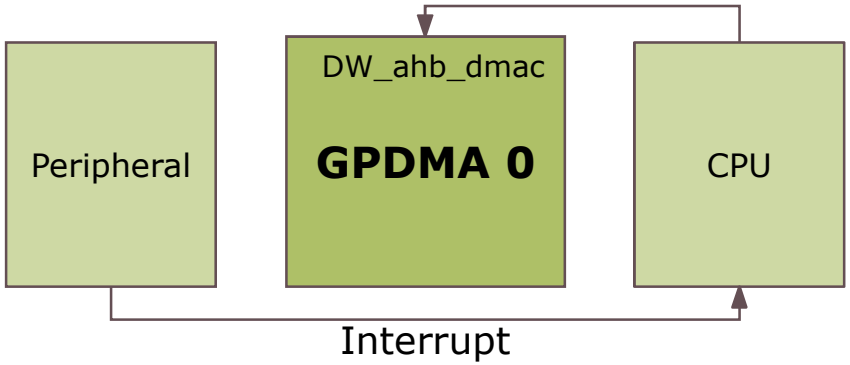
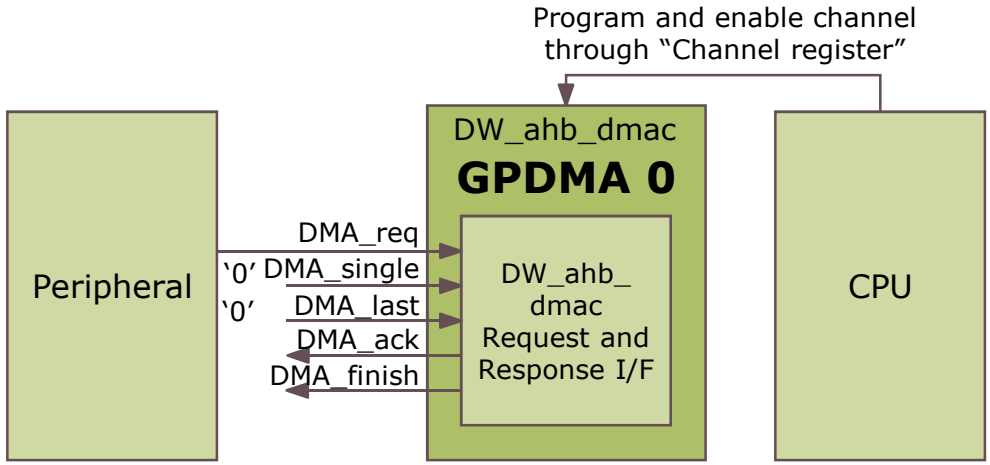
GPDMA
Software or hardware triggered DMA

- **Software controlled transfers** or synchronous transfers, when the peripheral requires to perform a DMA transaction triggers an interrupt. The interrupt service routine makes use of the software handshaking registers to initiate and control the DMA transaction acting as flow controller



- **Hardware triggered transfers** or asynchronous transfers make use of the service request signals of the peripheral to initiate the DMA transaction. DMA acts as flow controller



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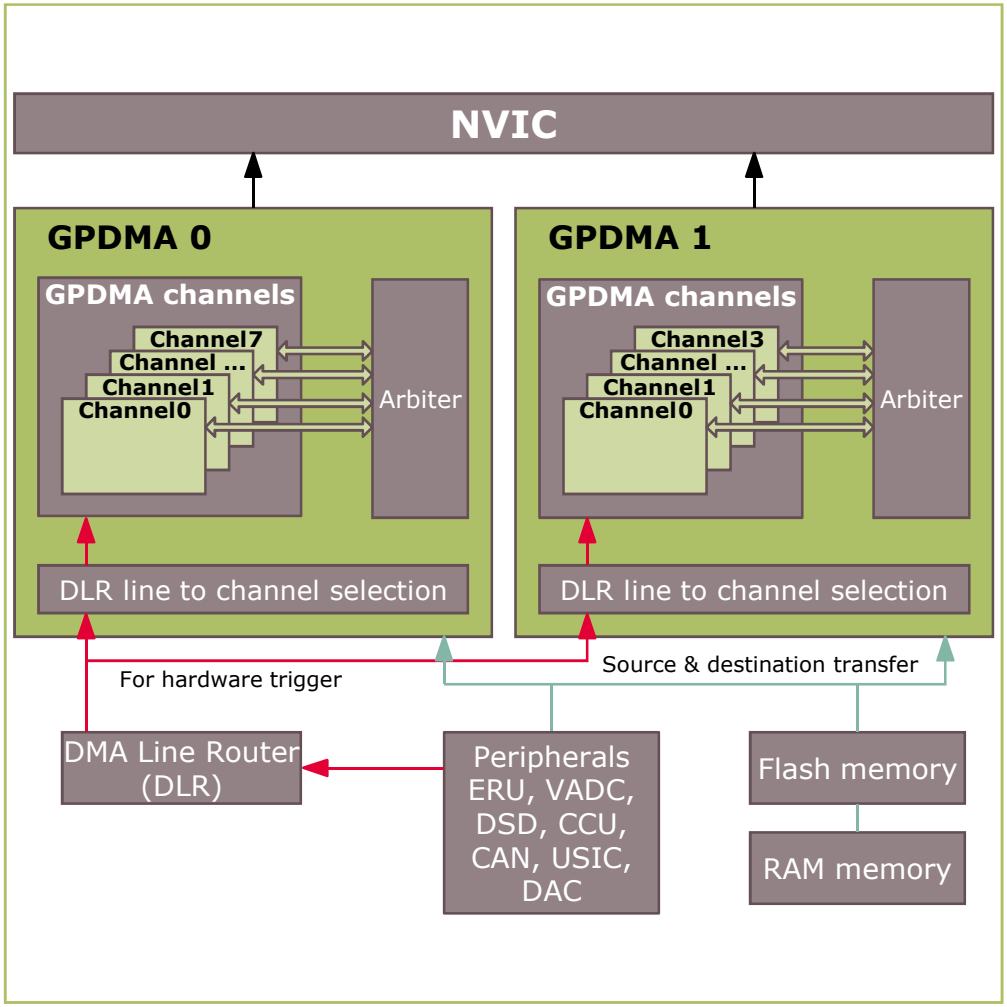

XMC™4500	XMC™4400	XMC™4200
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- The DMA can be triggered by the peripherals through the DMA line router
- DMA transfer is available for memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- DMA service can be generated for each channel due to DMA activity:
  - Source transaction complete
  - Destination transaction complete
  - Block transfer complete
  - DMA transfer complete
  - Error

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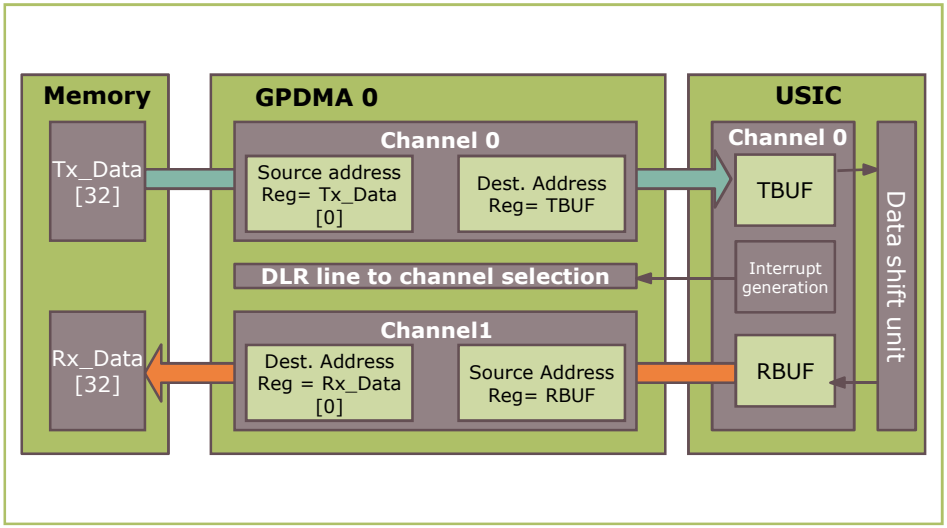
Application example
Integrated solution for data transfer



In brief

For communication, there is always a need to rely on software to copy data from memory to a transmit buffer or from a receive buffer to a memory area.

However this software copy process can be replaced by DMA transfer with hardware trigger, hence reducing the CPU loading.

Overview

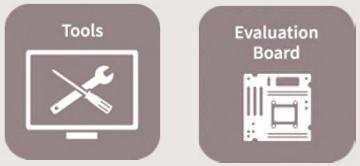
Memory to peripheral

During transmission, with every byte of data being transmitted by the USIC will actually trigger the DMA to fetch the next byte of data from the memory and move to USIC TBUF.

Peripheral to memory

For receiving, when the UART had received a data, the DMA is triggered for a data transfer from the USIC RBUF to a designated memory buffer.

Support material

Collaterals and Brochures 	– Product Briefs – Selection Guides – Application Brochures – Presentations – Press Releases, Ads	– www.infineon.com/XMC
Technical Material 	– Application Notes – Technical Articles – Simulation Models – Datasheets, MCDS Files – PCB Design Data	– www.infineon.com/XMC – Kits and Boards – DAVE™ – Software and Tool Ecosystem
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