EBU
External Bus Unit

XMC™ microcontrollers
September 2016

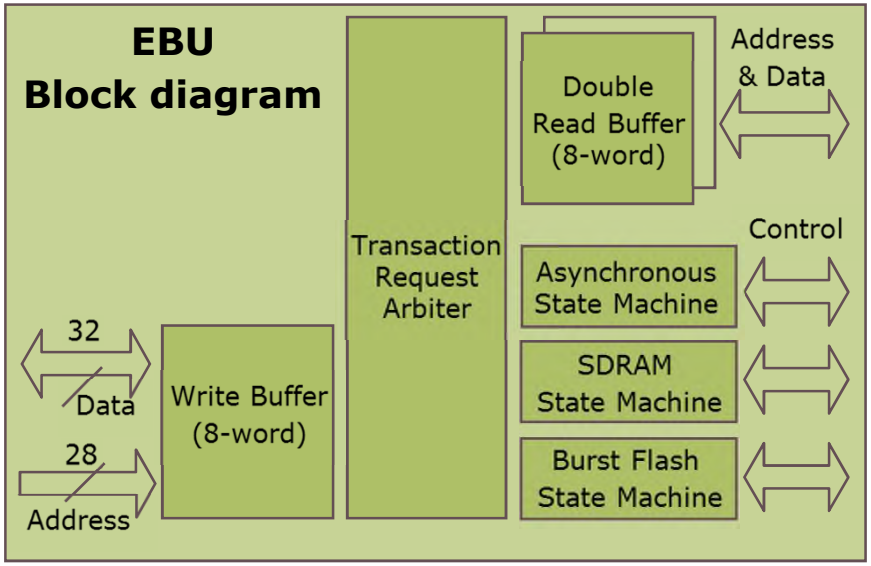
Agenda

1. Overview
2. Key feature: multiple memory type access
3. Key feature: flexible bus protocol parameterization
4. Key feature: external code execution and data access
5. System integration
6. Application examples

Agenda

1. Overview
2. Key feature: multiple memory type access
3. Key feature: flexible bus protocol parameterization
4. Key feature: external code execution and data access
5. System integration
6. Application examples

EBU
External Bus Unit



Highlights

Transparently connects CPU and GPDMA controller to external devices such as memories, LCDs, ASICs or FPGAs.
Both code execution and data storage is possible.
Several types of external memories are supported.

Key feature

- Multiple memory type access in time-multiplex
- Highly flexible bus protocol parameterization
- External code execution and data access

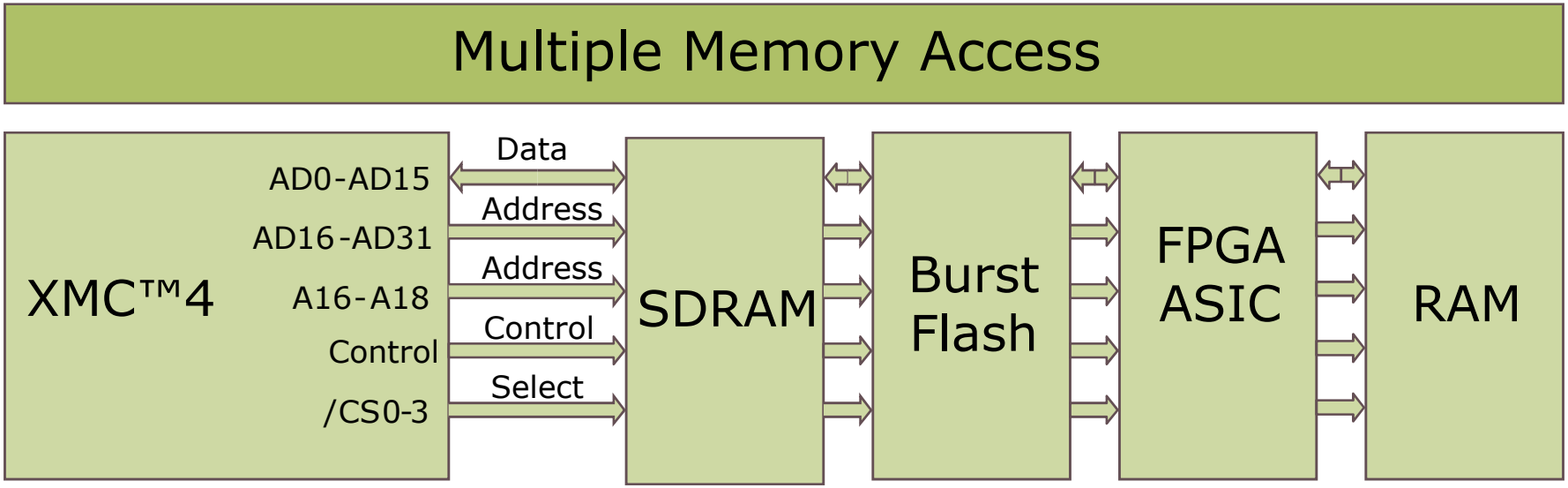
Customer benefits

- Solve complex applications with low footprint package (BGA144)
- Select memory extension with the best price/performance/quality ratio
- Enable huge protocol stacks and process data image storage

Agenda

1. Overview
2. Key feature: multiple memory type access
3. Key feature: flexible bus protocol parameterization
4. Key feature: external code execution and data access
5. System integration
6. Application examples

EBU: multiple memory type access in time-multiplex (1/3)



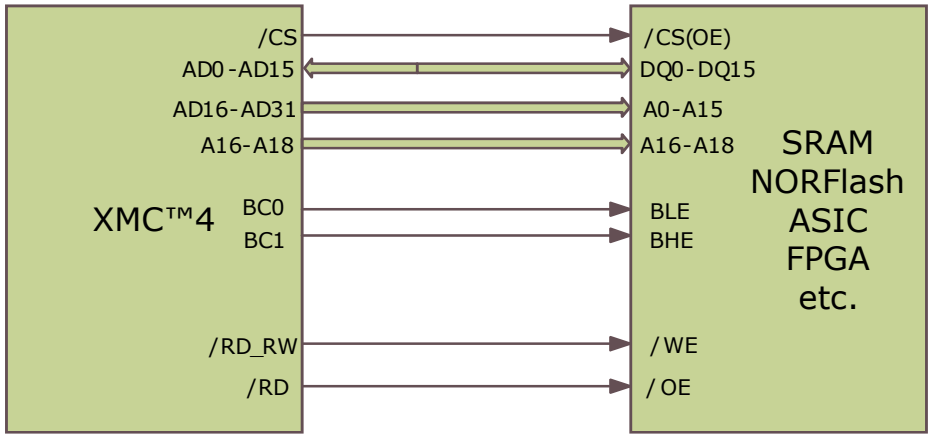
- EBU supports parallel operation of synchronous, asynchronous and burst protocols in one bus
- Up to four chip-selects available
- This allows low footprint package (e.g. BGA144) for complex applications

EBU: multiple memory type access in time-multiplex (2/3)

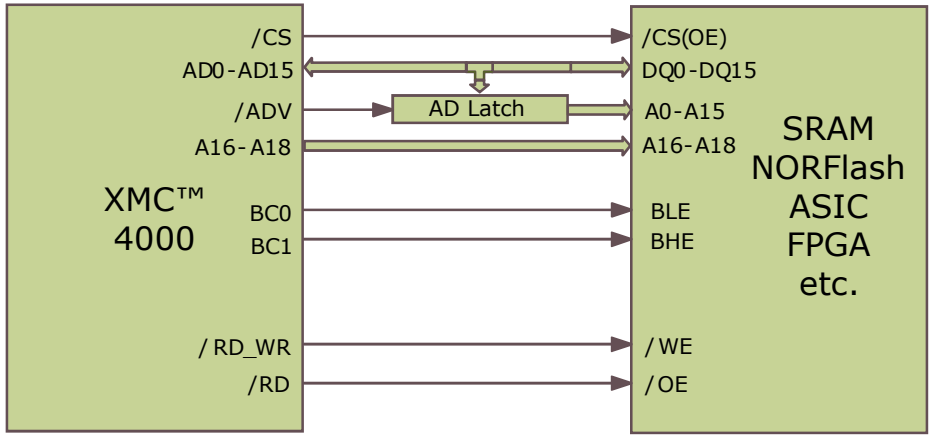
- Modes (Intel-style peripheral/device support)
  - 16-bit multiplexed or
  - 16-bit de-multiplexed or
  - 32-bit multiplexed
  - Up to 64 MB address range

- SRAM
  - E.g. *ISSY IS61WV series*
- NOR Flash
  - E.g. *Micron M29EW series*
- ASIC
  - E.g. *Beckhoff ET1100*
- FPGA
  - E.g. *Altera Cyclone IV/V*

Asynchronous access – 16-bit demultiplexed

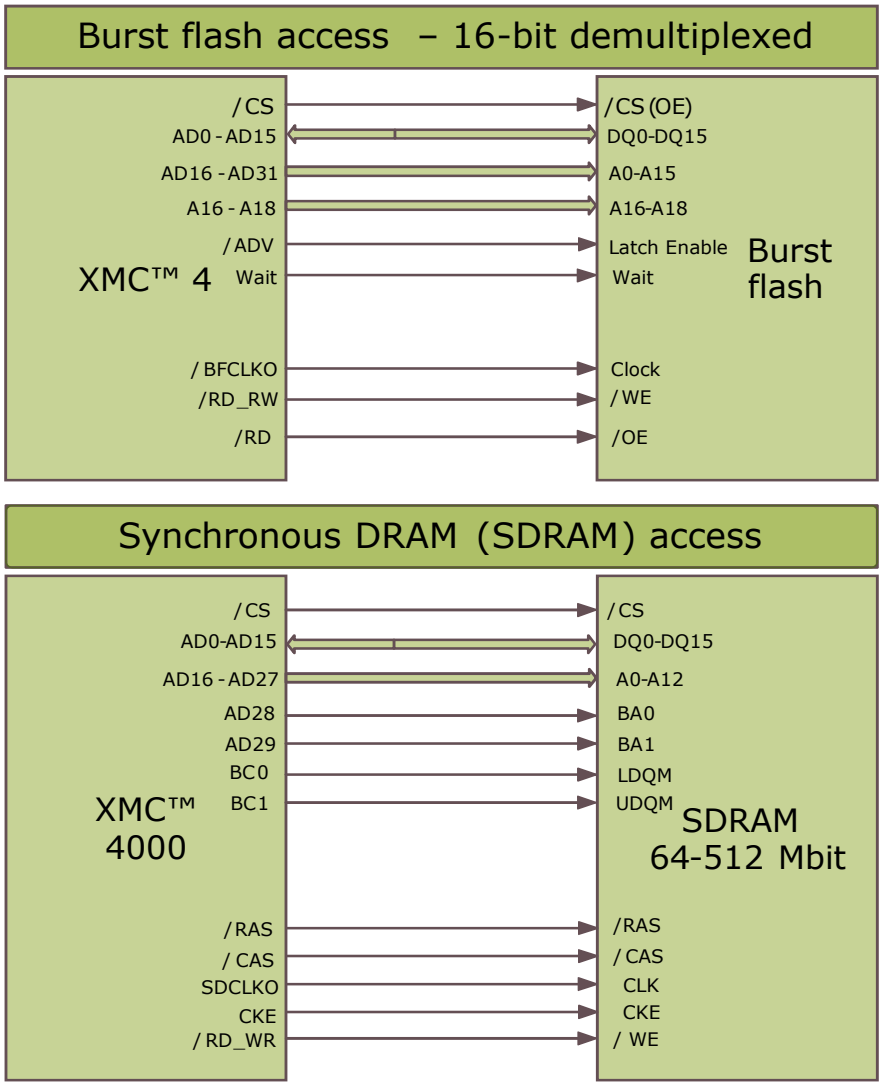


Asynchronous access – 16-bit multiplexed



EBU: multiple memory type access in time-multiplex (3/3)

- Burst flash
  - Up to 256 Mbit
  - E.g. *Spansion S29CL032J*
- Synchronous RAM
  - E.g. *ISSY IS61LF series*
- SDRAM
  - 64-512 Mbit
- E. g. *Micron MT48L series, ISSI IS42/45S series*



Agenda

1. Overview
2. Key feature: multiple memory type access
3. Key feature: flexible bus protocol parameterization
4. Key feature: external code execution and data access
5. System integration
6. Application examples

EBU
Highly flexible bus protocol parameterization

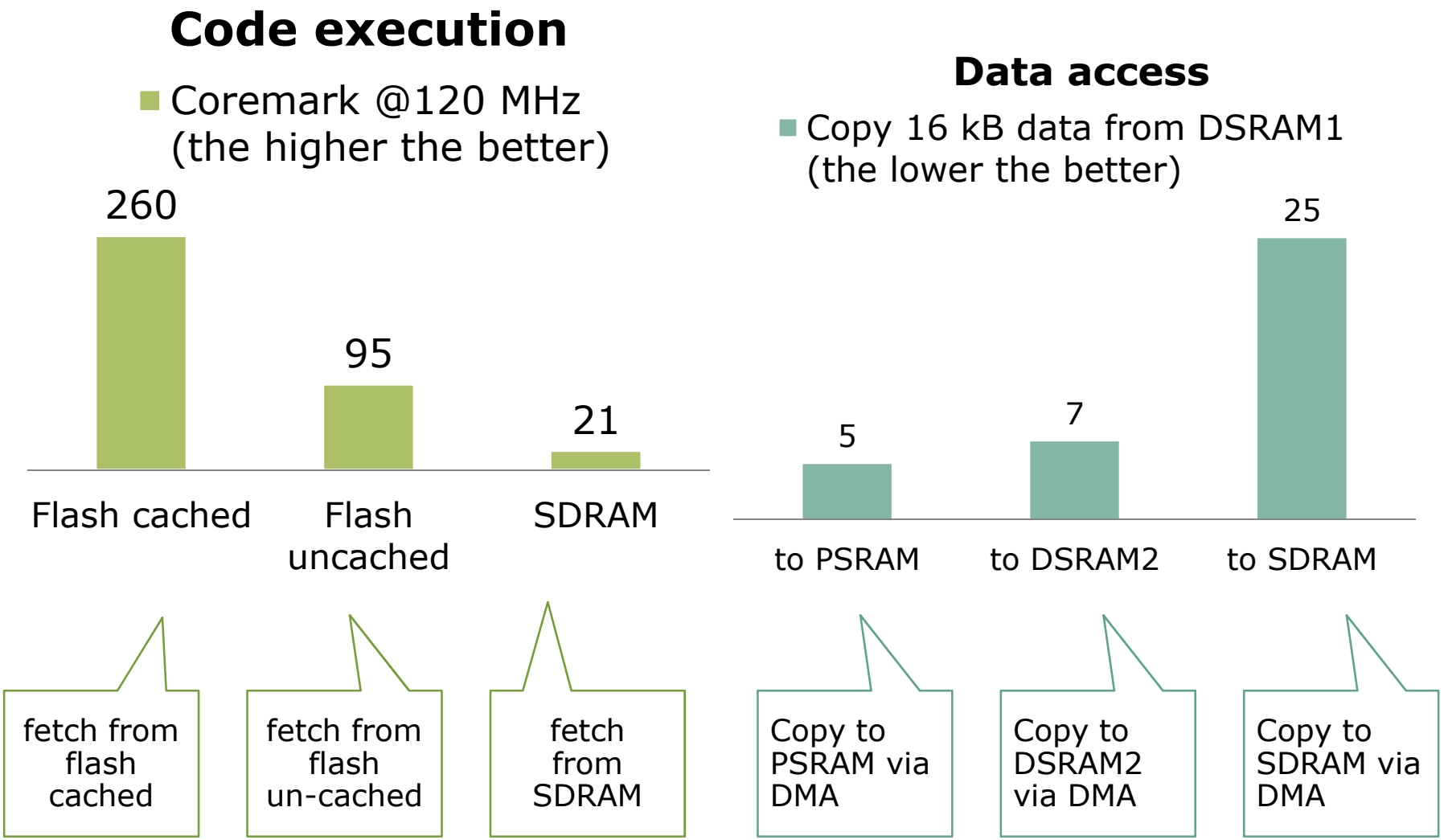
- EBU supports different memory protocols
  - Up to 4 chip selects available assigned to four programmable address regions
  - Highly programmable timing parameters for each memory type
  - Bus arbitration scheme supported
- Adjustable clock ratio CPU:Memory
  - SDRAM: 1:1, 1:2, 1:3
  - Asynchronous: 1:1, 1:2, 1:3, 1:4
- Up to 80 MHz bus timing on A2-type pads
  - CPU@120 MHz → memory@60 MHz
  - CPU@80 MHz → memory@80 MHz

- Setup
- Hold
- Multiplex
- Demutiplex
- Burst
- Synchronous
- Asynchronous
- Wait
- Hold
- Acknowledge
- Busrequest
- Chipselect
- Waitstate
- Clock
- …

Agenda

1. Overview
2. Key feature: multiple memory type access
3. Key feature: flexible bus protocol parameterization
4. Key feature: external code execution and data access
5. System integration
6. Application examples

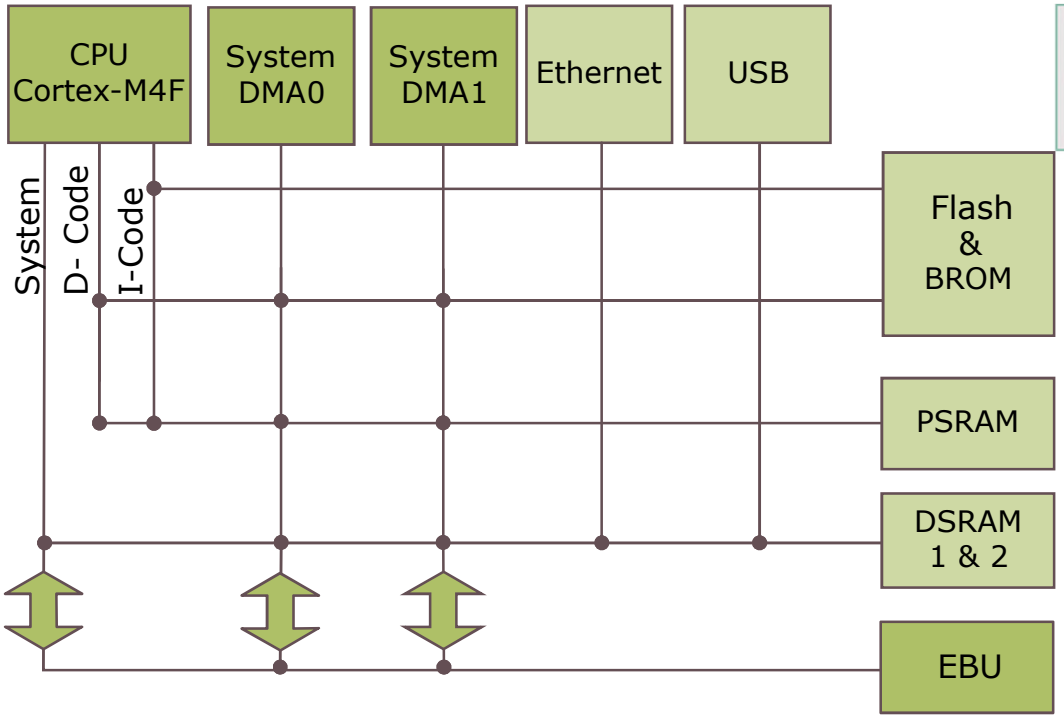
EBU
External code execution and data access

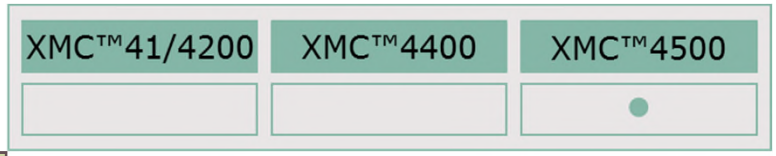


Agenda

1. Overview
2. Key feature: multiple memory type access
3. Key feature: flexible bus protocol parameterization
4. Key feature: external code execution and data access
5. System integration
6. Application examples

EBU
System integration





CPU and both DMAs can access external memories or devices via EBU.

Due to the multilayer bus matrix, CPU can fetch code from internal flash while a DMA fetches data from external memory without timing penalty.

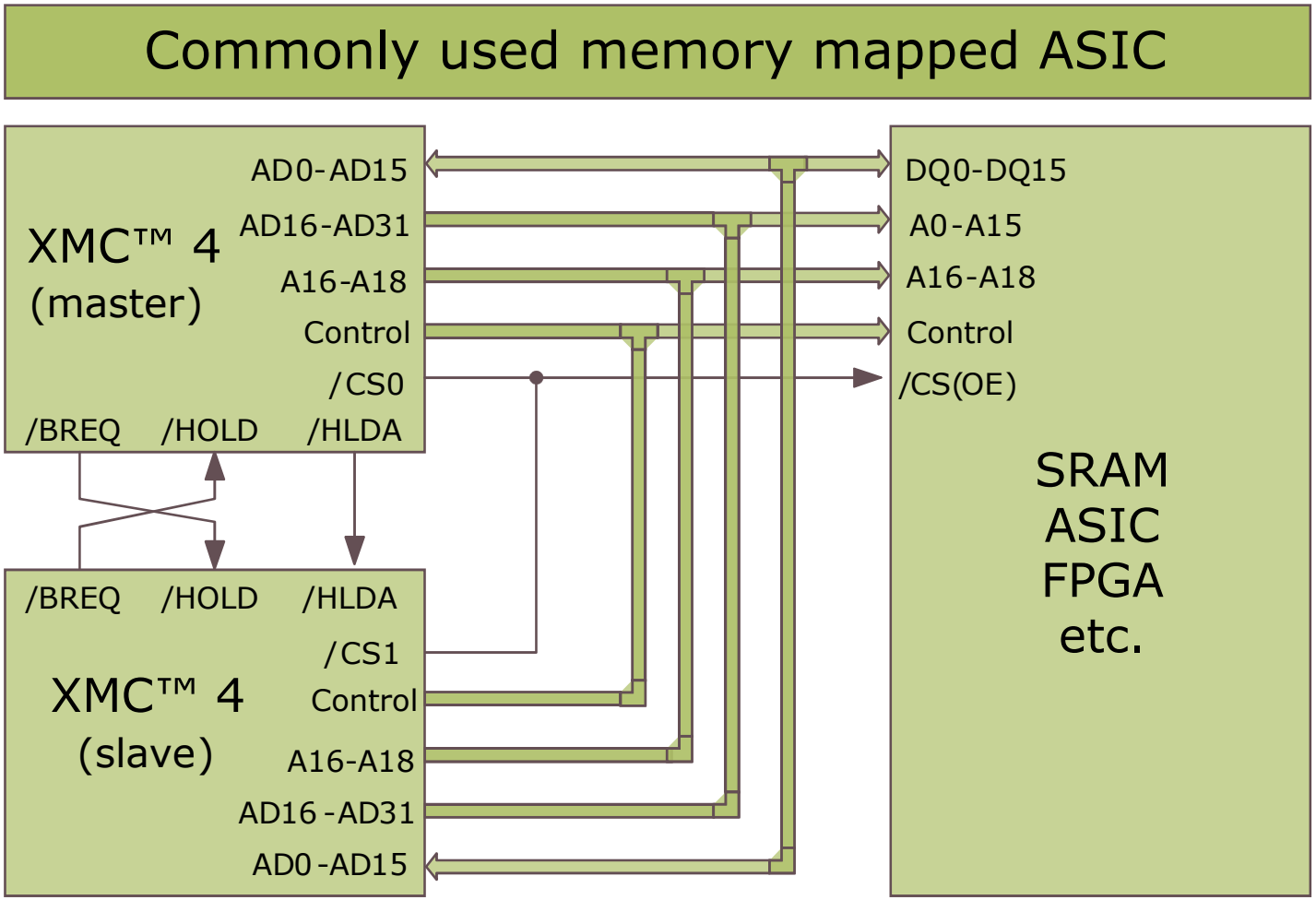
CPU can fetch code and data via EBU from external device.

- Target applications
  - Controls and PLCs
  - HMI and LCDs

Agenda

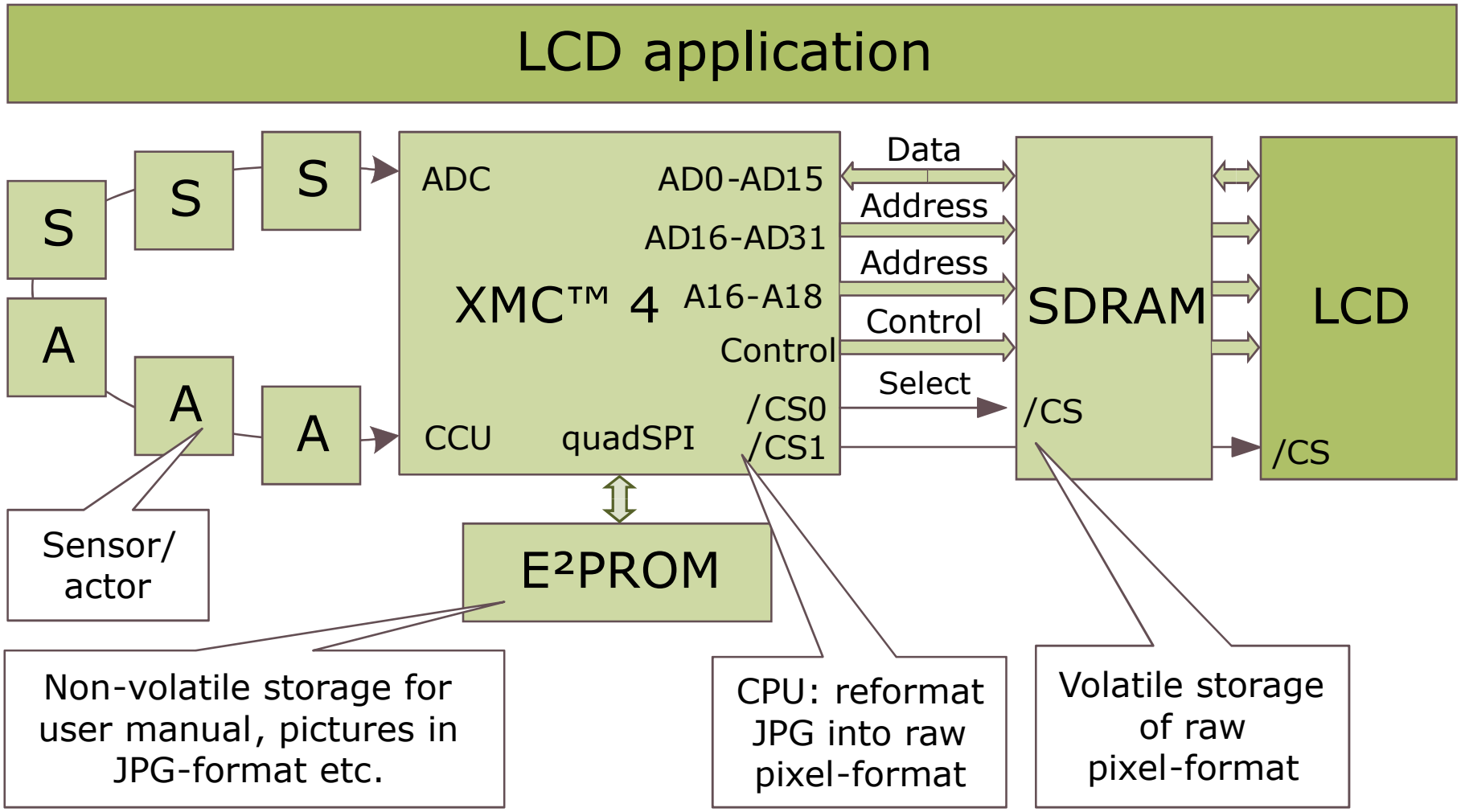
1. Overview
2. Key feature: multiple memory type access
3. Key feature: flexible bus protocol parameterization
4. Key feature: external code execution and data access
5. System integration
6. Application examples

Application example: commonly used memory between two XMC™4000



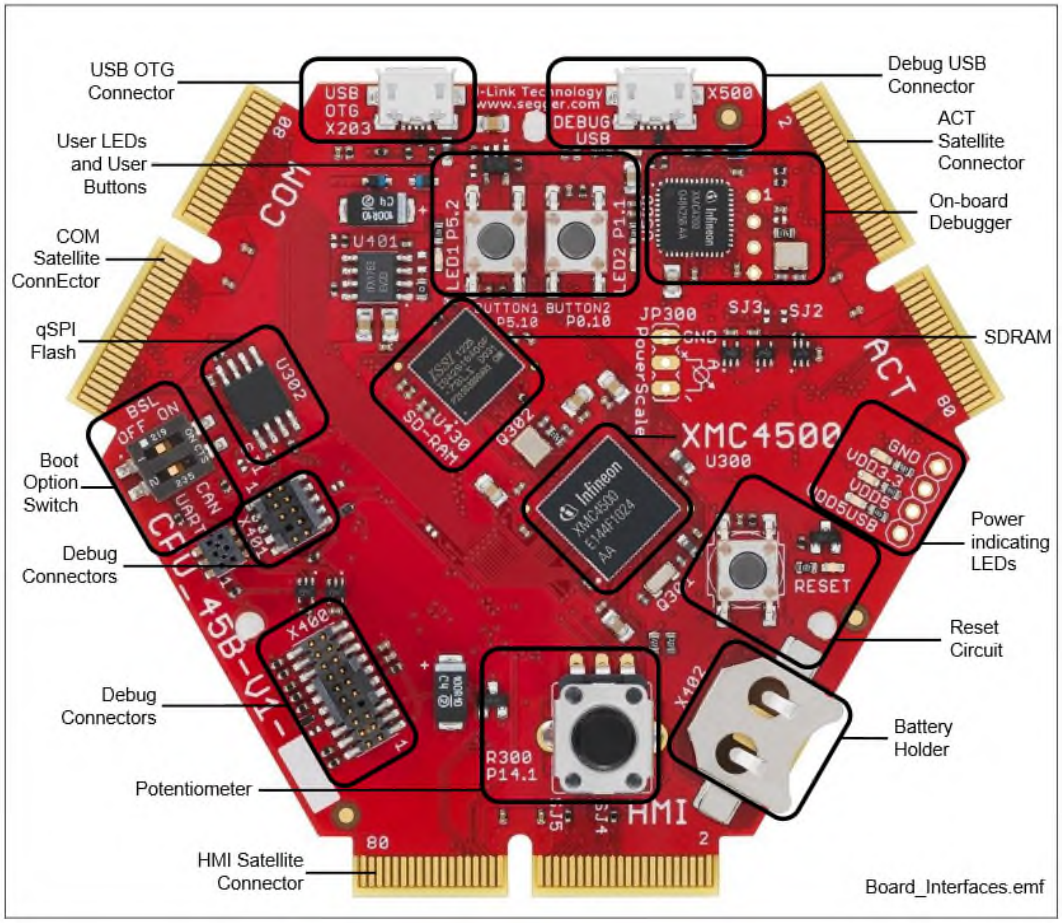
› Two XMC™4 can share an external memory (mailbox) or can commonly access an ASIC (e.g. Industrial Ethernet device) or a FPGA

Application example
LCD via EBU



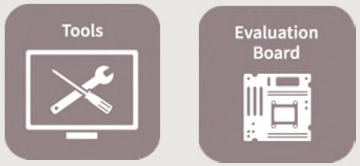
Application example
XMC™4500 application kit with SDRAM

- CPU board
  XMC™4500 SDRAM
  - SDRAM
  - EEPROM
  - Intel-style interface on COM connector



http://www.infineon.com/cms/en/product/productType.html?productType=db3a304433b8a4100133daf9cc041122

Support material

Collaterals and Brochures 	– Product Briefs – Selection Guides – Application Brochures – Presentations – Press Releases, Ads	– www.infineon.com/XMC
Technical Material 	– Application Notes – Technical Articles – Simulation Models – Datasheets, MCDS Files – PCB Design Data	– www.infineon.com/XMC – Kits and Boards – DAVE™ – Software and Tool Ecosystem
Videos 	– Technical Videos – Product Information Videos	– Infineon Media Center – XMC Mediathek
Contact 	– Forums – Product Support	– Infineon Forums – Technical Assistance Center (TAC)

Disclaimer

The information given in this training materials is given as a hint for the implementation of the Infineon Technologies component only and shall not be regarded as any description or warranty of a certain functionality, condition or quality of the Infineon Technologies component.

Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this training material.

Part of your life. Part of tomorrow.

Infineon